# AN-1144
## I2C IO Controllers 8-bit BUS

*Author: Yu-Han Sun*

*Date: September 19, 2016*

## Introduction

This app note is a corollary to another app note **AN-1090 Simple I2C IO Controllers with SLG46531V**. AN-1090 explains how to make I2C IO Controllers with separate input and output pins. However, this app note will explain how to setup an 8-bit bus controller which combines input pins with output pins. Refer to Figure 1 for the System Level View.

## Digital Input/Output and OE

To combine inputs with outputs, each pin interfacing the bus is set to 'Digital Input/Output'. Only 9 GPIOs in the SLG46531V are 'Digital Input/Output' capable and we will be using 8 of those pins: PINs #19, 18, 16, 14, 13, 7, 5, 3. Each of these pins have an OE signal that toggles the mode. Set the properties as shown in Figure 3 and setup the matrix connections as shown in Figure 2.

Each output signal is controlled by an I2C Virtual Input. OE is controlled by 2-bit LUT0. The inputs to the 2-bit LUT0 are both gnd. Therefore, if the LUT is configured as in Figure 4a, then OE will be logic 1. If the LUT is configured as in Figure 4b, then OE will be logic 0. We will be using I2C to change the LUT configuration on the fly.

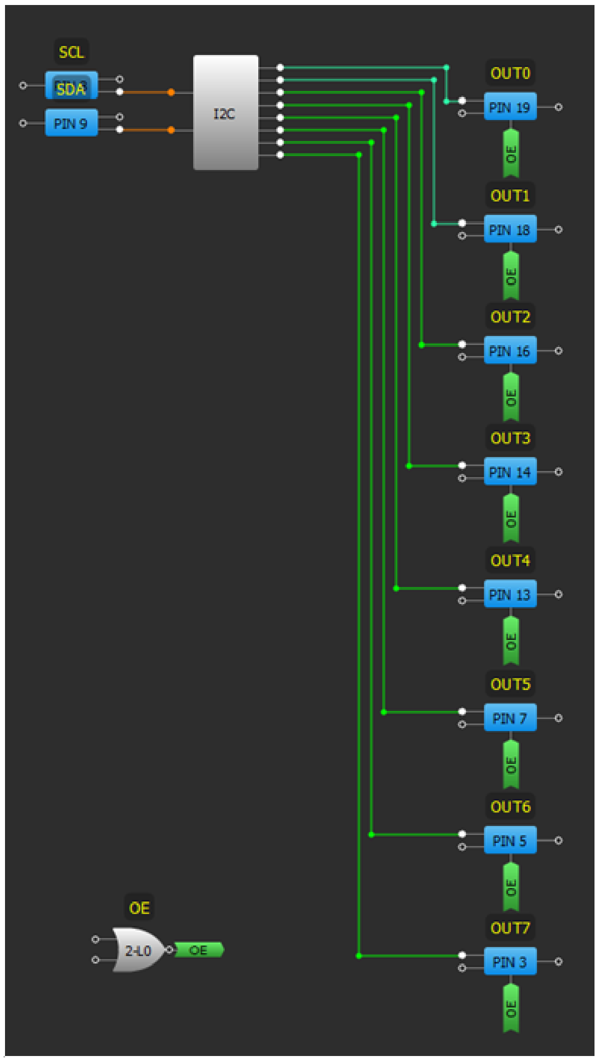


**Figure 2. GreenPAK Design**

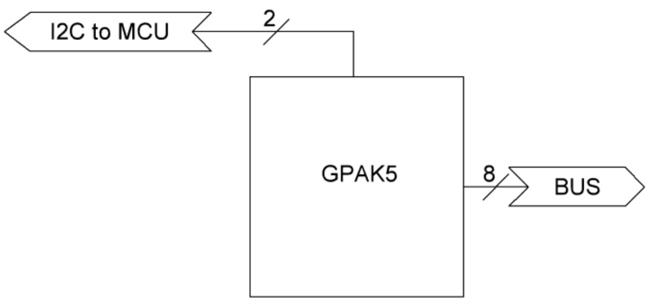
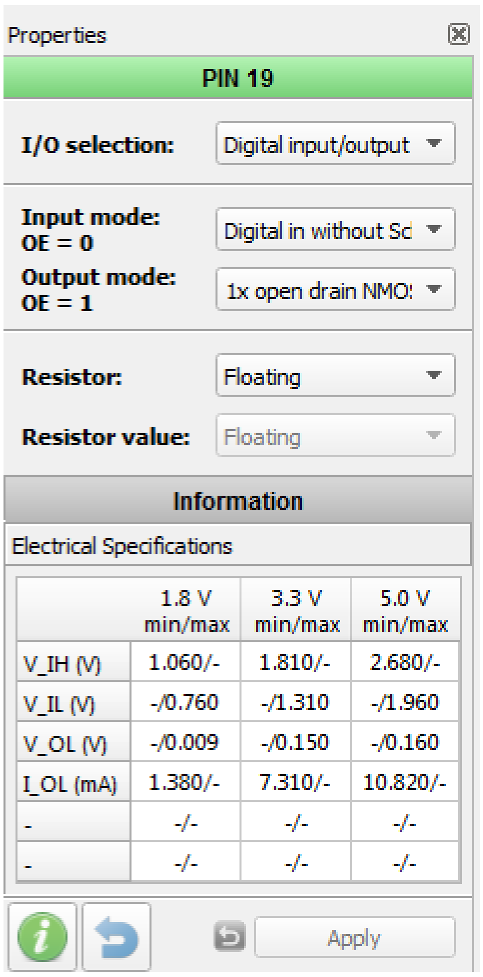


**Figure 1. System Level View**



I/O selection: Digital input/output

Input mode: OE = 0 — Digital in without Sc

Output mode: OE = 1 — 1x open drain NMO

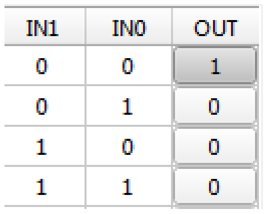
Resistor: Floating

Resistor value: Floating

Electrical Specifications

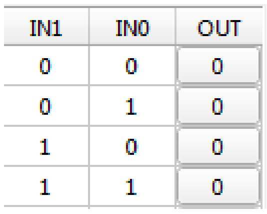
| | 1.8 V min/max | 3.3 V min/max | 5.0 V min/max |
|---|---|---|---|
| V_IH (V) | 1.060/- | 1.810/- | 2.680/- |
| V_IL (V) | -/0.760 | -/1.310 | -/1.960 |
| V_OL (V) | -/0.009 | -/0.150 | -/0.160 |
| I_OL (mA) | 1.380/- | 7.310/- | 10.820/- |
| - | -/- | -/- | -/- |
| - | -/- | -/- | -/- |

**Figure 3. PIN Configuration**



| IN1 | IN0 | OUT |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Figure 4a. OE = 1**



| IN1 | IN0 | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Figure 4b. OE =0**

## I2C Bus Write

To write the bus, the MCU must send 2 commands: first write to the I2C Virtual Inputs, then set OE = 1 by re-configuring 2-bit LUT0:

i) **W: I2C Virtual Inputs**, write to address 0xF4. Each bit corresponds to an I2C Virtual Input. The order from left to right is PINs #19, 18, 16, 14, 13, 7, 5 and 3.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0xF4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0xF4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

ii) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x8. To mask the first nibble, read the byte and change only the latter four bits.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0x96 | X | X | X | X | 1 | 0 | 0 | 0 |

## I2C Bus Read

To read from the bus, the MCU must send 2 commands: first set OE = 0 by reconfiguring 2-bit LUT0, then read from the GPIO Input Levels.

i) **W: 2-bit LUT0**, write to the second nibble of address 0x96 with the byte value 0x0. To mask the first nibble, read the byte and change only the latter four bits.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0x96 | X | X | X | X | 0 | 0 | 0 | 0 |

ii) **R: Input levels**, read from address 0xF0 and 0xF6 the input levels of PIN#3, 5, 7 and PIN#13, 14, 16, 18, 19 respectively. Then parse the data based on bit location.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0XF0 | X | X | PIN3 | X | PIN5 | X | PIN7 | X |

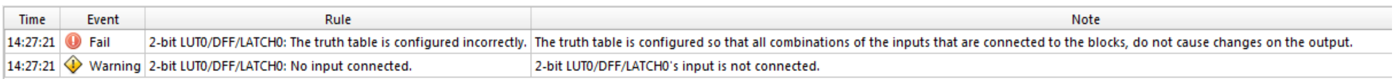
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0XF6 | X | PIN13 | PIN14 | X | PIN16 | 0 | PIN18 | PIN19 |

## Warning

The following warning can be ignored because 2-bit LUT0 inputs are intentionally left static and the truth table will be re-configured through I2C.

## Examples I2C Commands

The output of each example is shown in Figure 7 through 10, which are screenshots from the I2C Tool.



| Time | Event | Rule | Note |
|---|---|---|---|
| 14:27:21 | Fail | 2-bit LUT0/DFF/LATCH0: The truth table is configured incorrectly. | The truth table is configured so that all combinations of the inputs that are connected to the blocks, do not cause changes on the output. |
| 14:27:21 | Warning | 2-bit LUT0/DFF/LATCH0: No input connected. | 2-bit LUT0/DFF/LATCH0's input is not connected. |

Figure 5. Warnings and Rules Checker

## Emulation

Each Digital IO pin has a pull-up active-low button. Enable I2C Tools after Emulation.

Syntax**: [** is the start bit, **]** is the stop bit, and **SA** is the slave address with a r/w bit.

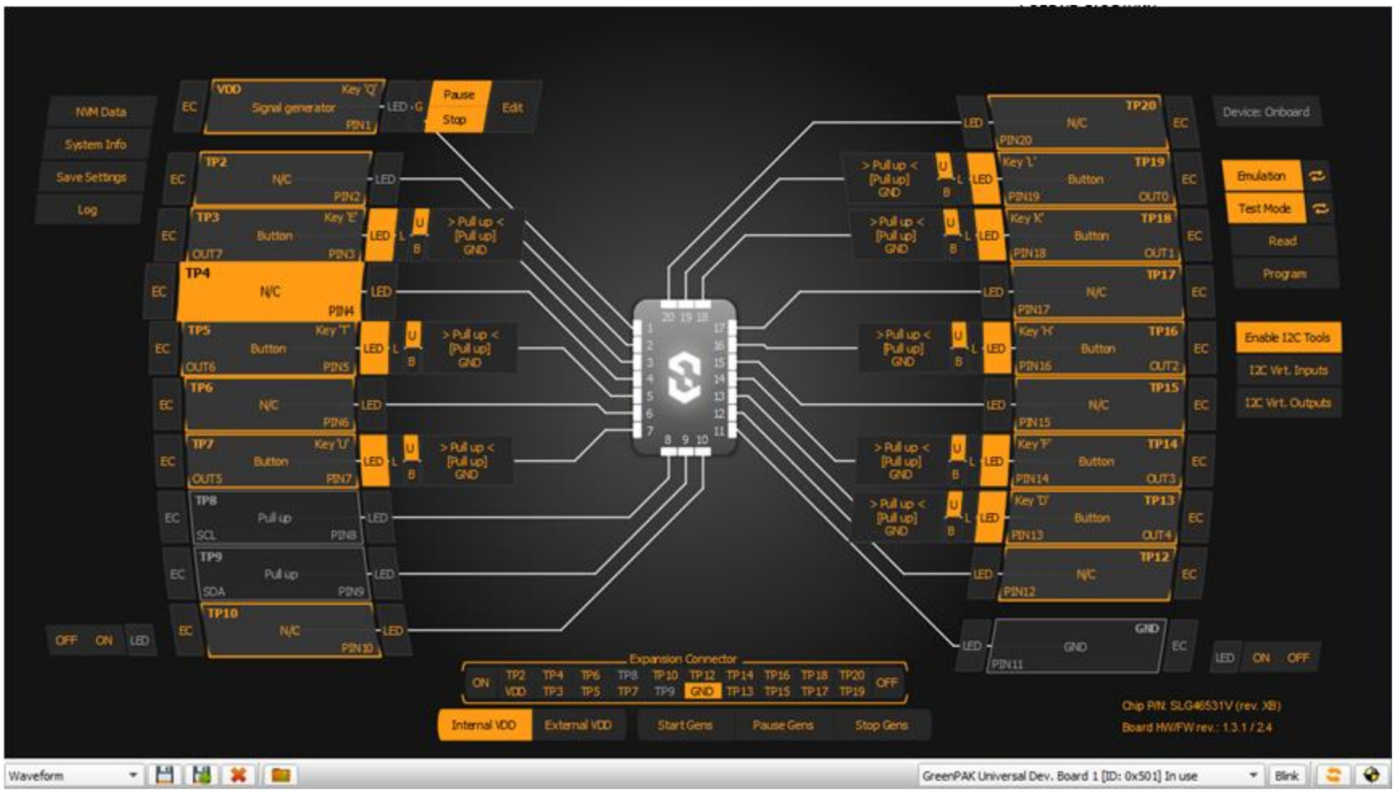


Figure 6. Emulator Configuration

i) I2C write to I2C Virtual Inputs the logic 0, 0, 0, 1, 0, 1, 1, 1.

**[ SA** 0xF4, 0xE8 **]**

ii) I2C write 2-bit LUT0 configuration to 1, 0, 0, 0:

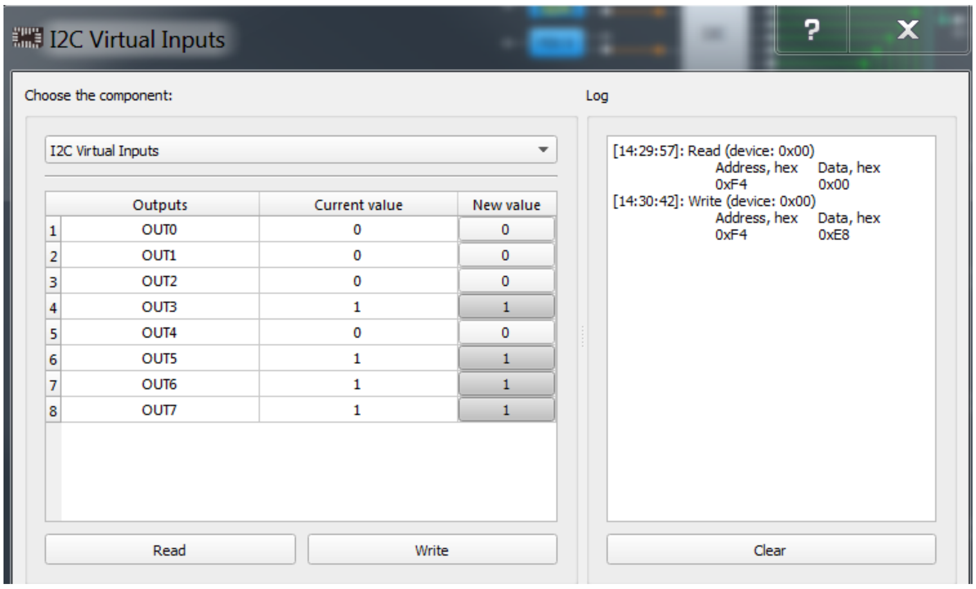
**[ SA** 0x96 0x08 **]**

iii) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

**[ SA** 0x96 0x00 **]**

iv) I2C Read the input levels from PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

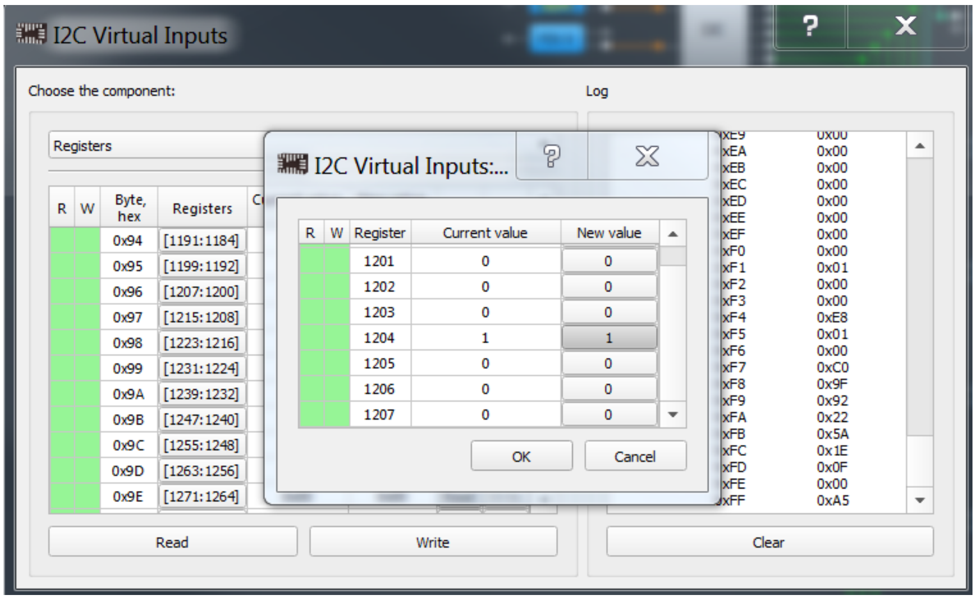
**[ SA** 0xF0 **[** 0xSA read **]**



| | Outputs | Current value | New value |
|---|---|---|---|
| 1 | OUT0 | 0 | 0 |
| 2 | OUT1 | 0 | 0 |
| 3 | OUT2 | 0 | 0 |
| 4 | OUT3 | 1 | 1 |
| 5 | OUT4 | 0 | 0 |
| 6 | OUT5 | 1 | 1 |
| 7 | OUT6 | 1 | 1 |
| 8 | OUT7 | 1 | 1 |

```
[14:29:57]: Read (device: 0x00)
            Address, hex   Data, hex
            0xF4           0x00
[14:30:42]: Write (device: 0x00)
            Address, hex   Data, hex
            0xF4           0xE8
```

Figure 7. Example i



| R | W | Byte, hex | Registers |
|---|---|---|---|
| 🟩 | 🟩 | 0x94 | [1191:1184] |
| 🟩 | 🟩 | 0x95 | [1199:1192] |
| 🟩 | 🟩 | 0x96 | [1207:1200] |
| 🟩 | 🟩 | 0x97 | [1215:1208] |
| 🟩 | 🟩 | 0x98 | [1223:1216] |
| 🟩 | 🟩 | 0x99 | [1231:1224] |
| 🟩 | 🟩 | 0x9A | [1239:1232] |
| 🟩 | 🟩 | 0x9B | [1247:1240] |
| 🟩 | 🟩 | 0x9C | [1255:1248] |
| 🟩 | 🟩 | 0x9D | [1263:1256] |
| 🟩 | 🟩 | 0x9E | [1271:1264] |

| R | W | Register | Current value | New value |
|---|---|---|---|---|
| 🟩 | 🟩 | 1201 | 0 | 0 |
| 🟩 | 🟩 | 1202 | 0 | 0 |
| 🟩 | 🟩 | 1203 | 0 | 0 |
| 🟩 | 🟩 | 1204 | 1 | 1 |
| 🟩 | 🟩 | 1205 | 0 | 0 |
| 🟩 | 🟩 | 1206 | 0 | 0 |
| 🟩 | 🟩 | 1207 | 0 | 0 |

```
xE9     0x00
xEA     0x00
xEB     0x00
xEC     0x00
xED     0x00
xEE     0x00
xEF     0x00
xF0     0x00
xF1     0x01
xF2     0x00
xF3     0x00
xF4     0xE8
xF5     0x01
xF6     0x00
xF7     0xC0
xF8     0x9F
xF9     0x92
xFA     0x22
xFB     0x5A
xFC     0x1E
xFD     0x0F
xFE     0x00
xFF     0xA5
```

Figure 8. Example ii

v) I2C write 2-bit LUT0 configuration to 0, 0, 0, 0:

**[ SA** 0x96 0x00 **]**

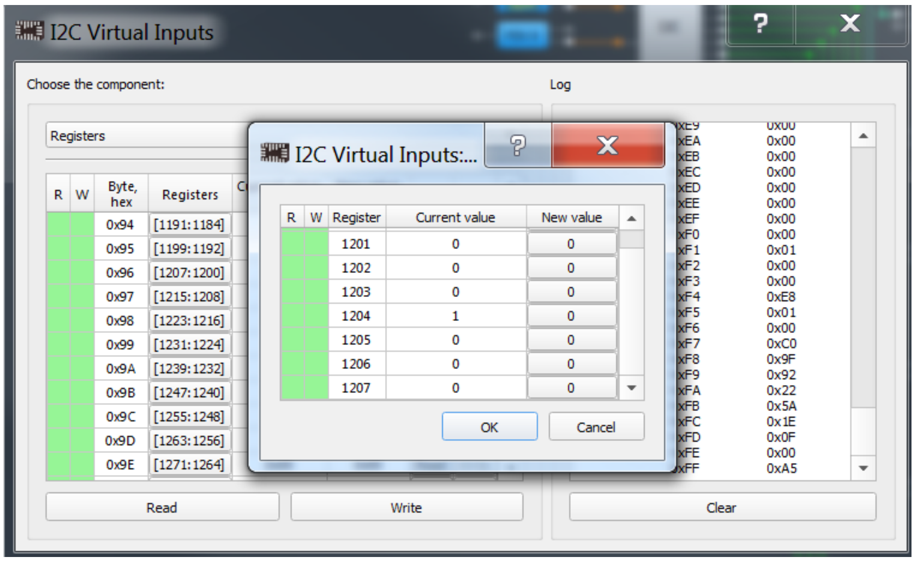
vi) I2C Read the input levels from PINs #7, 5 and 3 and also #19, 18, 16, 14 and 13:

**[ SA** 0xF0 **[** 0xSA read **]**

**[ SA** 0xF6 **[** 0xSA read **]**

## Conclusion

By the end of this app note, you should be able to make a GreenPAK Design and the I2C Commands. Unlike AN-1090, this design uses less GPIOs at the expense of more I2C commands.

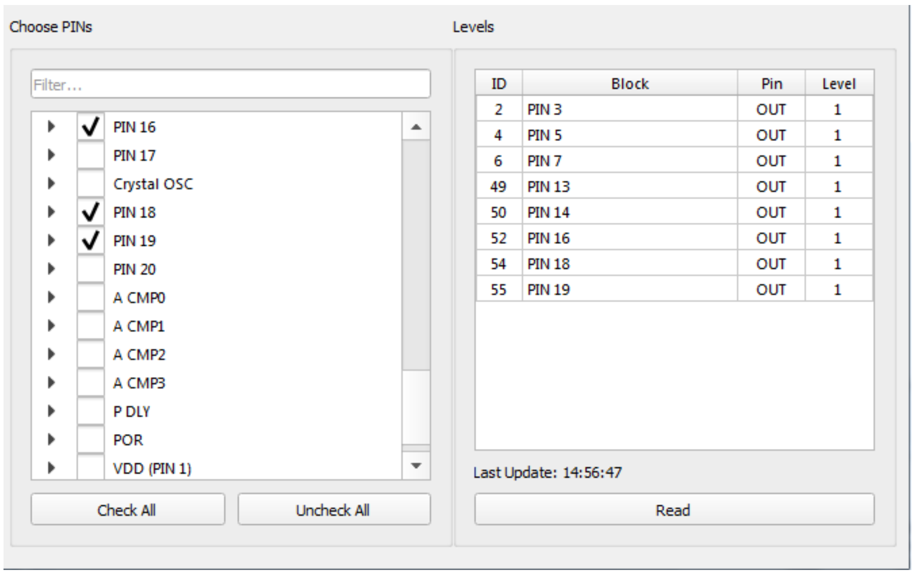


| R | W | Byte, hex | Registers |
|---|---|---|---|
| 🟩 | 🟩 | 0x94 | [1191:1184] |
| 🟩 | 🟩 | 0x95 | [1199:1192] |
| 🟩 | 🟩 | 0x96 | [1207:1200] |
| 🟩 | 🟩 | 0x97 | [1215:1208] |
| 🟩 | 🟩 | 0x98 | [1223:1216] |
| 🟩 | 🟩 | 0x99 | [1231:1224] |
| 🟩 | 🟩 | 0x9A | [1239:1232] |
| 🟩 | 🟩 | 0x9B | [1247:1240] |
| 🟩 | 🟩 | 0x9C | [1255:1248] |
| 🟩 | 🟩 | 0x9D | [1263:1256] |
| 🟩 | 🟩 | 0x9E | [1271:1264] |

| R | W | Register | Current value | New value |
|---|---|---|---|---|
| 🟩 | 🟩 | 1201 | 0 | 0 |
| 🟩 | 🟩 | 1202 | 0 | 0 |
| 🟩 | 🟩 | 1203 | 0 | 0 |
| 🟩 | 🟩 | 1204 | 1 | 0 |
| 🟩 | 🟩 | 1205 | 0 | 0 |
| 🟩 | 🟩 | 1206 | 0 | 0 |
| 🟩 | 🟩 | 1207 | 0 | 0 |

```
xE9    0x00
xEA    0x00
xEB    0x00
xEC    0x00
xED    0x00
xEE    0x00
xEF    0x00
xF0    0x00
xF1    0x01
xF2    0x00
xF3    0x00
xF4    0xE8
xF5    0x01
xF6    0x00
xF7    0xC0
xF8    0x9F
xF9    0x92
xFA    0x22
xFB    0x5A
xFC    0x1E
xFD    0x0F
xFE    0x00
xFF    0xA5
```

Figure 9. Example iii



| | |
|---|---|
| ✓ | PIN 16 |
| | PIN 17 |
| | Crystal OSC |
| ✓ | PIN 18 |
| ✓ | PIN 19 |
| | PIN 20 |
| | A CMP0 |
| | A CMP1 |
| | A CMP2 |
| | A CMP3 |
| | P DLY |
| | POR |
| | VDD (PIN 1) |

| ID | Block | Pin | Level |
|---|---|---|---|
| 2 | PIN 3 | OUT | 1 |
| 4 | PIN 5 | OUT | 1 |
| 6 | PIN 7 | OUT | 1 |
| 49 | PIN 13 | OUT | 1 |
| 50 | PIN 14 | OUT | 1 |
| 52 | PIN 16 | OUT | 1 |
| 54 | PIN 18 | OUT | 1 |
| 55 | PIN 19 | OUT | 1 |

Last Update: 14:56:47

Figure 10. Example iv