DECOUPLING DOUBLE-DENSITY™ COMPONENTS

APPLICATION NOTE AN-116

By Stanley Hronik

INTRODUCTION

Double-Density is IDT's FCT-T family of 16, 18, and 20 bit bus interface components. The family is functionally compatible with the other 16 bit families, but offers users power savings, higher speeds, and excellent guaranteed low noise operation with a choice of output drive characteristics. The components are available in a 64ma drive version for use in backplane driving where line termination exists, a balanced drive 24ma version with internal series line termination for quiet operation, and a 3.3V version for use in applications requiring the lower supply voltage.

Although IDT's Double-Density family is more forgiving than the older eight bit families, the decoupling must be properly executed to achieve optimum results. The three versions of the Double-Density components (64ma, 24ma, and 3.3V) have similar switching speeds and therefore have similar decoupling needs despite having different device parameters and output specifications. Because of this, the techniques for decoupling which are addressed herein apply uniformly across all versions of the Double-Density family.

When setting goals for decoupling a circuit, a designer should focus his attention on reducing the radiated emissions to meet the FCC limitations for the geographical area in which his circuit will be used. When this has been accomplished, the low noise levels needed to prevent cross talk and false switching will probably have been achieved. If the circuit contains low-level analog signals, additional decoupling will probably be necessary.

SELECTING THE CAPACITOR PACKAGE

The effectiveness of decoupling capacitors is often degraded by the series resistance and inductance inherent in the capacitor. The use of chip capacitors reduces the inductance due to the capacitor leads and through hole placement, making chip capacitors the optimum choice where that package style can be used. If the use of chip capacitors is not possible, the package should allow the capacitor to fit close to the board with very short lead lengths. With through hole capacitors the excess lead should be trimmed as close to the board surface as possible.

PC BOARD POWER AND GROUND PLANE

IDT's Double-Density devices are packaged in a 48- or 56-pin SSOP, TSSOP, or TVSOP, with multiple power and ground pins as shown in Figure 1. Unlike older logic families with corner Vcc and ground pins, Double-Density packages have eight ground pins and 4 Vcc pins which are equally spaced on both sides of the package. By providing multiple, short, parallel paths for current, the lead inductance is lowered, reducing the effects of simultaneous switching noise. This also reduces the effects of inductance in the board metalization by decentralizing the current path.

When laying out a circuit board for use with Double-Density, the designer should use full ground and power planes with all ground and power pins on all devices connected to the proper plane. No power or ground pins on any Double-Density device should be left floating. The board should have a large capacitor near the power entry point on the board to stabilize any power surges from the power distribution system. If the board has an effective power distribution system, decoupling Double-Density should be easier than decoupling corner Vcc and ground packages.

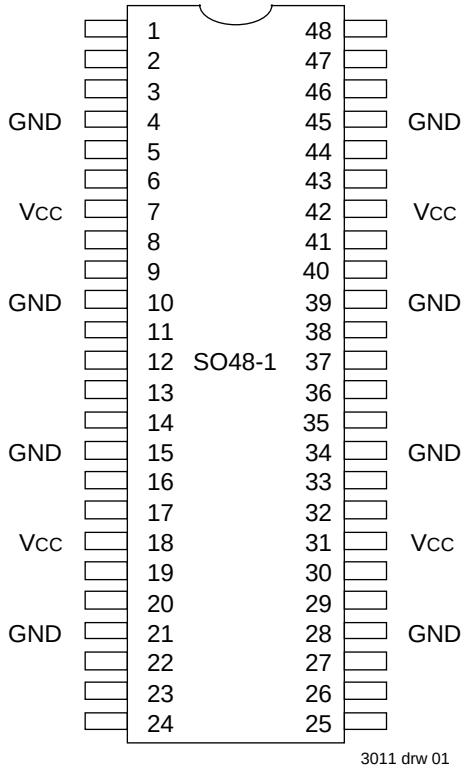

Figure 1. A 48-pin Double Density package

Capacitors have a circle of influence around them meaning that pins and components that are in the immediate proximity of the capacitor will be effectively decoupled while those components that are further away will be less affected. This characteristic is modeled in Figure 2.

While the number of capacitors per component will vary depending upon the decoupling needs of the circuit and the cost sensitivity of the design, it is suggested that the designer use at least one ceramic capacitor per IC on the board. In cost sensitive applications it may be possible to reduce the overall number of capacitors to less than one per component. In noise

sensitive circuits (e.g. A/D applications) more than one capacitor type per component may be necessary. Tantalum capacitors work well in high frequency analog situations which already include a ceramic capacitor.

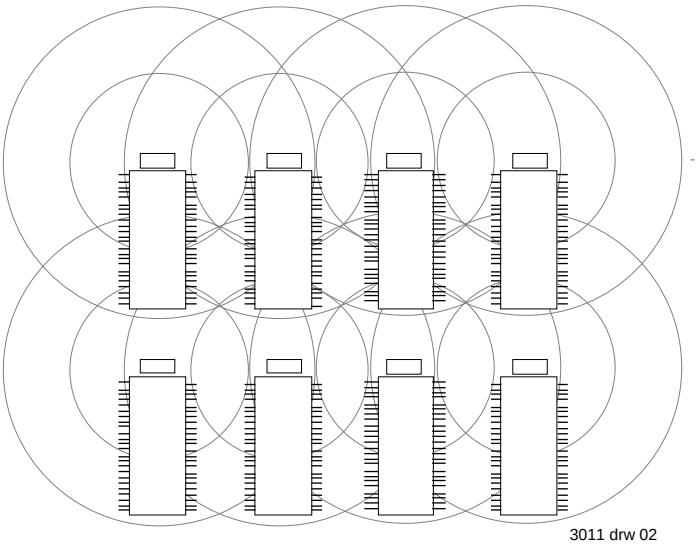

Figure 2. All capacitors have a "circle of influence" around them

CAPACITOR PLACEMENT RELATIVE TO THE COMPONENT

The decoupling capacitor should be placed as close as possible to the component being decoupled. It is not necessary to provide a separate capacitor for each Vcc on the device, but the decoupling capacitor should be solidly connected to both planes providing a short conductive path to all power and ground pins on the device. Relative to the component, the optimum placement would be on the reverse side of the board, centered over the device as shown in Figure 3.

The power and ground pins on the SSOP package that are adjacent to the device outputs will generate more switching noise than pins near the device inputs or enable pins. Since these pins are usually near the center of the package, placing the decoupling capacitor on the reverse side of the board centered over the component will provide the shortest path from the capacitor to the pins giving optimum decoupling.

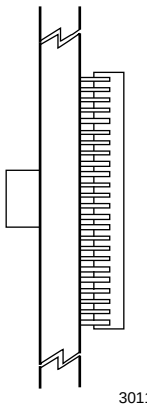

Figure 3. Capacitor placement for a board with components on both sides

If the board has components on only one side, the capacitor can be placed at either end of the device (considering the direction to the power source) with a solid connection to the power and ground planes as shown in Figure 4. This will give

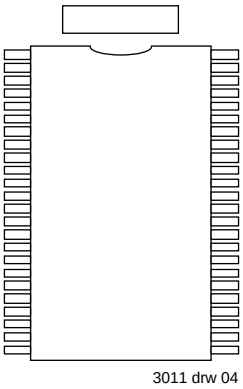

Figure 4. Capacitor macement for boards with one component side

the board designer direct access to the sides of the package to run traces and avoid placement interference.

If more than one capacitor is used, the capacitors can be placed at either end of the package or if that causes placement conflicts the capacitors can be located at adjacent corners of the package as shown in Figure 5.

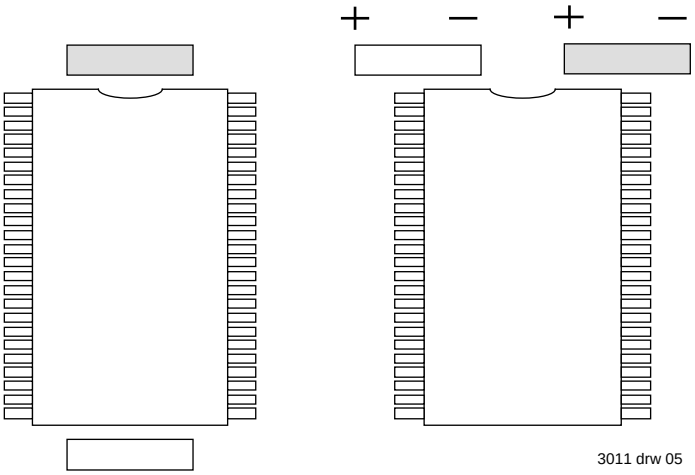

Figure 5. Placement of dual capacitors on the component side for special applications

POSITION RELATIVE TO POWER ENTRY

The decoupling capacitor should be placed between the power entry point on the board and the component that is being decoupled as is shown in Figure 6. Since the ultimate source of all charge is the power entry point, placing the capacitor between the component and the entry point positions the capacitor to receive and stabilize the voltage prior to the component. If the capacitor and component are reversed, the charge will flow directly from the entry point to the component and not pass the capacitor. This will make it easier for noise in the power system to reach the component, and for noise generated by the component to propagate into the

power system. When the capacitor is not in the path of the charge flow, the capacitor can only react to noise after it has passed into the component or power system rather than prevent it.

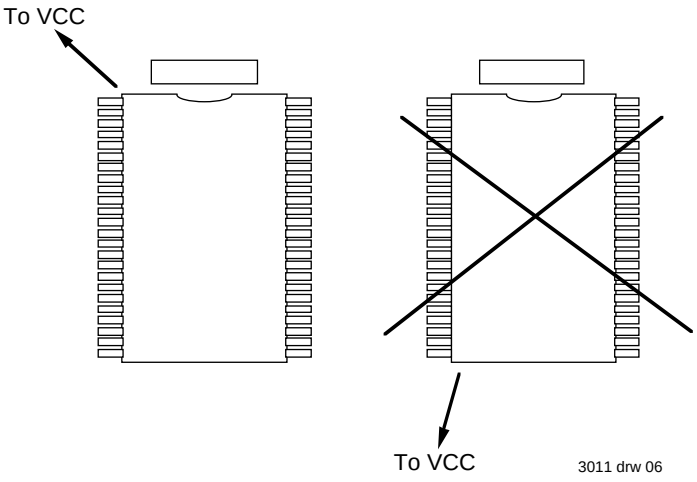

Figure 6. The decoupling capacitor works best if placed between the power source and the pin being decoupled

FREQUENCY CONSIDERATIONS

IDT's Double-Density components have very high internal switching speeds, but the lead inductance, packaging, and board placement will absorb most of the high frequency components above 120MHz before the noise can enter the power distribution system or radiate. The frequencies most likely to cause problems by reaching the power distribution system are in the 60-80MHz range (40-120MHz on a broader scale) and therefore the decoupling effort should be focused on this range.

Capacitors can be modeled as a capacitor in series with an inductor and a resistor as shown in Figure 7. With typical ceramic capacitors at low noise frequencies (<10MHz), the model can be considered as a single capacitive element with no inductance or resistance. As the noise frequency increases to levels above 50MHz the influence of the inductance and resistance increases to the point that the inductance becomes the dominating component of the capacitor's impedance. If noise issues are critical, the designer may be required to use two capacitors to cover both the high and low frequency components of the spectrum.

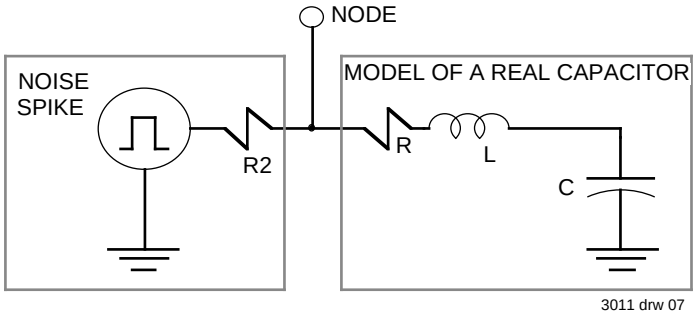

Figure 7. Model of the influence of a noise source and a decoupling capacitor on a node

Capacitors that are operating near their characteristic frequency will resonate at that frequency and provide good noise filtration with no inductive kick. Using this characteristic, designers frequently use a 0.01uf or a 0.001uf capacitor to filter out high frequency noise. The characteristic frequency of the capacitor can be obtained by contacting the capacitor manufacturer. Typically ceramic capacitors have a characteristic frequency in the 20-40MHz range. Tantalum capacitors typically work best at frequencies above 80MHz and have decreasing effectiveness at lower frequencies.

While picking capacitors at the resonant frequency of the circuit will prove beneficial to noise suppression, the selection of smaller valued capacitors will not. The value of the capacitor should always be at the resonant frequency or have a larger capacitance value. If small valued capacitors are used, it will be necessary to have good low frequency decoupling through additional larger valued capacitors located near the component.

USING CAPACITORS WITH DIFFERING INTERNAL STRUCTURES

When using capacitors of different values and different types on the same board in close proximity to one another, it is possible for the two capacitors to begin interacting with one another. With different frequency responses, the two capacitors will respond with different timings to voltage spikes with the result being an instantaneous difference in the internal voltages between the two capacitors. The two capacitors can then begin oscillating by passing charge between themselves through their characteristic series inductors as modeled in Figure 8. The end result will be a reduction in the effective decoupling that takes place and the possible addition of a noise source on the board.

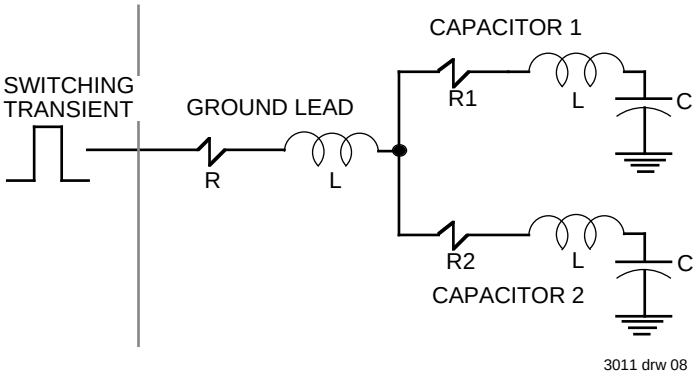

Figure 8. If using two capacitors with different characteristics, oscillations may develop between them

Additionally, two capacitors with highly different dielectric constants in close proximity on the same board may affect each other because the high dielectric constant part will dampen the high frequency resonance of the low dielectric constant capacitor and the end result will be reduced noise suppression.

To effectively handle the problem of capacitors with differing internal structures, be sure the two types are not placed in close proximity to one another as shown in Figure 9. This can be done by placing the different capacitors at opposite ends

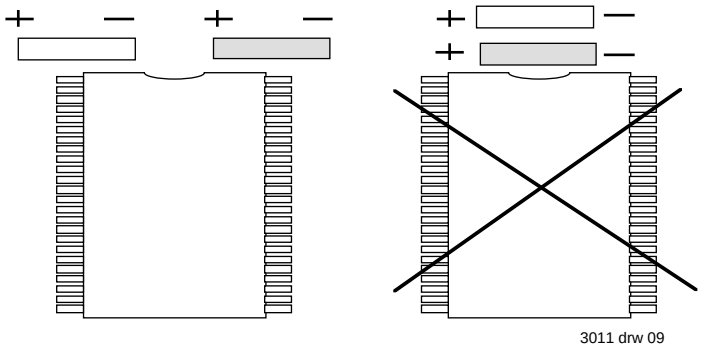

Figure 9. Exercise care when positioning two capacitors with differing frequency response in close proximity to one another

of the device or equally spaced on the back side of the board. If these choices are not feasible, the capacitors can be spaced in opposing corners of the device. The key to placement is to avoid having the Vcc pins of two capacitors adjacent or having the Gnd pins of two capacitors adjacent.

CONCLUSIONS

To properly decouple IDT's Double-Density parts do the following:

1) Select a capacitor that will meet the needs of the component. A 0.1uf ceramic is a good starting point. A 0.01uf ceramic may be better in situations which have good low frequency decoupling elsewhere on the board but are experiencing high frequency noise.

2) For best results use at least one capacitor per IC. More may be necessary in noisy situations, fewer may be possible with careful component and capacitor placement.

3) Place the capacitor as close to the component as possible. On the reverse side of the board is best. At either end of the component is also good.

4) Make sure that there is a good connection between all ground pins on the component and the capacitor. This should be in the form of a solid ground plane under the device. The same is true for the Vcc pins.

5) Place the capacitor between the component and the power entry point on the board if possible.

6) In critical situations two or more capacitors of different values may be used. In this case select a larger capacitor to provide low frequency stability and a smaller capacitor to give a series resonance to higher frequencies. Examples may be a 0.1uf or a 1uf ceramic along with a 0.001uf or a 0.01uf.

7) If capacitors of different internal structures are used, they should not be placed in close proximity to one another. Capacitors of different types that are close to one another may resonate between themselves and negate any positive effect of using two capacitors.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.