How to Enable Hot-Plug Implementing on IDT PCI Express® Switches Evaluation Boards

Application Note AN-538

Notes

By Bryan Le

Introduction

The PCI Express® architecture is designed to natively support both hot-add and hot-removed ("hot-plug") of adapters and provides a "toolbox" of mechanisms that allow different user/operator models to be supported using a self-consistent infrastructure. IDT PCIe® switches support hot-plug on all of its downstream ports. There are software and hardware elements required to support the Hot Plug environment. The major software elements include the User Interface, Hot-Plug Service, Hot Plug System Driver, and Device Driver. As for major hardware elements, Hot-Plug Controller, Card Slot Power Switching logic, Card Reset logic, Power Indicator, Attention Indicator Attention Button, and Card Present Detect Pins are included.

IDT PCIe switches utilize an external SMBus/I^{2}C-bus I/O expander connect to the master SMBus interface for hot-plug related signals associated with downstream ports as illustrated in Figure 1.

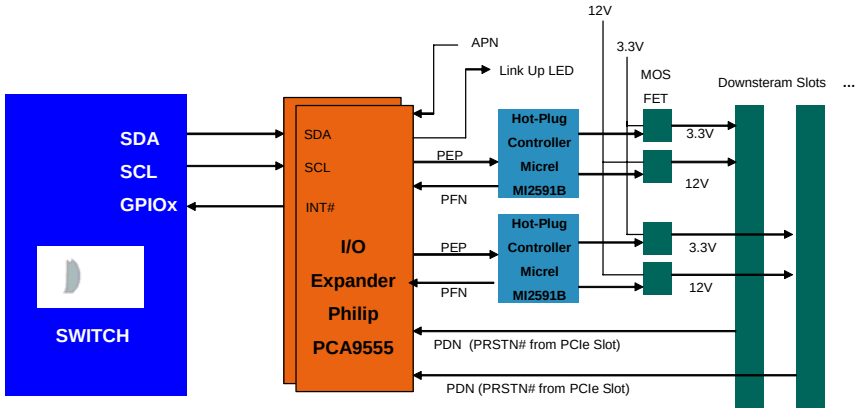

Figure 1 Hot-Plug Block Diagram

This application note describes how to prepare the EBPES24N3A evaluation board (using the PES24N3A PCIe switch) for a hot-add and hot-removed on one of its downstream ports. A similar process can be applied to the second downstream port on other IDT PCIe switches.

I/O Expander Initialization

The PES24N3A utilizes an external SMBus/I2C-bus I/O expander connected to the master SMBus interface for hot-plug related signals associated with downstream ports. These I/O expander and Hot-Plug functions are disabled in default mode. Therefore, they must be enabled and initialized prior to the bus enumeration from the root complex via a serial EEPROM. Table 1 provides the registers required to prepare the PES24N3A Port 2 for a hot-plug process. Refer to the PCIBrowser Manual on how to modify the PES24N3A registers and program an EEPROM.

Notes

Offset	Value	Description
0x00000404	0x00000008	SWCTL - Set Unlock Register
0x00000408	0x14140000	Disable MRL automatic power off
0x00000418	0x00000007	GPIOFUNC - Enable I/O Expander 0 to generate reset output for down-stream port 2
0x00002040	0x4161C010	PCIECAP - Set Slot Implement bit
0x00002054	0x0020007F	PCIESCAP - Set attention button present bit Set power control present bit Set MRL Sensor present bit Set attention indicator present bit Set power indicator present bit Set hot-plug surprise bit Set hot-plug capable bit
0x00002058	0x000001DF	Port2 PCIESCTL - Enable attention press button Enable power fault detect Enable MRL sensor change Enable presence detect Enable command complete interrupt Turn off attention indicator Turn on power indicator
0x00000434	0x00000040	Set I/O Expander 0 Address
0x00000404	0x00000000	SWCTL - Reset UnLock Register

Table 1 Hot-Plug EEPROM Image

Modifications to the EB24N3A evaluation board are listed in Table 2.

Ref Designator	Setting	Description
W13	Open	Use Hot-Plug controller to generate +12V and +3.3V to downstream Port 2
R134	Remove	Disable Hot Plug controller auto force on
R133	Install	Use Port 2 Power Good to enable hot-plug controller out-put

Table 2 Hot-Plug Setting

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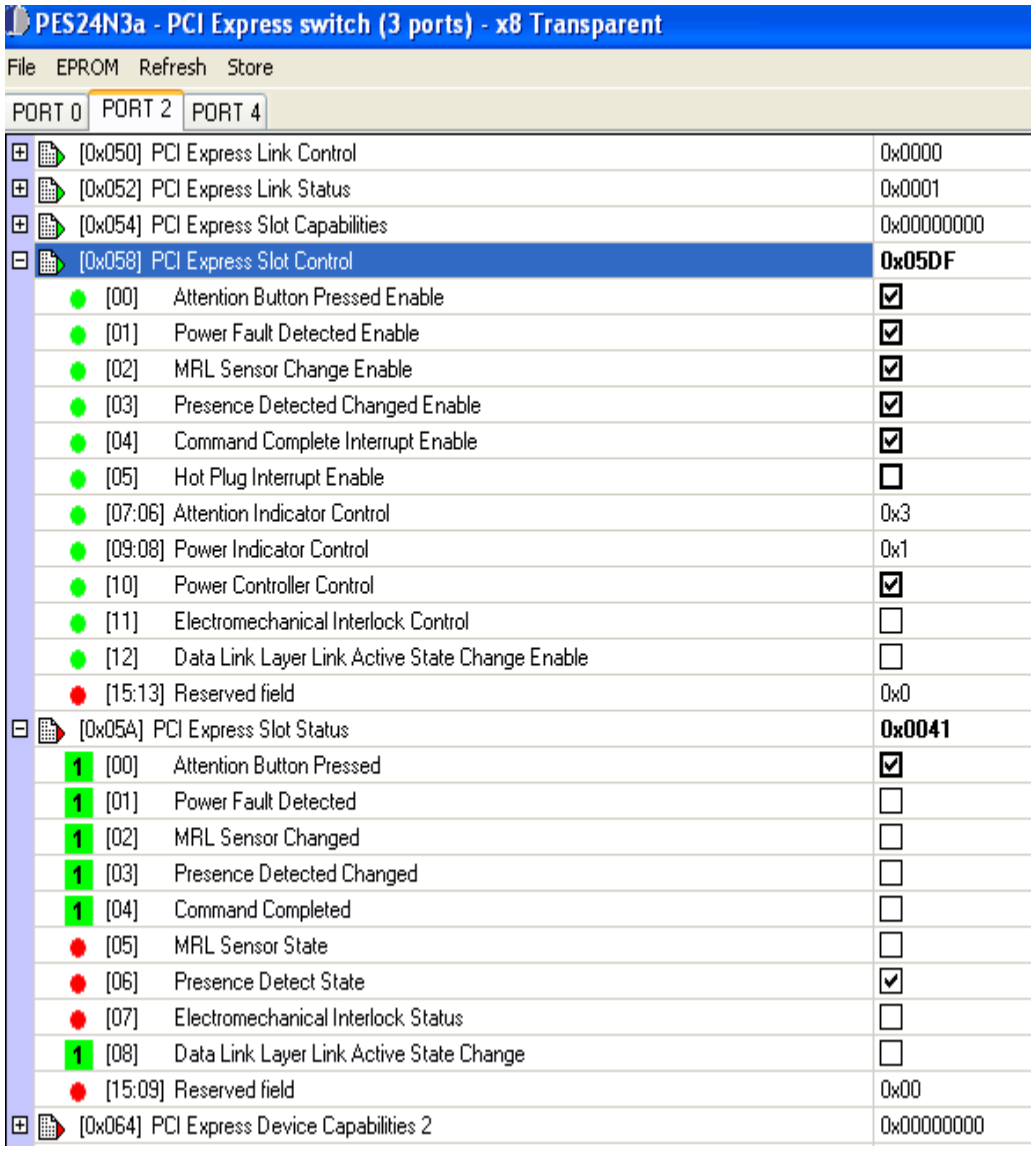

Hot-Removed and Hot-Add Procedures

It should be noted that the procedures described in the following sections assume that the Hot-Plug System Driver is responsible for configuring a newly-installed device. The PCIBrowser will be used instead of the Hot-Plug System Driver to manually turn the slot power OFF/ON and to scan for newly-installed devices via the Windows Device Manager.

Turning Slot Off

The following steps ar required to turn Off a slot that is currently On:

1. Deactivate the link
2. Assert the PERST# signal to the slot.
3. Turn off REFCLK to the slot.
4. Remove power from the slot.

Notes

Turning Slot On

The following steps are required to turn On a slot that is currently Off:

1. Apply power to the slot.
2. Turn on REFCLK to the slot.
3. Deassert the PERST signal to the slot.

Hot-Removed Procedure

A number of steps must occur to prepare the software and hardware for safe removal of the card and to control indicators that provide visual evidence of the request to remove the card. The sequence of events is as follows:

1. Initiate the card removal request by depressing the slot's "attention button x3". The PCI Express Slot Status is updated and an interrupt is generated to the root complex.
2. Use PCIBrowser to verify the Attention Button request by reading the PCI Express Slot Status register (PCIESSTS). Bit zero should be set to “1”.
3. Software commands the Hot Plug Controller to turn the slot Off. This can be achieved by using the PCIBrowser to write a "1" to the PCC bit in the PCIe Slot Control Register. The on-board hot plug control logic will assert PERST# signal, turn Off the REFCLK, and remove power from the slot.

Hot-Add Procedure

The procedure for installing a new card basically reverses the steps listed above for Hot-Removed. The steps taken to insert and enable a card are as follows:

1. Install the card.
2. Notify the hot-add service that the card has been installed by pressing the "attention button x3". The PCI Express Slot Status is updated and an interrupt is generated to the root complex.
3. Software commands the Hot Plug Controller to turn the slot On. This can be achieved by using the PCIBrowser to write a "0" to the PCC bit in the PCIe Slot Control Register. The on-board hot plug control logic will deassert PERST# signal, turn On the REFCLK, and turn power On from the slot.
4. Once link training is complete, the OS commands the Platform Configuration Routine to configure the card function by assigning the necessary resources.

Allocating Resources to Downstream Bridges

When Windows XP encounters multiple downstream bridges (as might be common when a PCIe switch is hot-plugged into a PCIe hot-plug port), all of the memory and I/O resources that are available in the upstream port are allocated to the first downstream bridge that is enumerated, which leaves no resources to assign to additional parallel downstream bridges. Functions attached to those bridges are inoperable because no resources are assigned to them. Figure 2 illustrates this situation.

Notes

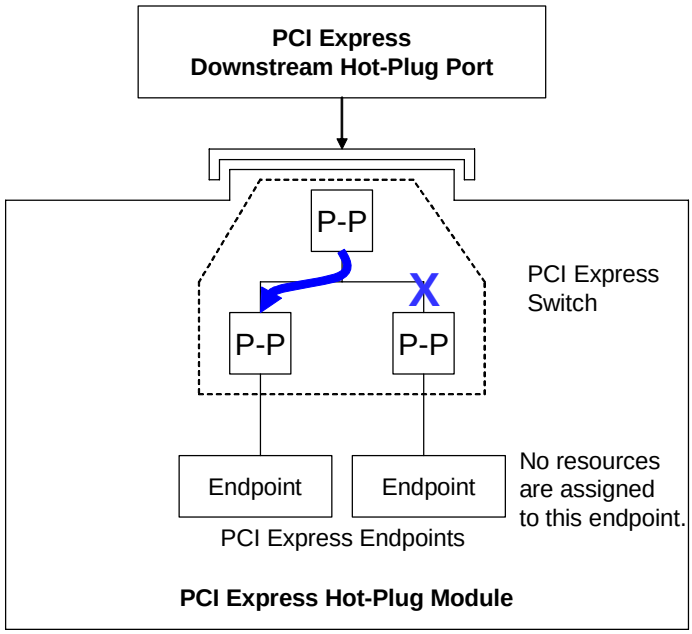

Figure 2 Bridge Resource Assignments Behind a PCIe Switch

As shown in Figure 2, all of the resources available in the upstream bridge (and elsewhere, as this is a bridge characteristic) are assigned to the downstream port on the left of the diagram. No resources are assigned to the downstream port on the right of the diagram. To prevent this, the hot-plug module must be inserted before the system is powered On. As firmware enumerates the PCIe tree, resources are assigned to all functions that are present, thus enabling the previously nonfunctional devices.

If a PCIe hot-plug module is removed after firmware has enumerated and assigned resources to the hot-plugged bridge configuration registers, Windows XP does not alter the resources that were assigned to the system board's downstream hot-plug port. But if the same module is removed and re-inserted during the same power-up session, it demonstrates the same starvation of resources as described above.

Resources

IDT 89HPES24N3A User Manual

IDT 89EBPES24N3A Evaluation Board Manual

PCI Express Browser User Manual

Firmware Support for PCI Express Hot-Plug and Windows

PCI Express Base Specification Revision 1.1

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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