

APPLICATION NOTE

From SPICE Netlist to Allegro Design Sub-Circuit

Introduction

Intersil provides a SPICE model for all our new precision Opamps. The SPICE model netlist is included in the data sheet, along with simulation vs characterization curves. Refer to <u>AN1556</u> for more details about making SPICE models.

This application note will walk the user through the process of taking the netlist from the data sheet and creating a sub-circuit to drop into a Cadence Allegro Design simulator.

Copying the SPICE Netlist

Download the Intersil data sheet from the web. The data sheet will be in .pdf format. Open the .pdf document and right click to enable the select tool, if it is not already selected (Figure 1). This will enable you to then copy and paste the entire list into Notepad.

ISL28114, ISL28214, ISL28414

		R_R11 R_R12	16 V++ 1 TC=0,0 V- 16 1 TC=0,0	
f=125Hz * SR = 2.5V/us, GBWP {	🗸 📐 Select Tool		¹ 2nd Gair G G3	1 Stage V++ VG 16 VMID 24.893e-3
short ckt I limit *Copyright 2009 by Inte *Refer to data sheet "LI	⁽¹⁾ <u>H</u> and Tool ⁽¹⁾ Marquee <u>Z</u> oom		G_G4 V_V5 V_V6	V- VG 18 VMID 24.893e-3 19 VG .604 VG 20 .604
"this model indicates yo "terms and provisions in	📀 Previous <u>V</u> iew	Alt+Left Arrow	D_D5 D_D6	19 V++ DX V 20 DX
* Connections:	<u>R</u> otate Clockwise	Shift+Ctrl+Plus	R_R13 R_R14	VG V++ 636.658e3 TC=0,0 V- VG 636.658e3 TC=0,0
:	🖶 Print	Ctrl+P	C_C2 C_C3	VG V++ 2E-09 TC=0.0 V VG 2E-09 TC=0.0



Scroll towards the end of the datasheet and find the SPICE netlist (Figure 3) and copy it into notepad. Name the file with the extension **.MOD** (not case sensitive) as shown in Figure 2. This file needs to be saved in a common directory with all the other SPICE files for this design.



FIGURE 2. SAVING NOTE PAD FILE AS . MOD

ISL28114, ISL28	3214, ISL28414
* source ISL28114_SPICEmodel	R_R11 16 V++ 1 TC=0,0
* Revision C, LaFontaine October 7th 2009 * Model for Noise, supply currents, CMRR 72dB 1-80kHz AVOL 90dB f=125Hz	R_R12 V-16 1 TC-0,0
SR = 2.5V/us, GBWP 5MHz, 2nd pole 6MHz Output voltage clamp and	"2nd Gain Stage G G3 V++ VG 16 VMID 24.893e-3
short ckt I limit "Copyright 2009 by Intersil Corporation	G_G4 V-VG 16 VMID 24.893e-3
"Refer to data sheet "LICENSE STATEMENT" Use of	V_V5 19 VG .604
"this model indicates your acceptance with the	V_V6 VG 20.604
"terms and provisions in the License Statement.	D_D5 19 V++ DX D_D6 V-20 DX
* Connections: +input	R R13 VG V++ 636.658e3 TC=0.0
- Input	R R14 V-VG 636.658e3 TC=0,0
+Vsupply	C C2 VG V++ 2E-09 TC=0,0
-Vsupply	C_C3 V-VG 2E-09 TC+0,0
* j j output	
·	"Mid supply Ref
.subckt ISL28114subckt VIn+ VIn- V+ V- VOUT	E_E4 VMID V- V++ V- 0.5
* source ISL28114_DS rev1	E_E2 V++0V+01
-	E_E3 V=0V-01
"Voltage Nolse E En VIN+ EN 28 0 1	LISY V+ V- DC 300e-6
D D13 29 28 DN	"Common Mode Gain Stage with Zero
V V9 29 0.00035	G G5 V++ VC VCM VMID 2.5118E-10
R_R21 28 0 500E3 TC=0,0	G G6 V-VC VCM VMID 2.5118E-10
	E EOS 1 EN VC VMID 1
"Input Stage	R R15 VC 21 1e6 TC=0.0
M_M14 3155 NCHANNELMOSFET	R_R16 22 VC 1e6 TC=0,0
M_M15 4 VIN-66 NCHANNELMOSFET	R_R22 EN VCM 5e11 TC=0,0
M_M16 11 VIN- 9 9 PMOSISIL	R R23 VCM VIN- 5e11 TC=0,0
M_M17 12 1 10 10 PMOSISIL	L_L1 21 V++ 1.9895
1_11 7 V- DC 5e-3	L_L2 22 V- 1.9895
I_12 V++ 8 DC 5e-3 I IOS VIN- 1 DC 25e-12	•
G G1A V++ 14 4 3 1404	"Pole Satge
G G2A V-14 11 12 1404	G_G7 V++ 23 VG VMID 376.98e-6
V_V1 V++ 2 1e-6	G_G8 V-23 VG VMID 376.98e-6 R R17 23 V++ 2652.66 TC-0.0
V_V2 13 V-1e-6	R R18 V-23 2652.66 TC=0.0
R_R1 32 1.0004 TC=0,0	C_C4 23 V++ 10e-12 TC=0,0
R_R2 4 2 1.0004 TC=0,0	C C5 V-23 10e-12 TC-0.0
R_R3 57 10 TC=0,0	
R R4 7 6 10 TC=0,0	"Output Stage with Correction Current Sources
R_R5 98 10 TC=0,0	G_G9 25 V- VOUT 23 0.02
R_R6 8 10 10 TC=0,0 R R7 13 11 1 TC=0.0	G_G10 27 V-23 VOUT 0.02
R R8 1312 1 TC-0.0	G_G11 VOUT V++ V++ 23 0.02
R RA1 14 V++ 1 TC=0.0	G_G12 V-VOUT 23 V-0.02
R RA2 V-14 1 TC=0.0	V_V7 24 VOUT.08
C CIND# VIN-EN 1.02E-12 TC=0.0	V_V8 VOUT 25.08 D D7 23.24 DX
C Cin1 V-EN 1.26e-12 TC-0.0	D_D8 2523 DX
C Cin2 V-VIN- 1.26e-12 TC=0,0	D D9 V++ 26 DX
.=	D D10 V++ 27 DX
"1st Gain Stage	D D11 V-25 DY
G_G1 V++ 16 15 VMD 334.753e-3	D_D12 V-27 DY
G_G2 V- 16 15 VMID 334.753e-3	R_R19 VOUT V++ 50 TC=0,0
V_V3 17 16.61	R_R20 V-VOUT 50 TC-0,0
V_V4 16 18.61	.model pmosisil pmos (kp=16e-3 vto=0.6)
D_D1 15 VMID DX	.model NCHANNELMOSFET nmos (kp=3e-3 vto=0.6)
D_D2 VMID 15 DX	.model DN D(KF=6.69e-9 AF=1)
D_D3 17 V++ DX D_D4 V-18 DX	.MODEL DX D(IS=1E-12 Rs=0.1)
R_R9 1514 100 TC=0,0	MODEL DY D(IS=1E-15 BV=50 Rs=1)
R R10 15 VMID 1e9 TC=0,0	.ends ISL28114subckt

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FIGURE 3. NETLIST FROM DATA SHEET

FIGURE 21. SPICE NET LIST

Model Editor

Open the Cadence model editor via the path shown in Figure 4 (Cadence SPB 16.2\AMS Simulator\Simulation Accessories \setminus Model Editor)

Microsoft Office		G	AMS Simulator	►	G	Simulation Accessories	1	Magnetic Parts Editor
Oracle 8i		Ē	PCB Editor Utilities				(III)	Model Editor
Oracle - ORANT9I	,	õ	Tutorials					Simulation Manager
Oracle Installation Products	,	õ	What's New in Release 16.2		ŕ		1	Stimulus Editor
Reflection Web	,	Ē	Cadence Help					
Report2Web PageMart Viewer	•		Design Entry CIS					
Startup	•	R	Design Entry HDL					
WinZip	,	*	Design Entry HDL Rules Checker					
Adobe Reader 9		2	Layout Plus					
🧉 Internet Explorer		1	Layout Plus SmartRoute Calibrate					
Initiator Clear Cache		m	Library Explorer					
JInitiator Control Panel 1.1.8.19		ė	License Client Configuration Utility					
Microsoft Office Communicator 2007 R2		2	Model Integrity					
Outlook Express			Package Designer					
Remote Assistance		×	PCB Editor					
Windows Media Player		6	PCB Router					
🔏 Windows Messenger		×	PCB SI					
Windows Movie Maker		×	Physical Viewer					
Cisco Systems VPN Client	,	8	Project Manager					
Dell ControlPoint	•		README CCR					
m Mathcad	•	ing National	SigXplorer					
noxio Creator DE	•		SIP					
2) Using Intersil WiFi		2	SiP Digital Architect					
Adobe FrameMaker 9	,	Z	System Architect					
Cadence SPB 16.2	•	20	Uninstall Cadence SPB 16.2					

FIGURE 4. PATH TO CADENCE MODEL EDITOR

Note: This document is written using the SPB16.2 software. The look and feel may change with different revisions of the Cadence software, but the procedure will be the same.



After selecting the Model Editor, the screen in Figure 5 will open up. Select Capture and click DONE.



FIGURE 5. SELECT DESIGN ENTRY TOOL

Click on File in the tool bar and select New. Figure 6 will appear.

👑 Untitled1.lib - AMS Model Editor	- 🗆 ×
File Edit View Model Plot Tools Window Help	cādence
SPELA 🛃 XOB QQAQ 🖬 XM 250000	
Models List X	
Model Name Type Modifier	

FIGURE 6. BEGINNING OF NEW MODEL

Click on Model in the tool bar and select Import. Then browse to the folder where you put the .MOD file. Figure 7 will appear. Select the desired .MOD file and click Open.



FIGURE 7. SELECT .MOD NETLIST

This will load the netlist into the Model editor tool as shown in Figure 8.

File Edit View Model Plot Too	ls Window Help	cādence	_ /# ×
🗅 🗁 🖃 🛆 尾	X06 QQAQ 0 X1 20	M	
ndels List Xi Audel Hame Type Noc SL2811494.but SLBCXT	<pre>* source 19120114_SPICEmodel * Bevision C, LaFontaine October 7th 1009 * Model Tor Noise, supply currents, CREW 72dB 1=00kI * 1588 * SV/ss, GBUP SHIE, 2nd pole 6HIE Output vole * SR * SV/ss, GBUP SHIE, 2nd pole 6HIE Output vole * Output 2009 Intersil Corporation * Parter data abact "LICENSE SITIEMENT" Use of * the smodel indicates your acceptance with the * commetions in the License Statement. * commetion: *input * - input * - veuply * output * DIE 28 NN V_V9 28 0.00005 R_PA124 0 Statement * Volcage Noise E_PA VIN* FN 28 0 1 D_P13 29 28 NN V_V9 28 0.00005 R_PA124 0 Statement * Input Statement * Input Statement * Input Statement * Input Statement * Youtput * Statement * Youtput * Statement * Youtput * </pre>		
	M_M14 3 1 5 5 NCHANNELHOSFET M_M15 4 VIN- 6 6 NCHANNELHOSFET		

FIGURE 8. NETLIST LOADED INTO MODEL EDITOR

Click on File in the tool bar and select Save As. Then type the part name as the file name in Figure 9 and click Save. The file with the complete netlist is now saved as a .lib library file.

Save As				? ×
Save in	SPICE Mode	l Folder	💽 G 👂 🖻 🖽	-
My Recent Documents Desktop My Documents	☐ I5L28114.lib			
My Computer: NBK8QJBPH1	File name:	ISL28114.IIb		Save
My Network Places	File name: Save as type:	Model Library Files (*.lib)		Cancel

FIGURE 9. FILE SAVED AS .lib

Click on File in the tool bar and select Export to Capture Part Library. The Input Model Library path and the Output Part Library path will automatically be loaded as shown in Figure 10.

Create Parts for Library	×
Enter Input Model Library:	
ppnotes\AN1613\SPICE Model Folder\ISL28114.lib Browse	1
	-
Enter Output Part Library:	
pnotes\AN1613\SPICE Model Folder\ISL28114.olb Browse	1
	-
OK Cancel Help	

FIGURE 10. LIBRARY CREATION

Verify that the files paths are the same with the only difference being the .lib and .olb extensions.



Click OK and verify no Error messages or Warning messages as shown in Figure 11. Click OK.



FIGURE 11. SCHEMATIC TO CAPTURE TRANSLATOR CHECK

Click on File in the tool bar and select Import Wizard [Capture]. Like before, both path names will load automatically and should have the same file paths with the only difference being the .lib and .olb extensions as shown in Figure 12.



FIGURE 12. ASSOCIATE SYMBOL WITH SPICE MODEL

Click Next and the screen shown in Figure 13 will appear. This is the screen in which we will associate the pins of our SPICE model to the pins of the sub-circuit model. The symbol shown is a generic 5 pin device. We want our Opamp symbol to look like an Opamp. To do this click on the Replace Symbol button and select from the list of symbols provided with the Cadence program. This list is located at the following location on your C drive. C:\Cadence\SPB.16.2\tools\capture\libary\OPAmp.olb



FIGURE 13. REPLACE GENERIC SYMBOL

If the location of your Cadence software was loaded in a different location, then search for Cadence \SPB.

When selecting your symbol, all that matters is the pin count. The numbers assigned to the symbol pins can be changed later. Just scroll through the list to find a symbol that matches a desired pinout and pin count of your device. In this example, we selected the TLC2201. Click Next.

Model Import Wizard : Select Matching				
r 10 Andreas and 10 Andreas and 10	Select library to pick matching symbols : [C:\Cadence\SPB_16.2\tools\capture\library\OF	PAmp.olb	.	
	Model : ISL28114SUBCKT		Symbol : TLC2201	
	Matching Symbols TLC2201 LMC6492 LMC6492 LM358/SO CA3401 EL2540C-W EL244C-N L2242/SO LM127O LM675 LT1017/SOL MAX430 MAX430			
View Model Text	< Back	Ne	xt > Cancel Help	

FIGURE 14. ASSOCIATE OP AMP SYMBOL WITH MODEL

Then click on the row under the Symbol Pin column to activate pull down menu box under the symbol column. Now pick the associated pin to match the Model Terminal function in the model terminal column. As shown in Figure 15.



FIGURE 15. DEFINE PINS OF SYMBOL TO PINS OF MODEL

Repeat for all Model Terminal pins as shown in Figure 16.



FIGURE 16. ALL PINS ASSOCIATED TO SYMBOL



Click Save Symbol, and Figure 17 will appear. Verify no Error messages or Warning messages appear. Click OK and then close the Model Editor.

Model Import Wizard : H:\AMS Files\1 Precision and MicroPower Amplifiers\ 🗙				
Log File Error File				
STATUS: PSpice Model Import Wizard for "Capture" (16.2.0.s003) STATUS: INFD: LBd driven flow INFD: Input File: H:VAMS Files\1 Precision and MicroPower Amplifiers\Appnotes\AN1613\SPICE INFD: Dutput File: H:VAMS Files\1 Precision and MicroPower Amplifiers\Appnotes\AN1613\SPICE STATUS: STATUS: Identifying matching symbols automaticallystarted at Tuesday, November 09, 2010 17:+ STATUS: INFD: Symbol "ISL28114SUBCKT" already exists for model "ISL28114SUBCKT". STATUS: STATUS: STATUS: STATUS: STATUS: Completed identifying matching symbols automaticallyat Tuesday, November 09, 2010 STATUS: INFD: Symbol "ISL28114SUBCKT" updated for model "ISL28114SUBCKT". STATUS: 0 Error messages, 0 Warning messages				
OK				

FIGURE 17. MODEL IMPORT WIZARD CHECK

Using the New Sub-Circuit to Run Simulations

Open the Cadence Software. Figure 18 shows the path to select the Design Entry CIS.



FIGURE 18. PATH TO DESIGN ENTRY CIS

Figure 19 shows the Cadence Product Choices. Select Allegro Design Entry CIS and Click OK.

Please select the suite from which to check out the OrCAD Captu	ire feature:
Allegro Design Entry CIS Allegro PCB Design CIS L Allegro PCB Librarian XL Allegro PCB Design CIS XL	OK Cancel
Use as default	

FIGURE 19. CADENCE PRODUCT CHOICES

Click on File in the tool bar and select New, and then Project. The screen shown in Figure 20 will appear. Type in the name of the project and select Analog of Mixed A/D button. Browse to where you saved the Netlist in the common directory (you must have all the files located in the same directory) and click OK.

New Project	×
Name ISL28114_AN1613	OK Cancel
Create a New Project Using Analog or Mixed A/D C PC Board Wizard Programmable Logic Wizard C Schematic	Help Tip for New Users Create a new Analog or Mixed A/D project. The new project may be blank or copied from an existing template.
Location H:\AMS Files\1 Precision and MicroPower Amplifi	ers\PSPICE Browse

FIGURE 20. SCREEN TO SETUP NEW PROJECT

The screen shown in Figure 21 will appear. The user can select to base their new project on an existing project or start a new one. Selecting to base upon an existing project will carry over the existing project with all the simulation profiles and schematics. This can be a real time saver if the new project is very similar to an old project. In this example, we will chose to create a new project.

Create PSpice Project	×
C Create based upon an existing project	ОК
H:\AMS Files\1 Precision and MicroPower Amplifiers\PSPICE model	Browse
Create a blank project	Cancel
·· Create a brank project	Help

FIGURE 21. CREATING A NEW PROJECT OPTIONS



Click OK, and the screen in Figure 22 will appear. Click on the SCHEMATIC1 to open the Page tab and then Click on the page tab to open the Schematic1 page. This is where the new sub-circuit will be placed to run the simulations.

👪 Allegro Design Entry CIS		
File Edit View Tools Place Macro PSp	ice Accessories Options Window Help	
	୬ ୧ ୦ ୮ ୩ ୩ ୩ ୩	
		1 ==
15120114 PAGE1		
📑 H: VAMS Files V1 Pre 🗕 🗆 🗙	/- (SCHEMATIC1 : PAGE1)	- 🗆 X
Analog or Mixed A/D		
File 4. Hierarchy		::: -
E- Design Resources		1111
🖃 🔛 .\isi28114_an1613.dsn		
C SCHEMATICI		
PAGE1		
Library		
Cutputs		1111
F - PSpice Resources		
	•	1111
		1111
		1111
		1000
	•	
		1.1.1
	JJ	· · · ·
	4	▶ //.

FIGURE 22. SIMULATION SCHEMATIC PAGE

Before we can place the new sub-circuit model and run a simulation, we need to set-up the simulation profile and add the library. Click on PSpice in the tool bar and select New Simulation Profile. Figure 23 will appear. Then type in any name that will help you keep track of the different simulations. Then click Create and Figure 24 will appear.

New Simulation	×
Name:	Create
AC Analysis	Ciodio
	Cancel
Inherit From:	
none 💌 🛄	
Root Schematic: SCHEMATIC1	

FIGURE 23. NAMING SIMULATION PROFILE

Click the Configuration Files tab. Then click on Library in the Category field (highlighted in blue). Browse to where to saved the Library file. Then click the Add to Design button. The Simulation Settings screen should look like that shown in Figure 24 with the file path name being the location of the common directory. Click the Apply button.

Simulation Setting	gs - AC Analysis 🗙 🗙
General Analysis Category:	Configuration Files Options Data Collection Probe Window Details
Stimulus Library	Appnotes\AN1613\SPICE Model Folder\ISL28114.lib Browse
Include	Configured Files
	H:\AMS Files\1 Precision and MicroPower Amplifie Add as Global
	nom.lib Add to Design
	Add to Profile
	Edit
	Change
	Library Path
	"C:\Cadence\SPB_16.2\tools\pspice\library" Browse
	OK Cancel Apply Help

FIGURE 24. CONFIGURATION FILE TO ADD LIBRARY

Now click the analysis tab and configure the simulation as shown in Figure 25. The analysis selected for this example is an AC Sweep/Noise. Other types of analysis are: Time Domain (Transient), DC Sweep and Bias Point. Just click the down arrow in the analysis type section to access the different Analysis options. When done, click OK.

Simulation Settings - AC Ana	alysis	×
General Analysis Configuratio	n Files Options Data Coll	lection Probe Window
Analysis type: AC Sweep/Noise	AC Sweep Type	Start Frequency: 0.1
Options:	Logarithmic	End Frequency: 100Meg
General Settings Monte Carlo/Worst Case Parametric Sweep Temperature (Sweep) Save Bias Point Load Bias Point		Points/Decade: 100
	controlled sources	ias point information for nonlinear and semiconductors (.OP)
	ОК С	Cancel Apply Help

FIGURE 25. SCREEN TO SET-UP THE ANALYSIS PROFILE CONFIGURED

Add the Library .olb to the simulator. Click Place in the tool bar and select Part. This will bring up the part placement tool at the far right of the simulator as shown in Figure 26. To add the library, click on the tab where the arrow is pointing to in Figure 26.



FIGURE 26. PART PLACEMENT TOOL

This will bring up the screen shown in Figure 27. Browse to where you saved the Netlist in the common directory and click Open.

Browse File		? ×
Look in	n: 🗀 SPICE Model Folder 💽 🕓 🍺 😕 🖽 🗸	
My Conputer: My Conputer: My Computer: My Computer: My Computer: My Computer:	EL28114_ANI613-PSpiceFiles ■ ISL28114.0LB	
My Network Places	File name: ISL28114.0LB Image: Op Files of type: Capture Library(*.olb) Image: Capture Captur	

FIGURE 27. CONNECTING THE SYMBOL LIBRARY TO SIMULATOR

Now you are ready to add the sub-circuit to your simulation schematic and start your simulations.

Adding the Sub-Circuit to Your Simulation Schematic

With the .lib file added to the simulation profile and the .olb file added to the Part placement tool, your are now ready to place the Opamp sub-circuit into your simulation schematic. Figure 28 shows the part placement tool after the .olb has been added to it. Under the Libraries section, find the new .olb symbol you added in the previous step (highlighted in blue). Double click the file to add the sub-circuit to the Part list section (also highlighted in blue). Double click the Part in the part list section to add the sub-circuit to the simulation schematic.



FIGURE 28. ADDING A SUB-CIRCUIT TO A SIMULATION SCHEMATIC

Figure 29 shows sub-circuit in a basic non-inverting application circuit. The simulation result showing AVOL (green trace) and Phase (pink) are shown in Figure 30.



FIGURE 29. SIMULATION SCHEMATIC





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