R32C/118 Group and R32C/118A Group

Differences between R32C/118 (144-pin Package) and R32C/118A (176-pin Package)

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1. Abstract

This document is a reference to ascertain the changes in functions from the 144-pin package for the R32C/118 Group and the 176-pin package for the R32C/118A Group. For details on functions, refer to the hardware user's manual.

2. Introduction

This document applies to the following products:
R32C/118 Group 144-pin package and R32C/118A Group 176-pin package
R32C/117 Group 144-pin package and R32C/117A Group 176-pin package
R32C/116 Group 144-pin package and R32C/116A Group 176-pin package

3. Overview of Comparison

3.1 Overview of Functions

Table 3.1 lists the differences between products.

Table 3.1 Comparison Chart: Overview of Functions

Item	R32C/118	R32C/118A
Memory	Flash memory: 384 Kbytes to 1 Mbyte RAM: 40/48/63 Kbytes	Flash memory: 512 Kbytes to 1 Mbyte RAM: 96 Kbytes
Watchdog timer	—	Automatic timer start function is available
DMAC	Request sources: 57	Request sources: 61
I/O ports	120 CMOS I/O ports (32 are 5 V tolerant)	• 156 CMOS I/O ports (52 are 5 V tolerant) • Self test function
Serial interface	9 channels (UART0 to UART8)	11 channels (UART0 to UART10)
A/D converter	—	Self test/Open-circuit detection assist
Protect area	—	Available
Operating frequency	50 MHz	64 MHz
Flash memory	—	• Forcible erase function • Standard serial I/O mode disable function

3.2 Pin Characteristics

Table 3.2 to Table 3.7 list the number and characteristics of each pin, and changes from the R32C/118

Table 3.2 Pin No. and Changes (1/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
1	1	P9_6/TXD4/SDA4/SRXD4/CAN1OUT/ANEX1	—
2	2	P9_5/CLK4/CAN1IN/$\overline{\text{CAN1WU}}$/ANEX0	—
3	3	P9_4/TB4IN/$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$/DA1	—
4	4	P9_3/TB3IN/$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$/DA0	—
5	5	P9_2/TB2IN/TXD3/SDA3/SRXD3/OUTC2_0/ISTXD2/IEOUT	—
6	6	P9_1/TB1IN/RXD3/SCL3/STXD3/ISRXD2/IEIN	—
7	7	P9_0/TB0IN/CLK3	—
8	—	P19_7	Added: P19_7
9	8	P14_6/$\overline{\text{INT8}}$	—
10	—	P19_6	Added: P19_6
11	9	P14_5/$\overline{\text{INT7}}$	—
12	10	P14_4/$\overline{\text{INT6}}$	—
13	11	P14_3	—
14	12	VDC0	—

Table 3.3 Pin No. and Changes (2/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
15	13	P14_1	—
16	14	VDC1	—
17	15	NSD	—
18	16	CNVSS	—
19	17	XCIN/P8_7	—
20	18	XCOUT/P8_6	—
21	19	$\overline{\text{RESET}}$	—
22	20	XOUT	—
23	21	VSS	—
24	22	XIN	—
25	23	VCC	—
26	24	P8_5/$\overline{\text{NMI}}$	—
27	25	P8_4/$\overline{\text{INT2}}$	—
28	26	P8_3/$\overline{\text{INT1}}$/CAN0IN/$\overline{\text{CAN0WU}}$/CAN1IN/$\overline{\text{CAN1WU}}$	—
29	27	P8_2/$\overline{\text{INT0}}$/CAN0OUT/CAN1OUT	—
30	28	P8_1/TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/IIO1_5/UD0B/UD1B	—
31	29	P8_0/TA4OUT/U/RXD5/SCL5/STXD5/UD0A/UD1A	—
32	-	P18_1	Added: P18_1
33	-	P18_0	Added: P18_0
34	30	P7_7/TA3IN/CLK5/CAN0IN/CAN0WU/IIO1_4/ UD0B/UD1B	—
35	31	P7_6/TA3OUT/TXD5/SDA5/SRXD5/CTS8/RTS8/ CAN0OUT/IIO1_3/UD0A/UD1A	—
36	32	P7_5/TA2IN/$\overline{\text{W}}$/RXD8/IIO1_2	—
37	33	P7_4/TA2OUT/W/CLK8/IIO1_1	—
38	—	P17_7	Added: P17_7
39	—	P17_6	Added: P17_6
40	—	P17_5	Added: P17_5
41	—	P17_4	Added: P17_4
42	34	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8/IIO1_0	—
43	35	P7_2/TA1OUT/V/CLK2	—
44	36	P7_1/TB5IN/TA0IN/RXD2/SCL2/STXD2/MSCL/ IIO1_7/OUTC2_2/ISRXD2/IEIN	—
45	37	P7_0/TA0OUT/TXD2/SDA2/SRXD2/MSDA/ IIO1_6/OUTC2_0/ISTXD2/IEOUT	—
46	38	P6_7/TXD1/SDA1/SRXD1	—
47	39	P14_7	Deleted: VCC Added: P14_7
48	40	P6_6/RXD1/SCL1/STXD1	—

Table 3.4 Pin No. and Changes (3/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
49	41	P11_7	Deleted: VSS Added: P11_7
50	42	P6_5/CLK1	—
51	43	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$/OUTC2_1/ISCLK2	—
52	44	P6_3/TXD0/SDA0/SRXD0	—
53	45	P6_2/TB2IN/RXD0/SCL0/STXD0	—
54	46	P6_1/TB1IN/CLK0	—
55	47	P6_0/TB0IN/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	—
56	—	P19_5	Added: P19_5
57	48	P13_7/OUTC2_7/D31	—
58	49	P13_6/OUTC2_1/ISCLK2/D30	—
59	50	P13_5/OUTC2_2/ISRXD2/IEIN/D29	—
60	51	P13_4/OUTC2_0/ISTXD2/IEOUT/D28	—
61	—	P19_4	Added: P19_4
62	52	P5_7/$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/$\overline{\text{RDY}}$/$\overline{\text{CS3}}$	—
63	53	P5_6/RXD7/ALE/$\overline{\text{CS2}}$	—
64	54	P5_5/CLK7/$\overline{\text{HOLD}}$	—
65	55	P5_4/TXD7/$\overline{\text{HLDA}}$/$\overline{\text{CS1}}$	—
66	56	P13_3/OUTC2_3/D27	—
67	57	VSS	—
68	58	P13_2/OUTC2_6/D26	—
69	59	VCC	—
70	60	P13_1/OUTC2_5/D25	—
71	61	P13_0/OUTC2_4/D24	—
72	62	P5_3/CLKOUT/BCLK	—
73	63	P5_2/$\overline{\text{RD}}$	—
74	64	P5_1/$\overline{\text{WR1}}$/$\overline{\text{BC1}}$	—
75	65	P5_0/$\overline{\text{WR0}}$/$\overline{\text{WR}}$	—
76	66	P12_7/D23	—
77	67	P12_6/D22	—
78	68	P12_5/D21	—
79	—	P19_3	Added: P19_3
80	—	P17_3	Added: P17_3
81	—	P17_2	Added: P17_2
82	—	P17_1	Added: P17_1
83	—	P17_0	Added: P17_0
84	—	P19_2	Added: P19_2

Table 3.5 Pin No. and Changes (4/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
85	69	P4_7/TXD6/SDA6/SRXD6/$\overline{CS0}$/A23	—
86	70	P4_6/RXD6/SCL6/STXD6/$\overline{CS1}$/A22	—
87	71	P4_5/CLK6/$\overline{CS2}$/A21	—
88	72	P4_4/$\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$/$\overline{CS3}$/A20	—
89	73	P4_3/TXD3/SDA3/SRXD3/OUTC2_0/ISTXD2/ IEOUT/A19	—
90	74	P11_6	Deleted: VCC Added: P11_6
91	75	P4_2/RXD3/SCL3/STXD3/ISRXD2/IEIN/A18	—
92	76	P11_5	Deleted: VSS Added: P11_5
93	77	P4_1/CLK3/A17	—
94	78	P4_0/$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$/A16	—
95	—	P16_7/TXD10	Added: P16_7/TXD10
96	—	P16_6/RXD10	Added: P16_6/ RXD10
97	—	P16_5/CLK10	Added: P16_5/CLK10
98	—	P16_4/$\overline{CTS10}$/$\overline{RTS10}$	Added: P16_4/ $\overline{CTS10}$/$\overline{RTS10}$
99	79	P3_7/TA4IN/$\overline{U}$/A15(/D15)	—
100	80	P3_6/TA4OUT/U/A14(/D14)	—
101	81	P3_5/TA2IN/$\overline{W}$/A13(/D13)	—
102	82	P3_4/TA2OUT/W/A12(/D12)	—
103	—	P16_3/TXD9	Added: P16_3/TXD9
104	—	P16_2/RXD9	Added: P16_2/RXD9
105	—	P16_1/CLK9	Added: P16_1/CLK9
106	—	P16_0/$\overline{CTS9}$/$\overline{RTS9}$	Added: P16_0/$\overline{CTS9}$/ $\overline{RTS9}$
107	83	P3_3/TA1IN/$\overline{V}$/A11(/D11)	—
108	84	P3_2/TA1OUT/V/A10(/D10)	—
109	85	P3_1/TA3OUT/UD0B/UD1B/A9(/D9)	—
110	86	P12_4/D20	—
111	87	P12_3/$\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$/D19	—
112	88	P12_2/RXD6/SCL6/STXD6/D18	—
113	89	P12_1/CLK6/D17	—
114	90	P12_0/TXD6/SDA6/SRXD6/D16	—
115	91	VCC	—
116	92	P3_0/TA0OUT/UD0A/UD1A/A8(/D8)	—
117	93	VSS	—

Table 3.6 Pin No. and Changes (5/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
118	94	P2_7/TXD10/AN2_7/A7(/D7)	Added: TXD10
119	95	P2_6/RXD10/AN2_6/A6(/D6)	Added: RXD10
120	96	P2_5/CLK10/AN2_5/A5(/D5)	Added: CLK10
121	97	P2_4/$\overline{\text{CTS10}}$/$\overline{\text{RTS10}}$/AN2_4/A4(/D4)	Added: $\overline{\text{CTS10}}$/$\overline{\text{RTS10}}$
122	98	P2_3/TXD9/AN2_3/A3(/D3)	Added: TXD9
123	99	P2_2/RXD9/AN2_2/A2(/D2)	Added: RXD9
124	100	P2_1/CLK9/AN2_1/A1(/D1)/$\overline{\text{BC2}}$(/D1)	Added: CLK9
125	101	P2_0/$\overline{\text{CTS9}}$/$\overline{\text{RTS9}}$/AN2_0/A0(/D0)/$\overline{\text{BC0}}$(/D0)	Added: $\overline{\text{CTS9}}$/$\overline{\text{RTS9}}$
126	102	P1_7/$\overline{\text{INT5}}$/IIO0_7/IIO1_7/D15	—
127	103	P1_6/$\overline{\text{INT4}}$/IIO0_6/IIO1_6/D14	—
128	104	P1_5/$\overline{\text{INT3}}$/IIO0_5/IIO1_5/D13	—
129	105	P1_4/IIO0_4/IIO1_4/D12	—
130	106	P1_3/IIO0_3/IIO1_3/D11	—
131	107	P1_2/IIO0_2/IIO1_2/D10	—
132	108	P1_1/IIO0_1/IIO1_1/D9	—
133	109	P1_0/IIO0_0/IIO1_0/D8	—
134	110	P0_7/AN0_7/D7	—
135	111	P0_6/AN0_6/D6	—
136	112	P0_5/AN0_5/D5	—
137	113	P0_4/AN0_4/D4	—
138	—	P19_1	Added: P19_1
139	114	P11_4/$\overline{\text{BC3}}$/$\overline{\text{WR3}}$	—
140	—	P19_0	Added: P19_0
141	115	P11_3/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/IIO1_3/$\overline{\text{CS3}}$/$\overline{\text{WR2}}$	—
142	116	P11_2/RXD8/IIO1_2/$\overline{\text{CS2}}$	—
143	117	P11_1/CLK8/IIO1_1/$\overline{\text{CS1}}$	—
144	118	P11_0/TXD8/IIO1_0/$\overline{\text{CS0}}$	—
145	—	P18_7	Added: P18_7
146	—	P18_6	Added: P18_6
147	—	P18_5	Added: P18_5
148	—	P18_4	Added: P18_4
149	—	P18_3	Added: P18_3
150	—	P18_2	Added: P18_2
151	119	P0_3/AN0_3/D3	—
152	120	P0_2/AN0_2/D2	—
153	121	P0_1/AN0_1/D1	—
154	122	P0_0/AN0_0/D0	—

Table 3.7 Pin No. and Changes (6/6)

R32C/118A 176-pin Package Pin No.	R32C/118 144-pin Package Pin No.	R32C/118A Functions	Changes from the R32C/118
155	123	P15_7/$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$/IIO0_7/AN15_7	—
156	124	P15_6/CLK6/IIO0_6/AN15_6	—
157	125	P15_5/RXD6/SCL6/STXD6/IIO0_5/AN15_5	—
158	126	P15_4/TXD6/SDA6/SRXD6/IIO0_4/AN15_4	—
159	127	P15_3/$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/IIO0_3/AN15_3	—
160	128	P15_2/RXD7/IIO0_2/AN15_2	—
161	129	P15_1/CLK7/IIO0_1/AN15_1	—
162	130	VSS	—
163	131	P15_0/TXD7/IIO0_0/AN15_0	—
164	132	VCC	—
165	133	P10_7/$\overline{\text{KI3}}$/AN_7	—
166	134	P10_6/$\overline{\text{KI2}}$/AN_6	—
167	135	P10_5/$\overline{\text{KI1}}$/AN_5	—
168	136	P10_4/$\overline{\text{KI0}}$/AN_4	—
169	137	P10_3/AN_3	—
170	138	P10_2/AN_2	—
171	139	P10_1/AN_1	—
172	140	AVSS	—
173	141	P10_0/AN_0	—
174	142	VREF	—
175	143	AVCC	—
176	144	P9_7/RXD4/SCL4/STXD4/$\overline{\text{ADTRG}}$	—

4. Detailed Comparison

4.1 Clock

Table 4.1 lists the changes in SFRs associated with the clock.

Table 4.1 Comparison Chart: Clock-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
PM2	40035h	40035h	2	—	Watchdog timer count source protect bit
			3	—	Watchdog timer count source select bit

4.2 Protection

Table 4.2 lists the changes in SFRs associated with protection.

Table 4.2 Comparison Chart: Protection-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
PRR	0007h	0007h	—	Control the protection for registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23.	Control the protection for registers CCR, FMCR, PBC, FEBC, EBC0 to EBC3, CB01, CB12, and CB23.
PRCR4	—	4404Ch	—	—	Available only in the R32C/118A

4.3 Interrupts

Table 4.3 lists the changes in SFRs associated with interrupts.
The relocatable vector tables and interrupt priority level select circuitry of each are different.

Table 4.3 Comparison Chart: Interrupt-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
S9TIC	—	00D9h	—	—	Available only in the R32C/118A
S10TIC	—	00DBh	—	—	Available only in the R32C/118A
S9RIC	—	00F9h	—	—	Available only in the R32C/118A
S10RIC	—	00FBh	—	—	Available only in the R32C/118A

4.4 Watchdog Timer

Table 4.4 and Table 4.5 list the changes in the watchdog timer and associated SFRs, respectively.

Table 4.4 Comparison Chart: Watchdog Timer

Item	R32C/118	R32C/118A
Clock source for watchdog timer	Peripheral bus clock	Peripheral bus clock, on-chip oscillator clock
Watchdog timer prescaler divide ratio	Divide-by-16 or -128	When peripheral bus clock is selected: Divide-by-16 or -128 When on-chip oscillator clock is selected: Divide-by-1, -2, -4, -8, -16, -32, -64, -128, -256, -512, or -1024
Automatic timer start function	—	Available

Table 4.5 Comparison Chart: Watchdog Timer-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
WDK	—	4404Dh	—	—	Available only in the R32C/118A
WDC	4404Fh	4404Fh	4 to 0	Upper 5 bits of the watchdog timer (b14 to b10)	Upper 5 bits of the watchdog timer, when the peripheral bus clock is used: b14 to b10 When the on-chip oscillator is used: b10 to b6 (1)
OFS	—	FFFFFFEFh	—	—	Available only in the R32C/118A

Note:
1. When the on-chip oscillator clock is used as the count source, the read value may be undefined due to a change in the count value while being read.

4.5 DMAC

Table 4.6 lists the changes in DMAC.

Table 4.6 Comparison Chart: DMAC

Item	R32C/118	R32C/118A
DMA request sources	UART0 to UART8 transmit/receive interrupt requests	UART0 to UART11 transmit/receive interrupt requests

4.6 Serial Interface

Table 4.7 lists the changes in serial interface associated SFRs.

Table 4.7 Comparison Chart: Serial Interface-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
U9MR	—	40300h	—	—	Available only in the R32C/118A
U9BRG	—	40301h	—	—	Available only in the R32C/118A
U9TB	—	40303h to 40302h	—	—	Available only in the R32C/118A
U9C0	—	40304h	—	—	Available only in the R32C/118A
U9C1	—	40305h	—	—	Available only in the R32C/118A
U9RB	—	40307h to 40306h	—	—	Available only in the R32C/118A
U10MR	—	40308h	—	—	Available only in the R32C/118A
U10BRG	—	40309h	—	—	Available only in the R32C/118A
U10TB	—	4030Bh to 4030Ah	—	—	Available only in the R32C/118A
U10C0	—	4030Ch	—	—	Available only in the R32C/118A
U10C1	—	4030Dh	—	—	Available only in the R32C/118A
U10RB	—	4030Fh to 4030Eh	—	—	Available only in the R32C/118A
U910CON	—	40310h	—	—	Available only in the R32C/118A

4.7 A/D Converter

Table 4.8 and Table 4.9 list the changes in A/D converter and associated SFRs, respectively.

Table 4.8 Comparison Chart: A/D Converter

Item	R32C/118	R32C/118A
Operating modes	—	Open-circuit detection, self-test mode

Table 4.9 Comparison Chart: A/D Converter-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
AD0CON5	—	0393h	—	—	Available only in the R32C/118A

4.8 Protected Areas

The R32C/118A Group has five 32-bit areas protected from unexpected write accesses. Like RAM, the protected areas are randomly accessible. However, they are not rewritable while the protection is locked. Table 4.10 lists the address range of protected areas and Table 4.11 lists the protected area-associated SFRs.

Table 4.10 Address Range of Protected Areas

Protected Area	Address Range
Protected Area 0	42000h to 4201Fh
Protected Area 1	42020h to 4203Fh
Protected Area 2	42040h to 4205Fh
Protected Area 3	42060h to 4207Fh
Protected Area 4	42080h to 4209Fh

Table 4.11 Comparison Chart: Protected Area-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
PAPR	—	420F0h	—	—	Available only in the R32C/118A
PAWF	—	420F2h	—	—	Available only in the R32C/118A

4.9 I/O Pins

Table 4.12 to Table 4.15 list the changes in I/O pin-associated SFRs.

Table 4.12 Comparison Chart: I/O Pin-associated SFRs (1/4)

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
P11	03D5h	03D5h	5	—	Port P11_5 bit
			6	—	Port P11_6 bit
			7	—	Port P11_7 bit
P14	03DCh	03DCh	7	—	Port P14_7 bit
PD11	03D7h	03D7h	5	—	Port P11_5 direction bit (1)
			6	—	Port P11_6 direction bit (1)
			7	—	Port P11_7 direction bit (1)
PD14	03DEh	03DEh	7	—	Port P14_7 direction bit (1)
PUR3	03F3h	03F3h	4	P12_0 to P12_3 pull-up control bit	—
			5	P12_4 to P12_7 pull-up control bit	—
PUR4	03F4h	03F4h	7	—	P17_4 to P17_7 pull-up control bit (2)
PUR5	-	03F5h	—	—	Available only in the R32C/118A (3)
PCR	03FFh	03FFh	3	—	Read data select bit
			6	—	PD11_5 to PD11_7, PD14_7 write enable bit
			7	Port P9_0, P9_2, P11 to P15 enable bit	Reserved
IFS3	4009Bh	4009Bh	4	—	UART9 input pin switch bit (2)
			5	—	UART10 input pin switch bit (2)

Notes:
1. Set the PDWE bit in the PCR register to 1 (write enabled) before rewriting this bit.
2. This bit should be set to 0 in the 144-pin package.
3. This register should be set to 00h in the 144-pin package.

Table 4.13 Comparison Chart: I/O Pin-associated SFRs (2/4)

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
P2_0S	400B0h	400B0h	6	—	N-channel open drain output select bit
P2_1S	400B2h	400B2h	6	—	N-channel open drain output select bit
P2_2S	400B4h	400B4h	6	—	N-channel open drain output select bit
P2_3S	400B6h	400B6h	6	—	N-channel open drain output select bit
P2_4S	400B8h	400B8h	6	—	N-channel open drain output select bit
P2_5S	400BAh	400BAh	6	—	N-channel open drain output select bit
P2_6S	400BCh	400BCh	6	—	N-channel open drain output select bit
P2_7S	400BEh	400BEh	6	—	N-channel open drain output select bit
P11_5S	—	400FBh	—	—	Available only in the R32C/118A
P11_6S	—	400FDh	—	—	Available only in the R32C/118A
P11_7S	—	400FFh	—	—	Available only in the R32C/118A
P12_4S	40108h	40108h	6	—	N-channel open drain output select bit
P12_5S	4010Ah	4010Ah	6	—	N-channel open drain output select bit
P12_6S	4010Ch	4010Ch	6	—	N-channel open drain output select bit
P12_7S	4010Eh	4010Eh	6	—	N-channel open drain output select bit
P14_7S	—	4011Fh	—	—	Available only in the R32C/118A

Table 4.14 Comparison Chart: I/O pin-associated SFRs (3/4)

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
P16	—	03E0h	—	—	Available only in the R32C/118A
P17	—	03E1h	—	—	Available only in the R32C/118A
PD16	—	03E2h	—	—	Available only in the R32C/118A
PD17	—	03E3h	—	—	Available only in the R32C/118A
P18	—	03E4h	—	—	Available only in the R32C/118A
P19	—	03E5h	—	—	Available only in the R32C/118A
PD18	—	03E6h	—	—	Available only in the R32C/118A
PD19	—	03E7h	—	—	Available only in the R32C/118A

Table 4.15 Comparison Chart: I/O pin-associated SFRs (4/4)

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
P16_0S	—	40120h	—	—	Available only in the R32C/118A
P17_0S	—	40121h	—	—	Available only in the R32C/118A
P16_1S	—	40122h	—	—	Available only in the R32C/118A
P17_1S	—	40123h	—	—	Available only in the R32C/118A
P16_2S	—	40124h	—	—	Available only in the R32C/118A
P17_2S	—	40125h	—	—	Available only in the R32C/118A
P16_3S	—	40126h	—	—	Available only in the R32C/118A
P17_3S	—	40127h	—	—	Available only in the R32C/118A
P16_4S	—	40128h	—	—	Available only in the R32C/118A
P17_4S	—	40129h	—	—	Available only in the R32C/118A
P16_5S	—	4012Ah	—	—	Available only in the R32C/118A
P17_5S	—	4012Bh	—	—	Available only in the R32C/118A
P16_6S	—	4012Ch	—	—	Available only in the R32C/118A
P17_6S	—	4012Dh	—	—	Available only in the R32C/118A
P16_7S	—	4012Eh	—	—	Available only in the R32C/118A
P17_7S	—	4012Fh	—	—	Available only in the R32C/118A
P18_0S	—	40130h	—	—	Available only in the R32C/118A
P19_0S	—	40131h	—	—	Available only in the R32C/118A
P18_1S	—	40132h	—	—	Available only in the R32C/118A
P19_1S	—	40133h	—	—	Available only in the R32C/118A
P18_2S	—	40134h	—	—	Available only in the R32C/118A
P19_2S	—	40135h	—	—	Available only in the R32C/118A
P18_3S	—	40136h	—	—	Available only in the R32C/118A
P19_3S	—	40137h	—	—	Available only in the R32C/118A
P18_4S	—	40138h	—	—	Available only in the R32C/118A
P19_4S	—	40139h	—	—	Available only in the R32C/118A
P18_5S	—	4013Ah	—	—	Available only in the R32C/118A
P19_5S	—	4013Bh	—	—	Available only in the R32C/118A
P18_6S	—	4013Ch	—	—	Available only in the R32C/118A
P19_6S	—	4013Dh	—	—	Available only in the R32C/118A
P18_7S	—	4013Eh	—	—	Available only in the R32C/118A
P19_7S	—	4013Fh	—	—	Available only in the R32C/118A

4.10 Flash Memory

Table 4.16 lists the changes in flash memory-associated SFRs, Table 4.17 lists the changes in registers in single-chip mode, and Table 4.18 lists the changes in registers in the memory expansion mode.

Table 4.16 Comparison Chart: Flash Memory-associated SFRs

Symbol	Address		Bit	R32C/118	R32C/118A
	R32C/118	R32C/118A			
FEBC	—	0009h to 0008h	—	—	Available only in the R32C/118A
FEBC0	001Dh to 001Ch	—	—	Available only in the R32C/118	—
FEBC3	0011h to 0010h	—	—	Available only in the R32C/118	—
FMR0	40000h	40000h	6	Reserved	Suspend request acknowledge flag
FMSR0	40001h	40001h	3	Reserved	Program suspend status flag
			6	Reserved	Erase suspend status flag
FMR1	40009h	40009h	0	Reserved	Suspend request interrupt level select bit
			5	Reserved	Suspend request bit
			6	Reserved	Suspended and ready flag
			7	Reserved	Suspend enable bit

Table 4.17 Comparison Chart: Registers in Single-chip Mode

Item	R32C/118	R32C/118A
Bus setting in the program area	FEBC0 register	FEBC register
Bus setting in the data area		

Table 4.18 Comparison Chart: Registers in Memory Expansion Mode

Item	R32C/118	R32C/118A
Bus setting in the program area	FEBC0 register	FEBC register
Bus setting in the data area	FEBC3 register	

5. Reference Documents

User's Manuals
R32C/118 Group User's Manual: Hardware Rev.1.00
R32C/118A Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website

Website and Support

Renesas Electronics website
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REVISION HISTORY	R32C/118 Group and R32C/118A Group Differences between R32C/118 (144-pin Package) and R32C/118A (176-pin Package)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 15, 2010	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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