GENERAL LAYOUT GUIDELINES FOR 1893

- Use a power supply noise filtering scheme similar to the one shown on the corresponding evaluation board schematic.
- 0.01uF decoupling capacitors should be mounted on the component side of the board as close to the VDD pins as possible. The PCB trace to the VDD pins should be kept as short as possible, as should the PCB trace to the ground via.
- The external crystal should be mounted just next to the device with short traces. They should be separated and away from other traces.
- An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers.
- Use proper series termination resistors wherever applicable to match the board impedance.
- The impedance matching resistor/inductor network should be connected as close to the twisted pair Transmit/Receive lines as possible.
- The cable side center tap connections and shield of the integrated magnetics module should be bypassed to chassis ground, not chip VSS. Transformer center tap on the ICS1893 side should bypass to VSS if used. Check datasheet for correct connection. Ground planes are broken through the magnetics. Chip side bypass connections are to VSS. Cable side bypass connections are to chassis ground.
- If you are using non-integrated magnetics make sure that the unused twisted pairs and terminated using Bob Smith termination scheme. The Bob Smith termination absorbs capacitive coupled energy from the two twisted pairs not used in the Cat5 cable.

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