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# **R8C/Tiny Series**

# General-purpose Program for Example for Initial Setting Assembler

#### Abstract

This program is an example of initial settings accomplished by using the directive commands of the assembler.

#### 2. Introduction

The program shown here consists of the following:

- (1) Map file information output
- (2) Global symbol name specification
- (3) Numeric symbol definition
- (4) RAM area allocation
- (5) Bit symbol definition
- (6) Initial setup program
  - Interrupt stack pointer setting
  - FB register setting
  - · SB register setting
  - INTB register setting
  - RAM clear
- (7) Peripheral I/O interrupt vector table
- (8) Nonmaskable interrupt fixed vector table

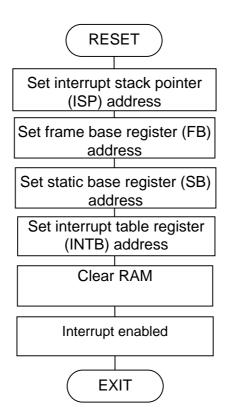
The following shows the range of the FB and SB relative addresses in this program.

	380H to 47FH
	-128
FB	<b>↑</b>
	-400H
	↓
	+ 127
SB	480H to 57FH
	480H
	↓
	+ 255

This program can also be used when operating other microcomputers within the R8C /10 group, provided they have the same vector table as the R8C microcomputers. However, some functions may have been modified. Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.



# 3. Flowchart





# 4. The example of a reference program

.*********	******	*******	************			
; CPU ;	ogram Collecti : R8C/Tir	ny	* * *			
;=======	=======		**************************************			
; Outline:	_	5g				
; (1)	Assemble cor	ntrol				
; (2)	Address conti	rol				
; (3)	(3) Link control					
; (4)	(4) List control					
; (5)	Branch instru	ction optimization	control			
; Notes:						
;		;				
•	information o	utput ::	;			
,	.VER	•	; 'Ver1.02' is output when generating map file			
;		;				
; Global s	symbol name s		;			
;		;	; [Global symbol specification]			
,	.GLB	RUTINE	; Externlly referenced symbol			
	.GLB	MAIN	; Public symbol			
;			;			
;			; [Global bit symbol specification]			
	.BTGLB	P3_0	; Externally referenced symbol			
	.BTGLB	P0_7	; Public symbol			
;			;			
; Numerio	symbol defin	ition	;			
; VramTOP	.EQU	; 000400H	; Declares start address of RAM			
VramEND	.EQU	0006FFH	; Declares last address of RAM			
VIstack	.EQU	000600H	; Interrupt stack pointer			
VproTOP	.EQU	00D000H	; Declares start address of program			
VECTOR_AD	OR .EQU	00FE00h	; Declares start address of variable vector table			
FIX_VECTO	R.EQU	00FFDCh	; Declares fixed interrupt vector address			
; CNT125ms	.EQU	125	; ; Sets 125 in CNT125ms			
; AUTOchar	.EQU	-8	; ; Sets -8 in AUTOchar			
;	.FORM	45,160	; ; [List output control instruction]			
;	.i Ordivi	10,100	; Specifies 45 lines, 160 columns per page of list file			
			, -,			



	.LIST	ON	; [List output control]
			; Outputs assembler list
	.PAGE	'RAM'	; [List page break and title specification]
	.SECTION	MEMORY,DATA	; [Section name specification]
			; Declares DATA attribute section of section name "MEMORY"
	.ORG	VramTOP	; [Absolute address setting]
			; Sets location to 400H
		;	
RAM a	rea allocation		;
		;	
			; [RAM area 1-byte allocation]
CHAR:	.BLKB	10	; Allocates 10-byte area
			;
			; [RAM area 2-byte allocation]
SHORT:	.BLKW	10	; Allocates 20-byte area
		. •	
			, ; [RAM area 3-byte allocation]
ADDR:	.BLKA	10	; Allocates 30-byte anocation;
NDDIN.	.DLIVA	10	, Allocates 50-byte area
			, IDAM area 4 buts allegation.
ONC.	DLIZI	40	; [RAM area 4-byte allocation]
ONG:	.BLKL	10	; Allocates 40-byte area
			;
			; [Single-precision, floating-point RAM area allocation]
SFLOAT:	.BLKF	10	; Allocates 40-byte area
			;
			; [Double-precision, floating-point RAM area allocation]
OFLOAT:	.BLKD	10	; Allocates 80-byte area
			;
CHECK:	.BLKW	10	;
			;
		;	
Bit sym	bol definition		;
		<del>;</del>	
BIT4 .B	TEQU 4,0	CHAR	; Sets bit 4 of displacement CHAR to BIT4
MSB	.BTEQI	J 15,SHORT	; Sets bit 15 of displacement SHORT to MSB
P0_7	.BTEQU	7,3E0H	; Sets bit 7 at address 3E0 to P0_7
			;
	.SECTION	PROG,CODE	; Declares CODE attribute section of section name "PROG"
	.ORG	VproTOP	; Sets location to F0000H
	.OPTJ	OFF	; [Branch instruction optimize specification]
			; Does not optimize branch instruction after this line
	.FB Vr	amTOP	; [Assumption of FB register value]
			; Assumes 400H for FB register value
	.SB Vr	amTOP+80H	; [Assumption of SB register value]
	•••		; Assumes 480H for SB register value
	.FBSYM	SHORT	
	.SBSYM	CHECK	•
			,
=======			=======;
Prograi			



```
RESET:
            #VIstack,ISP
    LDC
                                                   ; Sets interrupt stack pointer
    LDC
            #VramTOP,FB
                                                       ; Sets frame base register
    LDC
            #VramTOP+80H,SB
                                                           ; Sets static base register
    LDINTB #VECTOR_ADR
                                                           ; Sets interrupt table register
    MOV.W #0,R0
                                                       ; Sets store data (0)
    MOV.W #((VramEND+1)-VramTOP)/2,R3
                                                       ; Sets number of transfers performed
    MOV.W #VramTOP,A1
                                                       ; Sets address where to start storing
    SSTR.W
                                                       ; Executes clearing of RAM
    FSET I
                                                       ; Enables interrupt
    Main program
    MOV.W #1234H,SHORT
    MOV.W #5678H,CHECK
    JSR
            ROUTINE
    BSET
            P0_7
            (Here is your program.)
ROUTINE:
            (Here is your program.)
    RTS
NOTUSE:
            (Here is your program.)
    RTS
            .PAGE
                         'VECTOR'
            .SECTION UINTER,ROMDATA
                                                           ; Declares FOMDATA attribute section of section name "UINTER"
                     VECTOR_ADR
    Peripheral I/O interrupt vector table
                         NOTUSE
                                                       ; BRK instruction
                                                                            (vector 0)
            .lword
                     (VECTOR_ADR+52)
            .org
                         NOTUSE
                                                       ; Key input interrupt
                                                                            (vector 13)
            .lword
```



.lword		NOTUSE		; A-D		(vector	14)	
.org	(VE	CTOR_ADR+68)						
.lword		NOTUSE		; UART0 trans	smit (vec	tor 17)		
.lword		NOTUSE		; UART0 rece	ive	(vector	r 18)	
.lword		NOTUSE		; UART1 trans	smit (vec	tor 19)		
.lword		NOTUSE		; UART1 rece	ive	(vector	20)	
.lword		NOTUSE		; INT2		(vector	121)	
.lword		NOTUSE		; Timer X	(vec	tor 22)		
.lword		NOTUSE		; Timer Y	(vec	tor 23)		
.lword		NOTUSE		; Timer Z	(vec	tor 24)		
.lword		NOTUSE		; INT1		(vector	25)	
.lword		NOTUSE		; INT3		(vector	r 26)	
.lword		NOTUSE		; Timer C	(vec	tor 27)		
.org	(VE	CTOR_ADR+116)						
.lword		NOTUSE		; INTO		(vector	r 29)	
.org	(VE	CTOR_ADR+128)						
.lword		NOTUSE		; vector 32 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 33 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 34 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 35 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 36 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 37 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 38 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 39 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 40 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 41 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 42 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 43 (fo	r user or MR30	))		
.lword	NOT	TUSE	; vec	tor 44 (for use	er or MR30)			
.lword		NOTUSE		; vector 45 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 46 (fo	r user or MR30	))		
.lword		NOTUSE		; vector 4	17 (for user or N	ИR30)		
.SEC	ΓΙΟΝ	INTER,ROMDATA		; Declares FC	MDATA attribu	te secti	on of section name "II	NTER"
.ORG		FIX_VECTOR		; Sets location	to FFFDCH			
.LWO	RD	NOTUSE		; FFFDC to F	Undefined ins	truction	ı	
.LWO	RD	NOTUSE		; FFFE0 to 3	Overflow			
.LWO	RD	NOTUSE		; FFFE4 to 7	BRK instruction	n		
.LWO	RD	NOTUSE		; FFFE8 to B	Address coinc	idence		
.LWO	RD	NOTUSE		; FFFEC to F	Single steppin	ıg		
.LWO	RD	NOTUSE		; FFFF0 to 3	Watchdog time	er		
.LWO	RD	NOTUSE		; FFFF4 to 7	Debugger			
.LWO	RD	NOTUSE		; FFFF8 to B	NMI			
.LWO	RD	RESET		; FFFFC to F	Reset			
;; End of assembl		; ion		;				
,		;						
.END				;				



## 5. Reference

SOFTWARE MANUAL
R8C/Tiny Series SOFTWARE MANUAL
(Acquire the most current version from Renesas web-site)

# 6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com/jpn

Contact for M16C family microcomputer technical support

Mail to: support\_apl@renesas.com



# **REVISION HISTORY**

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