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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

Normal Mode Data Transfer by the EXDMAC

Introduction

Data transfer is performed by the EXDMAC in normal transfer mode.

Target Device

H8S/2377

Contents

1. Specifications 2
2. Applicable Conditions 3
3. Description of Functions 4
4. Description of Operation 5
5. Description of Software 6
6. Flowchart 12

1. Specifications

- The EXDMAC is activated by software and transfers 1024 bytes of data in flash memory to SRAM.
- DMA transfer is configured as shown in table 1.
- Flash memory is allocated to CS1 and SRAM is allocated to CS2.

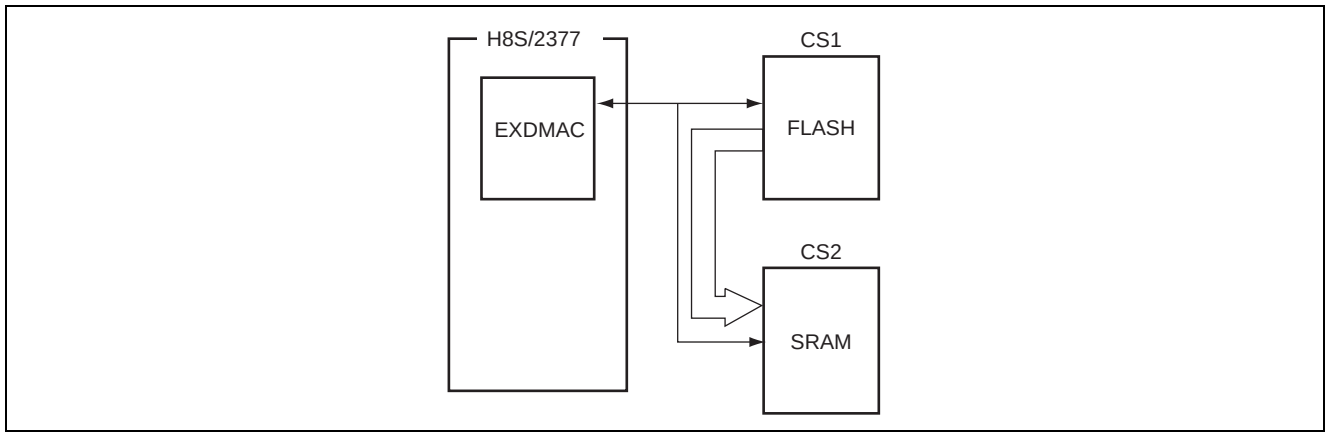


Figure 1 Transfer by EXDMAC

Table 1 Configuration of EXDMAC

Item	Description
DMA transfer request	Auto-request mode
Bus mode	Cycle steal mode
Transfer mode	Normal transfer mode
Address mode	Dual-address mode
Transfer size	One byte

2. Applicable Conditions

Table 2 Applicable Conditions

Item	Description	
Operating frequency	Input clock:	19.6608 MHz
	System clock (Iϕ):	19.6608 MHz
	Peripheral module clock (Pϕ):	19.6608 MHz
	External bus clock (Bϕ):	19.6608 MHz
Operating mode	Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)	
Development tool	HEW: version 3.01.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler: version 6.00.02 (from Renesas Technology Corp.)	
Compile options	-cpu = 2000a:24, -code = machinecode, -optimize=1, -regparam = 3 -speed = (register,shift,struct,expression)	

Table 3 Section Settings

Address	Section Name	Description
H'000000	CV1	Reset vector
H'001000	P	Program area

3. Description of Functions

Figure 2 shows the block diagram of the EXDMAC, which is described below.

- The EXDMA source address register 2 (EDSAR_2)
  EDSAR_2 is a 32-bit readable/writable registers that specifies the transfer source address. It has an address update function which allows the register contents to be updated to the next source address each time transfer processing is performed.
- The EXDMA destination address register 2 (EDDAR_2)
  EDDAR_2 is a 32-bit readable/writable registers that specifies the transfer destination address. It has an address update function which allows the register contents to be updated to the next destination address each time transfer processing is performed.
- The EXDMA transfer count register 2 (EDTCR_2)
  EDTCR_2 is loaded with the size of data to be transferred (total transfer size). Each time data is transferred, the value of this register is decremented according to the access size of the transferred data. In this sample task, EDTCR_2 is loaded with H'00000400, which corresponds to 1024 bytes, and the data access size is set to one byte. During EXDMA operation, EDTCR_2 value is decremented by 1, indicating the number of remaining transfers.
- The EXDMA mode control register 2 (EDMDR_2)
  EDMDR_2 controls the operation of the EXDMAC.
- The EXDMA address control register 2 (EDACR_2)
  EDACR_2 sets the operating mode, transfer method, etc.

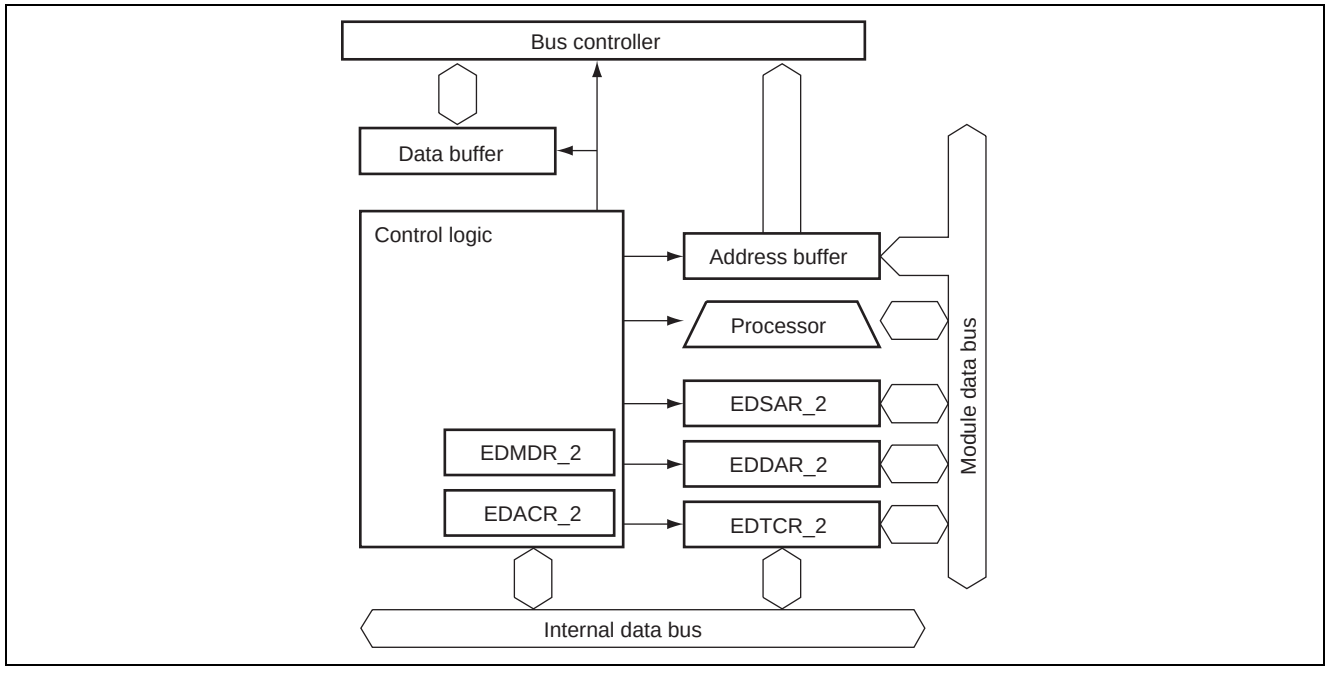


Figure 2 Block Diagram of EXDMAC

4. Description of Operation

The operation of normal transfer in dual-address mode is outlined below.

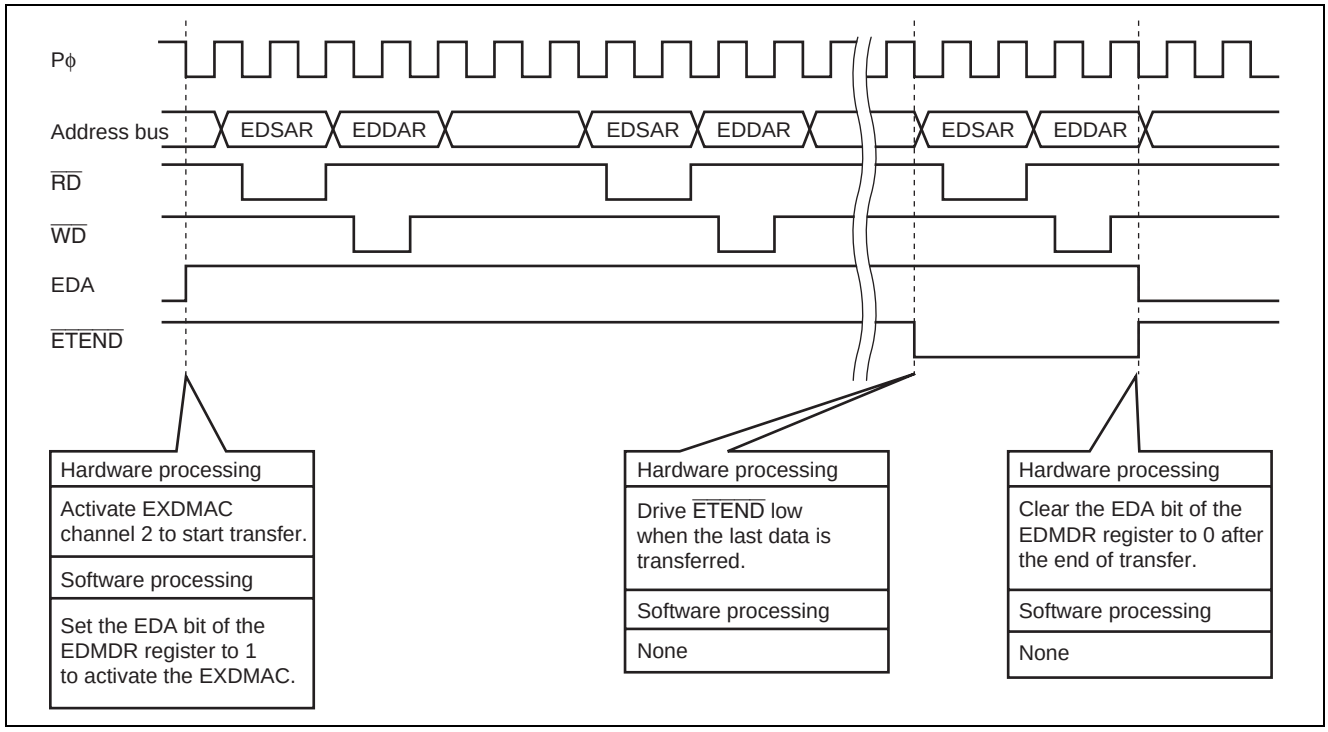


Figure 3 Example of Normal Transfer Operation

5. Description of Software

5.1 List of Functions

Table 4 List of Functions

Function Name	Function
init	Initialization routine Sets CCR, configures clocks, cancels module stop modes, and calls the BscInit and main functions.
BscInit	BSC setting Configures the bus.
main	Main routine Configures transfer functions and starts transfer.

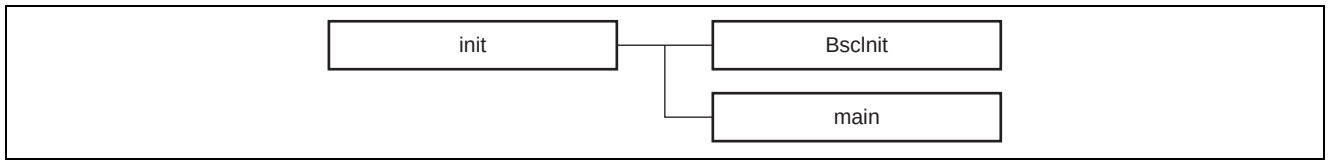


Figure 4 Hierarchy of Functions

5.2 Arguments

No argument is used in this sample task.

5.3 Internal registers

This section describes the internal registers used in this sample task.

- System Clock Control Register (SCKCR) Address: H'FFFF3B

Bit	Bit Name	Setting	Function
2	SCK2	0	System clock select 2, 1, 0
1	SCK1	0	000: Division ratio is 1/1.
0	SCK0	0	

- PLL Control Register (PLLCR) Address: H'FFFF45

Bit	Bit Name	Setting	Function
1	STC1	0	Frequency multiplication factor setting
0	STC0	0	00: Frequency multiplication factor of the PLL circuit is ×1.

- Module Stop Control Register H, L (MSTPCRH, MSTPCRL) Address: H'FFFF40, H'FFFF41

Bit	Bit Name	Setting	Function
15	ACSE	0	All-module-clocks-stop mode enable 0: Disables all-module-clocks-stop mode. 1: Enables all-module-clocks-stop mode.
14	MSTP14	0	EXDMA controller (EXDMA) 0: Cancels module stop mode. 1: Sets module stop mode.
13	MSTP13	0	DMA controller (DMAC) 0: Cancels module stop mode. 1: Sets module stop mode.
12	MSTP12	0	Data transfer controller (DTC) 0: Cancels module stop mode. 1: Sets module stop mode.
11	MSTP11	0	16-bit timer pulse unit (TPU) 0: Cancels module stop mode. 1: Sets module stop mode.
10	MSTP10	0	Programmable pulse generator (PPG) 0: Cancels module stop mode. 1: Sets module stop mode.
9	MSTP9	0	D/A converter (channels 0, 1) 0: Cancels module stop mode. 1: Sets module stop mode.
8	MSTP8	0	D/A converter (channels 2, 3) 0: Cancels module stop mode. 1: Sets module stop mode.
7	MSTP7	0	D/A converter (channels 4, 5) 0: Cancels module stop mode. 1: Sets module stop mode.
6	MSTP6	0	A/D converter 0: Cancels module stop mode. 1: Sets module stop mode.
5	MSTP5	0	Serial communication interface 4 (SCI_4) 0: Cancels module stop mode. 1: Sets module stop mode.
4	MSTP4	0	Serial communication interface 3 (SCI_3) 0: Cancels module stop mode. 1: Sets module stop mode.
3	MSTP3	0	Serial communication interface 2 (SCI_2) 0: Cancels module stop mode. 1: Sets module stop mode.
2	MSTP2	0	Serial communication interface 1 (SCI_1) 0: Cancels module stop mode. 1: Sets module stop mode.
1	MSTP1	0	Serial communication interface 0 (SCI_0) 0: Cancels module stop mode. 1: Sets module stop mode.
0	MSTP0	0	8-bit timer (TMR) 0: Cancels module stop mode. 1: Sets module stop mode.

- Extension Module Stop Control Register H, L (EXMSTPCRH, EXMSTPCRL)

Address: H'FFFF42, H'FFFF43

Bit	Bit Name	Setting	Function
4	MSTP20	0	I^2C bus interface 2_1 (IIC2_1) 0: Cancels module stop mode. 1: Sets module stop mode.
3	MSTP19	0	I^2C bus interface 2_0 (IIC2_0) 0: Cancels module stop mode. 1: Sets module stop mode.

- System Control Register (SYSCR) Address: H'FFFF3D

Bit	Bit Name	Setting	Function
7	RAME	1	RAM enable 0: Disables the on-chip RAM. 1: Enables the on-chip RAM.

- Port Function Control Register 0 (PFCR0) Address: H'FFFE32

Bit	Bit Name	Setting	Function
7	CS7E	1	CS7 to CS0 enable
6	CS6E	1	Each bit of this register enables/disables the corresponding $\overline{CSn}$
5	CS5E	1	output.
4	CS4E	1	0: The pin functions as an I/O port pin.
3	CS3E	1	1: The pin functions as the $\overline{CSn}$ output pin. (n = 7 to 0)
2	CS2E	1	
1	CS1E	1	
0	CS0E	1	

- Port Function Control Register 1 (PFCR1) Address: H'FFFE33

Bit	Bit Name	Setting	Function
7	A23E	1	Address A23 to A16 enable
6	A22E	1	Each bit of this register enables/disables the corresponding address
5	A21E	1	output (A23 to A16).
4	A20E	1	0: Outputs DR when PAnDDR = 1. (n = 7 to 0)
3	A19E	1	1: Outputs Amm when PAnDDR = 1. (n = 7 to 0, mm = 23 to 16)
2	A18E	1	
1	A17E	1	In this sample task, PFCR1 is set to H'FF to enable address outputs
0	A16E	1	A23 to A16.

- Port Function Control Register 2 (PFCR2) Address: H'FFFE34

Bit	Bit Name	Setting	Function
3	ASOE	1	AS output enable 0: PF6 functions as an I/O port pin. 1: PF6 functions as the $\overline{AS}$ output pin.
2	LWROE	1	LWR output enable 0: PF3 functions as an I/O port pin. 1: PF3 functions as the $\overline{LWR}$ output pin.

- Port A data direction register (PADDR) Address: H'FFFE29
  Function: Sets the PA7 to PA0 pins to function as address output pins.
  Setting: H'FF
- Port B data direction register (PBDDR) Address: H'FFFE2A
  Function: Sets the PB7 to PB0 pins to function as address output pins.
  Setting: H'FF
- Port C data direction register (PCDDR) Address: H'FFFE2B
  Function: Sets the PC7 to PC0 pins to function as address output pins.
  Setting: H'FF
- Port F data direction register (PFDDR) Address: H'FFFE2E
  Function: Sets the PF7 pin to output ϕ, and PF6 to PF0 to function as input pins.
  Setting: H'80
- Port G data direction register (PGDDR) Address: H'FFFE2F
  Function: Sets the PG3 to PG0 pins to function as the $\overline{CS3}$ to $\overline{CS0}$ input pins.
  Setting: H'0F
- Port H data direction register (PHDDR) Address: H'FFFF74
  Function: Sets the PH3 to PH0 pins to function as the $\overline{CS7}$ to $\overline{CS4}$ input pins.
  Setting: H'0F
- Bus width control register (ABWCR) Address: H'FFFEC0
  Function: Designates areas 7 to3, 1, 0 as 16-bit access space and area 2 as 8-bit access space.
  Setting: H'04
- Access state control register (ASTCR) Address: H'FFFEC1
  Function: Designates areas 7 to 0 as 3-state access space
  Setting: H'FF
- Wait control register A (WTCRA) Address: H'FFFEC2
  Function: Selects the number of program wait states to be inserted: 7 states for areas 7 and 6, and 3 states for areas 5 and 4.
  Setting: H'7733
- Wait control register B (WTCRB) Address: H'FFFEC4
  Function: Selects the number of program wait states to be inserted: 1 state for areas 3 and 2, and 2 states for areas 1 and 0.
  Setting: H'1122

- Read strobe timing control register (RDNCR) Address: H'FFFEC6
  Function: Sets so that, in read access to areas 7 to 0, RD is negated at the end of the read cycle.
  Setting: H'00

- Bus control register (BCR) Address: H'FFFECC

Bit	Bit Name	Setting	Function
15	BRLE	0	External bus release enable 0: Disables external bus release. 1: Enables external bus release.
12	IDLC	1	Select number of states in idle cycle Specifies the number of states in the idle cycles set by ICIS2, ICIS1 and ICIS0 0: One state. 1: Two states.
11	ICIS1	1	Idle cycle insertion 1 When consecutive external read cycles are executed in different areas, an idle cycle can be inserted between the bus cycles. 0: Idle cycle not inserted 1: Idle cycle inserted
10	ICIS0	1	Idle cycle insertion 0 When an external read cycle and external write cycle are performed consecutively, an idle cycle can be inserted between the bus cycles. 0: Idle cycle not inserted 1: Idle cycle inserted
8	WAITE	1	$\overline{\text{WAIT}}$ pin enable 0: Disables wait insertion by the $\overline{\text{WAIT}}$ pin. The $\overline{\text{WAIT}}$ pin can be used as an I/O port pin. 1: Enables wait insertion by the $\overline{\text{WAIT}}$ pin.
2	ICIS2	0	Idle cycle insertion 2 When an external write cycle and external read cycle are performed consecutively, an idle cycle can be inserted between the bus cycles. 0: Idle cycle not inserted 1: Idle cycle inserted

- EXDMA source address register 2 (EDSAR_2) Address: H'FFFDE0
  Function: Sets the transfer source address.
  Setting: H'00200000
- EXDMA destination address register 2 (EDDAR_2) Address: H'FFFDE4
  Function: Sets the transfer destination address.
  Setting: H'00400000
- EXDMA transfer count register 2 (EDTCR_2) Address: H'FFFDE8
  Function: Sets the transfer source address.
  Setting: H'00200000
- EXDMA mode control register 2 (EDMDR_2) Address: H'FFFDEC

Bit	Bit Name	Setting	Description
15	EDA	0	EXDMA active 0: Disables data transfer. 1: Enables data transfer.
10	AMS	0	Address mode select 0: Dual-address mode 1: Single-address mode
9	MDS1	0	Mode select 1, 0
8	MDS0	0	00: Auto-request, cycle steal mode, normal transfer mode
3	DTSIZE	0	Data transmit size 0: One byte 1: One word

- EXDMA address control register 2 (EDACR_2) Address: H'FFFDEE

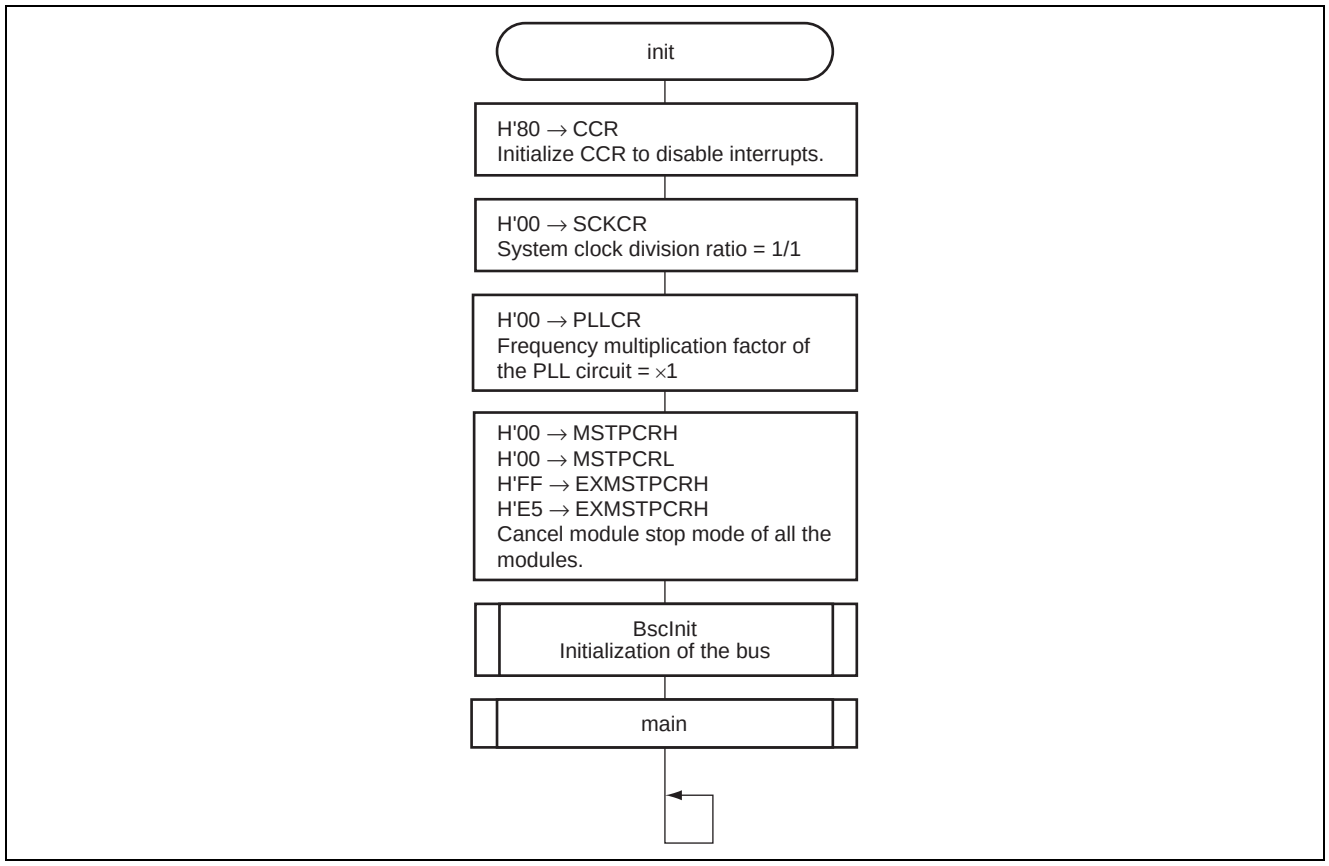
Bit	Bit Name	Setting	Description
15	SAT1	1	Source address update mode
14	SAT0	0	10: Source address is incremented.
7	DAT1	1	Destination address update mode
6	DAT0	0	10: Destination address is incremented.

5.4 RAM Usage

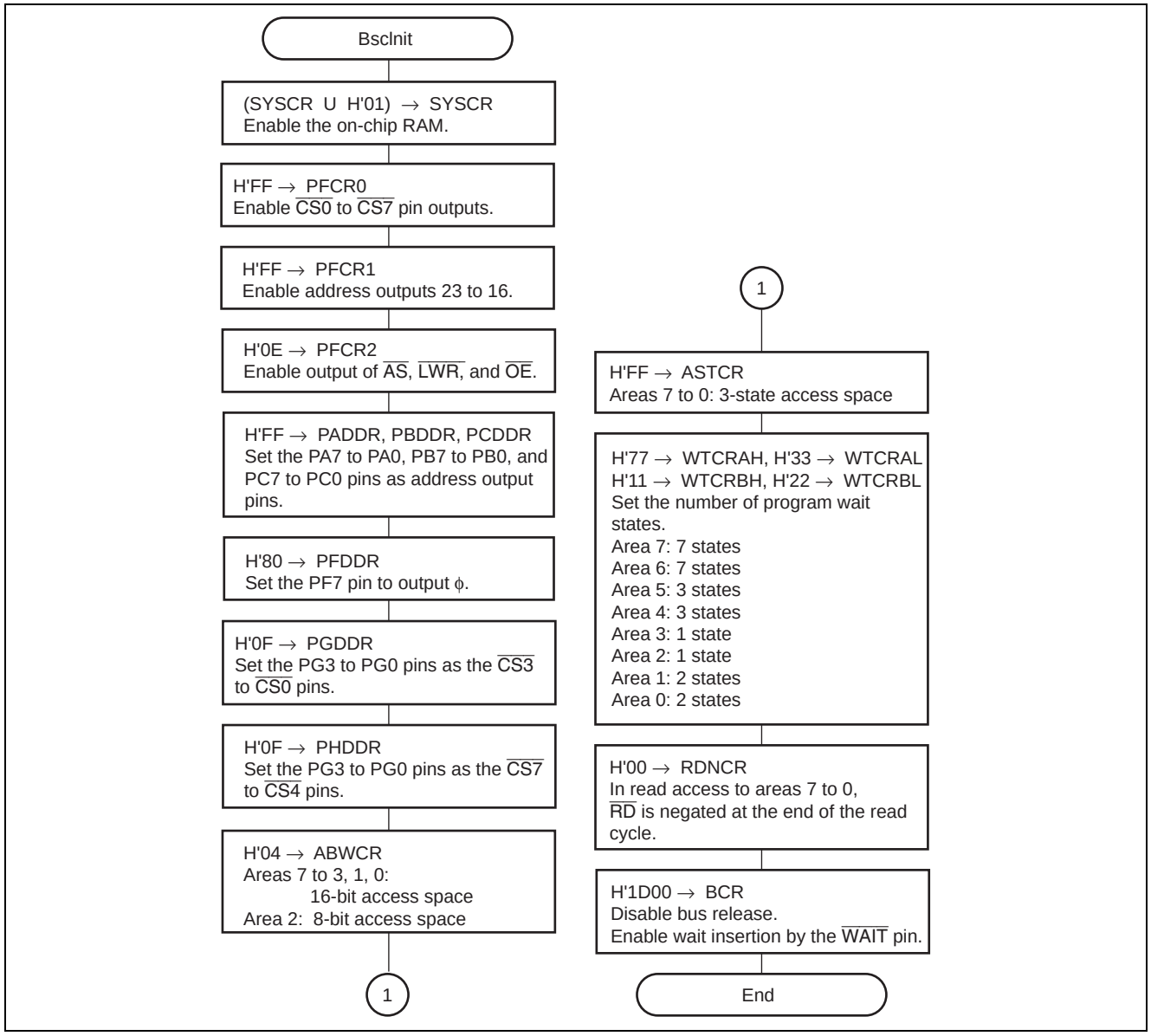
This sample task does not use RAM.

6. Flowchart

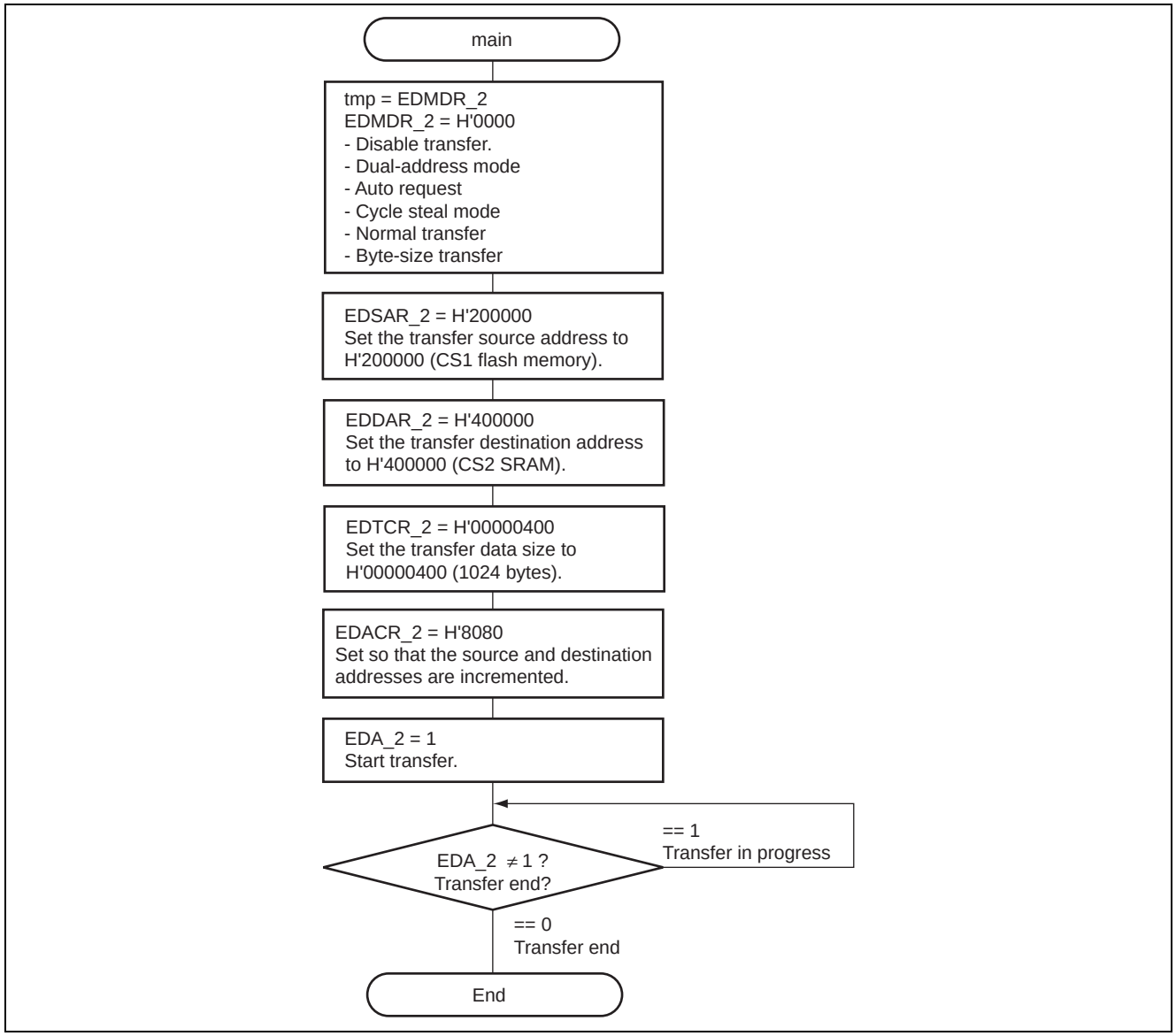
6.1 init Function



6.2 Bsclnit Function



6.3 main Function



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