RX230/RX231 Group, RX630 Group

Points of Difference Between RX231 Group and RX630 Group

Summary

This application note is intended principally as a reference providing an overview of the peripheral functions of the RX231 Group and RX630 Group, to enable checking of the points of difference between the I/O registers and pin functions of the two groups, and to allow confirmation of key points related to migration.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin LQFP package version B of the RX231 Group and the 100-pin LQFP package version of the RX630 Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX231 Group and RX630 Group

Contents

1. Comparison of Functions of RX231 Group and RX630 Group

A comparison of the functions of the RX231 Group and RX630 Group is provided below. For details of the functions, see 2, Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX231 and RX630.

Table 1.1 Comparison of Functions of RX231 and RX630

Function	RX630	RX231
CPU	△	△
Operating mode	△	△
Address Space	△	△
Resets	△	△
Option-setting memory	△	△
Voltage detection circuit (LVDA): RX630, (LVDAb): RX231	△	△
Clock generation circuit	△	△
Frequency measurement circuit (MCK)	○	×
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	△	△
Battery backup function	△	△
Register write protection function	△	△
Exception handling	△	△
Interrupt controller (ICUb)	△	△
Buses		
Memory-protection unit (MPU)	○	○
DMA controller (DMACA)		
Data transfer controller (DTCa)		
Event link controller (ELC)	×	○
I/O ports		
Multi-function pin controller (MPC)		
Multi-function timer pulse unit 2 (MTU2a)		
Port output enable 2 (POE2a)		
16-bit timer pulse unit (TPUa)		
Programmable pulse generator (PPG)	○	×
8-bit timer (TMR)		
Compare match timer (CMT)		
Realtime clock (RTCa): RX630, (RTCe): RX231		
Low-power timer (LPT)	×	○
Watchdog timer (WDTA)	○	○
Independent watchdog timer (IWDTa)		
USB 2.0 function module (USBa): RX630 USB 2.0 host/function module (USBd): RX231		
Serial communications interface (SCIc, SCId): RX630 Serial communications interface (SCIg, SCIh): RX231		
IrDA interface	×	○
I²C bus interface (RIIC): RX630, (RIICa): RX231		
CAN module (CAN): RX630, (RSCAN): RX231		
Serial sound interface (SSI)	×	○
Serial peripheral interface (RSPI): RX630, (RSPIa): RX231		
IEbus™ controller (IEB)	○	×
CRC calculator (CRC)	○	○

Function	RX630	RX231
SD host interface (SDHIa)	×	○
Security functions	×	○
Capacitive touch sensing unit (CTSU)	×	○
12-bit A/D converter (S12ADa): RX630, (S12ADE): RX231		
10-bit A/D converter (ADb)	○	×
D/A converter (DAa): RX630 12-bit D/A converter (R12DAA): RX231		
Temperature sensor: RX630, (TEMPSA): RX231		
Comparator B (CMPBa)	×	
Data operation circuit (DOC)	×	
RAM		
Flash memory (ROM)		
Flash memory (E2 DataFlash)		
Boundary scan		×
Package (LQFP100 only)		

Note:  : Function implemented, ×: Function not implemented,
 : Differences exist between implementation of function on RX630 and RX231.

2. Comparative Overview of Functions

2.1 CPU

Table 2.1 shows a comparative overview of the CPU specifications, and Table 2.2 shows a comparative overview of CPU registers.

Table 2.1 Comparative Overview of CPU Specifications

Item	RX630	RX231
Central processing unit	• Maximum operating frequency: 100 MHz • 32-bit RX CPU (RX) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 9 control registers (32 bits) 1 accumulator (64 bits) • 73 basic instructions • 8 floating-point instructions • 9 DSP instructions • 10 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 54 MHz • 32-bit RX (RXv2) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 10 control registers (32 bits) 2 accumulators (72 bits) • 75 basic instructions • 11 floating-point instructions • 23 DSP instructions • 11 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and exceptions in conformance with the IEEE754 standard

Table 2.2 Comparative Overview of CPU Registers

Register	Bit	RX630	RX231
EXTB	-	-	Exception Table Register
ACC	-	ACC: 64-bits (DSP, multiply and multiply-and-accumulate)	ACC0: 72-bits (DSP, multiply and multiply-and-accumulate) ACC1: 72-bits (DSP)

2.2 Operating Modes

Table 2.3 shows a comparative overview of the operating mode specifications, and Table 2.4 shows a comparative overview of the operating mode registers.

Table 2.3 Comparative Overview of Operating Modes Specifications

Item	RX630	RX231
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	User boot mode	—
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.4 Comparative Overview of Operating Mode Registers

Register	Bit	RX630	RX231
MDSR	—	Mode status register	—

2.3 Address Space

Figure 2.1 to Figure 2.3 shows the memory maps in the respective operating modes.

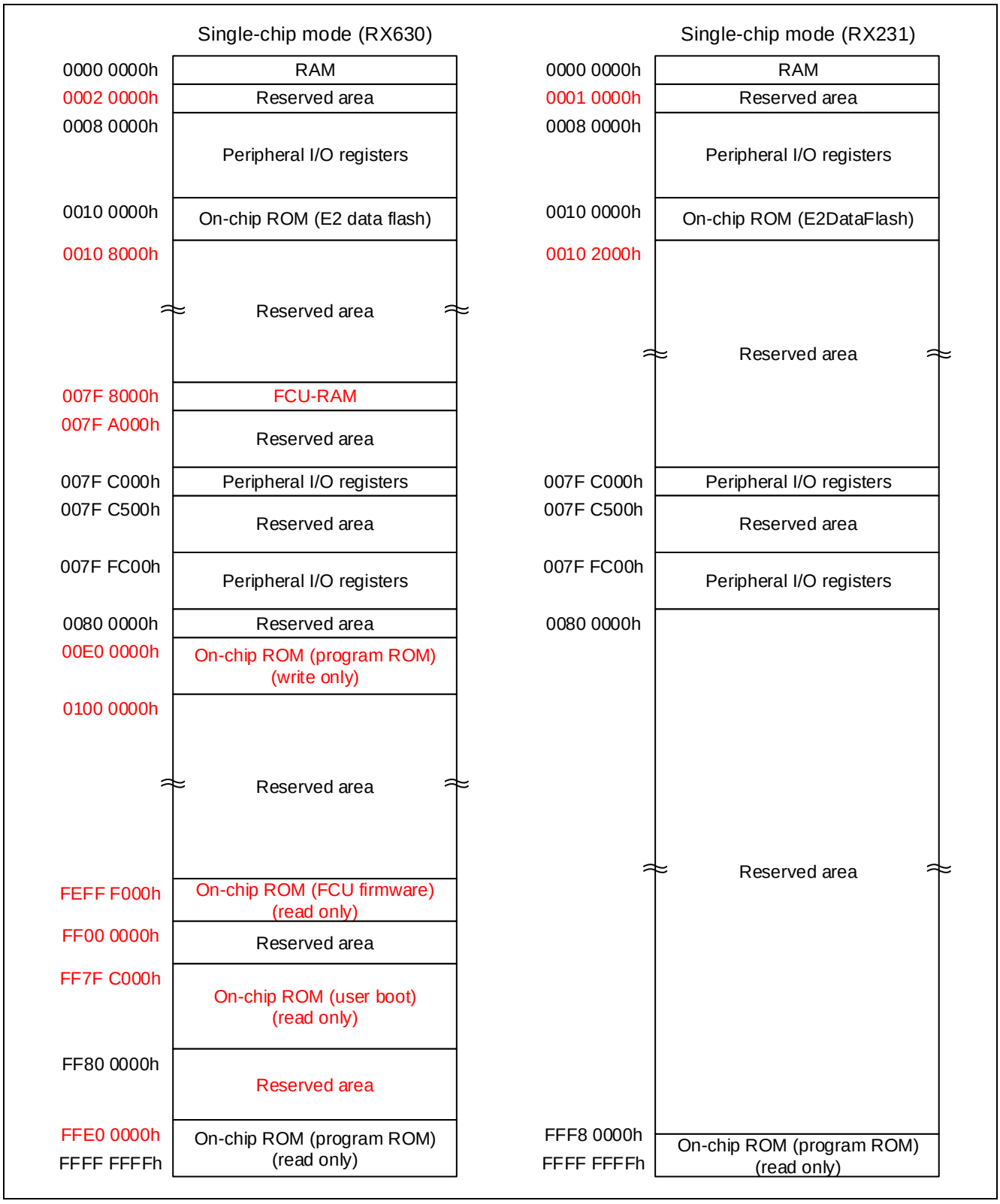

Figure 2.1 Memory Map in Each Operating Mode (Single-chip mode)

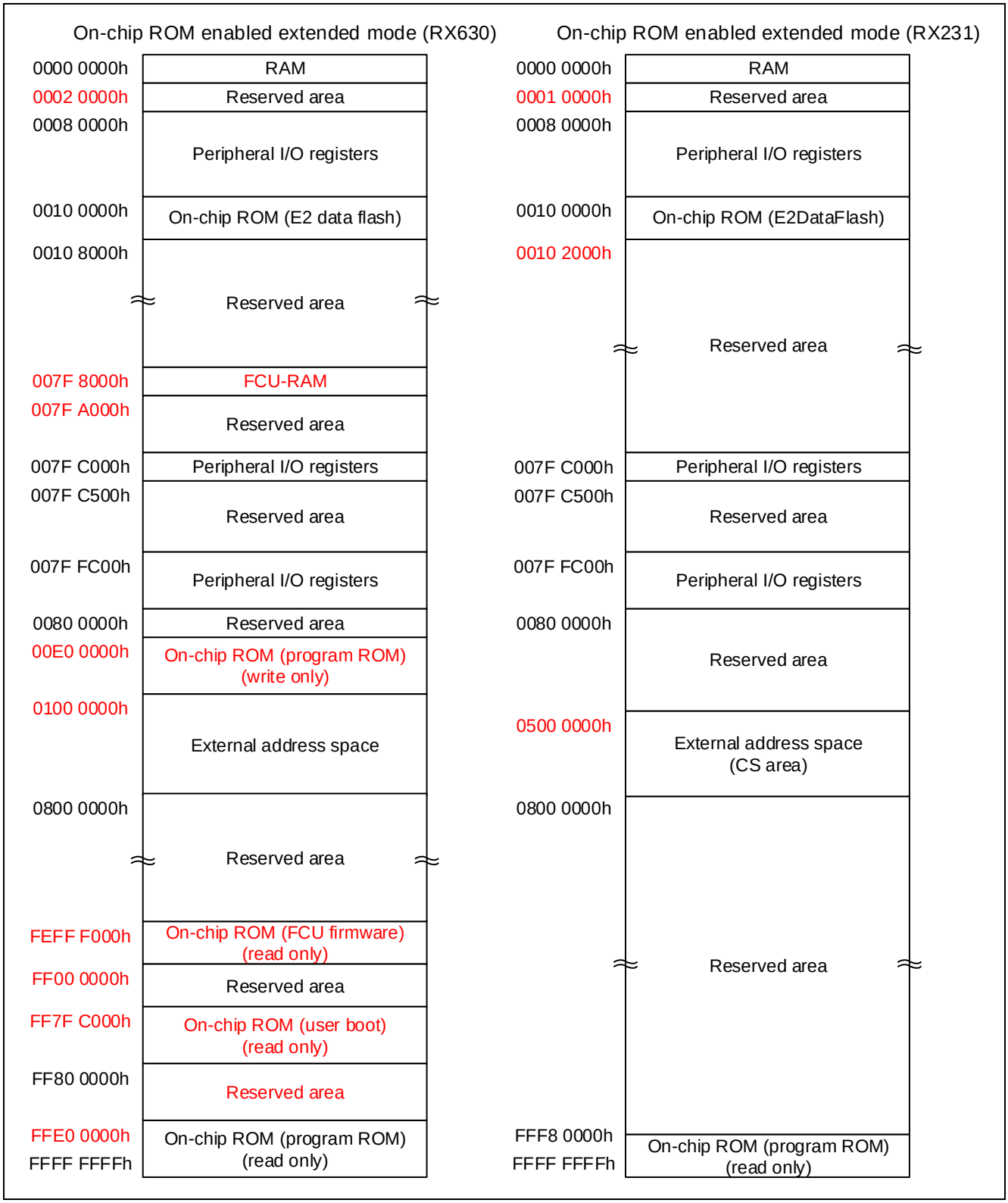

Figure 2.2 Memory Map in Each Operating Mode (On-chip ROM enabled extended mode)

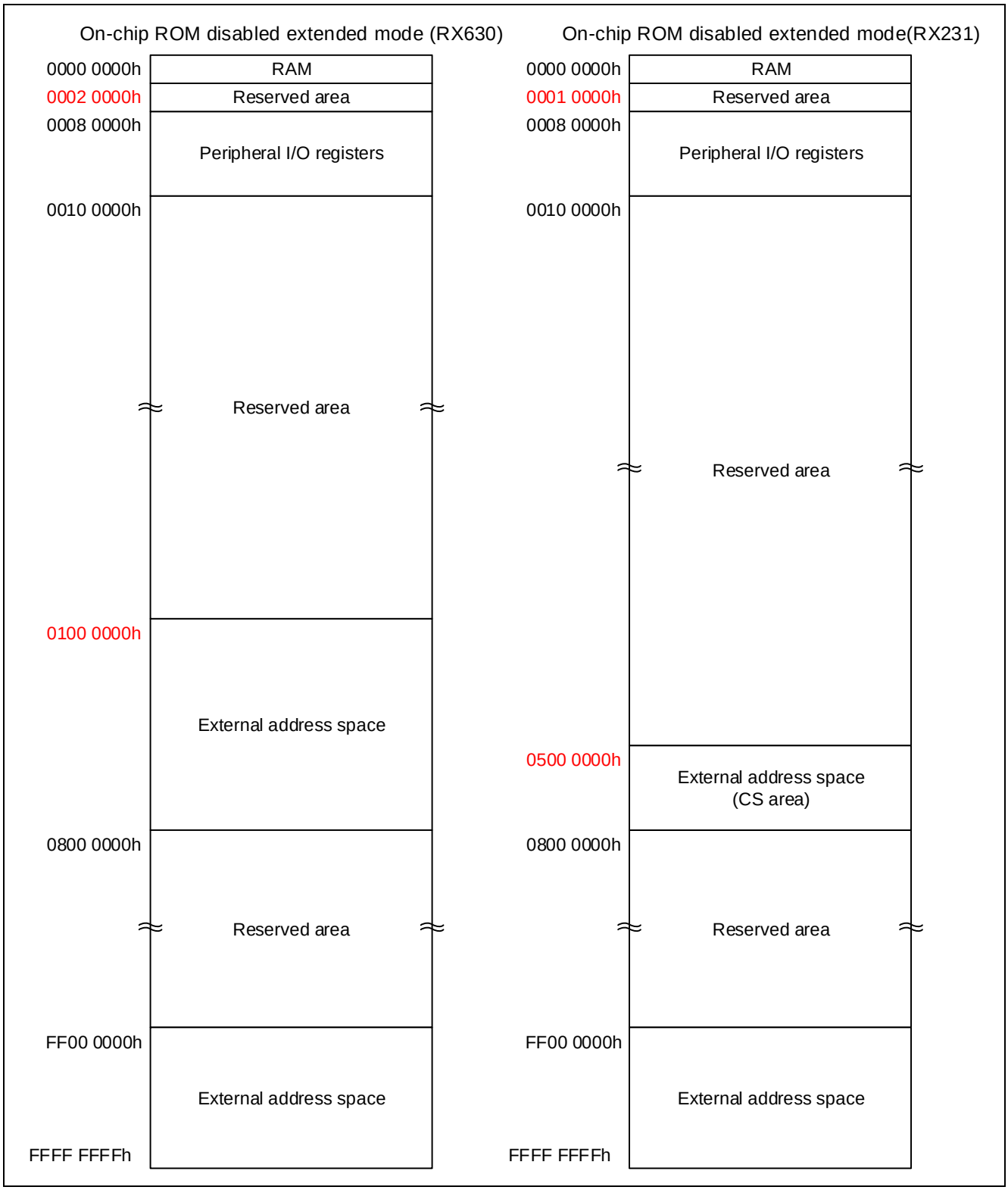

Figure 2.3 Memory Map in Each Operating Mode (On-chip ROM disabled extended mode)

2.4 Resets

Table 2.5 shows a comparative overview of the reset specifications, and Table 2.6 shows a comparative overview of the reset registers.

Table 2.5 Comparative Listing of Reset Specifications

Item	RX630	RX231
Reset sources	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	Voltage monitoring 0 reset	Voltage monitoring 0 reset
	Voltage monitoring 1 reset	Voltage monitoring 1 reset
	Voltage monitoring 2 reset	Voltage monitoring 2 reset
	Deep software standby reset	—
	Independent watchdog timer reset	Independent watchdog timer reset
	Watchdog timer reset	Watchdog timer reset
	Software reset	Software reset

Table 2.6 Comparative Listing of Reset Registers

Register	Bit	RX630	RX231
RSTSR0	DPSRSTF	Deep software standby reset flag	—

2.5 Option-Setting Memory

Table 2.7 shows a comparative overview of the option-setting memory registers, and Figure 2.4 shows a comparative of the option-setting memory.

Table 2.7 Comparative Overview of Option-Setting Memory Registers

Register	Bit	RX630	RX231
OFS0	IWDTTOPS [1:0]	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	IWDTCKS [3:0]	IWDT timeout period select bits b7 b4 0 0 0 0: ×1 (cycle period: 131 ms) 0 0 1 0: ×16 (cycle period: 2.10 sec.) 0 0 1 1: ×32 (cycle period: 4.19 sec.) 0 1 0 0: ×64 (cycle period: 8.39 sec.) 1 1 1 1: ×128 (cycle period: 16.8 sec.) 0 1 0 1: ×256 (cycle period: 33.6 sec.)	IWDT timeout period select bits b7 b4 0 0 0 0: ×1 (cycle period: 136 ms) 0 0 1 0: ×16 (cycle period: 2.18 sec.) 0 0 1 1: ×32 (cycle period: 4.36 sec.) 0 1 0 0: ×64 (cycle period: 8.73 sec.) 1 1 1 1: ×128 (cycle period: 17.5 sec.) 0 1 0 1: ×256 (cycle period: 34.9 sec.)
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
	FASTSTUP	—	Power-on fast startup time bit
MDES: RX630 MDE: RX231	MDE[2:0]	Endian select register S	Endian select register
MDEB	MDE[2:0]	Endian select register B	—
UB code A	—	Codes required when using user boot mode	—
UB code B	—		—

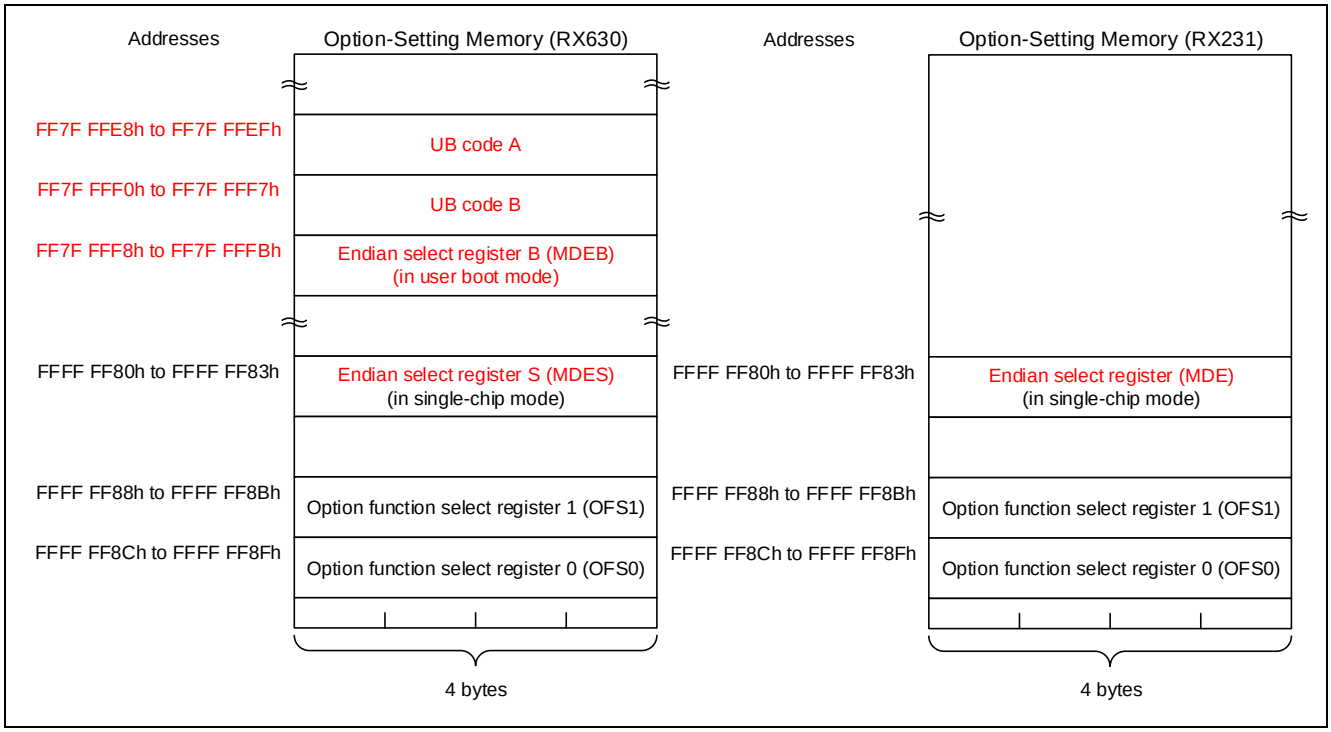

Figure 2.4 Comparative of Option-Setting Memory

2.6 Voltage Detection Circuit

Table 2.8 shows a comparative overview of the voltage detection circuit specifications, and Table 2.9 shows a comparative overview of the voltage detection circuit registers.

Table 2.8 Comparative overview of Voltage Detection Circuit Specifications

Item		RX630 (LVDA)			RX231 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
				—			Selectable between VCC and CMPA2 pin input voltage using LVCMPCR.EXVCCINP2 bit.
	Detection voltage	One level fixed	Specify voltage using LVDLVLR.LVD1LVL[3:0] bits	Specify voltage using LVDLVLR.LVD2LVL[3:0] bits	Selectable from four levels using OFS1 register.	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin.

Item		RX630 (LVDA) Voltage Monitoring 0	RX630 (LVDA) Voltage Monitoring 1	RX630 (LVDA) Voltage Monitoring 2	RX231 (LVDAb) Voltage Monitoring 0	RX231 (LVDAb) Voltage Monitoring 1	RX231 (LVDAb) Voltage Monitoring 2
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin and when VCC or CMPA2 pin > Vdet2, or one or the other.
Digital filter	Enable/ disable switching	—	Available	Available	—	—	—
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	—	—
Event link function		—	—	—	—	Available: Vdet1 pass-through detection event output	Available: Vdet2 pass-through detection event output

Table 2.9 Comparative Overview of Voltage Detection Circuit Registers

Register	Bit	RX630 (LVDA)	RX231 (LVDAb)
LVD1CR1	LVD1IRQSEL	—	Voltage monitoring 1 interrupt type select bit
LVD2CR1	LVD2IDTSEL [1:0]	Voltage Monitoring 2 Interrupt Generation Condition Select b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Settings prohibited	Voltage Monitoring 2 Interrupt ELC Event Generation Condition Select b1 b0 0 0: When VCC or the CMPA2 pin ≥ Vdet2 (rise) is detected 0 1: When VCC or the CMPA2 pin < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited
	LVD2IRQSEL	—	Voltage monitoring 2 interrupt type select bit
LVD2SR	LVD2MON	Voltage Monitoring 2 Signal Monitor Flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	Voltage Monitoring 2 Signal Monitor Flag 0: VCC or the CMPA2 pin < Vdet2 1: VCC or the CMPA2 pin ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVCCINP2	—	Voltage detection 2 comparison voltage external input select bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 1 0 1 0: 2.95 V Do not set to values other than the above.	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Do not set to values other than the above.
		Initial value after a reset is different.	

Register	Bit	RX630 (LVDA)	RX231 (LVDAb)
	LVD2LVL[3:0]: RX630 LVD2LVL[1:0]: RX231	Voltage detection 2 level select bits (standard voltage during drop in voltage) b7 b4 1 0 1 0: 2.95 V Do not set to values other than the above.	Voltage detection 2 level select bits (standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V
		Initial value after a reset is different.	
LVD1CR0	LVD1DFDIS	Voltage monitoring 1 digital filter disable mode select bit	—
	LVD1FSAMP[1:0]	Sampling clock select bits	—
LVD2CR0	LVD2DFDIS	Voltage monitoring 2 digital filter disable mode select bit	—
	LVD2FSAMP[1:0]	Sampling clock select bits	—
	LVD2RN	Voltage monitoring 2 reset negation select bit 0: Negation follows stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows stabilization time (tLVD2) after assertion of LVD2 reset.	Voltage monitoring 2 reset negation select bit 0: Negation follows stabilization time (tLVD2) after VCC or CMPA2 pin > Vdet2 is detected. 1: Negation follows stabilization time (tLVD2) after assertion of LVD2 reset.

2.7 Clock Generation Circuit

Table 2.10 shows a comparative overview of the clock generation circuit specifications, and Table 2.11 shows a comparative overview of the clock generation circuit registers.

Table 2.10 Comparative Overview of Clock Generation Circuit Specifications

Item	RX630	RX231
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB) supplied to the peripheral modules. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the IEBUS clock (IECLK) to be supplied to the IEBUS. • Generates the RTC-dedicated sub-clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the MTU2. • Generates the peripheral module clocks (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (PCLKD) to be supplied to the S12ADC. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAN clock (CANMCLK) supplied to the RSCAN. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the SSI clock (SSISCK) supplied to the SSI. • Generates the LPT clock (LPTCLK) supplied to the LPT.

Item	RX630	RX231
Operating frequencies	• ICLK: 100 MHz (max.) • PCLKB: 50 MHz (max.) • FCLK: 4 MHz to 50 MHz (for programming and erasing the ROM and E2 DataFlash) 50 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 50 MHz (max.) • BCLK pin output: 25 MHz (max.) • UCLK: 48 MHz (max.) • CANMCLK: 20 MHz (max.) • IECLK: 50 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 4 MHz to 16 MHz • IWDTCLK: 125 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz • CANMCLK: 20 MHz (max.) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • SSISCK: 20 MHz (max.) • LPTCLK: Same frequency as selected oscillator
Main clock oscillator	• Resonator frequency: 4 MHz to 16 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function

Item	RX630	RX231
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 16 MHz • Frequency multiplication ratio: Selectable within range from 8, 10, 12, 16, 20, 24, 25, 50 • VCO oscillation frequency: 104 MHz to 200 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable within range from 4 to 13.5 (increments of 0.5) • Oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)
USB-dedicated PLL circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 6 MHz, 8 MHz, 12 MHz • Frequency multiplication ratio: Selectable within range from 4, 6, 8, 12 • Oscillation frequency: 48 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 50 MHz • HOCO power supply control	• Oscillation frequency: 32 MHz and 54 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max.)	—
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock

Table 2.11 Comparative Overview of Clock Generation Circuit Registers

Register	Bit	RX630	RX231
SCKCR	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
SCKCR2	—	System clock control register 2	—
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×8 0 0 1 0 0 0: ×10 0 0 1 0 1 1: ×12 0 0 1 1 1 1: ×16 0 1 0 0 1 1: ×20 0 1 0 1 1 1: ×24 0 1 1 0 0 0: ×25 1 1 0 0 0 1: ×50 Do not set to values other than the above.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 . . . 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 Do not set to values other than the above.
		Initial value after a reset is different.	
UPLLCR	—	—	USB-dedicated PLL control register
UPLLCR2	—	—	USB-dedicated PLL control register 2
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register

Register	Bit	RX630	RX231
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time select bits b4 b0 Wait time 0 0 0 0 0: 2 cycles 0 0 0 0 1: 4 cycles 0 0 0 1 0: 8 cycles 0 0 0 1 1: 16 cycles 0 0 1 0 0: 32 cycles 0 0 1 0 1: 64 cycles 0 0 1 1 0: 512 cycles 0 0 1 1 1: 1,024 cycles 0 1 0 0 0: 2,048 cycles 0 1 0 0 1: 4,096 cycles 0 1 0 1 0: 16,384 cycles 0 1 0 1 1: 32,768 cycles 0 1 1 0 0: 65,536 cycles 0 1 1 0 1: 131,072 cycles 0 1 1 1 0: 262,144 cycles 0 1 1 1 1: 524,288 cycles Do not set to values other than the above.	Main clock oscillator wait time select bits b4 b0 Wait time 0 0 0 0 0: 2 cycles 0 0 0 0 1: 1,024 cycles 0 0 0 1 0: 2,048 cycles 0 0 0 1 1: 4,096 cycles 0 0 1 0 0: 8,192 cycles 0 0 1 0 1: 16,384 cycles 0 0 1 1 0: 32,768 cycles 0 0 1 1 1: 65,536 cycles Do not set to values other than the above.
		Initial value after a reset is different.	
SOSCWTCR	—	Sub-clock oscillator wait control register	—
CKOCR	—	—	CLKOUT output control register
MOFCR	MOFXIN	Main clock oscillator forced oscillation bit	—
	MODRV21	—	Main clock oscillator drive capability switch bit
	MOSEL	—	Main clock oscillator switch bit
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—
MEMWAIT	—	—	Memory wait cycle setting register
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0 or 3)

2.8 Low Power Consumption Functions

Table 2.12 shows a comparative overview of the low power consumption function specifications, Table 2.13 to Table 2.17 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.18 shows a comparative overview of the low power consumption function registers.

Table 2.12 Comparative Overview of Low Power Consumption Functions Specifications

Item	RX630	RX231
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and Flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.13 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX231
	Sleep Mode	Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	—	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	Operating possible (Retained)	—
RAM0 (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	Operating possible (Retained)
DMAC	Operating possible	Operating possible
DTC	Operating possible	Operating possible
Flash memory	Operating	Operating
USB 2.0 function module (USB)	Operating possible	Operating possible
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	Operating possible	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.14 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (All-Module Clock Stop Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX231
	All-Module Clock Stop Mode	All-Module Clock Stop Mode
Entry trigger	Control register + instruction	—
Exit trigger	Interrupt	—
After exiting from each mode, CPU begins from	Interrupt handling	—
Main clock oscillator	Operating possible	—
Sub-clock oscillator	Operating possible	—
High-speed on-chip oscillator	Operating possible	—
Low-speed on-chip oscillator	Operating possible	—
IWDT-dedicated on-chip oscillator	Operating possible	—
PLL	Operating possible	—
USB-dedicated PLL	—	—
CPU	Stopped (Retained)	—
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	—
DMAC	Stopped (Retained)	
DTC	Stopped (Retained)	—
Flash memory	Stopped (Retained)	—
USB 2.0 function module (USB)	Stopped	—
Watchdog timer (WDT)	Stopped (Retained)	—
Independent watchdog timer (IWDT)	Operating possible	—
Realtime clock (RTC)	Operating possible	—
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
Low power timer (LPT)	—	—
Voltage detection circuit (LVD)	Operating possible	—
Power-on reset circuit	Operating	—
Peripheral modules	Stopped (Retained)	—
I/O ports	Retained	—
RTCOUT	Operating possible	—
CLKOUT	—	—
Comparator B	—	—

Table 2.15 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 Software Standby Mode	RX231 Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Stopped
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
USB-dedicated PLL	—	Stopped
CPU	Stopped (Retained)	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained)	—
RAM (0000 0000h to 0000 FFFFh)	—	Stopped (Retained)
DMAC	Stopped (Retained)	Stopped (Retained)
DTC	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
USB 2.0 function module (USB)	Stopped	Stopped (Retained)
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	Stopped (Retained)
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained
RTCOUT	Operating possible	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.16 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630	RX231
	Deep Software Standby Mode	Deep Software Standby Mode
Entry trigger	Control register + instruction	—
Exit trigger	Interrupt	—
After exiting from each mode, CPU begins from	Interrupt handling	—
Main clock oscillator	Operating possible	—
Sub-clock oscillator	Operating possible	—
High-speed on-chip oscillator	Stopped	—
Low-speed on-chip oscillator	Stopped	—
IWDT-dedicated on-chip oscillator	Stopped (Undefined)	—
PLL	Stopped	—
USB-dedicated PLL	—	—
CPU	Stopped (Undefined)	—
RAM1 (0001 0000h to 0001 FFFFh)	Stopped (Undefined)	—
RAM0 (0000 0000h to 0000 FFFFh)	Stopped (Retained/Undefined)	—
RAM (0000 0000h to 0000 FFFFh)	—	—
DMAC	Stopped (Undefined)	—
DTC	Stopped (Undefined)	—
Flash memory	Stopped (Retained)	—
USB 2.0 function module (USB)	Stopped (Retained/Undefined)	—
Watchdog timer (WDT)	Stopped (Undefined)	—
Independent watchdog timer (IWDT)	Stopped (Undefined)	—
Realtime clock (RTC)	Operating possible	—
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Undefined)	—
Low power timer (LPT)	—	—
Voltage detection circuit (LVD)	Operating possible	—
Power-on reset circuit	Operating	—
Peripheral modules	Stopped (Undefined)	—
I/O ports	Retained	—
RTCOUT	Stopped	—
CLKOUT	—	—
Comparator B	—	—

Table 2.17 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX630 Deep Sleep Mode	RX231 Deep Sleep Mode
Entry trigger	—	Control register + instruction
Exit trigger	—	Interrupt
After exiting from each mode, CPU begins from	—	Interrupt handling
Main clock oscillator	—	Operating possible
Sub-clock oscillator	—	Operating possible
High-speed on-chip oscillator	—	Operating possible
Low-speed on-chip oscillator	—	Operating possible
IWDT-dedicated on-chip oscillator	—	Operating possible
PLL	—	Operating possible
USB-dedicated PLL	—	Operating possible
CPU	—	Stopped (Retained)
RAM1 (0001 0000h to 0001 FFFFh)	—	—
RAM0 (0000 0000h to 0000 FFFFh)	—	—
RAM (0000 0000h to 0000 FFFFh)	—	Stopped (Retained)
DMAC	—	Stopped (Retained)
DTC	—	Stopped (Retained)
Flash memory	—	Stopped (Retained)
USB 2.0 function module (USB)	—	Operating possible
Watchdog timer (WDT)	—	Stopped (Retained)
Independent watchdog timer (IWDT)	—	Operating possible
Realtime clock (RTC)	—	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	—	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	—	Operating possible
Power-on reset circuit	—	Operating
Peripheral modules	—	Operating possible
I/O ports	—	Operating
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.18 Comparative Overview of Low Power Consumption Function Registers

Register	Bit	RX630	RX231
SBYCR	OPE	Output port enable bit 0: In software standby mode or deep software standby mode, the address bus and bus control signals are set to the high-impedance state. 1: In software standby mode or deep software standby mode, the address bus and bus control signals retain the output state.	Output port enable 0: In software standby mode, the address bus and bus control signals are set to the high-impedance state. 1: In software standby mode, the address bus and bus control signals retain the output state.
	SSBY	Software standby bit 0: Transition to sleep mode or all-module clock stop mode after WAIT instruction is executed 1: Transition to software standby mode after WAIT instruction is executed	Software standby bit 0: Transition to sleep mode or deep sleep mode after WAIT instruction is executed 1: Transition to software standby mode after WAIT instruction is executed
MSTPCRA	MSTPA10	Programmable pulse generator (unit 1) module stop bit	—
	MSTPA11	Programmable pulse generator (unit 0) module stop bit	—
	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop bit	—
	MSTPA19	D/A converter module stop bit	12-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	—
	MSTPA24	module stop A24 bit	—
	MSTPA27	module stop A27 bit	—
	MSTPA29	module stop A29 bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB0	CAN module 0 module stop bit Target module: CAN0	RSCAN0 module stop bit Target module: RSCAN0
	MSTPB1	CAN module 1 module stop bit Target module: CAN1	—
	MSTPB2	CAN module 2 module stop bit Target module: CAN2	—
	MSTPB4	Serial Communication Interface SCId Module Stop Target module: SCId (SCI12) 0: The module-stop state is canceled 1: Transition to the module-stop state is made	Serial Communication Interface SCIh Module Stop Target module: SCIh (SCI12) 0: This module clock is enabled 1: This module clock is disabled
	MSTPB6	—	DOC module stop bit
	MSTPB8	Temperature sensor module stop bit	—
	MSTPB9	—	ELC module stop bit
	MSTPB10	—	Comparator B module stop bit
	MSTPB16	Serial peripheral interface 1 module stop bit	—

Register	Bit	RX630	RX231
	MSTPB20	I²C bus interface 1 module stop bit	—
	MSTPB24	Serial communication interface 7 module stop bit	—
	MSTPB27	Serial communication interface 4 module stop bit	—
MSTPCRB	MSTPB28	Serial communication interface 3 module stop bit	—
	MSTPB29	Serial communication interface 2 module stop bit	—
MSTPCRC	MSTPC1	RAM1 module stop bit	—
	MSTPC16	I²C bus interface 3 module stop bit	—
	MSTPC17	I²C bus interface 2 module stop bit	—
	MSTPC18	IEBUS module stop bit	—
	MSTPC19	Frequency measurement module stop bit	Clock frequency accuracy measurement circuit module stop bit
	MSTPC20	—	IrDA module stop bit
	MSTPC22	Serial peripheral interface 2 module stop bit	—
	MSTPC24	Serial communication interface 11 module stop bit	—
	MSTPC25	Serial communication interface 10 module stop bit	—
	DSLPE	—	Deep sleep mode enable bit
MSTPCRD	—	—	Module stop control register D
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed mode 1 1 0: Low-speed mode 1 1 1 1: Low-speed mode 2 Do not set to values other than the above.	Operating power control mode select bits b2 b0 0 0 0: High-speed mode 0 1 0: Middle-speed mode Do not set to values other than the above.
		Initial value after a reset is different.	
	OPCMTSF	Operating power control mode transition status flag Read 0: Transition completed 1: Transition in progress Write The write value should be 0.	Operating power control mode transition status flag 0: Transition completed 1: Transition in progress Note: This bit it read-only.
SOPCCR	—	—	Sub operating power control register

Register	Bit	RX630	RX231
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits b2 b0 0 0 1: HOCO selected. 0 1 0: Main clock oscillator is selected.	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO selected. 0 0 1: HOCO selected. 0 1 0: Main clock oscillator is selected.
MOSCWTCR *1	MSTS[4:0]	Main clock oscillator wait time select bits b4 b0 Wait time 0 0 0 0 0: 2 cycles 0 0 0 0 1: 4 cycles 0 0 0 1 0: 8 cycles 0 0 0 1 1: 16 cycles 0 0 1 0 0: 32 cycles 0 0 1 0 1: 64 cycles 0 0 1 1 0: 512 cycles 0 0 1 1 1: 1,024 cycles 0 1 0 0 0: 2,048 cycles 0 1 0 0 1: 4,096 cycles 0 1 0 1 0: 16,384 cycles 0 1 0 1 1: 32,768 cycles 0 1 1 0 0: 65,536 cycles 0 1 1 0 1: 131,072 cycles 0 1 1 1 0: 262,144 cycles 0 1 1 1 1: 524,288 cycles Do not set to values other than the above.	Main clock oscillator wait time select bits b4 b0 Wait time 0 0 0 0 0: 2 cycles 0 0 0 0 1: 1,024 cycles 0 0 0 1 0: 2,048 cycles 0 0 0 1 1: 4,096 cycles 0 0 1 0 0: 8,192 cycles 0 0 1 0 1: 16,384 cycles 0 0 1 1 0: 32,768 cycles 0 0 1 1 1: 65,536 cycles Do not set to values other than the above.
		Initial value after a reset is different.	
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER1	—	Deep standby interrupt enable register 1	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIER3	—	Deep standby interrupt enable register 3	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR1	—	Deep standby interrupt flag register 1	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIFR3	—	Deep standby interrupt flag register 3	—

Register	Bit	RX630	RX231
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR1	—	Deep standby interrupt edge register 1	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—
DPSIEGR3	—	Deep standby interrupt edge register 3	—
DPSBKRy	—	Deep standby backup register (y = 0 to 31)	—

Note 1. In the User's Manual: Hardware of the RX231 Group, MOSCWTCR is described in the Clock Generation Circuit section.

2.9 Battery Backup Function

Table 2.19 shows a comparative overview of the battery backup function registers.

Table 2.19 Comparative Overview of Battery Backup Function Registers

Register	Bit	RX630	RX231
VBATTCR	—	—	VBATT control register
VBATTSR	—	—	VBATT status register
VBTLVDICR	—	—	VBATT pin voltage drop detection interrupt control register

2.10 Register Write Protection Function

Table 2.20 shows a comparative overview of the register write protection function, and Table 2.21 shows a comparative overview of the register write protection function registers.

Table 2.20 Comparative Overview of Register Write Protection Function

Item	RX630	RX231
PRC0 bit	Registers related to the clock generation circuit SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR	Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, BCKCR, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3
PRC1 bit	• Registers related to the operating modes SYSCR0, SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR3 • Registers related to the clock generation circuit MOFCR, HOCOPCR • Software reset register SWRR	• Registers related to the operating modes SYSCR0, SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR
PRCR2 bit	—	Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to the battery backup function VBATTCR, VBATTSR, VBTLVDICR

Table 2.21 Comparative Overview of Register Write Protection Function Registers

Register	Bit	RX630	RX231
PRCR	PRC1	Enables writing to the registers related to operating modes, low power consumption functions, and software reset.	Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset.
	PRC2	—	Enables writing to the registers related to the low power timer.

2.11 Exception Handling

Table 2.22 shows a Comparative Listing of Vector, and Table 2.23 shows a Comparative Listing of Return from Exception Handling Routine.

Table 2.22 Comparative Listing of Vector

Exception (Event)		RX630	RX231
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than above	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.23 Comparative Listing of Return from Exception Handling Routine

Exception		RX630	RX231
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception		RTE	RTE
Reset		Return is impossible	Return is impossible
Non-maskable interrupt		Prohibited	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than above	RTE	RTE
Unconditional trap		RTE	RTE

2.12 Interrupt Controller

Table 2.24 shows a comparative overview of the interrupt controller specifications, and Table 2.25 shows a comparative overview of the interrupt controller registers.

Table 2.24 Comparative Overview of Interrupt Controller Specifications

Item		RX630 (ICUb)	RX231 (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source. • Interrupt grouping: Multiple interrupt requests can be allocated to a single interrupt vector. — Number of groups for edge detection interrupts: 7 (groups 0 to 6) — Number of groups for edge detection interrupts: 1 (group 12) • Interrupt unit selection: One of two interrupt requests can be selected as the interrupt request source. — Number of units: 6	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Sources: 16 • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupts generated by writing to a register. • Interrupt sources: 1	• Interrupts generated by writing to a register. • Interrupt source: 1
	Event link interrupt	—	The ELSR8I, ELSR18I, or ELSR19I interrupt is generated by an ELC event.
	Interrupt priority level	Priority is specified by register settings.	Priority is specified by register settings.
	Fast interrupt function	Faster interrupt processing by the CPU can be specified only for a single interrupt source.	Faster interrupt processing by the CPU can be specified only for a single interrupt source.
	DTC and DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.

Item		RX630 (ICUb)	RX231 (ICUb)
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt at oscillation stop detection	Interrupt at oscillation stop detection
	WDT underflow/ refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	IWDT underflow/ refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
	VBATT voltage monitoring interrupt	—	VBATT voltage monitoring interrupt
Return from low power consumption modes	Sleep mode	Return is initiated by non-maskable interrupt or any interrupt source.	Return is initiated by non-maskable interrupt or any interrupt source.
	Deep sleep mode	—	Return is initiated by non-maskable interrupt or any interrupt source.
	All-module clock stop mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, TMR interrupts, USB resume interrupts, and RTC alarm and period interrupts.	—
	Software standby mode	Return is initiated by non-maskable interrupts, IRQ0 to IRQ15 interrupts, RTC alarm and period interrupts, and USB resume interrupts.	Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, RTC alarm and period interrupts.
	Deep software standby mode	Return is initiated by some pins that generate external pin interrupts and peripheral function interrupts (RTC alarm and period, USB resume, voltage monitor 1, and voltage monitor 2).	—

Table 2.25 Comparative Overview Interrupt Controller Registers

Register	Bit	RX630 (ICUb)	RX231 (ICUb)
IRQCRi	—	IRQ control register i (i = 0 to 15)	IRQ control register i (i = 0 to 7)
IRQFLTE1	—	IRQ pin digital filter enable register 1	—
IRQFLTC1	—	IRQ pin digital filter setting register 1	—
NMISR	VBATST	—	VBATT voltage monitoring interrupt status flag
NMIER	VBATEN	—	VBATT voltage monitoring interrupt enable bit
NMICLR	VBATCLR	—	VBAT clear bit
GRPn	—	Group m interrupt source register (m = 00 to 06, 12)	—
GENn	—	Group m interrupt enable register (m = 00 to 06, 12)	—
GCRn	—	Group m interrupt clear register (m = 00 to 06)	—
SEL	—	Unit selecting register	—

2.13 Buses

Table 2.26 shows a comparative overview of the bus specifications, Table 2.27 shows a comparative overview of the external bus specifications, and Table 2.28 shows a comparative overview of the bus registers.

Table 2.26 Comparative Overview of Bus Specifications

Bus Type		RX630	RX231
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and code flash memory). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the ROM
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC and DMAC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC and DMAC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 3	• Connected to peripheral modules (USB). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (USB0, CAN, and CTSU). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	Reserved area	• Connected to peripheral modules (MTU2). • Operates in synchronization with the peripheral module clock (PCLKA).

Bus Type		RX630	RX231
Internal peripheral buses	Internal peripheral bus 5	Reserved area	Reserved area
	Internal peripheral bus 6	• Connected to the ROM (in P/E) and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to the flash control module and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK).
External bus	CS area	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).

Table 2.27 Comparative Overview of External Bus Specifications

Item	RX630	RX231
External address space	• The external address space is divided into eight CS areas (CS0 to CS7) for management. • Chip select signals can be output for each area. • The bus width can be specified for each area. — Separate bus: An 8, 16, or 32-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be specified for each area.	• The external address space is divided into four CS areas (CS0 to CS3) for management. • Chip select signals can be output for each area. • The bus width can be specified for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be specified for each area.
CS area controller	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control — Timing of assertion and negation of chip-select signals (CS0# to CS7#) — Timing of assertion of the read signal (RD#) and write signals (WR#, WR0# to WR3#) — Timing of start and end of data output. • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.	• Recovery cycles can be inserted. — Read recovery: Up to 15 cycles — Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control — Timing of assertion and negation of chip-select signals (CS0# to CS3#) — Timing of assertion of the read signal (RD#) and write signals (WR#, WR0#, and WR1#) — Timing of start and end of data output. • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.

Item	RX630	RX231
Frequency	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).	The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK).

Table 2.28 Comparative Overview of Bus Registers

Register	Bit	RX630	RX231
CSnCR	BSIZE[1:0]	External bus width select bits (n = 0 to 7) b5 b4 0 0: A 16-bit bus width is selected. 0 1: A 32-bit bus width is selected. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.	External bus width select bits (n = 0 to 3) b5 b4 0 0: A 16-bit bus width is selected. 0 1: Setting prohibited. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.
	EMODE	Endian mode bit (n = 0 to 7) 0: Endian mode of area n is the same as the endian mode of the operating mode. 1: Endian mode of area n is not the endian mode of the operating mode.	Endian mode bit (n = 0 to 3) 0: Endian mode of area n is the same as the endian mode of the operating mode. 1: Endian mode of area n is not the endian mode of the operating mode.
	MPXEN	Address/data multiplexed I/O interface select bit (n = 0 to 7) 0: Separate bus interface is selected for area n. 1: Address/data multiplexed I/O interface is selected for area n.	Address/data multiplexed I/O interface select bit (n = 0 to 3) 0: Separate bus interface is selected for area n. 1: Address/data multiplexed I/O interface is selected for area n.
CSnREC	—	CSn recovery cycle register (n = 0 to 7)	CSn recovery cycle register (n = 0 to 3)
CSnMOD	—	CSn mode register (n = 0 to 7)	CSn mode register (n = 0 to 3)
CSnWCR1	—	CSn weight control register 1 (n = 0 to 7)	CSn weight control register 1 (n = 0 to 3)
CSnWCR2	—	CSn weight control register 2 (n = 0 to 7)	CSn weight control register 2 (n = 0 to 3)
BUSPRI	BPHB[1:0]	—	Internal peripheral bus 4 priority control bits

2.14 Memory Protection Unit

Table 2.29 shows a comparative overview of the memory protection unit registers.

Table 2.29 Comparative Overview of Memory Protection Unit Registers

Register	Bit	RX630 (MPU)	RX231 (MPU)
MPESTS	IA: RX630 IMPER: RX231	Instruction memory protection error generated bit	Instruction memory protection error generated bit
	DA: RX630 DMPER: RX231	Data memory protection error generated bit	Data memory protection error generated bit

2.15 DMA Controller

Table 2.30 shows a comparative overview of the DMA controller specifications.

Table 2.30 Comparative Overview of DMA Controller Specifications

Item		RX630 (DMACA)	RX231 (DMACA)
Number of channels		4 (DMACm (m = 0 to 3))	4 (DMACm (m = 0 to 3))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1 MB data units (maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)	1 MB data units (maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)
DMAC activation sources		• Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	• Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer modes	Normal transfer mode	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• One data transfer per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data	• One data transfer per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data
	Block transfer mode	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer per DMA transfer request • Maximum settable block size: 1,024 data
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX630 (DMACA)	RX231 (DMACA)
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link activation		—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

2.16 Data Transfer Controller

Table 2.31 shows a comparative overview of the data transfer controller specifications.

Table 2.31 Comparative Overview of Data Transfer Controller Specifications

Item	RX630 (DTCa)	RX231 (DTCa)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256 × 32 bits = 1,024 bytes
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC transfer request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC transfer request from the ICU). • Data of multiple channels can be transferred on a single transfer request (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• 16 Mbytes in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 Gbytes in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)	• 16 Mbytes in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 Gbytes in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)
Data transfer units	• Single data: 8 bits, 16 bits, or 32 bits • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.

Item	RX630 (DTCa)	RX231 (DTCa)
Event link activation	—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Read skip	It is possible to specify that reading of transfer information be skipped.	It is possible to specify that reading of transfer information be skipped.
Write-back skip	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.32 Comparative Overview of Data Transfer Controller Registers

Register	Bit	RX630 (RIIC)	RX231 (RIICa)
DTCVBR	—	DTC Vector Base Register The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 12 bits are reserved and the values are fixed to 0. Write 0 to the lower 12 bits if necessary. It can be set in the range of 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h in 4-Kbyte units.	DTC Vector Base Register The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Writing to the upper 4 bits (b31 to b28) is ignored, and the address of this register is extended by the value specified by b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary. It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units.

2.17 I/O Ports

Table 2.33 shows a comparative overview of the I/O port specifications, and Table 2.34 shows a comparative listing of I/O port functions, and Table 2.35 shows a comparative overview of the I/O port registers.

Table 2.33 Comparative Overview of I/O port Specifications

Port Symbol	RX630 (100-pin)	RX231 (100-pin)
PORT0	P05, P07	P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH0 to PH3
PORTJ	PJ3	PJ3

Table 2.34 Comparative Listing of I/O Port Functions

Item	Port Symbol	RX630 (100-pin)	RX231 (100-pin)
Input pull-up function	PORT0	P05, P07	P03, P05, P07
	PORT1	P12～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34, P36, P37	P30～P34, P36, P37
	PORT4	P40～P47	P40～P47
	PORT5	P50～P55	P50～P55
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PE7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTH	—	PH0～PH3
	PORTJ	PJ3	PJ3
Open-drain output	PORT0	P05, P07	—
	PORT1	P12～P17	P12～P17
	PORT2	P20～P27	P20～P27
	PORT3	P30～P34, P36, P37	P30～P34, P36, P37
	PORT4	P40～P47	—
	PORT5	P50～P52, P53, P54, P55	P50～P52, P54
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PE7	—
	PORTE	PE0～PE7	PE0～PE7
	PORTH	—	—

Item	Port Symbol	RX630 (100-pin)	RX231 (100-pin)
	PORTJ	PJ3	PJ3
Drive capacity switching function	PORT0	P05*1, P07*1	P03*2, P05*2, P07*2
	PORT1	P12～P17*1	P12～P17
	PORT2	P20～P26*1, P27	P20～P26, P27
	PORT3	P30～P34*1, P36*2, P37*1	P30～P34, P36*2, P37*2
	PORT4	P40～P47*2	P40～P47*2
	PORT5	P50～P52, P53～P55*1	P50～P52, P53～P55
	PORTA	PA0～PA7	PA0～PA7
	PORTB	PB0～PB7	PB0～PB7
	PORTC	PC0～PC7	PC0～PC7
	PORTD	PD0～PD7	PD0～PD7
	PORTE	PE0～PE7	PE0～PE7
	PORTH	—	PH0～PH3
	PORTJ	PJ3*1	PJ3
5 V tolerant	PORT0	P07	
	PORT1	P12, P13, P14, P15, P16, P17	P12, P13, P16, P17
	PORT2	P20～P25	—
	PORT3	P30～P32, P33, P34	P30～P32
	PORT4	—	—
	PORT5	P50～P52, P54～P57	—
	PORTA	PA1～PA4, PA6	—
	PORTB	PB0～PB4, PB5, PB6, PB7	PB5
	PORTC	PC0～PC7	—
	PORTD	—	—
	PORTE	—	—
	PORTH	—	—
	PORTJ	—	—

Note 1. Fixed to high drive output
Note 2. Fixed to normal output

Table 2.35 Comparative Overview of I/O Port Registers

Register	Bit	RX630	RX231
ODR0	B2, B3	Pm1 output format specification bit P21, P31, P41, P51, PA1, PB1, PC1, PD1 Other than PE1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Setting prohibited	Pm1 output format specification bit P21, P31, P51, PA1, PB1, PC1 Other than PE1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z

2.18 Multi-Function Pin Controller

Table 2.36 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.37 shows a comparative overview of the multi-function pin controller registers.

Blue characters exist only in the RX630, and orange characters exist only in the RX231. "√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates no assignment pin for function, Grey hatching indicates pin function not implemented.

Table 2.36 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Interrupt	NMI (input)	P35	○	○
	IRQ0-DS (input)	P30	○	
	IRQ0 (input)	P10	×	-
		PD0	○	○
		P30	-	○
		PH1	-	○
	IRQ1-DS (input)	P31	○	
	IRQ1 (input)	P11	×	-
		PD1	○	○
		P31	-	○
		PH2	-	○
	IRQ2-DS (input)	P32	○	
	IRQ2 (input)	P12	○	○
		PD2	○	○
		P32	-	○
	IRQ3-DS (input)	P33	○	
	IRQ3 (input)	P13	○	○
		PD3	○	○
		P33	-	○
	IRQ4-DS (input)	PB1	○	
	IRQ4 (input)	P14	○	○
		P34	○	○
		PD4	○	○
		PF5	×	-
		PB1	-	○
	IRQ5-DS (input)	PA4	○	
	IRQ5 (input)	P15	○	○
		PD5	○	○
		PE5	○	○
		PA4	-	○
	IRQ6-DS (input)	PA3	○	
	IRQ6 (input)	P16	○	○
		PD6	○	○
		PE6	○	○
		PA3	-	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Interrupt	IRQ7-DS (input)	PE2	○	
	IRQ7 (input)	P17	○	○
		PD7	○	○
		PE7	○	○
		PE2	-	○
	IRQ8-DS (input)	P40	○	
	IRQ8 (input)	P00	×	
		P20	○	
	IRQ9-DS (input)	P41	○	
	IRQ9 (input)	P01	×	
		P21	○	
	IRQ10-DS (input)	P42	○	
	IRQ10 (input)	P02	×	
		P55	○	
	IRQ11-DS (input)	P43	○	
	IRQ11 (input)	P03	×	
		PA1	○	
	IRQ12-DS (input)	P44	○	
	IRQ12 (input)	PB0	○	
		PC1	○	
	IRQ13-DS (input)	P45	○	
	IRQ13 (input)	P05	○	
		PC6	○	
	IRQ14-DS (input)	P46	○	
	IRQ14 (input)	PC0	○	
		PC7	○	
	IRQ15-DS (input)	P47	○	
	IRQ15 (input)	P07	○	
		P67	×	
Clock generation circuit	CLKOUT(output)	PE3		○
		PE4		○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	○
		PB3	○	○
	MTIOC0B (input/output)	P13	○	○
		P15	○	○
		PA1	○	○
	MTIOC0C (input/output)	P32	○	○
		PB1	○	○
	MTIOC0D (input/output)	P33	○	○
		PA3	○	○
	MTIOC1A (input/output)	P20	○	○
		PE4	○	○
	MTIOC1B (input/output)	P21	○	○
		PB5	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Multi-function timer unit 2	MTIOC2A (input/output)	P26	○	○
		PB5	○	○
	MTIOC2B (input/output)	P27	○	○
		PE5	○	○
	MTIOC3A (input/output)	P14	○	○
		P17	○	○
		PC1	○	○
		PC7	○	○
	MTIOC3B (input/output)	P17	○	○
		P22	○	○
		P80	×	-
		PB7	○	○
		PC5	○	○
	MTIOC3C (input/output)	P16	○	○
		P56	×	-
		PC0	○	○
		PC6	○	○
		PJ3	○	○
	MTIOC3D (input/output)	P16	○	○
		P23	○	○
		P81	×	-
		PB6	○	○
		PC4	○	○
	MTIOC4A (input/output)	P24	○	○
		P82	×	-
		PA0	○	○
		PB3	○	○
		PE2	○	○
	MTIOC4B (input/output)	P30	○	○
		P54	○	○
		PC2	○	○
		PD1	○	○
		PE3	○	○
	MTIOC4C (input/output)	P25	○	○
		P83	×	-
		PB1	○	○
		PE1	○	○
		PE5	○	○
	MTIOC4D (input/output)	P31	○	○
		P55	○	○
		PC3	○	○
		PD2	○	○
		PE4	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Multi-function timer unit 2	MTIC5U (input)	P12	×	-
		PA4	○	○
		PD7	○	○
	MTIC5V (input)	P11	×	-
		PA6	○	○
		PD6	○	○
	MTIC5W (input)	P10	×	-
		PB0	○	○
		PD5	○	○
	MTCLKA (input)	P14	○	○
		P24	○	○
		PA4	○	○
		PC6	○	○
	MTCLKB (input)	P15	○	○
		P25	○	○
		PA6	○	○
		PC7	○	○
	MTCLKC (input)	P22	○	○
		PA1	○	○
		PC4	○	○
	MTCLKD (input)	P23	○	○
		PA3	○	○
		PC5	○	○
Port output enable 2	POE0# (input)	PC4	○	○
		PD7	○	○
	POE1# (input)	PB5	○	○
		PD6	○	○
	POE2# (input)	P34	○	○
		PA6	○	○
		PD5	○	○
	POE3# (input)	P33	○	○
		PB3	○	○
		PD4	○	○
	POE8# (input)	P17	○	○
		P30	○	○
		PD3	○	○
		PE3	○	○
16-bit timer pulse unit	TIOCA0 (input/output)	P86	×	-
		PA0	○	○
	TIOCB0 (input/output)	P17	○	○
		PA1	○	○
	TIOCC0 (input/output)	P32	○	○
	TIOCD0 (input/output)	P33	○	○
		PA3	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
16-bit timer pulse unit	TIOCA1 (input/output)	P56	×	-
		PA4	○	○
	TIOCB1 (input/output)	P16	○	○
		PA5	○	○
	TIOCA2 (input/output)	P87	×	-
		PA6	○	○
	TIOCB2 (input/output)	P15	○	○
		PA7	○	○
	TIOCA3 (input/output)	P21	○	○
		PB0	○	○
	TIOCB3 (input/output)	P20	○	○
		PB1	○	○
	TIOCC3 (input/output)	P22	○	○
		PB2	○	○
	TIOCD3 (input/output)	P23	○	○
		PB3	○	○
	TIOCA4 (input/output)	P25	○	○
		PB4	○	○
	TIOCB4 (input/output)	P24	○	○
		PB5	○	○
	TIOCA5 (input/output)	P13	○	○
		PB6	○	○
	TIOCB5 (input/output)	P14	○	○
		PB7	○	○
	TCLKA (input)	P14	○	○
		PC2	○	○
	TCLKB (input)	P15	○	○
		PA3	○	○
		PC3	○	○
	TCLKC (input)	P16	○	○
		PB2	○	○
		PC0	○	○
	TCLKD (input)	P17	○	○
		PB3	○	○
		PC1	○	○
	TIOCA6 (input/output)	PC6	×	
	TIOCB6 (input/output)	PC7	×	
	TIOCC6 (input/output)	PC4	×	
	TIOCD6 (input/output)	PC5	×	
	TIOCA7 (input/output)	PD0	×	
	TIOCB7 (input/output)	PD1	×	
	TIOCA8 (input/output)	PD2	×	
	TIOCB8 (input/output)	PD3	×	

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
16-bit timer pulse unit	TIOCA9 (input/output)	PE2	×	
	TIOCB9 (input/output)	PE3	×	
	TIOCC9 (input/output)	PE0	×	
	TIOCD9 (input/output)	PE1	×	
	TIOCA10 (input/output)	PE4	×	
	TIOCB10 (input/output)	PE5	×	
	TIOCA11 (input/output)	PE6	×	
	TIOCB11 (input/output)	PE7	×	
	TCLKE (input)	PC4	×	
	TCLKF (input)	PC5	×	
	TCLKG (input)	PD1	×	
	TCLKH (input)	PD3	×	
Programmable pulse generator	PO0 (output)	P20	○	
	PO1 (output)	P21	○	
	PO2 (output)	P22	○	
	PO3 (output)	P23	○	
	PO4 (output)	P24	○	
	PO5 (output)	P25	○	
	PO6 (output)	P26	○	
	PO7 (output)	P27	○	
	PO8 (output)	P30	○	
	PO9 (output)	P31	○	
	PO10 (output)	P32	○	
	PO11 (output)	P33	○	
	PO12 (output)	P34	○	
	PO13 (output)	P13	○	
		P15	○	
	PO14 (output)	P16	○	
	PO15 (output)	P14	○	
		P17	○	
	PO16 (output)	P73	×	
		PA0	○	
	PO17 (output)	PA1	○	
		PC0	○	
	PO18 (output)	PA2	○	
		PC1	○	
		PE1	○	
	PO19 (output)	P74	×	
		PA3	○	
	PO20 (output)	P75	×	
		PA4	○	
	PO21 (output)	PA5	○	
		PC2	○	
	PO22 (output)	P76	×	
		PA6	○	

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Programmable pulse generator	PO23 (output)	P77	×	
		PA7	○	
		PE2	○	
	PO24 (output)	PB0	○	
		PC3	○	
	PO25 (output)	PB1	○	
		PC4	○	
	PO26 (output)	P80	×	
		PB2	○	
		PE3	○	
	PO27 (output)	P81	×	
		PB3	○	
	PO28 (output)	P82	×	
		PB4	○	
		PE4	○	
	PO29 (output)	PB5	○	
		PC5	○	
	PO30 (output)	PB6	○	
		PC6	○	
	PO31 (output)	PB7	○	
		PC7	○	
8-bit timer	TMO0 (output)	P22	○	○
		PB3	○	○
		PH1	-	○
	TMCI0 (input)	P01	×	-
		P21	○	○
		PB1	○	○
		PH3	-	○
	TMRI0 (input)	P00	×	-
		P20	○	○
		PA4	○	○
		PH2	-	○
	TMO1 (output)	P17	○	○
		P26	○	○
	TMCI1 (input)	P02	×	-
		P12	○	○
		P54	○	○
		PC4	○	○
	TMRI1 (input)	P24	○	○
		PB5	○	○
	TMO2 (output)	P16	○	○
		PC7	○	○
	TMCI2 (input)	P15	○	○
		P31	○	○
		PC6	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
8-bit timer	TMRI2 (input)	P14	○	○
		PC5	○	○
	TMO3 (output)	P13	○	○
		P32	○	○
		P55	○	○
	TMCI3 (input)	P11	×	-
		P27	○	○
		P34	○	○
		PA6	○	○
	TMRI3 (input)	P10	×	-
		P30	○	○
		P33	○	○
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○
		P33	○	-
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○
		P32	○	-
	SCK0 (input/output)	P22	○	○
		P34	○	-
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○
		PJ3	○	-
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○
		P30	○	○
		PF2	×	-
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○
		P26	○	○
		PF0	×	-
	SCK1 (input/output)	P17	○	○
		P27	○	○
		PF1	×	-
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○
		P31	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	
		P52	○	
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	○	
		P50	○	
	SCK2 (input/output)	P11	×	
		P51	○	
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Serial communications interface	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	
		P25	○	
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	○	
		P23	○	
	SCK3 (input/output)	P15	○	
		P24	○	
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	×	
		PK4	×	
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	×	
		PK5	×	
	SCK4 (input/output)	P70	×	
		PB3	×	
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	×	
		PE6	×	
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○
		PA3	○	○
		PC2	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○
		PC3	○	○
	SCK5 (input/output)	PA1	○	○
		PC1	○	○
		PC4	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○
		PC0	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	×	-
		P33	○	○
		PB0	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	×	-
		P32	○	○
		PB1	○	○
	SCK6 (input/output)	P02	×	-
		P34	○	○
		PB3	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○
		PJ3	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Serial communications interface	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P92	×	
	TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P90	×	
	SCK7 (input/output)	P91	×	
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	×	
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○
	SCK8 (input/output)	PC5	○	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○
		PK3	×	-
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○
		PK2	×	-
	SCK9 (input/output)	P60	×	-
		PB5	○	○
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P61	×	-
		PB4	○	○
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	×	
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	P82	×	
	SCK10 (input/output)	P80	×	
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	P83	×	
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	×	

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Serial communications interface	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	P77	×	
	SCK11 (input/output)	P75	×	
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	P74	×	
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○
	SCK12 (input/output)	PE0	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○
I²C bus interface	SCL0[FM+] (input/output)	P12	○	
	SDA0[FM+] (input/output)	P13	○	
	SCL1 (input/output)	P21	×	
	SDA1 (input/output)	P20	×	
	SCL2-DS (input/output)	P16	○	
	SDA2-DS (input/output)	P17	○	
	SCL3 (input/output)	PC0	×	
	SDA3 (input/output)	PC1	×	
I²C bus interface	SCL (input/output)	P16		○
		P12		○
	SDA (input/output)	P17		○
		P13		○
USB 2.0 Function Module	USB0_DPUPE (output)	P14	○	
	USB0_VBUS (input)	P16	○	○
		PB5	-	○
USB 2.0 host/function module	USB0_EXICEN (output)	P21		○
		PC6		×
	USB0_VBUSEN (output)	P16		○
		P24		○
		P26		×
		P32		○
	USB0_OVRCURA (input)	P14		○
	USB0_OVRCURB (input)	P16		○
		P22		○
	USB0_ID (input)	P20		○
		PC5		×

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
CAN module	CRX0 (input)	P33	○	
		PD2	○	
	CTX0 (output)	P32	○	
		PD1	○	
	CRX1-DS (input)	P15	○	
	CRX1 (input)	P55	○	
	CTX1 (output)	P14	○	
		P54	○	
	CRX2 (input)	P67	×	
	CTX2 (output)	P66	×	
	CRXD0 (input)	P15		○
		P55		○
	CTXD0 (output)	P14		○
		P54		○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○
		PB0	○	○
		PC5	○	○
	MOSIA (input/output)	P16	○	○
		PA6	○	○
		PC6	○	○
	MISOA (input/output)	P17	○	○
		PA7	○	○
		PC7	○	○
	SSLA0 (input/output)	PA4	○	○
		PC4	○	○
	SSLA1 (output)	PA0	○	○
		PC0	○	○
	SSLA2 (output)	PA1	○	○
		PC1	○	○
	SSLA3 (output)	PA2	○	○
		PC2	○	○
	RSPCKB (input/output)	P27	○	
		PE1	○	
		PE5	○	
	MOSIB (input/output)	P26	○	
		PE2	○	
		PE6	○	
	MISOB (input/output)	P30	○	
		PE3	○	
		PE7	○	
	SSLB0 (input/output)	P31	○	
		PE4	○	
	SSLB1 (output)	P50	○	
		PE0	○	
	SSLB2 (output)	P51	○	
		PE1	○	

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Serial peripheral interface	SSLB3 (output)	P52	○	
		PE2	○	
	RSPCKC (input/output)	PD3	×	
	MOSIC (input/output)	PD1	×	
	MISOC (input/output)	PD2	×	
	SSLC0 (input/output)	PD4	×	
	SSLC1 (output)	PD5	×	
	SSLC2 (output)	PD6	×	
	SSLC3 (output)	PD7	×	
IEBus controller	IERXD (input)	P16	○	
		PC2	○	
	IETXD (output)	P17	○	
		PC3	○	
IrDA interface	IRTXD5 (output)	PA4		○
		PC3		○
	IRRXD5 (input)	PA2		○
		PA3		○
		PC2		○
Serial sound interface	SSISCK0 (input/output)	P23		○
		P31		○
		PA1		○
	SSIWS0 (input/output)	P21		○
		P27		○
		PA6		○
	SSITXD0 (output)	P17		○
		PA4		○
	SSIRXD0 (input)	P20		○
		P26		○
		PA3		○
	AUDIO_MCLK (input)	P22		○
		P30		○
		PE3		○
SD host interface	SDHI_CLK (output)	PB1		○
	SDHI_CMD (input/output)	PB0		○
	SDHI_D0 (input/output)	PC3		○
	SDHI_D1 (input/output)	PB6		○
		PC4		○
	SDHI_D2 (input/output)	PB7		○
	SDHI_D3 (input/output)	PC2		○
	SDHI_CD (input)	PB5		○
	SDHI_WP (input)	PB3		○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Realtime clock	RTCOUT (output)	P16	○	○
		P32	○	○
	RTCIC0 (input)	P30	○	○
	RTCIC1 (input)	P31	○	○
	RTCIC2 (input)	P32	○	○
12-bit A/D converter	AN000 (input)	P40	○	○
	AN001 (input)	P41	○	○
	AN002 (input)	P42	○	○
	AN003 (input)	P43	○	○
	AN004 (input)	P44	○	○
	AN005 (input)	P45	○	○
	AN006 (input)	P46	○	○
	AN007 (input)	P47	○	○
	AN008 (input)	PD0	○	
	AN009 (input)	PD1	○	
	AN010 (input)	PD2	○	
	AN011 (input)	PD3	○	
	AN012 (input)	PD4	○	
	AN013 (input)	PD5	○	
	AN014 (input)	P90	×	
	AN015 (input)	P91	×	
	AN016 (input)	P92	×	-
		PE0	-	○
	AN017 (input)	P93	×	-
		PE1	-	○
	AN018 (input)	P00	×	-
		PE2	-	○
	AN019 (input)	P01	×	-
		PE3	-	○
	AN020 (input)	P02	×	-
		PE4	-	○
	AN021 (input)	PE5		○
	AN022 (input)	PE6		○
	AN023 (input)	PE7		○
	AN024 (input)	PD0		○
	AN025 (input)	PD1		○
	AN026 (input)	PD2		○
	AN027 (input)	PD3		○
	AN028 (input)	PD4		○
	AN029 (input)	PD5		○
	AN030 (input)	PD6		○
	AN031 (input)	PD7		○
	ADTRG0# (input)	P07	○	○
		P16	○	○
		P25	○	○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
10-bit A/D converter	AN0 (input)	PE2	○	
	AN1 (input)	PE3	○	
	AN2 (input)	PE4	○	
	AN3 (input)	PE5	○	
	AN4 (input)	PE6	○	
	AN5 (input)	PE7	○	
	AN6 (input)	PD6	○	
	AN7 (input)	PD7	○	
	ANEX0 (output)	PE0	○	
	ANEX1 (input)	PE1	○	
	ADTRG# (input)	P13	○	
		P17	○	
D/A converter	DA0 (output)	P03	×	○
	DA1 (output)	P05	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0		○
		PC7		○
		PH0		○
LVD voltage detection input	CMPA2 (input)	PE4		○
Comparator B	CMPB0 (input)	PE1		○
	CVREFB0 (input)	PE2		○
	CMPB1 (input)	PA3		○
	CVREFB1 (input)	PA4		○
	CMPB2 (input)	P15		○
	CVREFB2 (input)	P14		○
	CMPB3 (input)	P26		○
	CVREFB3 (input)	P27		○
	CMPOB0 (output)	PE5		○
	CMPOB1 (output)	PB1		○
	CMPOB2 (output)	P17		○
	CMPOB3 (output)	P30		○
Capacitive touch sensing unit (CTSU)	TSCAP (output)	PC4		○
	TS0 (output)	P34		○
	TS1 (output)	P33		○
	TS2 (output)	P27		○
	TS3 (output)	P26		○
	TS4 (output)	P25		○
	TS5 (output)	P24		○
	TS6 (output)	P23		○
	TS7 (output)	P22		○
	TS8 (output)	P21		○
	TS9 (output)	P20		○
	TS12 (output)	P15		○
	TS13 (output)	P14		○
	TS15 (output)	P55		○
	TS16 (output)	P54		○

Module/Function	Pin Functions	Allocation Port	RX630 100 pin	RX231 100 pin
Capacitive touch sensing unit (CTSU)	TS17 (output)	P53		○
	TS18 (output)	P52		○
	TS19 (output)	P51		○
	TS20 (output)	P50		○
	TS22 (output)	PC6		○
	TS23 (output)	PC5		○
	TS27 (output)	PC3		○
	TS30 (output)	PC2		○
	TS33 (output)	PC1		○
	TS35 (output)	PC0		○

Table 2.37 Comparative Overview of Multi-Function Pin Controller Registers

Register	Bit	RX630 (MPC)	RX231 (MPC)
P0nPFS	ISEL	Interrupt Input Function Select	—
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P00: AN018 (177/176/145/144 pins) P01: AN019 (177/176/145/144 pins) P02: AN020 (177/176/145/144 pins) P03: DA0 (177/176/145/144 pins) P05: DA1 (177/176/145/144/100/80 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin P03: DA0 (100/64 pins) P05: DA1 (100/64 pins)
P1nPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 input switch (177/176 pins) P11: IRQ1 input switch (177/176 pins) P12: IRQ2 input switch (177/176/145/144/100/80 pins) P13: IRQ3 input switch (177/176/145/144/100/80 pins) P14: IRQ4 input switch (177/176/145/144/100/80 pins) P15: IRQ5 input switch (177/176/145/144/100/80 pins) P16: IRQ6 input switch (177/176/145/144/100/80 pins) P17: IRQ7 input switch (177/176/145/144/100/80 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100 pins) P13: IRQ3 input switch (100 pins) P14: IRQ4 input switch (100/64/48 pins) P15: IRQ5 input switch (100/64/48 pins) P16: IRQ6 input switch (100/64/48 pins) P17: IRQ7 input switch (100/64/48 pins)
	ASEL	—	Analog Function Select
P2nPFS	ISEL	Interrupt Input Function Select	—
	ASEL	—	Analog Function Select

Register	Bit	RX630 (MPC)	RX231 (MPC)
P3nPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (177/176/145/144/100/80 pins) P31: IRQ1-DS (177/176/145/144/100/80 pins) P32: IRQ2-DS (177/176/145/144/100/80 pins) P33: IRQ3-DS (177/176/145/144/100 pins) P34: IRQ4 (177/176/145/144/100/80 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/64/48 pins) P31: IRQ1 input switch (100/64/48 pins) P32: IRQ2 input switch (100 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100 pins)
P4nPFS	ISEL	Interrupt Input Function Select	—
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. P40: AN000 (177/176/145/144/100/80 pins) P41: AN001 (177/176/145/144/100/80 pins) P42: AN002 (177/176/145/144/100/80 pins) P43: AN003 (177/176/145/144/100/80 pins) P44: AN004 (177/176/145/144/100/80 pins) P45: AN005 (177/176/145/144/100/80 pins) P46: AN006 (177/176/145/144/100/80 pins) P47: AN007 (177/176/145/144/100/80 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/64/48 pins) P41: AN001 (100/64/48 pins) P42: AN002 (100/64/48 pins) P43: AN003 (100/64 pins) P44: AN004 (100/64 pins) P45: AN005 (100 pins) P46: AN006 (100/64/48 pins) P47: AN007 (100 pins)
P5nPFS	ISEL	Interrupt Input Function Select	—
P6nPFS	—	P6n Pin Function Control Registers	—
P7nPFS	—	P7n Pin Function Control Registers	—
P8nPFS	—	P8n Pin Function Control Registers	—
P9nPFS	—	P9n Pin Function Control Registers	—
PAnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 input switch (177/176/145/144/100/80 pins) PA3: IRQ6-DS input switch (177/176/145/144/100/80 pins) PA4: IRQ5-DS input switch (177/176/145/144/100/80 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/64/48 pins) PA4: IRQ5 input switch (100/64/48 pins)
	ASEL	—	Analog Function Select

Register	Bit	RX630 (MPC)	RX231 (MPC)
PBnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100/80 pins) PB1: IRQ4-DS (177/176/145/144/100/80 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/64/48 pins)
PCnPFS	ISEL	Interrupt Input Function Select	—
PDnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (177/176/145/144/100/80 pins) PD1: IRQ1 (177/176/145/144/100/80 pins) PD2: IRQ2 (177/176/145/144/100/80 pins) PD3: IRQ3 (177/176/145/144/100 pins) PD4: IRQ4 (177/176/145/144/100 pins) PD5: IRQ5 (177/176/145/144/100 pins) PD6: IRQ6 (177/176/145/144/100 pins) PD7: IRQ7 (177/176/145/144/100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100 pins) PD1: IRQ1 input switch (100 pins) PD2: IRQ2 input switch (100 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)
	ASEL	Analog Input Function Select 0: Used other than as analog pin 1: Used as analog pin PD0: AN008 (177/176/145/144/100/80 pins) PD1: AN009 (177/176/145/144/100/80 pins) PD2: AN010 (177/176/145/144/100/80 pins) PD3: AN011 (177/176/145/144/100/ pins) PD4: AN012 (177/176/145/144/100 pins) PD5: AN013 (177/176/145/144/100 pins) PD6: AN6 (177/176/145/144/100 pins) PD7: AN7 (177/176/145/144/100 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin PD0: AN024 (100 pins) PD1: AN025 (100 pins) PD2: AN026 (100 pins) PD3: AN027 (100 pins) PD4: AN028 (100 pins) PD5: AN029 (100 pins) PD6: AN030 (100 pins) PD7: AN031 (100 pins)

Register	Bit	RX630 (MPC)	RX231 (MPC)
PEnPFS	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (177/176/145/144/100/80 pins) PE5: IRQ5 (177/176/145/144/100/80 pins) PE6: IRQ6 (177/176/145/144/100 pins) PE7: IRQ7 (177/176/145/144/100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/64/48 pins) PE5: IRQ5 input switch (100/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)
	ASEL	Analog Input Function Select 0: Used other than as analog pin. 1: Used as analog pin. PE0: ANEX0 (177/176/145/144/100/80 pins) PE1: ANEX1 (177/176/145/144/100/80 pins) PE2: AN0 (177/176/145/144/100/80 pins) PE3: AN1 (177/176/145/144/100/80 pins) PE4: AN2 (177/176/145/144/100/80 pins) PE5: AN3 (177/176/145/144/100/80 pins) PE6: AN4 (177/176/145/144/100 pins) PE7: AN5 (177/176/145/144/100 pins)	Analog Function Select 0: Used other than as analog pin 1: Used as analog pin PE0:AN016 (100/64 pins) PE1:AN017 or CMPB0 (100/64/48 pins) PE2:AN018 or CVREFB0 (100/64/48 pins) PE3:AN019 (100/64/48 pins) PE4:AN020 (100/64/48 pins) PE5:AN021 (100/64 pins) PE6:AN022 (100 pins) PE7:AN023 (100 pins)
PFnPFS	—	PFn Pin Function Control Registers	—
PHnPFS	—	—	PHn Pin Function Control Registers
PKnPFS	—	PKn Pin Function Control Registers	—
PFCSE	CS4E	CS4 Enable 0: CS4# output disabled 1: CS4# output enabled	CS0 Enable of P24 0: Configures the P24 as an I/O pin. 1: Configures the P24 as an CS0# output pin.
	CS5E	CS5 Enable 0: CS5# output disabled 1: CS5# output enabled	CS1 Enable of P25 0: Configures the P25 as an I/O pin. 1: Configures the P25 as an CS1# output pin.
	CS6E	CS6 Enable 0: CS6# output disabled 1: CS6# output enabled	CS2 Enable of PC5 0: Configures the PC5 as an I/O pin. 1: Configures the PC5 as an CS2# output pin.
	CS7E	CS7 Enable 0: CS7# output disabled 1: CS7# output enabled	CS3 Enable of PC4 0: Configures the PC4 as an I/O pin. 1: Configures the PC4 as an CS3# output pin.
PFCSS0	—	CS output pin select register 0	—
PFCSS1	—	CS output pin select register 1	—

Register	Bit	RX630 (MPC)	RX231 (MPC)
PFBCR0	ADRHMS	A16 to A23 output enable bit	—
	DH32E	D16 to D31 output enable bit	—
	WR32BC32E	WR3#/BC3# output enable bit WR2#/BC2# output enable bit	—
PFBCR1	WAITS[1:0]	WAIT select bits b1b0 0 0: Configures P57 as the WAIT# input pin. 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.	WAIT select bits b1b0 0 0: Setting prohibited 0 1: Configures P55 as the WAIT# input pin. 1 0: Configures PC5 as the WAIT# input pin. 1 1: Configures P51 as the WAIT# input pin.
PFUSB0	—	USB0 control register	—

2.19 Multi-Function Timer Pulse Unit 2

Table 2.38 shows a comparative overview of the multi-function timer pulse unit 2 specifications.

Table 2.38 Comparative Overview of Multi-Function Timer Pulse Unit 2 Specifications

Item	RX630 (MTU2a)	RX231 (MTU2a)
Pulse input/output	Maximum 16	Maximum 16
Pulse input	3	3
Count clocks	7 or 8 or clocks per channel (4 clocks for MTU5)	7 or 8 or clocks per channel (4 clocks for MTU5)
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, and MTU4] • Ability to specify buffer operation • Ability to select between 2 types of waveform output (chopping and level) for AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output	[MTU0, MTU3, and MTU4] • Ability to specify buffer operation • Ability to select between 2 types of waveform output (chopping and level) for AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output
	[MTU1 and MTU2] • Ability to specify phase counting mode independently • Cascade connection operation	[MTU1 and MTU2] • Ability to specify phase counting mode independently • Cascade connection operation
	[MTU3 and MTU4] • A total of 6 layers of waveform output, including 3 phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3 and MTU4] • A total of 6 layers of waveform output, including 3 phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation
	[MTU5] • Dead time compensation counter function • Input capture function (noise filter setting) • Counter clear operation	[MTU5] • Dead time compensation counter function • Input capture function (noise filter setting) • Counter clear operation
Complementary PWM modes	• Interrupts at counter peak and trough • A/D converter start trigger skipping function	• Interrupts at counter peak and trough • A/D converter start trigger skipping function
Interrupt sources	28	28
Buffer operation	Automatic transfer of register data	Automatic transfer of register data

Item	RX630 (MTU2a)	RX231 (MTU2a)
Trigger generation	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
	Programmable pulse generator (PPG) output trigger generation is available.	—
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.20 Port Output Enable 2

Table 2.39 shows a comparative overview of the port output enable 2 specifications.

Table 2.39 Comparative Overview of Port Output Enable 2 Specifications

Item	RX630 (POE2a)	RX231 (POE2a)
High-impedance control by input level detection	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be specified for each of the POE0# to POE3# and POE8# input pins. • Pins for complementary PWM output from the MTU can be placed in the high-impedance state at falling-edge detection or sampling of the low level on the POE0# to POE3# pins. • MTU0 output pins can be placed in the high-impedance state at falling-edge detection or sampling of the low level on the POE8# pin.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be specified for each of the POE0# to POE3# and POE8# input pins. • Pins for complementary PWM output from the MTU can be placed in the high-impedance state at falling-edge detection or sampling of the low level on the POE0# to POE3# pins. • MTU0 output pins can be placed in the high-impedance state at falling-edge detection or sampling of the low level on the POE8# pin.
High-impedance control by output level comparison	Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more cycles, the pins can be placed in the high-impedance state.	Levels output on pins for complementary PWM output from the MTU are compared, and when simultaneous output of the active level continues for one or more cycles, the pins can be placed in the high-impedance state.
High-impedance control by oscillation stop detection	Pins for complementary PWM output from the MTU and the MTU0 output pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops.	Pins for complementary PWM output from the MTU and the MTU0 output pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops.
High-impedance control by software (registers)	Pins for complementary PWM output from the MTU and the MTU0 output pins can be placed in the high-impedance state by writing to the POE registers.	Pins for complementary PWM output from the MTU and the MTU0 output pins can be placed in the high-impedance state by writing to the POE registers.
High-impedance control by event signal	—	Pins for complementary PWM output from the MTU and the MTU0 output pins can be placed in the high-impedance state in response to an event signal from the event link controller (ELC).
Interrupts	Interrupts are generated in response to the results of POE0# to POE3# and POE8# input-level detection and MTU complementary PWM output-level comparison.	Interrupts are generated in response to the results of POE0# to POE3# and POE8# input-level detection and MTU complementary PWM output-level comparison.

2.21 16-Bit Timer Pulse Unit

Table 2.40 shows a comparative overview of 16-bit timer pulse unit specifications, and Table 2.41 shows a comparative overview of the 16-bit timer pulse unit registers.

Table 2.40 Comparative Overview of 16-Bit Timer Pulse Unit Specifications

Item	RX630 (TPUa)	RX231 (TPUa)
Pulse input/output	Maximum 32 (Unit 0: 16, unit 1: 16)	Maximum 16
Count clocks	7 and 8 clocks for each channel	7 and 8 clocks for each channel
Available operations	• Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascade connection operation available	• Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase PWM output by combination with synchronous operation • Cascade connection operation available
Buffer operation	• Channels 0, 3, 6, and 9 • Automatic transfer of register data	• Channels 0 and 3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, 5, 7, 8, 10, and 11	Channels 1, 2, 4, and 5
Interrupt sources	52 (Unit 0: 26, unit 1: 26)	26
Trigger generation	Programmable pulse generator (PPG) output trigger generation is available.	—
	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.41 Comparative Overview of 16-Bit Timer Pulse Unit Registers

Register	Bit	RX630 (TPUa)	RX231 (TPUa)
TPUA.TSTR: RX630 TSTR: RX231	—	Timer start register (Unit 0)	Timer start register
TPUB.TSTR	—	Timer start register (Unit 1)	—
TPUA.TSYR: RX630 TSYR: RX231	—	Timer synchronous register (Unit 0)	Timer synchronous register
TPUB.TSYR	—	Timer synchronous register (Unit 1)	—

2.22 8-Bit Timer

Table 2.42 shows a comparative overview of 8-bit timer specifications, and Table 2.43 shows a comparative overview of the 8-bit timer registers.

Table 2.42 Comparative Overview of 8-Bit Timer Specifications

Item	RX630 (TMR)	RX231 (TMR)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A, compare match B, and external reset signal.	Selectable among compare match A, compare match B, and external reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 and TMR2)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 and TMR2) (2) Event counter (TMR0 and TMR2) (3) Counter restart (TMR0 and TMR2)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	—
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of baud rate clock for SCI
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

Table 2.43 Comparative Overview of 8-Bit Timer Registers

Register	Bit	RX630 (TMR)	RX231 (TMR)
TCSR	ADTE	A/D trigger enable bit	—
TCSTR	—	—	Time counter start register

2.23 Compare Match Timer

Table 2.44 shows a comparative overview of the compare match timer specifications.

Table 2.44 Comparative Overview of Compare Match Timer Specifications

Item	RX630 (CMT)	RX231 (CMT)
Count clocks	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested individually for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.24 Realtime Clock

Table 2.45 shows a comparative overview of the realtime clock specifications, and Table 2.46 shows a comparative overview of the realtime clock registers.

Table 2.45 Comparative Overview of Realtime Clock Specifications

Item	RX630 (RTCa)	RX231 (RTCe)
Count modes	Calendar count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupt	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated to indicate when a carry occurs on the second counter, or when the 64 Hz counter is read at the same time as a carry occurs on the 64 Hz counter.	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time.

Item	RX630 (RTCa)	RX231 (RTCe)
Interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	• Time capture using edge detection on the time capture event input pin is available. • At each input event the month, date, hour, minute, and second is captured.	• Time capture using edge detection on the time capture event input pin is available. • At each input event the month, date, hour, minute, and second is captured, or the 32-bit binary counter value is captured.
Event link function	—	Periodic event output

Table 2.46 Comparative Overview of Realtime Clock Registers

Register	Bit	RX630 (RTCd)	RX231 (RTCe)
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
BCNT2AR*1	—	—	Binary counter 2 alarm register
BCNT3AR*1	—	—	Binary counter 3 alarm register
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit

Register	Bit	RX630 (RTCd)	RX231 (RTCe)
RCR1	PES[3:0]	Periodic interrupt select bits b7 b4 0 1 1 0: A periodic interrupt is generated every 1/256 second. (However, when the main clock is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0110b, a periodic interrupt is generated every 1/128 second.) 0 1 1 1: A periodic interrupt is generated every 1/128 second. 1 0 0 0: A periodic interrupt is generated every 1/64 second. 1 0 0 1: A periodic interrupt is generated every 1/32 second. 1 0 1 0: A periodic interrupt is generated every 1/16 second. 1 0 1 1: A periodic interrupt is generated every 1/8 second. 1 1 0 0: A periodic interrupt is generated every 1/4 second. 1 1 0 1: A periodic interrupt is generated every 1/2 second. 1 1 1 0: A periodic interrupt is generated every 1 second. 1 1 1 1: A periodic interrupt is generated every 2 seconds. Do not set to values other than the above.	Periodic interrupt select bits b7 b4 0 1 1 0: A periodic interrupt is generated every 1/256 second. 0 1 1 1: A periodic interrupt is generated every 1/128 second. 1 0 0 0: A periodic interrupt is generated every 1/64 second. 1 0 0 1: A periodic interrupt is generated every 1/32 second. 1 0 1 0: A periodic interrupt is generated every 1/16 second. 1 0 1 1: A periodic interrupt is generated every 1/8 second. 1 1 0 0: A periodic interrupt is generated every 1/4 second. 1 1 0 1: A periodic interrupt is generated every 1/2 second. 1 1 1 0: A periodic interrupt is generated every 1 second. 1 1 1 1: A periodic interrupt is generated every 2 seconds. Do not set to values other than the above.
RCR2	CNTMD	—	Count mode select bit
RCR3	RTCDV[2:0]	—	Sub-clock oscillator drive capacity control bits
RCR4	—	RTC control register 4	—
RFRH/L	—	Frequency register H/L	—
BCNT0CPy*1	—	—	BCNT0 capture register y (y = 0 to 2)
BCNT1CPy*1	—	—	BCNT1 capture register y (y = 0 to 2)
BCNT2CPy*1	—	—	BCNT2 capture register y (y = 0 to 2)
BCNT3CPy*1	—	—	BCNT3 capture register y (y = 0 to 2)

Note 1. In binary count mode

2.25 Independent Watchdog Timer

Table 2.47 shows a comparative overview of the independent watchdog timer specifications, and Table 2.48 shows a comparative overview of the independent watchdog timer registers.

Table 2.47 Comparative Overview of Independent Watchdog Timer Specifications

Item	RX630 (IWDTa)	RX231 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Count restart (auto-start mode: count restarts automatically; register start mode: count restarts after the counter is refreshed)	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Count restart (auto-start mode: count restarts automatically after a reset or output of a non-maskable interrupt request; register start mode: count restarts after the counter is refreshed)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Interrupt sources	Non-maskable interrupts • Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)	Non-maskable interrupt sources • Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX630 (IWDTa)	RX231 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.48 Comparative Overview of Independent Watchdog Timer Registers

Register	Bit	RX630 (IWDTa)	RX231 (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode

2.26 USB 2.0 Function Module

Table 2.49 shows a comparative overview of the USB 2.0 function module specifications, and Table 2.50 shows a comparative overview of the USB 2.0 function module registers.

Table 2.49 Comparative Overview of USB 2.0 Function Module Specifications

Item	RX630 (USBa)	RX231 (USBd)
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 • 1 port	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 Support for host controller, function controller, and on-the-go (OTG) functionality (1 channel) • Software can switch between the Host controller and function controller modes.
	• Self-power mode or bus-power mode can be selected. • Transfer interval setting function for isochronous and interrupt transfers	• Self-power mode or bus-power mode can be selected. • Battery Charging Specification, Revision 1.2 (BC1.2) is supported.
	—	When host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers
	• Support for full-speed transfer (12 Mbps) (Low-speed transfer (1.5 Mbps) is not supported when function controller operation is selected.) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	When function controller operation is selected: • Support for full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer

Item	RX630 (USBa)	RX231 (USBd)
Pipe configuration	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer: 64-bytes single buffer • PIPE1 and PIPE2: Ability to specify 64-byte double buffering for bulk transfer Ability to specify 256-byte double buffering for isochronous transfer • PIPE3 to PIPE5: Ability to specify 64-byte double buffering for bulk transfer • PIPE6 to PIPE9: Interrupt transfer: 64-bytes single buffer	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer: 64-bytes single buffer • PIPE1 and PIPE2: Ability to specify 64-byte double buffering for bulk transfer Ability to specify 256-byte double buffering for isochronous transfer • PIPE3 to PIPE5: Ability to specify 64-byte double buffering for bulk transfer • PIPE6 to PIPE9: Interrupt transfer: 64-bytes single buffer
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip DP/DM pull-up and pull-down resistors
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.50 Comparative Overview of USB 2.0 Function Module Registers

Register	Bit	RX630 (USBa)	RX231 (USBd)
SYSCFG	DMRPU	—	D– line resister control bit
	DRPD	—	D+/D– line resister control bit
	DCFM	—	Controller function select bit
	CNEN	—	Single end receiver enable bit
SYSSTS0	LNST[1:0]	USB data line status monitor bits b1b0 0 0: SE0 0 1: J-State 1 0: K-State 1 1: SE1	USB data line status monitor bits Low-speed operation b1b0 0 0: SE0 0 1: K-State 1 0: J-State 1 1: SE1 Full-speed operation b1b0 0 0: SE0 0 1: J-State 1 0: K-State 1 1: SE1
	IDMON	—	External ID0 input pin monitor bit
	HTACT	—	USB host sequencer status monitor bit
	OVCMON [1:0]	—	USB data line status monitor bit
DVSTCTR0	RHST[2:0]	USB bus reset status flag b2 b0 0 0 0: Communication speed not determined 1 0 0: USB bus reset in progress 0 1 0: Full-speed connection	USB bus reset status bits • When the Host controller is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection • When the Function controller is selected b2 b0 0 0 0: Communication speed not determined 0 1 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection
	UACT	—	USB bus enable bit
	RESUME	—	Resume output bit
	USBRST	—	USB bus reset output bit
	RWUPE	—	Wakeup detection enable bit

Register	Bit	RX630 (USBa)	RX231 (USBd)
DVSTCTR0	VBUSEN	—	USB0_VBUSEN output pin control bit
	EXICEN	—	USB0_EXICEN output pin control bit
	HNPBTOA	—	Host negotiation protocol (HNP) control bit
INTENB1	—	—	Interrupt enable register 1
SOFCFG	TRNENSEL	—	Transaction-enabled time select bit (When stopping the USB module clock, confirm that this bit has been cleared to 0.)
INTSTS1	—	—	Interrupt status register 1
DVCHGR	—	Device state changing register	—
USBADDR	—	USB address register	—
DCPCFG	—	—	DCP configuration register
DCPMAXP	DEVSEL [3:0]	—	Device select bits
DCPCTR	SUREQCLR	—	SUREQ bit clear bit
	SUREQ	—	SETUP token transmission bit
PIPEMAXP	DEVSEL [3:0]	—	Device select bits
DEVADDn	—	—	Device address n configuration register (n = 0 to 5)
USBMC	—	—	USB module control register
USBBCCTRL0	—	—	BC control register 0
DPUSR0R	—	Deep standby USB transceiver control/pin monitor register	—
DPUSR1R	—	Deep standby USB suspend/ resume interrupt register	—

2.27 Serial Communication Interface

The RX630 Group has 9 independent serial communications interface channels (SCIc: 8 channels, SCId: 1 channel).

The RX231 Group has 7 independent serial communications interface channels (SCIg: 6 channels, SCIh: 1 channel).

Table 2.51 shows a comparative overview of the SCIc specifications, Table 2.52 shows a comparative overview of the SCId specifications, Table 2.53 shows a comparative overview of the SCI channel specifications, and Table 2.54 shows a comparative overview of the serial communications interface registers.

Table 2.51 Comparative Overview of SCIc Specifications

Item		RX630 (SCIc)	RX231 (SCIg)
Number of channels		8 channels	6 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX630 (SCIc)	RX231 (SCIg)
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
Asynchronous mode	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Maximum 384 kbps Fast mode is supported.	Fast mode is supported.
	Noise canceler	• The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters. • The noise cancellation bandwidth is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters. • The noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Item	RX630 (SCIc)	RX231 (SCIg)
Event link function	—	Error (receive error, error signal detection) event output
	—	Receive data full event output
	—	Transmit data empty event output
	—	Transmit end event output

Table 2.52 Comparative Overview of SCId Specifications

Item		RX630 (SCId)	RX231 (SCIh)
Number of channels		1 channel	1 channel
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Module stop state can be set.	Module stop state can be set.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Low level detection	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the internal register directly.	When a framing error occurs, a break can be detected by reading the internal register directly.
	Clock source	An internal or external clock can be selected.	An internal or external clock can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.

Item		RX630 (SCId)	RX231 (SCIh)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	• The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters. • The noise cancellation bandwidth is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters. • The noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX630 (SCId)	RX231 (SCIh)
Extended serial mode	Start frame transmission	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection
	Start frame reception	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates
	I/O control functions	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCId when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 2.53 Comparative Overview of SCI Channel Specifications

Item	RX630 (SCIc, SCId)	RX231 (SCIg and SCIh)
Asynchronous mode	SCI0, SCI1, SCI2, SCI3, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple I²C mode	SCI0, SCI1, SCI2, SCI3, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI5, SCI6, SCI8, SCI9, SCI12	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5

Table 2.54 Comparative Overview of Serial Communication Interface Registers

Register	Bit	RX630 (SCIc and SCId)	RX231 (SCIg and SCIh)
SMR	PM	Parity Mode (Valid only when the PE bit is 1 in asynchronous mode) 0: Selects even parity 1: Selects odd parity	Parity Mode (Valid only when the PE bit is 1) 0: Selects even parity 1: Selects odd parity
	CHR	Character Length (Valid only in asynchronous mode) 0: Selects 8 bits as the data length 1: Selects 7 bits as the data length	Character Length (Valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communications Mode 0: Asynchronous mode 1: Clock synchronous mode	Communications Mode 0: Asynchronous mode or simple I2C mode 1: Clock synchronous mode or simple SPI mode
SSR	RDRF	—	Receive data full flag
	TDRE	—	Receive data empty flag
SCMR	CHR1	—	Character length bit 1
SEMR	BRME	—	Bit rate modulation enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
TDRHL	—	—	Transmit data register HL
RDRHL	—	—	Receive data register HL

Register	Bit	RX630 (SCIc and SCId)	RX231 (SCIg and SCIh)
MDDR	—		Modulation duty register
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited.	Bus collision detection clock select bits • When SEMR.BGDM bit = 0, or SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = other than 00b b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited. • When SEMR.BGDM bit = 1 and SMR.CKS[1.0] bits = 00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited. 1 1: Setting prohibited.

2.28 I²C Bus Interface

Table 2.55 shows a comparative overview of the I²C bus interface specifications, and Table 2.56 shows a comparative overview of the I²C bus interface registers.

Table 2.55 Comparative Overview of I²C Bus Interface Specifications

Item	RX630 (RIIC)	RX231 (RIICa)
Number of channels	4 channels	1 channel
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 1 Mbps	Fast mode is supported. (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX630 (RIIC)	RX231 (RIICa)
Arbitration	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Module stop state can be set.
RIIC operating modes	4 modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	4 modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

Item	RX630 (RIIC)	RX231 (RIICa)
Event link function	—	Four sources • Communication error or event occurrence Arbitration detection, NACK detection, timeout detection, start condition detection (including restart condition), stop condition detection • Receive data full • Transmit data empty • Transmit end

Table 2.56 Comparative Overview of I²C Bus Interface Registers

Register	Bit	RX630 (RIIC)	RX231 (RIICa)
ICMR2	TWME	Timeout internal counter write enable bit	—
ICFER	FMPE	Fast-mode plus enable bit	—
TMOCNTL	—	Timeout internal counter L	—
TMOCNTU	—	Timeout internal counter U	—

2.29 CAN Module

Table 2.57 shows a comparative overview of the CAN module specifications, and Table 2.58 shows a comparative overview of the CAN module registers.

Table 2.57 Comparative Overview of CAN Module Interface Specifications

Item	RX630 (CAN)	RX231 (RSCAN)
Number of channels	1 channel on products with 512 KB or less of RAM 2 channels on products with 768 KB or more of RAM	1 channel
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Maximum 1 Mbps
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	16 message boxes
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (standard ID, extended ID, or both IDs) • Sets interrupt enable/disable for each FIFO. • Mirror function (to receive messages transmitted from own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Refer to reception filtering function.

Item	RX630 (CAN)	RX231 (RSCAN)
Reception filtering function	—	• Ability to select receive messages using a total of 16 receive rules • Ability to set the number of receive rules (0 to 16) for each channel • Acceptance filtering: Ability to set ID and mask for each receive rule • DLC filter processing: Ability to specify DLC filter checking for each receive rule
Receive message transfer function	—	• Routing function Ability to transfer receive messages to user-defined buffers (max. transfer buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, or transmit/receive FIFO buffer • Label addition function Ability to simultaneously store label information when storing a message in a receive buffer and FIFO buffer
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Ability to select ID priority mode or mailbox number priority mode • Ability to abort transmission requests (and ability to confirm abort completion with a flag) • Ability to enable or disable transmit end interrupt individually by mailbox	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (standard ID, extended ID, or both IDs) • Programmable one-shot transmission function • Ability to select ID priority transmission or transmit buffer number priority transmission • Transmit abort function (with ability to confirm abort completion with a flag) • Ability to enable or disable interrupt individually by transmit buffer or transmit/receive FIFO buffer
Interval transmission function	—	Ability to set the message transmission interval time (transmit mode of transmit/receive FIFO buffers)
Transmit history function	—	Function for storing history information for transmitted messages
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to channel halt mode at bus-off entry • Automatic transition to channel halt mode at bus-off end • Transition to channel halt mode by a program • Transition to error-active state by a program (forcible return from the bus-off state)

Item	RX630 (CAN)	RX231 (RSCAN)
Error status monitoring	• Monitoring of CAN bus errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, and ACK delimiter errors) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • The error counters can be read.	• Monitoring of CAN protocol errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, ACK delimiter errors, and bus dominant locking) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • The error counters can be read. • DLC error monitoring
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • Time stamp clock source division function
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	• 5 • Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channels (3 sources per channel) Channel transmit interrupts — Transmit end interrupt — Transmit abort interrupt — Transmit/receive FIFO transmit end interrupt — Transmit history interrupt Transmit/receive FIFO receive interrupt Channel error interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	—
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLK), CANMCLK
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.58 Comparative Overview of CAN Module Registers

Register	Bit	RX630 (CAN)	RX231 (RSCAN)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0	—	FIFO received ID compare register 0	—
FIDCR1	—	FIFO received ID compare register 1	—
MKIVLR	—	Mask invalid register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 31)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source judge register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code store register	—
TSR	—	Time stamp register	—
TCR	—	Test control register	—
CFGL	—	—	Bit configuration register L
CFGH	—	—	Bit configuration register H
CTRL	—	—	Control register L
CTRH	—	—	Control register H
STSL	—	—	Status register L
STSH	—	—	Status register H
ERFLL	—	—	Error flag register L
ERFLH	—	—	Error flag register H
GCFGL	—	—	Global configuration register L
GCFGH	—	—	Global configuration register H
GCTRL	—	—	Global control register L
GCTRH	—	—	Global control register H
GSTS	—	—	Global status register
GERFLL	—	—	Global error flag register
GTINTSTS	—	—	Global transmit interrupt status register
GTSC	—	—	Timestamp register
GAFLCFG	—	—	Receive rule number configuration register
GAFLIDLj	—	—	Receive rule entry register jAL (j = 0 to 15)
GAFLIDHj	—	—	Receive rule entry register jAH (j = 0 to 15)

Register	Bit	RX630 (CAN)	RX231 (RSCAN)
GAFLMLj	—	—	Receive rule entry register jBL (j = 0 to 15)
GAFLMHj	—	—	Receive rule entry register jBH (j = 0 to 15)
GAFLPLj	—	—	Receive rule entry register jCL (j = 0 to 15)
GAFLPHj	—	—	Receive rule entry register jCH (j = 0 to 15)
RMNB	—	—	Receive buffer number configuration register
RMND0	—	—	Receive buffer receive complete flag register
RMIDLn	—	—	Receive buffer register nAL (n = 0 to 15)
RMIDHn	—	—	Receive buffer register nAH (n = 0 to 15)
RMTSn	—	—	Receive buffer register nBL (n = 0 to 15)
RMPTRn	—	—	Receive buffer register nBH (n = 0 to 15)
RMDF0n	—	—	Receive buffer register nCL (n = 0 to 15)
RMDF1n	—	—	Receive buffer register nCH (n = 0 to 15)
RMDF2n	—	—	Receive buffer register nDL (n = 0 to 15)
RMDF3n	—	—	Receive buffer register nDH (n = 0 to 15)
RFCCm	—	—	Receive FIFO control register m (m = 0 or 1)
RFSTSm	—	—	Receive FIFO status register m (m = 0 or 1)
RFPCTRm	—	—	Receive FIFO pointer control register m (m = 0 or 1)
RFIDLm	—	—	Receive FIFO access register mAL (m = 0 or 1)
RFIDHm	—	—	Receive FIFO access register mAH (m = 0 or 1)
RFTSm	—	—	Receive FIFO access register mBL (m = 0 or 1)
RFPTRm	—	—	Receive FIFO access register mBH (m = 0 or 1)
RFDF0m	—	—	Receive FIFO access register mCL (m = 0 or 1)
RFDF1m	—	—	Receive FIFO access register mCH (m = 0 or 1)
RFDF2m	—	—	Receive FIFO access register mDL (m = 0 or 1)
RFDF3m	—	—	Receive FIFO access register mDH (m = 0 or 1)

Register	Bit	RX630 (CAN)	RX231 (RSCAN)
CFCCL0	—	—	Transmit/receive FIFO control register 0L
CFCCH0	—	—	Transmit/receive FIFO control register 0H
CFSTS0	—	—	Transmit/receive FIFO status register 0
CFPCTR0	—	—	Transmit/receive FIFO pointer control register 0
CFIDL0	—	—	Transmit/receive FIFO access register 0AL
CFIDH0	—	—	Transmit/receive FIFO access register 0AH
CFTS0	—	—	Transmit/receive FIFO access register 0BL
CFPTR0	—	—	Transmit/receive FIFO access register 0BH
CFDF00	—	—	Transmit/receive FIFO access register 0CL
CFDF10	—	—	Transmit/receive FIFO access register 0CH
CFDF20	—	—	Transmit/receive FIFO access register 0DL
CFDF30	—	—	Transmit/receive FIFO access register 0DH
RFMSTS	—	—	Receive FIFO message lost status register
CFMSTS	—	—	Transmit/receive FIFO message lost status register
RFISTS	—	—	Receive FIFO interrupt status register
CFISTS	—	—	Transmit/receive FIFO receive interrupt status register
TMCp	—	—	Transmit buffer control register p (p = 0 to 3)
TMSTSp	—	—	Transmit buffer status register p (p = 0 to 3)
TMTRSTS	—	—	Transmit buffer transmit request status register
TMTCSTS	—	—	Transmit buffer transmit complete status register
TMTASTS	—	—	Transmit buffer transmit abort status register
TMIEC	—	—	Transmit buffer interrupt enable register
TMIDLp	—	—	Transmit buffer register pAL (p = 0 to 3)
TMIDHp	—	—	Transmit buffer register pAH (p = 0 to 3)
TMPTRp	—	—	Transmit buffer register pBH (p = 0 to 3)
TMDF0p	—	—	Transmit buffer register pCL (p = 0 to 3)

Register	Bit	RX630 (CAN)	RX231 (RSCAN)
TMDF1p	—	—	Transmit buffer register pCH (p = 0 to 3)
TMDF2p	—	—	Transmit buffer register pDL (p = 0 to 3)
TMDF3p	—	—	Transmit buffer register pDH (p = 0 to 3)
THLCC0	—	—	Transmit history buffer control register
THLSTS0	—	—	Transmit history buffer status register
THLACC0	—	—	Transmit history buffer access register
THLPCTR0	—	—	Transmit history buffer pointer control register
GRWCR	—	—	Global RAM window control register
GTSTCFG	—	—	Global test configuration register
GTSTCTRL	—	—	Global test control register
GLOCKK	—	—	Global test protection unlock register
RPGACCr	—	—	RAM test register r (r = 0 to 127)

2.30 Serial Peripheral Interface

Table 2.59 shows a comparative overview of the serial peripheral interface specifications, and Table 2.60 shows a comparative overview of the serial peripheral interface registers.

Table 2.59 Comparative Overview of Serial Peripheral Interface Specifications

Item	RX630 (RSPI)	RX231 (RSPIa)
Number of channels	2 channels	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.

Item	RX630 (RSPI)	RX231 (RSPIa)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection When master receive and the RSPCK auto-stop function are enabled, the transfer clock stops at the point in time when overrun error detection occurs, so no overrun error is generated. • Parity error detection
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pins is input, and SSLn1 to SSLn3 pins are either output or unused. • In slave mode: SSLn0 pins is input, and SSLn1 to SSLn3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)

Item	RX630 (RSPI)	RX231 (RSPIa)
Event link function (output)	—	The following events can be output to the event link controller (RSPI0): • Receive buffer run event signal • Transmit buffer empty event signal • Mode fault, overrun, or parity error event signal • RSPI idle event signal • Transmit end event signal
Other functions	• Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.60 Comparative Overview of Serial Peripheral Interface Registers

Register	Bit	RX630 (RSPI)	RX231 (RSPIa)
SPSR	SPTEF	—	Transmit buffer empty flag
	SPRF	—	Receive buffer full flag
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit

2.31 12-Bit A/D Converter

Table 2.61 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.62 shows a comparative overview of the 12-bit A/D converter registers.

Table 2.61 Comparative Overview of 12-Bit A/D Converter Specifications

Item	RX630 (S12ADa)	RX231 (S12ADE)
Number of units	1 units	1 unit
Input channels	21 channels	24 channels
Extended analog inputs	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz)	0.83 µs per channel (when operating with A/D conversion clock ADCLK = 54 MHz)
A/D conversion clock (ADCLK)	4 clocks: PCLK, PCLK/2, PCLK/4, PCLK/8	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: PCLKB: ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• For analog input: 21 data registers • For temperature sensor: One data register • For internal reference voltage: One data register • The results of A/D conversion are stored in 12-bit A/D data registers. • In A/D-converted value addition mode, A/D conversion results are stored in a 14-bit A/D data register.	• For analog input: 24 data registers one data register for each unit for A/D conversion data duplication in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX630 (S12ADa)	RX231 (S12ADE)
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 21 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 21 user-selected channels. (Continuous scan mode should not be used when temperature sensor output or the internal reference voltage is selected.)	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 user-selected channels. • Group scan mode: — Analog inputs of up to 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected as a group unit is performed only once. — The scanning start conditions (synchronous trigger) for group A and group B can be selected independently, allowing A/D conversion of group A and group B to be started at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, and TMR. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (unit 0).

Item	RX630 (S12ADa)	RX231 (S12ADE)
Functions	• Variable sampling state count • A/D-converted value adding mode	• Sample-and-hold function • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • A/D data register auto-clear function • Compare function (window A, window B) • 16 ring buffers when the compare function is used
Interrupt sources	• An scan end interrupt request (S12ADI0) can be generated on completion of A/D conversion. • A S12ADI0 interrupt can activate the DMAC and DTC.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated group B or group C scan end interrupt request (GBADI) can be generated. • The DMAC or DTC can be activated by the S12ADI0 or GBADI interrupt.

Item	RX630 (S12ADa)	RX231 (S12ADE)
Event link function	—	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	It is possible to specify transition to the module-stop state. (When the module-stop state is canceled, A/D conversion can be started after 10 ms has elapsed.)	It is possible to specify transition to the module-stop state. (When the module-stop state is canceled, A/D conversion can be started after at least 1 µs has elapsed.)

Table 2.62 Comparative Overview of 12-Bit A/D Converter Registers

Register	Bit	RX630 (S12ADa)	RX231 (S12ADE)
ADDBLDR	—	—	A/D data duplication register
ADRD	—	—	A/D self-diagnostic data register
ADCSR	DBLANS [4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger start enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	A/D conversion clock select bits	—
	ADHSC	—	A/D conversion select bit
	ADIE	Scan end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS: RX630 ADCS[1:0]: RX231	Scan mode select bit 0: Single scan mode 1: Continuous scan mode	Scan mode select bit b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D conversion start bit (b7)	A/D conversion start bit (b15)
ADANS0	—	A/D conversion channel select bit 0	—
ADANS1	—	A/D conversion channel select bit 1	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1

Register	Bit	RX630 (S12ADa)	RX231 (S12ADE)
ADADS0	—	A/D-converted value addition mode select register 0	A/D-converted value addition/averaging channel select register 0
ADADS1	—	A/D-converted value addition mode select register 1	A/D-converted value addition/averaging channel select register 1
ADADC	ADC[1:0]: RX630 ADC[2:0]: RX231	Addition count select bits b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition count select bits b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Do not set to values other than the above.
	AVEE	—	Average mode enable bit
ADCER	DIAGVAL [1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	ADSTRS [3:0]	A/D conversion start trigger select bits	—
	TRSB[5:0]	—	A/D conversion start trigger for group B select bits
	TRSA[5:0]	—	A/D conversion start trigger select bits
ADEXICR	TSSAD	Temperature sensor output A/D-converted value addition mode select bit	Temperature sensor output A/D-converted value addition/averaging mode select bit
	OCSAD	Internal reference voltage A/D conversion select bit	Internal reference voltage A/D-converted value addition/averaging mode select bit
	TSS: RX630 TSSA: RX231	Temperature sensor output A/D conversion select bit	Temperature sensor output A/D conversion select bit
	OCS: RX630 OCSA: RX231	Internal reference voltage A/D-conversion select bit	Internal reference voltage A/D-conversion select bit
ADDRy	—	A/D data register y (y = 0 to 20)	A/D data register y (y = 0 to 7, 16 to 31)
ADSSTR01	—	A/D sampling state register 01	—
ADSSTR23	—	A/D sampling state register 23	—

Register	Bit	RX630 (S12ADa)	RX231 (S12ADE)
ADSSTRn	—	—	A/D sampling state register n (n = 0 to 7, L, T, and O)
ADDISCR	—	—	A/D disconnection detection controller
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A compare condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A compare condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADHVREFCNT	—	—	A/D high-side/low-side reference voltage control register
ADWINMON	—	—	A/D comparison function window A/B status monitor register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADBUFn			A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register

2.32 D/A Converter

Table 2.63 shows a comparative overview of the D/A converter specifications, and Table 2.64 shows a comparative overview of the D/A converter registers.

Table 2.63 Comparative Overview of D/A Converter Specifications

Item	RX630 (DAa)	RX231 (R12DAA)
Resolution	10 bits	12 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	• Measure against interference between D/A and A/D conversion: (Products with a ROM capacity of 1.5 MB or more are not equipped with a function to prevent mutual interference between analog modules.) D/A converted data update timing is controlled by the 10-bit A/D converter synchronous D/A conversion enable input signal output by the the 10-bit A/D converter. (Degradation of A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.)	• Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the the 12-bit A/D converter. Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	Module stop state can be set.	Module stop state can be set.
Event link function (input)	—	Ability to activate DA0 by event signal input

Table 2.64 Comparative Overview of D/A Converter Registers

Register	Bit	RX630 (DAa)	RX231 (R12DAA)
DADRm) (m = 0, 1)	—	D/A Data Register m • DADPR.DPSEL bit = 0 (data is flush with the right end of the register) Data placement : b9 to b0 • DADPR.DPSEL bit = 1 (data is flush with the left end of the register) Data placement : b15 to b6	D/A Data Register m • DADPR.DPSEL bit = 0 (data is flush with the right end of the register) Data placement : b11 to b0 • DADPR.DPSEL bit = 1 (data is flush with the left end of the register) Data placement : b15 to b4
DACR	DAE	D/A enable bit	—
DAADSCR	DAADST	D/A A/D synchronous conversion bit 0: D/A converter operation is not synchronized with 10-bit A/D converter operation (function to prevent mutual interference between D/A and A/D conversion disabled). 1: D/A converter operation is synchronized with 10-bit A/D converter operation (function to prevent mutual interference between D/A and A/D conversion enabled).	D/A A/D synchronous conversion bit 0: D/A converter operation is not synchronized with 12-bit A/D converter operation (function to prevent mutual interference between D/A and A/D conversion disabled). 1: D/A converter operation is synchronized with 12-bit A/D converter operation (function to prevent mutual interference between D/A and A/D conversion enabled).
DAVREFCR	—	—	D/A VREF control regsiter

2.33 Temperature Sensor

Table 2.65 shows a comparative overview of the temperature sensor specifications, and Table 2.66 shows a comparative overview of the temperature sensor register.

Table 2.65 Comparative Overview of D/A Converter Specifications

Item	RX630 (TEMPS)	RX231 (TEMPSA)
Temperature sensor voltage output	12-bit A/D converter	Output to the 12-bit A/D converter
Low power consumption function	Module stop state can be set.	—
Temperature sensor calibration data registers	These registers store temperature sensor reference data measured for each chip at the time of shipment. (Calibration data registers are provided on version G products only.)	These registers store temperature sensor reference data measured for each chip at the time of shipment.

Table 2.66 Comparative Overview of Temperature Sensor Register

Register	Bit	RX630 (TEMPS)	RX231 (TEMPSA)
TSCR	—	Temperature sensor control register	—

2.34 RAM

Table 2.67 shows a comparative overview of the RAM specifications.

Table 2.67 Comparative Overview of RAM Specifications

Item	RX630	RX231
RAM capacity	• 64 KB RAM0: 64 KB • 96 KB RAM0: 64 KB, RAM1: 32 KB • 128 KB RAM0: 64 KB, RAM1: 64 KB	• 32 KB RAM0: 32 KB • 64 KB RAM0: 64 KB
RAM address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh • When the RAM capacity is 96 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 7FFFh • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 FFFFh	• When the RAM capacity is 32 KB RAM0: 0000 0000h to 0000 7FFFh • When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Data retention function	Data in RAM0 can be retained in deep software standby mode.	—
Low power consumption function	The module-stop state is independently selectable for RAM0 and RAM1.	Module stop state can be set.

2.35 Flash Memory (ROM)

Table 2.68 shows a comparative overview of the flash memory specifications, and Table 2.69 shows a comparative overview of the flash memory registers.

Table 2.68 Comparative Overview of Flash Memory Specifications

Item	RX630	RX231
Memory space	• User area: Maximum 2 MB • Data area: 32 KB • User boot area: 16 KB	• User area: Maximum 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID.
Read cycle	• Code flash High-speed read operation using 1 cycle of ICLK is supported. • E2 DataFlash A read operation requires 6 FCLK cycles during word or byte access.	Less than 32 MHz: No-wait memory access 32 MHz to 54 MHz: Wait states. No wait state if the instruction is served by a ROM accelerator hit.
Value after erase	• Code flash FFh • E2 DataFlash Undefined value	• ROM FFh • E2 DataFlash FFh
Programming/ erasing method	• On-chip dedicated sequencer (FCU) for programming the ROM/E2 DataFlash • Programming/erasing the ROM are handled by issuing commands to the FCU. • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	• Following transition to a dedicated sequencer mode for programming and erasing, programming and erasing can be accomplished by issuing programming and erasing commands. • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Prevents unauthorized modification or reading of data.	Prevents unauthorized modification or reading of data.
Protection function	• Software-controlled protection function: Registers and lock bits can be set to prevent unintentional programming. • FCU command-lock function: When abnormal operations are detected during programming/erasure, any further programming/erasure is disabled.	• Prevents unintentional programming of the flash memory.
Background operation (BGO) function	The CPU can run programs in the ROM area while the E2 DataFlash is being programmed or erased.	Programs in the ROM can be executed while the E2 DataFlash is being programmed.

Item	RX630	RX231
Suspend/resume function	• Halts (suspends) programming/erasure of the ROM, allowing the CPU to execute program code from the ROM area. • Programming/erasure of the ROM can be restarted (resumed) after suspension.	—
Units of programming and erasure	• Programming the user area and user boot area: 128 bytes • Erasing the user area: One block (64, 32, 16, 4 KB) • Erasing the user boot area: 16 KB • Programming the data area: 2 bytes • Erasing the data area: One block (32 KB)	• Programming the user area: 8 bytes • Erasing the user area: One block (2 KB) • Programming the data area: 4 bytes • Erasing the data area: One block (1 KB)
Other functions	Ability to accept interrupts during self-programming	Ability to accept interrupts during self-programming
	Ability to specify initial settings for the microcontroller in option-setting memory	Ability to specify initial settings for the microcontroller in option-setting memory
	—	Ability to select block 0 to 7 or 8 to 15 as the startup area of the code flash memory
On-board programming	• Programming in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Programming in USB boot mode — USB0 is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming in user boot mode — Users can create their own boot programs. • Programming by a routine for ROM programming within the user program — This allows ROM programming without resetting the system.	• Programming in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming in boot mode (USB interface) — Channel 0 (USB0) of the USB 2.0 Function module is used. — A personal computer can be connected using only a USB cable. — Flash programming can be performed in either self-powered or bus-powered mode. • Programming in boot mode (FINE interface) — Uses FINE. • Programming/erasing by a routine for flash programming within the user program — This allows ROM programming without resetting the system.
Programming/ erasing with dedicated parallel programmer	A flash programmer can be used to program the user area and user boot area. (It is not possible to program the data area using a flash programmer.)	A flash programmer (serial programmer or parallel programmer) can be used to program the user area and data area.

Item	RX630	RX231
Unique ID	A unique 16-byte ID code is provided for each MCU. (The unique ID is only available for the G-version products.)	A unique 16-byte ID code is provided for each MCU.
ID code protect	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with a parallel programmer can be enabled or disabled using ROM codes.	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes. • Connection with a parallel programmer can be enabled or disabled using ROM codes.
Start-up program protection function	—	This function is used to safely rewrite blocks 0 to 7 (1 block = 2 KB).
Area protection	—	This function enables rewriting of only the specified range in the user area and disables rewriting of the other blocks during self-programming.

Table 2.69 Comparative Overview of Flash Memory Registers

Register	Bit	RX630	RX231
FWBn	—	—	Flash write buffer n register (n = 0 to 3)
FWEPROR	—	Flash P/E protection register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
DFLRE0	—	E2 DataFlash read enable register 0	—
DFLRE1	—	E2 DataFlash read enable register 1	—
DFLWE0	—	E2 DataFlash P/E enable register 0	—
DFLWE1	—	E2 DataFlash P/E enable register 1	—
FCURAME	—	FCURAM enable register	—
FSTATR0	PRGSPD	Programming suspend status flag	—
	ERSSPD	Erasure suspend status flag	—
	SUSRDY	Suspend ready flag	—
	PRGERR	Program error flag (b4)	Program error flag (b1)
	ERSERR: RX630 ERERR: RX231	Erasure error bit (b5)	Erase error flag (b0)
	ILGLERR	Illegal command error flag (b6)	Illegal command error flag (b4)
	FRDY	Flash ready flag	—
	BCERR	—	Blank check error flag
	EILGLERR	—	Extra area illegal command error flag
FSTATR1	FLOCKST	Lock bit status bit	—
	FCUERR	FCU error flag	—
	FRDY	—	Flash ready flag
	EXRDY	—	Extra area ready flag
DFLCTL	—	—	E2 DataFlash control register
FENTRYR	FENTRY1	ROM P/E mode entry bit 1	—
	FENTRY2	ROM P/E mode entry bit 2	—
	FENTRY3	ROM P/E mode entry bit 3	—
FPROTR	—	Flash protection register	—
FPR	—	—	Protection unlock register
FPSR	—	—	Protection unlock status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial setting register
FRESETR	FRKEY[7:0]	Key code	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
DFLBCCNT		E2 DataFlash blank check control register	—
FPESTAT		Flash P/E status register	—

Register	Bit	RX630	RX231
DFLBCSTAT		E2 DataFlash blank check status register	—
PCKAR		Peripheral clock notification register	—
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FWBn		—	Flash write buffer n register
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash start-up setting monitor register
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register

2.36 Flash memory (E2 DataFlash)

Table 2.70 shows a comparative overview of the flash memory (Data flash) specifications.

Table 2.70 Comparative Overview of Flash Memory (Data Flash) Specifications

Item	RX630	RX231
Memory capacity	32 Kbytes	8 Kbytes
Value after erasure	Undefined	FFh
Block configuration	Block: 32 bytes	Block: 1 Kbytes
Number of blocks	1024	8

2.37 Package (LQFP100 only)

There are some differences in the outline drawing of the LQFP100 package, so please be careful when designing the board.

For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.71 Comparison of package codes

Item	RX630	RX231
100 pin LQFP	PLQP0100KB-A	PLQP0100KB-B

3. Comparison of Pin Functions

A comparison of pin functions, power supplies, clocks, and system control pins is shown below. Items that apply to one group only are colored blue, while items that are implemented on both groups but with points of difference are colored red. Items are shown in **black** when there are no points of difference in their specifications.

3.1 100-Pin LQFP Package

Table 3.1 shows a comparative listing of the pin functions on the 100-pin LQFP package.

Table 3.1 Comparative Listing of Pin Functions on 100-pin LQFP Package

100-Pin LQFP	RX630	RX231
1	VREFH	VREFH
2	EMLE	P03/DA0
3	VREFL	VREFL
4	PJ3/MTIOC3C/CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#
5	VCL	VCL
6	VBATT	VBATT
7	MD/FINED	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL/P37	XTAL/P37
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36
14	VCC	VCC
15	P35/NMI	P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/POE2#/ SCK6/SCK0/IRQ4	P34/MTIOC0A/TMCI3/POE2#/SCK6/TS0/ IRQ4
17	P33/MTIOC0D/TIOCD0/TMRI3/PO11/ POE3#/RXD6/RXD0/SMISO6/SMISO0/ SSCL6/SSCL0/CRX0*1/IRQ3-DS	P33/MTIOC0D/TMRI3/POE3#/TIOCD0/RXD6/ SMISO6/SSCL6/TS1/IRQ3
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/CTX0*1/IRQ2-DS	P32/MTIOC0C/TMO3/TIOCC0/RTCOUT/ RTCIC2/TXD6/SMOSI6/SSDA6/ USB0_VBUSEN/IRQ2
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0/IRQ1-DS	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSISCK0/IRQ1
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB/ IRQ0-DS	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/ CMPOB3
21	TCK/FINEC/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB	P27/CS3#/MTIOC2B/TMCI3/SCK1/SSIWS0/ TS2/CVREFB3
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/SSIRXD0/TS3/CMPB3
23	P25/CS5#/MTIOC4C/MTCLKB/TIOCA4/PO5/ RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/TS4/ ADTRG0#
24	P24/CS4#/MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4/SCK3	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/ TIOCB4/USB0_VBUSEN/TS5

100-Pin LQFP	RX630	RX231
25	P23/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/ CTS0#/RTS0#/SMOSI3/SS0#/SSDA3	P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/ RTS0#/SS0#/SSISCK0/TS6
26	P22/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/ SCK0	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/ SCK0/USB0_OVRCURB/AUDIO_MCLK/TS7
27	P21/MTIOC1B/TIOCA3/TMCI0/PO1/RXD0/ SMISO0/SSCL0/IRQ9	P21/MTIOC1B/TMCI0/TIOCA3/RXD0/ SMISO0/SSCL0/USB0_EXICEN/SSIWS0/TS8
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/IRQ8	P20/MTIOC1A/TMRI0/TIOCB3/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/TS9
29	P17/MTIOC3A/MTIOC3B/TIOCB0/TCLKD/ TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/IETXD/IRQ7/ ADTRG#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA/SSITXD0/ IRQ7/CMPOB2
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/MOSIA/ SCL2-DS/IERXD/USB0_VBUS/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/ TCLKC/RTCOUT/TXD1/SMOSI1/SSDA1/ MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/ TCLKB/RXD1/SMISO1/SSCL1/CRXD0/TS12/ IRQ5/CMPB2
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/ TCLKA/CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA/TS13/IRQ4/CVREFB2
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG#	P13/MTIOC0B/TMO3/TIOCA5/SDA/IRQ3
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/SCL/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	USB0_DM
37	USB0_DP	USB0_DP
38	VSS_USB	VSS_USB
39	P55/WAIT#/MTIOC4D/TMO3/CRX1/IRQ10	P55/WAIT#/MTIOC4D/TMO3/CRXD0/TS15
40	P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/ SS2#/CTX1	P54/ALE/MTIOC4B/TMCI1/CTXD0/TS16
41	BCLK/P53*2	BCLK/P53/TS17
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3	P52/RD#/TS18
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2	P51/WR1#/BC1#/WAIT#/TS19
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1	P50/WR0#/WR#/TS20
45	PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ PO31/TXD8/SMOSI8/SSDA8/MISOA/IRQ14	UB*3/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TXD8/SMOSI8/SSDA8/MISOA/ CACREF
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ PO30/RXD8/SMISO8/SSCL8/MOSIA/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ RXD8/SMISO8/SSCL8/MOSIA/TS22
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/PO29/SCK8/RSPCKA	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA/TS23
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SSLA0	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/ SSLA0/SDHI_D1/TSCAP
49	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/IETXD	PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/ SSDA5/IRTXD5/SDHI_D0/TS27

100-Pin LQFP	RX630	RX231
50	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3/IERXD	PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/ SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30
51	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2/IRQ12	PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2/ TS33
52	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1/IRQ14	PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/ SS5#/SSLA1/TS35
53	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9	PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9/SDHI_D2
54	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9	PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/S SCL9/SDHI_D1
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE1#/SCK9	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/ TIOCB4/SCK9/USB0_VBUS/SDHI_CD
56	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE3#/SCK6	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/ TIOCD3/TCLKD/SCK6/SDHI_WP
58	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#	PB2/A10/TIOCC3/TCLKC/CTS6#/RTS6#/ SS6#
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/ TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/ CMPOB1
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/RSPCKA/IRQ12	PB0/A8/MTIC5W/TIOCA3/RXD6/SMISO6/ SSCL6/RSPCKA/SDHI_CMD
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/MISOA	PA7/A7/TIOCB2/MISOA
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/A6/MT/IC5V/MTCLKB/TMCI3/POE2#/ TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0
65	PA5/A5/TIOCB1/PO21/RSPCKA	PA5/A5/TIOCB1/RSPCKA
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0/ IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/ TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/ IRTXD5/IRQ5/CVREFB1
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/ RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/ IRQ6/CMPB1
68	PA2/A2/PO18/RXD5/SMISO5/SSCL5/SSLA3	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5
69	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/PO17/ SCK5/SSLA2/IRQ11	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/ SSLA2/SSISCK0
70	PA0/A0/BC0#/MTIOC4A/TIOCA0/PO16/ SSLA1	PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/ CACREF
71	PE7/D15[A15/D15]/MISOB/IRQ7/AN5	PE7/D15[A15/D15]/IRQ7/AN023
72	PE6/D14[A14/D14]/MOSIB/IRQ6/AN4	PE6/D14[A14/D14]/IRQ6/AN022
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ RSPCKB/IRQ5/AN3	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ IRQ5/AN021/CMPOB0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ PO28/SSLB0/AN2	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/ AN020/CMPA2/CLKOUT
75	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/ CTS12#/RTS12#/SS12#/MISOB/AN1	PE3/D11[A11/D11]/MTIOC4B/POE8#/ CTS12#/RTS12#/SS12#/AUDIO_MCLK/ AN019/CLKOUT

100-Pin LQFP	RX630	RX231
76	PE2/D10[A10/D10]/MTIOC4A/PO23/RXD12/ SMISO12/SSCL12/RXDX12/SSLB3/MOSIB/ IRQ7-DS/AN0	PE2/D10[A10/D10]/MTIOC4A/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7/AN018/ CVREFB0
77	PE1/D9[A9/D9]/MTIOC4C/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2/ RSPCKB/ANEX1	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/ SIOX12/SMOSI12/SSDA12/AN017/CMPB0
78	PE0/D8[A8/D8]/SCK12/SSLB1/ANEX0	PE0/D8[A8/D8]/SCK12/AN016
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN7	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN031
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN6	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN030
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN013	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN029
82	PD4/D4[A4/D4]/POE3#/IRQ4/AN012	PD4/D4[A4/D4]/POE3#/IRQ4/AN028
83	PD3/D3[A3/D3]/POE8#/IRQ3/AN011	PD3/D3[A3/D3]/POE8#/IRQ3/AN027
84	PD2/D2[A2/D2]/MTIOC4D/CRX0*1/ IRQ2/AN010	PD2/D2[A2/D2]/MTIOC4D/IRQ2/AN026
85	PD1/D1[A1/D1]/MTIOC4B/CTX0*1/ IRQ1/AN009	PD1/D1[A1/D1]/MTIOC4B/IRQ1/AN025
86	PD0/D0[A0/D0]/IRQ0/AN008	PD0/D0[A0/D0]/IRQ0/AN024
87	P47/IRQ15-DS/AN007	P47/AN007
88	P46/IRQ14-DS/AN006	P46/AN006
89	P45/IRQ13-DS/AN005	P45/AN005
90	P44/IRQ12-DS/AN004	P44/AN004
91	P43/IRQ11-DS/AN003	P43/AN003
92	P42/IRQ10-DS/AN002	P42/AN002
93	P41/IRQ9-DS/AN001	P41/AN001
94	VREFL0	VREFL0
95	P40/IRQ8-DS/AN000	P40/AN000
96	VREFH0	VREFH0
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/DA1

Note 1. Valid for products with a ROM capacity of 768 KB or more.
Note 2. When the external bus is enabled, P53 cannot be used as an I/O port because it also functions as the BCLK pin.
Note 3. The indication UB does not appear in the listing of pin functions for the RX630, but when selecting the operating mode the same settings are required as on the RX630.

4. Notes on Migration

4.1 Operating Voltage Range

4.1.1 Power Supply Voltage

The power supply voltage ranges of the RX630 Group and RX231 Group differ.

Table 4.1 shows a comparative listing of the power supply voltage ranges.

Table 4.1 Comparative Listing of Power Supply Voltage Ranges

Item	RX630	RX231
VCC	2.7 V to 3.6 V	1.8 V to 5.5 V*1 3.0 V to 3.6 V*2 4.0 V to 5.5 V*3
AVCC0	Same potential as VCC	1.8 V to 5.5 V*4
VREFH0	2.7 V to AVCC0	1.8 V to AVCC0
VREFH	Same potential as VCC	1.8 V to AVCC0
VCC_USB	Same potential as VCC	Same potential as VCC
VBATT	2.3 V to 3.6 V	1.8 V to 5.5 V

Note 1. When not using USB
Note 2. When using USB but not using a USB regulator
Note 3. When using USB and a USB regulator
Note 4. When VCC ≥ 2.0 V, AVCC0 and VCC may be set independently, within the usable range.
When VCC < 2.0 V, AVCC0 = VCC.
The power-on sequence for the VCC and AVCC0 pins should be either simultaneous power-on of both pins or VCC power-on followed by AVCC0 power-on.

4.1.2 Analog Power Supply Voltage

On the RX231 Group AVCC0 and VCC may be set independently, within the usable range, if VCC ≥ 2.0 V.

4.2 Notes on the Pin Design

4.2.1 Power Supply Pins and Operating Frequency

On the RX231 Group the upper limit of the operating frequency differs according to the voltage (VCC) input on the power supply pins. For details on power supply voltages and operating frequencies, refer to refer to the User's Manual: Hardware of the RX230 Group and RX231 Group, listed in 5, Reference Documents.

4.2.2 Main Clock Oscillator

When connecting an oscillator (ceramic resonator or crystal oscillator) to the EXTAL or XTAL pin on the RX231 Group, ensure that the oscillation frequency of the oscillator is within the range 1 MHz to 20 MHz (VCC ≥ 2.4 V) or 1 MHz to 8 MHz (VCC < 2.4 V).

In the crystal oscillator connection examples for the RX630 Group and RX231 Group, the capacitor and damping resistor reference values differ. For detailed information on connecting a crystal oscillator, refer to the User's Manual: Hardware of the RX230 Group and RX231 Group, listed in 5, Reference Documents.

The processing when the EXTAL or XTAL pin will not be used differs for the RX630 Group and RX231 Group. On the RX231 Group the P36/EXTAL should be set as general port P36 and the P37/XTAL pin as general port P37 when the main clock is not used. If these pins are not used as general ports, they should be processed in the same manner as port 3.

4.2.3 VCL Pin (External Capacity)

On the RX231 Group, connect a 4.7μF smoothing capacitor to the VCL pin for internal power supply stabilization.

4.2.4 Mode Setting Pins

After a reset the mode setting pins on the RX630 Group are the MD and PC7 pins, but on the RX231 Group they are the MD pin and the UB/PC7 pin.

When using the on-chip debugging emulator (E1/E20 emulator), connect the MD pin to the E1/E20 emulator and drive the PC7/UB pin low, or connect the MD pin and PC7/UB pin to the E1/E20 emulator.

4.2.5 General I/O Ports

The processing when port 0 and port 4 are unused pins differs on the RX630 Group and RX231 Group. If the port 0 and port 4 pins will not be used on the RX231 Group, set both pins as input (PORTn.PDR bit = 0) and then connect each pin to AVCC0 or AVSS0 via a resistor. Alternatively, set both pins as output (PORTn.PDR bit = 1) and leave them open.

4.2.6 Analog Input Pins for A/D Converter

On the RX231 Group, ensure that AVCC0 = VCC when performing A/D conversion on signals input on analog input pins AN016 to AN031.

4.2.7 Integrated Pull-Up and Pull Down Resistors for USB DP and DM Pins

The RX231 Group has integrated pull-up and pull down resistors for the DP and DM pins.

USB external connection circuit examples for the RX630 Group and RX231 Group are therefore different.

For detailed information on the USB external connection circuit, refer to the User's Manual: Hardware of the RX630 Group and RX231 Group, listed in 5, Reference Documents.

4.2.8 Inputting an External Clock

On the RX630 Group it is permissible to input on the XTAL pin a signal that is the antiphase of the external clock signal input on the EXTAL pin. On the RX231 Group, however, this is not allowed. Keep this in mind when designing your system.

When inputting an external clock to the RX231 Group, it is necessary to set the main clock oscillator switch bit (MOSEL) in the main clock oscillator forced oscillation control register (MOFCR) to 1.

4.3 Notes on the Function Settings

4.3.1 UB Code

User boot mode is not provided in the RX231 Group. UB code A and UB code B necessary for user boot mode are also not provided. In the RX231 Group, the user area/data area of the flash memory can be programmed and read with an arbitrary interface using start-up program protection instead of user boot mode. For details, refer to the User's Manual: Hardware of the RX630 Group and RX231 Group, listed in 5, Reference Documents.

4.3.2 Battery Backup Function

On the RX630 Group it was possible to utilize the battery backup function by enabling voltage monitor 0 reset (OFS1.LVDAS bit = 0), but on the RX231 Group it is necessary both to enable voltage monitor 0 reset (OFS1.LVDAS bit = 0) and to select 2.51 V as the voltage monitor 0 level in order to use this function.

4.3.3 12-Bit A/D Converter

The number of I/O registers used with the 12-bit A/D converter has increased on the RX231 Group. In addition, software that makes use of the eight channels on pins AN008 to AN015 on RX210 Group microcontrollers must be altered to use channels among the 16 channels on pins AN016 to AN031 on RX231 Group microcontrollers.

4.3.4 12-Bit D/A Converter

When using the D/A converter on the RX630 group, care must be taken to ensure that the 10-bit A/D converter does not enter the module stop state when the DAADSCR.DAADST bit is set to 1 (measure against interference between D/A and A/D conversion enabled).

When using the 12-bit D/A converter on the RX231 Group, ensure that the 12-bit A/D converter does not enter the module stop state when the DAADSCR.DAADST bit is set to 1 (measure against interference between D/A and A/D conversion enabled). Otherwise, not only A/D conversion but also D/A conversion could be halted.

4.3.5 Memory Wait Cycle

RX231 Group microcontrollers have a memory wait cycle setting register (MEMWAIT), but RX630 Group microcontrollers do not. To select a high-speed ICLK clock frequency above 32 MHz on the RX231 Group, set the MEMWAIT bit to 1 (wait states). For details, refer to the User's Manual: Hardware of the RX231 Group, which are listed in 5, Reference Documents.

4.3.6 Transferring Firmware Contents to FCU RAM

In order to use FCU commands on the RX630 Group it is necessary to store the contents of the FCU firmware in the FCU RAM. This processing is not needed on the RX231 Group.

4.3.7 Using Commands to Program Flash Memory

On the RX630 Group programming and erasing of the flash memory is accomplished by issuing commands to the FCU. On the RX231 Group, in contrast, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for programming and erasing the ROM and then issuing software commands.

Table 4.2 compares the specifications of FCU commands and software commands.

Table 4.2 Comparison of FCU Command and Software Command Specifications

Item	FCU Commands (RX630)	Software Commands (RX231)
Command issue area	Program/erase address (00E0 0000h to 00FF FFFFh)	—
Usable commands	• P/E Normal mode transition • Status read mode transition • Lock bit read mode transition • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming • Blank check	• Programming • Block erase • P/E suspend • P/E resume • Status register clear • Forced end • Configuration setting

4.3.8 Supplemental Information on RAM Self-Diagnostics

The RX231 Group provides a buffer to enable fast access between the RAM and CPU. When a write to RAM is followed by a read access to the same address, the data may be read not from the RAM but from the buffer in some cases. Such read and write operations present no problems in a buffered configuration, but programs that expect to actually read from the RAM the previously written data (for example, software that performs self-diagnostics on on-chip RAM) may not operate as expected (because the data is read from the buffer instead).

To ensure that data is actually read from the RAM, do the following.

When reading data from an address in RAM aligned with a 4-byte boundary*1 after a write to RAM completes, first perform a write to another address that is different from that address aligned with a 4-byte boundary that you wish to read, then start the read from the desired address in RAM.

Note 1. An address aligned with a 4-byte boundary refers to an address whose lowest two bits have a value of 00b to 11b.

5. Reference Documents

User's Manual: Hardware

RX230 Group, RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX630 Group User's Manual: Hardware Rev.1.60 (R01UH0040EJ0160)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Migration Design Guide between RX Families: Package Dimensions Difference (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 23, 2017	-	First edition issued
1.10	May. 8, 2019	Whole	Confirmed the contents of the description again (Addition of description mistake etc.)
		8	Add memory map comparison of address space
		13	Add area comparison of option setting memory
		24	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		34	Add comparison of exception handling
		46	Add comparative listing of functions assigned to each multiplexed pin
		61	Add comparison of pin function control register
		116	Add comparison of flash memory (E2 Data Flash)
		116	Add differences in package external form

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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