PowerSpan II™ Initialization Application Note

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1. Introduction

This application note is intended to be used for software and hardware initialization of single and dual port PowerSpan II designs. It details the major functions of PowerSpan and how to initialize them. The focus is to get a board design working quickly and efficiently.

1.1 Background

The reader should be familiar with the following documents: *PCI Local Bus Specification (Revision 2.2)* and the processor's user manual. If designing with an MPC8260, the reader may find the PowerSpan II MPC8260 Connection Application Note of particular interest. PowerSpan II can be configured many different ways and is not limited to the applications of this document.

2. Hardware Initialization

Knowledge of the system design is very important before the hardware initialization of PowerSpan II. The following key system design characteristics must be considered:

- What is the power up sequence?
- What is the PCI bus clock speed?
- Is the application a PCI host or adapter?
- Who is the arbiter on the PCI buses (PCI-1, PCI-2)?
- Who is the arbiter on the Processor Bus (or 60x bus)?
- Which PCI interface is primary (PCI-1 or PCI-2)?
- Is the primary PCI bus 32-bit or 64-bit?

2.1 Power-up Sequencing

Power-up sequencing is the order in which different devices on the board are supplied power. PowerSpan II requires three voltages for proper operation: Ground (VSS), I/O buffers supply (VDD IO = 3.3) and the core voltage (VDD CORE = 2.5V).

2.1.1 How to Sequence Power-up of PowerSpan II

It is expected that both VDD IO and VDD CORE will ramp up at approximately the same time (< 1ms). For Compact PCI HotSwap support please see section 3.4.

An input signal rising to 3.3V before VDD IO is available can cause latch up or fuse current to the I/O buffer

2.2 Bus Clock Speed

PowerSpan II has three input bus clocks for each port (P1_CLK, P2_CLK, and PB_CLK). Each clock must be present and clock speed must be selected prior to coming out of reset to lock PowerSpan II internal PLLs. PowerSpan II will stay in reset if the clocks are not present and will not come out of reset until locked. For more information on clock speed selection please see Chapter 11 of the
PowerSpan II User Manual.

Any signal with a P2_ prefix refers to the PCI-2 interface and only applies to Dual PCI PowerSpan II.

2.2.1 How to Set Bus Clock Speed

PowerSpan II must initialize the PCI-1 and PCI-2 bus clocks operational frequency, between 25MHz and 66MHz. For backwards compatibility Px_M66EN have been kept but have internal pull-ups. The processor bus can be initialized to operate either between 25MHz and 100MHz (see Table 1).

Table 1: Bus Clock Initialization

Signal Name	Value	Description
PB_FAST	0	Initializes the processor bus to operate >25MHz and <50MHz
	1	Initializes the processor bus to operate >50MHz and <100MHz
P1_M66EN	0	Initializes the PCI-1 bus to operate >25MHz and <33MHz
	1	Initializes the PCI-1 bus to operate >33MHz and <66MHz
P2_M66EN	0	Initializes the PCI-2 bus to operate >24MHz and <33MHz
	1	Initializes the PCI-2 bus to operate >33MHz and <66MHz

2.3 Reset Direction

PowerSpan II has four reset pins PO_RST_, PB_RST_, P1_RST_, and P2_RST_. Power-on reset (PO_RST_) is always an input to PowerSpan II and is asserted at system power-on. Based upon reset direction control pins, the remaining reset pins can be configured as either inputs or outputs depending on your application needs (host or adapter). For example, if PowerSpan II is used on an adapter card, PowerSpan II should be reset from the PCI side (P1_RST_ is configured as an input) and should propagate reset to both the secondary PCI side (P2_RST_ is configured as an output) and the 60x side (PB_RST_ is configured as an output). For more information on configuring reset pins see Chapter 11 in the *PowerSpan II User Manual* or for more information on host and adapter reset sequences see Chapter 17 *PowerSpan II User Manual*.

2.3.1 How To Set Reset Direction

If PowerSpan II is reset from the processor bus, PB_RST_ should be configured as an input, P1_RST_ and P2_RST_ should be configured as outputs. To configure the reset pins as an input or output pin, see Chapter 11 of the *PowerSpan II User Manual*.

2.4 Power-Up Options

After deassertion of PO_RST_ critical options need to be configured that are dependent on the system's design for PowerSpan II to be powered up in a known state. The options that must be configured include: bus arbitration, primary PCI select, PCI-1 bus width select, boot select, 7400 mode select, and PLL bypass select. These options are explained in more detail in the following subsections.

There are two modes of initialization for power-up options: multiplexed system pin mode, and 60x configuration slave mode. Configuration slave mode options will overwrite the multiplexed pin options. For more information on power up option modes see Chapter 11 of the *PowerSpan II User Manual*.

2.4.1 Bus Arbitration

Both the PCI and processor buses can support multiple bus masters. Bus arbitration must be used to ensure that two masters cannot drive the bus at the same time. PowerSpan II implements a fair arbitration scheme (round robin) for each port (PCI-1, PCI-2, and 60x buses). For more information on arbitration see Chapter 6 of the *PowerSpan II User Manual*.

PowerSpan II does not have to be the arbiter on any bus, so the power-up arbiter option must be initialized at reset.

2.4.2 Primary PCI Select

The primary PCI interface has programmable capabilities that the secondary PCI interface does not have. PowerSpan II can configure PCI-1 or PCI-2 as primary. The added capabilities include CompactPCI Hot Swap support, vital product data, and I2O shell interface. See the *PowerSpan II User Manual* for more information on these capabilities.

2.4.3 PCI-1 Bus Width Select

The PCI-1 bus can be configured to either be 32bit PCI, or 64bit PCI. PCI-2 is a 32 bit port only. See the *PCI Local Bus Specification* for more details on 32 and 64 bit PCI.

2.4.4 Boot Select

This parameter is essential for powering up PowerSpan II and for the boot controller to master the bus for initialization before enabling other interfaces to master a bus. When PowerSpan II is the arbiter, the flexibility of PowerSpan II increases for use in both adapter and host PCI systems. For the boot controller to have sole ownership of the bus, PowerSpan II implements a boot select power-up option. This option locks out all bus requests at the PowerSpan II arbiters until the boot controller enables them. For example in a host application, if the boot controller resides on the processor bus, the PowerSpan II arbiter locks out all other processor bus and PCI bus requests allowing the boot controller to initialize a memory controller or cache until the boot controller enables the ports.

2.4.5 7400 Mode

This power-up option is specifically for processors, like the MPC7400, that allow misaligned data transfers. When this power-up option is set, the processor bus supports misaligned data transfers from the MPC7400 (see section 3 of the *PowerSpan II User Manual*).

2.4.6 PLL Bypass Select

PowerSpan II has three PLLs (Phase Locked Loops) that provides for minimal clock tree insertion affects. All PLLs can be bypassed by enabling PLL bypass.

IDT does not guarantee timing targets with the PLLs disabled.

2.4.7 How to Configure Power Up Options

PowerSpan II critical power up options must be configured before PowerSpan II can operate. The options can be configured by either two modes: multiplexed system pin mode or by 60x configuration slave mode. The configuration modes are described in the following subsections.

2.4.7.1 How to Configure Power Up Options using Multiplexed System Pin Mode

Multiplexed system pin power up option configuration is the default mode for configuring PowerSpan II. When PowerSpan II is coming out of power-up reset the system pins are always sampled. For more information on multiplexed system pin mode see Chapter 11 of the *PowerSpan II User Manual*. The pins required to configure PowerSpan II must be pulled to the applicable logic level (see Table 2).

Table 2: Multiplexed System Pin Power Up options

Signal Name	Value	Description
PB_FAST	0	Processor bus arbiter disabled
	1	Processor bus arbiter enabled
P1_M66EN	0	PCI-1 arbiter disabled
	1	PCI-1 arbiter enabled
P2_M66EN	0	PCI-2 arbiter disabled
	1	PCI-2 arbiter enabled
INT[5]_	0	PCI-2 is primary PCI bus
	1	PCI-1 is primary PCI bus
INT[4]_	0	PCI-1 is 64 bit PCI with P1_REQ64_ enabled on reset
	1	PCI-1 is 32 bit PCI
INT[3]_	0	PCI boot
	1	Processor bus boot
INT[2]_	0	Enable 7400 mode
	1	Disable 7400 mode
INT[1]_	0	Enable PLL bypass mode
	1	Disable PLL bypass mode

2.4.7.2 How to Configure Power Up Options Using 60x Configuration Slave Mode

Multiplexed system pin power up options can be overwritten using 60x configuration slave mode. This mode is enabled by toggling PB_RSTCONF while HRESET_ is still asserted latching the configuration word by PowerSpan II. The 60x configuration master puts the PowerSpan II configuration word on the PB_D[0:7] pins (see Table 3).

Table 3: 60x Configuration Slave Power Up Options

Signal Name	Value	Description
PB_D[0]	0 1	Processor bus arbiter disabled processor bus arbiter enabled
PB_D[1]	0 1	PCI-1 arbiter disabled PCI-1 arbiter enabled
PB_D[2]	0 1	PCI-1 arbiter disabled PCI-1 arbiter enabled
PB_D[3]	0 1	PCI-1 is primary PCI bus PCI-2 is primary PCI bus
PB_D[4]	0 1	PCI-1 is 32-bit PCI with P1_REQ64_ enabled on reset PCI-1 is 64-bit PCI
PB_D[5]	0 1	Processor bus boot selected PCI boot selected
PB_D[6]	0 1	Disable 7400 mode Enable 7400 mode
PB_D[7]	0 1	Disable PLL bypass mode Enable PLL bypass mode

An external controller should toggle power up options during reset and manage loading of configuration words to processor bus devices. For more information on 60x configuration slave mode see Chapter 11 of the *PowerSpan II User Manual*.

3. Software Initialization

This section is a continuation of PowerSpan II hardware initialization. It is assumed that the correct hardware configuration has been chosen for the given design. Ensure the proper power options have been loaded for your application. The PowerSpan II contains 4kBytes of register space for initialization and configuration. For the complete PowerSpan II memory map see Chapter 15 of the *PowerSpan II User Manual*.

In order to initialize PowerSpan II, the *PCI Local Bus Specification*, *PowerSpan II User Manual*, and the system configuration must be understood. PowerSpan II can be configured in many ways depending on the system architecture and performance requirements. The large suite of features PowerSpan II offers can be controlled by accessing PowerSpan II register space from any of the PowerSpan II ports.

The following section describes enabling of only the major functions of PowerSpan II applications are not limited to the scope of this section. The *PowerSpan II and MPC8260 Connection Application Note* describes performance settings when used with an MPC8260.

The following system characteristics must be determined during system design:

- What is the processor bus memory map?
- What is the PCI-1, PCI-2 memory map?
- What are the power-up options?
- What is the interrupt scheme?

Using software, PowerSpan II can be initialized from a PCI host, processor bus master, or by EEPROM load. EEPROM interface and software initialization is discussed in Section 3.6.

3.1 Software Initialization of PCI and Processor Bus Ports

After hardware initialization the host PCI enumerator software scans all the PCI adapter cards to determine which devices are present and their configuration requirements. This is often done by the PCI BIOS in a PCI application or system host in a Compact PCI application.

3.1.1 How to initialize the PCI side

The following steps are a guideline to initialize the PowerSpan II PCI port(s). The registers are accessed using PCI configuration cycles. For more information on configuration cycles see the *PCI Local Bus Specification*.

1. The appropriate power-up options for initialization from the PCI side (the bus select must be PCI), or the processor bus must clear the Px_LOCKOUT bit in the Miscellaneous Control and Status Register.
2. After hardware initialization the PCI base address registers are not visible from the PCI side until the BSREG_BAR_EN is set in the PCI-n Miscellaneous Control and Status Register.
3. The MS bit must be set in the Px control and status register (P1_CSR, P2_CSR) to allow PowerSpan II to accept memory cycles as a PCI target.
4. The base address in the Px register image base address register (P1_BSREG, P2_BSREG) has to be initialized for the PowerSpan II to know what address range to decode for the PowerSpan II registers. For PCI, the bus enumerator must know the required size and load it from the EEPROM channel. For more information on the EEPROM interface please see Section 3.6.

3.1.2 How to initialize the Processor Bus

To configure the processor bus the following fields must be programmed:

- The processor bus register image base address register is 0x30000 by default. Depending on the address map, the base address field can be changed to conform to a given board address map.
- IDT recommends the ARTRY bit should be set in the processor bus miscellaneous control and status register (PB_MISC_CSR) to increase performance on the processor bus.

3.2 Initializing PCI Target Images

In order to communicate through PowerSpan II from the PCI side to the processor bus the PCI target image must be initialized with software. A PCI target image is an address range (in PCI address space) where PowerSpan II responds to the master's request. For more information on PowerSpan II PCI target interface see Chapter 3 of the *PowerSpan II User Manual*.

After decoding the address requested by the master, PowerSpan II becomes the target for that transaction. Once the target image is initialized either PCI bus can read from and write to both the processor bus and other PCI buses. For more information on PCI transactions see the *PCI Local Bus Specification*.

3.2.1 How to Initialize the PCI Target Image

The following registers must be initialized using PCI configuration write cycles. For more information on configuration cycles see Chapter 6 of the PCI Local Bus Specification.

Table 4: PCI Target Register Initialization

Register	Field	Description
Pn_BSTx	BA	Initialized so PowerSpan II knows what address range to decode for the target image.
Pn_TIx_CTL	BAR_EN	Enables the base address register and is visible to PCI BIOS
Pn_TIx_CTL	BS	Specifies the block size of the target image (see table 87 of the *PowerSpan II User Manual*)
Pn_TIx_CTL	DEST	Specifies the destination bus to be either PCI-n or processor bus
Pn_TIx_CTL	IMG_EN	Enables the target image. This bit should be set last.

Depending on application requirements, PowerSpan II registers can be initialized for more PowerSpan II register options (see Chapter 15 of the *PowerSpan II User Manual*.)

3.3 Initializing the Processor Bus Slave Image

In order to communicate through PowerSpan II from the processor bus to either PCI bus the processor bus slave image must be initialized with software. A processor bus slave image is an address range (in processor bus address space) where PowerSpan II responds to a master's request. For more information on PowerSpan II processor bus slave interface see Chapter 4 of the *PowerSpan II User Manual*.

After decoding the address requested by the master PowerSpan II becomes the slave of that transaction. Once the processor bus slave image is initialized the processor bus can read and write from either PCI bus.For more information on processor bus transactions see Chapter 4 of the *PowerSpan II User Manual*.

3.3.1 How to Initialize the Processor Bus Slave Image

Processor bus slave images must be initialized to accept transactions targeted for the processor bus. Table 5 shows which registers must be initialized.

Table 5: Processor Bus Slave Register Initialization

Register	Field	Description
PB_SIx_BADDR	BA	Initialized so PowerSpan II knows what address range to decode for the slave image.
PB_SIx_CTL	BS	Specifies the block size of the slave image (see table 87 for block size translations) NOTE: Must use memory cycles for register access
PB_SIx_CTL	DEST	Specifies the destination bus to be either PCI-1 or PCI-2 NOTE: Must use memory cycles for register access
PB_SIx_CTL	IMG_EN	Enables the slave image. Enable this bit last.
Px_CSR	BM	Enables PCI-n interface to initiate bus master transactions

3.4 Translation Addresses

PowerSpan II can support the automatic translation of addresses from any source port to any destination port. Before designing begins it is important to know the system memory map. The memory map should consist of each image base address and block size. In a given system there is finite memory space available, so it may be desirable to translate an address from one port to another. For example, if a device on the processor bus with base address of 0x4000_0000 requires a block size of 64k, but another device on PCI-1 may already have a portion of that address space the processor bus could map this address range to 0x5000_0000. PowerSpan II can translate PCI-1 accesses from 0x5000_wxyz to processor bus addresses 0x4000_wxyz.

3.4.1 How to Initialize Processor Bus Translation Address

Processor bus address translation must be enabled in the Processor Bus Slave Image x Control Register (PB_SIx_CTL), and the translation address must be set in the Processor Bus Slave Image x Translation Address Register (Pn_SIx_TADDR).

Table 6: Processor Bus Translation Register Settings

Register Name	Field	Field Description
PB_SIx_TADDR	TADDR	Replaces the processor bus address upper address bits
PB_SIx_CTL	TA_EN	Enables translation address. Enable this bit last.

3.4.2 How to initialize PCI translation address

PCI address translation must be enabled in the Px Target Image n Control Register (Px_TIn_CTL), and the translation address must be set in the Px Target Image n Translation Address Register (Px_TIn_TADDR).

Table 7: Px Translation Register Settings

Register Name	Field	Field Description
Pn_TIx_TADDR	TADDR	Replaces the Px upper address bits
Pn_TIx_CTL	TA_EN	Enables translation address

3.5 Interrupts

PowerSpan II has support for a number of transaction exceptions and various interrupt schemes. The general purpose interrupts are for DMA transactions, doorbells, and mailboxes. The transaction exceptions are primarily due to errors in transmission on any port. For a complete list of exceptions see Chapter 9 of the *PowerSpan II User Manual*.

Interrupt schemes are configured by mapping the proper interrupt to the proper pin, PowerSpan II has 8 interrupt pins: P1_INTA_, P2_INTA_, and INT[5:0]_. The status of a given interrupt can be ascertained by reading the interrupt status registers. An ISR reading from and, subsequent writing to, the appropriate interrupt status register clears pending interrupts.

3.5.1 How to Set Interrupts

The interrupt enable registers allow the interrupt sources to be active or masked. To enable an interrupt source the corresponding enable bit must be enabled, see Chapter 15 of the *PowerSpan II User Manual* for Interrupt Enable Registers (IER). Each enabled interrupt source must be mapped to an interrupt pin, which is set in the Interrupt Map Registers (IMR), see Chapter 15 of the *PowerSpan II User Manual*. At this point the interrupts are enabled and signal an interrupt on the appropriate interrupt pins through interrupt mapping.

3.6 EEPROM Interface

Loading various registers directly through an EEPROM on the I^2C port can also initialize PowerSpan II ports and images. Using EEPROM loading enables PowerSpan II to boot without a processor on the processor bus, and allows for VPD support. There are two types of EEPROM load sequences, a short and a long load. A short load allows software configuration of the PCI bus and PCI target images. A long load extends the configuration to include the processor bus, processor bus slave images, and VPD.

3.6.1 How to Initialize PowerSpan II with the EEPROM interface

By default, PowerSpan II polls for an EEPROM on its I2C bus at boot time by issuing a read from the I2C master interface. If an EEPROM is present, it will reply to the read and PowerSpan II loads register settings from the EEPROM after deassertion of P1_RST_. The first byte read from the EEPROM dictates which load is to be used (short or long). For more information on the EEPROM load sequence see Chapter 8 of the *PowerSpan II User Manual*.

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