Application Note

PV88080 Voltage Rail Sequencing

AN-PV-005

Abstract

The application note describes control of the power rail sequencing of the PV88080 PMIC.

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1 Terms and Definitions

BOM	Bill of materials
GPIO	General purpose input/output
GPO	General purpose output
GUI	Graphical user interface
OTP	One time programable
PMIC	Power management integrated circuit
STBY	Standby

2 References

None

3 Introduction

PV88080 is a 4-channel PMIC with integrated advanced power sequencing to control the power-up and power-down sequence of its buck converters. The on-board OTP stores the sequencing, but the sequencing can also be controlled by an I²C command issued in either the GUI or host processor. In applications requiring multiple PV88080s, GPIO and STBY pins can be used to control cascaded devices.

4 Sequencing

In the PV88080 digital system, there are 15 time slots for sequencing. The system sequences through the time slots from 1 to 15 during power-on, and from 15 to 1 during power-down. The available bucks should be assigned to slots between 1 and 15. The power-on sequence, once defined, can use the SYSTEM_END parameter to separate the standby and active mode operations. When STBY is pulled high, the system runs through the sequence before the SYSTEM_END slot, and ends in standby mode. When STBY is pulled low, all of the slots run in sequence, and ends in active mode, see Figure 1.

Note
If the STBY pin is not used in your application, then SYSTEM_END is not available.

A SLOT0 assignment means that function will not follow the power-on or power-off sequence. The buck that is assigned to SLOT0 will not be enabled in the power-on sequence. It can be enabled using the I²C.

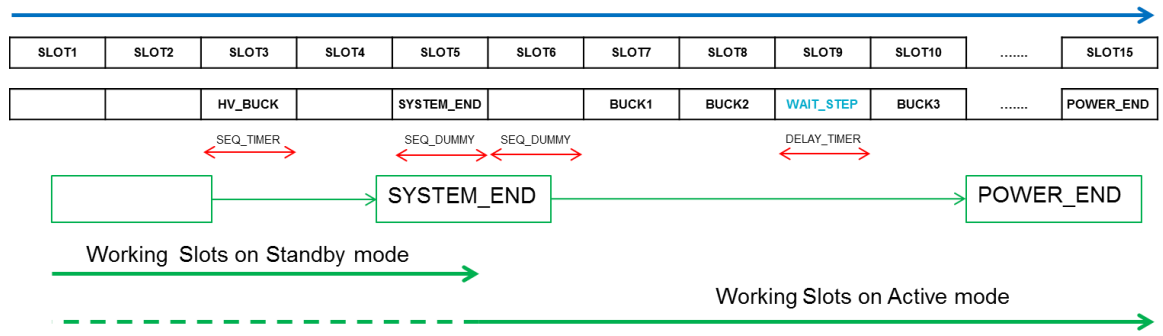

Figure 1: Sequencing Slots Model

There are two types of time slots, a normal slot which is put in the sequence, like HV_BUCK or LV BUCK1, and empty slots called dummy slots. The dummy slot duration is set in the SEQ_DUMMY register bits. For example, SLOT1, SLOT2, SLOT4, and SLOT6 in Figure 1 are empty and are therefore dummy slots. The SYSTEM_END slot will use the dummy slot duration rather than a normal slot duration. The normal and dummy slot durations can be programed in register 0x29.

4.1 General Power Sequencing Setting

For General purpose sequencing, every buck converter should be assigned to a slot. Figure 2 shows an example of power sequencing in the order it is assigned to follow: HVBUCK [3], Buck1 [7], Buck2 [8], and Buck3 [10]. Every power rail can have its own slot number; two different power rails can be set to the same slot if they need to be turned on together. Set the SEQ_TIME and SET_DUMMY to adjust the slot duration to control the delay time between the two different slots.

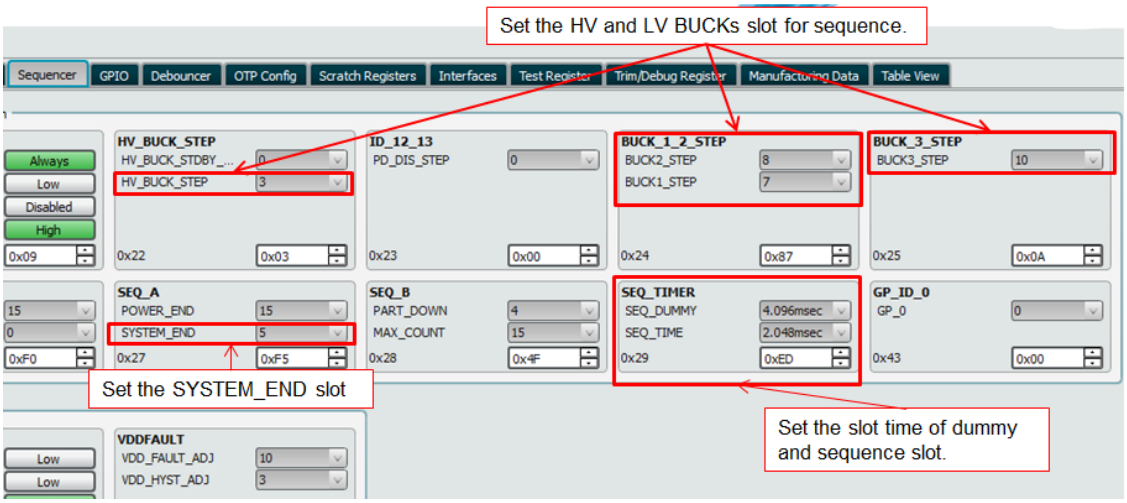

Figure 2: Sequencing and GUI

For example, assume that the system requires that Buck1 turns on 2 ms before Buck2, and that Buck3 turns on 6 ms after Buck2.

- Set SEQ_TIME = 2.048 ms
- Buck1 is set to one slot before Buck2
- Buck2 is in SLOT8
- Buck3 is in SLOT10
- SLOT9 is empty

The delay time between Buck2 and Buck3 equals the normal sequence time plus the dummy sequence time, so the result is 6.114 ms. Therefore, the SET_DUMMY = 4.096 ms. The resulting sequence is shown in Figure 3.

The slots and slot times are configurable to meet different system requirements.

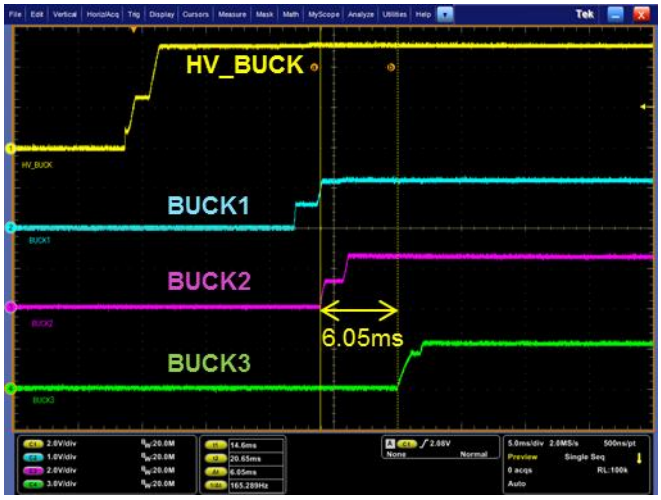

Figure 3: Sequencing Waveform

4.2 Specific Delay Time between Power Sequences

In some circumstances, a system may need a longer sequence than is supported by 15 slots and dummy slots. In this situation, the PV88080 WAIT_ID function can be used to insert a time slot and to add a delay time.

ID_0 (0x21[8]) sets the WAIT_ID slot. It can be programed to work for power-up and power-down sequences, or, alternatively, for the first power-on sequence.

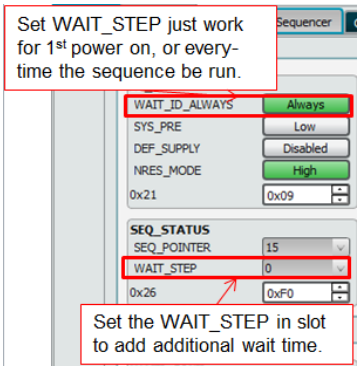

Figure 4: WAIT_ID Behavior and Slot Setting

WAIT_STEP can insert a delay time in the slot; set in DELAY_TIME 0x39[0] with a range from 549 µs to 8.4 s. To illustrate the WAIT_ID function, consider a system that needs a 34 ms delay between Buck2 and Buck3 and keeps the original sequence time between HV_BUCK, Buck1, and Buck2, see Figure 3.

The DELAY_TIME is set to 32.8 ms and the WAIT_ID to SLOT9. The delay time between Buck2 and Buck3 increases to 34.848 ms (Typ). Figure 4 shows the result with the additional delay time in SLOT9 between Buck2 and Buck3.

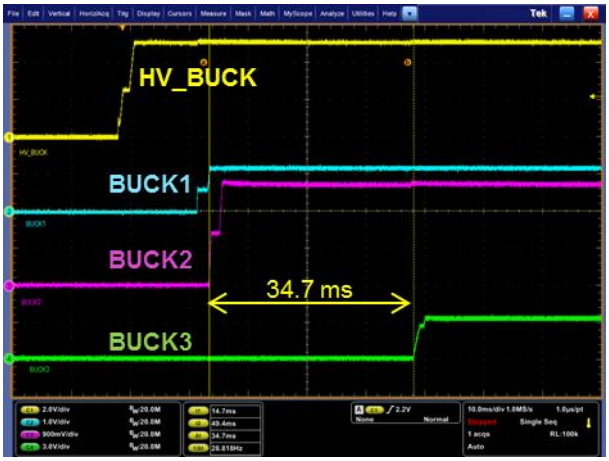

Figure 5: Sequencing with Additional WAIT_STEP Slot

Depending on the system requirements, the WAIT_ID slot can be set to work for the first power-up, or every time the sequence is initiated.

When WAIT_ID_ALWAYS is set to first use, the WAIT_ID delay time only runs once after the first power-on sequence.

When WAIT_ID_ALWAYS is set to always, the WAIT_ID delay time runs every time the system runs the sequence.

4.3 STBY Pin and Enable Function

PV88080 uses the STBY pin to further increase the versatility of the sequencing engine.

The SYSTEM_END slot is controlled by the STBY pin. It provides a standby mode to disable some power rails and suspend function between sequences. If STBY = 0, the power sequence runs to the end of the sequence. If STBY = 1, the power-down sequence runs until standby mode is reached. Essentially, all of the slots after SYSTEM_END are turned off. This allows the bucks to cycle down whenever the STBY pin is asserted.

For example, in Figure 1, the SYSTEM_END is in SLOT5, Bucks 1 to 3 are controlled by STBY pin. The delay time between STBY and Buck1 can be set by a slot time as well.

SYSTEM_END can also be used for systems that need some always-on power rails and others that are disabled in standby. For this arrangement, the always-on power rails are set to the slots before SYSTEM_END, and the others are set to the slots after the SYSTEM_END slot.

For example, if the HV_BUCK is in SLOT3 and SYSTEM_END is in SLOT5, the HV_BUCK will remain on when STBY is asserted; the other power rails will shut down.

If SEQ_TIME = 2.048 ms and SET_DUMMY = 4.096 ms, if the STBY pin is pulled high and then the device is powered, the sequence will remain at the end of SYSTEM_END. After HV_BUCK is ready, pulling STBY low, Buck1 will follow its start-up sequence as in Figure 6. There is a dummy slot delay to Buck1between STBY and Buck1 of approximately 4 ms.

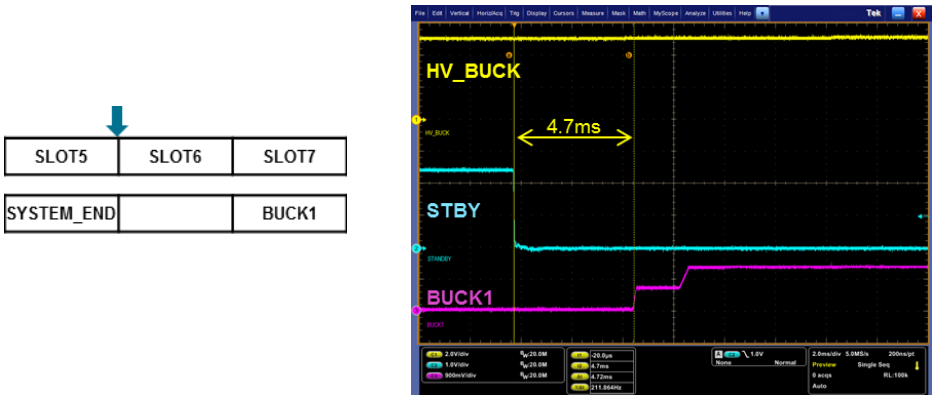

Figure 6: STBY Sequencing Control in Power-Down Mode

If STBY is pulled high after the entire power sequence has already run, the sequence will move back to the start of SLOT5, meaning, the system moves back to standby from active mode. Therefore, if the system is pulled low again, the delay is equal to
SLOT5 + SLOT6: 4.096 ms + 4.096 ms = 8.192 ms, see Figure 6.

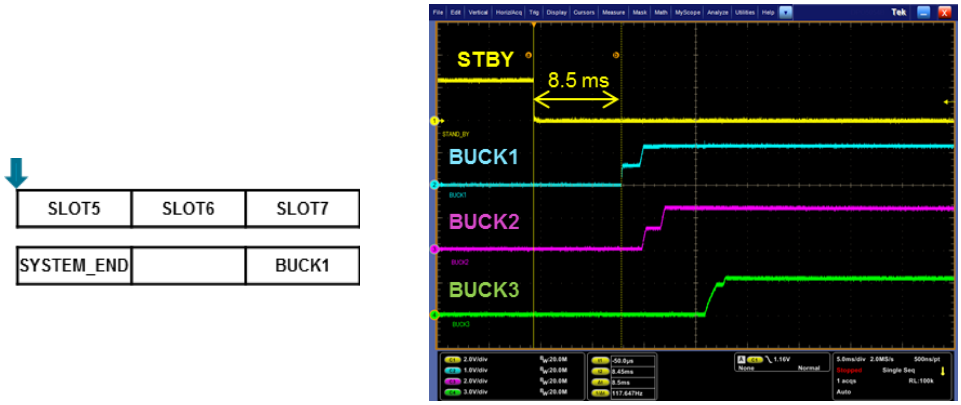

Figure 7: STBY Sequencing Control

4.4 GPIO and Multiple PV88080 Control

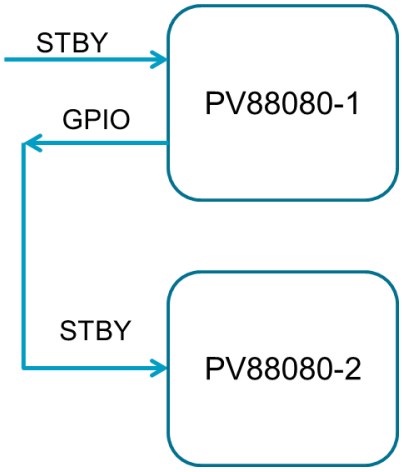

Figure 8: Multiple PV88080 Connection

For systems that need more than four power rails, the sequence of multiple PV88080 devices can be controlled using the GPIO and STBY functions.

PV88080-1 acts as the master and the others act as slaves. One GPIO pin is configured as the power sequence control GPO in PV88080-1 and connected to the other PV88080 STBY pin.

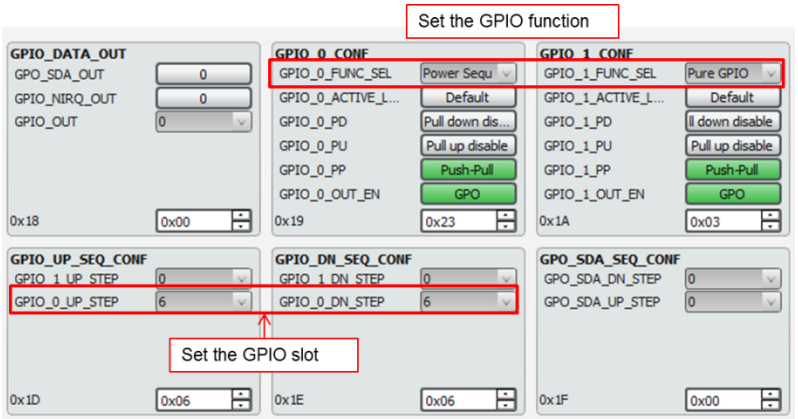

Figure 9: GPIO Function Selection

In Figure 8, assuming the STBY signal is low (not active) at power-on reset, the sequencer will run through all 16 slots and turn on all bucks. The sequencer is then held at the POWER_END slot. If the STBY signal is asserted high, then the sequencer turns on and loops back to the SYSTEM_END slot and begins to move through the remaining slots, turning off any bucks that are in the path. Once this occurs, the sequencing will go back to the SYSTEM_END slot and wait for STBY to go inactive. Once this happens then the sequencer begins to move through the slots and turns on all bucks in the path.

If the STBY signal is asserted at power-up then the 16 slot sequence is run through up to the slot where SYSTEM_END is assigned. Any bucks before SYSTEM_END will be turned on. Any buck assigned to slots after SYSTEM_END will not turn on until the STBY signal is deasserted. Once this happens then the sequencer will run through the remaining slots and turn on any bucks assigned to slots after SYSTEM_END. The sequencer will then loop back to the SYSTEM_END slot and wait until STBY is reasserted. Thus, all bucks are on at this point. It should be noted that if in a slave arrangement, as shown above, the GPIO of the master controls the STBY pin of the slave. Thus, in order for the master to have control of the buck sequence in the slave, the bucks in the slave need to be assigned to slots after SYSTEM_END in the slave sequencer. This is because any buck that is assigned a slot before SYSTEM_END in the slave will come on at power-on reset independent of the state of the STBY pin. Additionally, by design the sequencer, in both the master and the slave, will

not run until internal initialization (OTP load) is complete. This allows the state of the GPIO/STBY pins to be established before the sequencer begins to run.

5 Conclusion

PV88080 provides flexible sequencing control with OTP and I^2C setup and commands. This reduces the BOM, die area, and host GPIOs, therefore, improving reliability with reduced component count.

Revision History

Revision	Date	Description
1.0	<23-Jul-2017>	Initial version.

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