R8C/38C Group

Timer RD (PWM3 Mode)

R01AN0083EJ0100
Rev.1.00
Sep. 27, 2010

1. Abstract

This document describes a setting method and an application example for timer RD in PWM3 mode in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/38C Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Two PWM waveforms with 200 μs periods are output. The PWM period is generated at a compare match of timer RD counter 0 (TRD0) and general register A0 (TRDGRA0). PWM change points are generated at the compare match of the TRD0 register and general registers TRDGRA1, TRDGRB0, and TRDGRB1. An interrupt is generated at the compare match of registers TRD0 and TRDGRA0. Output signals are as follows:

TRDIOA0 pin: Active high level 60 μs = 1/20 MHz × (TRDGRA0 – TRDGRA1)
= 50 ns × (3999 – 2799) = 50 ns × 1200
TRDIOB0 pin: Active high level 60 μs = 1/20 MHz × (TRDGRB0 – TRDGRB1)
= 50 ns × (1999 – 799) = 50 ns × 1200

The 200 μs PWM period is set to the TRDGRA0 register.
200 μs = 1/20 MHz × (TRDGRA0 + 1) = 50 ns × 4000

PWM output change of TRDIOA0 pin (Set the active level timing in the TRDGRA1 register.)
140 μs = 1/20 MHz × (TRDGRA1 + 1) = 50 ns × 2800
PWM output change of TRDIOB0 pin (Set the timing that returns to initial output level in the TRDGRB0 register.)
100 μs = 1/20 MHz × (TRDGRB0 + 1) = 50 ns × 2000
PWM output change of TRDIOB0 pin (Set the active level timing in the TRDGRB1 register.)
40 μs = 1/20 MHz × (TRDGRB1 + 1) = 50 ns × 800

Settings

- Use f1 (XIN clock: 20 MHz) as the count source.
- Clear the TRD0 register at the compare match with the TRDGRA0 register.
- Select TRDGRA0 and TRDGRB0 pin output levels as active high and the initial output level as inactive low.
- Output an active high level from the TRDIOA0 output pin at the compare match of registers TRD0 and TRDGRA1.
- Output an active high level from the TRDIOB0 output pin at the compare match of registers TRD0 and TRDGRB1.
- Do not use buffer operations (BFC0, BFD0, BFC1, and BFD1).
- Do not use the pulse output forced cutoff input function.
- Do not use A/D triggers.
- Use the timer RD0 interrupt.

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Timing Diagram. Table 3.1 lists the pins used and their functions.

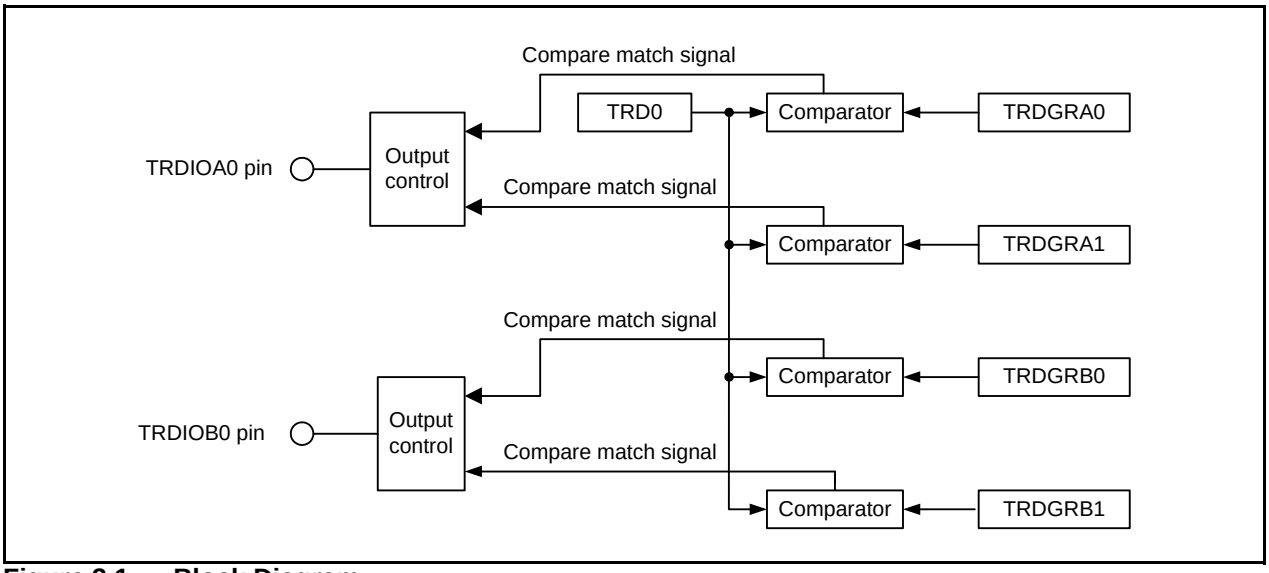


Figure 3.1 Block Diagram

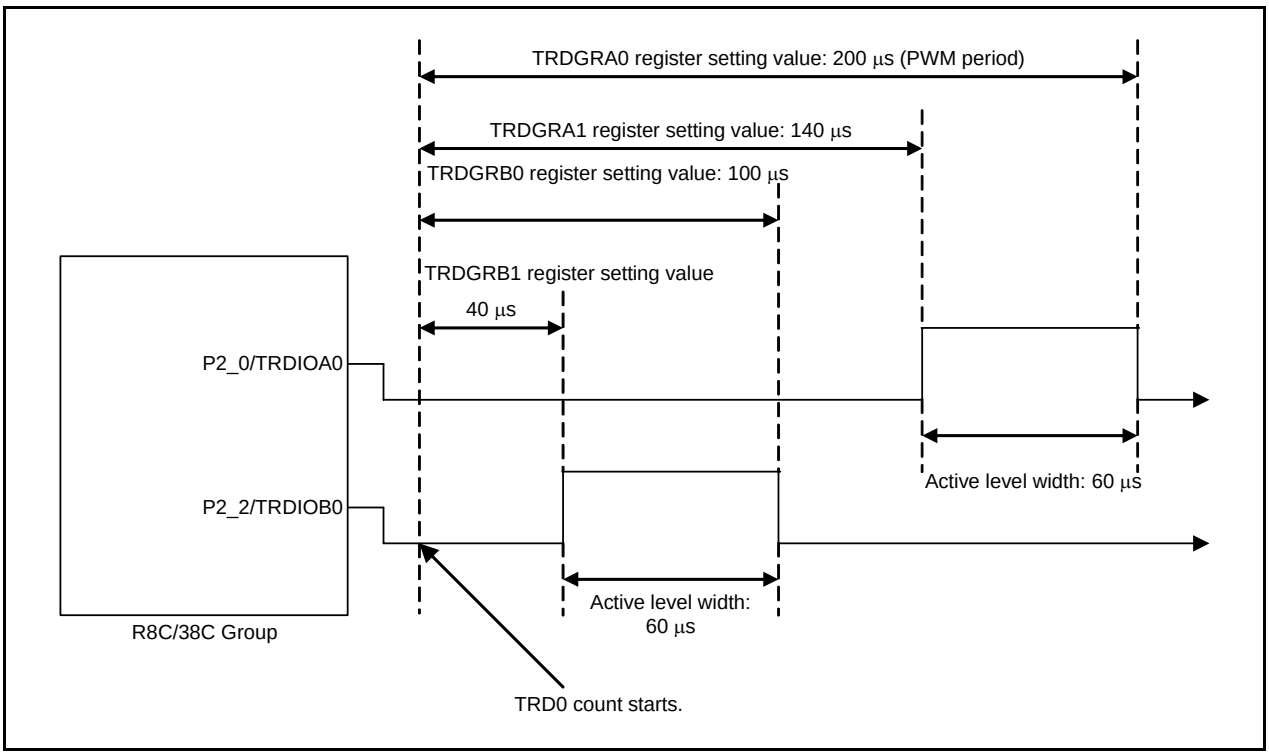


Figure 3.2 Timing Diagram

Table 3.1 Pins and Their Functions

Pin Name	I/O	Function
P2_0/TRDIOA0	Output	PWM output
P2_2/TRDIOB0	Output	PWM output

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	192 bytes	In the r01an0083_src.c module
RAM	0 bytes	In the r01an0083_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

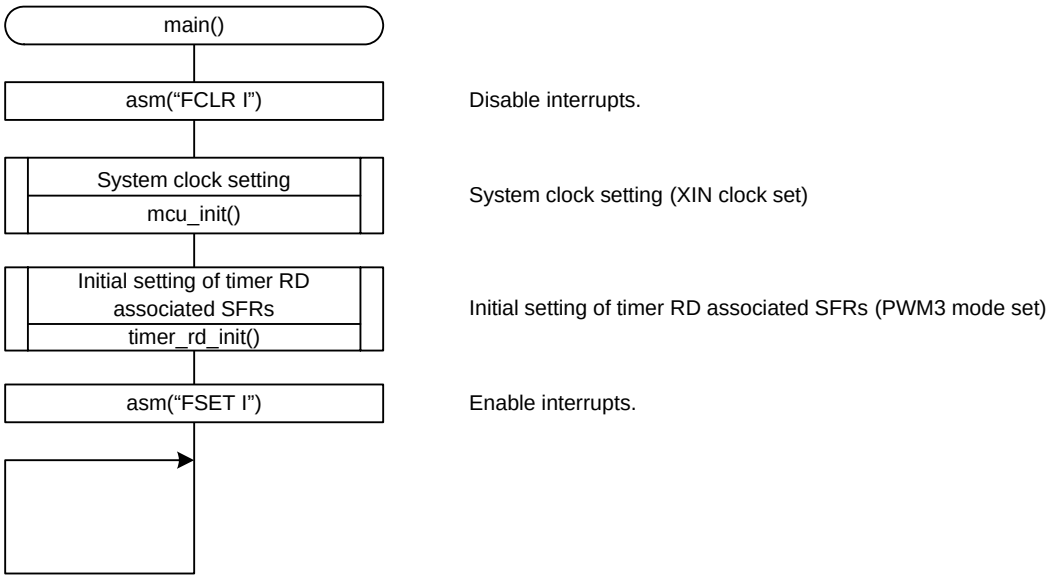
Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void timer_rd_init(void)		
Outline	Initial setting of timer RD associated SFRs		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize timer RD associated SFRs to use timer RD in PWM3 mode.		

Declaration	void _timer_rd_ch0(void)		
Outline	Timer RD0 interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform timer RD0 interrupt handling.		

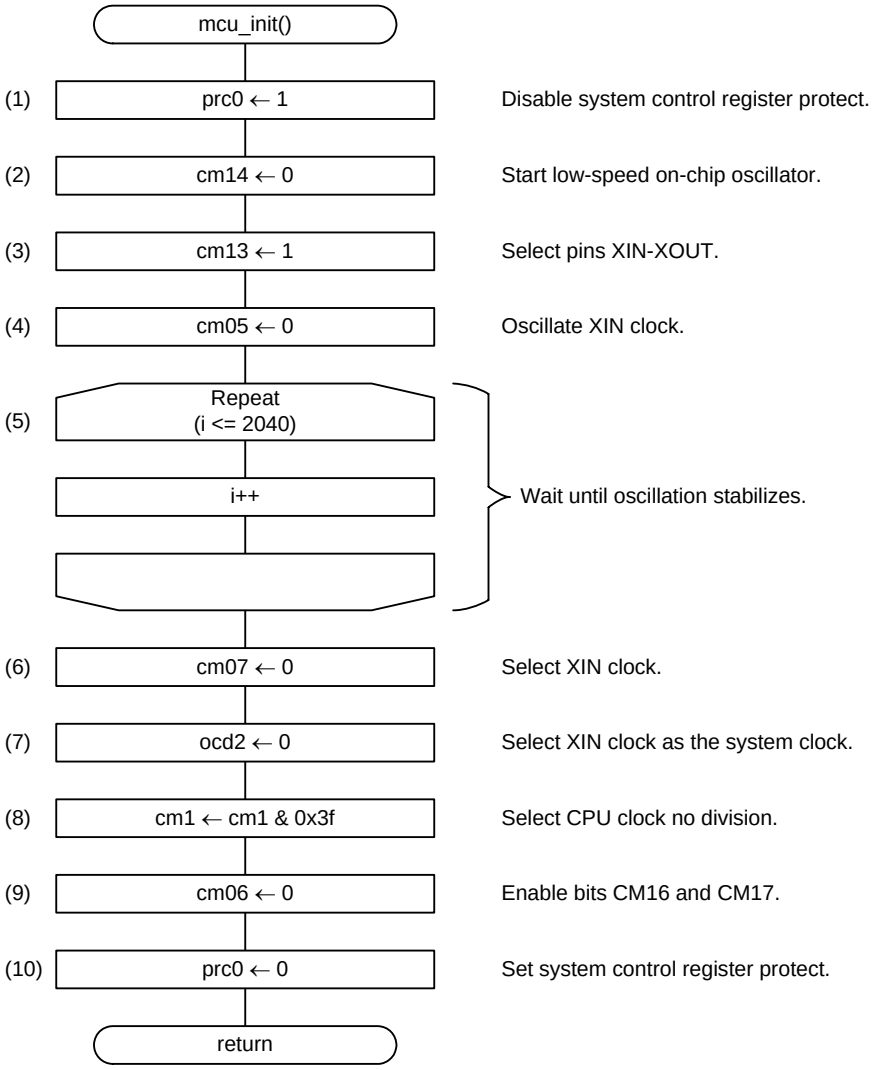
4.2 Main Function

• Flowchart



4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0		x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set system clock control register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—		1	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	CM13	Port/XIN-XOUT switch bit	1: XIN-XOUT pin	R/W

(4) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			0	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	0: XIN clock oscillates	R/W

(5) Wait until oscillation stabilizes.

(6) Select the XIN clock.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0			x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	CM07	XIN, XCIN clock select bit	0: XIN clock	R/W

(7) Select the XIN clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	0	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	0: XIN clock selected	R/W

(8) Set system clock register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—			x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0		x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

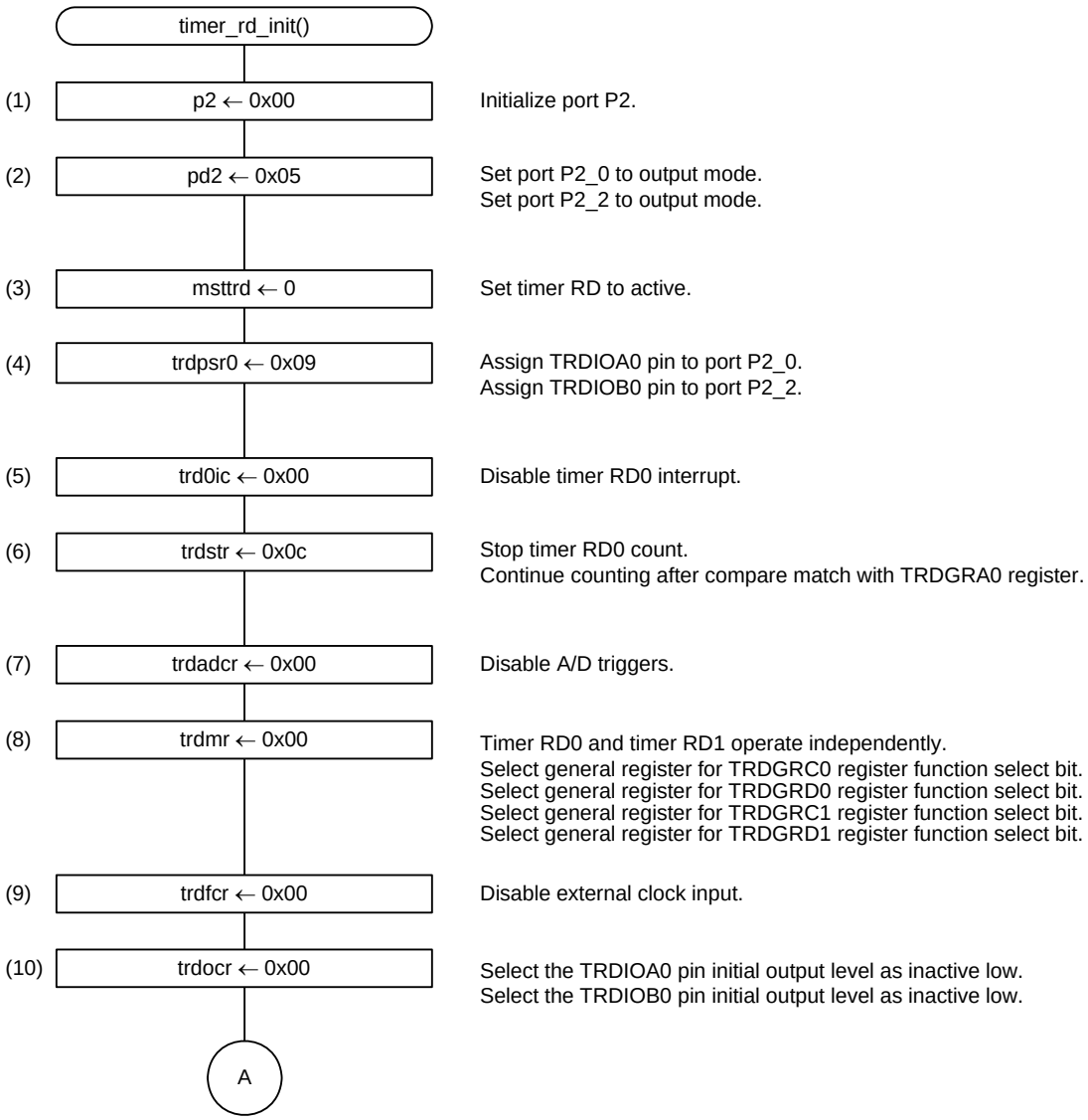
Protect Register (PRCR)

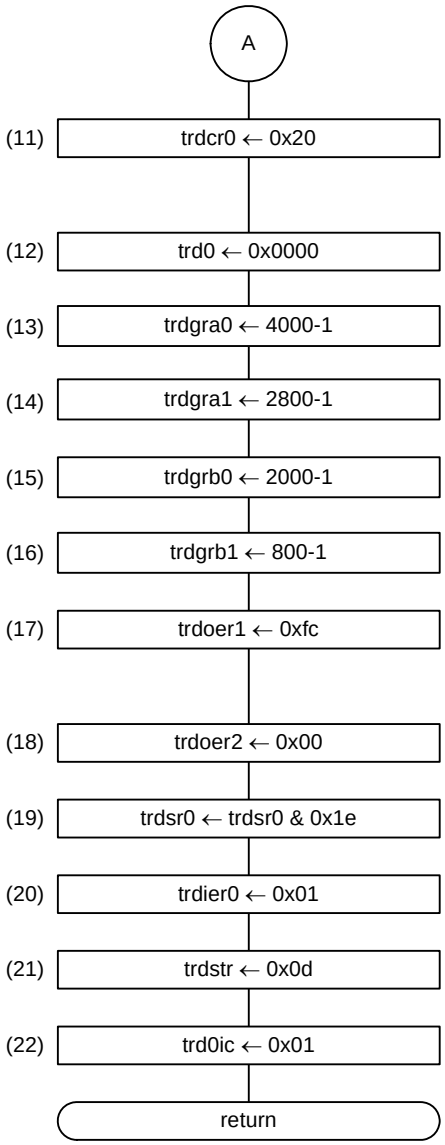
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Initial Setting of Timer RD Associated SFRs

• Flowchart





Select f1 as count source.
Clear TRD0 register at compare match with TRDGRA0 register.

Initialize TRD0 register count value to 0000h.

Set 200 μs for PWM period (50 ns × 4000 = 200 μs)

Set 140 μs (50 ns × 2800 = 140 μs) for PWM output change point (timing that TRDIOA0 pin becomes active level).

Set 100 μs (50 ns × 2000 = 100 μs) for PWM output change point (timing that TRDIOB0 pin returns to initial output level).

Set 40 μs (50 ns × 800 = 40 μs) for PWM output change point (timing that TRDIOB0 pins becomes active level).

Enable TRDIOA0 output.
Enable TRDIOB0 output.

Disable pulse output forced cutoff input.

Clear input capture/compare match flag A.

Set IMFA bit to enable IMIA interrupt.

Start timer RD0 count.

Enable timer RD0 interrupt (level 1).

• Register settings

(1) Initialize port P2.

Port P2 Register (P2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	0	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	P2_0	Port P2_0 bit	0: “L” level	R/W
b2	P2_2	Port P2_2 bit		R/W

(2) Set ports P2_0 and P2_2 to output mode.

Port P2 Direction Register (PD2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	1	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PD2_0	Port P2_0 direction bit	1: Output mode (functions as an output port)	R/W
b2	PD2_2	Port P2_2 direction bit		R/W

(3) Set timer RD to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	0	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b4	MSTTRD	Timer RD standby bit	0: Active	R/W

(4) Set timer RD pin select register 0.

Timer RD Pin Select Register 0 (TRDPSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	x	1	0	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	1: P2_0 assigned	R/W
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	b3 b2 1 0: P2_2 assigned	R/W
b3	TRDIOB0SEL1			R/W

(5) Disable the timer RD0 interrupt.

Interrupt Control Register (TRD0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(6) Stop the timer RD0 count and set the timer RD0 count operation.

Timer RD Start Register (TRDSTR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	0: Count stops	R/W
b2	CSEL0	TRD0 count operation select bit	1: Count continues after the compare match with the TRDGRA0 register	R/W

(7) Disable A/D triggers.

Timer RD Trigger Control Register (TRDADCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	0	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled	R/W

(8) Set the timer RD mode register.

Timer RD Mode Register (TRDMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	0	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Registers TRD0 and TRD1 operate independently	R/W
b4	BFC0	TRDGRC0 register function select bit	0: General register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register	R/W

(9) Set the timer RD function control register.

Timer RD Function Control Register (TRDFCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	R/W
b1	CMD1			R/W
b6	STCLK	External clock input select bit	Set this bit to 0 (external clock input disabled) in PWM3 mode.	R/W
b7	PWM3	PWM3 mode select bit	Set this bit to 0 (PWM3 mode) in PWM3 mode.	R/W

(10) Set the timer RD output control register.

Timer RD Output Control Register (TRDOCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	0: Active level “H”, initial output “L”, “H” output at compare match with the TRDGRA1 register, “L” output at compare match with the TRDGRA0 register	R/W
b1	TOB0	TRDIOB0 output level select bit	0: Active level “H”, initial output “L”, “H” output at compare match with the TRDGRB1 register, “L” output at compare match with the TRDGRB0 register	R/W

(11) Set timer RD control register 0.

Timer RD Control Register 0 (TRDCR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	x	x	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 001b (the TRD0 register cleared at compare match with TRDGRA0 register) in PWM3 mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

(12) Initialize timer RD counter 0 to 0000h.

Timer RD Counter 0 (TRD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15-b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

(13) Set compare value 4000 - 1 (F9Fh) of timer RD counter 0 to timer RD general register A0.

Timer RD General Register A0 (TRDGRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	1	1	1

Bit	Function	R/W
b15-b0	General register. Set the PWM period. Setting range: Value set in TRDGRA1 register or above	R/W

(14) Set compare value 2800 - 1 (AEFh) of timer RD counter 0 to timer RD general register A1.

Timer RD General Register A1 (TRDGRA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	0	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	0	1	0

Bit	Function	R/W
b15-b0	General register. Set the changing point (the active level timing) of PWM output. Setting range: Value set in TRDGRA0 register or below	R/W

(15) Set compare value 2000 - 1 (7CFh) of timer RD counter 0 to timer RD general register B0.

Timer RD General Register B0 (TRDGRB0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	0	0	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	1	1	1

Bit	Function	R/W
b15-b0	General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: Value set in TRDGRB1 register or above, Value set in TRDGRA0 register or below	R/W

(16) Set compare value 800 - 1 (31Fh) of timer RD counter 0 to timer RD general register B1.

Timer RD General Register B1 (TRDGRB1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	1	1

Bit	Function	R/W
b15-b0	General register. Set the changing point (active level timing) of PWM output. Setting range: Value set in TRDGRB0 register or below	R/W

(17) Set timer RD output master enable register 1.

Timer RD Output Master Enable Register 1 (TRDOER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	0: Enable output	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output	R/W
b2	EC0	TRDIOC0 output disable bit	Set these bits to 1 (programmable I/O port) in PWM3 mode.	R/W
b3	ED0	TRDIOD0 output disable bit		R/W
b4	EA1	TRDIOA1 output disable bit		R/W
b5	EB1	TRDIOB1 output disable bit		R/W
b6	EC1	TRDIOC1 output disable bit		R/W
b7	ED1	TRDIOD1 output disable bit		R/W

(18) Set to pulse output forced cutoff input disabled.

Timer RD Output Master Enable Register 2 (TRDOER2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled	R/W

(19) Initialize input capture/compare match flag A.

Timer RD Status Register 0 (TRDSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

(20) Set the IMFA bit to enable the IMIA interrupt.

Timer RD Interrupt Enable Register 0 (TRDIER0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	1: Enable interrupt (IMIA) by the IMFA bit	R/W

(21) Start the timer RD0 count.

Timer RD Start Register (TRDSTR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x		x	1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	1: Count starts	R/W

(22) Enable the timer RD0 interrupt (level 1).

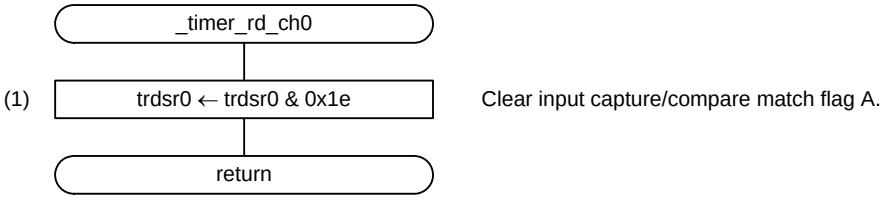
Interrupt Control Register (TRD0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

4.5 Timer RD0 Interrupt Handling

• Flowchart



• Register setting

(1) Initialize input capture/compare match flag A.

Timer RD Status Register 0 (TRDSR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read.	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/38C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/38C Group Timer RD (PWM3 Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 27, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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