RH850 Series

R01AN6027EJ0100
Rev.1.0

CAN Configuration（CAN FD Mode）

Summary

This document describes an example of a procedure for setting CAN Configuration using the RH850 series. Please refer to the notes in the latest user's manual hardware edition for the settings of each register.

Operation Confirmed Devices

This document applies to the RH850 series.

The variables described in the text are as follows.

Table 1-1　Target Devices and Variables

	Variable	Target MCU		
		RH850/E2x	RH850/E1M-S2	RH850/P1M-E
RS-CAN FD channel number	m	0~4	0~3	0~2
GAFLIDj, GAFLMj, GAFLP0j, GAFLP1j Register numbers	j	0~15	0~15	0~15
Transmit/Receive FIFO buffer number	k	0~14	0~11	0~8
Receive FIFO buffer number	x	0~7	0~7	0~7
Receive buffer number	q	0~79	0~63	0~47
Transmit buffer number	p	0~79	0~63	0~47
RAM test number	r	0~63	0~63	0~63
GAFLCFGi、GTINTSTSi register number	i	0	0	0
Number of each status register	y	0~2	0,1	0,1

The functions marked with "★" in the text are applicable to cases where 2 or more channels are installed.

In the text, CFD is omitted from the register names.

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1. CAN Configuration

In CAN configuration, set the functions required for CAN communication. Perform the configuration when resets MC, detects BUS failures, starts and restarts CAN communication after WAKEUP.

The stats available when performing CAN configuration are shown below. For CAN State (Mode), refer to “Section 2, CAN State (Mode) Transition”.

- After CAN module enable (the CAN0EN bit in the PER2 register is "1")
- Global reset mode
- Channel reset mode
- Channel halt mode

The required functions when setting CAN configuration are shown below. For details of each process, refer to the following chapters.

- CAN state (mode) transition
- Communication speed
- Global function
- Receive rule table
- Buffer
- Global error interrupt
- Channel function

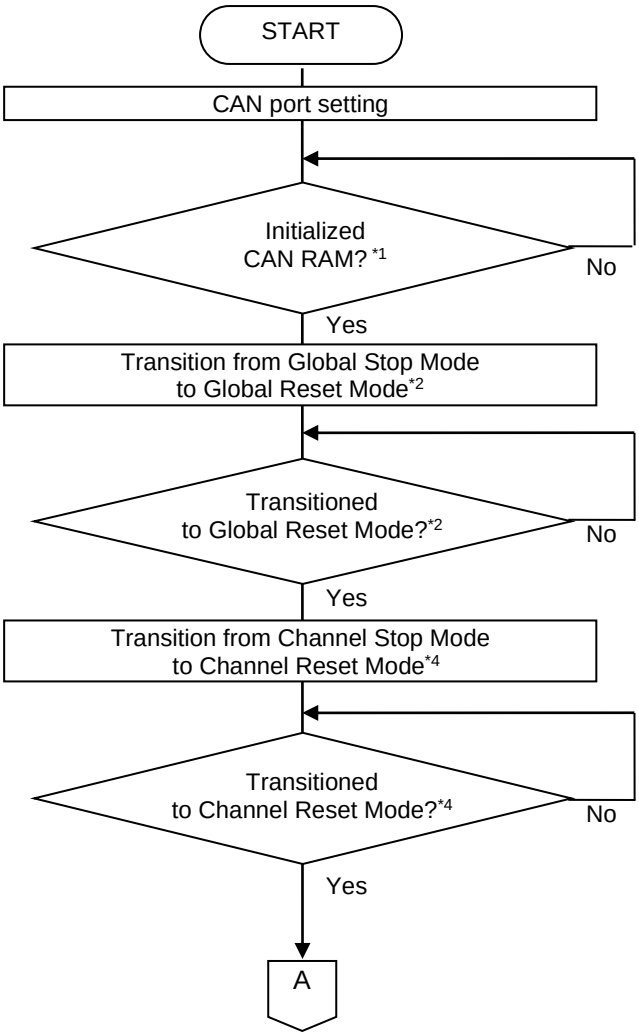
1.1 CAN Configuration after CAN Module Enable

1.1.1 CAN Configuration after CAN Module Enable

Perform the initialization of entire RS-CANFD modules after resetting MCU.

1.1.2 Setting Procedures of CAN Configuration after CAN Module Enable

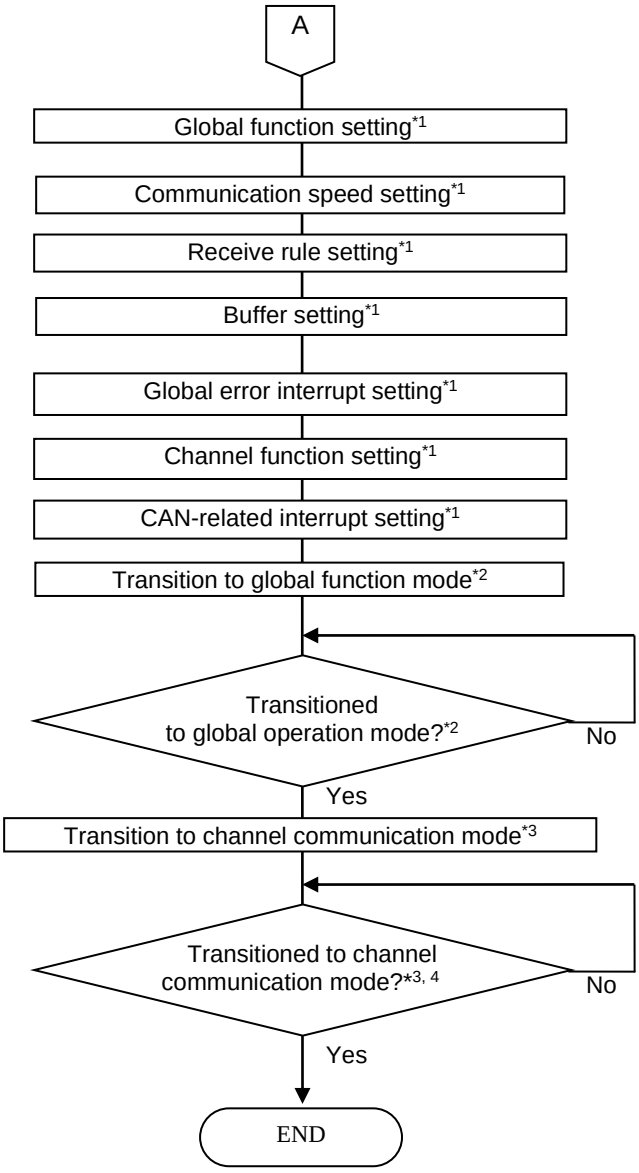
Figure 1-1 and Figure 1-2 shows the procedure of CAN Configuration after CAN Module Enable



【Note】 1. After resetting the MCU, do not access to CAN for RAM before initializing the CAN RAM. (the CAN0EN bit of the PER2 register is "1")

2. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the GMDC[1:0] bit until the mode is switched.
3. Rewrite the interface selection bit (RCMC bit) of GRMCFG register in global test mode only.
4. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.

Figure 1-1 Procedure of CAN Configuration after resetting MCU 1/2



【Note】 1. For processes of each functions, refer to the following chapters.

2. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the GMDC[1:0] bit until the mode is switched.
3. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.
4. After a transitions to channel communication mode, when 11 consecutive recessive bits have been detected, communication is ready (the COMSTS flag in the CmSTS register is “1”) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

Figure 1-2 Procedure of CAN Configuration after resetting MCU 2/2

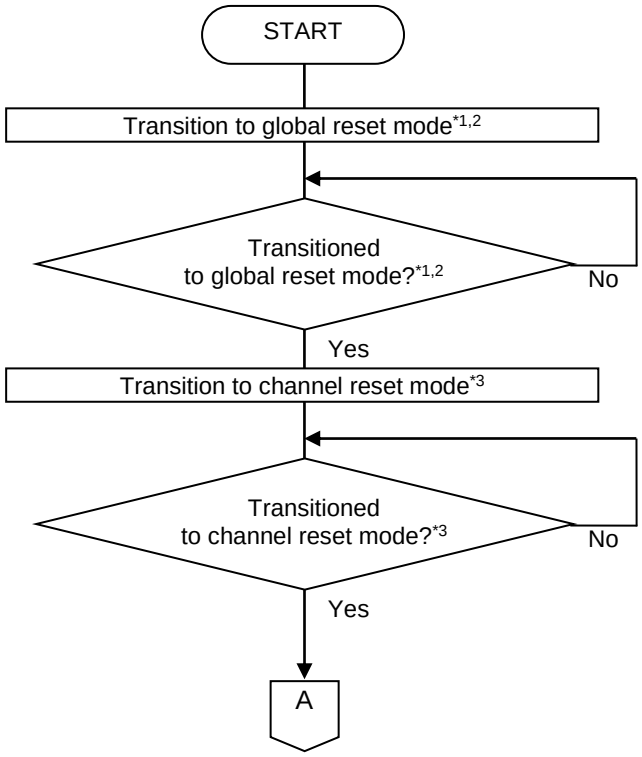
1.2 CAN Configuration after Global Reset Mode

1.2.1 CAN Configuration after Global Reset Mode

Perform the initialization of CAN configuration after global reset mode transition.

1.2.2 Setting Procedures of CAN Configuration after Global Reset Mode

Figure 1-3 and Figure 1-4 shows the procedure of CAN configuration after global reset mode.

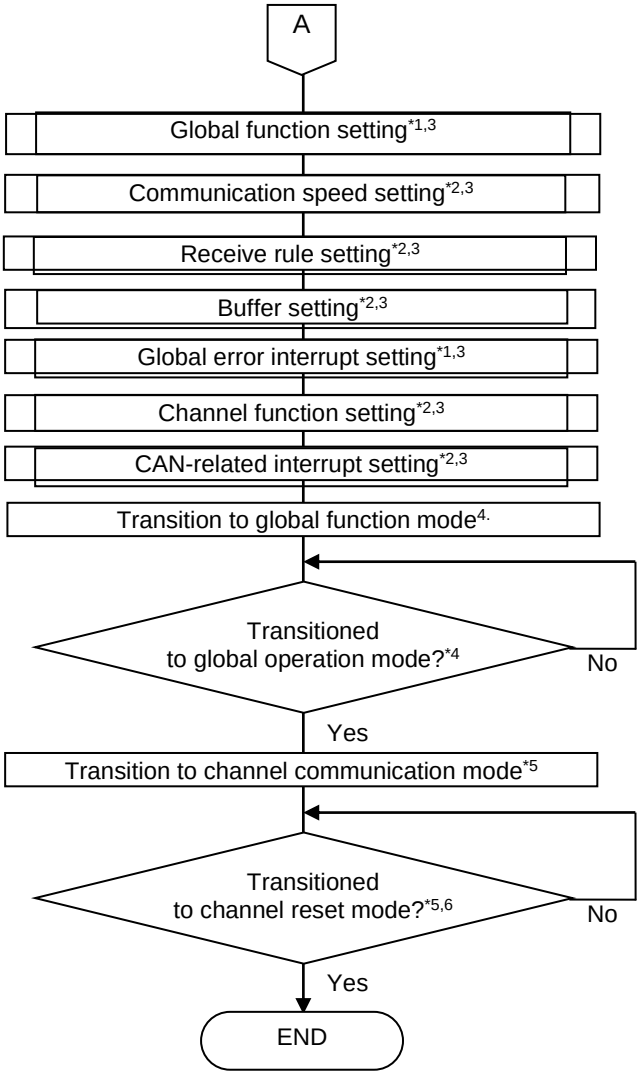


【Note】 1. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the GMDC[1:0] bit until the mode is switched.

2. Channel modes may transition in accordance with transitions of global modes. For details, refer to “Section 2.3,Change of Channel Mode for Transition of Global Mode”.

3. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.

Figure 1-2 Procedure of CAN Configuration after Global Reset Mode 1/2



【Note】 1. These settings and transmissions do not always have to be executed because the values are not reset in the transition of global reset mode.

2. These settings and transmissions do not always have to be executed because the values are not reset in the transition of channel reset mode.
3. For processes of each functions, refer to the following chapters.
4. If you change the global mode (the GSLPR bit of the GCTR register, GMDC [1: 0] bit), check that the mode is switched in the GSTS register. Do not change the GMDC[1:0] bit until the mode is switched.
5. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.
6. After a transitions to channel communication mode, when 11 consecutive recessive bits have been detected, communication is ready (the COMSTS flag in the CmSTS register is “1”) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

Figure 1-3 Procedure of CAN Configuration after Global Reset Mode 2/2

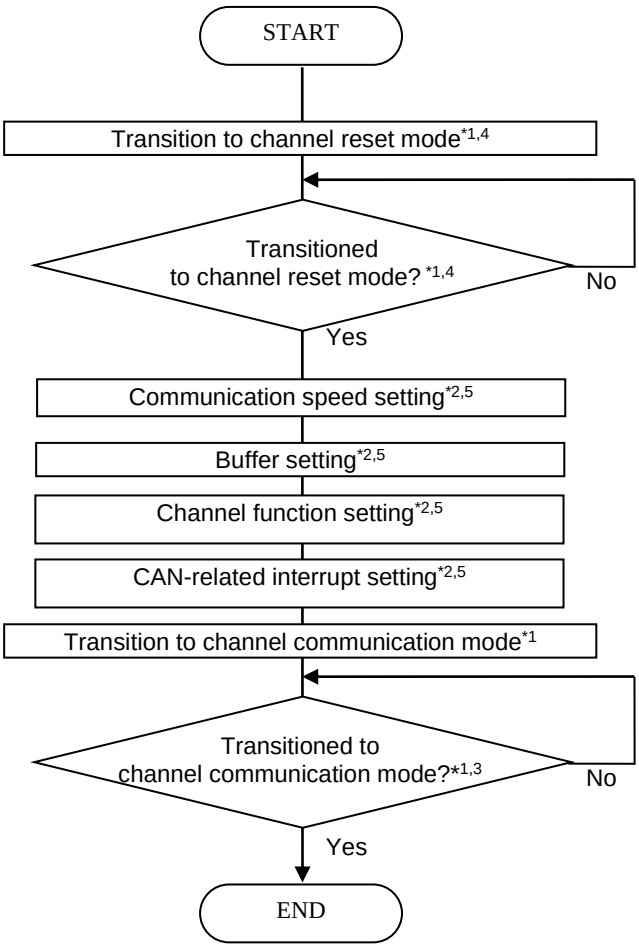
1.3 CAN Configuration after Channel Reset Mode

1.3.1 CAN Configuration after Channel Reset Mode

Perform the initialization of CAN configuration after channel reset mode transition.

1.3.2 Setting Procedures of CAN Configuration after Channel Reset Mode

Figure 1-5 shows the procedure of CAN configuration after channel reset mode.



【Note】 1. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.

2. These settings do not always have to be executed because the values are not reset in the transition of channel reset mode.
3. After a transitions to channel communication mode, when 11 consecutive recessive bits have been detected, communication is ready (the COMSTS flag in the CmSTS register is “1”) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.
4. To channel reset mode is transitioned before communication is completed. To allow transition to channel reset mode after communication is completed, confirm that communication has been completed and transition to channel halt mode has been completed, and then transition to channel reset mode.
5. For processes of each functions, refer to the following chapters.

Figure 1-4 Procedure of CAN Configuration after Channel Reset Mode

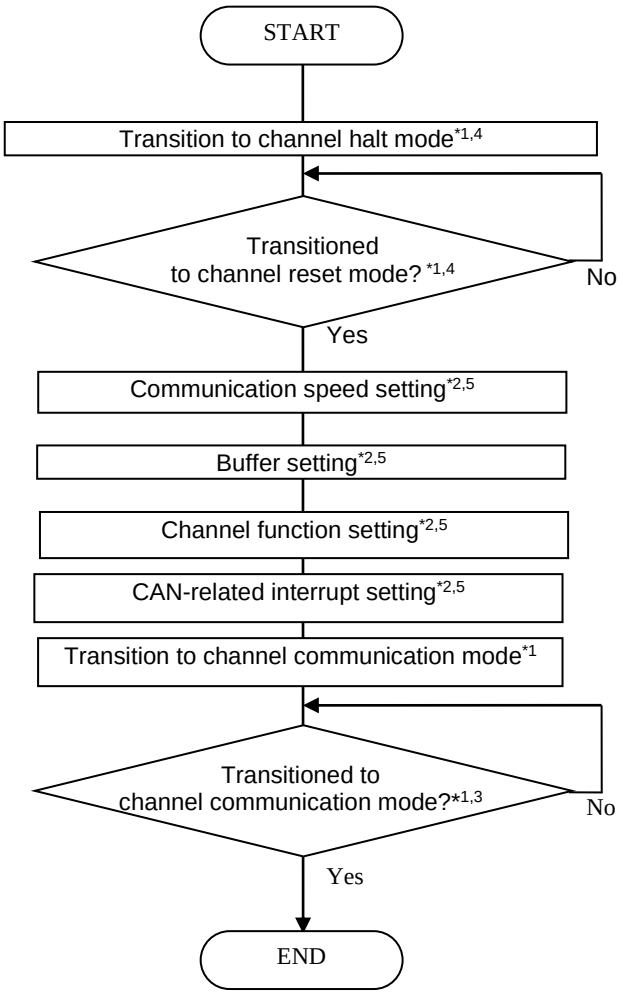
1.4 CAN Configuration after Channel Halt Mode

1.4.1 CAN Configuration after Channel Halt Mode

Perform the initialization of CAN configuration after channel halt mode transition.

1.4.2 Setting Procedures of CAN Configuration after Channel Halt Mode

Figure 1-6 shows the procedure of CAN configuration after channel halt mode.



【Note】 1. If you change the channel mode (the GSLPR bit of the CmCTR register, GHMDC [1: 0] bit), check that the mode is switched in the CmSTS register. Do not change the GHMDC[1:0] bit until the mode is switched.

2. These settings do not always have to be executed because the values are not reset in the transition of channel reset mode.
3. After a transitions to channel communication mode, when 11 consecutive recessive bits have been detected, communication is ready (the COMSTS flag in the CmSTS register is “1”) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.
4. While the CAN bus is locked to the dominant level (BLF flag in the CmERFLL register is “1”), transition to channel halt mode is not made. In that case, enter channel reset mode.
5. For processes of each functions, refer to the following chapters.

Figure 1-5 Procedure of CAN Configuration after Channel Halt Mode

2. CAN State (Mode) Transition

RS-CANFD module has the state of entire channels (here after called Global) and each channel (mode).

The states RS-CANFD module has are shows below.

- Global Mode
  - Global stop mode
  - Global reset mode
  - Global test mode
  - Global operation mode
- Channel Mode
  - Channel stop mode
  - Channel reset mode
  - Channel halt mode
  - Channel communication mode

2.1 Global Mode

This is the mode of entire RS-CANFD mode. Figure 2-1 shows the transition of global mode.

Channel modes may transition in accordance with transitions of global modes. For details, refer to “Section 2.3,Change of Channel Mode for Transition of Global Mode”.

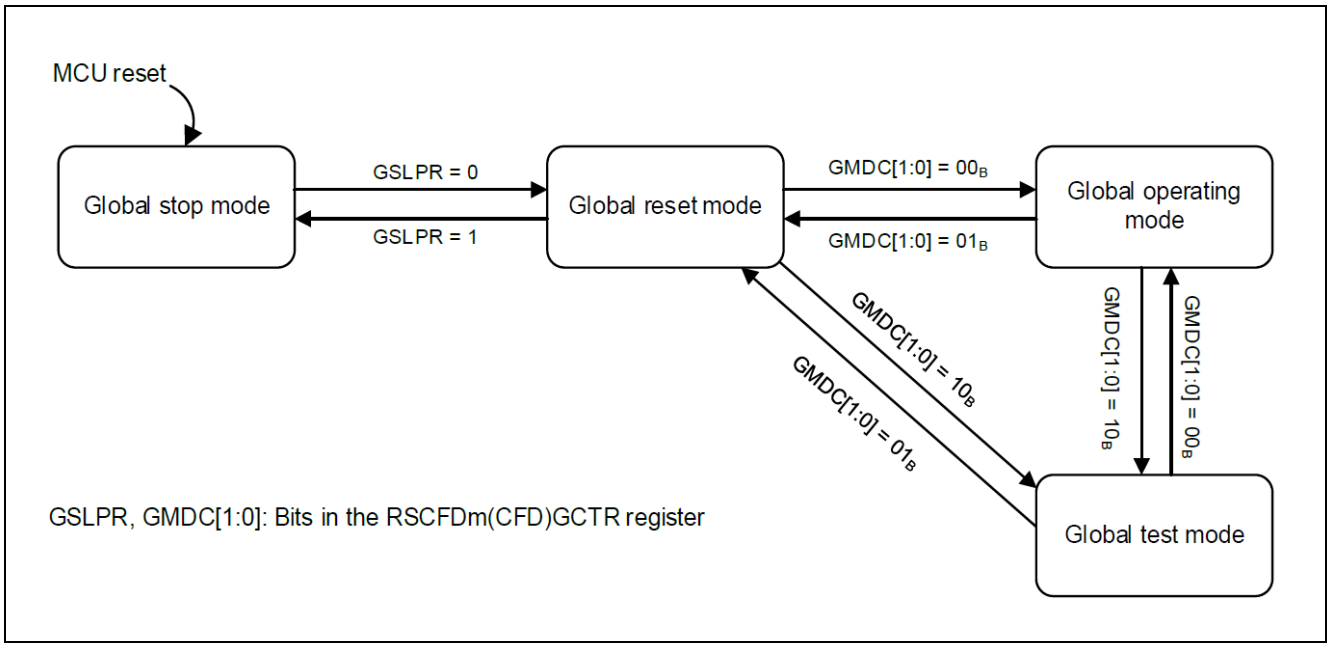


Figure 2-1 Transitions of Global Mode

2.1.1 Global Stop Mode

This mode stop RS-CANFD module clocks. CAN clock do not runt and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.

2.1.2 Global Reset Mode

This mode performs settings for entire RS-CANFD module. When the RS-CANFD module transitions to global reset mode, some registers are initialized. Table 2-2 and Table 2-3 show the list of the registers to be initialized.

2.1.3 Global Test Mode

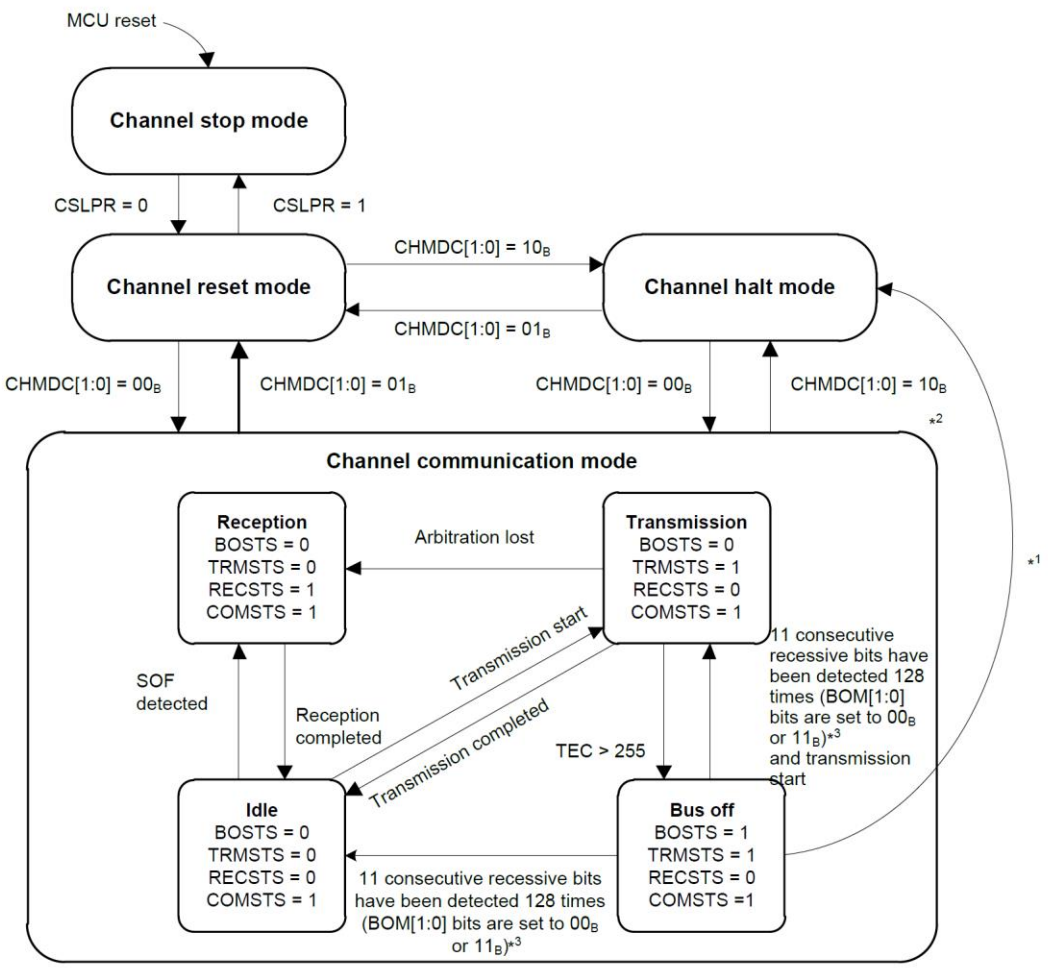
This mode performs settings for test-related resisters. When the RS-CANFD module transitions to global test mode, all CAN communications are disabled.

2.1.4 Global Operation Mode

This mode operates entire RS-CANFD module. When do a communication using each channel, transition to global operation mode is required.

2.2 Channel Mode

These modes is each of the channels. Figure 2-2 Shows a channel mode transition chart.



Note: CHMDC[1:0], CSLPR, BOM[1:0]: Bits in the RSCFDn(CFD)CmCTR register (m = see **Table 21.8**)
BOSTS, TRMSTS, RECSTS, COMSTS: Bits in the RSCFDn(CFD)CmSTS register

Note 1. Timing of transition from bus off state to channel halt mode
When BOM[1:0] = 01_B: Transition to channel halt CHMDC when TEC exceeds 255
When BOM[1:0] = 10_B: Transition to channel halt CHMDC when 11 consecutive recessive bits have been detected 128 times
When BOM[1:0] = 11_B: Transition to channel halt CHMDC when the CHMDC[1:0] bits are set to 10_B

Note 2. While the CAN bus is locked to the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode.

Note 3. When 11 consecutive recessive bits are detected 128 times before the CHMDC[1:0] bits are set to 10_B.

Figure 2-2 Transitions of Channel Mode

2.2.1 Channel Stop Mode

This mode stop RS-CANFD module clocks. CAN clock do not runt and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.

2.2.2 Channel Reset Mode

This mode performs settings for channel. When a transitions to channel reset mode, some channel-related registers are initialized. Table 2-2 shows the list of the registers to be initialized.

2.2.3 Channel Halt Mode

This mode performs settings for test-related resisters of the channel. When a channel transitions to channel halt mode, corresponding CAN communication of the channel stops.

2.2.4 Channel Communication Mode

This mode perform CAN communication. Each cannel waits following communication states during CAN communication.

- Idle
  Neither reception nor transmission is in progress.
- Reception
  Receiving a message sent from another node.
- Transmission
  Transmitting a message.
- Bus off
  Isolated from CAN communication.

2.3 Change of Channel Mode for Transition of Global Mode

Channel modes may transition in accordance with transitions of global modes. Table 2-1 and figure 2-3 show the transitions of channel modes depending on the global mode setting.

Table 2-1 Transitions of Channel Modes Depending on Global Mode Setting

Channel Mode before Setting	Channel Mode after setting			
	Global Operating	Global Test	Global Reset	Global Stop
Channel communication	Channel communication	**Channel halt**	**Channel reset**	*Transition prohibited*
Channel halt	Channel halt	Channel halt	**Channel reset**	*Transition prohibited*
Channel reset	Channel reset	Channel reset	Channel reset	**Channel stop**
Channel stop	Channel stop	Channel stop	Channel stop	Channel stop

【Note】 **Bold** : The positions are transitioned channel mode depending on the transition of global mode.
Red : Restriction

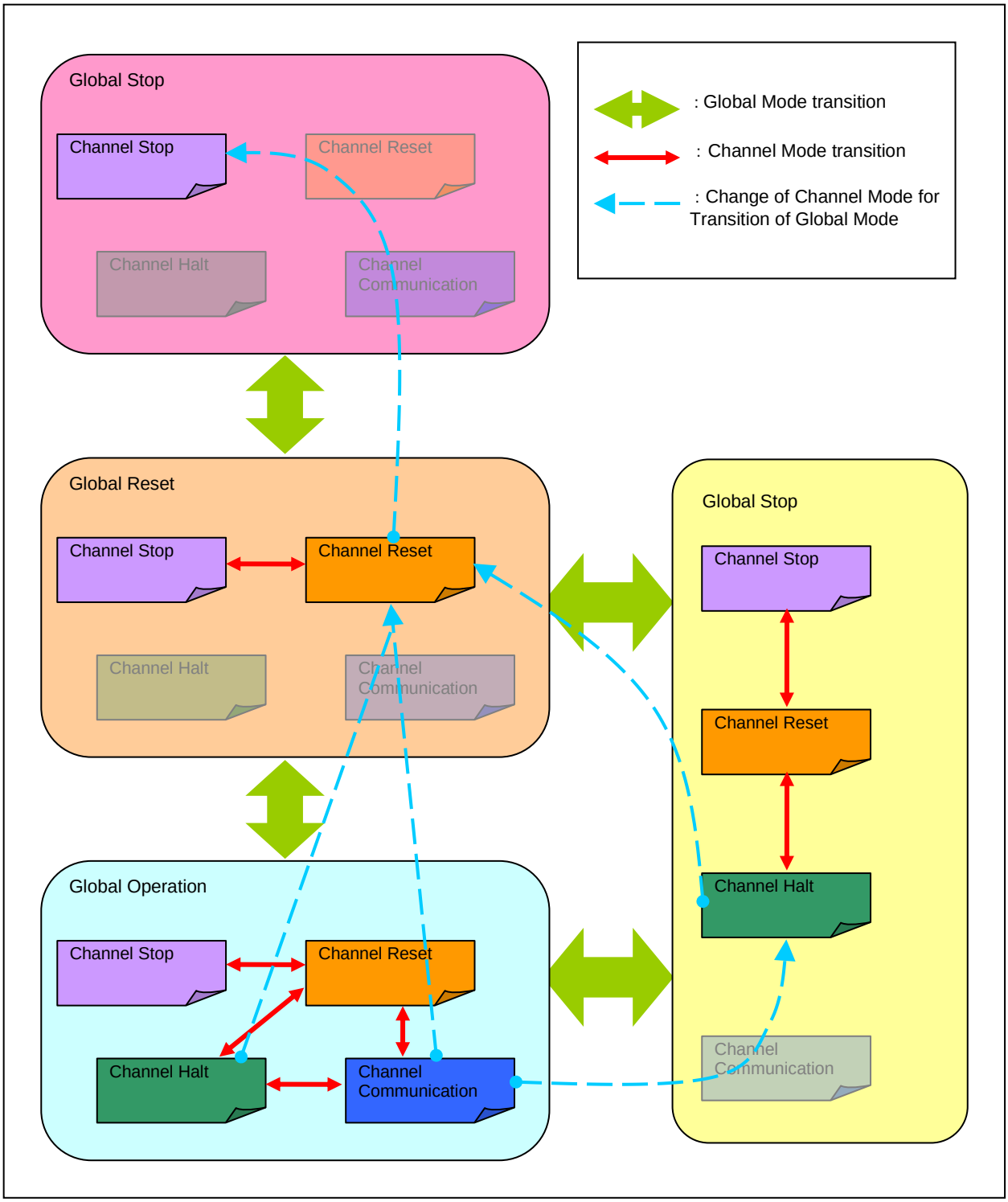


Figure 2-3 Transitions of Global Mode and Channel Mode

Table 2-2 Registers Initialized in Global Reset Mode or Channel Reset Mode

Registers	Bit/Flag
CmCTR register	（ROM）、CRCT、CTMS[1:0]、CTME、CHMDC[3:0]
CmSTS register	CHLTSTS、EPSTS、BOSTS、TRMSTS、RECSTS、COMSTS、（ESIF）、REC[7:0]、TEC[7:0]
CmERFL register	CRCREG[14:0]、ADERR、B0ERR、B1ERR、CERR、AERR、FERR、SERR、ALF、BLF、OVLF、BORF、BOEF、EPF、EWF、BEF
CmFDCTR register	EOCCLR、SOCCLR
CmFDSTS register	SOC[7:0]、EOC[7:0]、SOCO、EOCO、TDCVF、TDCR[6:0]、
CmFDCRC register	CRCREG[20:0]
CFCCk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode : CFE
CFSTSk register	When transmit/receive FIFO buffer is in transmit mode or gateway mode : CFMC[7:0]、CFFLL、CFEMP、CFMLT、CFRXIF、CFTXIF
CFTISTS register	CFkTXIF
TMCp register	TMOM、TMTAR、TMTR
TMSTSp register	TMTARM、TMTRM、TMTRF[1:0]、TMTSTS
TMTRSTSy register	TMTRSTSp (Bits of corresponding channel are initialized in channel reset mode.)
TMTARSTSy register	TMTARSTSp (Bits of corresponding channel are initialized in channel reset mode.)
TMTCSTSy register	TMTCSTSp(Bits of corresponding channel are initialized in channel reset mode.)
TMTASTSy register	TMTASTSp(Bits of corresponding channel are initialized in channel reset mode.)
TXQCCm register	TXQE
TXQSTSm register	TXQIF、TXQFLL、TXQEMP
THLCCm register	THLE
THLSTSm register	THLMC[4:0]、THLIF、THLELT、THLFLL、THLEMP
GTINTSTS0 register	TSIFm、TAIFm、TQIFm、CFTIFm、THIFm（m=0～3）

Note: Bits and flags in parentheses exist only in registers in CAN FD mode.

レジスタ	ビット／フラグ
CiCTRLレジスタ	CHMDC[1:0]
CiCTRHレジスタ	CTMS[1:0]、CTME
CiSTSLレジスタ	CHLTSTS、EPSTS、BOSTS、TRMSTS、RECSTS、COMSTS
CiSTSHレジスタ	REC[7:0]、TEC[7:0]
CiERFLLレジスタ	ADERR、B0ERR、B1ERR、CERR、AERR、FERR、SERR、ALF、BLF、OVLF、BORF、BOEF、EPF、EWF、BEF
CiERFLHレジスタ	CRCREG[14:0]
CFCCLkレジスタ	送受信FIFOバッファが送信モード：CFE
CFSTSkレジスタ	送受信FIFOバッファが送信モード：CFMC[5:0]、CFTXIF、CFRXIF、CFMLT、CFFLL、CFEMP
TMCpレジスタ	TMOM、TMTAR、TMTR
TMSTSpレジスタ	TMTARM、TMTRM、TMTRF[1:0]、TMTSTS
TMTRMSxxレジスタ	TMTRSTSp

TMTCSTSxxレジスタ	TMTCSTSp
TMTASTSxxレジスタ	TMTASTSp
THLCCiレジスタ	THLE
THLSTSiレジスタ	THLMC[3:0]、THLIF、THLELT、THLFLL、THLEMP
CGTISRレジスタ	TSIFi、TAIFi、CFTIFi、THIFi

Table 2-3 Registers Initialized in Global Reset Mode

Registers	Bit/Flag
GSTS register	GHLTSTS
GERFL register	EEF0、EEF1、EEF2、EEF3、（CMPOF）、THLES、MES、DEF
GTSC register	TS[15:0]
RMNDy register	RMNSq
RFCCx register	RFE
RFSTSx register	RFMC[7:0]、RFIF、RFMLT、RFFLL、RFEMP
CFCCk register	When transmit/receive is in receive mode：CFE
CFSTSk register	When transmit/receive FIFO is in receive mode：CFMC[7:0]、CFFLL、CFEMP、CFTXIF、CFRXIF、CFMLT
FESTS register	CFkEMP、RFxEMP
FFSTS register	CFkFLL、RFxFLL
FMSTS register	CFkMLT、RFxMLT
RFISTS register	RFxIF
CFRISTS register	CFkRXIF
CDTCT register	CFDMAEm、RFDMAEx
CDTSTS register	CFDMASTSm、RFDMASTSx
GTSTCFG register	RTMPS[6:0]、C0ICBCE、C1ICBCE、C2ICBCE、C3ICBCE
GTSTCTR register	RTME、ICBCTME

Note: Bits and flags in parentheses exist only in registers in CAN FD mode.

CiCTRL register	CHMDC[1:0]
CiCTRH register	CTMS[1:0]、CTME
CiSTSL register	CHLTSTS、EPSTS、BOSTS、TRMSTS、RECSTS、COMSTS
CiSTSH register	REC[7:0]、TEC[7:0]
CiERFLL register	ADERR、B0ERR、B1ERR、CERR、AERR、FERR、SERR、ALF、BLF、OVLF、BORF、BOEF、EPF、EWF、BEF
CiERFLH register	CRCREG[14:0]
CFCCLk register	When transmit/receive FIFO buffer is in tramsmit mode：CFE
CFSTSk register	When transmit/receive FIFO buffer is in transmit mode：CFMC[5:0]、CFTXIF、CFRXIF、CFMLT、CFFLL、CFEMP
TMCp register	TMOM、TMTAR、TMTR
TMSTSp register	TMTARM、TMTRM、TMTRF[1:0]、TMTSTS
TMTRMSxx register	TMTRSTSp
TMTCSTSxx register	TMTCSTSp
TMTASTSxx register	TMTASTSp
THLCCi register	THLE
THLSTSi register	THLMC[3:0]、THLIF、THLELT、THLFLL、THLEMP
CGTISR register	TSIFi、TAIFi、CFTIFi、THIFi
GSTS register	GHLTSTS
GERFLL register	THLES、MES、DEF
GTSC register	TS[15:0]

レジスタ	ビット／フラグ
GSTSレジスタ	GHLTSTS
GERFLLレジスタ	THLES、MES、DEF
GTSCレジスタ	TS[15:0]
RMNDnレジスタ	RMNSn
RFCCmレジスタ	RFE
RFSTSmレジスタ	RFMC[5:0]、RFIF、RFMLT、RFFL、RFELL
CFCCLkレジスタ	送受信FIFOが受信モード時：CFE
CFSTSkレジスタ	送受信FIFOバッファが受信モード時 : CFMC[5:0]、CFFLL、CFEMP、CFTXIF、CFRXIF、CFMLT
RFMSTSレジスタ	RFmMLT
CFMSTSレジスタ	CFkMLT
RFISTSレジスタ	RFmIF
CFISTSレジスタ	CFkIF
GTSTCFGレジスタ	RTMPS[2:0]
GTSTCTRレジスタ	RTME

3. Communication Speed

Set the communication speed for CAN communication. You need to perform the following settings to determine CAN communication speed.

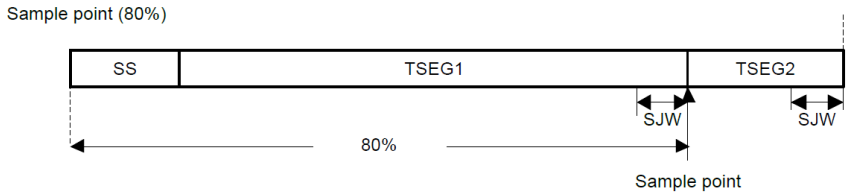
- Bit Timing Setting
- Communication Speed Setting

3.1 CAN Bit Timing Setting

In this CAN bit timing setting of RS-CANFD module, one bit of a communication frame consists of three segments. Figure 3-1 shows segments of bits and sample point.

In these segments, Time Segment 1(called TSEG1 hereafter) and Time Segment 2 (called TSEG2 hereafter) indicate the sample point. Also, it can be changed the timing for sampling by changing the values of segments. FD mode has 2 types of bit rate (nominal bit rate and data bit rate) and be sett for each of them.

This minimum protection area unit of timing setting is called 1 Time Quanta (called Tq hereafter), also it is consisted by inputted clock frequency and baud rate prescaler division value to RS-CANFD module.



Classical CAN mode:
SS = 1 Tq fixed
Set TSEG1 to a range of 4 Tq to 16 Tq
Set TSEG2 to a range of 2 Tq to 8 Tq
Set SJW to a range of 1 Tq to 4 Tq
Set SS + TSEG1 + TSEG2 to a range of 8 Tq to 25 Tq
TSEG1 > TSEG2 ≥ SJW

CAN FD mode:
Nominal bit rate
SS = 1 Tq fixed
Set TSEG1 to a range of 4 Tq to 128 Tq
Set TSEG2 to a range of 2 Tq to 32 Tq
Set SJW to a range of 1 Tq to 32 Tq
Set SS + TSEG1 + TSEG2 to a range of 8 Tq to 161 Tq
TSEG1 > TSEG2 ≥ SJW

DATA bit rate
SS = 1 Tq fixed
Set TSEG1 to a range of 2 Tq to 16 Tq
Set TSEG2 to a range of 2 Tq to 8 Tq
Set SJW to a range of 1 Tq to 8 Tq
Set SS + TSEG1 + TSEG2 to a range of 5 Tq to 25 Tq
TSEG1 ≥ TSEG2 ≥ SJW

- SS (synchronization segment):
  The SS is a segment that performs synchronization by monitoring the edge from recessive to dominant bits in the Interframe Space.
  Interframe Space consists of Intermission, Suspend Transmission, and Bus Idle. All nodes can start transmission during Bus Idle.
- TSEG1 (Time segment 1):
  TSEG1 is a segment that absorbs physical delay on the CAN network. The physical delay on the CAN network is twice of the total of the delay on the CAN bus, the delay in the input comparator, and the delay in the output driver.
- TSEG2 (Time segment 2):
  TSEG2 is a segment that compensates phase error due to an error in frequency.
- SJW (Resynchronization jump width)
  The SJW is a length to extend or reduce the time segment to compensate for an error in phase due to phase error.

Figure 3-1 Bit Segment Components and Sample Point

3.2 Communication Speed Setting

Communication speed is consisted by CAN clock (fCAN) that is clock source of RS-CANFD module , baud rate prescaler division value, and Tq count per bit. fCAN is available for use clkc or clk xincan. For fCAN setting, refer to “Section 4.5, CAN clock source setting”.

Table 3-1 and 3-2 show the main formula and example of communication speed. Table 3-3 shows example of bit timing setting.

Table 3-1 Example of Communication Speed setting (Nominal Bit Rate)

Formula of Communication Speed	fCAN / Nominal Bit Rate Prescaler Division Ration × Tq count of 1 bit time		
fCAN / Comm Speed	40MHz	20MHz	10MHz
1Mbps	10Tq(4) 20Tq(2)	10Tq(2) 20Tq(1)	10Tq(1)
500Kbps	10Tq(8) 20Tq(4)	10Tq(4) 20Tq(2)	10Tq(2) 20Tq(1)
250Kbps	10Tq(16) 20Tq(8)	10Tq(8) 20Tq(4)	10Tq(4) 20Tq(2)
125Kbps	10Tq(32) 20Tq(16)	10Tq(16) 20Tq(8)	10Tq(8) 20Tq(4)
83.3Kbps	8Tq(60) 10Tq(48) 12Tq(40) 15Tq(32) 16Tq(30) 20Tq(24) 24Tq(20)	8Tq(30) 10Tq(24) 12Tq(20) 15Tq(16) 16Tq(15) 20Tq(12) 24Tq(10)	8Tq(15) 10Tq(12) 12Tq(10) 15Tq(8) 20Tq(6) 24Tq(5)
33.3Kbps	8Tq(150) 10Tq(120) 12Tq(100) 15Tq(80) 20Tq(60) 24Tq(50)	8Tq(75) 10Tq(60) 12Tq(50) 15Tq(40) 20Tq(30) 24Tq(25)	10Tq(30) 12Tq(25) 15Tq(20) 20Tq(15)

Note: Values in ( ) are baud rate prescaler division values.

Table 3-2 Example of Communication Speed Setting (Data Bit Rate)

Formula of Communication Speed	fCAN / Data Bit Prescaler Divison Ration × Tq count of 1 bit time	
fCAN / Comm Speed	40MHz	20MHz
5Mbps	8Tq(1)	なし
2Mbps	20Tq(1)	10Tq(1)

Note: Values in ( ) are baud rate prescaler division values.

Table 3-3 Example of Bit Timing Setting

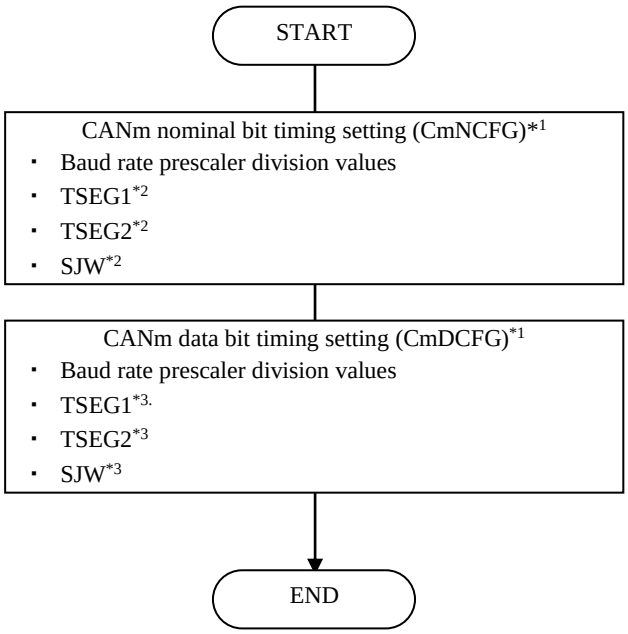
1 Bit	Setting Values（Tq）				Sample Point Percentage (%)
	SS	TSEG1	TSEG2	SJW	
5Tq	1	2	2	1	60.00
8Tq	1	4	3	1	62.50
	1	5	2	1	75.00
10Tq	1	6	3	1	70.00
	1	7	2	1	80.00
16Tq	1	10	5	1	68.75
	1	11	4	1	75.00
20Tq	1	12	7	1	65.00
	1	13	6	1	70.00
	1	15	4	3	80.00
24Tq	1	15	8	1	66.66
	1	16	7	1	70.83
50Tq	1	39	10	4	80.00

3.3 CAN Bit Timing and Communication Speed Setting Procedures

Figure 3-2 shows setting procedures of CAN bit timing and communication speed.

Perform these settings during CAN configuration.

Refer to “Section 1, CAN Configuration” for procedure of CAN configuration.



【Note】 1. Rewrite the CmNCFGL,H register and CmDCFG register in channel reset mode or channel halt mode. Also, set the registers before transitioning channel communication mode and channel hart mode. If you use classical CAN frame only, set the same values to CmDCFG register with CmNCFG register.

2. TSEG1, TSEG2, and SJW settings need to meet following conditions.
   TSEG1＞TSEG2 ≧ SJW
3. TSEG1, TSEG2, and SJW settings need to meet following conditions.
   TSEG1≧TSEG2 ≧ SJW

Figure 3-2 5.1 Setting up CAN Bit Timing and Communication Speed

4. Global Function

Set the following functions that are common to entire RS-CANFD Module (all channels).

- Transmit priority setting
- DLC check setting
- DLC replacement function setting
- Mirror function setting
- CAN clock source setting
- Timestamp clock setting
- Interval timer prescaler setting

4.1 Transmit Priority Setting

Set the transmit priority when the transmit request is requested from multiple transmit buffer in the same channel.

It is not able to set the transmit priority for each channel because the transmit priority is common to entire channels.

You can choose following two of judgment methods.

- **ID priority**
  The messages are transmitted according to the priority of stored message IDs. Priority of IDs conforms to the CAN bus arbitration specification defined in the CAN specification.
  Targets of priority determination are IDs of messages placed in transmit buffers, transmit/receive FIFO buffers (set to transmit mode or gateway mode★), and transmit queues.
  When transmit/receive FIFO buffers is used, the oldest message in a FIFO buffer becomes a target of priority determination.
  When a message is being transmitted from a transmit/receive FIFO buffer, the next message in the same FIFO buffer becomes a target of priority determination.
  When transmit queues are used, all messages in transmit queues are targets of priority determination.
  When the same ID is set for two or more buffers, the buffer with a lower number takes precedence.

- **Transmit buffer number priority**
  the message in the transmit buffer whose number is the lowest among buffers having transmit requests are transmitted first.
  When transmit/receive FIFO buffers is linked to transmit buffers, transmit priority is determined according to the linked transmit buffer numbers.

When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again whichever transmit priority is selected.

【Note】1. It is prohibited to select when using transmit queue. Select the ID priority.

4.2 DLC Check Setting

Set the ability and disability of DLC check function.

When the DLC check function is enabled, DLC filter processing is performed for messages that pass through the acceptance filter processing.

When the DLC check function is disenabled, DLC check is not performed after performing acceptance filter processing.

In DLC check, when the DLC value in a message is equal to or larger than the DLC value set in the receive rule, the message passes through the DLC filter processing. When the DLC value of the received message is smaller than that of the receive rule, the message does not pass through the DLC filter processing. In this case, the message is not stored in the receive buffer or the FIFO buffer and a DLC error is present.

Please refer to “Section 5, Receive Rule Table” for the receive rule.

4.3 DLC Replacement Function

Set the ability and disability of DLC replacement function.

DLC replacement is effective only when DLC check function is enabled.

When DLC replacement is enabled, the DLC value of the receive rule is stored in the buffer instead of the DLC value of the received message. In this case, a value of “00’H” is written to data bytes that are larger than the DLC value of the receive rule.

When DLC replacement is enabled, the DLC value of the received message is stored in the buffer. In this case, all the data bytes in the received message are stored in the buffer.

Please refer to “Section 5, Receive Rule Table” for the receive rule.

Table 4-1 DLC Filter Processing and DLC Replacement Processing

GCFGL Register		Received message DLC ／Receive rule DLC	Received Message	
DCE Bit	DRE Bit		Processing	Stored DLC
0 (DLC check disabled)	0 (DLC replacement is disabled)	Received message DLC ＜Received rule DLC	Stored to buffer*1	Received message DLC
		Received message DLC ≧Received rule DLC		
		Received rule DLC＝0		
	1 (DLC replacement is enabled)	Received message DLC ＜Received rule DLC		
		Received message DLC ≧Received rule DLC		
		Received rule DLC＝0		
1 (DLC check is enable)	0 (DLC replacement is disabled)	Received message DLC ＜Received rule DLC	Discard (DLC error)	—
		Received message DLC ≧Received rule DLC	Stored to buffer	Received message DLC
		Received rule DLC＝0	Stored to buffer	Received message DLC
	1 (DLC replacement is enabled)	Received message DLC ＜Received rule DLC	Discard (DLC error)	—
		Received message DLC ≧Received rule DLC	Stored to buffer	Received rule DLC*2
		Received rule DLC＝0	Stored to buffer	Received message DLC

【Note】1.DLC check itself is not performed.

2. “00’H” is written to data bytes that are larger than the DLC of the receive rule.

4.4 Mirror Function Setting

Set the ability and disability of mirror function.

The mirror function allows reception of own transmitted messages. When the mirror function is in use, receive rules for which mirror function is unused are applied to the data processing for messages received from other CAN nodes. When own transmitted messages are received, receive rules for which mirror function is unused are used for data processing.

Please refer to “Section 5, Receive Rule Table” for the receive rule.

Table 4-2 DLC Filter Processing and DLC Replacement Processing

MME Bit of GCFGL Register	GAFLLB Bit of GAFLDHj Register	Message Targeted for Data Processing of Receive rule
0 (Mirror function is disabled)	0	Message received from other CAN node
	1	No targeted message
1 (Mirror function is enabled)	0	Message transmitted from other CAN node
	1	Own transmitted message transmitted

4.5 CAN Clock Source Setting

Set the CAN clock (fCAN) which is clock source of CAN clock source in DCS bit of GCFG register. The clocks enabled as CAN clock source are shown below.

- clk_xincan
- clkc

4.6 Timestamp Clock Setting

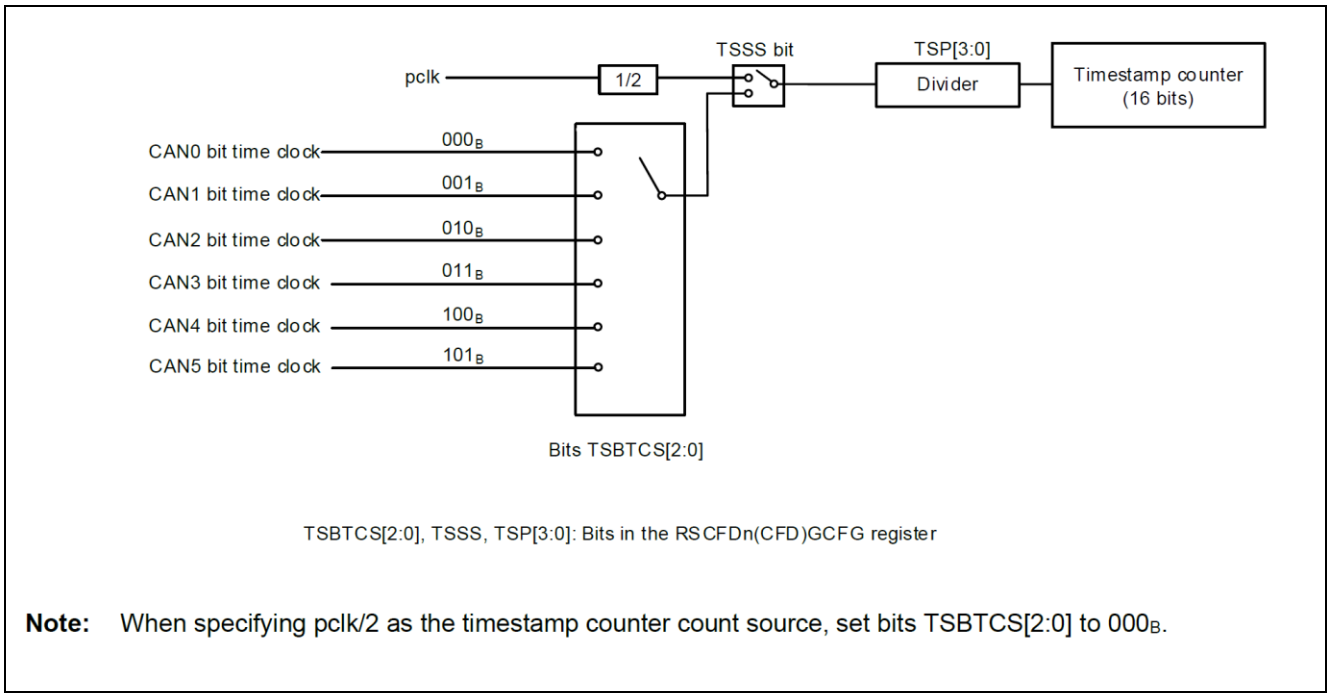
Set the clock source and the Division Ration for using timestamp clock.
The timestamp counter is a 16-bit free-running counter used for recording the message reception time and transmission time. The timestamp counter value is fetched at the SOF (Start of Frame)[*1] of the message and is then stored in a receive buffer or a FIFO buffer together with the message ID and data during data reception.

You can select the following clocks for using timestamp.

- pclk/2
- CANm nominal time clock

When the nominal CANm bit time clock is used as a clock source, the timestamp counter stops when the corresponding channel transitions to channel reset mode or channel halt mode. When pclk/2 is used as a clock source, the timestamp function is not affected by channel mode.

Figure 4-1 show the timstop function block diagram.



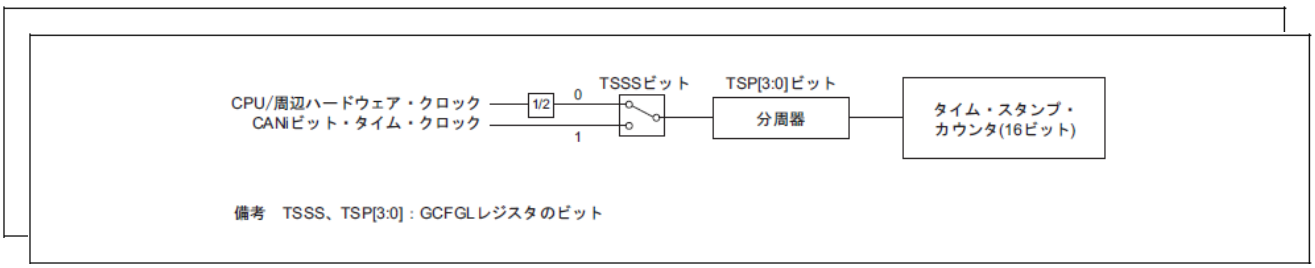


Figure 4-1 Timestamp Function Block Diagram

【Note】 1. Start Of Frame
Field represent start of frame

4.7 Interval Timer Prescaler Setting

Set the prescaler value when pclk is selected as an interval timer count source.

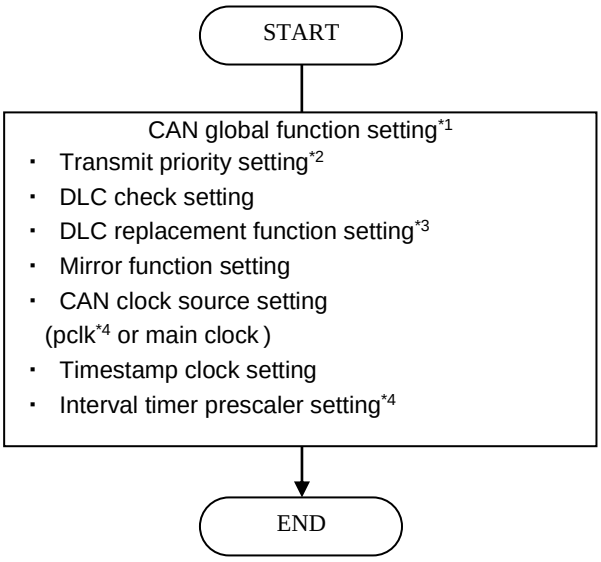
Please refer to “Section 6.4.3, Interval Timer Counter Setting” for interval timer function.

4.8 Global Function Setting

Figure 4-2 show global function setting procedures.

Perform these settings during CAN configuration.

Prese refer to “Section 1, CAN Configuration” for CAN configuration setting procedure.



【Note】 1. Rewrite the GCFG register in channel reset mode.

2. Select the ID priority (TPRI bit of GCFG register is “0”) when using transmit queue.
3. If you disabled DLC (DCE bit of GCFG register is “0”) check function, disable the function after setting “0” to DLC of receive rule table(GAFLDLC bit of GAFLP0j register).
4. Set pclk to 46MHZ or more.
5. If you use pclk for interval timer counter source, do not set “H’0000” to interval timer prescaler (ITRCP[15:0] bit of GCFG register).

Figure 4-2 Global Function Setting Procedure

5. Receive Rule Table

Set receive rule table for filtering received message.

Data processing using the receive rule table store selected messages to the specified buffer. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function processing.

Following setting is required for receive rule.

- Receive rule setting
- IDE/RTR/ID setting
- Receive rule target message setting
- IDE mask/RTR mask/ID mask setting
- DLC check setting
- Receive rule label setting
- Stored buffer setting

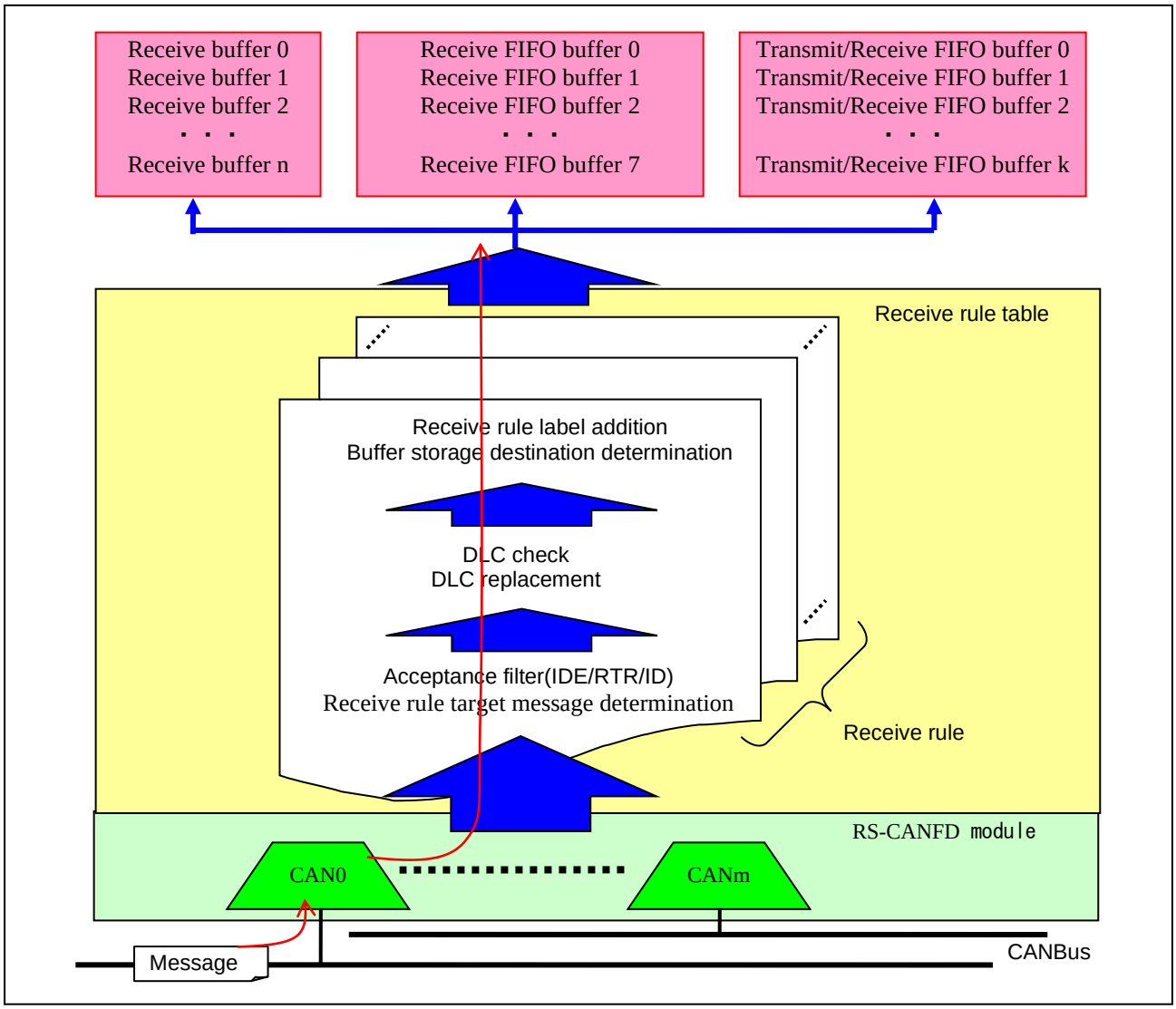


Figure 5-1 Filtering Image by Receive Rule Table

5.1 Receive Rules Setting

Set the receive rules for each channel.

The receive rules are 64×channels in entire module, and the maximum channel unable to register channel rules to a channel are 128.

Check processes begin with the lowest channel rule number in ascending order. When all the bits to be compared in a received message match the bits set in the receive rule or when all the receive rules are compared without any match, filter processing stops. When there is no matching receive rule, the received message is not stored in the receive buffer or FIFO buffer.

The restrictions of receive rules can be registered are shown below.

- Restriction of receive rules for each channel
  - CAN0 receive rules≦64 × channels
    ・
    ・
    ・
  - CANm receive rules≦64 × channels

- Restriction of all receive channels
  CAN0 receive rules ＋・・・＋CANm receive rules≦64 × channels

Figure 5-2 shows the receive rules registration diagram when channel 0,1 is used.

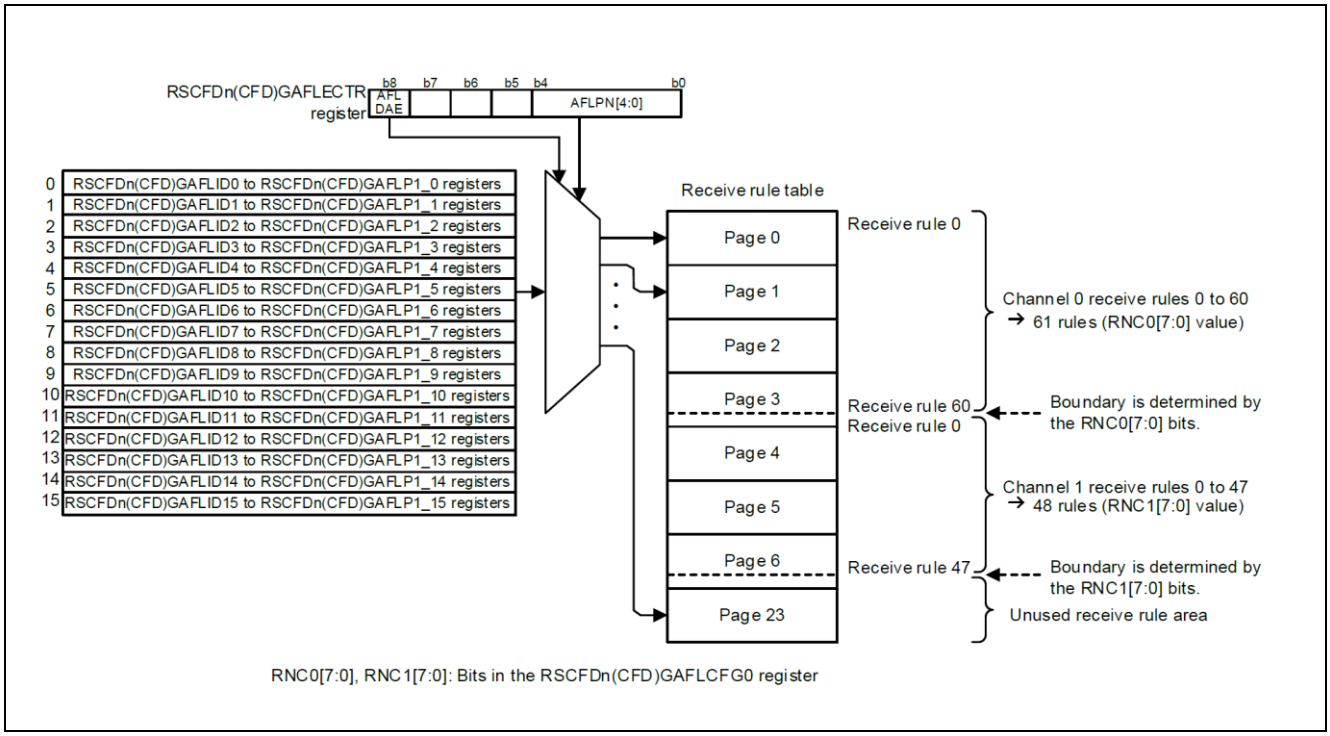


Figure 5-2 Receive Rule Registration (in the case of setting channel 0 and 1)

5.2 IDE/RTR/ID Setting

Set the ID format (standard ID or extended ID), frame format(data frame or remote frame), and receive ID of the received message.

5.3 Receive Rule Target Message Setting

When you set the transmitted message from another CAN node (GAFLLB bit of GAFLIDHj register is “0”), data processing to be performed using the receive rule when a message transmitted from another CAN node is received.

When you set the own transmitted message using mirror function (GAFLLB bit is “1”), data processing to be performed using the receive rule when the own transmitted message is received.

Please refer to “Section 4.4, Mirror Function Setting” for mirror function.

5.4 IDE Mask/RTR Mask/ID Mask Setting

Set the mask value that is set in IDE/RTR/ID.

The bit that is not masked in IDE mask/RTR mask/ID mask becomes effective by acceptance filter.

5.5 DLC Check Counter Value Setting

Set DLC value of the receive rule which is compered with DLC value of received message when DLC check is allowed DLC.

Please refer to “Section 4.2, DLC check setting” for DLC check.

5.6 Routing Processing

When the payload length of the received message exceeds the payload storage size of the storage buffer, the CMPOF flag in the GERFL register is set to 1 (payload overflow) and the processing is handled according to the CMPOC bit in the GCFG register. When the CMPOC bit is “0”, the received message which exceeds the payload storage size is not stored in the buffer. When the CMPOC bit is “1”, the received message is stored in the buffer with payloads exceeding the storage size being discarded.

5.7 Receive Rule Label Setting

Set added 12-bit label information when message that passed through filter processing is stored to buffer.

It is possible to set label voluntary, and it is able to freely use received message label by program. For example, if you set the receiving channel number to the label, it is possible to check which channel the message with same ID in the receive FIFO buffer was received.

5.8 Store Buffer Setting

Set the buffer stored the message that passed through filter processing.

Buffers be unable to select as storage destination are shown below.

- Receive buffer q (For 1 receive rule, 1 buffer is selectable.)
- Receive FIFO buffer q
- Transmit/Receive FIFO buffer k (receive mode)

Maximum 2 store buffer is selectable for 1 receive rule. However, It is only possible to select 1 buffer as storage destination. (For example, it is not possible to store to receive buffer 0 and 1.)

Example of maximum storage destination)

- Max 2 buffer = (Receive FIFO buffer x) : 1 piece
  ＋receive buffer q : 1 piece
- Max 2 buffer = (Receive FIFO buffer ＋ Transmit/Receive FIFO buffer k) : 2 piece

Unable/ Disable setting example)

○ : Store to receive buffer 0, receive FIFO buffer 2, and receive FIFO buffer 3

× : Store to receive buffer 0, receive buffer 1, and receive FIFO buffer 2 ＊Disable to store 2 receive buffer.

5.9 Receive Rule Usage Example

Receive rule usage example are shown below.

- Example. 1
  Example of each register is shown when below messages are received.
  - ID format : Standard ID
  - Message format : Data frame
  - Mirror Function : Massage receive from another CAN node
  - Receive ID : 120h,121h,122h,123h
  - DLC : Receive message DLC≧6
  - Label : 010h
  - Storage destination buffer : Receive buffer 3、Receive FIFO buffer 0, 1, 2

		GAFLIDE/GAFLIDEM	GAFLRTR/GAFLRTRM	GAFLLB	GAFLID/GAFLIDM			
GAFLIDLj,Hj		0	0	0	B’00000	B’00000000	B’00000001	B’00100000
GAFLMLj,Hj		1	1	—	B’00000	B’00000000	B’00000111	B’11111100
Receivable message	H’120	0	0	0	B’-----	B’--------	B’-----001	B’00100000
	H’121				B’-----	B’--------	B’-----001	B’00100001
	H’122				B’-----	B’--------	B’-----001	B’00100010
	H’123				B’-----	B’--------	B’-----001	B’00100011

	GAFLDLC	GAFLPTR	GAFLRMV	GAFLRMDP	GAFLFDP
GAFLP0Hj	6	H’010	—	—	—
GAFLP0Lj	—	—	1	3	B’00011

- Example. 2
  Example of each register is shown when below messages are received.
  — ID format : Standard ID
  — Message format : Remote frame, Data frame
  — Mirror Function : Massage receive from another CAN node
  — Receive ID : 130h
  — DLC : Unused DLC check
  — Label : 130h
  — Storage destination buffer : Receive FIFO buffer 4, 6, Transmit/Receive FIFO buffer 1, 2

		GAFLIDE/GAFLIDEM	GAFLRTR/GAFLRTRM	GAFLLB	GAFLID/GAFLIDM			
GAFLIDLj,Hj		0	0	0	B’00000	B’00000000	B’00000001	B’00110000
GAFLMLj,Hj		1	0	—	B’00000	B’00000000	B’00000111	B’11111111
Receivable Message	H’130（Data）	0	0	0	B’-----	B’--------	B’-----001	B’00110000
	H’130（Rmt）	0	1	0	B’-----	B’--------	B’-----001	B’00110000

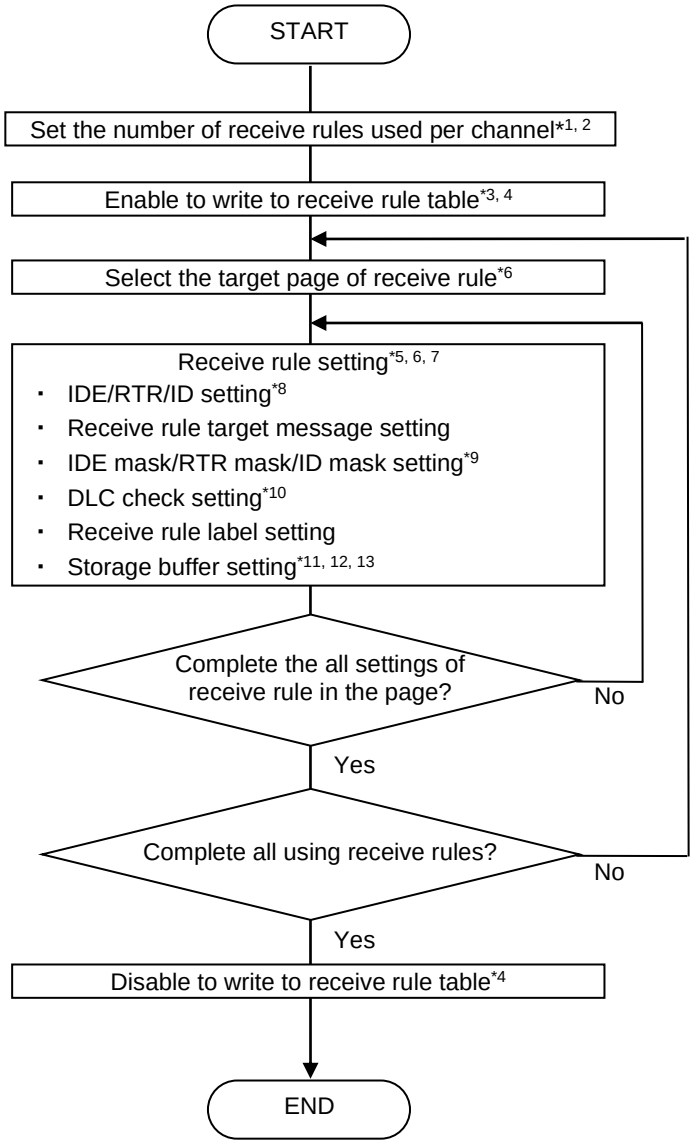
	GAFDLC	GAFLPTR	GAFLRMV	GAFLRMDP	GAFLFDP
GAFLP0Hj	0	H’130	—	—	—
GAFLP0Lj	—	—	0	0	B'10001

5.10 Receive Rule Table Setting Procedures

Figure 5-3 show receive rule table setting procedures.

Set these settings during CAN configuration.

Please refer to “section 1, CAN Configuration” for CAN configuration processing.



【Note】 1. Rewrite number of receive rule setting (RNCm [7:0]bit of GAFLCFGy register) in global reset mode.

2. Meet following conditions for the number of receive rules used per channel(RNCm[7:0] bit).
   ・Set number of channel rules 128 or less 1.
   ・The total of the number of rules allocated to each channel is not larger than the number of rules permitted to the entire module.
3. Unable to write to receive rule table in global reset mode (AFLDAE bit of GAFLECTR register is “1”).
3. Disable to write (AFLDAE bit of GAFLECTR register is “0”) after completed to write to receive rule table.

4. Do not set the page more than number of pages that can be set in module to setting target page.
5. Rewrite receive rule(GAFLIDj register, GAFLMj register, GAFLP0j register, GAFLP1j register) in the condition enabled to write to receive rule table and global reset mode.
6. Set receive rule continusly for each cahnnel. It is diabled to share and set alternately with another channel.
7. In standard ID, set standard ID values to b10~b0 ID(GAFLID[28:0] bit of GAFLIDj register), and set “0” to b28~b11.
8. If IDE bit is not compared (GAFLIDEM bit of GAFLMj register is “0”), set “do not compared all bit” (all GAFLIDEM[28:0] bit of GAFLMj register is “0”).
9. It is effective if DLC check function is allowed(DCE bit of GCFG register is “1”).
10. Maximum 8 FIFO buffers can be selected. However, maximum 7 buffers can be selected if the message is stored to receive buffer (GAFLRMV bit of GAFLP0j register is “1”).
11. Only select transmit/receive buffer set to receive FIFO buffer and receive mode, or gateway mode★.
12. If you select receive buffer as storage destination, enable to receive buffer (GAFLRMV bit is “1”), and set the number smaller than the number used receive buffer (Setting values to NRXMBm[7:0] bit of RMNBy register).

Figure 5-3 Receive Rule Table Setting Processing

6. Buffer, FIFO Buffer

Set buffer used in transmit/ receive and FFO buffer. Following buffer and FIFO buffer setting are required.

- Receive buffer setting
- Receive FIFO buffer setting
- Transmit/Receive FIFO buffer setting
- Transmit buffer setting
- Transmit qeue
- Transmit history buffer setting
- Payload strage size

The restriction of settable number of buffers to receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer are showed below.

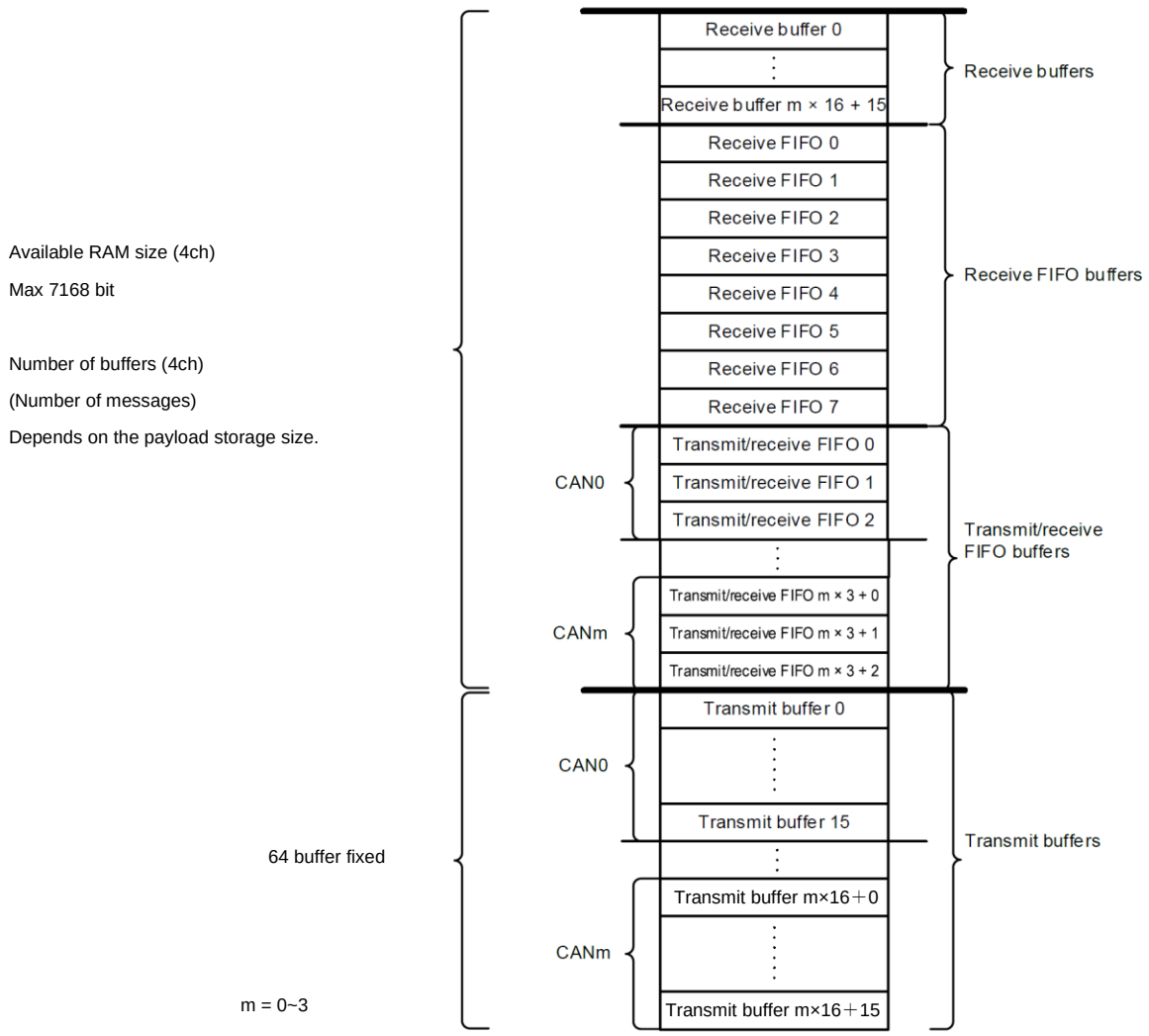
Receive buffer × （12＋Payload strage size）

＋Total (Stage number × (12＋Payload strage size)) of Receive FIFO buffer x

＋Total (Stage number × (12＋Payload strage size)) of Transmit/Receive FIFO buffer k

≦7168 byte

Figure 6-1 shows buffer configuration.



Note: Receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer are set continually.

Figure 6-1 Buffer Configuration

6.1 Receive Buffer Setting

Set number of buffer assigned to buffer and payload size abled to store to per buffer. It is possible to assign buffers of 0~16×number of channels to receive buffer. Receive buffer is not able to use if “0” is set to number of receive buffer.

There is no setting of related interrupt because there is no interrupt of related receive buffer.

6.2 Receive FIFO Buffer Setting

Required settings used for receive FIFO buffer are showed below.

- Number of buffers and payload size setting
- Interrupt enable/disable setting, and interrupt source setting

6.2.1 Number of Buffers setting

Set number of buffer assigned to FIFO buffer and payload size.

There are 8 receive buffers, and maximum 128 buffers can be assigned.

Number of buffers assigned to receive FIFO buffer are able to select from 0[*1], 4, 8, 16, 32, 48, 64, 128.

6.2.2 Interrupt enable/disable Setting, and Interrupt Source Setting

Set interrupt enable/disable setting, and interrupt source setting.

When you use receive FIFO interrupt, interrupt source able to select below.

- Receive FIFO interrupt occur (RFM bit of RFCCx register is “0”) when RFIGCV[2.0] bit of RFCCx register meet following conditions.
  - When the message stored to receive FIFO buffer is 1/8 full.[*2]
  - When the message stored to receive FIFO buffer is 2/8 full.
  - When the message stored to receive FIFO buffer is 3/8 full.[*2]
  - When the message stored to receive FIFO buffer is 4/8 full.
  - When the message stored to receive FIFO buffer is 5/8 full.[*2]
  - When the message stored to receive FIFO buffer is 6/8 full.
  - When the message stored to receive FIFO buffer is 7/8 full.[*2]
  - When receive FIFO buffer is full.
- Receive FIFO interrupt occurs every time when a message reception is completed (RFIM bit of RFCCx register is “1”).

【Note】 1. If you do not use receive FIFO buffer, set 0 message (RFDC[2:0] bit of RFCCx register is “B’000”) to buffer number of receive FIFO buffer.

2. Do not set if you set 4 messages (RFDC[2:0] bit is “B’001”) to buffer number of receive FIFO buffer.

6.3 Transmit/Receive FIFO Buffer Setting

Required settings for using transmit/receive FIFO is shown below.

- Number of buffers setting
- Interrupt enable/disable setting, and interrupt source setting
- Transmit/Receive FIFO mode setting
- Interval timer counter setting (Transmit mode, gateway mode★)
- Transmit buffer link setting (Transmit mode, gateway mode★)

6.3.1 Number of buffers setting

There are three transmit/receive FIFO buffers for each channel, and maximum 128 buffers are assigned. Number of buffers assigned to transmit/receive FIFO buffer are able to select from 0*1, 4, 8, 16, 32, 48, 64, 128.

6.3.2 Interrupt Enable/Disable Setting, and Interrupt Source Setting

Set interrupt enable/disable setting, and interrupt source setting of each transmit/receive FIFO buffer. Table 6-1 shows settable interrupt source for each transmit/receive FIFO mode.

Table 6-1 Transmit/Receive FIFO Buffer interrupt source

Transmit/Receive FIFO Mode	CFIM Bit of CFCCLk Register	Interrupt Source
Receive Mode	0	When receive message is met condition set in CFIGCV[2:0] bit of CFCCLK register, receive complete interrupt of transmit/receive FIFO is occurred. CFIGCV[2:0] bit setting 000_B : When the message stored to receive FIFO buffer is 1/8 full.*2 001_B : When the message stored to receive FIFO buffer is 2/8 full. 010_B : When the message stored to receive FIFO buffer is 3/8 full.*2 011_B : When the message stored to receive FIFO buffer is 4/8 full. 100_B : When the message stored to receive FIFO buffer is 5/8 full.*2 101_B : When the message stored to receive FIFO buffer is 6/8 full. 110_B : When the message stored to receive FIFO buffer is 7/8 full.*2 111_B : When receive FIFO buffer is full.
	1	Receive complete interrupt of transmit/receive FIFO is occurred when a message reception is completed.
Transmit Mode	0	Receive complete interrupt of transmit/receive FIFO is occurred when buffer becomes empty by completed message transmit.
	1	Receive complete interrupt of transmit/receive FIFO is occurred when a message transmit is completed.

【Note】 1. If you do not use transmit/receive FIFO buffer, set 0 message (CFDC[2:0] bit of CFCCLk register is “B’000”) to buffer number of transmit/receive FIFO buffer.
2. Do not set if you set 4 messages (RFDC[2:0] bit is “B’001”) to buffer number of transmit/receive FIFO buffer.

Transmit/Receive FIFO transmit complete interrupt becomes occurrence source of CANm transmit interrupt. The occurrence sources of CANm transmit interrupt are shown below.

CANm transmit complete interrupt

CANm transmit abort interrupt

CANm transmit/receive FIFO transmit comlete interrupt

CANm transmit qeue interrupt

CANm transmit history interrupt

6.3.3 Transmit/Receive FIFO Mode Setting

Set transmit/receive FIFO buffer mod. It is possible to select receive mode or transmit mode.

— Receive mode
  Operate as receive FIFO.
— Transmit mode
  Operate as transmit FIFO.

6.3.4 Interval Timer Counter Setting

Set counter source of interval timer counter and transmission interval. The interval timer counter is effective in transmit mode and gateway mode★.

Table 6-2 shows the count source of interval timer counter and formula of interval time.

Table 6-2 Count Source of Interval Timer counter and Formula of Interval Time

CFITR bit and CFITSS bit of CFCCHk register	Count Source	Formula
B’00	Clock obtained pclk by dividing ITRCP[15:0] of GCFGH register.	$1/f_{CLK} \times 2 \times a \times b$
B’10	10 times divided clock of clock obtained pclk by ITRCP[15:0] of GCFGH register.	$1/f_{CLK} \times 2 \times a \times 10 \times b$
B'x1	CANm nominal bit time clock	$1/f_{CANBIT} \times b$

【Note】 a : pclk prescaler value (setting value of ITRCP[15:0] bit)
b : Setting value of message transmit interval (CFITT[7:0] bit of CFCCHk register)
f_{CLK} : pclk frequency
f_{CANBIT} : CANm nominal bit time clock frequency

6.3.5 Transmit Buffer Link Setting

Link transmit/receive FIFO buffer to transmit buffer. The transmit buffer is effective in transmit mode and gateway mode★.

Do not assigin transmit buffer linked to transmit/receive FIFO buffer to receive qeue. Only one transmit/receive FIFO buffer can be linked to one transmit buffer. Do not link several transmit/receive FIFO buffers to the same number of transmit buffers.

6.4 Transmit Buffer Setting

Set transmit complete interrupt enable/disable for each transmit buffer.

The transmit buffer has 16 buffers per one channel, and it is able to use as either transmit buffer, transmit/receive FIFO buffer (transmit mode and gateway mode★) for link , or transmit queue.

When you use the transmit buffer as either transmit/receive FIFO buffer (transmit mode and gateway mode★) for link or transmit queue, set “H’00” to corresponding TMCp register. Also, set “0” (interrupt disable) to TMIEp bit of TMIECy register.

In addition, transmit complete interrupt becomes source of CANm transmit interrupt. Occurrence source of CANm transmit interrupt are shown below.

— CANm transmit complete interrupt
— CANm transmit abort interrupt
— CANm transmit/receive FIFO transmit complete interrupt
— CANm transmit queue interrupt
— CANm transmit history interrupt

6.5 Transmit Queue Setting

Required settings for using transmit queue are shown blow.

- Number of buffers setting
- Interrupt enable/disable setting, and interrupt source setting

6.5.1 Number of Buffers Settings

Set buffer number of transmit queue.

There is one transmit queue per channel, and up to 16 buffers are assinged. The transmit quque is assinged in descending order from the transmit buffer number [(16×m+15)]. Also, transmit buffer [(16×m+15)] becomes a common access window of each channel.

Select the transmit priority to ID priority when transmit qeue is used.

6.5.2 Interrupt Enable/Disable Setting, and Interrupt Source Setting

Set interrupt enable/disable setting and interrupt source setting. The intterrupt source that can be set when transmit queue intrrupt is used are shown below.

- Transmit queue interrupt is occurred when transmit queue became empty by tramsmit complete.
- Transmit queue interrupt is occurred each time one message trasmit is completed.

Also, transmit queue becomes occurance source of CANm transmit related interrupt. Occurance source of CANm transmit related interrupt are shown below.

- CANm transmit complete interrupt
- CANm transmit abort interrupt
- CANm transmit/receive FIFO transmit complete interrupt
- CANm transmit queue interrupt
- CANm transmit history interrupt

6.6 Transmit History Buffer Setting

Required settings for using transmit history buffer are shown below.

The transmit history buffer can store 8 transmit history data per channel.

- Storage target buffer setting
- Interrupt enable/disable and interrupt source settings

6.6.1 Storage Target Buffer Setting

Set target buffer for storing transmit history data to transmit history buffer. The target buffer to be stored can be selected below.

Also, you can set weather to store the transmit history data of the message when storing the transmit message.

- Entry from transmit/receive FIFO buffer and transmit queue.
- Entry from transmit buffer, transmit/receive FIFO buffer, and transmit queue.

6.6.2 Interrupt Enable/Disable and Interrupt Source Settings

Set transmit history interrupt enable/disable setting and interrupt source setting. Transmit history buffer interrupt sources are shown below.

- Transmit history interrupt is occurred when 6 data are stored to transmit history buffer.
- Transmit history interrupt is occurred each time a transmit history data storage is completed.

In addition, transmit history interrupt becomes occurrence source of CANm transmit interrupt. The occurrence sources of CANm transmit interrupt are shown below.

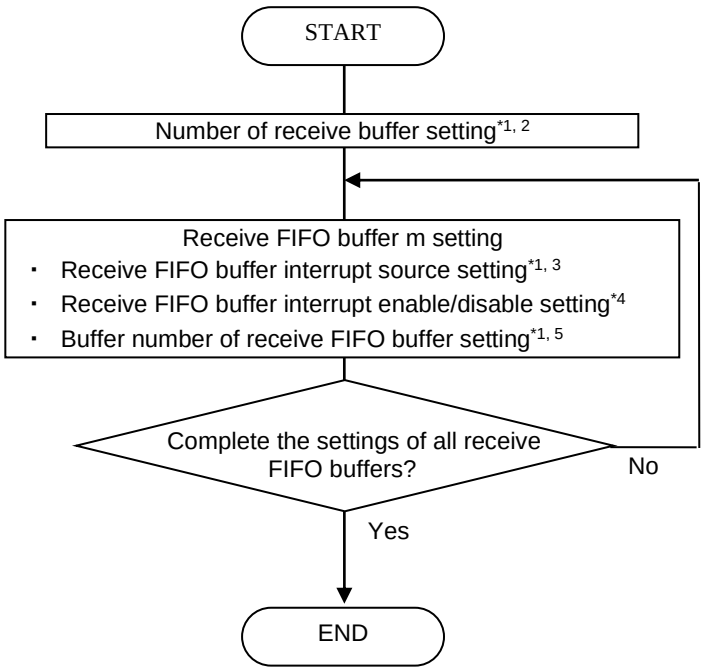
— CANm transmit complete interrupt
— CANm transmit abort interrupt
— CANm transmit/receive FIFO transmit complete interrupt
— CANm transmit queue interrupt
— CANm transmit history interrupt

6.7 Buffer Setting Procedures

Figure 6-2 shows receive buffer and receive FIFO buffer setting procedures. Figure 6-3 shows transmit FIFO buffer, transmit buffer, and transmit history buffer setting procedures.

Perform these settings during CAN configuration.

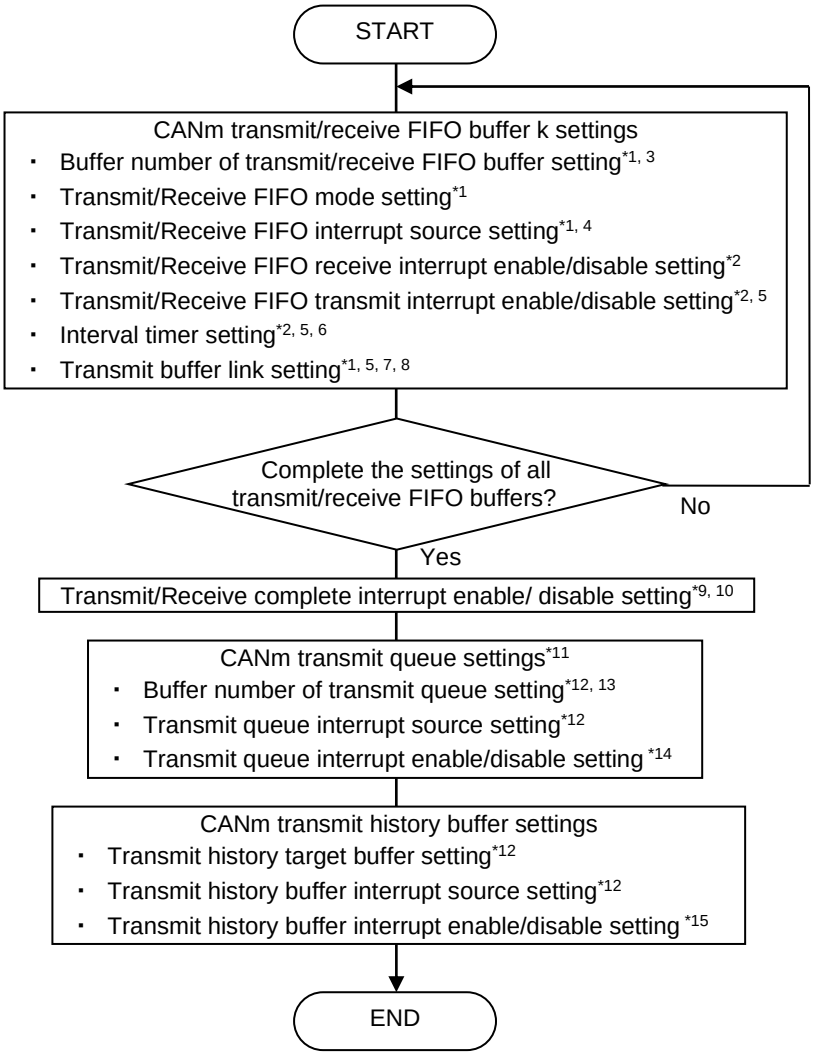
Please refer to “Section 1, CAN Configuration” for CAN configuration procedure.



【Note】 1. Rewrite the RMNB register, the RFIGCV[2:0] bit, the RFIM bit, and the RFDC[2:0] bit of the RFCCx register in the global reset mode.

2. The receive buffer cannot be used if number of receive buffer (NRXMB[7:0] bit of RMNB register) is set “0”. Also, set number of 0~16×channel.
3. If you set 4 messages (RFDC[2:0] bit is “B’001”) to the buffer number of the receive FIFO buffer, please set “B’001”, “B’011”, “B’101”, or “B’111” to RFIGCV[2:0] bit.
4. Perform the receive FIFO buffer enable/disable (RFIE bit of RFCCx register) settings in the state the receive FIFO buffer is not used (RFE bit of RFCCx register is “0”).
5. Do not use receive FIFO buffer if buffer number of receive FIFO buffer is set “0”(RFDC[2:0] bit is “B’000”).

Figure 6-2 Receive Buffer and Receive FIFO Buffer Setting Procedures



【Note】 1. Rewrite the CFDC[2:0] bit, the CFIM bit, the CFIGCV[2:0] bit, the CFM bit, and the CFTML[3:0] bit of the CFCCk register in the global reset mode.

2. Rewrite thr CFRXIE bit, the CFTXIE bit, the CFITR bit, the CFITSS bit, and the CFITT[7:0] bit of the CFCCk register in the state the transmit/receive FIFO buffer is not used (CFE bit of CFCCk register is “0”).
3. Set zero message (CFDC[2:0] bit is “B’000”) if the transmit/receive FIFO buffer is not used.
4. If you set four messages (CFDC[2:0] bit is “B’001”) to the buffer number of the transmit/receive FIFO buffer, please set “B’001”, “B’011”, “B’101”, or “B’111” to CFIGCV[2:0] bit.
5. Only set the transmit/receive FIFO buffers to the receive mode or the gateway mode are effective.
6. Set “0” to the message transmit interval (CFITT[7:] bit of CFCCk register) if the interval timer is not used.
7. Set the different values to the link (CFTML[3:0] bit) destination of the transmit/receive FIFO buffers (transmit mode, gateway mode★) in same channel .
8. Do not set assinged transmited buffer in the transmit queue as the link destination (CFTML[3:0] bit) to the transmit/receive FIFO buffer (transmit mode, gateway mode★).
9. Perform the transmit buffer interrupt enable/disable (TMIEp bit of TMIECy register) setting when the corresponded transmit buffer is no transmit request (TMTR flag of TMSTSp register is “0”).
10. Set “0” to the receive buffe linked with the transmit FIFO buffer and the TMIEp bit corresponded with assigned transmit buffer to transmit queue.
11. Select ID priority (TPRI bit of GCFG register is “0”) in the transmit priotity if the transmit queue is used.

12. Rewrite the TXQDC[3:0] bit and the TXQIM bit of the TXQCCm register, the THLDTE bit and the THLIM bit of the THLCCm register in the channel reset mode.
13. The transmit queue cannot be used if the buffer number of the transmit queue (TQDC[3:0] bit) is “0”. Also, do not set “1”.
14. Perform the transmit queue interrupt eanble/disabele (TQIE bit of TXQCCi register) settnig in the conditon transmit queue is not used (TQE bit is “0”).
15. Rewrite in the state transmit history buffer is not used(THLE bit of THLCCm register is “0”).

Figure 6-3 Transmit Buffer, Transmit/Receive FIFO Buffer, and Transmit History Buffer Setting Procedures

7. Global Error Interrupt

Set global error interrupt. When corresponded interrupt enable bit is enabled, interrupt request is outputted from CAN module. Occurrence of interrupts also depends on the interrupt control register settings of the interrupt controller.

7.1 Global Error Interrupt Setting

Occurrence sources of global error interrupt are shown below.

- DLC check error
- FIFO message lost
- Transmit history buffer overflow
- Payload overflow

7.1.1 DLC Check Error

When DLC check is enabled, the DLC check error is detected in case DLC of message in DLC check after passing acceptance filtering process is smaller than DLC of transmit rule.

7.1.2 FIFO Message Lost

The FIFO message lost is detected in case the state transmit/receive FIFO buffer is full and attempting to store new message to FIFO.

7.1.3 Transmit History Buffer Overflow

The transmit history buffer overflow is detected in case history buffer is full and attempting to store new transmit history data to transmit history buffer.

7.1.4 Payload Overflow

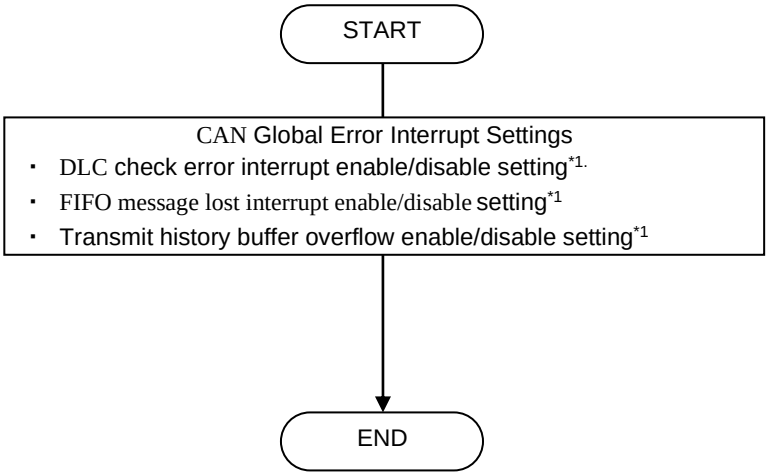
The payload overflow is detected in case payload length of received message exceeds payload storage size of storage destination buffer.

7.2 Global Error Interrupt Setting Procedure

Figure 7-1 shows global error interrupt setting procedure.

Please perform these settings during CAN configuration.

Please refer to “Section 1, CAN Configuration” for CAN configuration procedure.



【Note】 1. Rewrite the THLEIE bit, the MEIE bit, and the DEIE bit of the GCTR register in the global reset mode.

Figure 7-1 Global Error Interrupt Setting

8. Channel Function

Set the following functions for each channel.

- Channel error interrupt setting
- Transmit abort interrupt setting
- Bus off recovery mode setting
- Error display mode setting
- Communication test mode setting

8.1 CANm Error Interrupt

Set CANm error interrupt enable/disable. The occurrence sources of channel error interrupt are shown below.

- Bus error
- Error warning
- Error passive
- Bus off entry
- Bus off recovery
- Overload frame
- Bus lock
- Arbitration lost

8.1.1 Bus Error

Interrupt is occurred in case any one of the following is detected.

— A form error is detected in the ACK delimiter (ADERR flag of CmERFLL register is “1”).
— A recessive is detected even though a dominant is transmitted (B0ERR flag of CmERFLL register is “1”).
— A dominant is detected even though a recessive is transmitted (B1ERR flag of CmERFLL register is “1”)
— A CRC error is detected (CERR flag of CmERFLL register is “1”).
— An ACK error is detected (AERR flag of CmERFLL register is “1”).
— A form error is detected (FERR flag of CmERFLL register is “1”).
— A stuff error is detected (SERR flag of CmERFLL register is “1”)
.

8.1.2 Error Warning

The interrupt is occurred in case an error warning state (receive error counter or transmit error counter >95) is detected. The interrupt is occurred when only the receive error counter or transmit error counter first exceeds 95.

8.1.3 Error Passive

The interrupt is occurred in case an error passive state (receive error counter or transmit error counter >127) is detected. The interrupt is occurred when only the receive error counter or transmit error counter first exceeds 127.

8.1.4 Bus Off Entry

The interrupt is occurred in case a bus off state (transmit error counter >225) is detected.

The interrupt is also occurred in case the bus off recovery mode setting became the bus off state by the transition to channel halt mode (BOM[1:0] bit of CmCTR register is “b’01”) in bus off state.

8.1.5 Bus Off Recovery

The interrupt is occurred in case an 11 bit consecutive recessive is detected 128 times and the recovery from the buss off state is detected. Please refer to “Section 8.3, Buss Off Recovery Mode Setting” for detail.

8.1.6 Overload frame transmit

The interrupt is occurred in case transmit condition of overload frame is detected when receiving or transmitting.

8.1.7 Bus Lock

The interrupt is occurred in case a bus lock is detected.

It is judged as a bus lock when a 32 bit consecutive dominant is detected on the CAN bus in channel communication mode.

8.1.8 Arbitration Lost transmit/receive

The interrupt is occurred in case an arbitration lost is detected.

8.2 CANm Transmit Abort Interrupt

Set the transmit abort interrupt enable/disable. The interrupt is occurred when transmit abort complete has been detected in case the transmit abort interrupt is enabled.

Also, the transmit abort interrupt becomes occurrence sources of CANm transmit interrupt. The occurrence sources of the CANm transmit interrupt are shown below.

- CANm transmit coplete interrupt
- CANm transmit abort interrupt
- CANm transmit/receive FIFO transmit complete interrupt
- CANm transmit queue interrupt
- CANm transmit history inetrrupt

8.3 Bus Off Recovery Mode Setting

Set the operation when recovering bus off. Table 8-1, and Figure 8-1 ~ Figure 8-4 show the operation of each bus off recovery mode.

Table 8-1 The Operation When Recovering Bus Off

CmCTR BOM[1:0] Bit	Function	Bus Off Entry Interrupt	Bus Off Recovery Interrupt*1
B’00	ISO11898-1 compliant	Occur	Occur*2
B’01	Transitions to channel halt mode automatically at bus-off entry*3, 4	Occur	Not occur
B’10	Transitions to channel halt mode automatically at bus-off end*3, 4	Occur	Occur
B'11	Transitions to channel halt mode (in bus-off state) by program request	Occur	Occur*5

【Note】 1. When transitioning to channel reset mode before detecting an 11 bit recessive 128 times (Set “B’01” to CHMDC[1:0] bit of CmCTR register), the interrupt is not occurred in case.

2. When transitioned to channel halt mode (CHMDC[1:0] is “B’01”) before detecting a 11 bit consecutive recessive 128 times, it is not transmitted to channel halt mode until a 11 bit consecutive recessive is detected 128 times. Also, the interrupt is not occurred in case of recovering from bus off forcibly.
3. If the channel transitions to channel halt mode by the CAN module simultaneously when the program writes a value to the CHMDC[1:0] bits, writing by the program takes precedence.
4. An automatic transition to channel halt mode is made only in channel communication mode (CHMDC[1:0] bit is “B’00”).
5. When transitioned to channel halt mode by program request before detecting a 11 bit con recessive 128 times during bas off, the interrupt is not occurred.

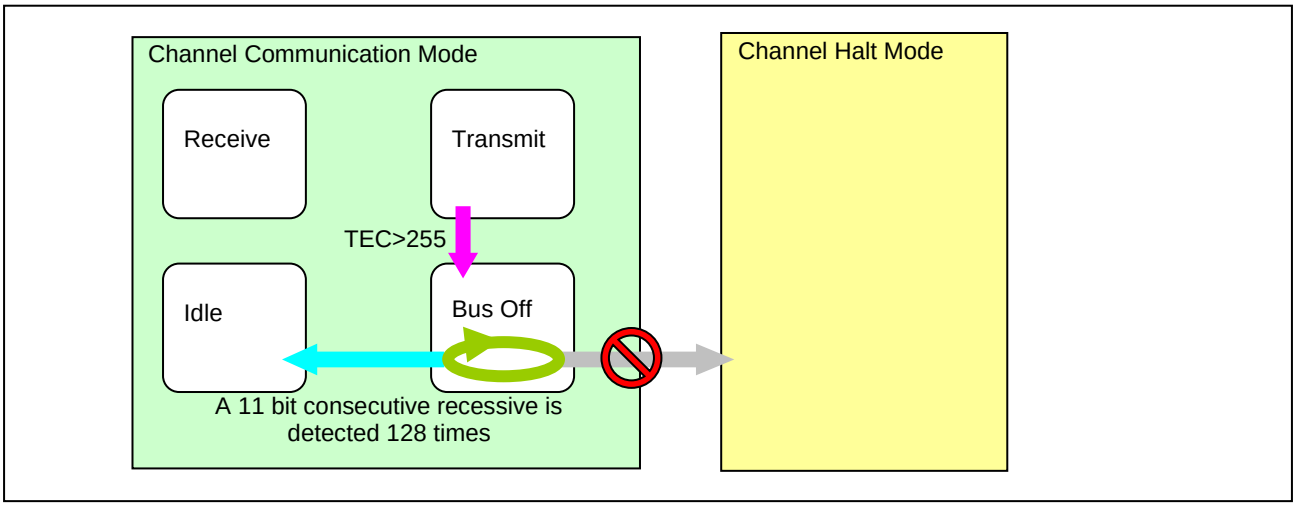


Figure 8-1 The operation when compliant ISO11898-1 (BOM[1:0] bit is B' 00)

D

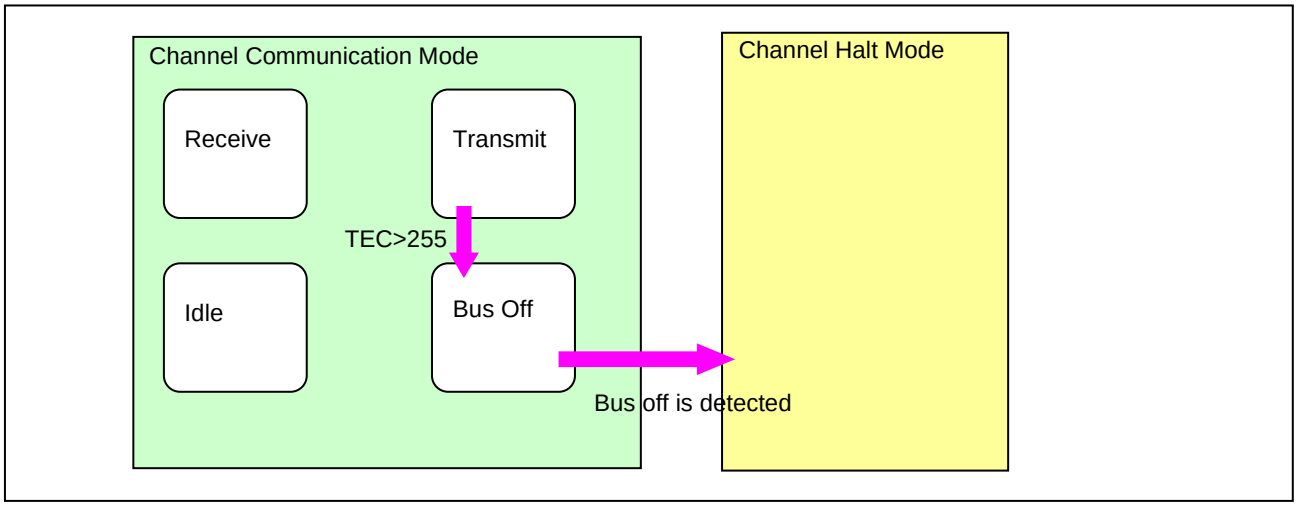


Figure 8-2 The operation when transitioning to channel halt mode at bus off entry (BOM[1:0] bit is B' 01)

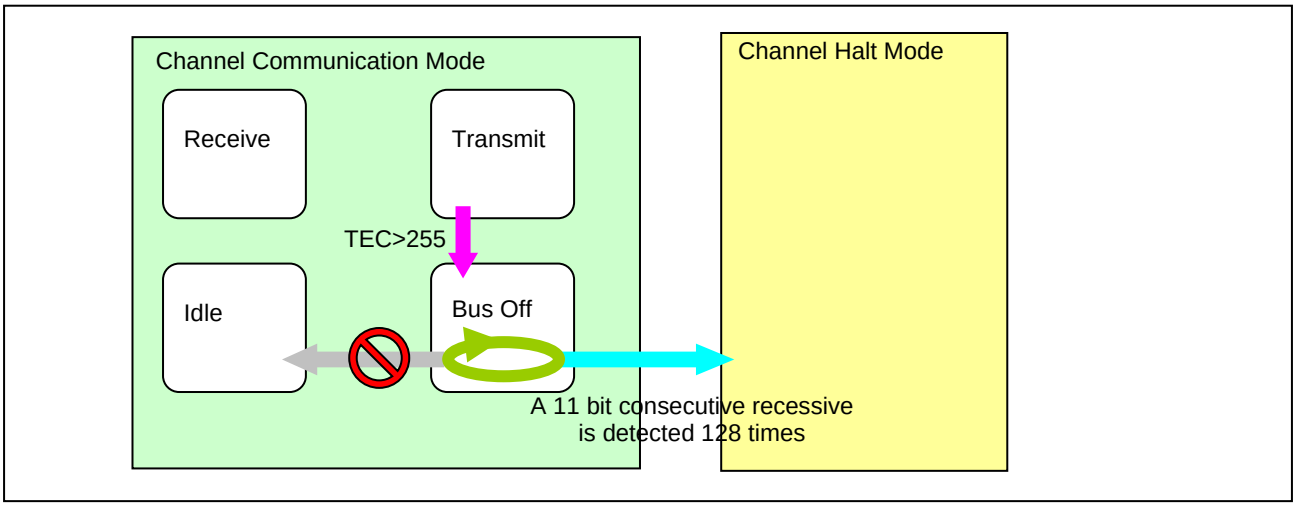


Figure 8-3 The operation when transitioning to channel halt mode at bus off end (BOM[1:0] bit is B' 01)

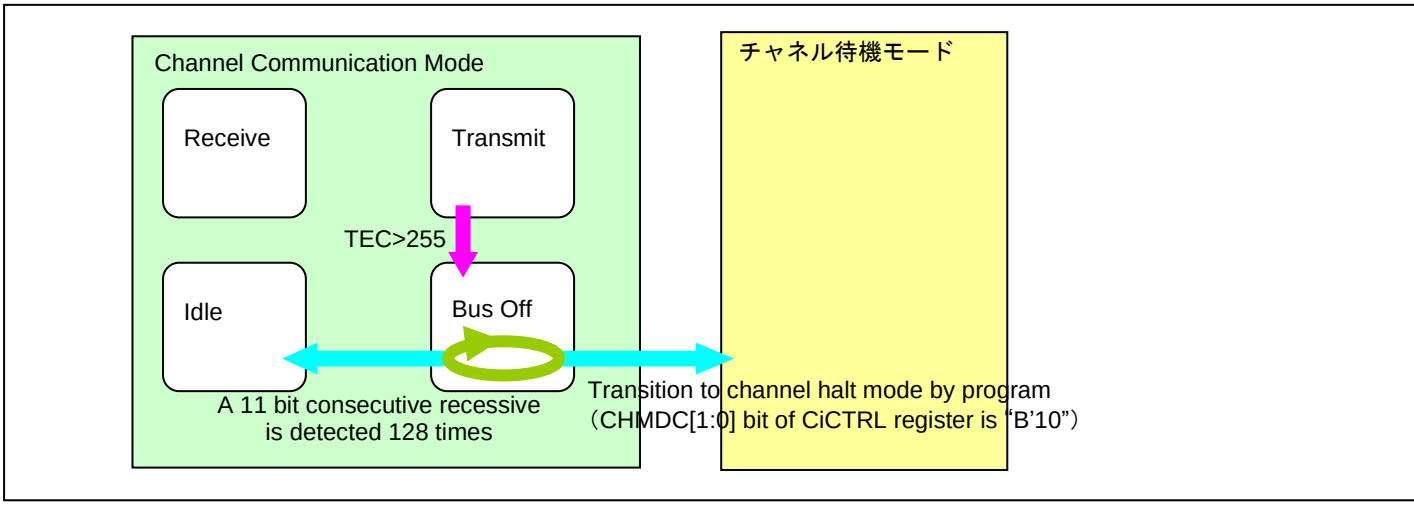


Figure 8-4 The operation when transitioning to channel halt mode by program request at bas off (BOM[1:0] bit is B' 11)

8.4 Error Display Mode Setting

When CAN bus error is occurred, set bit 14~8 display mode of CmERFLL register. The display mode enabled to set is shown below.

Display only the first occurred error information (ERRD bit of CmCTR register = “0”).

- The first occurred error flag only become “1”. When several errors are occurred at the same time, the flag of the detected several error will be “1”.
- Display all of the occurred error information. (ERRD bit = “1”).
  Regardless of the order of occurrence, all the flags of the errors that occur will be "1".

Figure 8-5 shows the operation example of CMERFLL register in each error display mode.

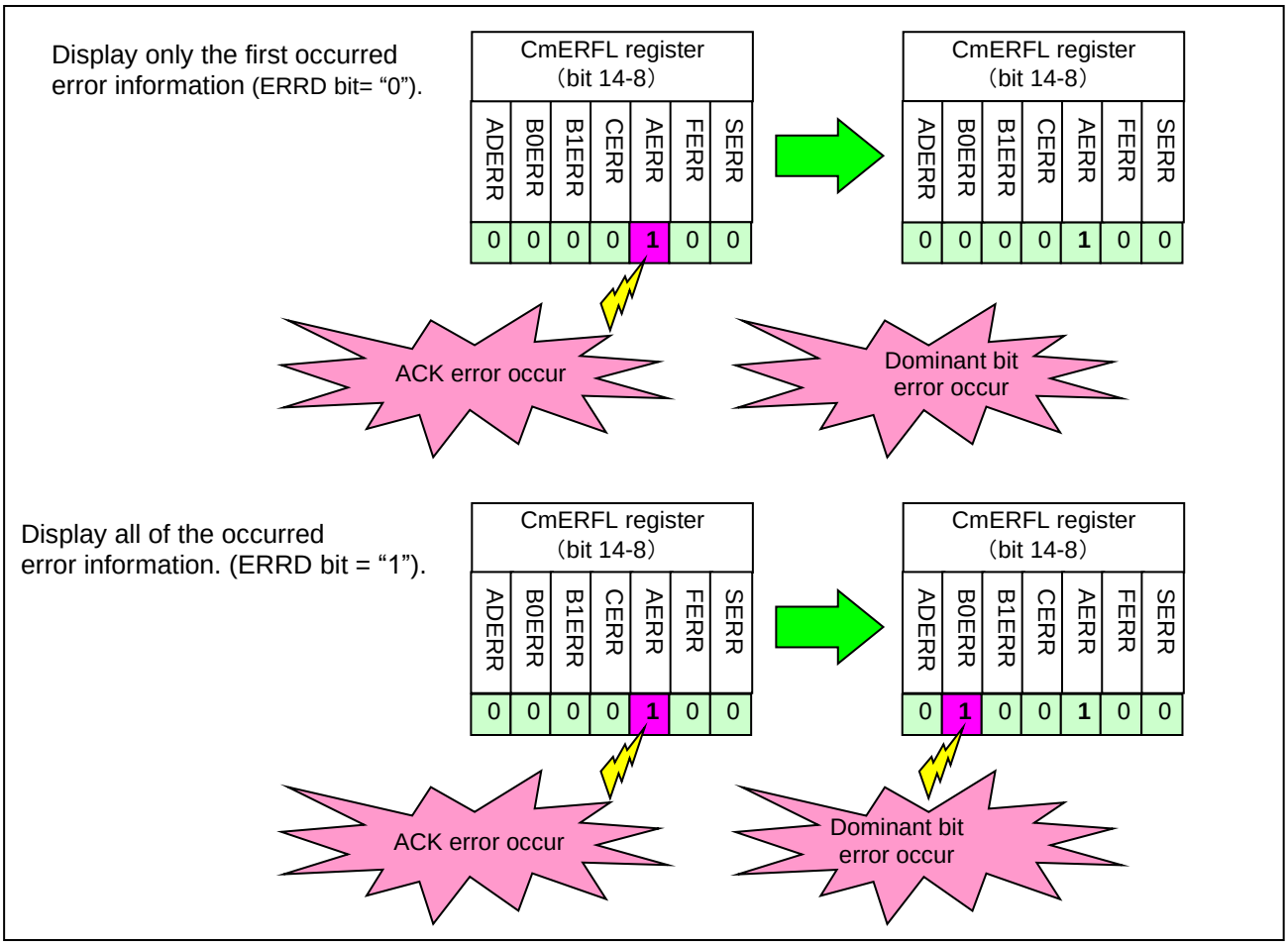


Figure 8-5 Operation Example of Error Display Mode

8.5 Communication Test Mode Setting

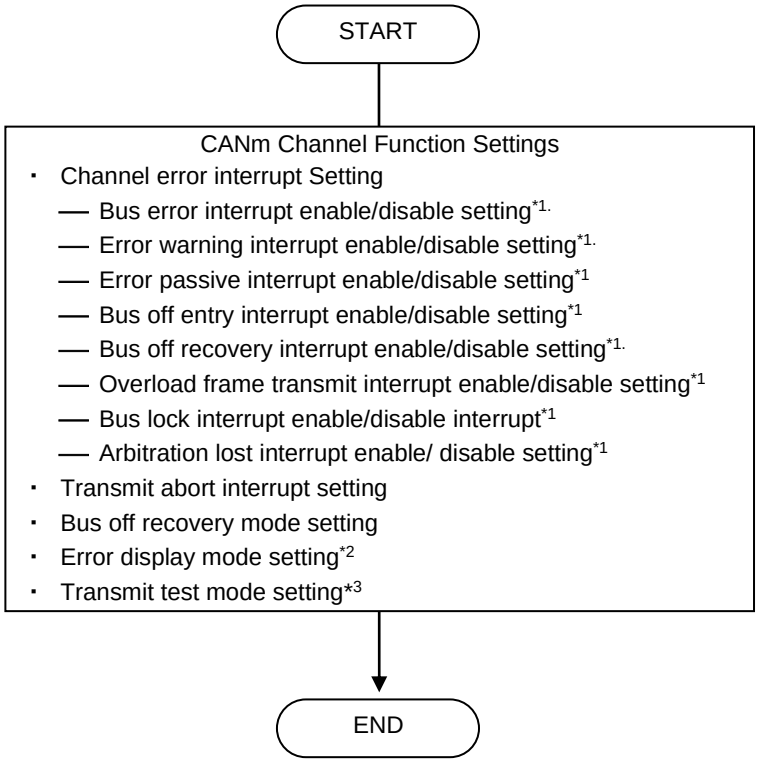
Set communication test mode. Please refer to “ Test Mode Procedure Application Note” for the communication test mode.

8.6 Channel Function Setting Procedure

Figure 8-6 shows the channel function procedure.

Please perform these settings during CAN configuration.

Refer to “Section 1, CAN Configuration” for procedure of CAN configuration.



【Note】 1. Rewrite the BEIE bit, the EWIE bit, the EPIE bit, the BOEIE bit, the BORIE bit, the OLIE bit, the BLIE bit, the ALIE bit, and the TAIE bit of the CmCTR register in the channel reset mode.

2. Rewrite the ERRD bit of the CmCTR register in the channel reset mode or the channel halt mode.

3. Rewrite the CTMS bit and the CTME bit of the CmCTR register in the channel halt mode. It becomes “0” in the channel reset mode.

Figure 8-6 Channel Function Setting Procedure

9. CAN-related Interrupt

Set the corresponding EI level interrupt control register (EIC register) for the CAN-related interrupt enable/disable.

The available CAN-related interrupts are shown below.

- Global receive FIFO interrupt
- Global error interrupt
- CANm transmit interrupt
- CANm transmit/receive FIFO receive complete interrupt
- CANm error interrupt
- CANm wakeup interrupt

Table 9-1 CAN-related Interrupt and Occurrence Source

Interrupt	Occurrence Source
Global receive FIFO interrupt	Receive FIFO buffer interrupt request generation
Global error interrupt	DLC check error
	FIFO message lost
	Transmit history buffer overflow
CANm transmit interrupt	CANm transmit complete interrupt request generation
	CANm transmit abort interrupt request generation
	CANm transmit/receive FIFO transmit complete interrupt request generation
	CANm transmit queue interrupt request generation
	CANm transmit history interrupt request generation
CANm transmit/receive FIFO complete interrupt	Channel m transmit/receive FIFO receive complete interrupt request generation
CANm error interrupt	Bus error
	Error warning
	Error passive
	Bus-off entry
	Bus-off end
	Overload flame transmit
	Bus lock
	Arbitration lost
	Transmitter Delay Compensation violation
CANm wakeup interrupt*1	CAN bus dominant edge detection

【Note】 1. The external INT interrupt is used.

9.1 CAN-related Interrupt Setting Procedure

Figure 9-1 shows the interrupt setting procedure.

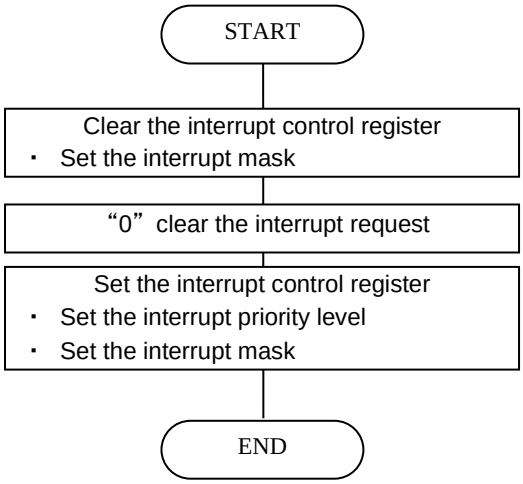


Figure 9-1 Interrupt Setting Procedure

10. Transmitter Delay Compensation (Only in CAN FD Mode)

A high baud rate is used in the data phase in CAN FD mode. Transmitter delay compensation is provided as a function to accept propagation delay in this case.

To use this function, set the TDCE bit in the FDCFG register to 1. Also set the secondary sample point (SSP) timing used in the data phase by the TDCOC bit and TDCO[6:0] bits in the FDCFG register.

When the TDCOC bit is 0, the SSP timing equals the total value of the delay measured by the RS-CANFD module and the TDCO[6:0] value. (This value is rounded off to the nearest integer of Tq.) Usually, the TDCO[6:0] value must be equal to SS + TSEG1, the sample point timing.

Figure 10-1 shows the SSP timing.

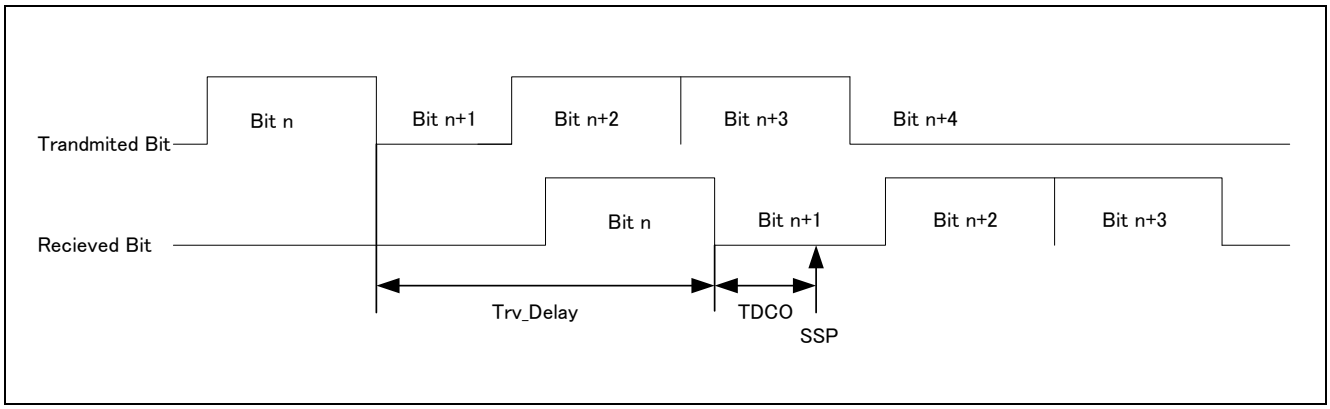


Figure 10-1 SSP Timing

When the TDCOC bit is “1”, the SSP timing is determined only by the TDCO[6:0] value. (When the DBRP[7:0] value in the DCFG register is larger than “0”, the TDCO[6:0] value is also rounded off to the nearest integer of Tq.) The SSP offset value becomes the set values of the TDCO[6:0] bit +1.

The RS-CANFD module compensates a delay up to 3 CANm bit time (2 fCAN). (CANm bit time is the value of data bit rate.)

The TDCR[6:0] flag in the FDSTS register is the bit that indicates the transmitter delay compensation result as a multiple of CAN clock frequency (fCAN). This result depends on the settings of the TDCOC bit and TDCO[6:0] bits in the FDCFG register. These flags are updated at a falling edge between the FDF bit and res bit when the TDCE bit in the FDCFG register is set to “1”(transmitter delay compensation enable) and also the TDCOC bit in the FDCFG register is set to “0” (measurement and offset).

The TDCVF bit in the FDSTS register indicates violation of transmitter delay compensation. The transmit data is compared with the reception CAN bus level delayed due to the transceiver’s loop delay. This delay changes due to physical factors such as temperature. Because the TDCR[6:0] flags are updated for each message, temporary maximum delay cannot be confirmed. This bit is set to “1” when the transmitter delay compensation exceeds the maximum compensation 3 CANm bit times (2fCAN). (CANm bit time is the value of data bit rate)

11. Precautions for Processing Flow

11.1 About Functions

In this application note, there is a part that is functionalized even in the processing of single line, but this is only described as a function to clarify the processing for each function. When you actually create a program, you don't necessarily have to make it functional.

11.2 Setting for Each Channel

In this application note, even if processing is required for each channel, only processing for one channel is described. When actually creating a program, perform the processes for multiple channels as necessary.

11.3 Infinite Loop

To simplify the notation, there are some infinite loops in the processing flow. When actually creating a program, give each loop a time limit so that it can be exited during overtime. Figure 11-1 shows an example of processing when the loop time limit is set. Table 11-1 and Table 11-2 shows the maximum transition time to individual modes

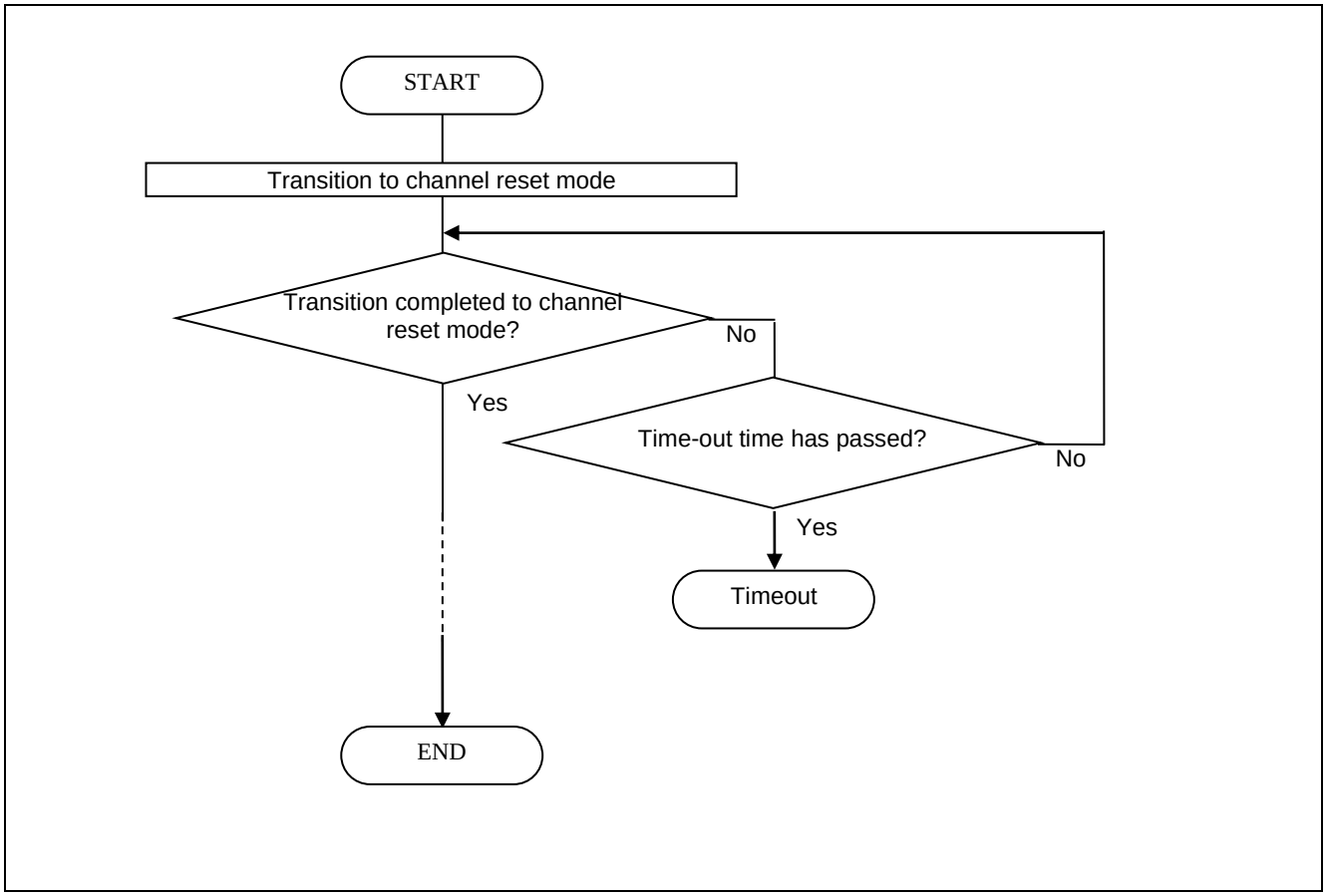


Figure 11-1 Example of Processing with Loop Time Limit

Table 11-1 Transition Time in Global Mode

Mode before transition	Mode after transition	Maximum transition time
Global stop	Global reset	3 clocks of pclk
Global reset	Global stop	3 clocks of pclk
Global reset	Global test	10 clocks of pclk
Global reset	Global operation	10 clocks of pclk
Global test	Global reset	2CAN bit time*1, 2
Global test	Global operation	3 clocks of pclk
Global operation	Global reset	2CAN bit time*1, 2
Global operation	Global test	2CANframes*1

【Note】 1. It is the CAN bit time and CAN frame time of the slowest communication speed among the channels used.

2. In CAN FD mode, the normal bit rate is CAN bit time.

Table 11-2 Transition Time in Channel Mode

Mode before transition	Mode after transition	Maximum transition time
Channel Stop	Channel reset	3 clocks of pclk
Channel reset	Channel Stop	3 clocks of pclk
Channel reset	Channel halt	3CANm bit time*1
Channel reset	Channel communication	4CANm bit time*1
Channel halt	Channel reset	2CANm bit time*1
Channel halt	Channel communication	4CANm bit time*1
Channel communication	Channel reset	3CANm bit time*1
Channel communication	Channel halt	2 CANm frames

【Note】 1. In CAN FD mode, the normal bit rate is CANm bit time.

12. Appendix

12.1 Performed CAN Configuration Processing in Individual States

Table 12-1 shows performed CAN configuration processing in individual states

Table 12-1 formed CAN Configuration Processing in Individual States

Processing		CAN Configuration*1			
		After MCU reset	After global reset mode	After channel reset mode	After channel halt mode
CAN state (mode) transition	Global mode trasition	○	○	—	—
	Channel mode transition	○	○	○	○
Global function setting	Transmit priority setting	○	△	—	—
	DLC check setting				
	DLC replacemt function setting				
	Mirror function setting				
	Clock setting				
	Timestamp clock setting				
	Interval timer prescaler setting				
Communication speed setting	Bit timing setting	○	△	△	△
	Communication speed setting				
Receive rulr table setting		○	△	—	—
Buffer setting	Receive buffer setting	○	△	—	—
	Receive FIFO buffer setting				
	Transmit/Receive FIFO buffer setting			△注2	△注2
	Transmit buffer setting			△	△
	Transmit queue setting				
	Transmit history buffer setting				
Global error interrupt setting		○	△	—	—
Channel function setting		○	△	△	△

【注】 1. ○：Setting required, ー：Cannot be set, △：No setting required
2. Rewrite the following bits in global reset mode.
CFTML[3:0] bit ,CFM[1:0] bit, CFIGCV[2:0] bit, CFIM bit, CFE bit in CFCCLk,Hk register

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Revision History

Rev.	Date	Description	
		Page	Summary
1.0	2017.5.10	-	Initial edition

Precautions for use of the product

This section describes the "Precautions" that apply to all microcontroller products. Please refer to this document and the Technical Update for precautions on individual products.

1. Treatment of unused pins

   [Caution] Please dispose of unused pins according to "Handling of unused pins" in the text.

   The impedance of the input pins of CMOS products is generally high impedance. If the unused pins are operated in an open state, noise around the LSI may be applied due to the induction phenomenon, a through current may flow inside the LSI, or it may be recognized as an input signal and malfunction may occur. Dispose of unused pins according to the instructions given in "Disposal of unused pins" in the text.

2. Treatment at power-on

   [Caution] The state of the product is undefined when the power is turned on.

   When the power is turned on, the state of the internal circuits of the LSI is indeterminate and the state of register settings and pins is undefined.

   For products that are reset using the external reset pin, the pin state cannot be guaranteed from the time the power is supplied until the reset becomes valid.

   Similarly, in the case of products that are reset using the built-in power-on reset function, the pin states cannot be guaranteed from the time the power is turned on until the voltage reaches a certain level.

3. Prohibition of Access to Reserved Addresses

   [Caution] Access to reserved addresses is prohibited.

   The address area has a reserved address allocated for future function expansion. The operation when these addresses are accessed cannot be guaranteed, so do not access them.

4. About clock

   [Caution] When resetting, release the reset after the clock has stabilized.

   When switching the clock during program execution, switch the clock after the switching destination clock is stable.

   In a system that starts operating with a clock that uses an external oscillator (or external oscillator circuit) at reset, release the reset after the clock is sufficiently stable. Also, when switching to a clock that uses an external oscillator (or external oscillator circuit) in the middle of a program, make sure that the clock to be switched to is sufficiently stable before switching.

5. Differences between products

   [Caution] When changing to a product with a different model name, perform a system evaluation test for each product model name.

   Even if the MCUs in the same group have different model numbers, the characteristic values, operating margins, noise immunity, noise radiation, etc. may differ within the range of electrical characteristics due to differences in internal ROM and layout patterns. When changing to a product with a different model name, perform a system evaluation test for each individual product.

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