RENESAS

RL78/F13, F14

Port setting procedures

Introduction

This application note describes the procedures for setting port-related registers of the RL78/F13 and the RL78/F14 microcontrollers.

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RENESAS

1.   Overview of port settings

   This application note describes the procedures for setting the port-related registers when each port is used as an analog input pin, digital I/O pin or peripheral function pin.

   Table 1 lists the port-related registers used for setting each port.

   Note that the register set values, the timing of setting the port-related registers, and the cpu instructions to be used depend on the user's specifications. Therefore, determine these according to the specifications of each user based on this application note.

<div align="center">Table 1 List of port-related registers</div>

Register name NOTE 1	Register specifications
Port mode register (PMxx)	Specifies a mode (input or output) for the port.
Port register (Pxx)	Sets the output latch value for the port when configured as an output. When the port is configured as an input (also, when the port is set to output mode [PMS.PMS0 = 1]), the pin level is read.
Pull-up resistor option register (PUxx)	Specifies whether to use the on-chip pull-up resistor. With the pin P40, the on-chip pull-up resistor will be enabled after reset.
Port input mode register (PIMx)	Sets the input buffer to "normal input" or "TTL input".
Port output mode register (POMx)	Sets the output mode to "normal output mode" or "N-ch open-drain output".
Port mode control register (PMCx) NOTE 2	Sets the corresponding pin to analog input or digital I/O.
A/D port configuration register (ADPC)	Sets the corresponding pin to analog input or digital I/O.
Peripheral I/O redirection register (PIORx)	Specifies which I/O port of a peripheral function is assigned to each input pin.
Port input threshold control register (PITHLx)	Selects a threshold to be input (Schmitt1 or Schmitt3).
Port output slew rate select register (PSRSEL)	Sets the port output slew rate to "normal" or "special (slower than the normal slew rate)".
SNOOZE status output control register (PSNZCNTx)	Selects a pin that outputs a signal indicating that SNOOZE mode has been entered through an external pin.
Port mode select register (PMS)	When the port is set to output mode (PMxx.PMmn=0), enables reading of output levels of pins.
STOP status output control register (STPSTC)	Enables/disables STOPST output when STOP mode is released.

NOTE 1: This application note is prepared on the assumption that the port-related registers are set by using MOV instructions. Also, some MCUs may not be provided with those registers/bits indicated in this application note. Therefore, with such products, do not attempt to access such registers. In addition, for the registers that have bits with no function, set a bit value after reset.

NOTE 2: With the following products having the PMC7 register, set 0 in the corresponding bits.

·   With the RL78/F14 MCU (the number of pins is 64 and the size of code flash memory is from 128 Kbytes to 256Kbytes): Set 0 in the PMC74 to PMC71 bits.

·   With the RL78/F14 MCU (the number of pins is 48 and the size of code flash memory is from 128 Kbytes to 256 Kbytes): Set 0 in the PMC73 bit.

2.   Procedure for setting port-related registers

In this chapter, the procedure for setting port-related registers when each pin is used as an analog input port or a digital I/O port is described in **Section 2.1** and the procedure for setting port-related registers where a peripheral function is used is described in **Section 2.2**.

2.1   Procedures for setting registers related to analog input ports and digital I/O ports

2.1.1   Setting procedure when analog input ports are selected

The setting procedure when the pin P70 is used as an analog input port is illustrated in **Figure 1**.
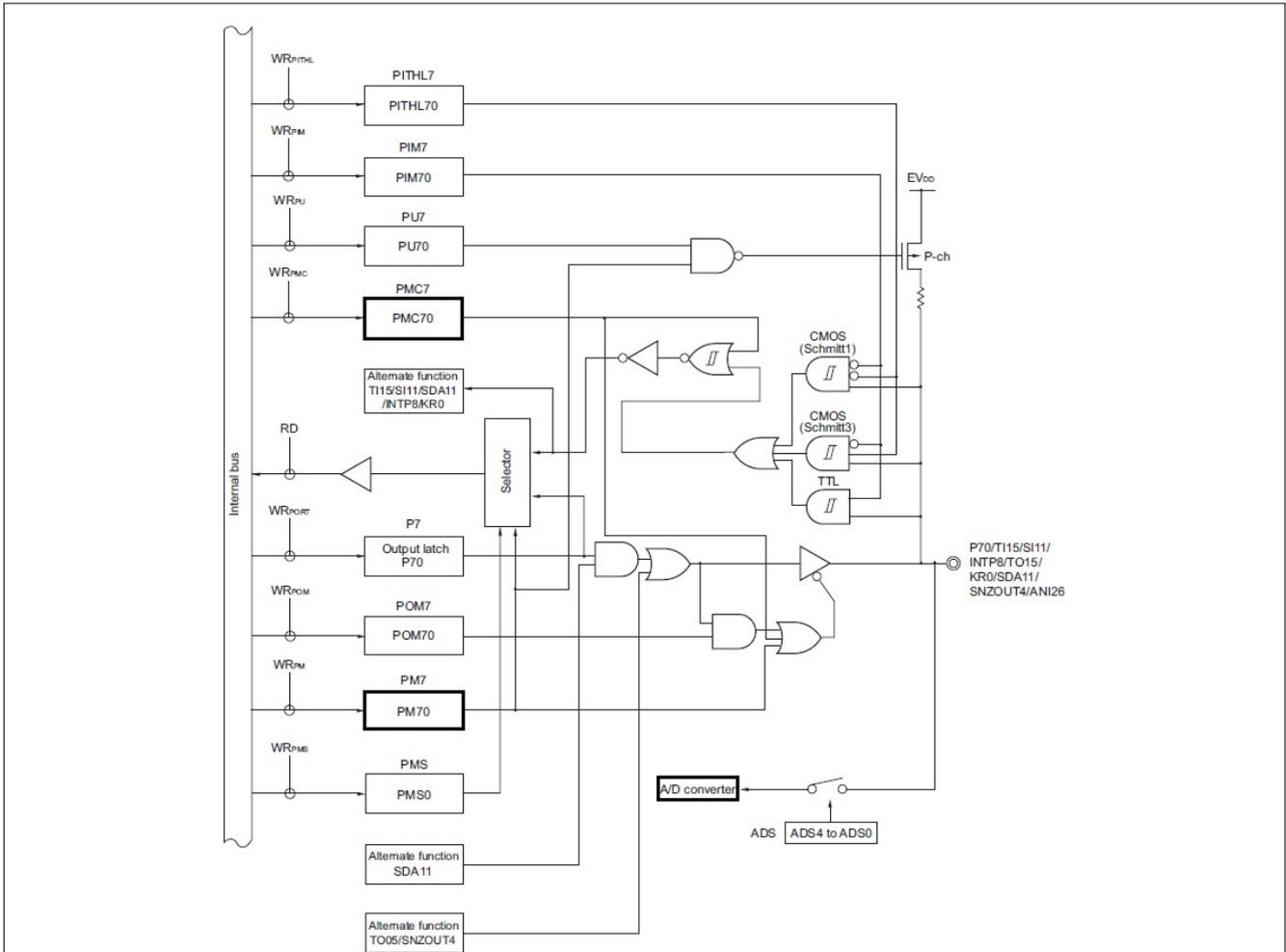
Step	Register	Register setting
1	PIORxx	Do not allocate the following peripheral functions to the corresponding pin (P70).
		·Input function (KR0/TI15/INTP8/SI11/SDA11)
		·Output function (TO15/SDA11/SNZOUT4)
		When analog input pins are used, the digital I/O function is not available.
2	ADPC/PMCx **NOTE**	Set the corresponding pin (P70) to analog input. (PMC70 = 1)
3	PMxx	Set the corresponding pin (P70) to input mode. (PM70 = 1)
4	Pxx	Setting not required
5	PUxx	Setting not required (On-chip pull-up resistors are disabled.)
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required

NOTE: Although the corresponding pin (P70) is provided with these registers, some other pins may not be provided with these registers. In that case, the settings to these registers are unnecessary.

Figure 1 Setting example of analog input port (P70/ANI26)

2.1.2 Procedure for setting port-related registers when digital input ports are selected

The setting procedure when the pin P70 is used as a digital input port is illustrated and described in **Figure 2**.

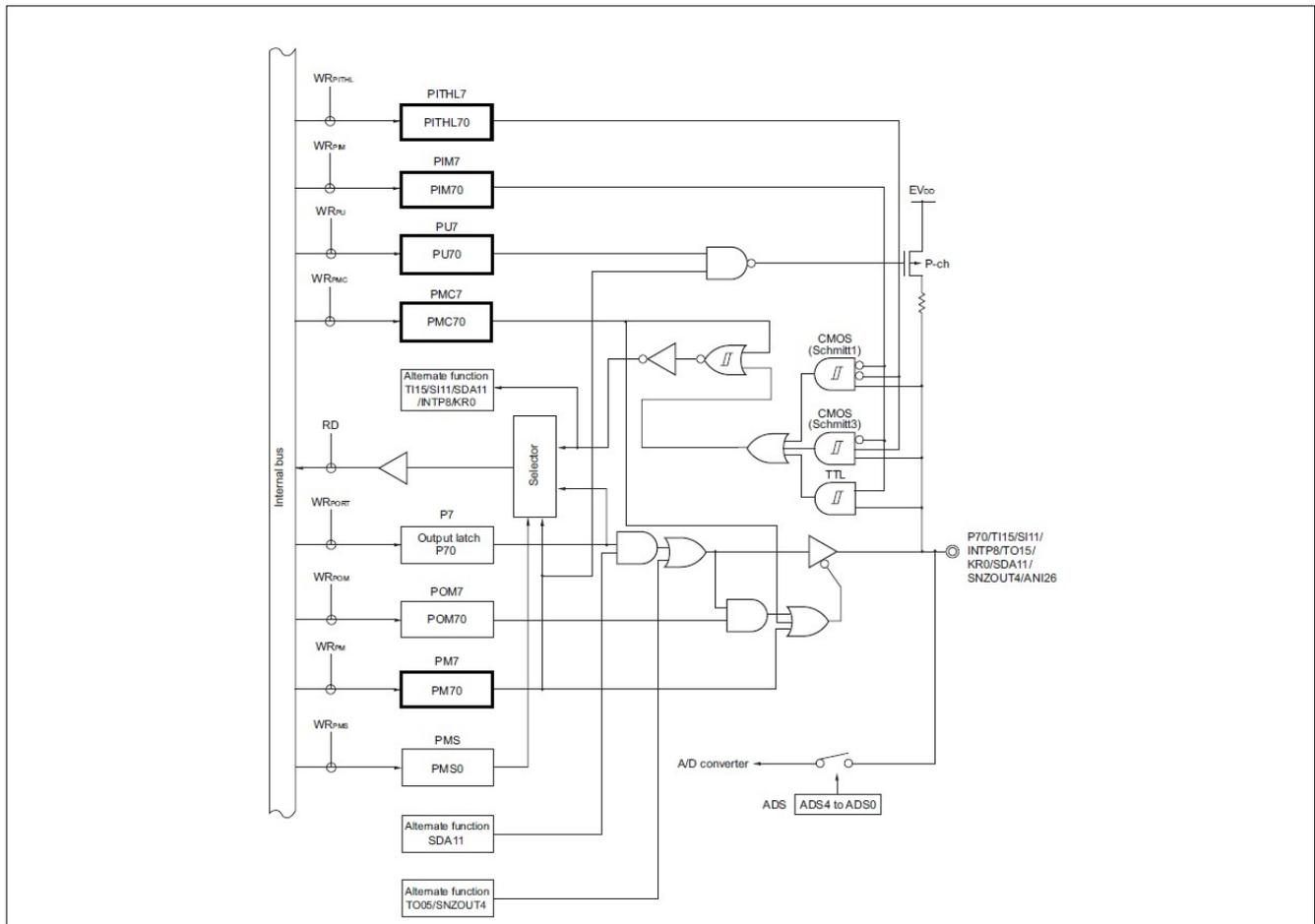| Step	Register	Register setting
1	PIORx	Do not allocate the following peripheral functions to the corresponding pins (P70). · Input function (KR0/TI15/INTP8/SI11/SDA11) Do not activate the corresponding peripheral functions. · Output function (TO15/SDA11/SNZOUT4) The corresponding peripheral functions are not available.
2	ADPC/PMCx **NOTE**	Set the corresponding pin (P70) to digital I/O. (PMC70 = 0)
3	PMxx	Set the corresponding pin (P70) to input mode. (PM70 = 1)
4	Pxx	Setting not required
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Settable (Set the input mode to normal input or TTL input.)
7	POMx	Setting not required
8	PITHLx	Settable [Set a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required

NOTE: Although the corresponding pin (P70) is provided with these registers, some other pins may not be provided with these registers. In that case, the settings to these registers are unnecessary.

Figure 2 Setting example of digital input port (P70)

2.1.3   Procedure for setting the port-related registers when digital output ports are selected

The setting procedure when the pin P70 is used as a digital output port is illustrated and described in **Figure 3**.

When the pin is used as a digital output port, output of the peripheral functions allocated to the pin must be disabled. **Table 2** shows the settings of the peripheral function registers to disable the output of the peripheral functions.

Step	Register	Register setting
1	PIORx	Do not allocate the following peripheral functions to the corresponding pin (P70).
		· Input function (KR0/TI15/INTP8/SI11/SDA11)
		Do not activate the corresponding peripheral functions.
		· Output function (TO15/SDA11/SNZOUT4)
		The corresponding peripheral functions are not available. (Disable the output from the peripheral functions. See **Table 2**.)
2	ADPC/PMCx NOTE 1	Set the corresponding pin (P70) to digital I/O. (PMC70 = 0)
3	Pxx	Set the output latch value.
4	PMxx	Set the corresponding pin (P70) to output mode. (PM70 = 0)
5	PUxx	Setting not required (On-chip pull-up resistors are disabled.)
6	PIMx	Setting not required
7	POMx	Settable (normal output/N-ch open drain output)
8	PITHLx	Setting not required
9	PSRSEL NOTE 2	Setting not required
10	PSNZCNTx NOTE 1	Set the corresponding pin (P70) to disable SNOOZE status output. (OUTEN4 = 0)
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.

NOTE 1: Although the corresponding pin (P70) is provided with these registers, some other pins may not be provided with these registers. In that case, the settings to these registers are unnecessary.

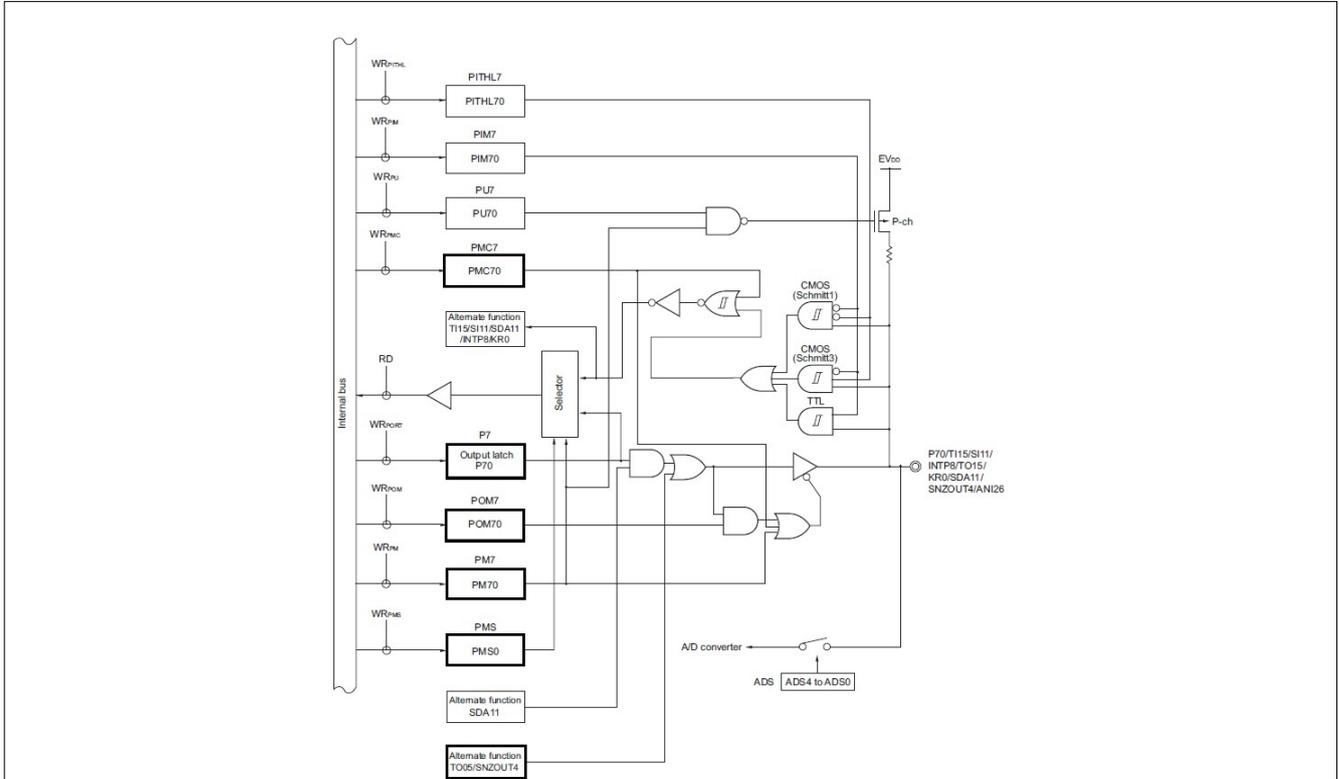**NOTE 2**: Although the corresponding pin (P70) is not provided with these registers, some other pins may be provided with these resisters. In that case, set the registers according to your specifications.

Figure 3 Setting example of digital output port (P70)

Table 2 Settings of each peripheral function when digital output ports are selected NOTE

Output pin of peripheral functions	Functions	Peripheral function settings
TOmn	Timer array unit output	TOm.TOmn = 0, TOEm.TOEmn = 0
TRJIO0	Timer RJ output	Other than "TRJMR0.TMOD[2:0] = 001B"
TRJO0	Timer RJ output	TRJIOC0.TOENA = 0
TRDIOAi, TRDIOBi, TRDIOCi, RDIODi	Timer RD output	TRDOER1.[b7:b0] = 1
TxDq, SDAr, SOp	Serial array unit (output)	SOm.SOmn = 1, SOEm.SOEmn = 0, SEm.SEmn = 0
SCKp, SCLr	Serial array unit (output)	SOm.CKOmn = 1, SOEm.SOEmn = 0, SEm.SEmn = 0
SCLA0, SDAA0	Clock/serial data output for IICA0	PER0.IICA0EN = 0
CTXD0	Serial data output from CAN	PER2.CAN0EN = 0
LTXD0, LTXD1	Serial data output from LIN	PER2.LINnEN = 0
PCLBUZ0	Clock output/buzzer output	CKS0.PCLOE0 = 0
RTC1HZ	Real-time clock correction clock output	RTCC0.RCLOE1 = 0
STOPST	STOP status output	STPSTC.STPOEN = 0
SNZOUTn	SNOOZE status output	PSNZCNTx.OUTENn = 0
VCOUT0	Comparator output	CMPCTL.COE = 0

NOTE: The settings indicated in the table above are not required for the pins in which a peripheral function is allocated by PIORx register. The pins can be used as a digital output port.

2.2 Procedure for setting port-related registers when peripheral functions are selected

2.2.1 Port latch setting for peripheral function pins

To use pins as the output of a peripheral function, port registers and port mode registers need to be set according to the peripheral function to be used.

Table 3 lists the port latch set values for pins that are used as an output of a peripheral function. Also, **Table 4** shows the setting values of the port registers (port latch) and port mode registers for pins that are used as an output of a peripheral function. Note that the port latch setting is not required for pins that are used as an input of a peripheral function.

Table 3 Port latch set values where pins are used as output pins of peripheral functions

Peripheral function output pin NOTE	Function NOTE	Port latch value	Setting value of port mode register
TOmn	Timer array unit (output)	Pmn = 0	PMmn = 0
TRJIO0, TRJO0	Timer RJ (output)	Pmn = 0	PMmn = 0
TRDIOji	Timer RD (output)	Pmn = 0	PMmn = 0
TxDq, SOp, SCKp, SCLr	Serial array unit (output)	Pmn = 1	PMmn = 0
LTXDn	LIN/UART module output	Pmn = 1	PMmn = 0
CTXD0	CAN interface output	Pmn = 1	PMmn = 0
PCLBUZ0	Clock output/buzzer output	Pmn = 0	PMmn = 0
RTC1HZ	Real-time clock correction clock output	Pmn = 0	PMmn = 0
STOPST	Standby function (STOP status output)	Pmn = 0	PMmn = 0
SNZOUTn	Standby function (SNOOZE status output)	Pmn = 0	PMmn = 0
VCOUT0	Comparator output	Pmn = 0	PMmn = 0
RESOUT	Reset output	Pmn = 0	X
ANO0	D/A converter output	—	PMmn = 1

— : Set a desired value (0, 1),   X: Setting not required

NOTE: Some products may not be provided with some pins (functions).

Table 4 Port latch set values where pins are used as I/O pins of peripheral functions

Peripheral function output pin NOTE	Function NOTE	Port latch set value	Set value of port mode register
SDAmn	Serial array unit (input/output)	Pmn = 1	PMmn = 0
SCLA0, SDAA0	Serial interface IICA (input/output)	Pmn = 0	PMmn = 0

NOTE: Some products may not be provided with some pins (functions).

2.2.2 Setting procedure when timer array units are used

(a) Procedure for setting timer array unit (input) (TImn)

The setting procedure when the P10 pin is used as TI15 (input) is illustrated and described in **Figure 4**.

Remark: When the 100-pin RL78/F14 product is used, m = 0/1 and n = 0 to 7.
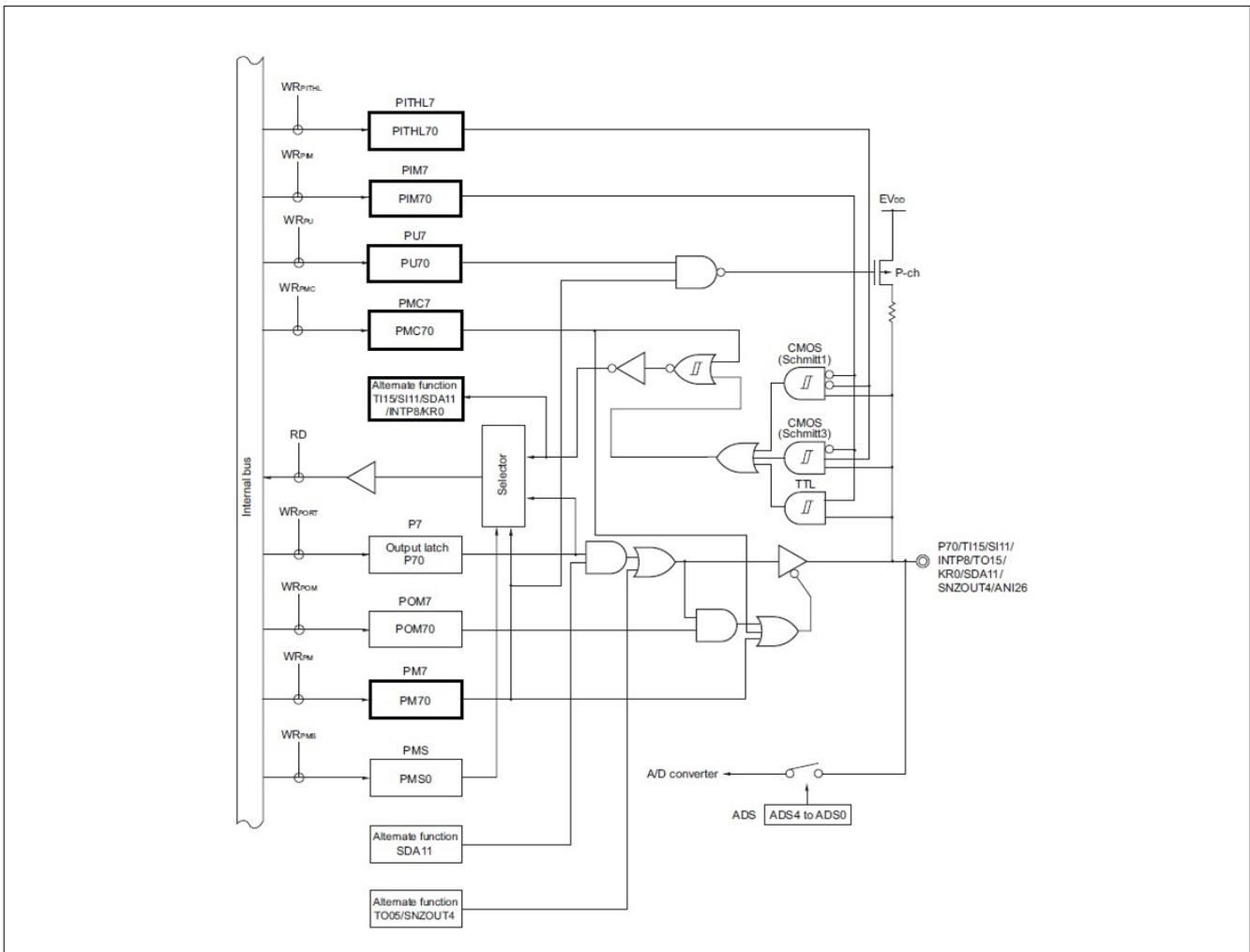
Step	Register	Register setting
1	PIORx	Assign the TI15 pin to the corresponding pin (P70) (PIOR25 = 0).
2	ADPC/PMCx NOTE	Set the corresponding pin (P70) to digital I/O. (PMC70 = 0)
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P70) to input mode. (PM70 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Set the corresponding pin (P70) to "normal input buffer" (PIM70 = 0).
7	POMx	Setting not required
8	PITHLx	Settable [Set a threshold value to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

NOTE: Although the corresponding pin (P70) is provided with these registers, some other pin may not be provided with these registers. In that case, the settings to these registers are unnecessary.

Figure 4 Setting example of timer array unit (input) (P70/TI15)

(b)   Procedure for setting timer array unit (output) (TOmn)

The setting procedure when the P70 pin is used as TO15 (output) is illustrated and described in **Figure 5**.

Remark: When the 100-pin RL78/F14 product is used, m = 0/1 and n = 0 to 7.
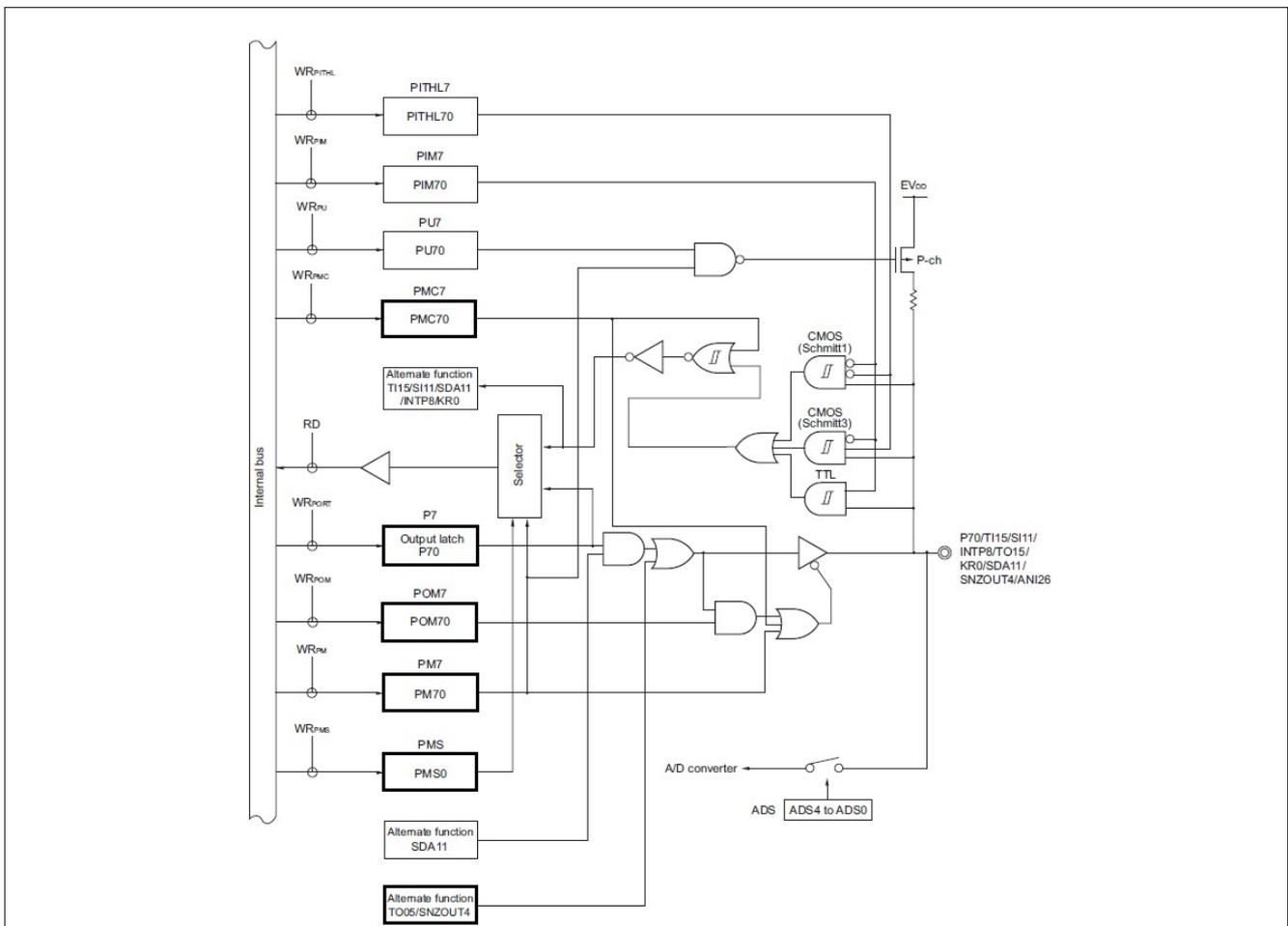
Step	Register	Register setting
1	PIORx	Assign the TO15 pin to the corresponding pin (P70). (PIOR35 = 0)
2	ADPC/PMCx NOTE 1	Set the corresponding pin (P70) to digital I/O. (PMC70 = 0)
3	Pxx	Set the output latch value. (P70 = 0)
4	PMxx	Set the corresponding pin (P70) to output mode. (PM70 = 0)
5	PUxx	Setting not required (On-chip pull-up resistors are disabled.)
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P70) to normal output mode.
8	PITHLx	Setting not required
9	PSRSEL NOTE 2	Setting not required
10	PSNZCNTx NOTE 1	Set the corresponding pin (P70) to disable SNOOZE status output. (OUTEN4 = 0)
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE 1: Although the corresponding pin (P70) is provided with these registers, some other pins may not be provided with these registers. In that case, the settings to these registers are unnecessary.
NOTE 2: Although the corresponding pin (P70) is not provided with this register, some other pins may be provided with this register. In that case, set the register according to your specifications.

Figure 5 Setting example of timer array unit (output) (P70/TO15)

2.2.3   Setting procedure when the timer RJ is used

(a)   Procedure for setting timer RJ (input) (TRJIO0)

The setting procedure when the P41 pin is used as TRJIO0 (input) is illustrated and described in **Figure 6**.

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Setting not required
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P41) to input mode. (PM41 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 6 Setting example of timer RJ (input) (P41/TRJIO0)

(b)   Procedure for setting timer RJ (output) (TRJIO0, TRJO0)

The setting procedure when the P10 pin is used as TRJIO0 (output) is illustrated and described in **Figure 7**.

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P10 = 0)
4	PMxx	Set the corresponding pin (P10) to output mode. (PM10 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P10) to normal output mode. (POM10= 0)
8	PITHLx	Setting not required
9	PSRSEL	Settable (normal slew rate/special slew rate)
10	PSNZCNTx	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

Figure 7 Setting example of timer RJ (output) (P10/TRJO0)

2.2.4   Setting procedure when the timer RD is used

(a)   Procedure for setting timer RD (input) (TRDIOAi, TRDIOBi, TRDIOCi, TRDIODi, TRDCLKi)

The setting procedure when the P13 pin is used as TRDIOA0 (input) is illustrated and described in **Figure 8**.

Remark: i = 0/1
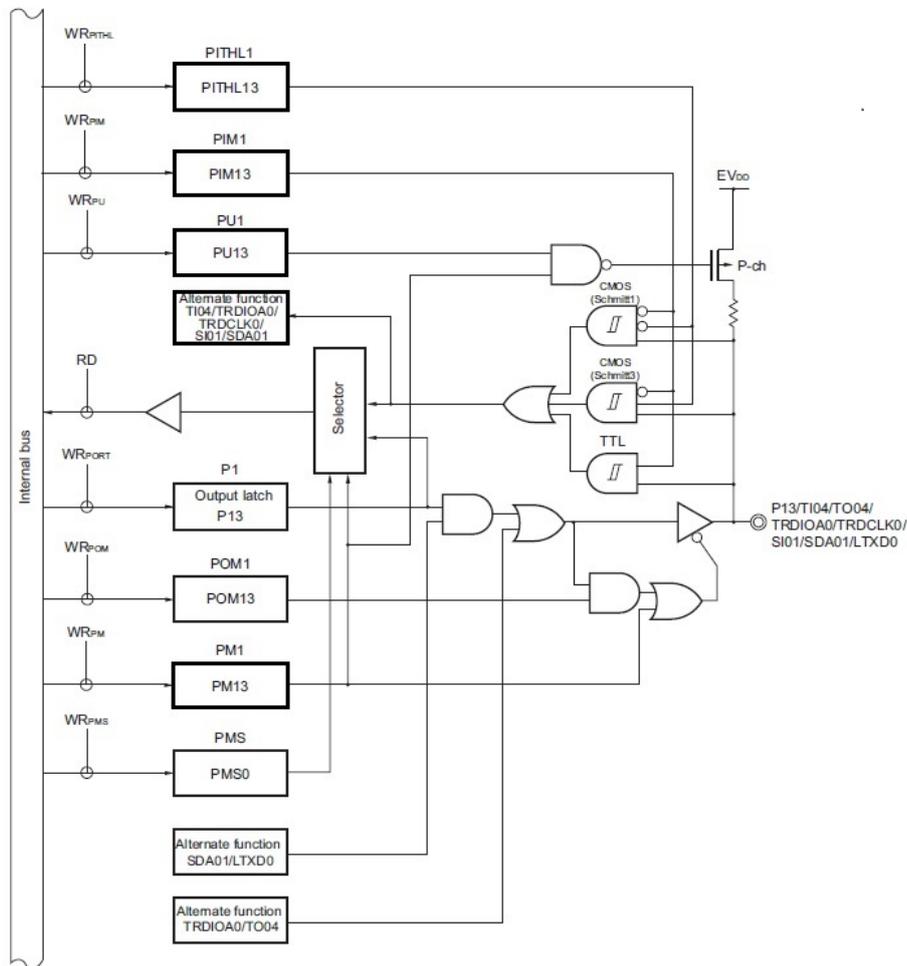
Step	Register	Register setting
1	PIORx	Assign the TRDIOA pin to the corresponding pin (P13). (PIOR70 = 0)
2	ADPC/PMCx **NOTE**	Setting not required
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P13) to input mode. (PM13 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Set the corresponding pin (P13) to normal input buffer. (PIM13 = 0)
7	POMx	Setting not required
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

NOTE: Although the corresponding pin (P13) is not provided with these registers, some other pins may be provided with these registers. In that case, set the corresponding pin to be used as digital I/O.

Figure 8 Setting example of timer RD (input) (P13/TRDIOA0)

(b)   Procedure for setting timer RD (output) (TRDIOAi, TRDIOBi, TRDIOCi, TRDIODi)

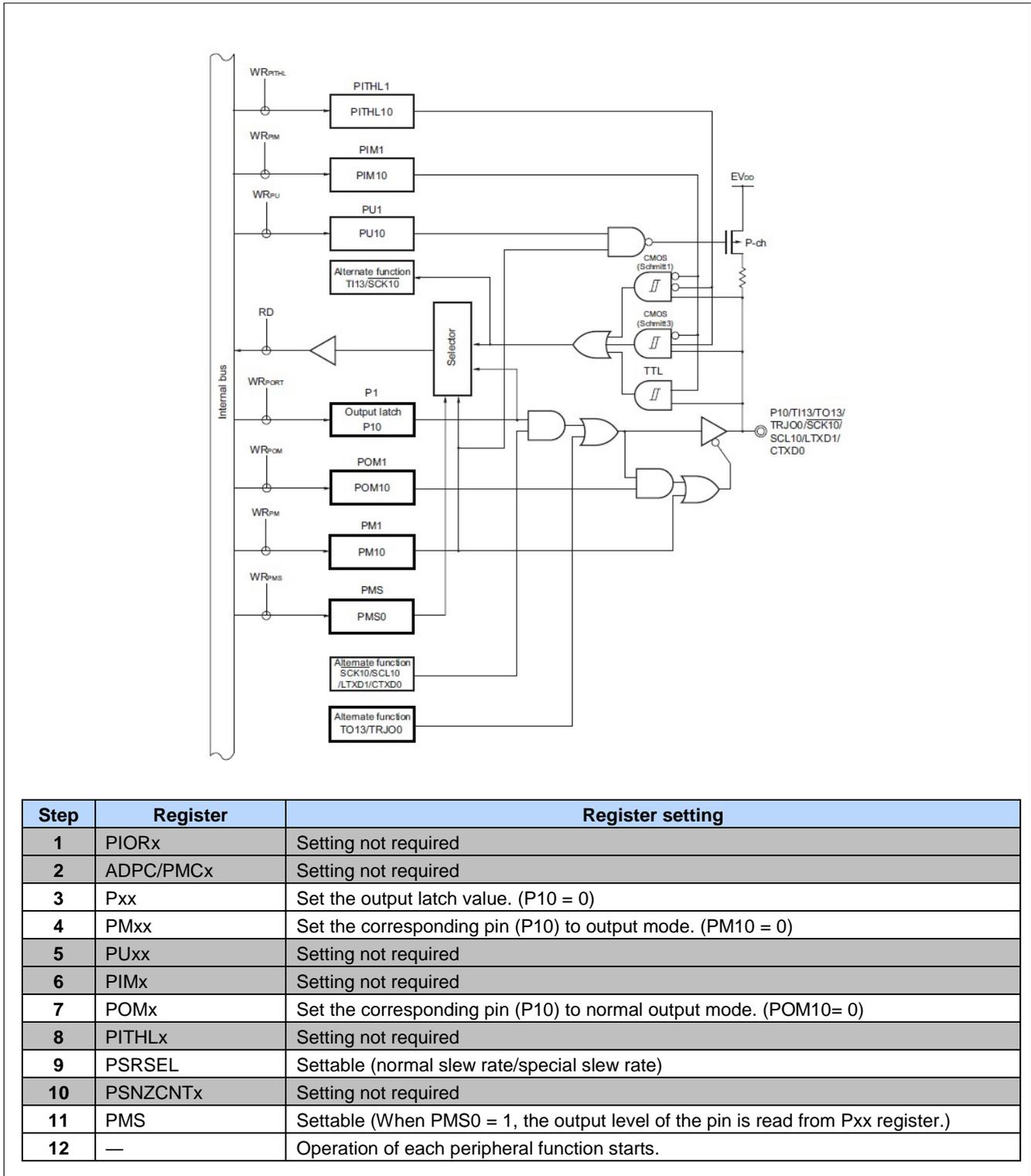The setting procedure when the P13 pin is used as TRDIOA0 (output) is illustrated and described in **Figure 9**.

Remark: i = 0/1
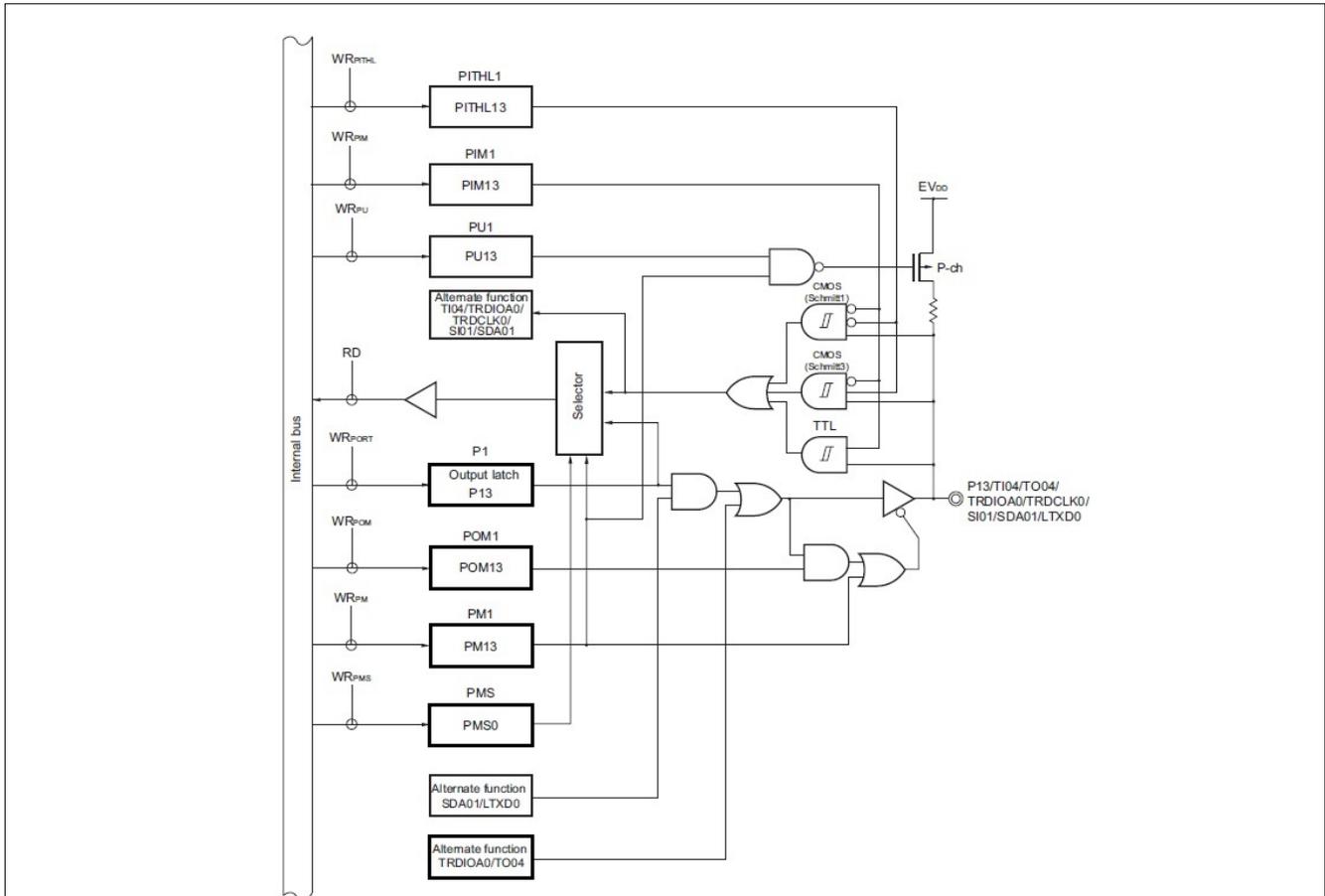
Step	Register	Register setting
1	PIORx	Assign the TRDIOA0 pin to the corresponding pin (P13). (PIOR70 = 0)
2	ADPC/PMCx NOTE 1	Setting not required
3	Pxx	Set the output latch value. (P13 = 0)
4	PMxx	Set the corresponding pin (P13) to output mode. (PM13 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P13) to normal output mode. (POM13 = 0)
8	PITHLx	Setting not required
9	PSRSEL NOTE 2	Setting not required
10	PSNZCNTx NOTE 3	Setting not required
11	PMS	Settable (When PMS0= 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE 1: Although the corresponding pin (P13) is not provided with these registers, some other pins may be provided with these registers. In that case, set the pin to be used as digital I/O.

NOTE 2: Although the corresponding pin (P13) is not provided with this register, some other pins may be provided with this register. In that case, set the register according to your specifications.

NOTE 3: Although the corresponding pin (P13) is not provided with this register, some other pins may be provided with this register. In that case, set this pin to disable SNOOZE status output.

Figure 9 Setting example of timer RD (output) (P13/TRDIOA0)

2.2.5 Setting procedure when the serial array unit is used

(a) Procedure for setting serial array unit (input) (RXDq, SIp, SCKp, SSIp)

The setting procedure when the P16 pin is used as RXD0 (input) is illustrated and described in **Figure 10**.

Remark: When the 100-pin RL78/F14 product is used, q = 0/1 and p = 00/01/10/11.

Step	Register	Register setting
1	PIORx	Assign the RXD0 pin to the corresponding pin (P16). (PIOR40 = 0)
2	ADPC/PMCx	Setting not required
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P16) to input mode. (PM16 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Settable (Set the input buffer to "normal" or "TTL".)
7	POMx	Setting not required
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 10 Setting example of serial array unit (input) (P16/RXD0)

(b)   Procedure for setting serial array unit (output) (TXDq, SOp, SCKp)

The setting procedure when the P15 pin is used as TXD0 (output) is illustrated and described in **Figure 11**.

Remark: When the 100-pin RL78/F14 product is used, q = 0/1 and p = 00/01/10/11.

Step	Register	Register setting
1	PIORx	Assign the TXD0 pin to the corresponding pin (P15). (PIOR40 = 0)
2	ADPC/PMCx NOTE 1	Setting not required
3	Pxx	Set the output latch value. (P15 = 0)
4	PMxx	Set the corresponding pin (P15) to output mode. (PM15 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Settable (Normal output/N-ch open drain output)
8	PITHLx	Setting not required
9	PSRSEL NOTE 2	Setting not required
10	PSNZCNTx NOTE 3	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

**NOTE 1**: Although the corresponding pin (P15) is not provided with these registers, some other pins may be provided with these registers. In that case, set the pin to be used as a digital I/O.
NOTE 2: Although the corresponding pin (P15) is not provided with this register, some other pins may be provided with this register. In that case, set the register according to your specifications.
NOTE 3: Although the corresponding pin (P15) is not provided with this register, some other pins may be provided with this register. In that case, set the corresponding pin(s) to disable the SNOOZE status output.

Figure 11 Setting example of serial array unit (P15/TXD0)

(c)   Procedure for setting serial array unit (input/output) (SDAr, SCLr)

The setting procedure when the P16 pin is used as SDA00 (input/output) is illustrated and described in **Figure 12.**

Remark: When the 100-pin RL78/F14 product is used, r = 00/01/10/11.
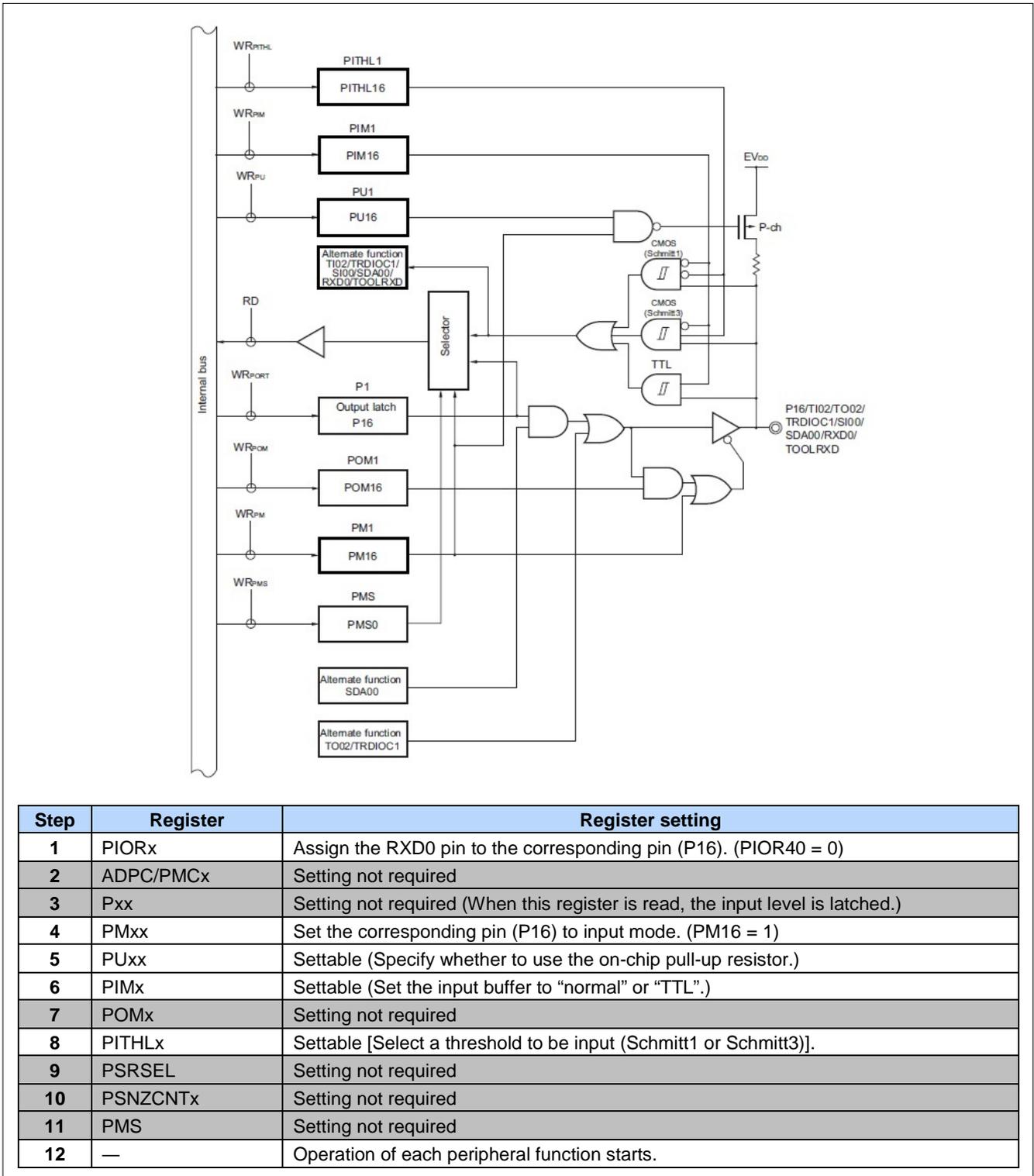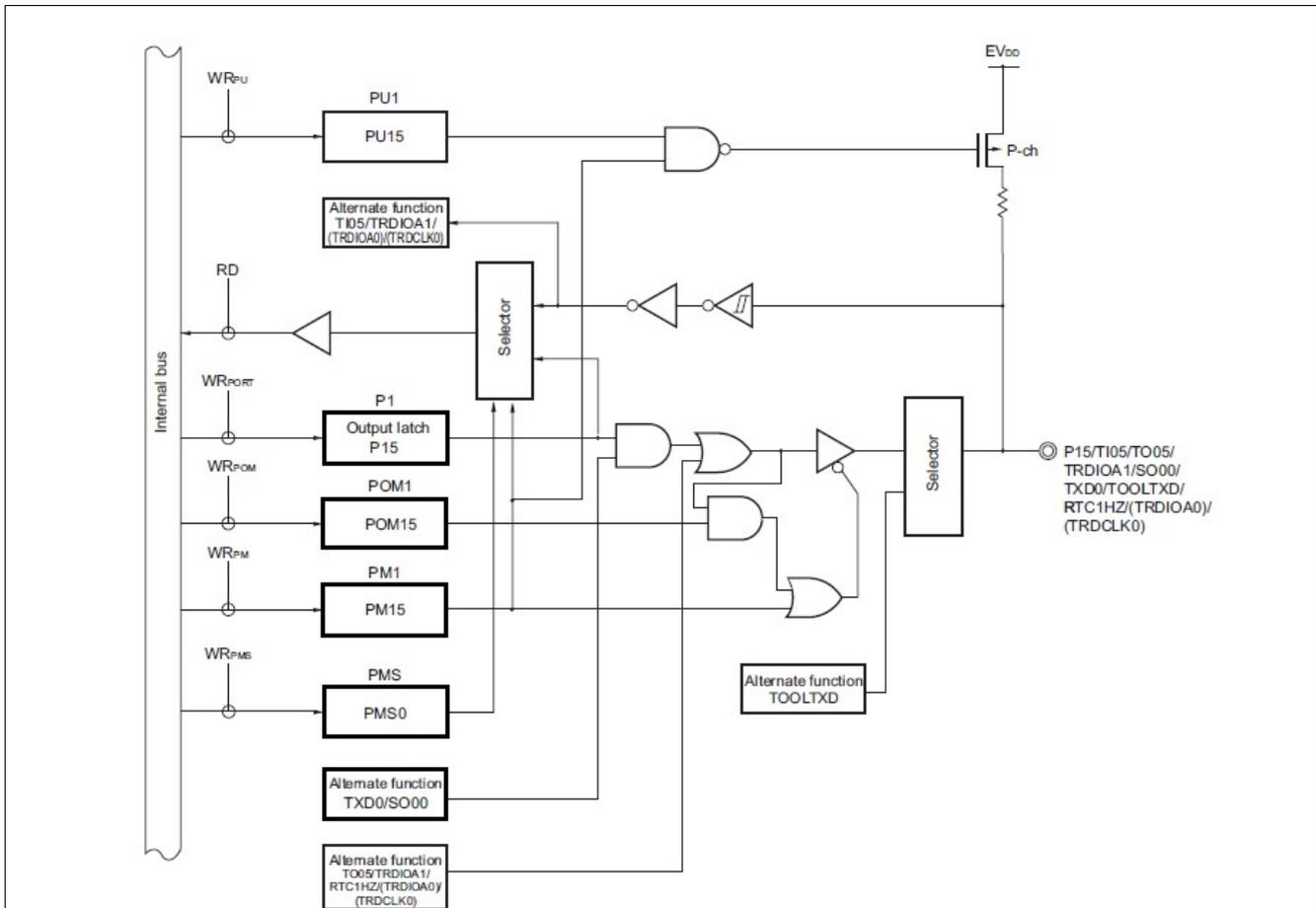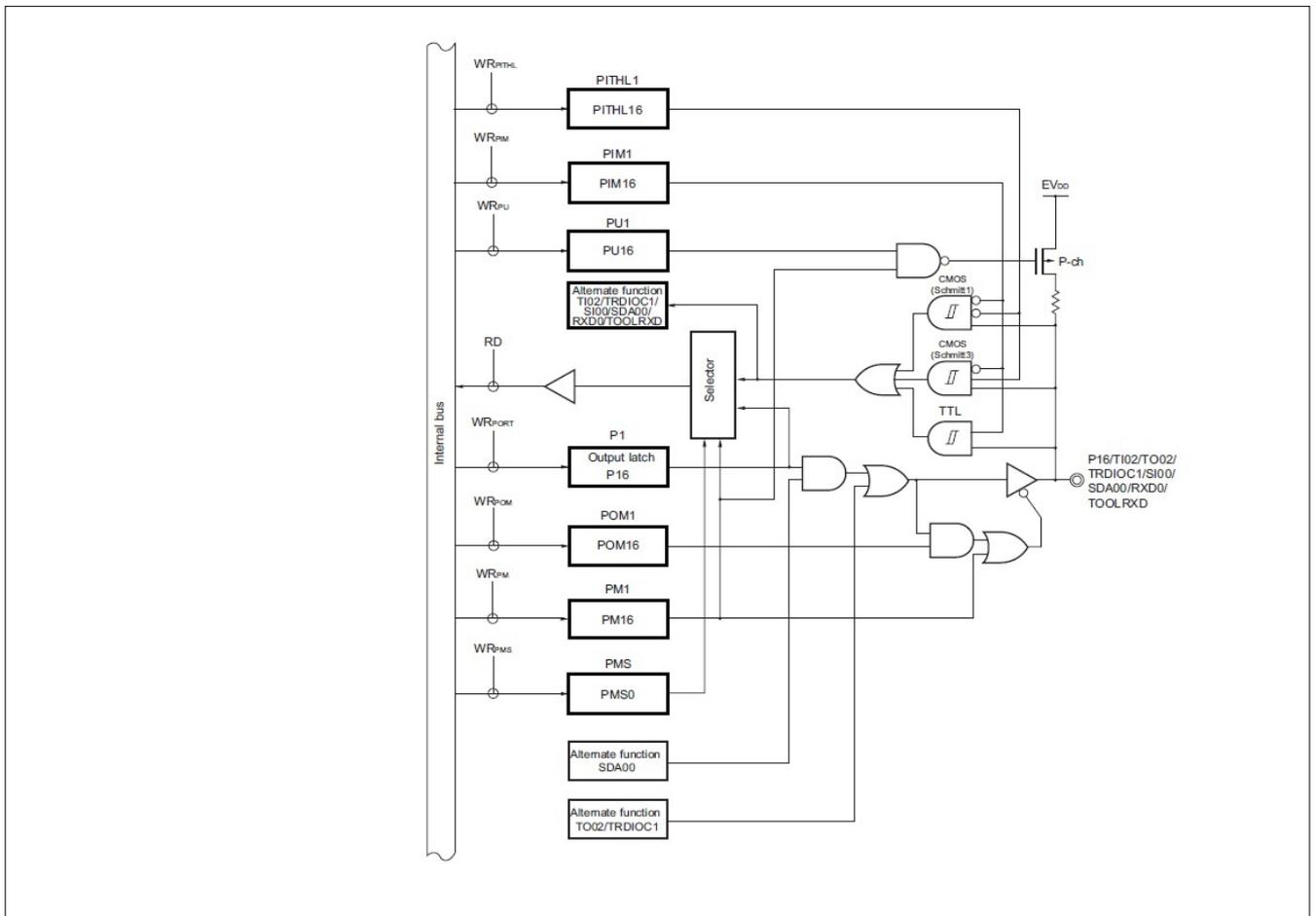

Step	Register	Register setting
1	PIORx	Assign the SDA00 pin to the corresponding pin (P16). (PIOR40 = 0)
2	ADPC/PMCx NOTE 1	Setting not required
3	Pxx	Set the output latch value. (P16 = 1)
4	PMxx	Set the corresponding pin (P16) to output mode. (PM16 = 0)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Settable (Set the input buffer to "normal" or "TTL".)
7	POMx	Set the corresponding pin (P16) to N-ch open drain output. (POM16 = 1)
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL NOTE 2	Setting not required
10	PSNZCNTx NOTE 3	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE 1: Although the corresponding pin (P16) is not provided with these registers, some other pins may be provided with these registers. In that case, set the corresponding pin to be used as a digital I/O.
NOTE 2: Although the corresponding pin (P16) is not provided with this register, some other pins may be provided with this register. In that case, set the registers according to your specifications.
**NOTE 3**: Although the corresponding pin (P16) is not provided with this register, some other pins may be provided with this register. In that case, set the corresponding pin to disable the SNOOZE status output.

Figure 12 Setting example of serial array unit (output) (P16/SDA00)

2.2.6   Setting procedure when the serial interface IICA is used

(a)   Procedure for setting serial array unit (input/output) (SDAA0, SCLA0)

The setting procedure when the P63 pin is used as SDAA0 (input/output) is illustrated and described in **Figure 13**.

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P63 = 0)
4	PMxx	Set the corresponding pin (P63) to output mode. (PM63 = 0)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Settable (Set the input buffer to "normal" or "TTL".)
7	POMx	Set the corresponding pin (P63) to N-ch open drain output. (POM63 = 1)
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 13 Setting example of serial interface IICA (input/output) (P63/SDAA0)

2.2.7   Setting procedure when the CAN interface is used

(a)   Procedure for setting serial array unit (input) (CRXD0)

The setting procedure when the P11 pin is used as CRXD0 (input) is illustrated and described in **Figure 14**.
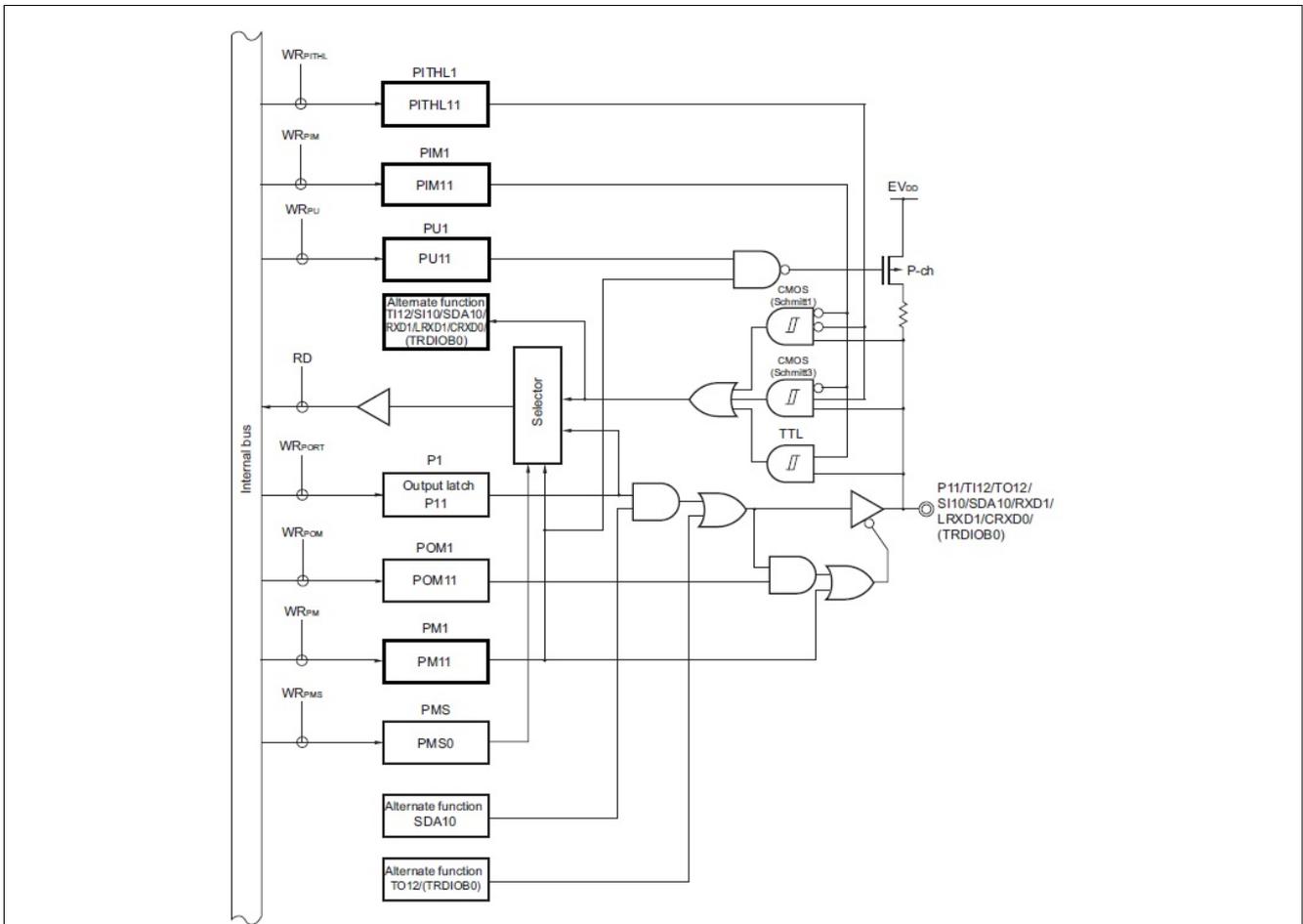
Step	Register	Register setting
1	PIORx	Assign the CRXD0 pin to the corresponding pin (P11). (PIOR46 = 0)
2	ADPC/PMCx **NOTE**	Setting not required
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P11) to input mode. (PM11 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Set the corresponding pin (P11) to normal input buffer. (PIM11 = 0)
7	POMx	Setting not required
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

NOTE: Although the corresponding pin (P11) is not provided with these registers, some other pins may be provided with these registers. In that case, set the corresponding pin to be used digital I/O.

Figure 14 Setting example of CAN interface (P11/CRXD0)

(b)   Procedure for setting serial array unit (output) (CTXD0)

The setting procedure when the P10 pin is used as CTXD0 (output) is illustrated and described in **Figure 15**.
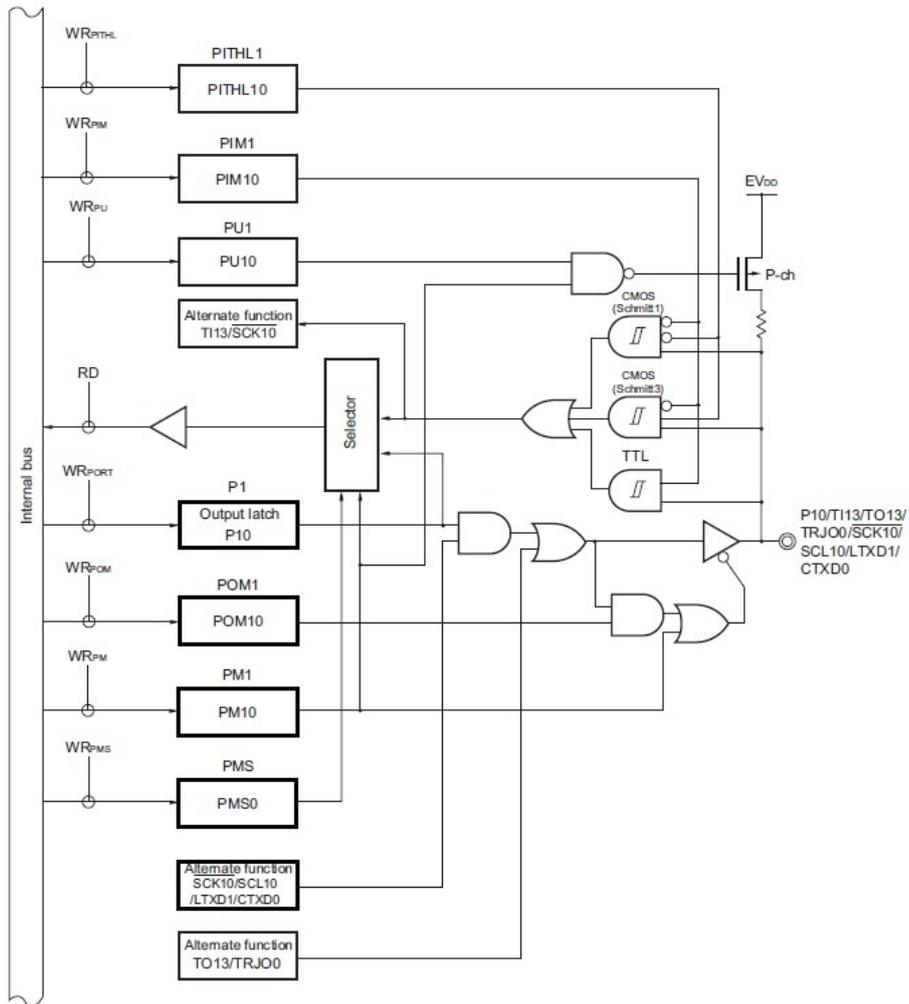
Step	Register	Register setting
1	PIORx	Assign the CTXD0 pin to the corresponding pin (P10). (PIOR46 = 0)
2	ADPC/PMCx NOTE 1	Setting not required
3	Pxx	Set the output latch value. (P10 = 0)
4	PMxx	Set the corresponding pin (P10) to output mode. (PM10 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P10) to normal output mode. (POM10 = 0)
8	PITHLx	Setting not required
9	PSRSEL	Set the corresponding pin (P10) to normal slew rate.
10	PSNZCNTx NOTE 2	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE 1: Although the corresponding pin (P10) is not provided with these registers, some other pins may be provided with these registers. In that case, set the corresponding pins to be used as digital I/O.
NOTE 2: Although the corresponding pin (P10) is not provided with this register, some other pins may be provided with this register. In that case, set the registers according to your specifications.

Figure 15 Setting example of CAN interface (output) (P10/CTXD0)

2.2.8 Setting procedure when the LIN/UART module is used

(a) Procedure for setting serial array unit (input) (LRXDn)

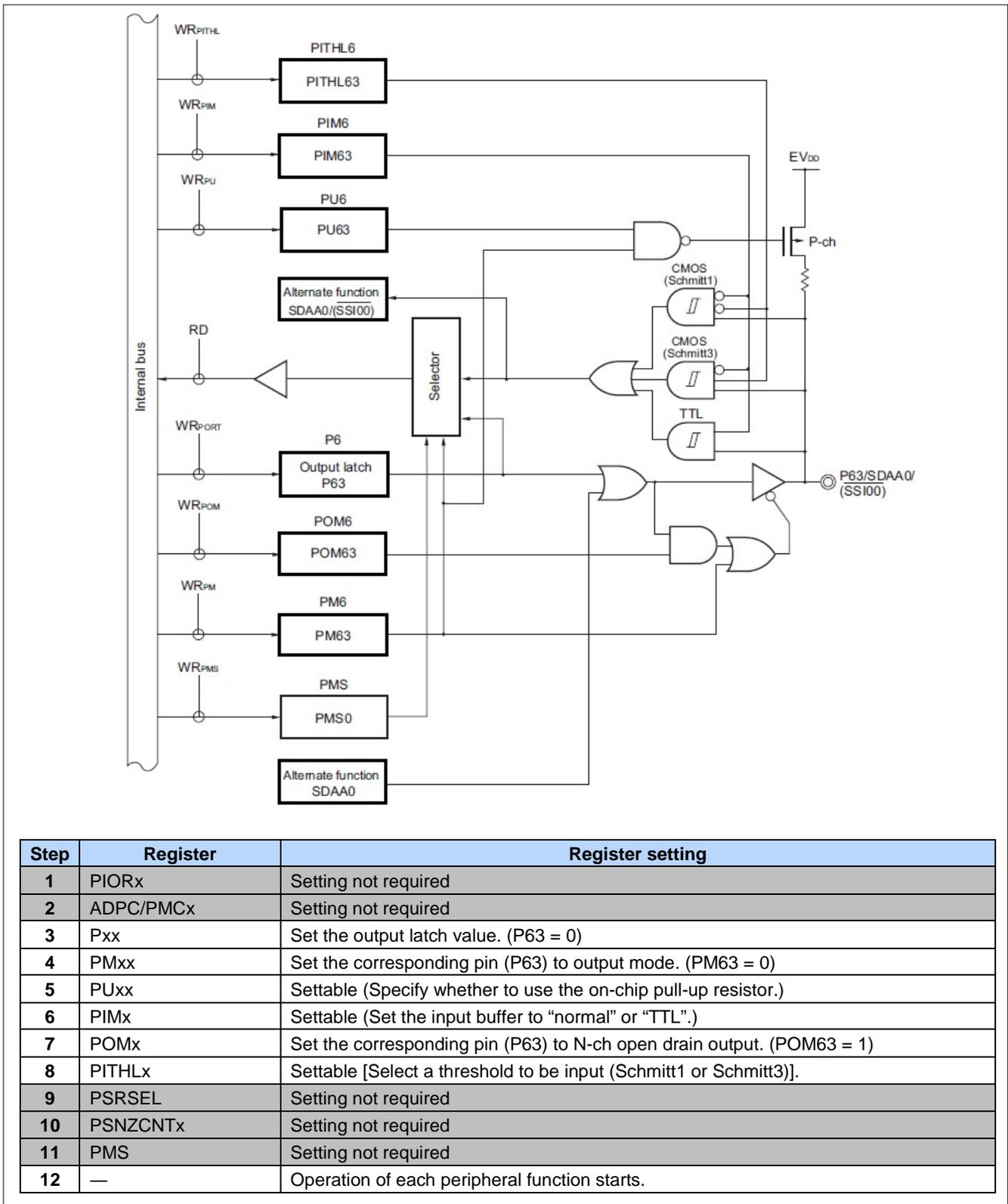The setting procedure when the P14 pin is used as LRXD0 (input) is illustrated and described in **Figure 16**.

Remark: When the 100-pin RL78/F14 product is used, n = 0/1.

Step	Register	Register setting
1	PIORx	Assign the LRXD0 pin to the corresponding pin (P14). (PIOR44 = 0)
2	ADPC/PMCx	Setting not required
3	Pxx	Setting not required (When this register is read, the input level is latched.)
4	PMxx	Set the corresponding pin (P14) to input mode. (PM14 = 1)
5	PUxx	Settable (Specify whether to use the on-chip pull-up resistor.)
6	PIMx	Set the corresponding pin (P14) to normal input buffer. (PIM14 = 0)
7	POMx	Setting not required
8	PITHLx	Settable [Select a threshold to be input (Schmitt1 or Schmitt3)].
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 16 Setting example of LIN/UART interface (P14/LRXD0)

(b)   Procedure for setting serial array unit (output) (LTXDn)

The setting procedure when the P13 pin is used as LTXD0 (output) is illustrated and described in **Figure 17**.

Remark: When the 100-pin RL78/F14 product is used, n = 0/1.

Step	Register	Register setting
1	PIORx	Assign the LTXD0 pin to the corresponding pin (P13). (PIOR44 = 0)
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P13 = 1)
4	PMxx	Set the corresponding pin (P13) to output mode. (PM13 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P13) to normal output mode. (POM13 = 0)
8	PITHLx	Setting not required
9	PSRSEL NOTE	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE: Although the corresponding pin (P13) is not provided with this register, some other pins may be provided with this register. In that case, set the register according to your specifications.

Figure 17 Setting example of LIN/UART interface (output)(P13/LTXD0)

2.2.9   Setting procedure when clock output/buzzer output controller is used

(a)   Procedure for setting PCLBUZ0 (clock output/buzzer output)

The setting procedure when the P140 pin is used as PCLBUZ0 (output) is illustrated and described in **Figure 18**.

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P140 = 0)
4	PMxx	Set the corresponding pin (P140) to output mode. (PM140 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Settable (Set the output port to normal slew rate or special slew rate.)
10	PSNZCNTx	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

Figure 18 Setting example of clock/buzzer output (P140/PCLBUZ0)

2.2.10   Setting procedure when the real-time clock is used

(a)   Procedure for setting RTC1HZ [real-time clock correction clock (1Hz) output]

The setting procedure when the P15 pin is used as RTC1HZ (output) is illustrated and described in **Figure 19**.

Step	Register	Register setting
1	PIORx	Assign the RTC1HZ pin to the corresponding pin (P15). (PIOR80 = 0)
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P15 = 0)
4	PMxx	Set the corresponding pin (P15) to output mode. (PM15 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Set the corresponding pin (P15) to normal output mode. (POM15 = 0)
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

Figure 19 Setting example of real-time clock correction output (P15/RTC1HZ)

2.2.11 Setting procedure when the standby function is used

(a) Procedure for setting STOPST (STOP status output)

The setting procedure when the P31 pin is used as STOPST (output) is illustrated and described in **Figure 20**.

Step	Register	Register setting
1	STPSTC	Assign the STOPST pin to the corresponding pin (P31). (STPLV = 0, STPSEL = 0)
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P31 = 0)
4	PMxx	Set the corresponding pin (P31) to output mode. (PM31 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

Figure 20 Setting example of STOP status output (P31/STOPST)

(b)   Procedure for setting SNZOUTn (SNOOZE status output)

The setting procedure when the P30 pin is used as SNZOUT0 (standby function) (output) is illustrated and described in **Figure 21**.

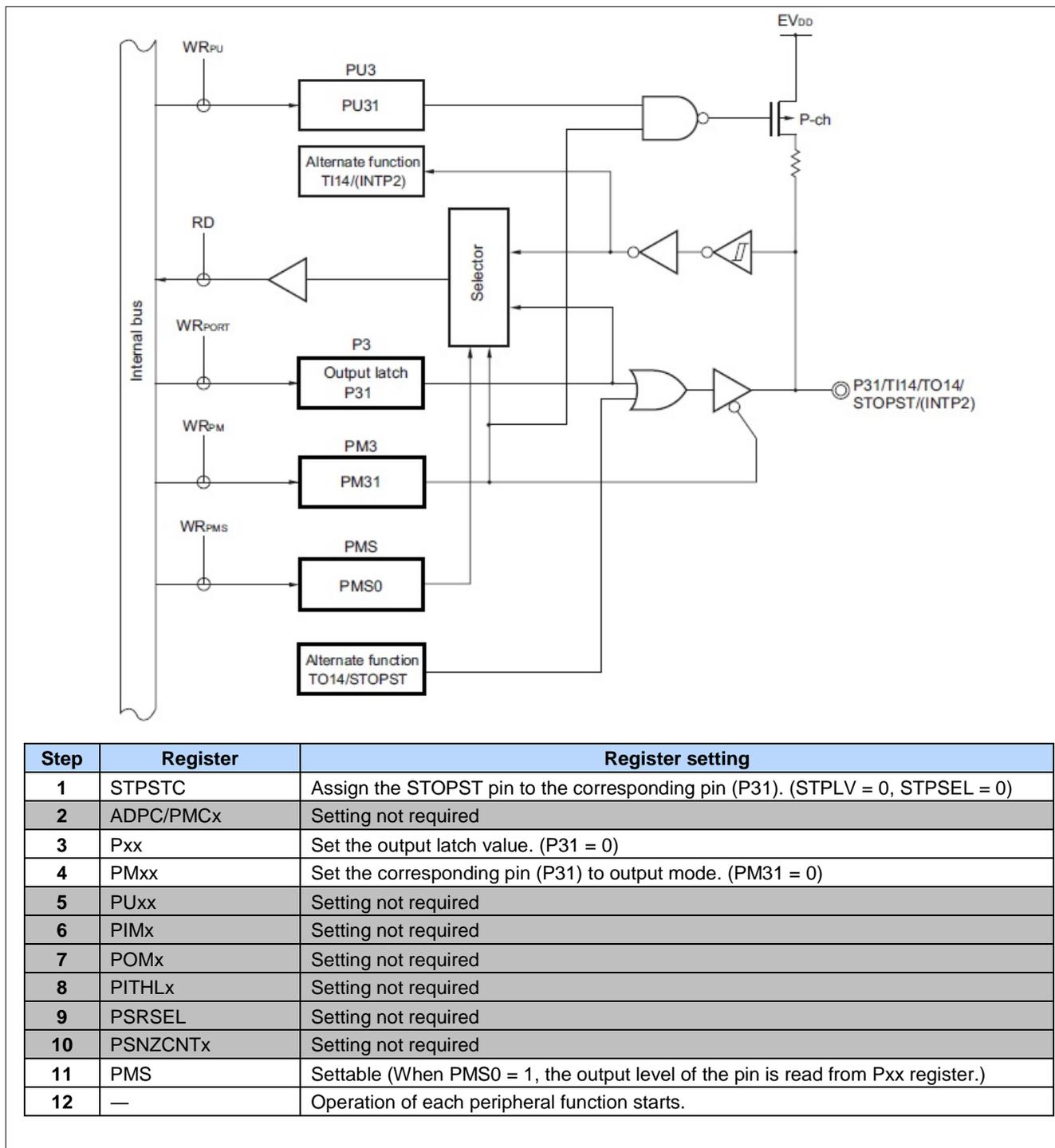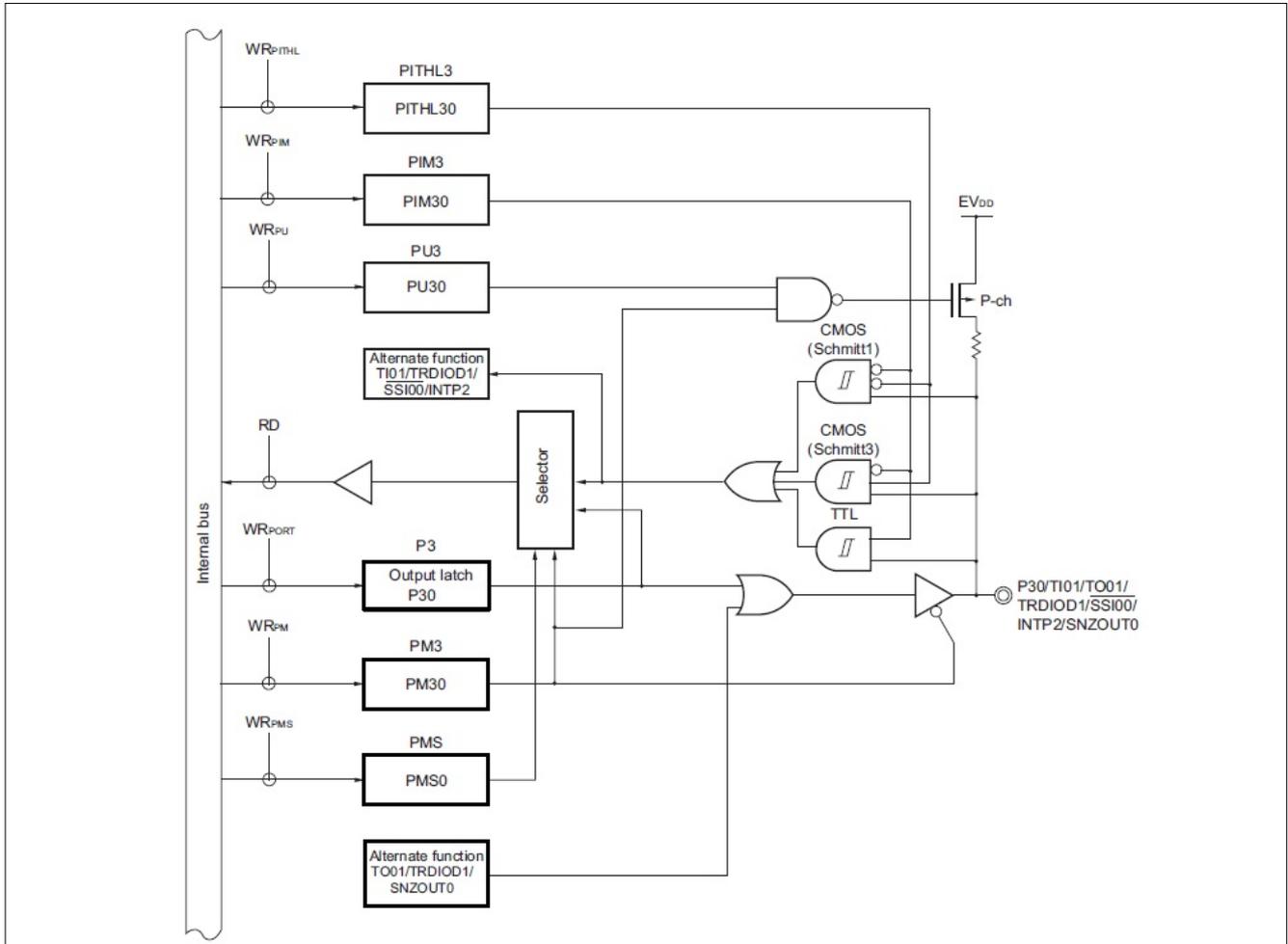**Remark**: When the 100-pin RL78/F14 product is used, n = 0 to 7.

Step	Register	Register setting
1	PIORx	Assign the SNZOUT0 pin to the corresponding pin (P30). (PIOR60 = 0)
2	ADPC/PMCx NOTE 1	Setting not required
3	Pxx	Set the output latch value. (P30 = 0)
4	PMxx	Set the corresponding pin (P30) to output mode. (PM30 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx NOTE 2	Setting not required
8	PITHLx	Setting not required
9	PSRSEL NOTE 2	Set the corresponding pin (P30) to normal slew rate. (PSR30 = 0)
10	PSNZCNTx	Set the corresponding pin (P30) to enable SNOOZE status. (OUTEN0 = 1)
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

NOTE 1: Although the corresponding pin (P30) is not provided with these registers, some other pins may be provided with these registers. In that case, set the pin to be used as digital I/O.

NOTE 2: Although the corresponding pin (P30) is provided with these registers, some other pins may not be provided with these registers. In that case, the settings to these registers are unnecessary.

Figure 21 Setting example of SNOOZE status output (P30/SNZOUT0)

2.2.12   Setting procedures when the comparator is used

(a)   Procedure for setting IVCMP0n (comparator input)

The setting procedure when the P81 pin is used as IVCMP00 (comparator) (input) is illustrated and described in **Figure 22.**

Remark: n = 0 to 3

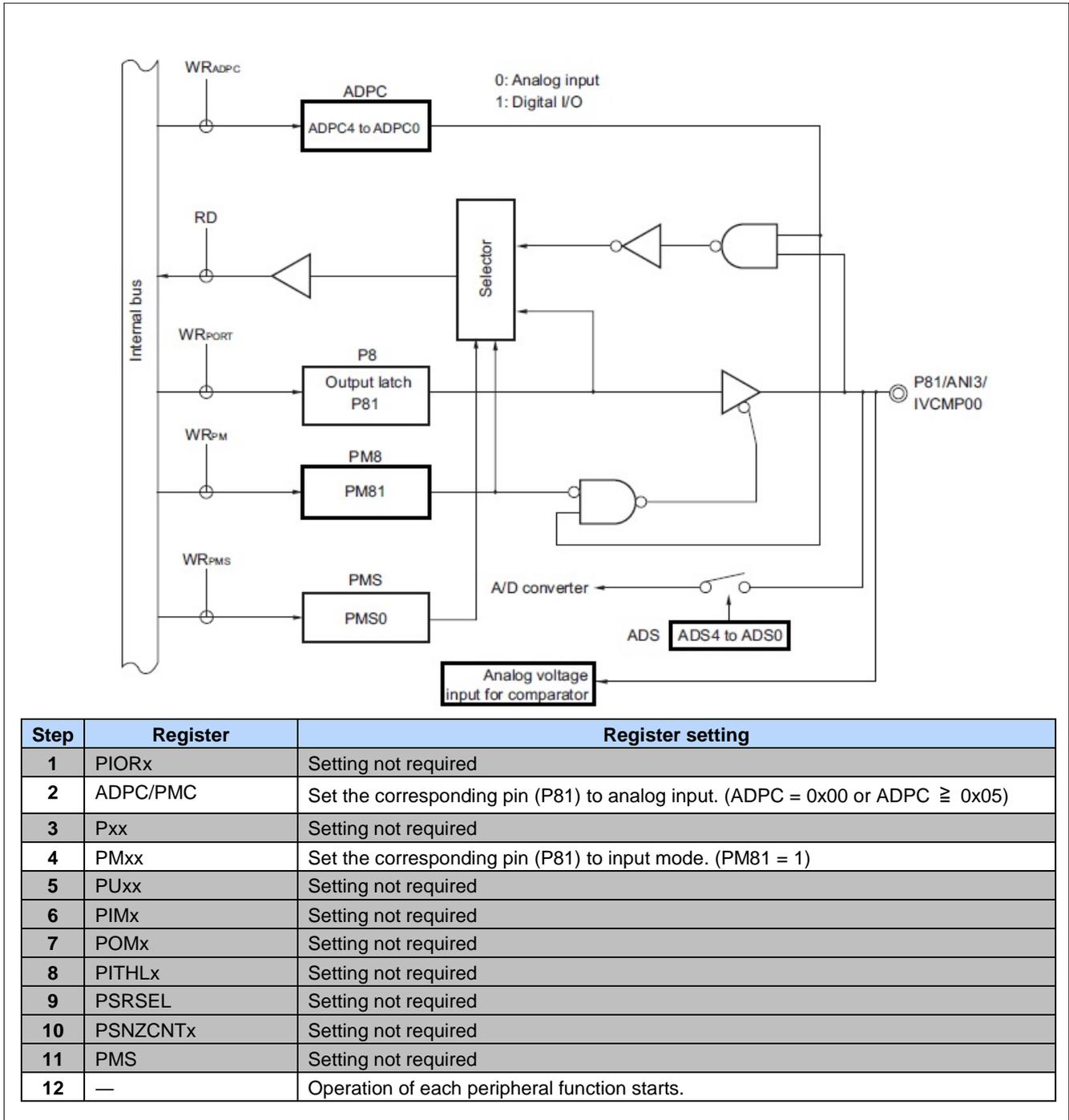| Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMC	Set the corresponding pin (P81) to analog input. (ADPC = 0x00 or ADPC ≧ 0x05)
3	Pxx	Setting not required
4	PMxx	Set the corresponding pin (P81) to input mode. (PM81 = 1)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 22 Setting example of comparator analog input (P81/IVCMP00)

(b)   Procedure for setting IVREF0 (external reference voltage input)

   The setting procedure when the P85 pin is used as IVREF0 (comparator) (external reference voltage input) is illustrated and described in **Figure 23**.

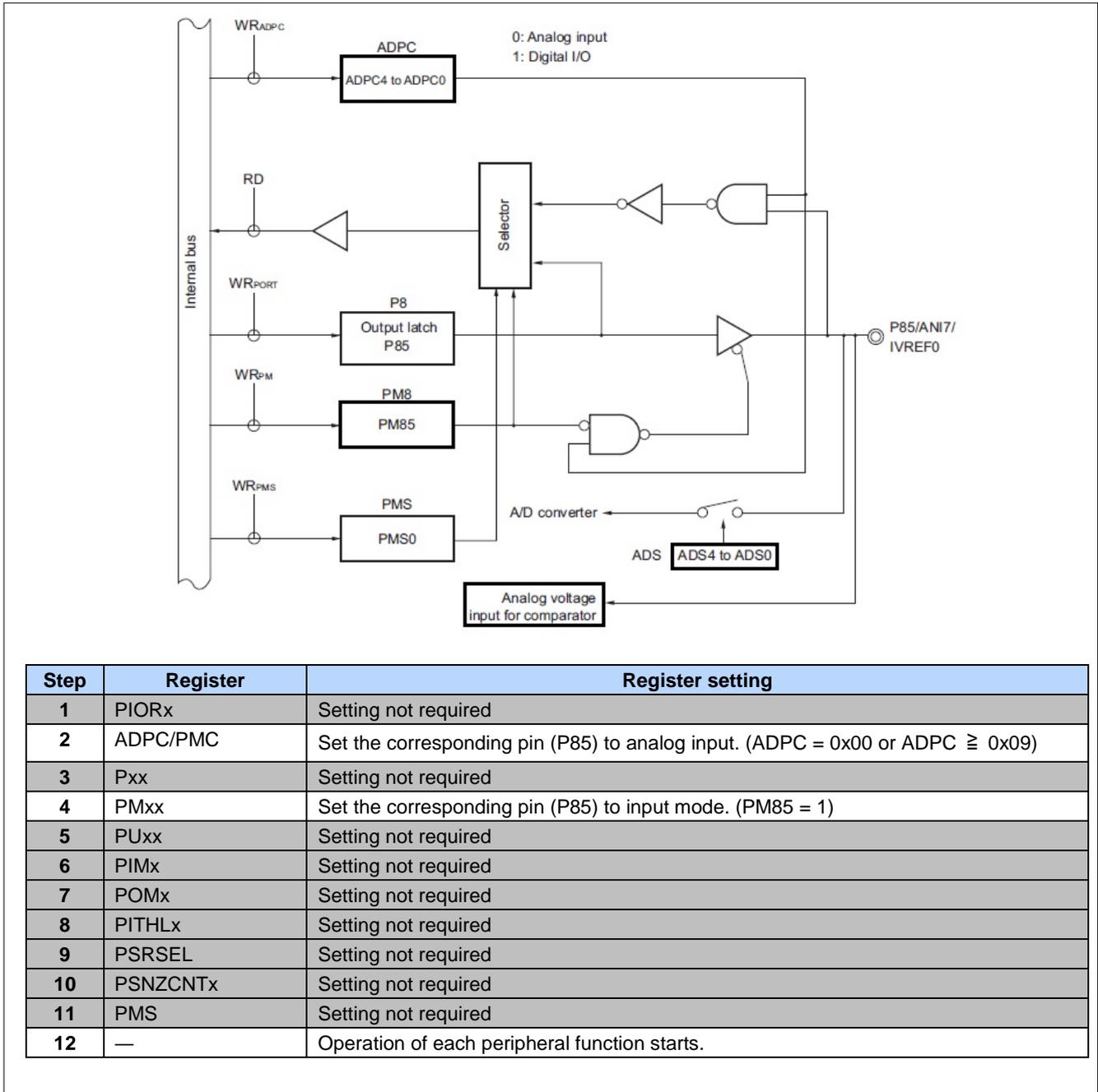| Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMC	Set the corresponding pin (P85) to analog input. (ADPC = 0x00 or ADPC ≧ 0x09)
3	Pxx	Setting not required
4	PMxx	Set the corresponding pin (P85) to input mode. (PM85 = 1)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 23 Setting example of comparator external reference voltage input (P85/IVREF0)

(c)   Procedure for setting VCOUT0 (comparator output)

The setting procedure when the P41 pin is used as VCOUT0 (comparator) (output) is illustrated and described in **Figure 24**.
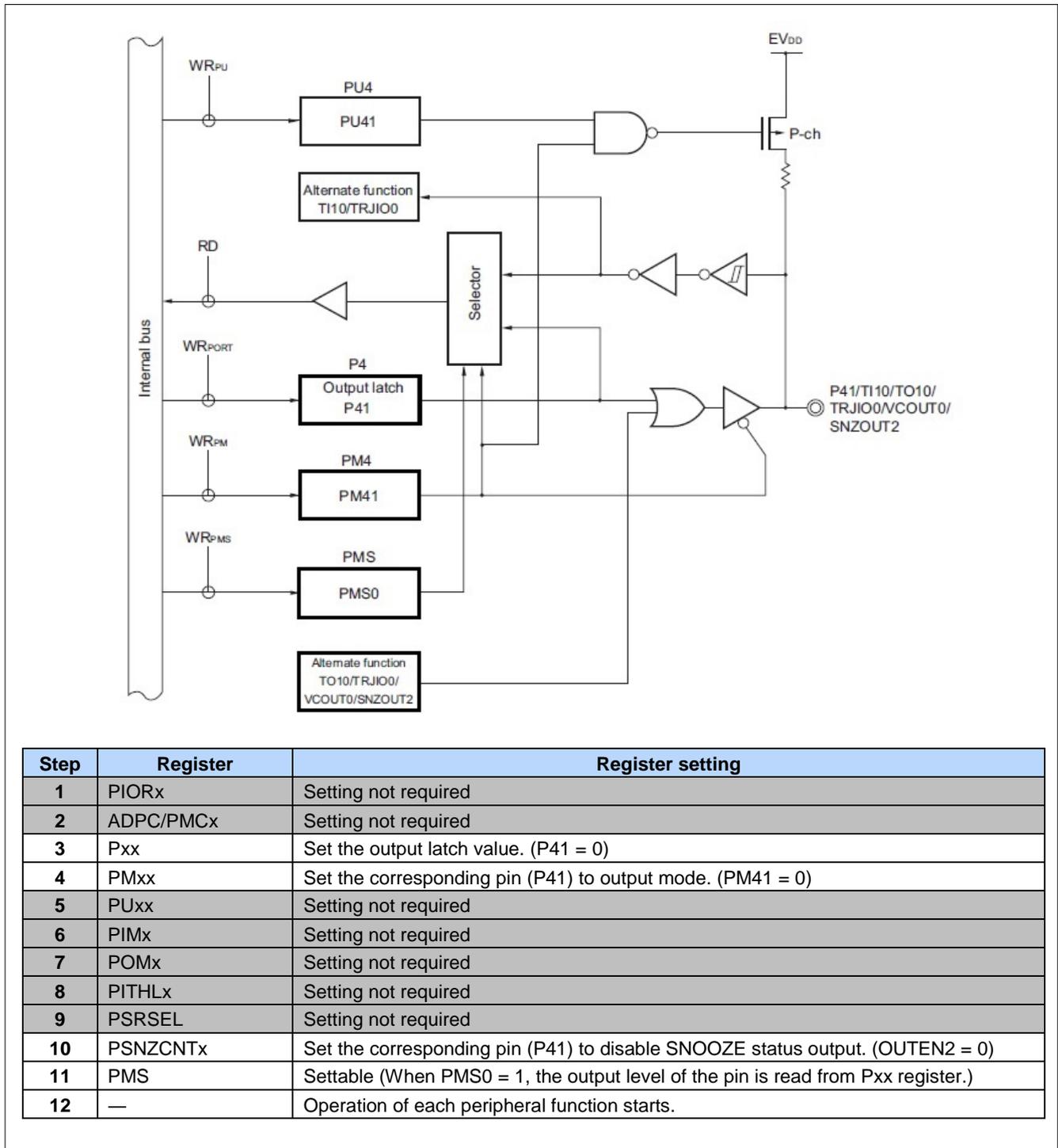

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Setting not required
3	Pxx	Set the output latch value. (P41 = 0)
4	PMxx	Set the corresponding pin (P41) to output mode. (PM41 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Set the corresponding pin (P41) to disable SNOOZE status output. (OUTEN2 = 0)
11	PMS	Settable (When PMS0 = 1, the output level of the pin is read from Pxx register.)
12	—	Operation of each peripheral function starts.

Figure 24 Setting example of comparator output (P41/VCOUT0)

2.2.13 Setting procedure when the A/D converter is used

(a) Procedure for ANin (analog input)

The setting procedure when the P33 pin is used as ANI0 (A/D converter) (input) is illustrated and described in **Figure 25**.

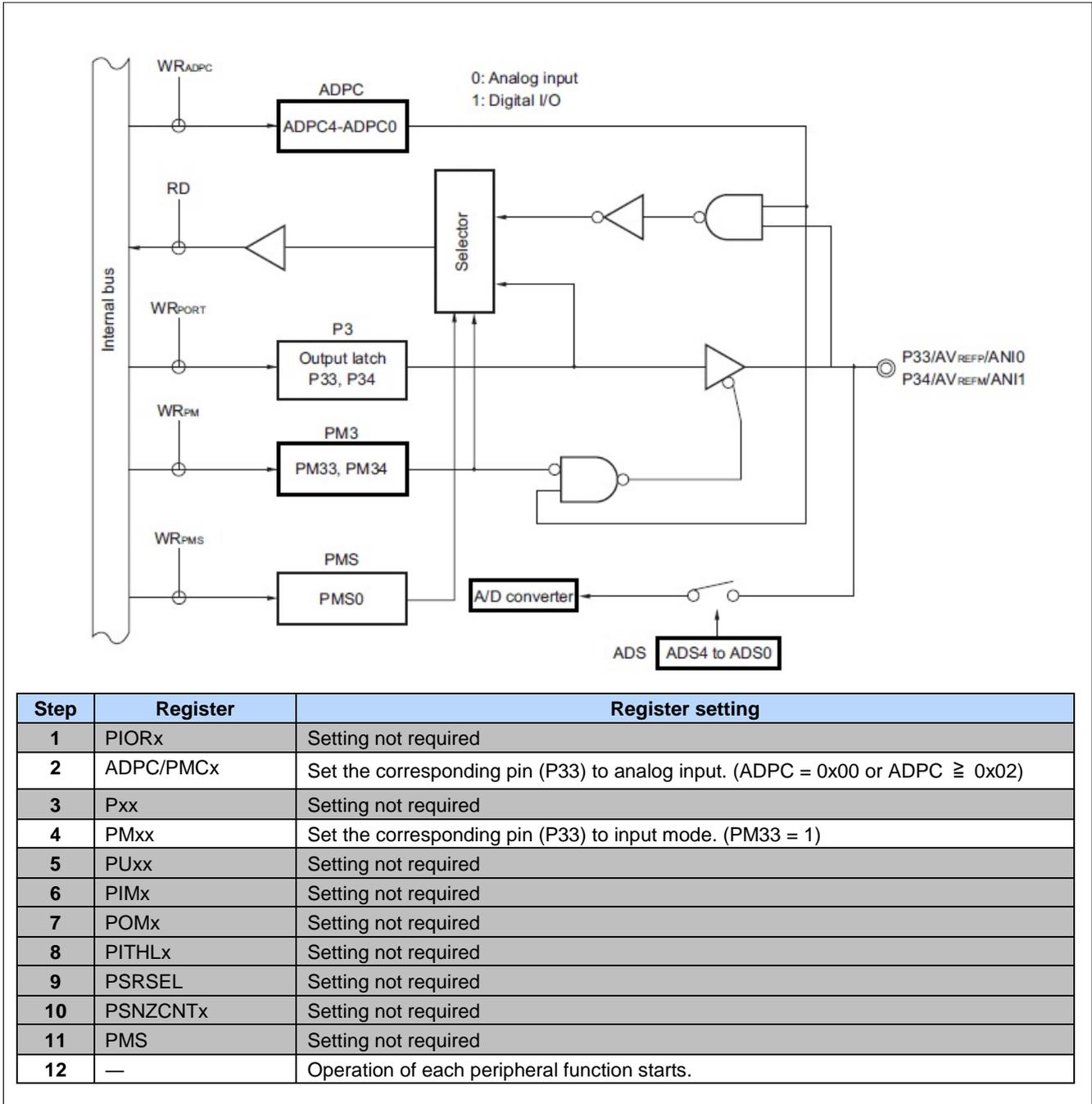**Remark**: When the 100-pin RL78/F14 product is used, n = 0 to 30.

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMCx	Set the corresponding pin (P33) to analog input. (ADPC = 0x00 or ADPC ≧ 0x02)
3	Pxx	Setting not required
4	PMxx	Set the corresponding pin (P33) to input mode. (PM33 = 1)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 25 Setting example of A/D converter analog input (P33/ANI0)

2.2.14   Setting procedure when the D/A converter is used

(a)   Procedure for setting ANO0 (D/A output)

The setting procedure when the P80 pin is used as ANO0 (D/A converter) (output) is illustrated and described in **Figure 26**.
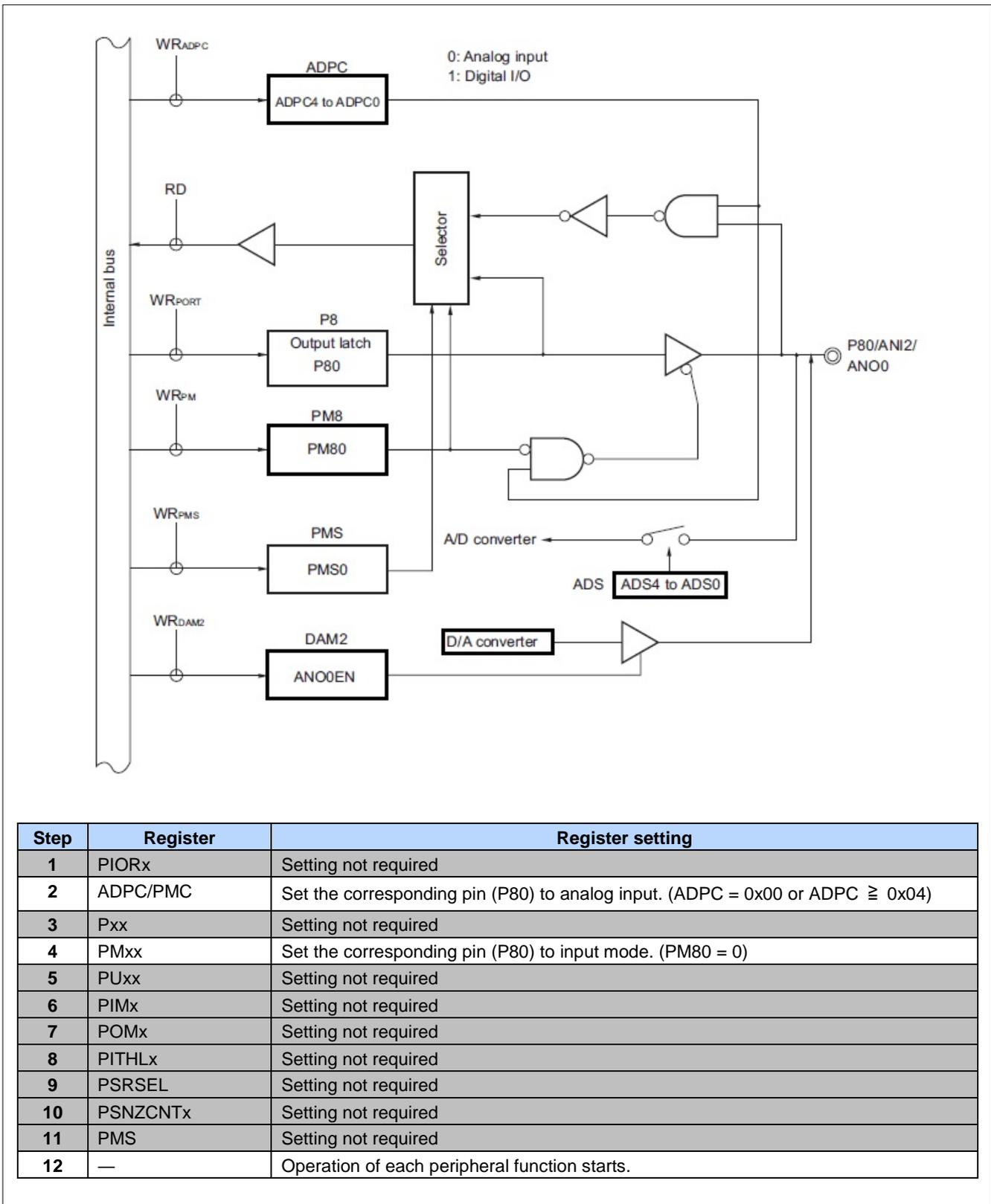

Step	Register	Register setting
1	PIORx	Setting not required
2	ADPC/PMC	Set the corresponding pin (P80) to analog input. (ADPC = 0x00 or ADPC $\geqq$ 0x04)
3	Pxx	Setting not required
4	PMxx	Set the corresponding pin (P80) to input mode. (PM80 = 0)
5	PUxx	Setting not required
6	PIMx	Setting not required
7	POMx	Setting not required
8	PITHLx	Setting not required
9	PSRSEL	Setting not required
10	PSNZCNTx	Setting not required
11	PMS	Setting not required
12	—	Operation of each peripheral function starts.

Figure 26 Setting example of D/A converter output (P80/ANO0)

3.   Cautionary note on setting port-related registers

• To set the peripheral I/O redirection register (PIORx), the corresponding peripheral functions must be stopped
  beforehand [the corresponding bit in PERx register must be set to 0 (stops the input clock supply to modules)].

• When using POMm register by setting POMmn bit to 1 (N-ch open-drain output mode), externally pull up the
  corresponding pin(s).

• If any write access to the port register (Pxx) is executed by using bit manipulation instructions or operations (AND,
  OR instructions) in the following cases, the current pin level (1 or 0) will be stored in a port latch for other bits:
    when the pin is set to input (the corresponding bit in PMxx register is set to 1) and the PMS0 bit in the PMS
    register is set to 1 (reads the output level of the pin).
    Before setting the port-related register, disable interrupts (DI) to avoid a state change of the port while an interrupt
    is handled.

     Example:
                P7 = 0x03;   /* The output latch of P70/P71 is set to 1. */
                PM70 = 0;   /* P70 is set to output mode (outputs "High"). */
                PMS0 = 1;   /* The output level of the pin is read. */
                P70 = 0;   /* The output latch of P70 is set to 0. */ ([NOTE 1])
                PM71 = 0;   /* P71 is set to output mode. */ ([NOTE 2])

     NOTE 1: When the level of the P71 pin is low, the value of the P71 bit is 0.
     NOTE 2: The P71 pin outputs a low level (L) instead of a high level (H) that is set by P7 = 0x03;.

• When no peripheral function is allocated to the corresponding pin by PIORx register, the pin can be used as another
  function (digital I/O, analog input, I/O of a peripheral function).
• It is impossible to simultaneously use multiple functions allocated to one pin.
• The procedures described in this application note are setting examples of the port-related registers. Please carefully
  examine the procedures, values and commands according to your specifications before actually setting the relevant
  registers.

Website and Support

Renesas Electronics Website
    http://www.renesas.com/

Inquiries
    http://www.renesas.com/contact/

Revision History

| Rev. | Date | Description | |
		Page	Summary
1.00	April 30, 2018	-	Initial issue

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.