RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Serial interface UART0 to Serial Array Unit

Introduction

This application note describes how to migrate the Serial interface UART0 of the 78K0/Kx2 to the serial array unit (SAU) of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Serial interface UART0 and Serial array unit

Table 1.1 shows the functions of the Serial interface UART0, and Table 1.2 shows the functions of the serial array unit (SAU).

Table 1.1 Functions of Serial interface UART0

Function	Explanation
Asynchronous serial interface (UART) mode	This is a start-stop synchronization function using two lines: serial data transmission (TxD0) and serial data reception (RxD0) lines.

Table 1.2 Functions of Serial Array Unit (SAU)

Function	Explanation
3-wire serial I/O	This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.
UART	This is a start-stop synchronization function using two lines: serial data transmission (TXD) and serial data reception (RXD) lines.
Simplified I2C (only master function with a single master)	This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA).
LIN Communication (Note)	LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Note. The LIN-bus is accepted in UART2 (channels 0 and 1 of unit 1)

The serial interface UART0 incorporated in the 78K0/Kx2 has one channel of input and output pins for data transfer. Figure 1.1 shows a block diagram of the serial interface UART0.

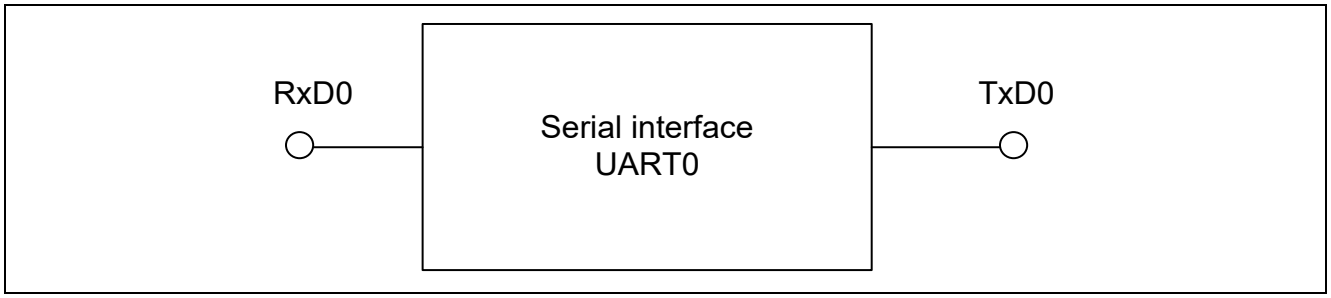

Figure 1.1 Block Diagram of Serial interface UART0

A single serial array unit (SAU) in the RL78/G13 has up to four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I2C communication. UART communication is implemented by two serial channels of SAU.

Figure 1.2 shows a block diagram of the UART in the serial array unit 0 (SAU0) of the RL78/G13.

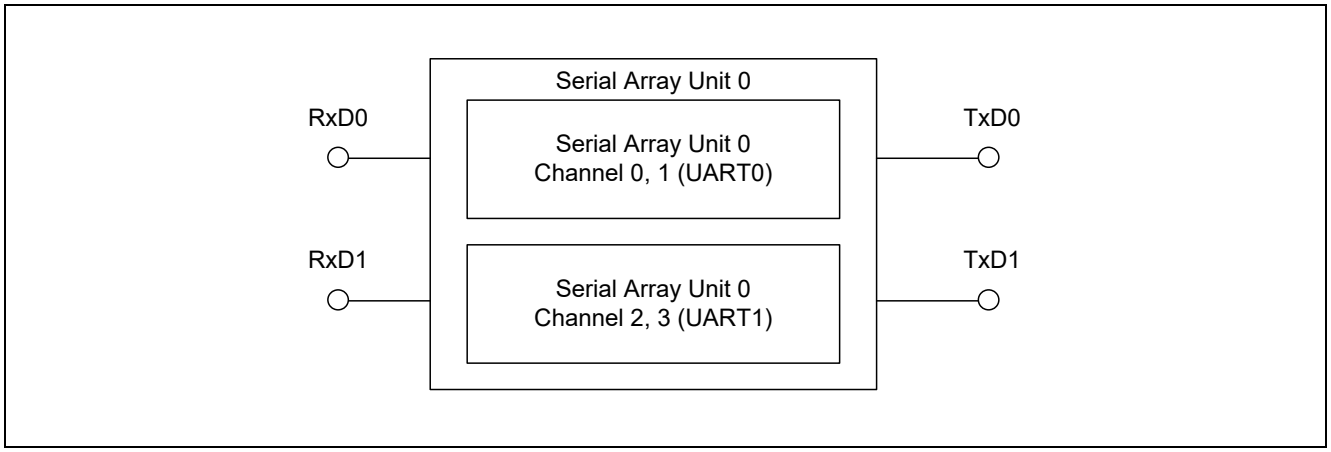

Figure 1.2 Block Diagram of Serial Array Unit 0 (SAU0) UART

Table 1.3 shows the SAU functions corresponding to the Serial interface UART0.

Table 1.3 Correspondence between Functions

78K0/Kx2 Serial interface UART0	RL78/G13 Serial Array Unit (SAU)
-	3-wire serial I/O
Asynchronous serial interface (UART) mode	UART
-	Simplified I^2C

The asynchronous serial interface (UART) mode of the Serial interface UART0 correspond to the UART of the SAU.

2. Difference between Serial interface UART0 and Serial Array Unit

Table 2.1 and Table 2.2 shows the differences between the UART.

Table 2.1 Differences between UART (1/2)

Item	78K0/Kx2 UART0	RL78/G13 Serial Array Unit (SAU) UARTq
Transfer data length	7 bits, 8 bits	7 bits, 8 bits, 9 bits (Note)
Maximum transfer rate	625kbps	5.3Mbps
First bit specification	LSB first	- LSB first - MSB first
Selection of parity bit	- Does not output the parity bit - Outputs 0 parity - Outputs even parity - Outputs odd parity	- Does not output the parity bit - Outputs 0 parity - Outputs even parity - Outputs odd parity
Selection of stop bit	Transmission 1 bit, 2 bits Reception 1 bit	Transmission 1 bit, 2 bits Reception 1 bit
Transfer data reverse function	None	Yes - Non-reverse output, Non-reverse input (default) - Reverse output, Reverse input
Continuous transmission function	None	Yes Use buffer empty interrupt (In Continuous Transmission Mode)
Noise elimination	Data are sampled with the base clock (f_{XCLK0}), and when two sampled values match, the value is determined as the received data.	Data are sampled with the operating clock (f_{MCK}) of the target channel, and when two sampled values match, the value is determined as the received data. Note that the SNFENq0 bit in the NFEN0 register should be set to 1.
Disables operation	ASIM0 register POWER0 = 0	STm register STmn = 1
Enables operation	ASIM0 register POWER0 = 1	SSm register SSmn = 1
Selection of operation mode	- Transmission - Reception - Transmission/reception (Full-duplex operation)	- Transmission - Reception - Transmission/reception (Full-duplex operation)
Transmit shift register	TXS0 register	Lower 8/9 bits of SDRmn register (note)
Receive buffer register	RXB0 register	Lower 8/9 bits of SDRmn register (note)

Note. Only the following UARTs can be specified for the 9-bit data length.

- 20 to 64-pin products: UART0
- 80 to 128-pin products: UART0, UART2

Remarks1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), q: UART number (q = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 2.2 Differences between UART0 (2/2)

Item	78K0/Kx2 UART0	RL78/G13 Serial Array Unit (SAU) UARTq
Data transmission is started	Write transmit data to TXS0 register. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.	Write transmit data to SDRmn register.
Data reception is started	When the start bit has been detected. Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin.	When the start bit has been detected.
Interrupt	Transmission - Completion interrupt request (INTST0) Reception - Reception completion interrupt (INTSR0) - Reception error interrupt (INTSR0) Note that the reception completion interrupt and the reception error interrupt are allocated to the same vector table address.	Transmission - Transfer end or buffer empty interrupt (INTSTq) Reception - Transfer end interrupt (INTSRq) - Communication error occurrence (INTSREq)
Interrupt occur timing	Transmission - After the last stop bit is transmitted. For example, when the stop bit length is set to two bits, an interrupt occurs when the second stop bit is transmitted. Reception - When the stop bit is received (including the case where a parity error or framing error occurs). - When an overrun error occurs.	Single-transmission mode - After the last stop bit is transmitted. Continuous transmission mode - When the transmit data is transferred from the SDRmn register to the shift register. Reception - When the stop bit is received (including the case where a parity error or framing error occurs). - When an overrun error occurs.
Reception errors	- Parity error - Framing error - Overrun error	- Parity error - Framing error - Overrun error
Clearing the error flag	Read ASIS0 register	Write 1 to the FECTmn, PECTmn, and OVCTmn bits in the SIRmn register.
Serial data input pin	RxD0 pin	RxDq pin
Serial data output pin	TxD0 pin	TxDq pin

Remarks1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), q: UART number (q = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

3. Register Compatibilities

Table 3.1 to Table 3.3 compares the registers for the 78K0/Kx2 Serial interface UART0 and the registers for the RL78/G13 Serial Array Unit used as UART.

Table 3.1 Comparison between Registers (1/3)

Item	78K0/Kx2	RL78/G13
Clock supply to serial array unit	None	PER0 register SAUmEN bit
Disables operation	ASIM0 register POWER0 bit	STm register STmn bit
Enables operation	ASIM0 register POWER0 bit	SSm register SSmn bit
Indication of operation enable/stop status	None	SEm register SEmn bit
Mode control Selection	ASIM0 register TXE0 bit, RXE0 bit	SCRmn register TXEmn bit (Note1), RXEmn bit (Note1)
Setting of parity bit	ASIM0 register PS01 bit, PS00 bit	SCRmn register PTCmn1 bit, PTCmn0 bit
Selection of data transfer sequence in CSI and UART modes	None	SCRmn register DIRmn bit
Setting data length of transmit/receive data	ASIM0 register CL0 bit	SCRmn register DLSmn1 bit (Note2), DLSmn0 bit
Setting of stop bits of transmit data	ASIM0 register SL0 bit	SCRmn register SLCmn1 bit (Note3), SLCmn0 bit
Status flag indicating parity error	ASIS0 register PE0 bit	SSRmn register PEFmn bit (Note4)
Status flag indicating framing error	ASIS0 register FE0 bit	SSRmn register FEFmn bit (Note5)
Status flag indicating overrun error	ASIS0 register OVE0 bit	SSRmn register OVFmn bit (Note5)
Transmit shift register	TXS0 register	Lower 8/9 bits (Note3) of SDRmn register (Note6)
Receive buffer register	RXB0 register	Lower 8/9 bits (Note4) of SDRmn register (Note6)

Note1. UART Transmission: TXEmn = 1, RXEmn = 0 (mn = 00, 02, 10, 12)
UART Reception: TXEmn = 0, RXEmn = 1 (mn = 01, 03, 11, 13)

Note2. UART0 (SCR00 and SCR01 registers) and UART2 (SCR10 and SCR11 registers) for 80 to 128-pins products only. Others are fixed to 1.

Note3. mn = 00, 02, 10, 12 (Even channel is UART transmission function)

Note4. mn = 01, 03, 11, 13 (Odd channel is UART reception function)

Note5. In the UART mode, this flag is valid only during reception.

Note6. Only the following UARTs can be specified for the 9-bit data length.

- 20 to 64-pin products: UART0
- 80 to 128-pin products: UART0, UART2

Remarks1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), q: UART number (q = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.2 Comparison between Registers (2/3)

Item	78K0/Kx2	RL78/G13
Base clock selection	BRGC0 register TPS01 bit, TPS00 bit	SPSm register PRSmk3 - PRSmk0 bit SMRmn register CKSmn bit, CCSmn bit
Selection of 5-bit counter output clock	BRGC0 register MDL04 - MDL00 bit	None
Transfer clock setting by dividing the operation clock	None	Upper 7 bits of SDRmn register
Selection of transfer clock (f_{TCLK}) of channel n	None	SMRmn register Set CCSmn bit to 0
Selection of start trigger source	None	SMRmn register STSmn bit
Controls inversion of level of receive data of channel n in UART mode	None	SMRmn register SISmn0 bit (Note)
Setting of operation mode of channel n	None	SMRmn register Set MDmn2 bit to 0, MDmn1 bit to 1
Selection of interrupt source of channel n	None	SMRmn register MDmn0 bit
Selection of data and clock phase in CSI mode	None	SCRmn register Set DAPmn bit to 0, CKPmn bit to 0
Mask control of error interrupt signal (INTSREq)	None	SCRmn register EOCmn bit
Clear trigger of framing error	None	SIRmn register FECTmn bit
Clear trigger of parity error flag	None	SIRmn register PECTmn bit
Clear trigger of overrun error flag	None	SIRmn register OVCTmn bit
Communication status indication flag	None	SSRmn register TSFmn bit
Buffer register status indication flag	None	SSRmn register BFFmn bit

Note. mn = 01, 03, 11, 13 (Odd channel is UART reception function)

Remarks1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), q: UART number (q = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.3 Comparison between Registers (3/3)

Item	78K0/Kx2	RL78/G13
Serial output enable/stop	None	SOEm register SOEmn bit
Serial clock output	None	SOm register CKOmn bit
Serial data output	None	SOm register SOmn bit
Selects inversion of the level of the transmit data of channel n in UART mode	None	SOLm register SOLmn bit (Note)
Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode	None	SSCm register SSECm bit
Setting of the SNOOZE mode	None	SSCm register SWCm bit
Switching channel 7 input of timer array unit	None	ISC register Set ISC1 bit to 0
Switching external interrupt (INTP0) input	None	ISC register Set ISC0 bit to 0
Use of noise filter	None	NFEN0 register Set SNFENq0 bit to 1

Note. mn = 00, 02, 10, 12 (Even channel is UART transmission function)

Remarks1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), q: UART number (q = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

4. Sample Code for Serial Array Unit

The sample code for the serial array unit is explained in the following application notes.

- RL78/G13 Serial Array Unit (UART Communication) CC-RL (R01AN2517)
- RL78/G13 DMA Controller (UART Sequential Reception) CC-RL (R01AN2835)
- RL78/G13 Self-Programming (Received Data via UART) CC-RL (R01AN2761)
- RL78/G13 Low-power Consumption Operation (UART in SNOOZE Mode) CC-RL (R01AN2713)

5. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.24, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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