RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RE to Real-time Clock

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Abstract

This document describes how to migrate from timer RE in the R8C/36M Group to the real-time clock (RTC) in RL78/G14.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences Between the R8C/36M Group and RL78/G14

1.1 Differences in Function Overview

Table 1.1 lists the differences between timer RE in the R8C/36M Group and the RTC in RL78/G14.

Table 1.1 Differences

Item	R8C/36M Group	RL78/G14
Modes	• Real-time clock mode • Output compare mode	• Year, month, week, day hour, minute, and second counters • Constant-period interrupt function
Count sources	• f2 • fC • f4 • f8 • fC4 (Note 1)	• f_{IL} (Note 2) • f_{SUB} (Note 3)
Reset	Yes	No
Transition to standby mode after operation starts	No	Yes

Notes: 1. Only fC4 can be used in real-time clock mode.
2. The constant-period interrupt function can be used only when f_{IL} is selected as the count source.
3. Years, months, weeks, days, hours, minutes, and seconds can be counted only when f_{SUB} is selected as the count source.

1.2 Differences Between Real-time Clock Mode and Counters

The year, month, week, day, hour, minute, and second counters in RL78/G14 correspond to real-time clock mode in the R8C/36M Group.

Table 1.2 lists the differences between real-time clock mode and the counters.

Table 1.2 Differences Between Real-time Clock Mode and Counters

Item	R8C/36M Group	RL78/G14
Mode	Real-time clock mode	Year, month, week, day, hour, minute, and second counters
Count source	fC4	f_{SUB} (Note)
Interrupt request generation timing	• Update second data • Update minute data • Update hour data • Update day of week data • When day of week data is set to 000b (Sunday)	• Once every 0.5 seconds (synchronized with counting up seconds) • Once per second (same time as counting up seconds) • Once per minute (at 00 seconds every minute) • Once per hour (at 00 minutes and 00 seconds every hour) • Once per day (at 00 hours, 00 minutes, and 00 seconds every day) • Once per month (on the 1st of every month at 00 hours, 00 minutes, and 00 seconds a.m.)
Alarm function	No	Yes
Watch error correction	No	Yes
Output pin	TREO	RTC1HZ
Output pin functions	• Programmable I/O ports • f2 • fC • f4 • f8 • 1 Hz	1Hz

Note: Years, months, weeks, days, hour, minutes, and seconds can be counted only when f_{SUB} is selected as the count source.

1.3 Differences Between Output Compare Mode and Constant-period Interrupt Function

The constant-period interrupt function in RL78/G14 corresponds to output compare mode in the R8C/36M Group. Table 1.3 lists the differences between output compare mode and the constant-period interrupt function.

Table 1.3 Differences Between Output Compare Mode and the Constant-period Interrupt Function

Item	R8C/36M Group	RL78/G14
Mode	Output compare mode	Constant-period interrupt function
Count sources	• f4 • f8 • f32 • fC4	f_{IL}
Count operations	• Increment • When the 8-bit counter value matches the TREMIN register value, the counter value returns to 00h and the count continues. The count value is retained while count stops.	• Count up
Use of 4-bit counter	Yes	No
Count period	• When RCS2 = 0 (4-bit counter is not used) 1/fi × 2 × (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi ×2 × (n+1) fi: Frequency of count source n: Setting value of TREMIN register	Constant-period (the value selected by the RTCC0 register) × f_{SUB}/f_{IL}
Interrupt request generation timing	When the 8-bit counter value matches the TREMIN register value	Count period
Output pin	TREO	No
Output pin functions	• Programmable I/O ports • f2, fC, f4, or f8 • Compare output	No
Compare output function	Yes	No

1.4 Assigned I/O Pins

Table 1.4 and Table 1.5 list the I/O pins assigned for use in timer RE in the R8C/36M Group, and the RTC in RL78/G14.

Table 1.4 R8C/36M Group I/O Pins

Pin Name	Assigned Pins	I/O
TREO	P0_4, or P6_0	Output

Table 1.5 RL78/G14 Group I/O Pins

Pin Name	Assigned Pins	I/O
RTC1HZ	P30	Output

2. Register Compatibility

Register compatibility between timer RE in the R8C/36M Group and the RTC in RL78/G14 is listed in Table 2.1 and Table 2.2.

Table 2.1 Register Compatibility (1/2)

Item	R8C/36M Group	RL78/G14
1st digit of second count	• TRESEC register Bits SC00 to SC03	• SEC register
2nd digit of second count	• TRESEC register Bits SC10 to SC12	• SEC register
Count data register	• TRESEC register	N/A
1st digit of minute count	• TREMIN register Bits MN00 to MN03	• MIN register
2nd digit of minute count	• TREMIN register Bits MN10 to MN12	• MIN register
Compare data register	• TREMIN register	• RTCC0 register Bits CT0 to CT2
1st digit of hour count	• TREHR register Bits HR00 to HR03	• HOUR register
2nd digit of hour count	• TREHR register Bits HR10 and HR11	• HOUR register
Day of week count	• TREWK register Bits WK0 to WK2	• WEEK register
Busy flags	• BSY bit in the TRESEC register • BSY bit in the TREMIN register • BSY bit in the TREHR register • BSY bit in the TREWK register	N/A
Count status flag	• TRECR1 register TCSTF bit	• RTCC1 register RWST bit
TREO pin output enable	• TRECR1 register TOENA bit	N/A
Interrupt request timing	• TRECR1 register INT bit	N/A
Reset setting	• TRECR1 register TRERST bit	N/A
A.m./p.m. select	• TRECR1 register PM bit	N/A
Operating mode select	• TRECR1 register H12_H24 bit	• RTCC0 register AMPM bit
Count start	• TRECR1 register TSTART bit	• RTCC0 register RTCE bit

Table 2.2 Register Compatibility (2/2)

Item	R8C/36M Group	RL78/G14
Periodic interrupt triggered every second enable/disable	• TRECR2 register SEIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every minute enable/disable	• TRECR2 register MNIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every hour enable/disable	• TRECR2 register HRIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every day enable/disable	• TRECR2 register DYIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every week enable/disable	• TRECR2 register WKIE bit	N/A
Compare match interrupt enable	• TRECR2 register COMIE bit	N/A
Count source select	• TRECSR register Bits RCS0 and RCS1	• OSMC register WUTMMCK0 bit
Use of 4-bit counter	• TRECSR register RCS2 bit	N/A
Real-time clock mode select	• TRECSR register RCS3 bit	N/A
Clock output select	• TRECSR register Bits RCS4 and RCS5	N/A
TREO pin select	• TIMSR register TREOSEL0 bit	N/A
RTC1HZ output control	N/A	• RTCC0 register RCLOE1 bit
Constant-period (0.5 second) interrupt enable/disable	N/A	• RTCC0 register Bits CT0 to CT2
Constant-period (month) interrupt enable/disable	N/A	• RTCC0 register Bits CT0 to CT2
Alarm control	N/A	• RTCC1 register WALE bit
Alarm interrupt (INTRTC) function control	N/A	• RTCC1 register WALIE bit
Alarm detection status flag	N/A	• RTCC1 register WAFG bit
Constant-period interrupt status flag	N/A	• RTCC1 register RIFG bit
RTC wait control	N/A	• RTCC1 register RWAIT bit
Day count	N/A	• DAY register
Month count	N/A	• MONTH register
Year count	N/A	• YEAR register
Watch error correction timing setting	N/A	• SUBCUD register DEV bit
Watch error correction value setting	N/A	• SUBCUD register F6 bit
Alarm minute setting	N/A	• ALARMWM register
Alarm hour setting	N/A	• ALARMWH register
Alarm day of week setting	N/A	• ALARMWW register

3. Comparison of Real-time Clock Mode and Counters Settings

3.1 Mode Select

3.1.1 R8C/36M Group

To use timer RE in real-time clock mode, set the RCS3 bit in the TRECSR register to 1.

3.1.2 RL78/G14

To use the RTC as counters for the year, month, week, day, hour, minute, and second, set the WUTMMCK0 bit in the OSMC register to 0 (subsystem clock (f_{SUB})).

Table 3.1 lists the functions of the WUTMMCK0 bit.

Table 3.1 WUTMMCK0 Bit Functions

WUTMMCK0 Bit	Selection of Operation Clock for Real-time Clock, 12-bit Interval Timer, and Timer RJ
0	• The subsystem clock is selected as the operation clock for the real-time clock and the 12-bit interval timer. The low-speed on-chip oscillator cannot be selected as the count source for timer RJ.
1	• The low-speed on-chip oscillator clock is selected as the operation clock for the real-time clock and the 12-bit interval timer. Either the low-speed on-chip oscillator or the subsystem clock can be selected as the count source for timer RJ.

3.2 Operating Clock

3.2.1 R8C/36M Group

The timer RE operating clock is set to fC4. In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week.

3.2.2 RL78/G14

Set the subsystem clock (f_{SUB}) as the RTC operation clock (f_{RTC}). The RTC counts years, months, days of the week, day, hours, minutes, and seconds only when f_{SUB} is selected. Set the WUTMMCK0 bit in the OSMC register to select the operation clock. Refer to Table 3.1 for the functions of the WUTTMMCK0 bit.

3.3 Count Start

3.3.1 R8C/36M Group

Timer RE starts counting by setting the TSTART bit in the TRECR1 register to 1 (count starts), and the TCSTF bit in the TRECR1 register is set to 1 (count in progress). Table 3.2 lists the functions of the TSTART bit, and Table 3.3 lists the functions of the TCSTF bit.

Table 3.2 TSTART Bit Functions

TSTART Bit	Timer RE Count Start Bit
0	Count stops
1	Count starts

Table 3.3 TCSTF Bit Functions

TCSTF Bit	Timer RE Count Status Flag
0	Count stopped
1	Count in progress

3.3.2 RL78/G14

The RTC starts counting by setting the RTCE bit in the RTCC0 register to 1 (starts counter operation). Table 3.4 lists the functions of the RTCE bit.

Table 3.4 RTCE Bit Functions

RTCE Bit	Real-time Clock Operation Control
0	Stops counter operation
1	Starts counter operation

3.4 Count Stop

3.4.1 R8C/36M Group

Timer RE stops counting by setting the TSTART bit in the TRECR1 register to 0 (count stops), and the TCSTF bit is set to 0 (count stopped). Refer to Table 3.2 for the functions of the TSTART bit, and Table 3.3 for the functions of the TCSTF bit.

3.4.2 RL78/G14

The RTC stops counting by setting the RTCE bit in the RTCC0 register to 0 (stops counter operation). Refer to Table 3.4 for the functions of the RTCE bit.

3.5 Timer Read

3.5.1 R8C/36M Group

The counter value can be obtained by reading registers TRESEC, TREMIN, TREHR, and TREWK. Make sure to read these registers when their BSY bits are 0 (data is not being updated). Table 3.5 lists the functions of the BSY bit.

Table 3.5 BSY Bit Functions

BSY Bit	Timer RE Busy Flag
0	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated
1	

3.5.2 RL78/G14

The counter value can be obtained by reading registers SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR. Set the RWAIT bit in the RTCC1 register to 1, and verify that the RWST bit in the RTCC1 register is set to 1 before reading these registers. Perform the processing to set the RWAIT bit to 1 to clear the bit to 0 within one second.

Table 3.6 lists the functions of the RWAIT bit. Table 3.7 lists the functions of the RWST bit.

Table 3.6 RWAIT Bit Functions

RWAIT Bit	Wait Control of Real-time Clock
0	Sets counter operation
1	Stops SEC to YEAR counters. Mode to read or write counter value

Table 3.7 RWST Bit Functions

RWST Bit	Wait Status Flag of Real-time Clock
0	Counter is operating
1	Mode to read or write counter value

3.6 Timer Count Value Write

3.6.1 R8C/36M Group

Write to registers TRESEC, TREMIN, TREHR, and TREWK when bits TSTART and TCSTF in the TRECR1 register are 0 (count stops).

3.6.2 RL78/G14

Write to registers SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR after setting the RWAIT bit in the RTCC1 register to 1, and verifying that the RWST bit in the RTCC1 register is set to 1. Clear the RWAIT bit to 0 after writing is completed. Perform the processing to set the RWAIT bit to 1 to clear the bit to 0 within one second.

Refer to Table 3.6 for the functions of the RWAIT bit, and Table 3.7 for the functions of the RWST bit.

To rewrite registers SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR while the counter is operating, set the RTCMK bit in the MK1H register to 1 (interrupt servicing disabled). After rewriting the RTCMK bit, set bits WAFG and RIFG in the RTCC1 register and the RTCIF bit in the 1F1H register to 0.

Table 3.8 lists the functions of the RTCMK bit.

Table 3.8 RTCMK Bit Functions

RTCMK Bit	Interrupt Servicing Control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Table 3.9 lists the functions of the WAFG bit. Table 3.10 lists the functions of the RIFG bit. Table 3.11 lists the functions of the RTCIF bit.

Table 3.9 WAFG Bit Functions

WAFG Bit	Alarm Detection Status Flag
0	Alarm mismatch
1	Detection of matching of alarm

Table 3.10 RIFG Bit Functions

RIFG Bit	Constant-period Interrupt Status Flag
0	Constant-period interrupt is not generated
1	Constant-period interrupt is generated

Table 3.11 RTCIF Bit Functions

RTCIF Bit	Interrupt Servicing Control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

3.7 Output Pins

3.7.1 R8C/36M Group

The TREO pin is used as a programmable I/O port, or can output f2, fC, f4, or f8. Set bits RCS4 to RCS6 in the TRECSR register to output clocks. Set the TOENA bit in the TRECR1 register to enable TREO pin output.

Table 3.12 lists the functions of bits RCS4 to RCS6. Table 3.13 lists the functions of the TOENA bit.

Table 3.12 RCS4 to RCS6 Bit Functions

RCS6 Bit	RCS5 Bit	RCS4 Bit	Clock Output Select Bit
0	0	0	f2
0	0	1	fC
0	1	0	f4
0	1	1	1 Hz
1	0	0	f8
Other than above			Do not set.

Table 3.13 TOENA Bit Functions

TOENA Bit	TREO Pin Output Enable Bit
0	Disable clock output
1	Enable clock output

Set the TREOSEL0 bit in the TIMSR register to select the port of the TREO pin. Table 3.14 lists the functions of the TREOSEL0 bit.

Table 3.14 TREOSEL0 Bit Functions

TREOSEL0 Bit	TREO Pin Select Bit
0	P0_4 pin assigned
1	P6_0 pin assigned

3.7.2 RL78/G14

The RTC1HZ pin outputs a 1-Hz signal. Set the RCLOE1 bit in the RTCC0 register to enable or disable output from the RTC1HZ pin. Table 3.15 lists the functions of the RCLOE1 bit.

Table 3.15 RCLOE1 Bit Functions

RCLOE1 Bit	RTC1HZ Pin Output Control
0	Disables output of the RTC1HZ pin (1 Hz)
1	Enables output of the RTC1HZ pin (1 Hz)

3.8 Interrupts

3.8.1 R8C/36M Group

Enable or disable the timer RE interrupts by the TRECR2 register. Table 3.16 lists the compatibility between interrupt sources and interrupt enable bits. Table 3.17 lists the functions of the periodic interrupts of the TRECR2 register.

Table 3.16 Compatibility Between Interrupt Sources and Interrupt Enable Bits

Interrupt Sources	Interrupt Enable Bits
Periodic interrupt triggered every second	SEIE
Periodic interrupt triggered every minute	MNIE
Periodic interrupt triggered every hour	HRIE
Periodic interrupt triggered every day	DYIE
Periodic interrupt triggered every week	WKIE

Table 3.17 SEIE, MNIE, HRIE, DYIE, WKIE Bit Functions

Periodic Interrupts (Note)	SEIE, MNIE, HRIE, DYIE, WKIE Periodic Interrupt Enable Bit
0	Disable periodic interrupt
1	Enable periodic interrupt

Note: SEIE, MNIE, HRIE, DYIE, WKIE

3.8.2 RL78/G14

Set the constant-period interrupt (INTRTC) by bits CT0 to CT2 in the RTCC0 register. Table 3.18 lists the functions of bits CT0 to CT2.

Table 3.18 CT0 to CT2 Bit Functions

CT2 bit	CT1 bit	CT0 bit	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once every 0.5 seconds (synchronized with counting up seconds)
0	1	0	Once per second (same time as counting up seconds)
0	1	1	Once per minute (second 00 every minute)
1	0	0	Once per hour (minute 00 and second 00 every hour)
1	0	1	Once per day (hour 00, minute 00, and second 00 every day)
1	1	×	Once per month (date 1, hour 00 a.m., minute 00, and second 00 every month)

×: Don't care.

4. Comparison of Output Compare Mode and Constant-period Interrupt Settings

4.1 Mode Select

4.1.1 R8C/36M Group

To use timer RE in output compare mode, set the RCS3 bit in the TRECSR register to 0.

4.1.2 RL78/G14

The RTC can use the constant-period interrupt function only when the low-speed on-chip oscillator clock is selected as the operating clock. Set the WUTMMCK0 bit in the OSMC register when not using f_{SUB}. Refer to Table 3.1 for the functions of the WUTMMCK0 bit.

4.2 Count Source

4.2.1 R8C/36M Group

Set bits RCS0 and RCS1 in the TRECSR register to select the count source. Table 4.1 lists the functions of bits RCS0 and RCS1.

Table 4.1 RCS0 and RCS1 Bit Functions

RCS0 Bit	RCS1 Bit	Count Source Select Bit
0	0	f4
0	1	f8
1	0	f32
1	1	fC4

4.2.2 RL78/G14

Set the WUTMMCK0 bit in the OSMC register to select the operating clock. Refer to Table 3.1 for the functions of the WUTMMCK0 bit.

4.3 Count Start

4.3.1 R8C/36M Group

Timer RE starts counting by setting the TSTART bit in the TRECR1 register to 1 (count starts), and the TCSTF bit in the TRECR1 register is set to 1 (count in progress). Refer to Table 3.2 for the functions of the TSTART bit, and Table 3.3 for the functions of the TCSTF bit.

4.3.2 RL78/G14

The constant-period interrupt count starts by setting the RTCE bit in the RTCC0 register to 1 (starts counter operation). Table 3.4 lists the functions of the RTCE bit.

4.4 Count Stop

4.4.1 R8C/36M Group

Timer RE stops counting by setting the TSTART bit in the TRECR1 register to 0 (count stops), and the TCSTF bit is set to 0 (count stops). Refer to Table 3.2 for the functions of the TSTART bit, and Table 3.3 for the functions of the TCSTF bit.

4.4.2 RL78/G14

The constant-period interrupt count stops by setting the RTCE bit in the RTCC0 register to 0 (stops counter operation). Refer to Table 3.4 for the functions of the RTCE bit.

4.5 Timer Read

4.5.1 R8C/36M Group

Read the TRESEC register to obtain the counter value, and read the TREMIN register to obtain the compare value.

4.5.2 RL78/G14

Read bits CT0 to CT2 in the RTCC0 register to verify the counter value. Refer to Table 3.18 for the functions of bits CT0 to CT2. When f_{IL} is selected (constant-period interrupt function), the constant-period interrupt interval is calculated with the constant-period (the value selected with the RTCC0 register) × f_{SUB}/f_{IL}.

4.6 Timer Write

4.6.1 R8C/36M Group

Write the compare value to the TREMIN register when bits TSTART and TCSTF in the TRECR1 register are 0 (count stops). The counter value cannot be written to the TRESEC register.

4.6.2 RL78/G14

Set the counter value by bits CT0 to CT2 in the RTCC0 register. Refer to Table 3.18 for the functions of bits CT0 to CT2. The constant-period interrupt interval is calculated with the constant-period (the value selected with the RTCC0 register) × f_{SUB}/f_{IL}.

4.7 Output Pins

4.7.1 R8C/36M Group

The TREO pin is used as a programmable I/O port, and can output f2, fC, f4, or f8. Set bits RCS4 to RCS6 in the TRECSR register to output clocks. Set the TOENA bit in the TRECR1 register to enable the TREO pin output.

Table 4.2 lists the functions of bits RCS4 to RCS6. Refer to Table 3.13 for the functions of the TOENA bit.

Table 4.2 RCS4 to RCS6 Bit Functions

RCS6 Bit	RCS5 Bit	RCS4 Bit	Clock Output Select Bit
0	0	0	f2
0	0	1	fC
0	1	0	f4
1	0	0	f8
1	1	0	Compare output
Other than above			Do not set.

Set the TREOSEL0 bit in the TIMSR register to select the port of the TREO pin. Refer to Table 3.14 for the functions of the TREOSEL0 bit.

4.7.2 RL78/G14

RL78/G14 does not have output pins for the constant-period interrupt function.

4.8 Interrupts

4.8.1 R8C/36M Group

Enable or disable the compare match interrupt by the COMIE bit in the TRECR2 register. Table 4.3 lists the functions of the COMIE bit.

Table 4.3 COMIE Bit Functions

COMIE Bit	Compare Match Interrupt Enable Bit
0	Disable compare match interrupt
1	Enable compare match interrupt

4.8.2 RL78/G14

Refer to 3.8.2 RL78/G14 for details on enabling the constant-period interrupt.

5. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware Rev.2.00 (R01UH0186EJ)

R8C/36M Group User's Manual: Hardware Rev.1.00 (R01UH0259EJ)

The latest versions can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RE to Real-time Clock

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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