

## RX111 Group

### Initial Setting

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#### Abstract

This document describes settings required after a reset such as clock settings, stop processing for active peripheral functions after a reset, and nonexistent port initialization according to usage conditions selected in the header files.

#### Products

- RX111 Group 64-pin package with a ROM size between 16 KB and 128 KB
- RX111 Group 48-pin package with a ROM size between 16 KB and 128 KB
- RX111 Group 40-pin package with a ROM size between 16 KB and 64 KB
- RX111 Group 36-pin package with a ROM size between 16 KB and 64 KB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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## 1. Specifications

In the sample code, peripheral functions operating after a reset are stopped, and nonexistent port and clock settings are configured. The application note assumes processing at power-on (cold start).

### 1.1 Stopping Peripheral Functions Operating after a Reset

Some peripheral functions operate at power-on, and the module-stop function is disabled for others. These include the DTC and RAM0. Although the sample code includes processing for stopping these peripheral functions, it is not executed in the sample code. Change the constant as required to execute processing.

### 1.2 Configuring Nonexistent Ports

Port direction registers which have nonexistent ports need to be specified with determined values. In the sample code, initial values are set for port direction registers in 64-pin products. Change the values according to the product used.

### 1.3 Setting Clocks

#### 1.3.1 Overview

Clocks are configured in the following steps:

1. Sub-clock setting (including the associated RTC settings)
2. Main clock setting
3. PLL clock setting
4. HOCO clock setting
5. System clock switching

In this application note, the clock settings are switched by changing the constants defined in `r_init_clock.h`.

In the sample code, the main clock is used as the system clock, and the sub-clock and RTC are not used. Change the constant to select the required clock setting.

#### 1.3.2 Clock Specifications Used in the Sample Code

Table 1.1 lists the Clock Specifications Used in the Sample Code. Values such as the oscillation stabilization time are calculated using values listed in Table 1.1.

**Table 1.1 Clock Specifications Used in the Sample Code**

| Clock                                        | Oscillation Frequency     | Oscillation Stabilization Time | Remarks             |
|----------------------------------------------|---------------------------|--------------------------------|---------------------|
| Crystal/ceramic resonator for the main clock | 16 MHz                    | 4.2 ms <sup>(2)</sup>          | Crystal used        |
| Crystal for the sub-clock                    | 32.768 kHz <sup>(1)</sup> | 1.3 sec. <sup>(2)</sup>        | For low clock loads |
| PLL clock                                    | 48 MHz <sup>(1)</sup>     | 50 $\mu$ s <sup>(3)</sup>      |                     |
| HOCO clock                                   | 32 MHz <sup>(1)</sup>     | 56 $\mu$ s <sup>(3)</sup>      |                     |

Notes:

1. The clock is disabled in the sample code.
2. The oscillation stabilization time of a crystal/ceramic resonator differs depending on the wiring pattern, conditions of oscillation parameters, and other settings in the user system. Contact the crystal/ceramic resonator manufacturer to evaluate the user system and provide an appropriate oscillation stabilization time.
3. Refer to the Electrical Characteristics in the User's Manual: Hardware.

### 1.3.3 Selecting Clocks

In the sample code, users can select the system clock source, whether clocks are oscillating or stopped, and other settings by changing constants defined in `r_init_clock.h`. Refer to Table 4.8 and Table 4.9 for constants that can be changed.

Table 1.2 lists Examples of Clock Selections and Table 1.3 lists Examples of the Sub-Clock and RTC Selections.

**Table 1.2 Examples of Clock Selections**

| No.                          |             | 1                         | 2                         | 3                         | 4                         |
|------------------------------|-------------|---------------------------|---------------------------|---------------------------|---------------------------|
| System clock                 |             | Main clock                | PLL                       | HOCO                      | Sub-clock                 |
| PLL clock                    |             | Stopped                   | Oscillating               | Stopped                   | Stopped                   |
| Main clock                   |             | Oscillating               | Oscillating               | Stopped                   | Stopped                   |
| HOCO clock                   |             | Stopped                   | Stopped                   | Oscillating               | Stopped                   |
| Sub-clock                    |             | Stopped <sup>(1)</sup>    | Stopped <sup>(1)</sup>    | Stopped <sup>(1)</sup>    | Oscillating               |
| Operating power control mode |             | High-speed operating mode | High-speed operating mode | High-speed operating mode | High-speed operating mode |
| Constants                    | SEL_SYSCCLK | CLK_MAIN                  | CLK_PLL                   | CLK_HOCO                  | CLK_SUB                   |
|                              | SEL_PLL     | B_NOT_USE                 | B_USE                     | B_NOT_USE                 | B_NOT_USE                 |
|                              | SEL_MAIN    | B_USE                     | B_USE                     | B_NOT_USE                 | B_NOT_USE                 |
|                              | SEL_HOCO    | B_NOT_USE                 | B_NOT_USE                 | B_USE                     | B_NOT_USE                 |
|                              | SEL_SUB     | B_NOT_USE <sup>(1)</sup>  | B_NOT_USE <sup>(1)</sup>  | B_NOT_USE <sup>(1)</sup>  | B_USE                     |
|                              | REG_OPCCR   | OPCM_HIGH                 | OPCM_HIGH                 | OPCM_HIGH                 | OPCM_HIGH                 |

Note:

1. When not using the sub-clock for the system clock, clock frequency accuracy measurement circuit (CAC), or the realtime clock (RTC), set the value of the SEL\_SUB constant to B\_NOT\_USE. When using the sub-clock, refer to Table 1.3.

**Table 1.3 Examples of the Sub-Clock and RTC Selections**

| Pattern                                         | Sub-Clock | System Clock <sup>(2)</sup> |                                    | RTC               |                                    |
|-------------------------------------------------|-----------|-----------------------------|------------------------------------|-------------------|------------------------------------|
|                                                 | Crystal   | Used/<br>Not Used           | Value in<br>SEL_SUB <sup>(1)</sup> | Used/<br>Not Used | Value in<br>SEL_RTC <sup>(1)</sup> |
| Sub-clock not used                              | None      | —                           | B_NOT_USE                          | —                 | B_NOT_USE                          |
| Sub-clock used as the system clock              | Used      | Used                        | B_USE                              | Not used          | B_NOT_USE                          |
| Sub-clock used for the RTC                      | Used      | Not used                    | B_NOT_USE                          | Used              | B_USE                              |
| Sub-clock used for the system clock and the RTC | Used      | Used                        | B_USE                              | Used              | B_USE                              |

Notes:

1. When setting B\_USE to both the SEL\_SUB and SEL\_RTC constants or either of them, the sub-clock oscillates.
2. The sub-clock oscillation is controlled by bits SOSCCR.SOSTP and RCR3.RTCEN. When the sub-clock is used as the system clock, it is controlled by the SOSCCR.SOSTP bit, and when the sub-clock is used as the RTC count source, it is controlled by the RCR3.RTCEN bit. Therefore the initial setting for the sub-clock differs depending on whether the sub-clock is used as the system clock or not. Also the sub-clock starts oscillating at power-on. Thus processing to stop the sub-clock is performed even when the sub-clock is not used.

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

**Table 2.1 Operation Confirmation Conditions**

| Item                               |                                                     | Contents                                                                                                                                                                                                                                                                                                                                                                       |
|------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCU used                           |                                                     | R5F51115ADFM (RX111 Group)                                                                                                                                                                                                                                                                                                                                                     |
| Operating frequencies              | When the main clock is selected as the system clock | <ul style="list-style-type: none"> <li>- Main clock: 16 MHz</li> <li>- Sub-clock: 32.768 kHz (stopped when the sub-clock is not used)</li> <li>- LOCO: 4 MHz</li> <li>- System clock (ICLK): 16 MHz (main clock divided by 1)</li> <li>- Peripheral module clock B (PCLKB): 16 MHz (main clock divided by 1)</li> </ul>                                                        |
|                                    | When the PLL clock is selected as the system clock  | <ul style="list-style-type: none"> <li>- Main clock: 16 MHz</li> <li>- Sub-clock: 32.768 kHz (stopped when the sub-clock is not used)</li> <li>- PLL: 48 MHz (main clock divided by 2 and multiplied by 6)</li> <li>- LOCO: 4 MHz</li> <li>- System clock (ICLK): 24 MHz (PLL divided by 2)</li> <li>- Peripheral module clock B (PCLKB): 24 MHz (PLL divided by 2)</li> </ul> |
|                                    | When the HOCO clock is selected as the system clock | <ul style="list-style-type: none"> <li>- Sub-clock: 32.768 kHz (stopped when the sub-clock is not used)</li> <li>- LOCO: 4 MHz</li> <li>- HOCO: 32 MHz</li> <li>- System clock (ICLK): 32 MHz (HOCO divided by 1)</li> <li>- Peripheral module clock B (PCLKB): 32 MHz (HOCO divided by 1)</li> </ul>                                                                          |
| Operating voltage                  |                                                     | 3.3 V                                                                                                                                                                                                                                                                                                                                                                          |
| Integrated development environment |                                                     | Renesas Electronics Corporation<br>e <sup>2</sup> studio Version 7.6.0                                                                                                                                                                                                                                                                                                         |
| C compiler                         |                                                     | Renesas Electronics Corporation<br>C/C++ Compiler Package for RX Family V.3.01.00                                                                                                                                                                                                                                                                                              |
|                                    |                                                     | Compile options<br>The default setting is used in the integrated development environment.                                                                                                                                                                                                                                                                                      |
| iodefine.h version                 |                                                     | V1.1A                                                                                                                                                                                                                                                                                                                                                                          |
| Endian                             |                                                     | Little endian                                                                                                                                                                                                                                                                                                                                                                  |
| Operating mode                     |                                                     | Single-chip mode                                                                                                                                                                                                                                                                                                                                                               |
| Processor mode                     |                                                     | Supervisor mode                                                                                                                                                                                                                                                                                                                                                                |
| Sample code version                |                                                     | Version 1.02                                                                                                                                                                                                                                                                                                                                                                   |
| Board used                         |                                                     | Renesas Starter Kit for RX111 (product part no.: R0K505111SxxxBE)                                                                                                                                                                                                                                                                                                              |

### 3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX Family Coding Example for Wait Processing by Software Rev. 1.00 (R01AN1852EJ).

The wait function in the reference application note is used in the sample code accompanying this application note. The revision number of the reference application note is as of when this application note was made. However the latest version is always recommended. Visit the Renesas Electronics Corporation website to check and download the latest version.

### 4. Software

In the sample code, peripheral functions operating after a reset are stopped, nonexistent ports are configured, and then clock settings are configured.

#### 4.1 Stop Processing for Active Peripheral Functions after a Reset

Peripheral functions that are operating after a reset are stopped in this processing.

The module-stop state is canceled after a reset only for modules listed in Table 4.1. To enter the module-stop state, set the module stop bit to 1 (transition to the module-stop state is made). Power consumption can be reduced by entering the module-stop state.

In the sample code, the MSTP\_STATE\_“target module” constant is set to 0 (MODULE\_STOP\_DISABLE), so the target module does not enter the module-stop state. When the system requires a module to enter the module-stop state, set the constant in r\_init\_stop\_module.h to 1 (MODULE\_STOP\_ENABLE).

Table 4.1 lists the Peripheral Modules whose Module-Stop States are Canceled after a Reset.

**Table 4.1 Peripheral Modules whose Module-Stop States are Canceled after a Reset**

| Peripheral Module | Module Stop Bit     | Value after a Reset                  | Value when not Using the Module                    |
|-------------------|---------------------|--------------------------------------|----------------------------------------------------|
| DTC               | MSTPCRA.MSTPA28 bit | 0<br>(module-stop state is canceled) | 1<br>(transition to the module-stop state is made) |
| RAM0              | MSTPCRC.MSTPC0 bit  |                                      |                                                    |

## 4.2 Nonexistent Port Initialization

### 4.2.1 Overview

The port direction registers which have nonexistent ports need to be specified with determined values. After the nonexistent port initialization function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the values listed in Table 4.2 and Table 4.3 to the I/O select bits in the PDR registers, and set the output data store bits in the PODR registers to 0.

Table 4.2 and Table 4.3 list Setting Values in the Port Direction Registers.

**Table 4.2 Setting Values in the Port Direction Registers (1/2)**

| Port Symbol | 64-Pin Package |    |    |    |    |    |    |    | 48-Pin Package |    |    |    |    |    |    |    |
|-------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
|             | b7             | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b7             | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| PORT0       | 1              | 1  |    | 1  |    | 1  | 1  | 1  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| PORT1       |                |    |    |    | 1  | 1  | 1  | 1  |                |    |    |    | 1  | 1  | 1  | 1  |
| PORT2       |                |    | 1  | 1  | 1  | 1  | 1  | 1  |                |    | 1  | 1  | 1  | 1  | 1  | 1  |
| PORT3       | 1              | 1  | 0  | 1  | 1  |    |    |    | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 1  |
| PORT4       | 1              |    | 1  |    |    |    |    |    | 1              |    | 1  | 1  | 1  |    |    |    |
| PORT5       | 1              | 1  |    |    | 1  | 1  | 1  | 1  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| PORTA       | 1              |    | 1  |    |    | 1  |    |    | 1              |    | 1  |    |    | 1  |    | 1  |
| PORTB       |                |    |    | 1  |    | 1  |    |    | 1              | 1  |    | 1  |    | 1  |    |    |
| PORTC       |                |    |    |    |    |    |    |    |                |    |    |    |    |    |    |    |
| PORTE       |                |    |    |    |    |    |    |    |                | 1  | 1  |    |    |    |    |    |
| PORTJ       |                |    | 1  | 1  | 1  | 1  | 1  | 1  |                |    | 1  | 1  | 1  | 1  | 1  | 1  |

**Table 4.3 Setting Values in the Port Direction Registers (2/2)**

| Port Symbol | 40-Pin Package |    |    |    |    |    |    |    | 36-Pin Package |    |    |    |    |    |    |    |
|-------------|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
|             | b7             | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b7             | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| PORT0       | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| PORT1       |                |    |    |    | 1  | 1  | 1  | 1  |                |    |    |    | 1  | 1  | 1  | 1  |
| PORT2       |                |    | 1  | 1  | 1  | 1  | 1  | 1  |                | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| PORT3       | 1              | 1  | 0  | 1  | 1  |    | 1  | 1  | 1              | 1  | 0  | 1  | 1  | 1  | 1  | 1  |
| PORT4       | 1              |    | 1  | 1  | 1  |    |    | 1  | 1              | 1  | 1  | 1  | 1  |    |    | 1  |
| PORT5       | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  |
| PORTA       | 1              |    | 1  |    |    | 1  |    | 1  | 1              |    | 1  |    |    | 1  | 1  | 1  |
| PORTB       | 1              | 1  | 1  | 1  |    | 1  | 1  |    | 1              | 1  | 1  | 1  |    | 1  | 1  |    |
| PORTC       | 1              | 1  | 1  |    | 1  | 1  | 1  | 1  | 1              | 1  | 1  |    | 1  | 1  | 1  | 1  |
| PORTE       | 1              | 1  | 1  |    |    |    |    |    | 1              | 1  | 1  |    |    |    |    |    |
| PORTJ       |                |    | 1  | 1  | 1  | 1  | 1  | 1  |                |    | 1  | 1  | 1  | 1  | 1  | 1  |

### 4.2.2 Selecting the Number of Pins

The number of pins in the sample code is set for the 64-pin package (PIN\_SIZE=64). This application note covers 64-pin, 48-pin, 40-pin, and 36-pin packages. When using products other than 64 pin-package, change PIN\_SIZE in r\_init\_port\_initialize.h to the number of pins on the package used.

## 4.3 Clock Settings

### 4.3.1 Clock Setting Procedure

Table 4.4 lists the Clock Setting Procedure with each processing and setting in the sample code. In the sample code, the main clock is operating, and the sub-clock, HOCO, and PLL are stopped.

**Table 4.4 Clock Setting Procedure**

| Step | Processing                           | Details                                                                                                                |                                                                                                                                                                                                                                                                     | Setting in the Sample Code             |
|------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|
| 1    | Sub-clock setting <sup>(1)</sup>     | Not used                                                                                                               | The sub-clock control circuit is initialized.                                                                                                                                                                                                                       | Sub-clock is not used.                 |
|      |                                      | Used                                                                                                                   | The sub-clock control circuit is initialized and the sub-clock oscillation is enabled. Then wait for the oscillation stabilization time <sup>(2)</sup> by software is processed.                                                                                    |                                        |
| 2    | Main clock setting <sup>(1)</sup>    | Not used                                                                                                               | No setting is required.                                                                                                                                                                                                                                             | Main clock is used.                    |
|      |                                      | Used                                                                                                                   | The main clock drive capability is set, the MOSCWTCR register is set with a wait time until the main clock output is provided to the internal clock, and then the main clock oscillation is enabled. Then wait for the oscillation stabilization time is processed. |                                        |
| 3    | PLL clock setting <sup>(1)</sup>     | Not used                                                                                                               | No setting is required.                                                                                                                                                                                                                                             | PLL clock is not used.                 |
|      |                                      | Used                                                                                                                   | The PLL input frequency division ratio and frequency multiplication factor are set, and PLL clock oscillation is enabled. Then wait for the oscillation stabilization time is processed.                                                                            |                                        |
| 4    | HOCO clock setting <sup>(1)</sup>    | Not used                                                                                                               | No setting is required.                                                                                                                                                                                                                                             | HOCO clock is not used.                |
|      |                                      | Used                                                                                                                   | The HOCOWTCR register is set with a wait time until the HOCO clock output is provided to the internal clock, and then the HOCO clock oscillation is enabled. Then wait for the oscillation stabilization time is processed.                                         |                                        |
| 5    | Operating power control mode setting | The operating power control mode is set according to the operating frequency and operating voltage in the user system. |                                                                                                                                                                                                                                                                     | High-speed operating mode is set       |
| 6    | Clock division ratio setting         | The clock division ratio is changed.                                                                                   |                                                                                                                                                                                                                                                                     | ICLK, PCLKB, PCLKD, FCLK: Divided by 1 |
| 7    | System clock switching               | The system clock is switched according to the user system.                                                             |                                                                                                                                                                                                                                                                     | Switched to the main clock.            |

Notes:

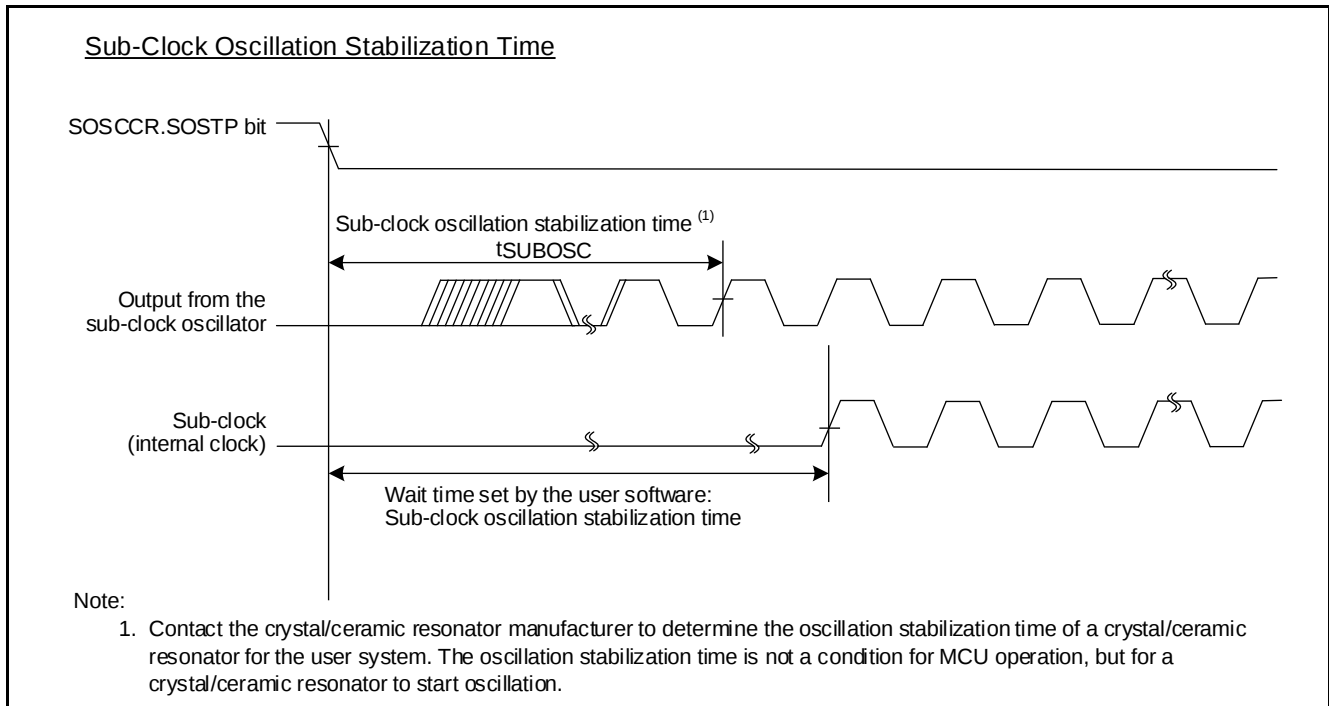
1. When selecting each clock usage, change the appropriate constant in `r_init_clock.h` as required.
2. Refer to 4.3.2 Sub-Clock Oscillation Stabilization Time for details on the sub-clock oscillation stabilization time.

### 4.3.2 Sub-Clock Oscillation Stabilization Time

This section describes the sub-clock oscillation stabilization time shown in Figure 4.1.

The sub-clock oscillation stabilization time ( $t_{SUBOSC}$ ) is set to the sub-clock oscillation stabilization time recommended by the crystal/ceramic resonator manufacturer. The wait time by software is set to a value greater than or equal to  $t_{SUBOSC}$ .

$t_{SUBOSC}$  used in the sample code is 1.3 seconds, thus the wait time by software is 1.31 seconds here.



**Figure 4.1 Sub-Clock Oscillation Stabilization Time**

#### 4.4 Section Composition

Table 4.5 lists the Section Data Changed in the Sample Code. For details on adding, changing, and deleting section, refer to the RX Family C/C++ Compiler Package User's Manual.

**Table 4.5 Section Data Changed in the Sample Code**

| Section Name | Change | Address     | Function                     |
|--------------|--------|-------------|------------------------------|
| End_of_RAM   | Add    | 0000 3FFCh* | Last address of internal RAM |

Notes: The capacity of the internal RAM is different every product. Change the address according to the product to be used.

#### 4.5 File Composition

Table 4.6 lists the Files Used in the Sample Code. Files generated by the integrated development environment should not be listed in this table.

**Table 4.6 Files Used in the Sample Code**

| File Name                | Outline                                                       | Remarks |
|--------------------------|---------------------------------------------------------------|---------|
| main.c                   | Main processing                                               |         |
| r_init_stop_module.c     | Stop processing for active peripheral functions after a reset |         |
| r_init_stop_module.h     | Header file for r_init_stop_module.c                          |         |
| r_init_port_initialize.c | Nonexistent port initialization                               |         |
| r_init_port_initialize.h | Header file for r_init_port_initialize.c                      |         |
| r_init_clock.c           | Clock initialization                                          |         |
| r_init_clock.h           | Header file for r_init_clock.c                                |         |
| r_delay.c                | Wait processing by software                                   |         |
| r_delay.h                | Header file for r_delay.c                                     |         |

#### 4.6 Option-Setting Memory

Table 4.7 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

**Table 4.7 Option-Setting Memory Configured in the Sample Code**

| Symbol | Address                  | Setting Value | Contents                                                                                                                                            |
|--------|--------------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| OFS0   | FFFF FF8Fh to FFFF FF8Ch | FFFF FFFFh    | The IWDT is stopped after a reset.                                                                                                                  |
| OFS1   | FFFF FF8Bh to FFFF FF88h | FFFF FFFFh    | Fast startup time at power-on is disabled.<br>The voltage monitor 1 reset is disabled after a reset.<br>HOCO oscillation is disabled after a reset. |
| MDE    | FFFF FF83h to FFFF FF80h | FFFF FFFFh    | Little endian                                                                                                                                       |

## 4.7 Constants

Table 4.8 and Table 4.9 list the constants used in the sample code, which can be changed by users. Table 4.10 lists the constants used in the sample code, which cannot be changed by users. Table 4.11 lists the Constants when a 64-Pin Package is Used (PIN\_SIZE=64), Table 4.12 lists the Constants when a 48-Pin Package is Used (PIN\_SIZE=48), Table 4.13 lists the Constants when a 40-Pin Package is Used (PIN\_SIZE=40), and Table 4.14 lists the Constants when a 36-Pin Package is Used (PIN\_SIZE=36).

**Table 4.8 Constants Used in the Sample Code (1/2)**  
(Users can change the constants listed in this table.)

| Constant Name                                | Setting Value  | Contents                                                                                                                                                                                                                                                       |
|----------------------------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEL_MAIN <sup>(1)</sup>                      | B_USE          | Selection of the main clock operation:<br>- B_USE: Used (main clock oscillating)<br>- B_NOT_USE: Not used (main clock stopped)                                                                                                                                 |
| MAIN_CLOCK_HZ <sup>(1)</sup>                 | 16,000,000L    | Oscillation frequency of a crystal/ceramic resonator for the main clock (Hz)                                                                                                                                                                                   |
| REG_MOFCR <sup>(1)</sup>                     | 20h            | Setting for the drive capability of the main clock oscillator (setting value in the MOFCR register)                                                                                                                                                            |
| REG_MOSCWTCR <sup>(1)</sup>                  | 06h            | Setting value in the main clock wait control register                                                                                                                                                                                                          |
| SEL_HOCO                                     | B_NOT_USE      | Selection of the HOCO clock operation:<br>- B_USE: Used (HOCO clock oscillating)<br>- B_NOT_USE: Not used (HOCO clock stopped)                                                                                                                                 |
| REG_HOCOWTCR                                 | 06h            | Setting value in the HOCO wait control register                                                                                                                                                                                                                |
| SEL_PLL                                      | B_NOT_USE      | Selection of the PLL clock operation:<br>- B_USE: Used (PLL clock oscillating)<br>- B_NOT_USE: Not used (PLL clock stopped)                                                                                                                                    |
| REG_PLLCR                                    | 0B01h          | PLL input frequency division ratio and frequency multiplication factor settings (setting values in the PLLCR register)                                                                                                                                         |
| SEL_SUB <sup>(1, 2)</sup>                    | B_NOT_USE      | Selection of the sub-clock usage for the system clock:<br>- B_USE: Used<br>- B_NOT_USE: Not used                                                                                                                                                               |
| SEL_RTC <sup>(1, 2)</sup>                    | B_NOT_USE      | Selection of the sub-clock usage for the RTC count source:<br>- B_USE: Used<br>- B_NOT_USE: Not used                                                                                                                                                           |
| SUB_CLOCK_HZ <sup>(1)</sup>                  | 32,768 L       | Oscillation frequency of a crystal for the sub-clock (Hz)                                                                                                                                                                                                      |
| WAIT_TIME_FOR_SUB_OSCILLATION <sup>(1)</sup> | 1,310,000,000L | Sub-clock oscillation stabilization time (ns)                                                                                                                                                                                                                  |
| REG_RCR3 <sup>(1)</sup>                      | DRIVE_MID      | Selection of the sub-clock oscillator drive capability:<br>- DRIVE_MID: Medium drive capacity (4.4 pF type)<br>- DRIVE_HIGH: High drive capacity (6.0 pF type)<br>- DRIVE_LOW: Low drive capacity (3.7 pF type)<br>- DRIVE_TYP: Drive capacity for standard CL |
| SEL_CNTMD <sup>(1)</sup>                     | CNTMD_CAL      | Selection of the real-time clock count mode<br>- CNTMD_CAL: Calendar count mode<br>- CNTMD_BIN: Binary count mode                                                                                                                                              |

Notes:

1. Change the setting value in r\_init\_clock.h according to the user system.
2. The sub-clock operation is set to be oscillating by setting B\_USE (sub-clock used) to either of the SEL\_SUB constant or SEL\_RTC constant, or both.

**Table 4.9 Constants Used in the Sample Code (2/2)**  
 (Users can change the constants listed in this table.)

| Constant Name                  | Setting Value           | Contents                                                                                                                                                                                                        |
|--------------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEL_SYSCLOCK <sup>(1)</sup>    | CLK_MAIN                | Clock source selection for the system clock<br>- CLK_HOCO: HOCO clock<br>- CLK_MAIN: Main clock<br>- CLK_SUB: Sub-clock<br>- CLK_PLL: PLL clock                                                                 |
| REG_OPCCR <sup>(1)</sup>       | OPCM_HIGH               | Selection of the operating power control mode <sup>(5)</sup><br>- OPCM_HIGH: High-speed operating mode<br>- OPCM_MID: Middle-speed operating mode<br>- OPCM_LOW: Low-speed operating mode <sup>(4)</sup>        |
| REG_SOPCCR <sup>(1)</sup>      | SOPCM_HIGH              | Selection of the sub operating power control mode <sup>(5)</sup><br>- SOPCM_HIGH: High-speed operating mode<br>- SOPCM_MID: Middle-speed operating mode<br>- SOPCM_LOW: Low-speed operating mode <sup>(4)</sup> |
| MSTP_STATE_DTC <sup>(2)</sup>  | MODULE_STOP_DISABLE     | Selection of the module-stop state for DTC<br>- MODULE_STOP_DISABLE: Module-stop state canceled<br>- MODULE_STOP_ENABLE: Entering the module-stop state                                                         |
| MSTP_STATE_RAM0 <sup>(2)</sup> | MODULE_STOP_DISABLE     | Selection of the module-stop state for RAM0<br>- MODULE_STOP_DISABLE: Operating<br>- MODULE_STOP_ENABLE: Stopped                                                                                                |
| PIN_SIZE <sup>(3)</sup>        | 64                      | Number of pins on the product used                                                                                                                                                                              |
| SUB_CLOCK_CYCLE                | (1000000L/SUB_CLOCK_Hz) | Sub-clock cycle (μs)                                                                                                                                                                                            |
| LOCO_CLOCK_KHZ                 | (4560L)                 | LOCO frequency (kHz)                                                                                                                                                                                            |
| FOR_CMT0_TIME                  | (7018*8)                | Count period (ns) of the timer (CMT0) to wait for oscillation to be stabilized<br>(LOCO = 4.56 MHz (max.) divided by 8 and PCLK divided by 32)                                                                  |

Notes:

1. Change the setting value in r\_init\_clock.h according to the user system.
2. Change the setting value in r\_init\_stop\_module.h according to the user system.
3. Change the setting value in r\_init\_port\_initialize.h according to the user system.
4. Low-speed operating mode can be selected only when the sub-clock is used as the system clock.
5. The ranges of the operating frequency and operating voltage differ depending on operating modes. Refer to the User's Manual: Hardware for details.

**Table 4.10 Constants Used in the Sample Code**  
(Users cannot change the constants listed in this table.)

| Constant Name            | Setting Value                                                          | Contents                                                                            |
|--------------------------|------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| B_NOT_USE                | 0                                                                      | Not used                                                                            |
| B_USE                    | 1                                                                      | Used                                                                                |
| DRIVE_MID                | 00h                                                                    | Sub-clock: Medium drive capacity (4.4 pF type)                                      |
| DRIVE_HIGH               | 02h                                                                    | Sub-clock: High drive capacity (6.0 pF type)                                        |
| DRIVE_LOW                | 04h                                                                    | Sub-clock: Low drive capacity (3.7 pF type)                                         |
| DRIVE_TYP                | 08h                                                                    | Sub-clock: Drive capacity for standard CL                                           |
| CNTMD_CAL                | 0                                                                      | RTC: Calendar count mode                                                            |
| CNTMD_BIN                | 1                                                                      | RTC: Binary count mode                                                              |
| CLK_MAIN                 | 0200h                                                                  | Clock source: Main clock                                                            |
| CLK_PLL                  | 0400h                                                                  | Clock source: PLL                                                                   |
| CLK_HOCO                 | 0100h                                                                  | Clock source: HOCO                                                                  |
| CLK_SUB                  | 0300h                                                                  | Clock source: Sub-clock                                                             |
| REG_SCKCR <sup>(1)</sup> | - 1100 0101h (when PLL is selected)<br>- 0000 0000h (other than above) | Setting for the internal clock division ratio (setting value in the SCKCR register) |
| SOPCM_MID                | 00h                                                                    | Sub-operating power control mode:<br>Middle-speed operating mode                    |
| OPCM_MID                 | 02h                                                                    | Operating power control mode:<br>Middle-speed operating mode                        |
| SOPCM_HIGH               | 00h                                                                    | Sub-operating power control mode:<br>High-speed operating mode                      |
| OPCM_HIGH                | 00h                                                                    | Operating power control mode:<br>High-speed operating mode                          |
| SOPCM_LOW                | 01h                                                                    | Sub-operating power control mode:<br>Low-speed operating mode                       |
| OPCM_LOW                 | 00h                                                                    | Operating power control mode:<br>Low-speed operating mode                           |
| MODULE_STOP_ENABLE       | 1                                                                      | Transition to the module stop-state is made                                         |
| MODULE_STOP_DISABLE      | 0                                                                      | Module stop-state is canceled                                                       |

Note:

1. The setting value varies depending on the clock source of the system clock selected.

Table 4.11 Constants when a 64-Pin Package is Used (PIN\_SIZE=64)

| Constant Name  | Setting Value | Contents                                         |
|----------------|---------------|--------------------------------------------------|
| DEF_P0PDR_MASK | 28h           | Mask value for the port P0 direction register    |
| DEF_P1PDR_MASK | F0h           | Mask value for the port P1 direction register    |
| DEF_P2PDR_MASK | C0h           | Mask value for the port P2 direction register    |
| DEF_P3PDR_MASK | 07h           | Mask value for the port P3 direction register    |
| DEF_P4PDR_MASK | 5Fh           | Mask value for the port P4 direction register    |
| DEF_P5PDR_MASK | 30h           | Mask value for the port P5 direction register    |
| DEF_PAPDR_MASK | 5Bh           | Mask value for the port PA direction register    |
| DEF_PBPDR_MASK | EBh           | Mask value for the port PB direction register    |
| DEF_PCPDR_MASK | FFh           | Mask value for the port PC direction register    |
| DEF_PEPDR_MASK | FFh           | Mask value for the port PE direction register    |
| DEF_PJPDR_MASK | C0h           | Mask value for the port PJ direction register    |
| DEF_P0PDR      | D7h           | Setting value for the port P0 direction register |
| DEF_P1PDR      | 0Fh           | Setting value for the port P1 direction register |
| DEF_P2PDR      | 3Fh           | Setting value for the port P2 direction register |
| DEF_P3PDR      | D8h           | Setting value for the port P3 direction register |
| DEF_P4PDR      | A0h           | Setting value for the port P4 direction register |
| DEF_P5PDR      | CFh           | Setting value for the port P5 direction register |
| DEF_PAPDR      | A4h           | Setting value for the port PA direction register |
| DEF_PBPDR      | 14h           | Setting value for the port PB direction register |
| DEF_PCPDR      | 00h           | Setting value for the port PC direction register |
| DEF_PEPDR      | 00h           | Setting value for the port PE direction register |
| DEF_PJPDR      | 3Fh           | Setting value for the port PJ direction register |

Table 4.12 Constants when a 48-Pin Package is Used (PIN\_SIZE=48)

| Constant Name  | Setting Value | Contents                                         |
|----------------|---------------|--------------------------------------------------|
| DEF_P0PDR_MASK | 00h           | Mask value for the port P0 direction register    |
| DEF_P1PDR_MASK | F0h           | Mask value for the port P1 direction register    |
| DEF_P2PDR_MASK | C0h           | Mask value for the port P2 direction register    |
| DEF_P3PDR_MASK | 00h           | Mask value for the port P3 direction register    |
| DEF_P4PDR_MASK | 47h           | Mask value for the port P4 direction register    |
| DEF_P5PDR_MASK | 00h           | Mask value for the port P5 direction register    |
| DEF_PAPDR_MASK | 5Ah           | Mask value for the port PA direction register    |
| DEF_PBPDR_MASK | 2Bh           | Mask value for the port PB direction register    |
| DEF_PCPDR_MASK | FFh           | Mask value for the port PC direction register    |
| DEF_PEPDR_MASK | 9Fh           | Mask value for the port PE direction register    |
| DEF_PJPDR_MASK | C0h           | Mask value for the port PJ direction register    |
| DEF_P0PDR      | FFh           | Setting value for the port P0 direction register |
| DEF_P1PDR      | 0Fh           | Setting value for the port P1 direction register |
| DEF_P2PDR      | 3Fh           | Setting value for the port P2 direction register |
| DEF_P3PDR      | DFh           | Setting value for the port P3 direction register |
| DEF_P4PDR      | B8h           | Setting value for the port P4 direction register |
| DEF_P5PDR      | FFh           | Setting value for the port P5 direction register |
| DEF_PAPDR      | A5h           | Setting value for the port PA direction register |
| DEF_PBPDR      | D4h           | Setting value for the port PB direction register |
| DEF_PCPDR      | 00h           | Setting value for the port PC direction register |
| DEF_PEPDR      | 60h           | Setting value for the port PE direction register |
| DEF_PJPDR      | 3Fh           | Setting value for the port PJ direction register |

Table 4.13 Constants when a 40-Pin Package is Used (PIN\_SIZE=40)

| Constant Name  | Setting Value | Contents                                         |
|----------------|---------------|--------------------------------------------------|
| DEF_P0PDR_MASK | 00h           | Mask value for the port P0 direction register    |
| DEF_P1PDR_MASK | F0h           | Mask value for the port P1 direction register    |
| DEF_P2PDR_MASK | C0h           | Mask value for the port P2 direction register    |
| DEF_P3PDR_MASK | 04h           | Mask value for the port P3 direction register    |
| DEF_P4PDR_MASK | 46h           | Mask value for the port P4 direction register    |
| DEF_P5PDR_MASK | 00h           | Mask value for the port P5 direction register    |
| DEF_PAPDR_MASK | 5Ah           | Mask value for the port PA direction register    |
| DEF_PBPDR_MASK | 09h           | Mask value for the port PB direction register    |
| DEF_PCPDR_MASK | 10h           | Mask value for the port PC direction register    |
| DEF_PEPDR_MASK | 1Fh           | Mask value for the port PE direction register    |
| DEF_PJPDR_MASK | C0h           | Mask value for the port PJ direction register    |
| DEF_P0PDR      | FFh           | Setting value for the port P0 direction register |
| DEF_P1PDR      | 0Fh           | Setting value for the port P1 direction register |
| DEF_P2PDR      | 3Fh           | Setting value for the port P2 direction register |
| DEF_P3PDR      | DBh           | Setting value for the port P3 direction register |
| DEF_P4PDR      | B9h           | Setting value for the port P4 direction register |
| DEF_P5PDR      | FFh           | Setting value for the port P5 direction register |
| DEF_PAPDR      | A5h           | Setting value for the port PA direction register |
| DEF_PBPDR      | F6h           | Setting value for the port PB direction register |
| DEF_PCPDR      | EFh           | Setting value for the port PC direction register |
| DEF_PEPDR      | E0h           | Setting value for the port PE direction register |
| DEF_PJPDR      | 3Fh           | Setting value for the port PJ direction register |

Table 4.14 Constants when a 36-Pin Package is Used (PIN\_SIZE=36)

| Constant Name  | Setting Value | Contents                                         |
|----------------|---------------|--------------------------------------------------|
| DEF_P0PDR_MASK | 00h           | Mask value for the port P0 direction register    |
| DEF_P1PDR_MASK | F0h           | Mask value for the port P1 direction register    |
| DEF_P2PDR_MASK | 80h           | Mask value for the port P2 direction register    |
| DEF_P3PDR_MASK | 00h           | Mask value for the port P3 direction register    |
| DEF_P4PDR_MASK | 06h           | Mask value for the port P4 direction register    |
| DEF_P5PDR_MASK | 00h           | Mask value for the port P5 direction register    |
| DEF_PAPDR_MASK | 58h           | Mask value for the port PA direction register    |
| DEF_PBPDR_MASK | 09h           | Mask value for the port PB direction register    |
| DEF_PCPDR_MASK | 10h           | Mask value for the port PC direction register    |
| DEF_PEPDR_MASK | 1Fh           | Mask value for the port PE direction register    |
| DEF_PJPDR_MASK | C0h           | Mask value for the port PJ direction register    |
| DEF_P0PDR      | FFh           | Setting value for the port P0 direction register |
| DEF_P1PDR      | 0Fh           | Setting value for the port P1 direction register |
| DEF_P2PDR      | 7Fh           | Setting value for the port P2 direction register |
| DEF_P3PDR      | DFh           | Setting value for the port P3 direction register |
| DEF_P4PDR      | F9h           | Setting value for the port P4 direction register |
| DEF_P5PDR      | FFh           | Setting value for the port P5 direction register |
| DEF_PAPDR      | A7h           | Setting value for the port PA direction register |
| DEF_PBPDR      | F6h           | Setting value for the port PB direction register |
| DEF_PCPDR      | EFh           | Setting value for the port PC direction register |
| DEF_PEPDR      | E0h           | Setting value for the port PE direction register |
| DEF_PJPDR      | 3Fh           | Setting value for the port PJ direction register |

## 4.8 Functions

Table 4.15 lists the Functions Used in the Sample Code.

**Table 4.15 Functions Used in the Sample Code**

| Function Name           | Outline                                                                                      |
|-------------------------|----------------------------------------------------------------------------------------------|
| main                    | Main processing                                                                              |
| R_INIT_StopModule       | Stop processing for active peripheral functions after a reset                                |
| R_INIT_Port_Initialize  | Nonexistent port initialization                                                              |
| R_INIT_Clock            | Clock initialization                                                                         |
| CGC_oscillation_main    | Main clock oscillation setting                                                               |
| CGC_oscillation_HOCO    | HOCO clock oscillation setting                                                               |
| CGC_oscillation_PLL     | PLL clock oscillation setting                                                                |
| CGC_oscillation_sub     | Sub-clock oscillation setting                                                                |
| CGC_disable_subclk      | Sub-clock stop setting                                                                       |
| oscillation_subclk      | Enabling sub-clock oscillation                                                               |
| init_RTC                | RTC initialization                                                                           |
| no_use_subclk_as_sysclk | Setting when the sub-clock is not used as the system clock                                   |
| cmt0_countstart         | CMT0 wait start setting (wait for sub-clock oscillation stabilization)                       |
| cmt0_endcheck           | CMT0 wait (wait for sub-clock oscillation stabilization) completion check and initialization |
| R_DELAY                 | Inline function to specify the number of loops                                               |
| R_DELAY_Us              | Function to specify the execution time                                                       |

## 4.9 Function Specifications

The following tables list the sample code function specifications.

|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| main                   |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Outline</b>         | Main processing                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Header</b>          | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Declaration</b>     | void main (void)                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Description</b>     | Calls the following functions: Stop processing for active peripheral functions after a reset, nonexistent port initialization, and clock initialization.                                                                                                                                                                                                                                                                                   |
| <b>Arguments</b>       | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Return Value</b>    | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| R_INIT_StopModule      |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Outline</b>         | Stop processing for active peripheral functions after a reset                                                                                                                                                                                                                                                                                                                                                                              |
| <b>Header</b>          | r_init_stop_module.h                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Declaration</b>     | void R_INIT_StopModule (void)                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>Description</b>     | Configures the setting to enter the module-stop state.                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Arguments</b>       | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Return Value</b>    | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Remarks</b>         | Transition to the module-stop state is not performed in the sample code.                                                                                                                                                                                                                                                                                                                                                                   |
| R_INIT_Port_Initialize |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Outline</b>         | Nonexistent port initialization                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Header</b>          | r_init_port_initialize.h                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Declaration</b>     | void R_INIT_Port_Initialize (void)                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Description</b>     | Initializes port direction registers for ports that do not exist in products.                                                                                                                                                                                                                                                                                                                                                              |
| <b>Arguments</b>       | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Return Value</b>    | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Remarks</b>         | The number of pins in the sample code is set for the 64-pin package (PIN_SIZE=64). After this function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the value listed in Table 4.2 and Table 4.3 to the I/O select bits in the PDR registers, and set the output data store bits in the PODR registers to 0. |
| R_INIT_Clock           |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>Outline</b>         | Clock initialization                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Header</b>          | r_init_clock.h                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <b>Declaration</b>     | void R_INIT_Clock (void)                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>Description</b>     | Initializes the clock.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>Arguments</b>       | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Return Value</b>    | None                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Remarks</b>         | The sample code selects processing which uses the main clock as the system clock without using the sub-clock and RTC.                                                                                                                                                                                                                                                                                                                      |

|                             |                                                                                                                                                                            |
|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CGC_oscillation_main</b> |                                                                                                                                                                            |
| <b>Outline</b>              | Main clock oscillation setting                                                                                                                                             |
| <b>Header</b>               | r_init_clock.h                                                                                                                                                             |
| <b>Declaration</b>          | void CGC_oscillation_main (void)                                                                                                                                           |
| <b>Description</b>          | Sets the main clock drive capability, sets the MOSCWTCR register, and enables main clock oscillation. Then waits for the main clock oscillation stabilization time.        |
| <b>Arguments</b>            | None                                                                                                                                                                       |
| <b>Return Value</b>         | None                                                                                                                                                                       |
| <b>CGC_oscillation_HOCO</b> |                                                                                                                                                                            |
| <b>Outline</b>              | HOCO clock oscillation setting                                                                                                                                             |
| <b>Header</b>               | r_init_clock.h                                                                                                                                                             |
| <b>Declaration</b>          | void CGC_oscillation_HOCO (void)                                                                                                                                           |
| <b>Description</b>          | Sets the HOCOWTCR register, and enables HOCO oscillation. Then waits for the HOCO clock oscillation stabilization time.                                                    |
| <b>Arguments</b>            | None                                                                                                                                                                       |
| <b>Return Value</b>         | None                                                                                                                                                                       |
| <b>CGC_oscillation_PLL</b>  |                                                                                                                                                                            |
| <b>Outline</b>              | PLL clock oscillation setting                                                                                                                                              |
| <b>Header</b>               | r_init_clock.h                                                                                                                                                             |
| <b>Declaration</b>          | void CGC_oscillation_PLL (void)                                                                                                                                            |
| <b>Description</b>          | Sets the PLL input frequency division ratio and frequency multiplication factor, and enables PLL clock oscillation. Then waits for the PLL oscillation stabilization time. |
| <b>Arguments</b>            | None                                                                                                                                                                       |
| <b>Return Value</b>         | None                                                                                                                                                                       |
| <b>CGC_oscillation_sub</b>  |                                                                                                                                                                            |
| <b>Outline</b>              | Sub-clock oscillation setting                                                                                                                                              |
| <b>Header</b>               | r_init_clock.h                                                                                                                                                             |
| <b>Declaration</b>          | void CGC_oscillation_sub (void)                                                                                                                                            |
| <b>Description</b>          | Configures the setting when the sub-clock is used as either the system clock or the RTC count source, or both.                                                             |
| <b>Arguments</b>            | None                                                                                                                                                                       |
| <b>Return Value</b>         | None                                                                                                                                                                       |
| <b>CGC_disable_subclk</b>   |                                                                                                                                                                            |
| <b>Outline</b>              | Sub-clock stop setting                                                                                                                                                     |
| <b>Header</b>               | r_init_clock.h                                                                                                                                                             |
| <b>Declaration</b>          | void CGC_disable_subclk (void)                                                                                                                                             |
| <b>Description</b>          | Configures the setting when the sub-clock is not used as the system clock or the RTC count source.                                                                         |
| <b>Arguments</b>            | None                                                                                                                                                                       |
| <b>Return Value</b>         | None                                                                                                                                                                       |

|                                     |                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <hr/> oscillation_subclk <hr/>      |                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Outline</b>                      | Enabling the sub-clock oscillation                                                                                                                                                                                                                                                                                                                                        |
| <b>Header</b>                       | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Declaration</b>                  | static void oscillation_subclk (void)                                                                                                                                                                                                                                                                                                                                     |
| <b>Description</b>                  | Configures settings for sub-clock oscillation.                                                                                                                                                                                                                                                                                                                            |
| <b>Arguments</b>                    | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Return Value</b>                 | None                                                                                                                                                                                                                                                                                                                                                                      |
| <hr/>                               |                                                                                                                                                                                                                                                                                                                                                                           |
| <hr/> init_RTC <hr/>                |                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Outline</b>                      | RTC initialization                                                                                                                                                                                                                                                                                                                                                        |
| <b>Header</b>                       | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Declaration</b>                  | static void init_RTC (void)                                                                                                                                                                                                                                                                                                                                               |
| <b>Description</b>                  | Configure the sub-clock setting for when it is not used as the system clock or RTC count source.                                                                                                                                                                                                                                                                          |
| <b>Arguments</b>                    | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Return Value</b>                 | None                                                                                                                                                                                                                                                                                                                                                                      |
| <hr/>                               |                                                                                                                                                                                                                                                                                                                                                                           |
| <hr/> no_use_subclk_as_sysclk <hr/> |                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Outline</b>                      | Processing when the sub-clock is not used as the system clock                                                                                                                                                                                                                                                                                                             |
| <b>Header</b>                       | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Declaration</b>                  | static void no_use_subclk_as_sysclk (void)                                                                                                                                                                                                                                                                                                                                |
| <b>Description</b>                  | Stops the sub-clock as the system clock when the sub-clock is used only as the RTC count source.                                                                                                                                                                                                                                                                          |
| <b>Arguments</b>                    | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Return Value</b>                 | None                                                                                                                                                                                                                                                                                                                                                                      |
| <hr/>                               |                                                                                                                                                                                                                                                                                                                                                                           |
| <hr/> cmt0_countstart <hr/>         |                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Outline</b>                      | CMT0 wait start setting (wait for sub-clock oscillation stabilization)                                                                                                                                                                                                                                                                                                    |
| <b>Header</b>                       | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Declaration</b>                  | static void cmt0_countstart (uint16_t cnt)                                                                                                                                                                                                                                                                                                                                |
| <b>Description</b>                  | When using the sub-clock oscillator, waits for the sub-clock oscillation stabilization time with CMT0. When starting to wait for the oscillation stabilization, CMT0 count starts.                                                                                                                                                                                        |
| <b>Arguments</b>                    | uint32_t cnt:   Oscillation stabilization time<br>cnt = oscillation stabilization time (ns) <sup>(1)</sup> ÷ FOR_CMT0_TIME <sup>(2)</sup>                                                                                                                                                                                                                                 |
| <b>Return Value</b>                 | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Remarks</b>                      | <ol style="list-style-type: none"> <li>1. The oscillation stabilization time varies depending on the crystal/ceramic resonator. Set the value referring to 4.3.2 Sub-Clock Oscillation Stabilization Time.</li> <li>2. The value of FOR_CMT0_TIME is calculated with 4.56 MHz (max.) of LOCO. The actual wait time may differ depending on the LOCO frequency.</li> </ol> |
| <hr/>                               |                                                                                                                                                                                                                                                                                                                                                                           |
| <hr/> cmt0_endcheck <hr/>           |                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Outline</b>                      | CMT0 wait (wait for sub-clock oscillation stabilization) completion check and initialization                                                                                                                                                                                                                                                                              |
| <b>Header</b>                       | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Declaration</b>                  | static void cmt0_endcheck (void)                                                                                                                                                                                                                                                                                                                                          |
| <b>Description</b>                  | When using the sub-clock oscillator, checks whether the wait processing for the sub-clock oscillation stabilization is completed. If completed, initializes CMT0.                                                                                                                                                                                                         |
| <b>Arguments</b>                    | None                                                                                                                                                                                                                                                                                                                                                                      |
| <b>Return Value</b>                 | None                                                                                                                                                                                                                                                                                                                                                                      |

---

**R\_DELAY**

---

|                     |                                                                                                          |
|---------------------|----------------------------------------------------------------------------------------------------------|
| <b>Outline</b>      | Inline function to specify the number of loops                                                           |
| <b>Header</b>       | r_delay.h                                                                                                |
| <b>Declaration</b>  | static void R_DELAY (unsigned long loop_cnt)                                                             |
| <b>Description</b>  | Wait processing which performs loops for the specified number of times (a loop is fixed at five cycles). |
| <b>Arguments</b>    | loop_cnt: The number of loops                                                                            |
| <b>Return Value</b> | None                                                                                                     |

---

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**R\_DELAY\_Us**

---

|                     |                                                                                                                                                                            |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Outline</b>      | Function to specify the execution time                                                                                                                                     |
| <b>Header</b>       | r_delay.h                                                                                                                                                                  |
| <b>Declaration</b>  | void R_DELAY_Us (unsigned long us, unsigned long khz)                                                                                                                      |
| <b>Description</b>  | Calculates the number of loops based on the execution time ( $\mu$ s) and the system clock (ICLK) frequency, and calls the inline function to specify the number of loops. |
| <b>Arguments</b>    | us: Execution time<br>khz: System clock (ICLK) frequency when the function is called.                                                                                      |
| <b>Return Value</b> | None                                                                                                                                                                       |

## 4.10 Flowcharts

### 4.10.1 Main Processing

Figure 4.2 shows the Main Processing.

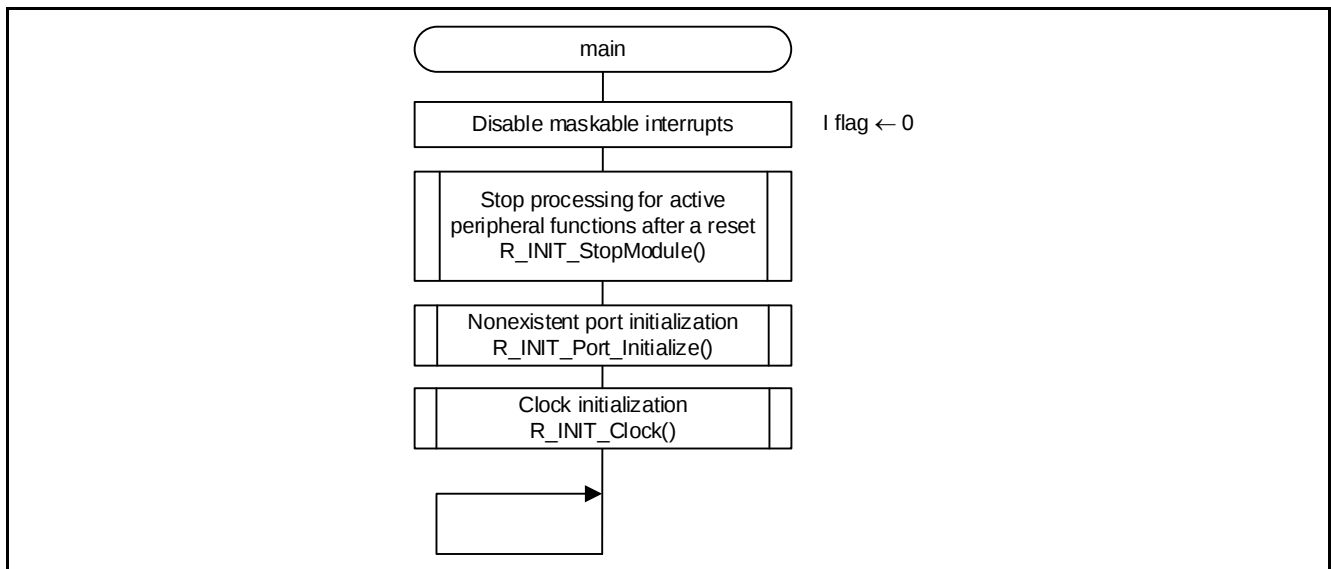


Figure 4.2 Main Processing

### 4.10.2 Stop Processing for Active Peripheral Functions after a Reset

Figure 4.3 shows the Stop Processing for Active Peripheral Functions after a Reset.

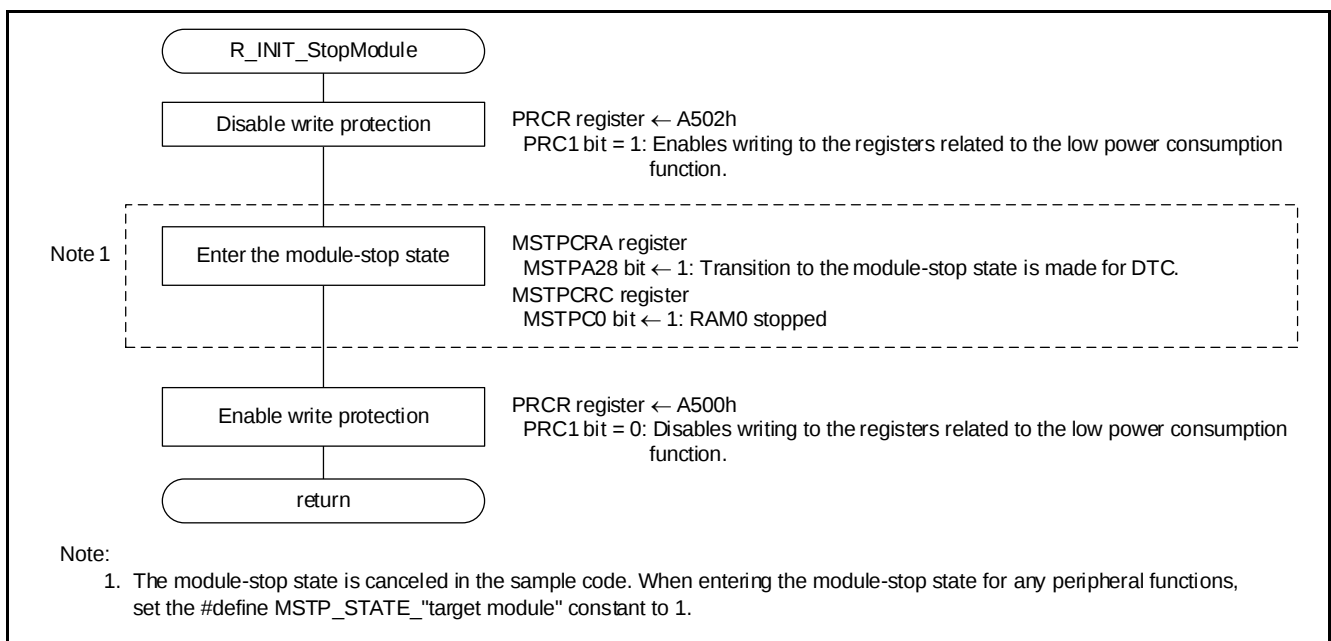
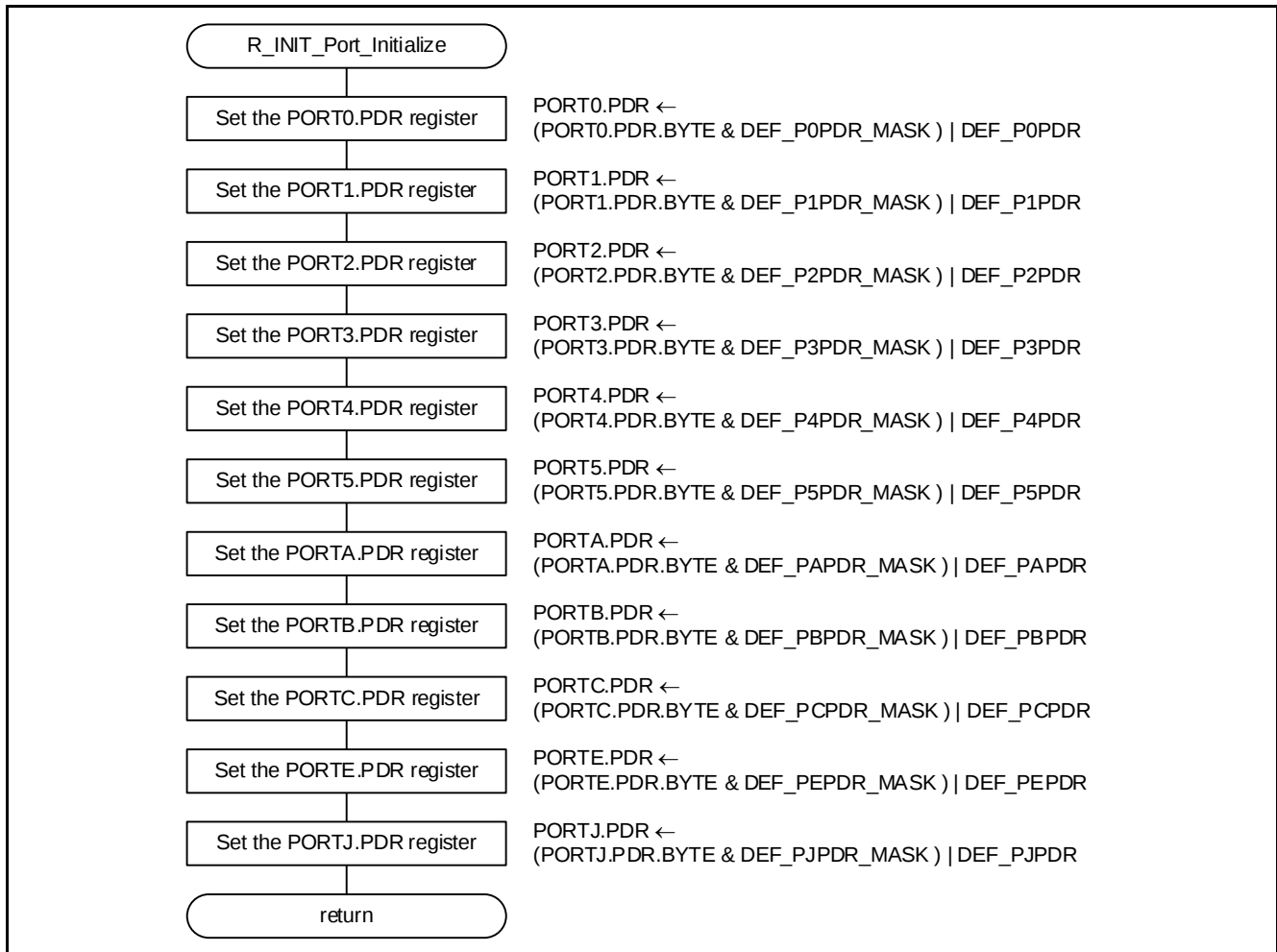


Figure 4.3 Stop Processing for Active Peripheral Functions after a Reset

### 4.10.3 Nonexistent Port Initialization

Figure 4.4 shows the Nonexistent Port Initialization.



**Figure 4.4 Nonexistent Port Initialization**

#### 4.10.4 Clock Initialization

Figure 4.5 and Figure 4.6 show the clock initialization.

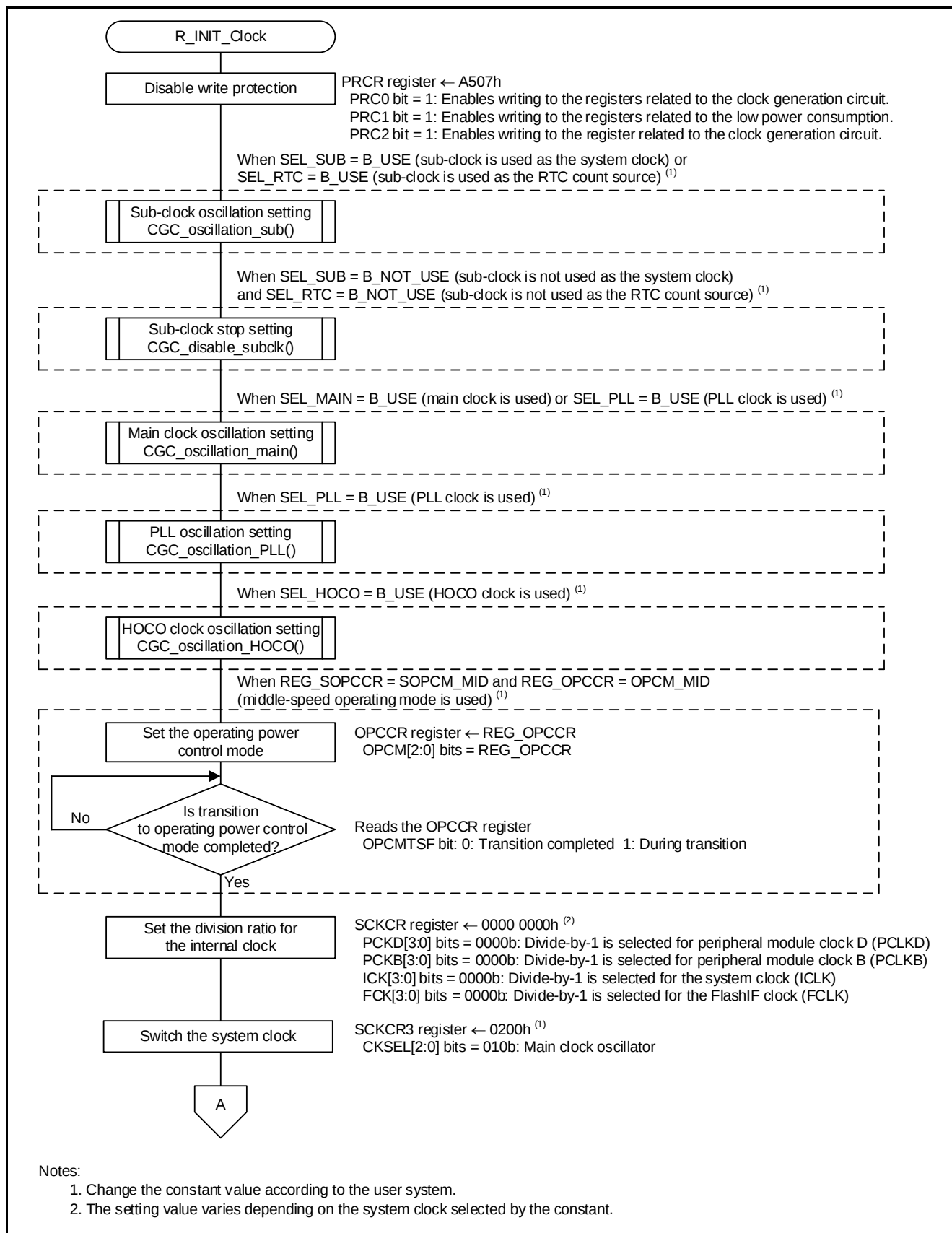


Figure 4.5 Clock Initialization (1/2)

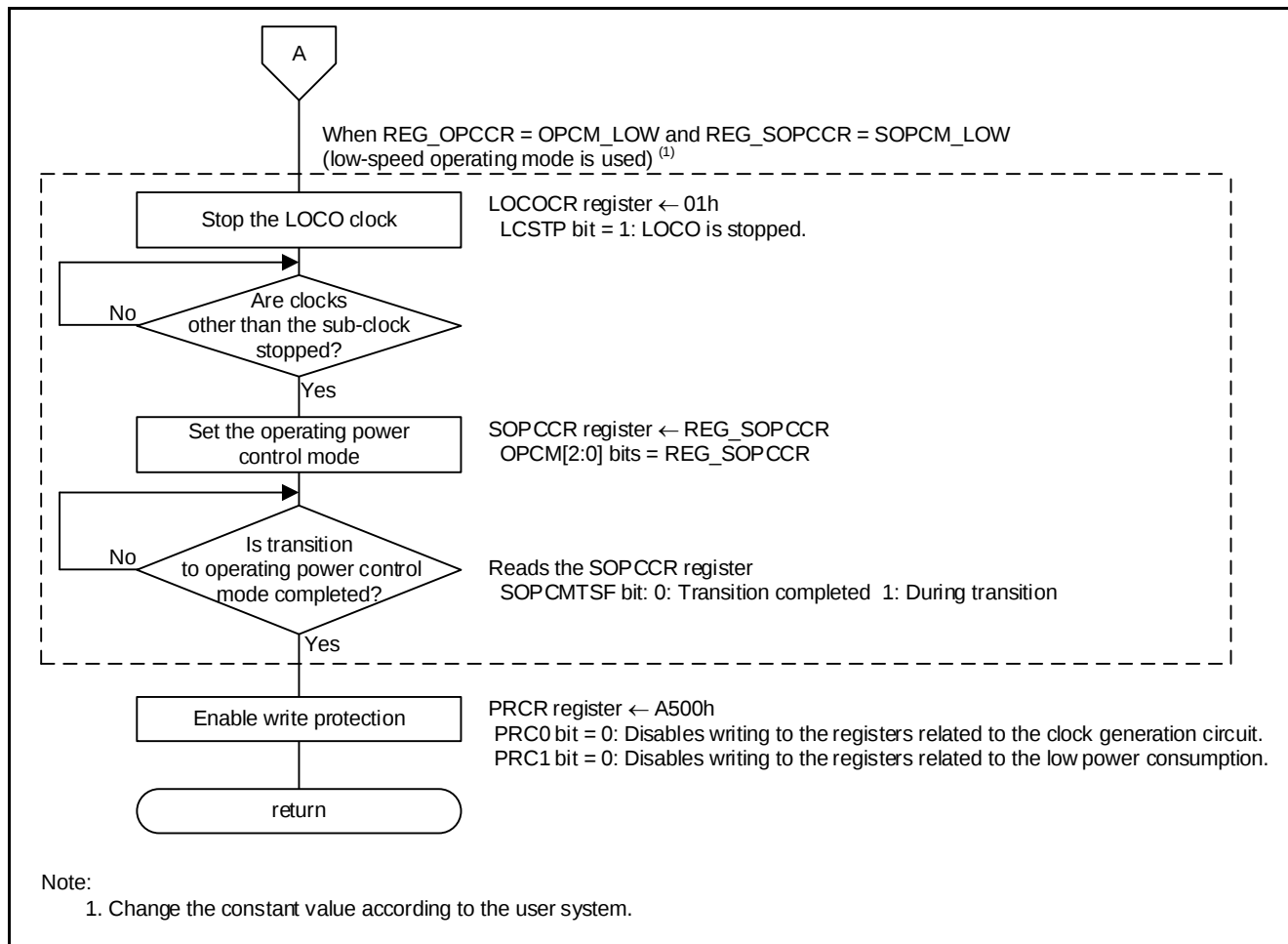


Figure 4.6 Clock Initialization (2/2)

#### 4.10.5 Main Clock Oscillation Setting

Figure 4.7 shows the Main Clock Oscillation Setting.

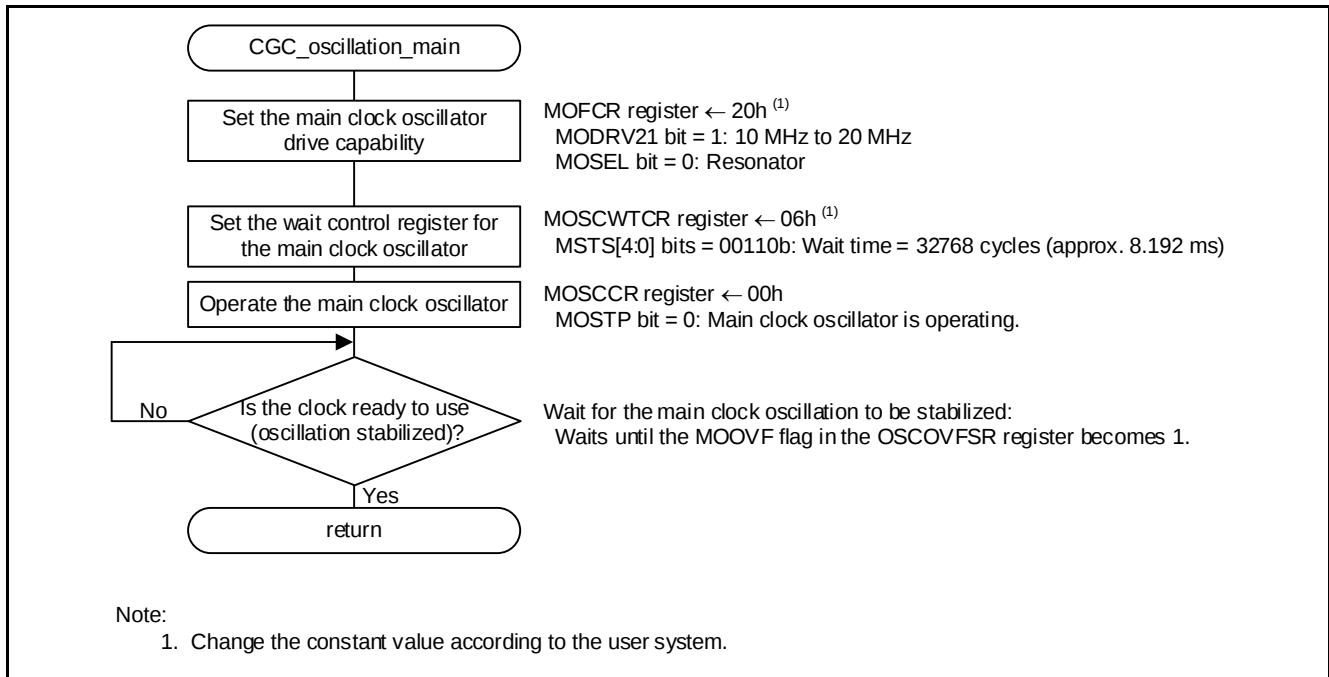


Figure 4.7 Main Clock Oscillation Setting

#### 4.10.6 HOCO Clock Oscillation Setting

Figure 4.8 shows the HOCO Clock Oscillation Setting.

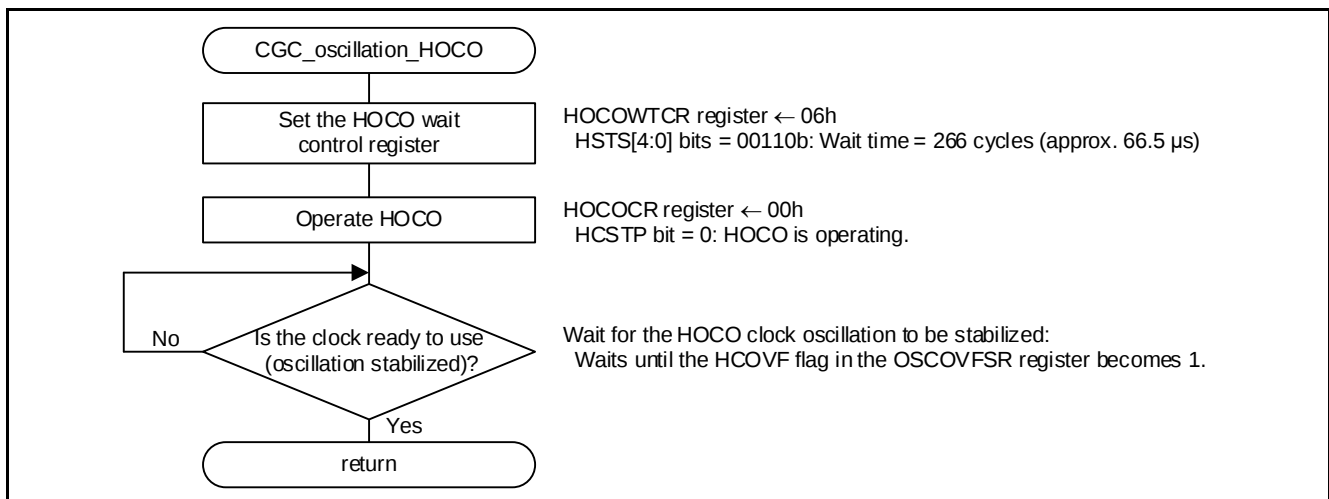
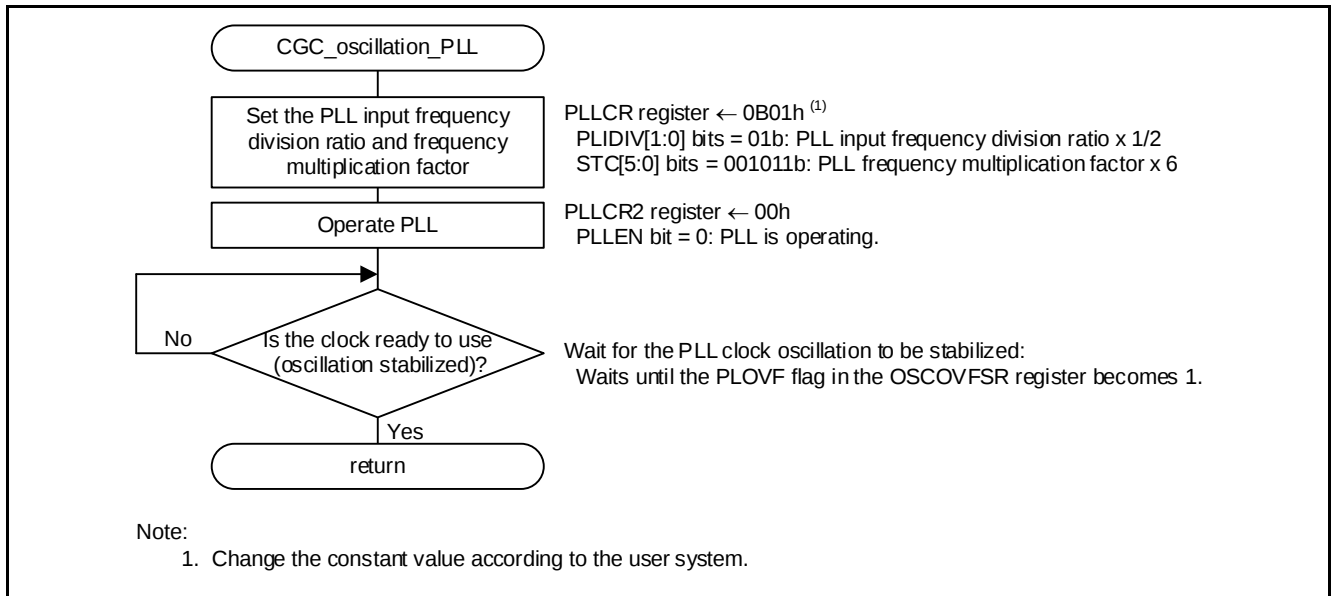


Figure 4.8 HOCO Clock Oscillation Setting

#### 4.10.7 PLL Clock Oscillation Setting

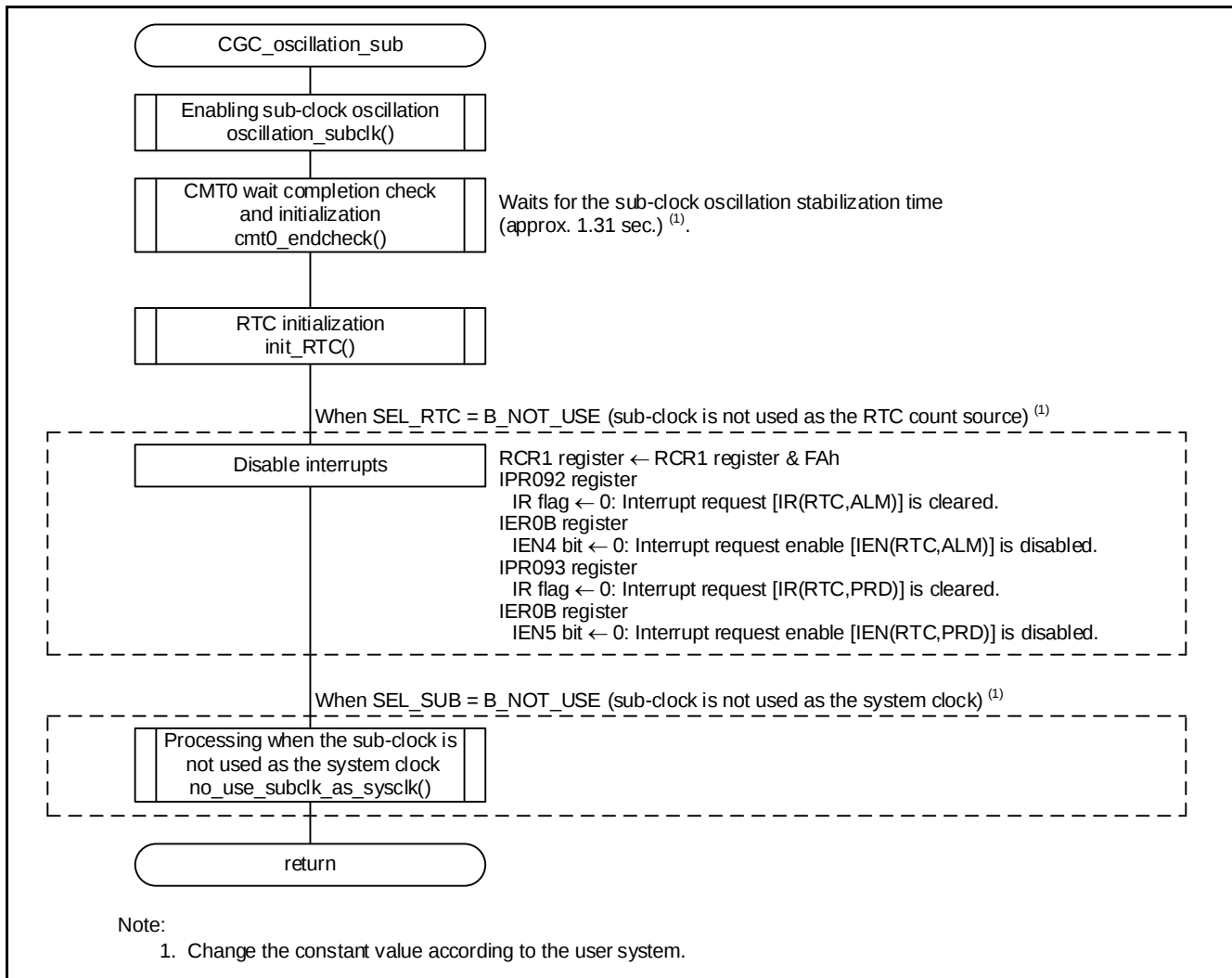
Figure 4.9 shows the PLL Clock Oscillation Setting.



**Figure 4.9 PLL Clock Oscillation Setting**

#### 4.10.8 Sub-Clock Oscillation Setting

Figure 4.10 to Figure 4.13 show the sub-clock oscillation setting.



**Figure 4.10 Sub-Clock Oscillation Setting**

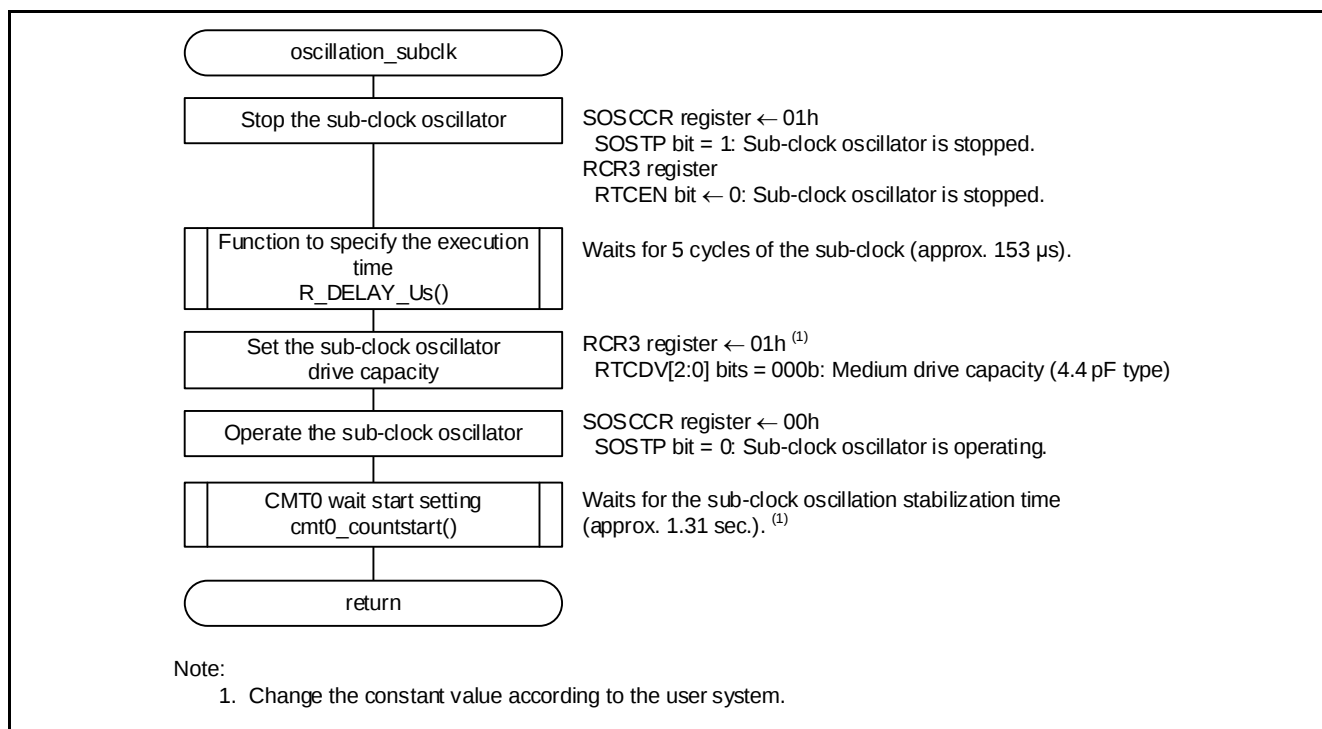


Figure 4.11 Enabling Sub-Clock Oscillation

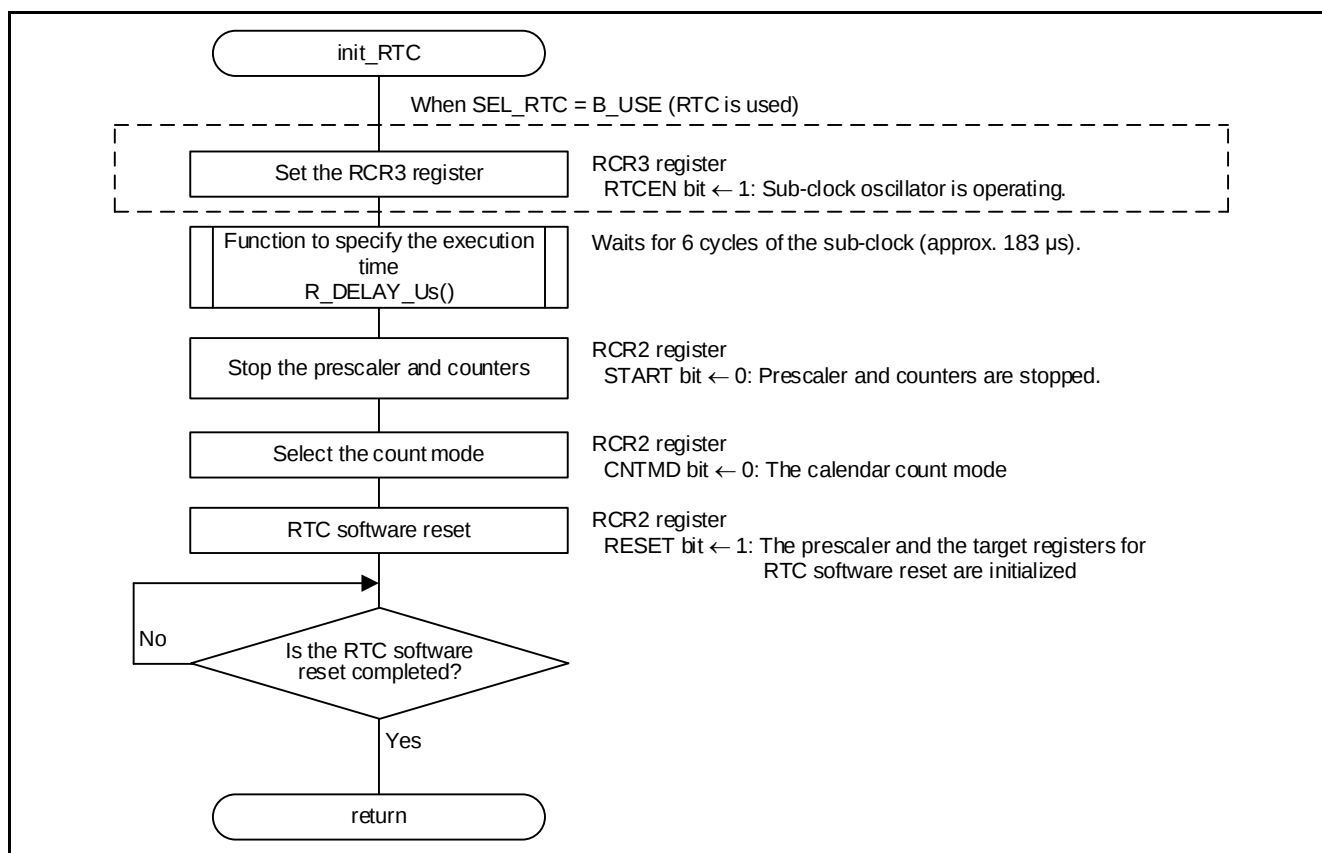


Figure 4.12 RTC initialization

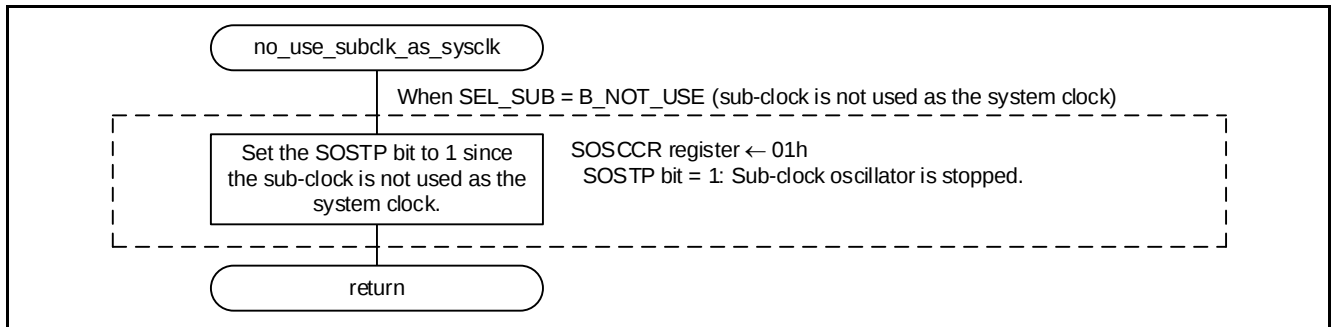


Figure 4.13 Processing when the Sub-Clock is not Used as the System Clock

#### 4.10.9 Sub-Clock Stop Setting

Figure 4.14 shows the Sub-Clock Stop Setting.

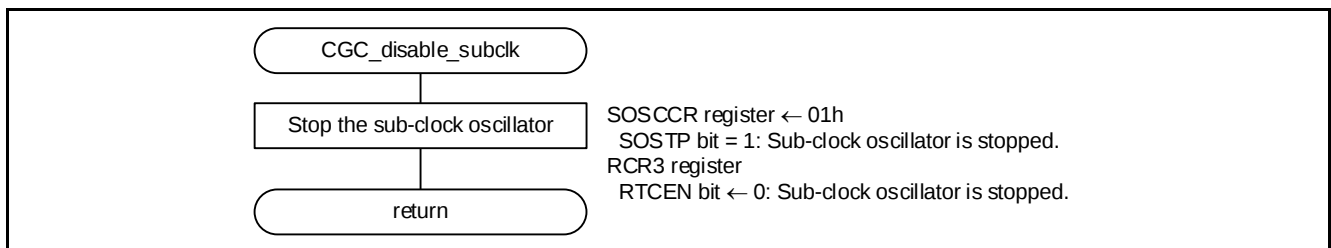


Figure 4.14 Sub-Clock Stop Setting

#### 4.10.10 CMT0 Wait Start Setting, and CMT0 Wait Completion Check and Initialization

Figure 4.15 and Figure 4.16 show the CMT0 Wait Start Setting, and CMT0 Wait Completion Check and Initialization.

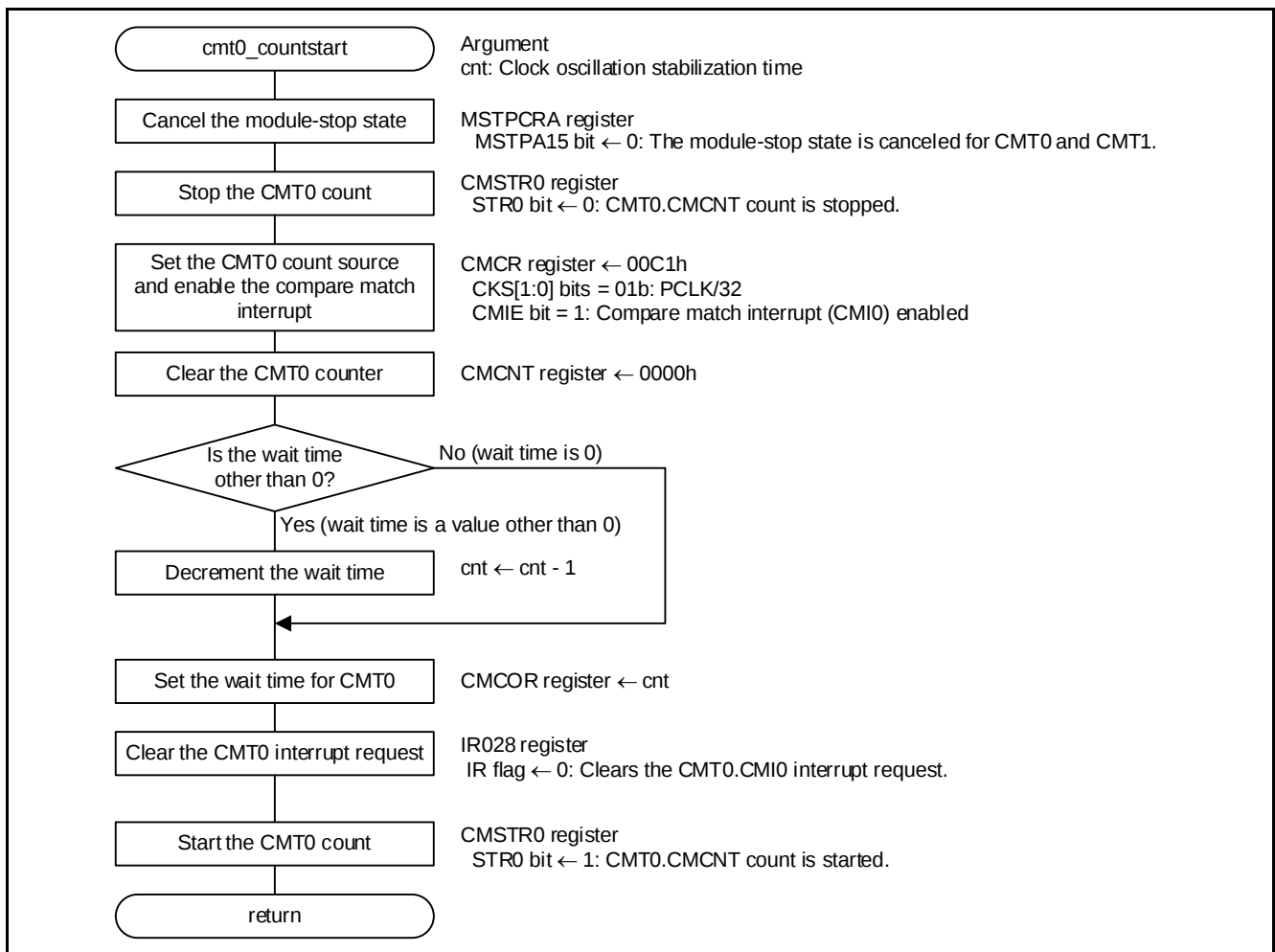


Figure 4.15 CMT0 Wait Start Setting

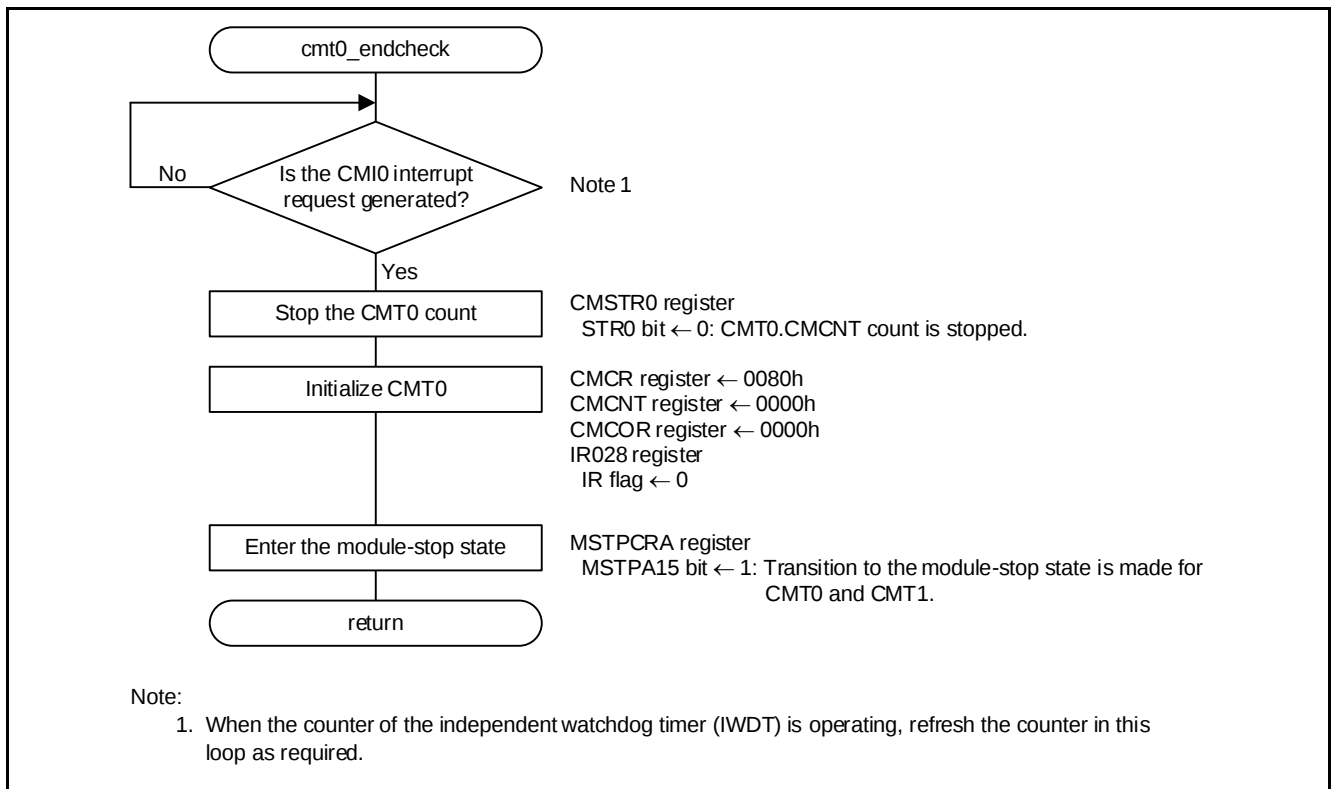


Figure 4.16 CMT0 Wait Completion Check and Initialization

## 5. Importing a Project

### 5.1 Importing a Project in the e<sup>2</sup> studio

When using the e<sup>2</sup> studio, follow the procedure shown below to import a project into the e<sup>2</sup> studio.

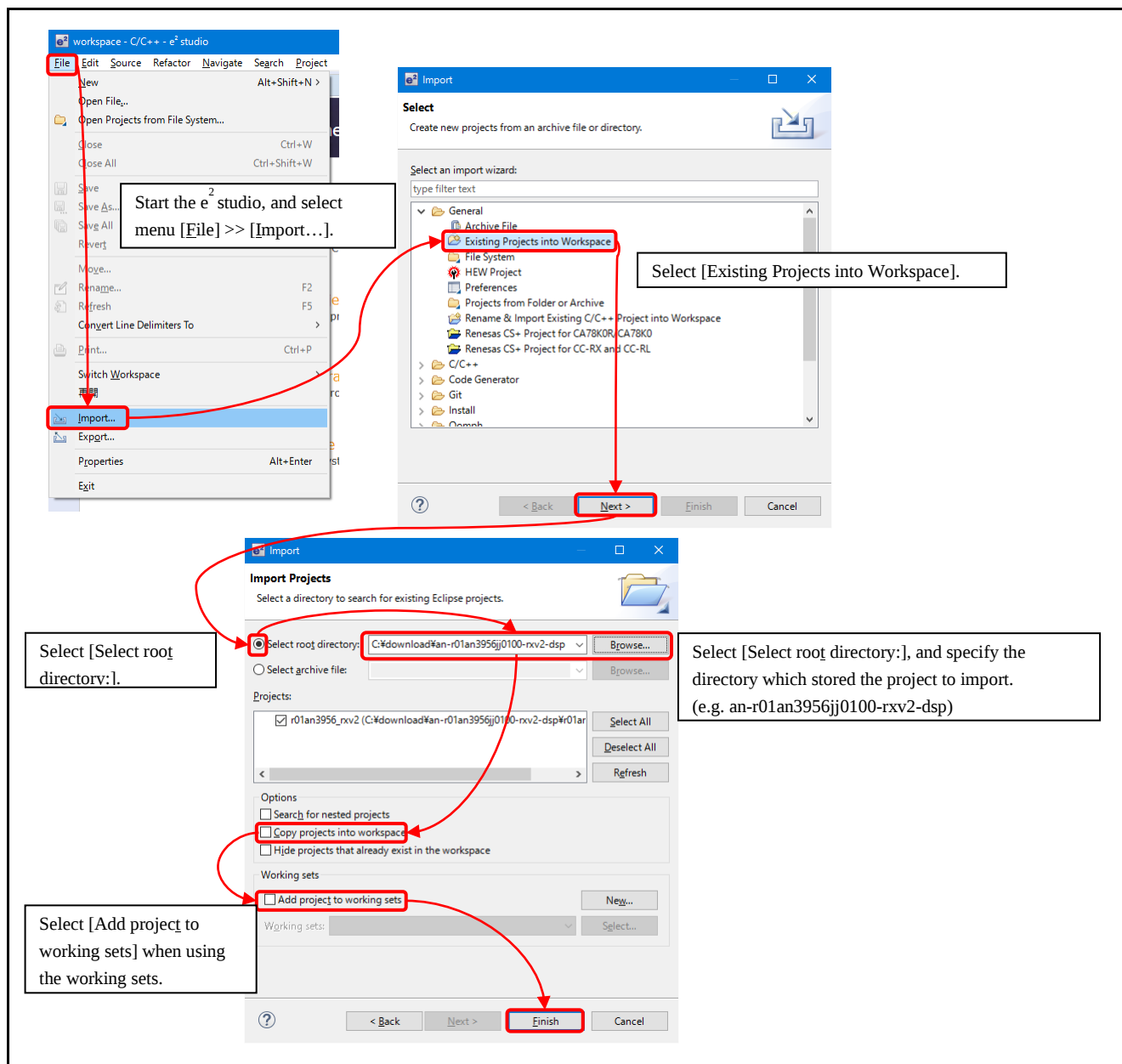


Figure 5.1 Importing a Project in the e<sup>2</sup> studio

## 5.2 Importing a Project in CS+

When using CS+, follow the procedure shown below to import a project into CS+.

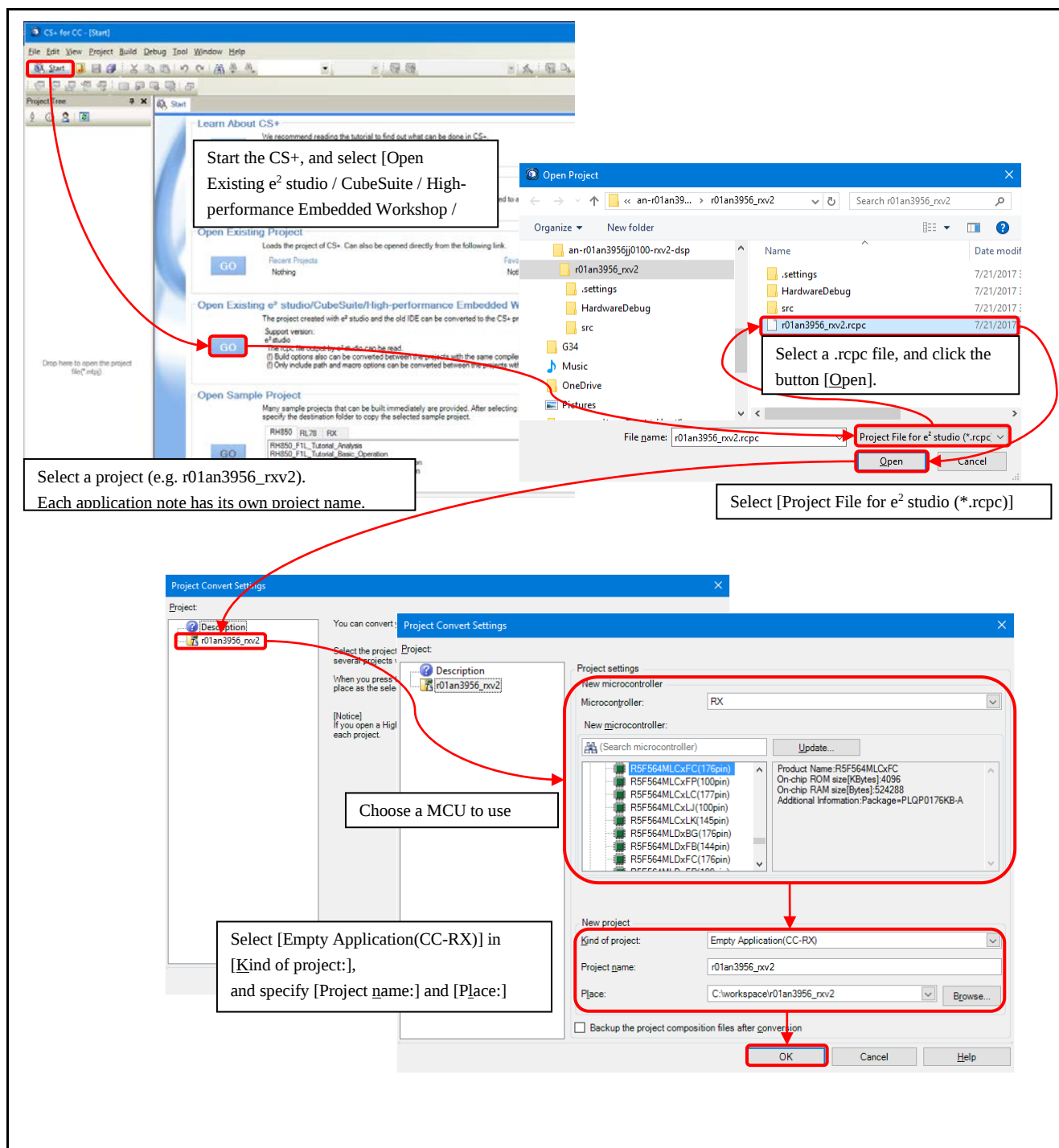


Figure 5.2 Importing a Project in CS+

## 6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 7. Reference Documents

User's Manual: Hardware

RX111 Group User's Manual: Hardware (R01UH0365EJ)

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

## Revision History

| Rev. | Date      | Description |                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |           | Page        | Summary                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1.00 | Feb.01.14 | —           | First edition issued                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1.01 | Mar.02.15 | 12,14       | Added the bit setting for the standard CL in the sub-clock oscillator drive capacity control bit.                                                                                                                                                                                                                                                                                                                                                    |
|      |           | 26          | Changed the setting value for the PRCR register.                                                                                                                                                                                                                                                                                                                                                                                                     |
|      |           | 37          | Updated the version of the reference document.                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1.02 | Dec.10.19 | —           | enable_RTC is deleted and init_RTC is added.                                                                                                                                                                                                                                                                                                                                                                                                         |
|      |           | 6           | Table 2.1 Operation Confirmation Conditions, changed.                                                                                                                                                                                                                                                                                                                                                                                                |
|      |           | 11          | 4.4 Section Composition is added.                                                                                                                                                                                                                                                                                                                                                                                                                    |
|      |           | 12          | Table 4.8 Constants Used in the Sample Code (1/2) (Users can change the constants listed in this table.), changed.                                                                                                                                                                                                                                                                                                                                   |
|      |           | 13          | Table 4.9 Constants Used in the Sample Code (2/2)(Users can change the constants listed in this table.), changed.                                                                                                                                                                                                                                                                                                                                    |
|      |           | 18          | Table 4.14 Constants when a 36-Pin Package is Used (PIN_SIZE=36), changed.                                                                                                                                                                                                                                                                                                                                                                           |
|      |           | 26          | Figure 4.5 Clock Initialization (1/2), changed.                                                                                                                                                                                                                                                                                                                                                                                                      |
|      |           | 30          | Figure 4.10 Sub-Clock Oscillation Setting, changed.                                                                                                                                                                                                                                                                                                                                                                                                  |
|      |           | 31          | Figure 4.12 RTC Initialization, changed.                                                                                                                                                                                                                                                                                                                                                                                                             |
|      |           | 32          | Figure 4.14 Processing when the Sub-Clock is not Used as the System Clock, changed.                                                                                                                                                                                                                                                                                                                                                                  |
|      |           | 37          | 7.Reference Documents, changed.                                                                                                                                                                                                                                                                                                                                                                                                                      |
|      |           | Program     | Changed the path of iodefine.h<br>Added section setting of End_of_RAM<br>Changed the function name for initialization RTC<br>From “enable_RTC” to “init_RTC”<br>Changed the following macro definition name<br>From “MAIN_CLOCK_Hz” to “MAIN_CLOCK_HZ”<br>From “SUB_CLOCK_Hz” to “SUB_CLOCK_HZ”<br>From “LOCO_CLOCK_Hz” to “LOCO_CLOCK_HZ”<br>Added confirmation processing after accessing RCR1 register<br>Added initialization when not using RTC |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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