RX62N Group, RX621 Group

Notes on Analog Power Supply Printed Circuit Board Patterns

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Introduction

This application note discusses the layout of the analog power supply lines on printed circuit boards used for RX62N Group and RX621 Group microcontroller applications.

Target Device

RX62N Group and RX621 Group microcontrollers

This application note also applies to other microcontrollers in the RX Family that have the same A/D and D/A converters as the RX62N Group and RX621 Group microcontrollers. Note, however, that since certain aspects of the functions used may be changed in other devices, the documentation for the device used must be checked carefully before using the information provided in this application note.

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1. Notes on Power Supply Pin Layout

1.1 Separating Digital and Analog Circuits

Digital and analog circuits should be separated as much as possible. In particular, avoid allowing digital signal lines to run close to or to cross analog signal lines so that digital circuit signals do not appear as noise in analog circuits.

Use the analog system ground (AVSS) to separate (isolate) the analog input pins (AN0 to AN7), the analog reference supply (VREFH), the analog system supply voltage (AVCC), and the analog reference ground (VREFL) from the digital circuits. Furthermore, both the analog reference ground (VREFL) and the analog system ground (AVSS) should be connected to a stable ground (VSS) at a single point.

To acquire high-quality analog I/O, if at all possible, allocate the analog ground plane and the digital ground plane to different layers in the printed circuit board.

The table below lists the setting ranges for analog pins. The AVCC, AVSS, VREFH, and VREFL pins must not be left open even if the A/D and D/A converters are not used.

Table 1 Analog Pin Setting Ranges

Analog Pin	When an A/D or D/A converter is used	When the A/D and D/A converters are not used
AVCC	AVCC = VCC	AVCC = VCC
AVSS	AVSS = VSS*[1]	AVSS = VSS
VREFH	VREFH = 2.7 V to AVCC	VREFH = AVCC
VREFL	VREFL = VSS*[1]	VREFL = VSS
ANn	VREFL ≤ VAN ≤ VREFH*[2]	*[4]
DAn	VREFL ≤ VDA ≤ VREFH*[3]	*[4]

Notes: 1. AVSS and VREFL should be connected to a stable ground (VSS) at a single point.
2. VAN: Voltage applied to the analog input pin ANn.
3. VDA: D/A converter output voltage
4. Unused pins must be handled as directed in the Hardware Manual for the device used.

1.2 Power Supply Pin Capacitors

Insert a 0.1 µF capacitor between each of the following pairs: between VCC and VSS, between AVCC and AVSS, and between VREFH and VREFL. Design the layout so that each of these power supply capacitors forms the shortest closed loop possible. The lengths of these lines between capacitor and power supply pin must be made as equal as possible and furthermore, as short as possible. Also, the power supply lines and ground lines should be made as wide as possible.

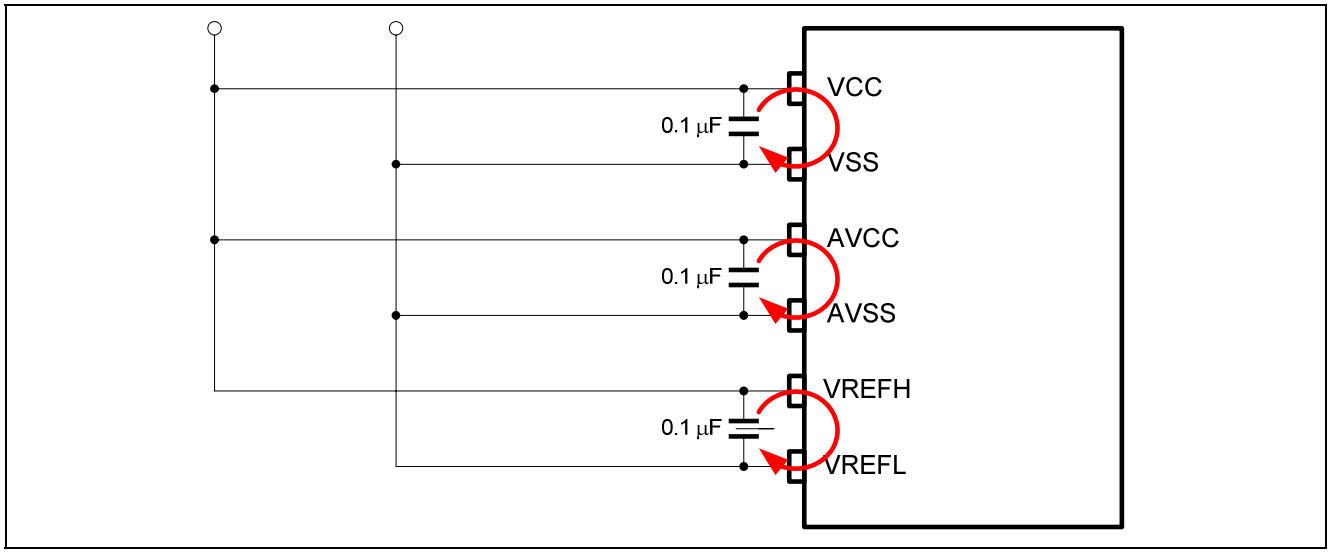


Figure 1 Power Supply Pin Capacitors and Closed Loops

1.3 Power Supply Pin Layout Examples

This section presents examples of analog power supply pin capacitor layouts using 4-layer printed circuit boards.

The board surfaces are allocated as follows: the top surface is the component plane, layer 2 is the ground plane, layer 3 is the power supply plane, and the back surface is the solder plane. After capacitor decoupling, each of the AVCC, VREFH, AVSS, and VREFL pins should be connected to the corresponding power supply plane. Although this example only shows the analog power supply pins, similar decoupling should also be used between VCC and VSS.

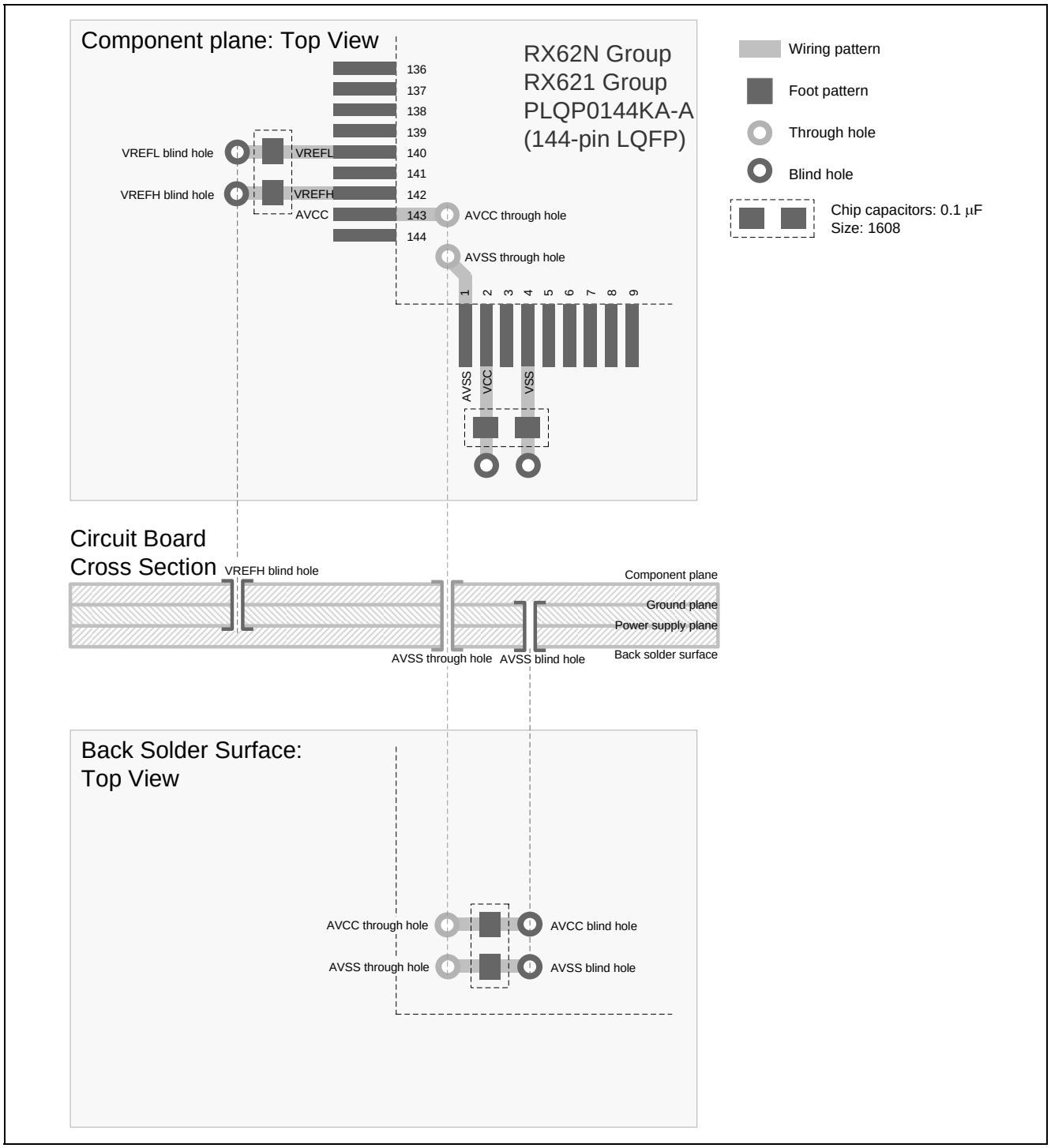


Figure 2 RX62N and RX621 144-Pin LQFP Package Power Supply Pin Capacitor Layout Example

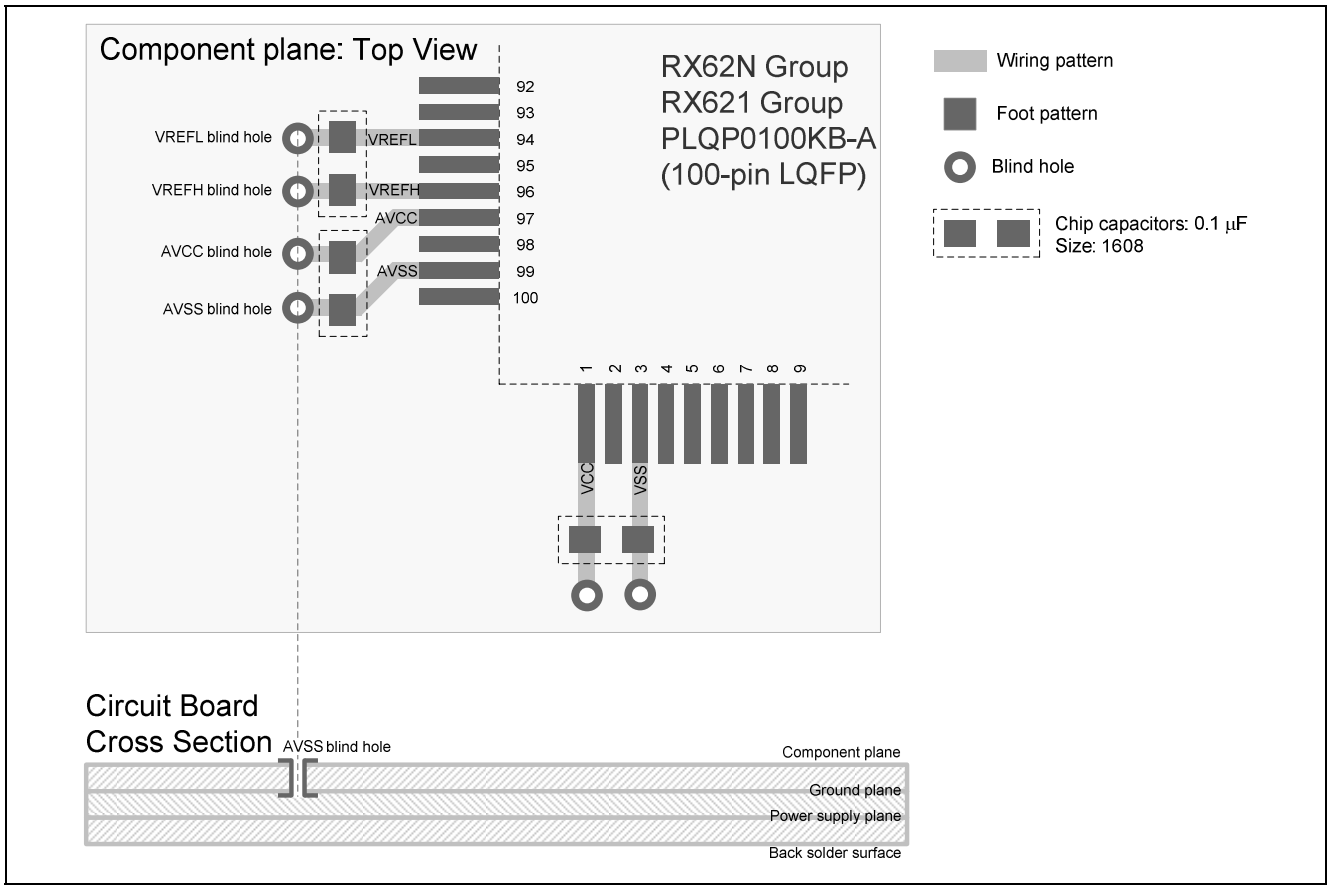
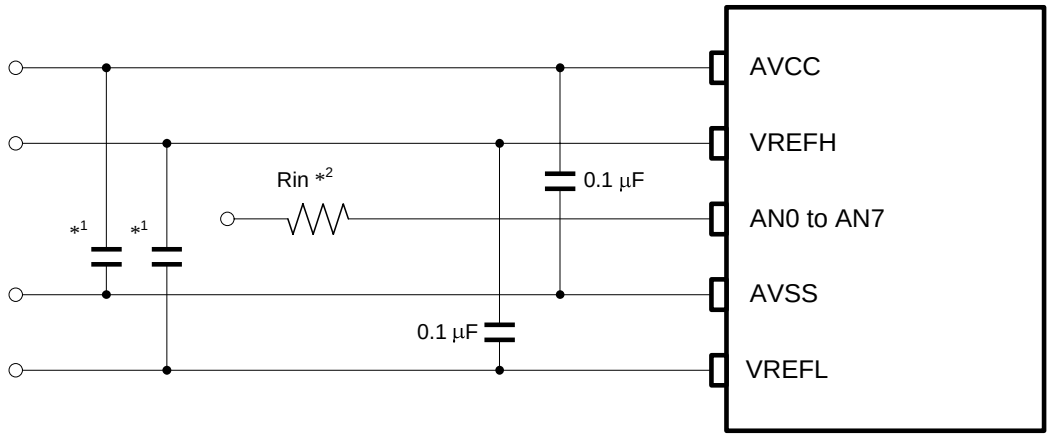


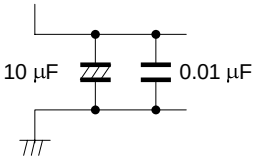
Figure 3 RX62N and RX621 100-Pin LQFP Package Power Supply Pin Capacitor Layout Example

1.4 Reducing Noise in Power Supply Lines

The 10 µF and 0.01 µF (values provided for reference purposes) capacitors shown in the circuit diagrams in the Hardware Manual for each microcontroller product are included as bypass capacitors for the analog power supply lines. The actual capacitances and layout details for these capacitors must be analyzed in conjunction with the end product or system characteristics (for example locating them near the power supply itself).



Notes: 1. The capacitance values indicated are for reference purposes only.



2. Rin: Signal source impedance

Figure 4 Reducing Noise in Power Supply Lines

2. Reference Documents

- Hardware Manual
  RX62N Group, RX621 Group User's Manual: Hardware
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates
  (The latest information can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.07.11	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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