Introduction

This application note describes a sample program that performs a failure detection test of the on-chip extended RAM (Data RAM 512KB) by using data comparison mode of the data operation circuit (DOC).

The major features of the program are listed below.

- The DOC compares data with reference data that is pre-set.
- When transfer of all data of the on-chip extended RAM (512 Kbytes) is complete, the DOC turns LED0 on. When the result of the comparison differs from the reference data, the DOC notifies an error to the error control module (ECM) and turns LED1 on by an ECM error detection interrupt.

Target Devices for Operation Checking

RZ/T1 Group

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

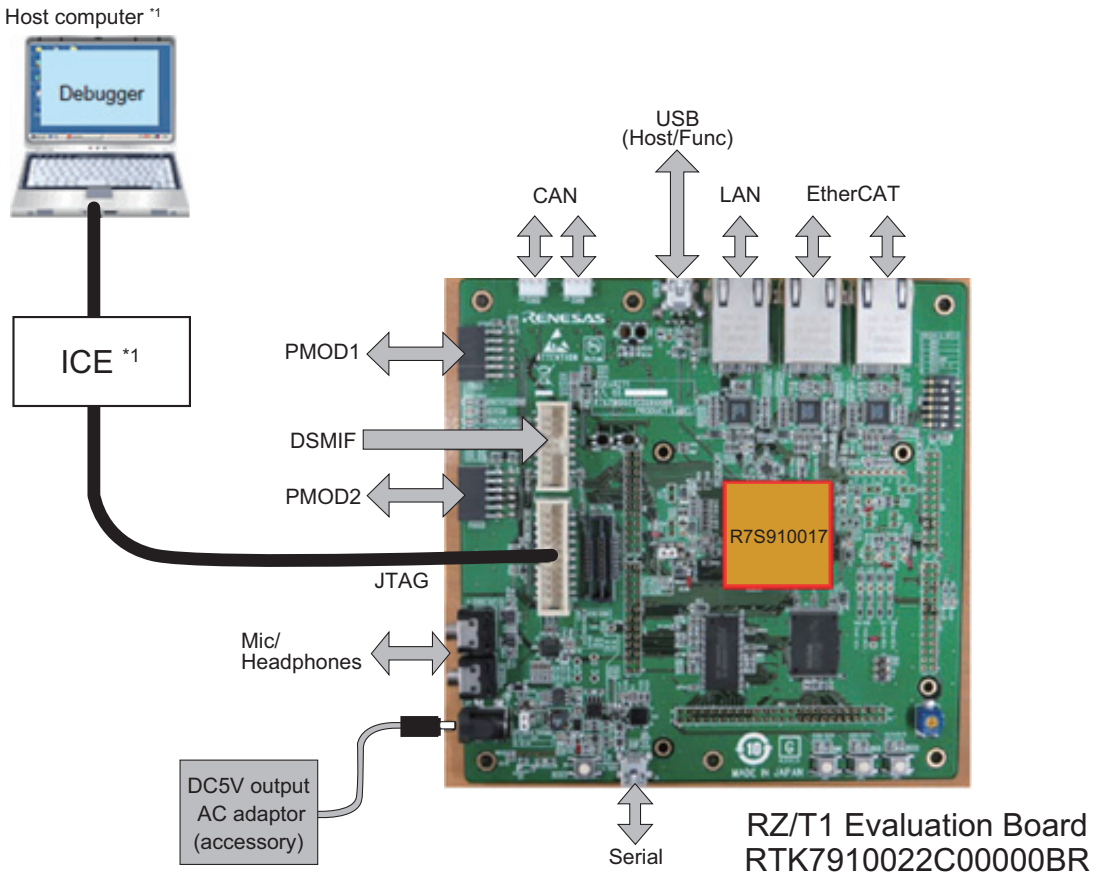
Table of Contents

1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications and Figure 1.1 shows the operating environment.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Clock pulse generator (CPG)	The CPG produces the CPU clock and low-speed on-chip oscillator clock signals
Interrupt controller unit (ICUA)	The ICUA is used for ECM error detection maskable interrupt (ERRD), DMA transfer software startup interrupt (DMASRQ0), and DMA transfer error interrupt (DMAERR0).
Data operation circuit (DOC)	The DOC is used to compare data
DMA controller (DMACAa)	DMACAa transfers data in the on-chip extended RAM to the DOC data input register
Error control module (ECM)	The ECM is used to initialize the ERROROUT# pins and used for ECM error detection interrupts
General input/output port	The general I/O port is used to control pins for turning the LEDs on and off



Note 1. Indicates the device that the user needs to prepare.

Figure 1.1 Operating Environment

2. Operating Environment

The sample program of this application is for the environment below.

Table 2.1 Operating Environment

Item	Description
Microcomputer	RZ/T1 Group
Operating frequency	CPUCLK = 450 MHz
Operating voltage	3.3 V
Integrated Development Environment	Manufactured by IAR Systems Embedded Workbench® for Arm Version 8.20.2 Manufactured by Arm DS-5™ 5.26.2 Manufactured by RENESAS e2studio 6.1.0
Operating modes	SPI boot mode 16-bit bus boot mode
Board	RZ/T1 Evaluation board (RTK7910022C00000BR)
Devices (functions to be used on the board)	• NOR flash memory (connected to CS0/CS1 space) Manufacturer: Macronix International Co. Ltd. Model: MX29GL512FLT2I-10Q • SDRAM (connected to CS2/CS3 space) Manufacturer: Integrated Silicon Solution Inc. Model: IS42S16320D-7TL • Serial flash memory Manufacturer: Macronix International Co. Ltd. Model: MX25L51245G

3. Related Documents

The application note related to this application note is given below for reference.

- RZ/T1 Group Initial Settings

4. Peripheral Functions

For the basics of the clock pulse generator (CPG), interrupt controller unit (ICUA), error control module (ECM), data operation circuit (DOC), DMA controller (DMAC), and general input/output port, refer to the RZ/T1 Group User's Manual: Hardware.

5. Hardware

5.1 Example of Hardware Configuration

Figure 5.1 shows an example of the hardware configuration.

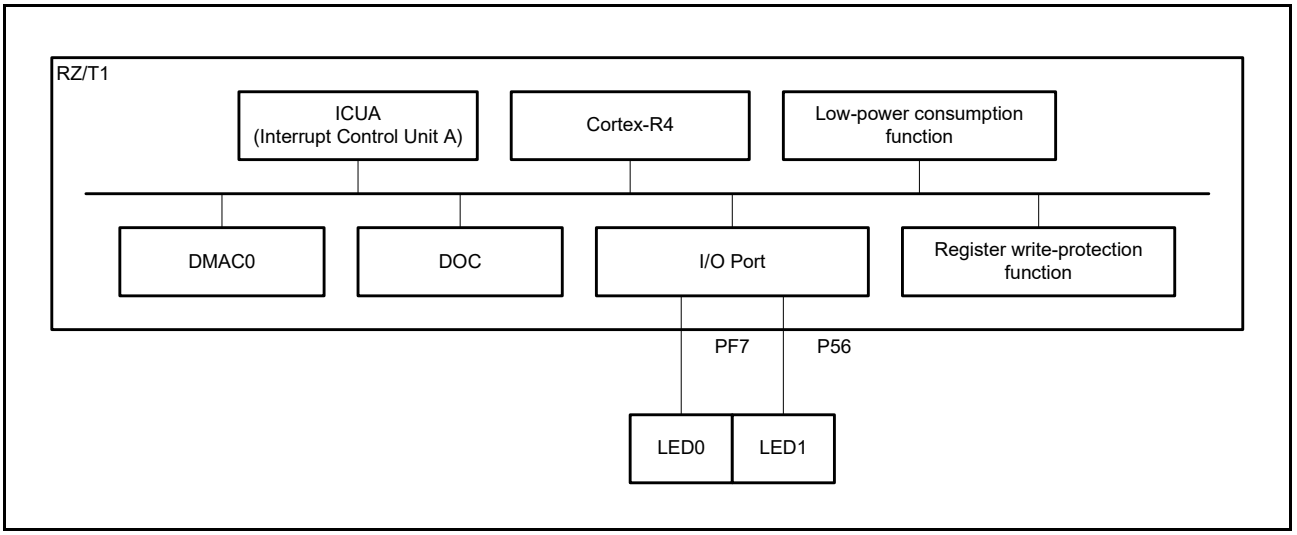


Figure 5.1 Example of Hardware Configuration

5.2 Pins

Table 5.1 lists pins to be used and their functions.

Table 5.1 Pins and Functions

Pin Name	I/O	Function
MD0	Input	Selection of operating modes MD0 = L, MD1 = L, MD2 = L (SPI boot mode) MD0 = L, MD1 = H, MD2 = L (16-bit bus boot mode)
MD1	Input	
MD2	Input	
PF7	Output	Turning LED0 on and off
P56	Output	Turning LED1 on and off

6. Software

6.1 Operation Overview

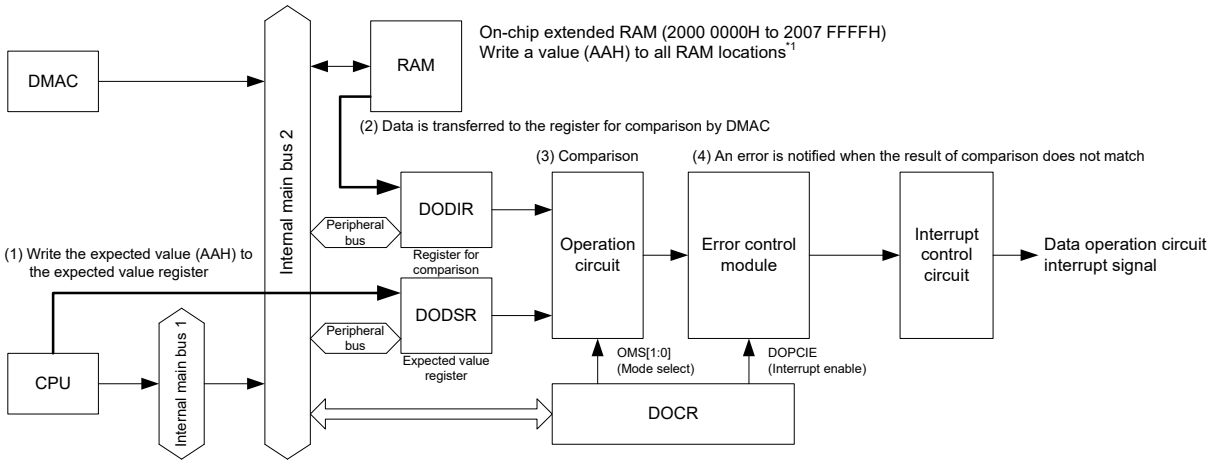
The sample program makes the initial settings of the data operation circuit (DOC) by writing data to the on-chip extended RAM (AAH). Then, the data in the on-chip extended RAM is transferred to the DOC data input register in 16-bit units in sequence by using the DMA controller (DMAC0). When the transfer of the all data in the on-chip extended RAM is complete, a DMA transfer complete interrupt is generated. LED0 is turned on in response to the interrupt processing.

When the value written in advance to the DOC data setting register and the data transferred to the DOC data input register do not match, the DOC notifies the ECM of an error and an ECM error detection interrupt is generated. LED1 is turned on as part of the interrupt processing.

Table 6.1 shows the operation overview of the sample program and Figure 6.1 illustrates the image of operations.

Table 6.1 Operation Overview

Function	Description
Data operating function	Comparison of 16-bit data
Interrupt	The result of data comparison is not a match.



DOCR: DOC control register
DODIR: DOC data input register
DODSR: DOC data setting register

Note 1. When data is written to all locations of the RAM, the data will be written to the mirror area (2200 0000H to 2207 FFFFH).

Figure 6.1 Image of Operations

6.1.1 Project Settings

For the settings of the project to be used on the EWARM for development environment, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2 Memory Map

For the address space of the RZ/T1 Group and a memory map of the RZ/T1 evaluation board, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.1 Assignment to Sections of Sample Program

Refer to the Application Note: RZ/T1 Group Initial Settings for the sections to be used in the program, assignment to sections (loading view) of the sample program in its initial state, and assignment to sections of the sample program following the application of scatter loading (execution view).

6.2.2 MPU Settings

For the settings of the MPU, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.3 Exception Processing Vector Table

For the vector table of exception processing, refer to the Application Note: RZ/T1 Group Initial Settings.

6.3 List of Interrupts

Table 6.2 shows interrupts to be used in the sample program.

Table 6.2 Interrupts for Sample Program

Interrupts (Source ID)	Priority	Description
ECM error detection interrupt (ERRD)	15	To check whether a data operation circuit error flag has been set, LED1 is turned on in case of an error.
DMA transfer software startup interrupt (DMASRQ0)	15	When DMA transfer of all data of the on-chip extended RAM, LED0 is turned on and the failure detection test of the on-chip extended RAM is complete.
DMA transfer error interrupt (DMAERR0)	15	To acknowledge that a data transfer error occurred.

6.4 Fixed-Width Integer Types

Table 6.3 lists fixed-width integers to be used in the sample program.

Table 6.3 Fixed-Width Integers for Sample Program

Symbol	Description
int8_t	8-bit signed integer (defined in the standard library)
int16_t	16-bit signed integer (defined in the standard library)
int32_t	32-bit signed integer (defined in the standard library)
int64_t	64-bit signed integer (defined in the standard library)
uint8_t	8-bit unsigned integer (defined in the standard library)
uint16_t	16-bit unsigned integer (defined in the standard library)
uint32_t	32-bit unsigned integer (defined in the standard library)
uint64_t	64-bit unsigned integer (defined in the standard library)

6.5 Constants/Error Codes

Table 6.4 lists constants of the sample program.

Table 6.4 Constants for Sample Program

Constant	Setting Value	Description
DOC_STAT_FLAG_SET	(1)	Indicates that the status flag is 1.
DOC_STAT_FLAG_CLEAR	(0)	Indicates that the status flag is 0.
DOC_CFG_PARAM_CHECKING_ENABLE	(1)	Indicates that parameter checking is enabled (1) or disabled (0) by using API function of the DOC.

6.6 Structures/Unions/Emulate Types

Figure 6.2 and Figure 6.3 show the structures, unions, and emulate types to be used in the sample program.

```
/* API ERROR RETURN CODES */
typedef enum e_doc_err            // DOC API error codes
{
    DOC_SUCCESS=0,
    DOC_ERR_OPEN_IGNORED,       // The module has already been Open()ed
    DOC_ERR_INVALID_ARG,        // Argument is not valid for parameter
    DOC_ERR_NULL_PTR,           // Received null pointer or missing required argument
    DOC_ERR_NOT_OPENED          // Open function has not yet been called
} doc_err_t;

/* Open() DEFINITIONS */
typedef enum e_doc_mode                  // DOC operation mode
{
    DOC_COMPARISON   = 0x00u,            // Data comparison mode
    DOC_ADDITION     = 0x01u,            // Data addition mode
    DOC_SUBSTRACTION = 0x02u,            // Data substraction mode
    DOC_PROHIBITED
} doc_mode_t;

typedef enum e_doc_detect                // DOC detection condition
{
    DOC_MISMATCH  = 0x00u,               // Data mismatch is detected
    DOC_MATCH     = 0x04u                // Data match is detected
} doc_detect_t;

typedef enum e_doc_interrupt             // DOC interrupt enable setting
{
    DOC_INTERRUPT_DISABLE = 0x00u,   // Disables interrupt from DOC
    DOC_INTERRUPT_ENABLE  = 0x10u    // Enables interrupt from DOC
} doc_interrupt_t;
```

Figure 6.2 Structures/Unions/Enumerated Types for Sample Program

```
typedef struct st_doc_config              // DOC configuration options used in Open function
{
      doc_mode_t          mode;                  // DOC operation mode
      doc_detect_t        detect;              // DOC detection condition
      doc_interrupt_t     interrupt;       // DOC interrupt enable setting
} doc_config_t;

/* Control() DEFINITIONS */
typedef enum e_doc_cmd                // Command used in Control function
{
      DOC_CMD_GET_STATUS,               // Get DOC status flag
      DOC_CMD_CLEAR_STATUS              // Clear DOC status flag
} doc_cmd_t;
```

Figure 6.3 Structures/Unions/Enumerated Types for Sample Program

6.7 Functions

Table 6.5 lists the functions to be used.

Table 6.5 Functions

Function	Page Number
main	14
init_ram	14
doc_init	15
test_ram	15
dmac0_init	15
R_DOC_Open	16
R_DOC_Control	16
R_IRQ20_isr	17
R_IRQ251_isr	17
R_IRQ293_isr	17

6.8 Specifications of Sample Program Functions

6.8.1 main

main	
Synopsis	Main processing
Declaration	int main (void)
Description	This function makes initial settings of the ports, ECM, ICU, DOC, DMAC, and on-chip extended RAM.
Arguments	None
Return value	None
Supplement	None

6.8.2 init_ram

init_ram		
Synopsis	Initializing the on-chip extended RAM	
Declaration	void init_ram (uint32_t value)	
Description	This function initializes the 512-Kbyte area starting from 2200 0000H with the value of the value argument.	
Arguments	uint32_t value	Specifies the value to be initialized
Return value	None	
Supplement	None	

6.8.3 doc_init

doc_init	
Synopsis	Initializing data operation circuit
Declaration	void doc_init (void)
Description	This function makes initial settings of the data operation circuit.
Arguments	None
Return value	None
Supplement	None

6.8.4 test_ram

test_ram	
Synopsis	Detecting failures of the on-chip extended RAM
Declaration	void test_ram (void)
Description	This function initializes the DMA controller (DMAC0) and performs DMA transfer of the data in the on-chip extended RAM to the DOC data input register in sequence.
Arguments	None
Return value	None
Supplement	None

6.8.5 dmac0_init

dmac0_init	
Synopsis	Initializing DMA controller (DMAC0)
Declaration	void dmac0_init (void)
Description	This function makes initial settings of the DMAC0.
Arguments	None
Return value	None
Supplement	None

6.8.6 R_DOC_Open

R_DOC_Open		
Synopsis	DOC open	
Header	r_doc_if.h	
Declaration	doc_err_t R_DOC_Open (void * const p_cfg)	
Description	This function initializes the DOC-related registers.	
Arguments	void * const p_cfg	The pointer that stores data group to be set in the DOC control register Operating modes DOC_COMPARISON DOC_ADDITION DOC_SUBTRACTION Selection of conditions for detection DOC_MISMATCH DOC_MATCH Data operation circuit interrupt enabling DOC_INTERRUPT_DISABLE DOC_INTERRUPT_ENABLE
Return value	The result of execution of the open function DOC_SUCCESS: DOC initialized DOC_ERR_OPEN_IGNORED: DOC opened DOC_ERR_INVALID_ARG: Invalid values included in the element of the p_cfg structure DOC_ERR_NULL_PTR: p_cfg pointer null	
Supplement	Setting DOC_CFG_PARAM_CHECKING_ENABLE that is defined by r_doc_config.h to 1 enables checking of the parameters of the arguments.	

6.8.7 R_DOC_Control

R_DOC_Control		
Synopsis	DOC control	
Header	r_doc_if.h	
Declaration	doc_err_t R_DOC_Control (doc_cmd_t const cmd, uint8_t * p_status)	
Description	This function reads and clears the state of the DOC.	
Arguments	doc_cmd_t const cmd	Specifies the command to be executed DOC_CMD_GET_STATUS DOC_CMD_CLEAR_STATUS
	uint8_t * p_status	The pointer to the position of storage of the status flags
Return value	The result of the execution of the control function DOC_SUCCESS : Normal termination DOC_ERR_INVALID_ARG: Invalid argument value DOC_ERR_NULL_PTR : p_status null DOC_ERR_NOT_OPENED: Open unread	
Supplement	Setting DOC_CFG_PARAM_CHECKING_ENABLE that is defined by r_doc_config.h to 1 enables checking of the parameters of the arguments.	

6.8.8 R_IRQ20_isr

R_IRQ20_isr	
Synopsis	IRQ20 interrupt (ECM error detection maskable interrupt)
Declaration	void R_IRQ20_isr (void)
Description	This function confirms the data operation circuit flag. LED1 is turned on when an error occurs. It clears the data operation circuit flag.
Arguments	None
Return value	None
Supplement	None

6.8.9 R_IRQ251_isr

R_IRQ251_isr	
Synopsis	IRQ251 interrupt (DMA transfer software startup interrupt)
Declaration	void R_IRQ251_isr (void)
Description	This function turns LED0 on when data transfer is complete.
Arguments	None
Return value	None
Supplement	This interrupt source triggers the DMAC as a software startup source and is conveyed to the interrupt controller on completion of the DAM transfer as a DAM transfer completed interrupt.

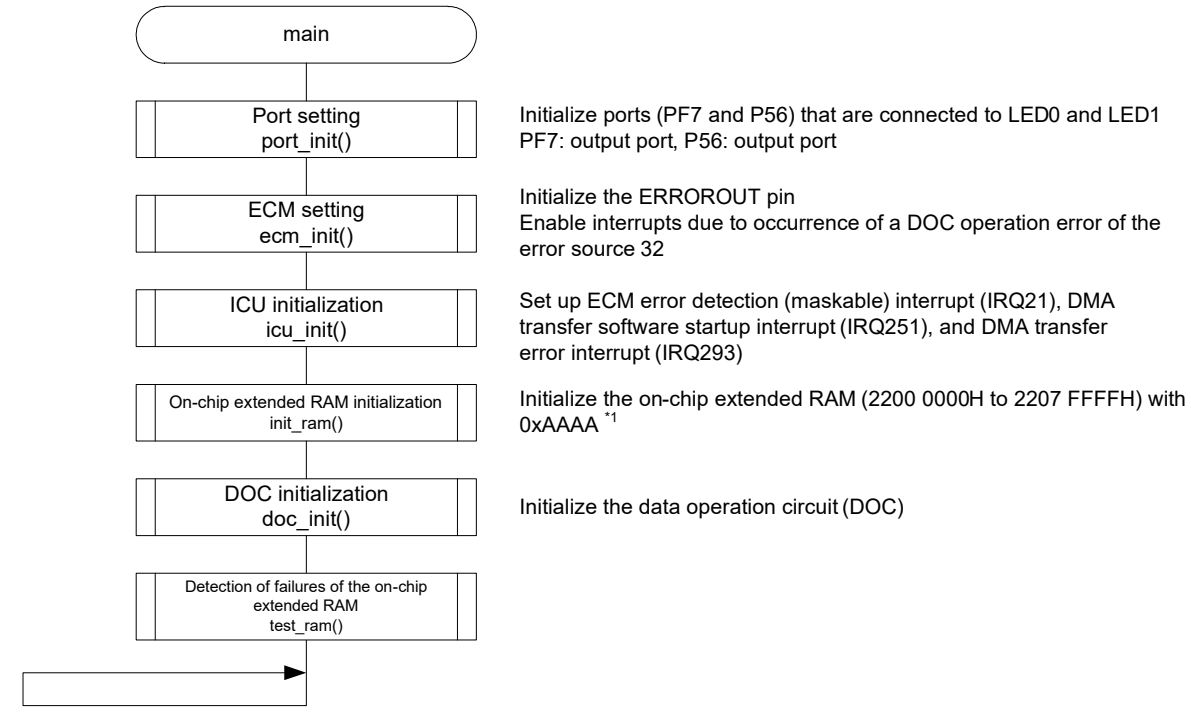
6.8.10 R_IRQ293_isr

R_IRQ293_isr	
Synopsis	IRQ293 interrupt (DMA transfer error interrupt)
Declaration	void R_IRQ293_isr (void)
Description	This function recognizes bus errors.
Arguments	None
Return value	None
Supplement	The program will not be in place if a bus error occurs. Add the program as required.

6.9 Flowcharts

6.9.1 Main Processing

Figure 6.4 show a flow chart of main processing.



Note 1. Mirror area

Figure 6.4 Main Processing

6.9.2 Initialization of On-Chip Extended RAM

Figure 6.5 show a flowchart of processing of initialization of the on-chip extended RAM.

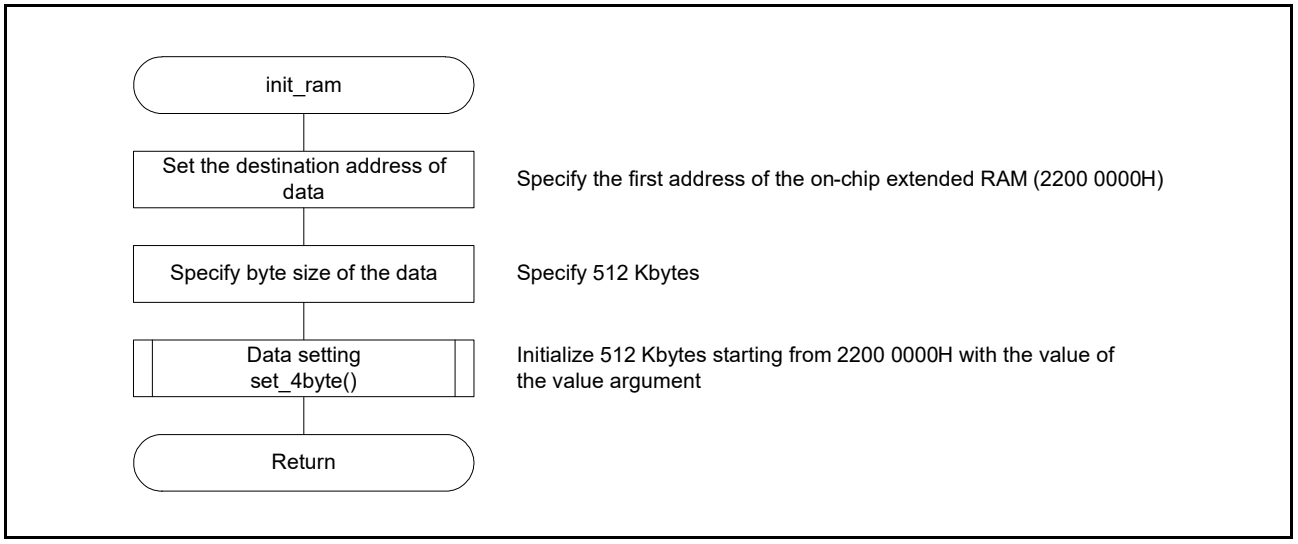


Figure 6.5 Initialization of On-chip Extended RAM

6.9.3 Initialization of Data Operation Circuit

Figure 6.6 shows a flowchart of processing of initialization of the data operation circuit.

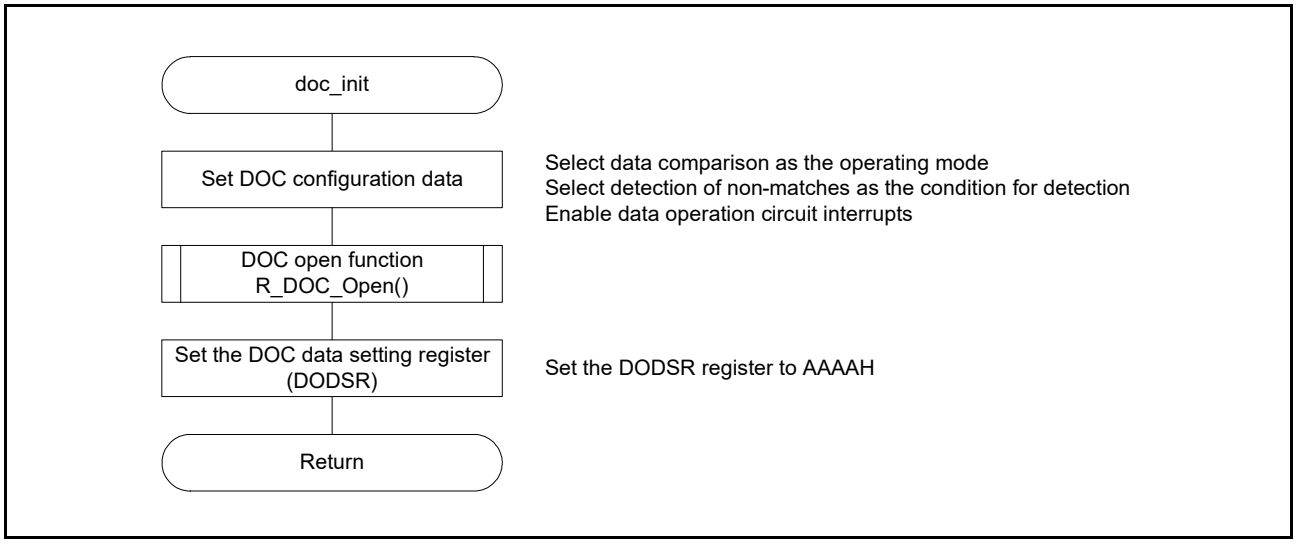


Figure 6.6 Initialization of Data Operation Circuit

6.9.4 Detection of Failure of On-chip Extended RAM

Figure 6.7 shows a flowchart of detecting failures of the on-chip extended RAM.

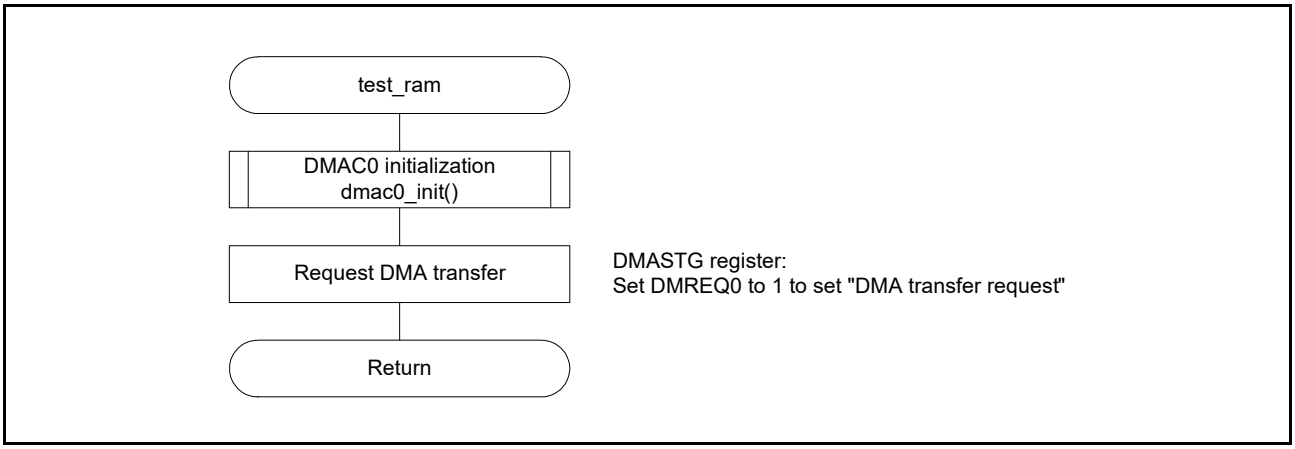


Figure 6.7 Detecting Failures of On-Chip Extended RAM

6.9.5 Initialization of DMA Controller

Figure 6.8 shows a flowchart of processing of initialization of the DMA controller.

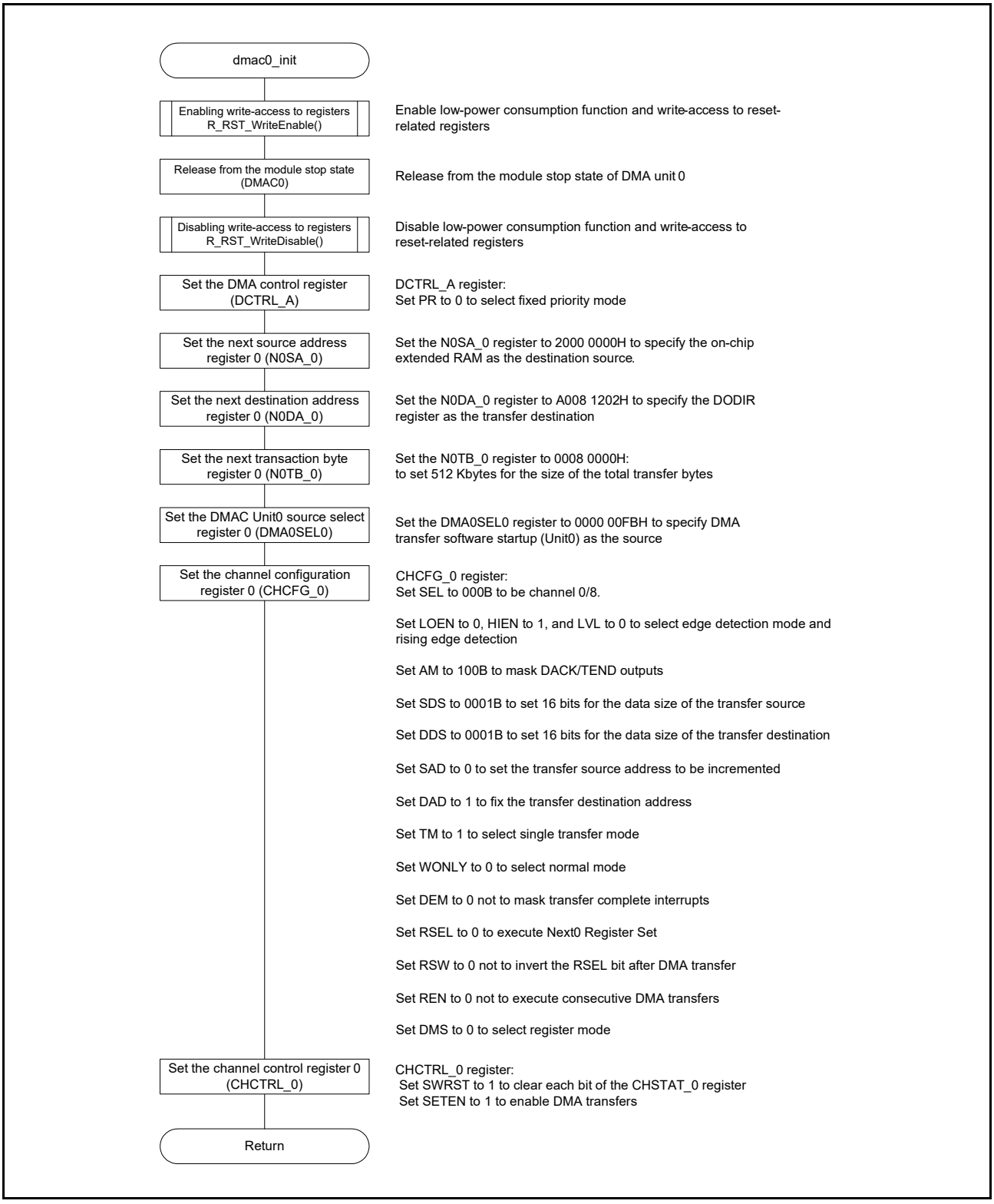
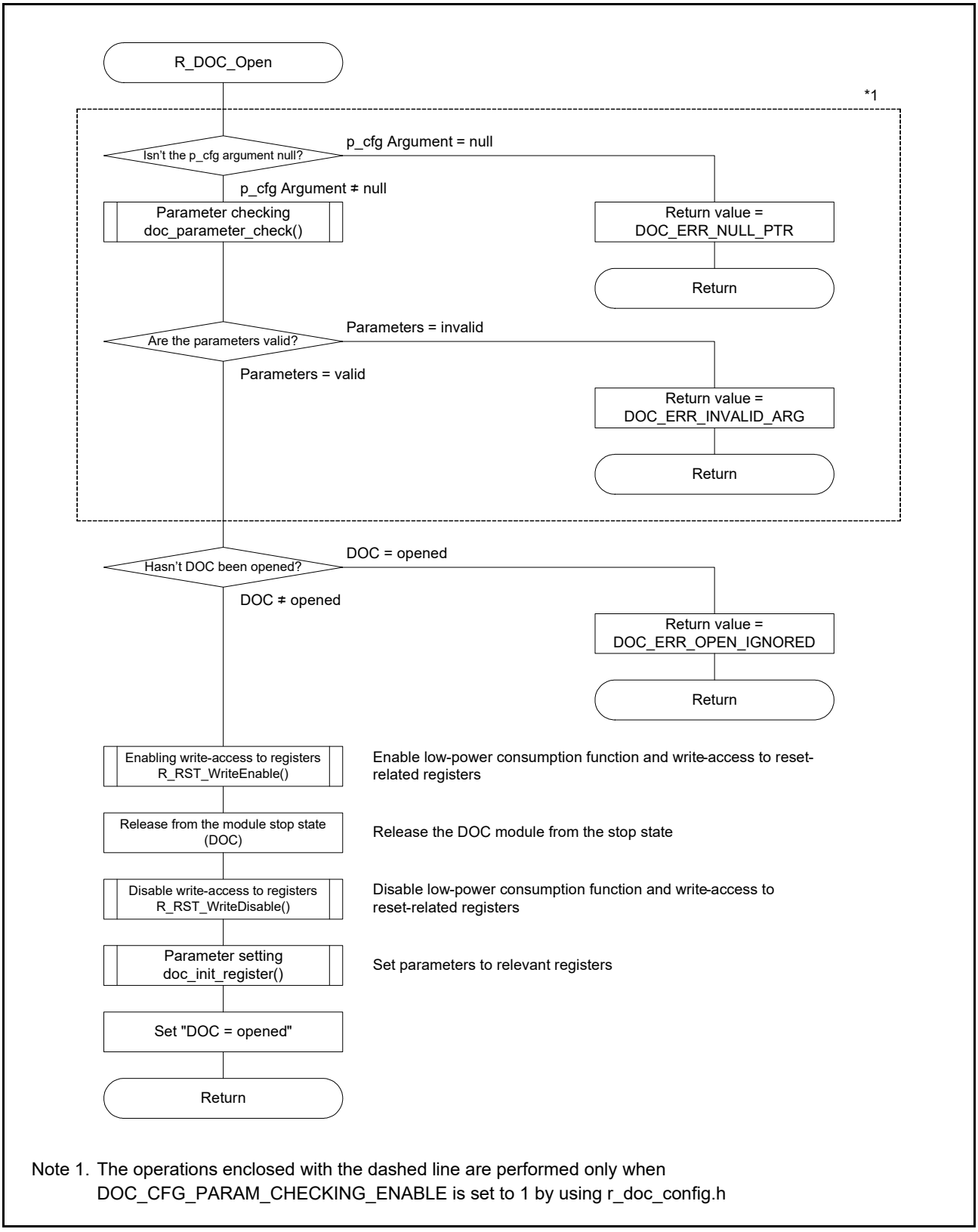


Figure 6.8 Initialization of DMA Controller

6.9.6 DOC Open Function

Figure 6.9 shows a flowchart of the DOC open function.

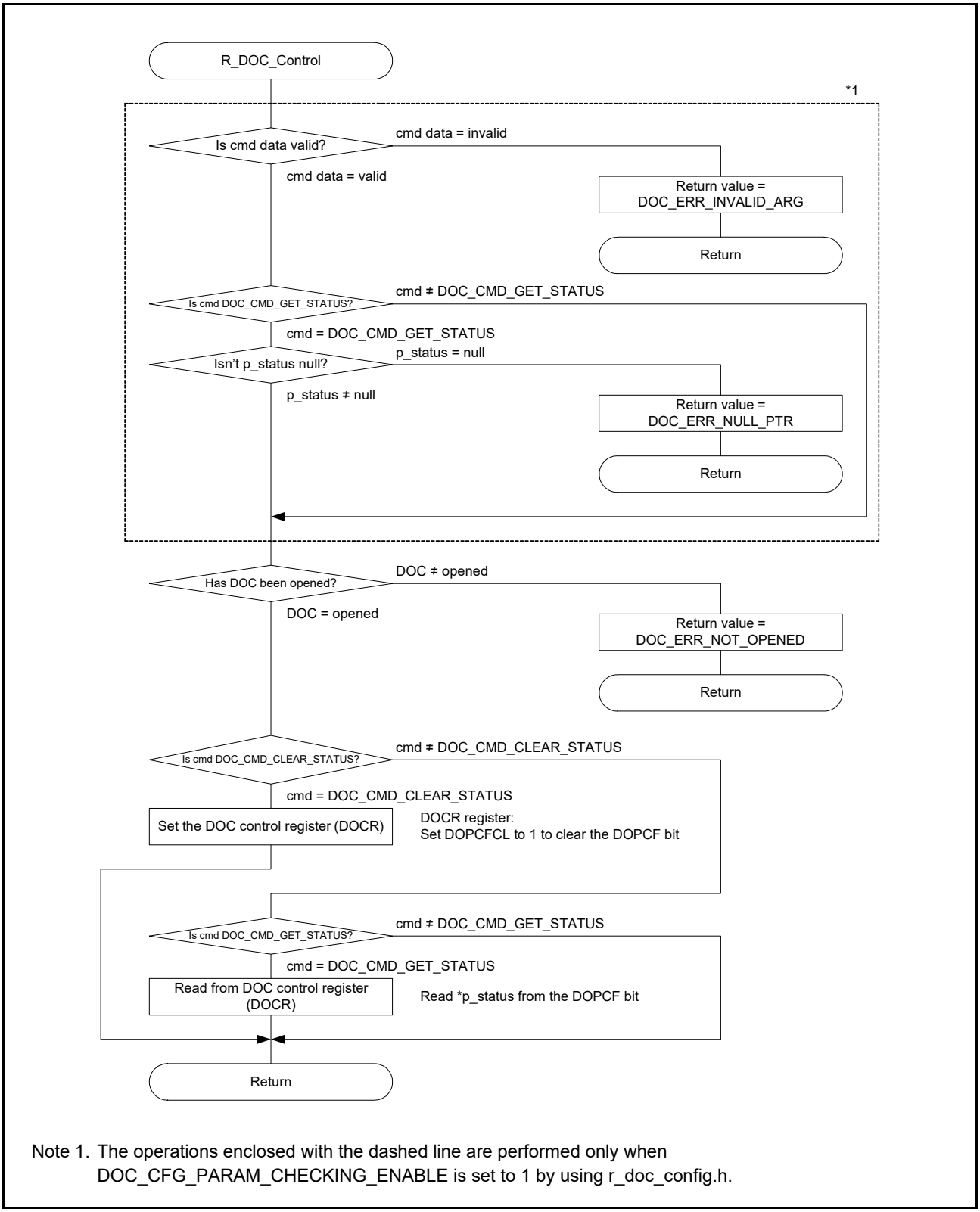


Note 1. The operations enclosed with the dashed line are performed only when DOC_CFG_PARAM_CHECKING_ENABLE is set to 1 by using r_doc_config.h

Figure 6.9 DOC Open Function

6.9.7 DOC Control Function

Figure 6.10 shows a flowchart of the DOC control function.



Note 1. The operations enclosed with the dashed line are performed only when DOC_CFG_PARAM_CHECKING_ENABLE is set to 1 by using r_doc_config.h.

Figure 6.10 DOC Control Function

6.9.8 IRQ20 Interrupt (ECM Error Detection Maskable Interrupt)

Figure 6.11 shows a flowchart of processing of the IRQ20 interrupt (ECM error detection maskable interrupt).

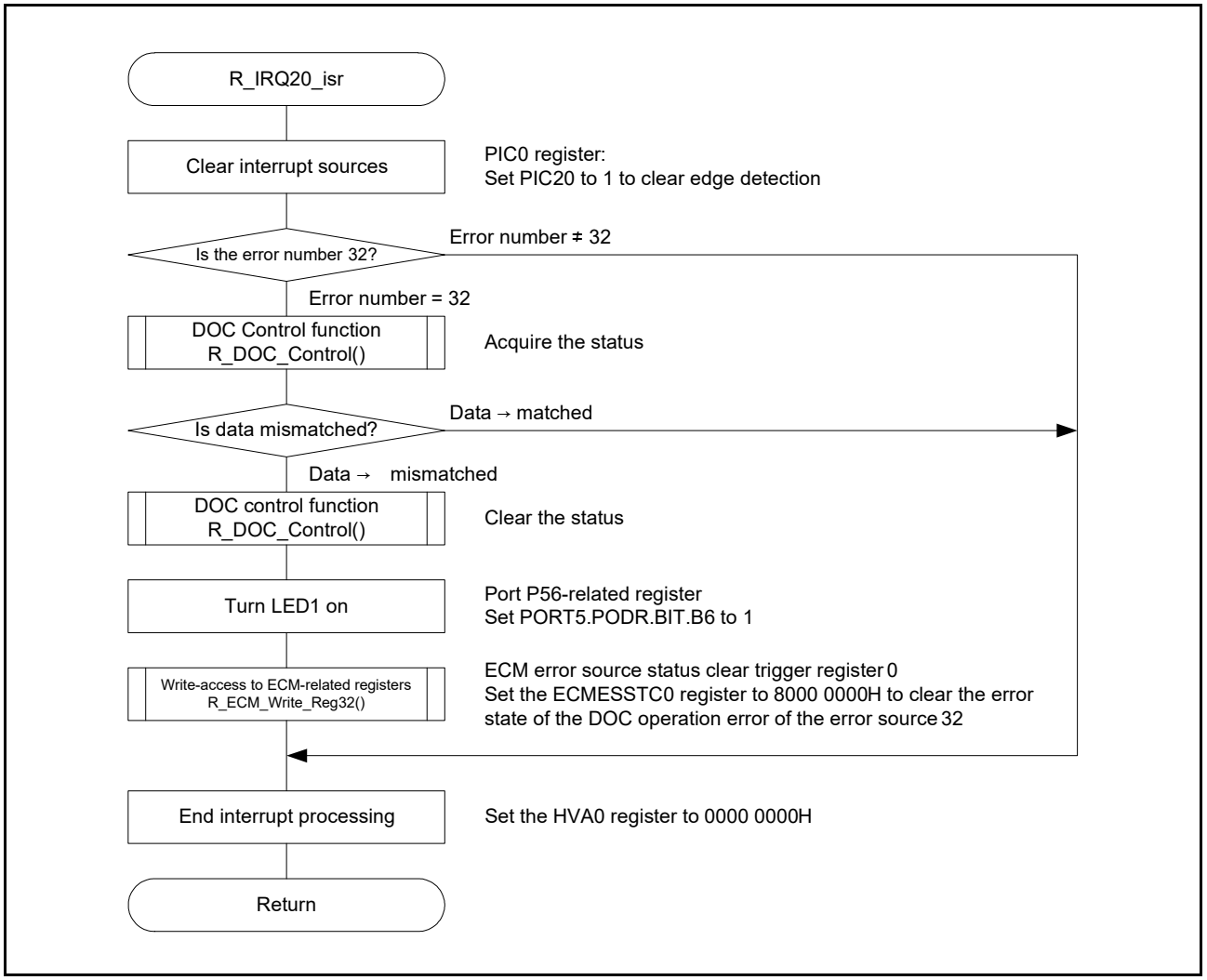


Figure 6.11 IRQ20 Interrupt (ECM Error Detection Maskable Interrupt)

6.9.9 IRQ251 Interrupt (DMA Transfer Software Startup Interrupt)

Figure 6.12 shows a flowchart of processing of the IRQ251 interrupt (DMA transfer software startup).

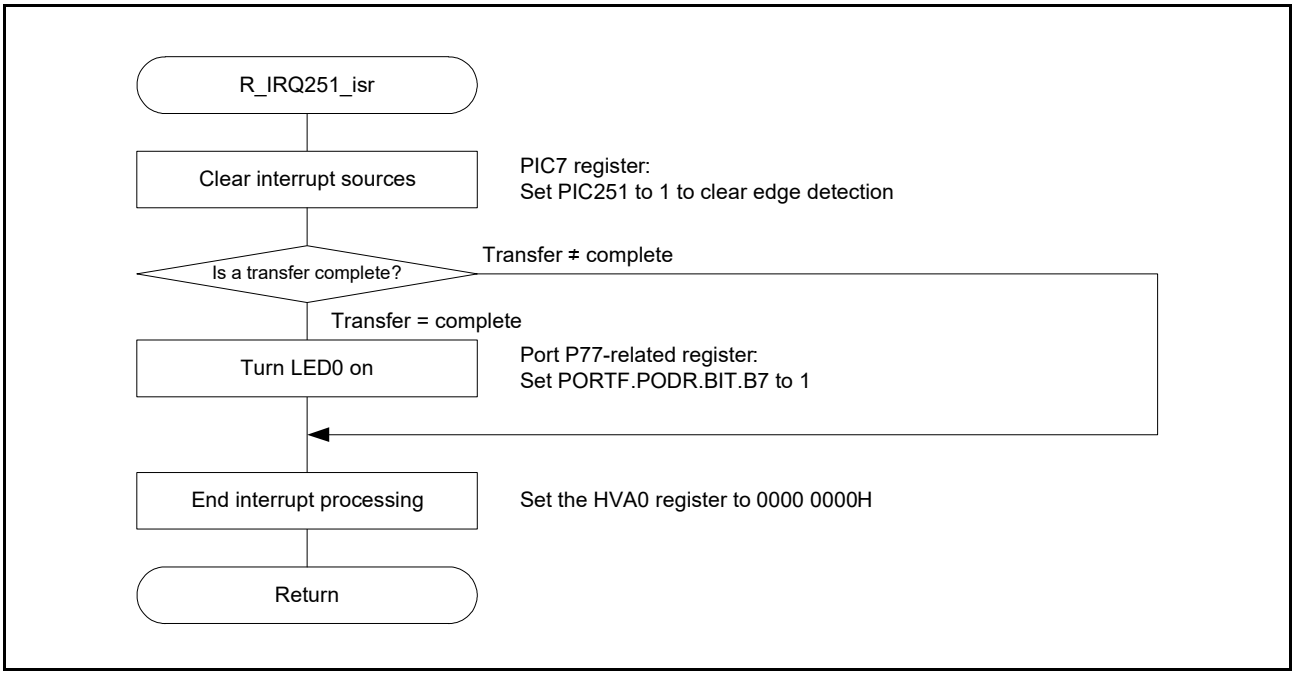


Figure 6.12 IRQ251 Interrupt (DMA Transfer Software Startup)

6.9.10 IRQ293 Interrupt (DMA Transfer Error Interrupt)

Figure 6.13 shows a flowchart of processing of the IRQ293 interrupt (DMA transfer error interrupt).

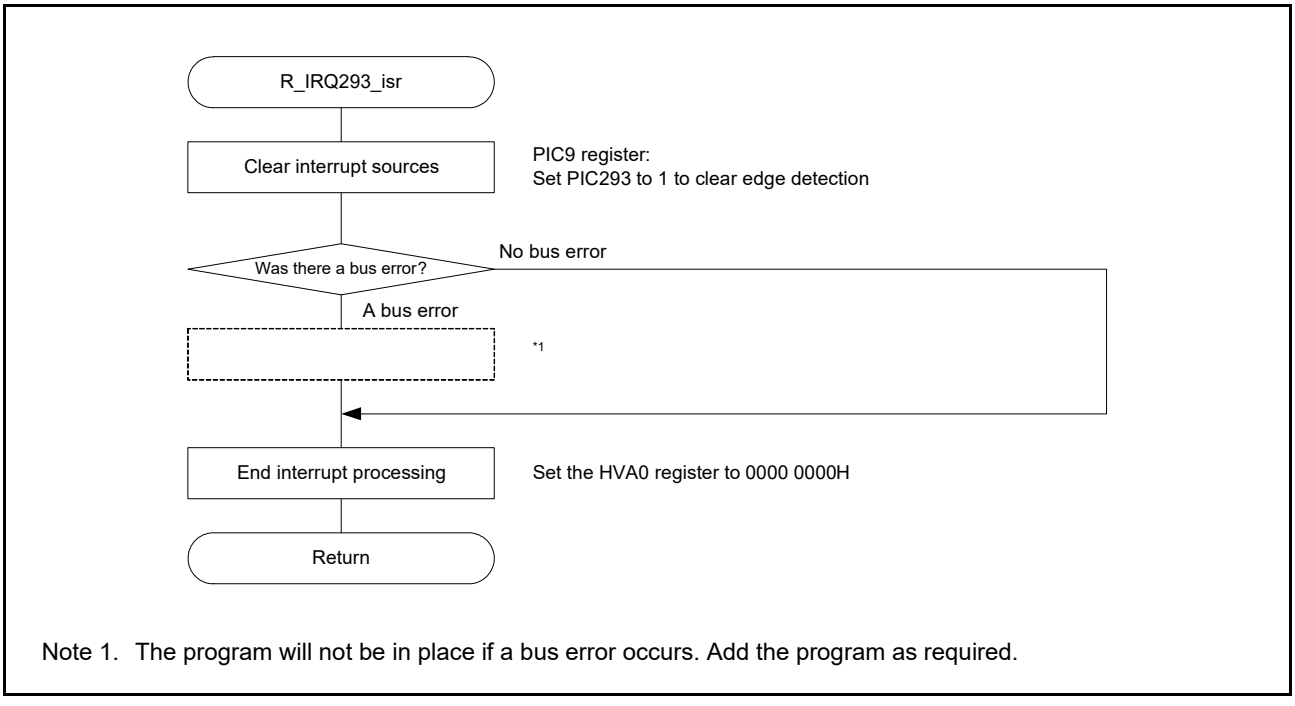


Figure 6.13 IRQ293 Interrupt (DMA Transfer Error Interrupt)

7. Sample Program

Download the sample program from the Renesas Electronics website.

8. Reference Documents

User's manual: hardware:
RZ/T1 Group User's Manual: Hardware
(Download the latest version of the manual from the Renesas Electronics website.)

RZ/T1 Evaluation Board RTK7910022C00000BR User's Manual
(Download the latest version of the manual from the Renesas Electronics website.)

Technical Update / Technical News
(Download the latest version of the update or news from the Renesas Electronics website.)

User's manual: Development Environment
For IAR integrated development environment (IAR Embedded Workbench® for Arm), visit the IAR Systems website.
(Download the latest version from the IAR Systems website.)

Website and Support

Renesas Electronics website

http://www.renesas.com/

Inquiries

http://www.renesas.com/inquiry

Revision History	Application Note: Data Operation Circuit (DOC)

Rev.	Date	Description	
		Page	Summary
0.10	Mar. 18, 2015	—	First Edition issued
1.00	Apr. 10, 2015	—	Only the revision number was changed to be posted on a website.
1.10	Aug. 18, 2015	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, partially amended and added
		6. Software	
		10	6.2.4 Required Memory Size: Description and reference added
		10	Table 6.2: Table title was partially amended
		11	Table 6.3 added
		11	Table 6.4 added
1.20	Dec. 04, 2015	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, information partially amended
1.30	Apr. 05, 2017	2. Operating Environment	
		5	Table 2.1 Operating Environment: Integrated Development Environment, modified
		6. Software	
		—	6.2.4 Required Memory Size, deleted
1.40	Jun. 07, 2018	2. Operating Environment	
		5	Table 2.1 Operating Environment: The description on the integrated development environment, modified
		5. Hardware	
		8	Figure 5.1 Hardware configuration example: The name of module, modified
		8. Related Documents	
		27	The name of IAR Embedded Workbench, modified

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
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5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

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