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RENESAS

Application Note

V850ES/Jx3-L

32-bit Single-Chip Microcontrollers

Power Supply Current

This Application Note describes the functions that relate to the power supply current of the V850ES/Jx3-L. Readers should use the information in this document to understand the features of this product's power supply current and the functions used to reduce it, and apply this knowledge to reduce the power supply current of their application system.

Target devices

μPD70F3735
μPD70F3736
μPD70F3737
μPD70F3738

CONTENTS

Document No. U19461EJ1V0AN00 (1st edition)
Date Published November 2008

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

INTRODUCTION

Target Readers

This Application Note is intended for users who understand the functions of the V850ES/Jx3-L and who will use this product to design application systems.

Purpose

The purpose of this Application Note is to help users understand how to reduce the power supply current of the V850ES/Jx3-L.

Organization

This document consists of the following main sections.

- Overview
- Features of V850ES/Jx3-L power supply current
- Functions used to reduce power supply current

How to Read This Document

It is assumed that the reader of this document has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To obtain an overview of the functions of the V850ES/Jx3-L:

→ Read this manual in the order of the **CONTENTS**.

To understand the features of the power supply current in the V850ES/Jx3-L:

→ Refer to **CHAPTER 2 FEATURES OF V850ES/Jx3-L POWER SUPPLY CURRENT**.

To understand the functions used to reduce the power supply current:

→ Refer to **CHAPTER 3 FUNCTIONS USED TO REDUCE POWER SUPPLY CURRENT**.

To learn more about the V850ES/Jx3-L's hardware functions:

→ See the hardware user's manual of each V850ES/Jx3-L product.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representation:	Binary.....xxxx or xxxxB
	Decimal xxxx
	Hexadecimal .....xxxxH

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/Jx3-L

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/JG3-L Hardware User's Manual	U18953E
V850ES/JF3-L Hardware User's Manual	U18952E

CONTENTS

CHAPTER 1 OVERVIEW

1.1 Introduction

This Application Note describes the functions that relate to the power supply current of the V850ES/Jx3-L. The features of the power supply current are explained in chapter 2, and the functions used to reduce the power supply current are described in chapter 3.

It is hoped that by understanding the features of the V850ES/Jx3-L's power supply current and the functions used to reduce it, the reader will be able to apply this knowledge to reduce the power supply current of their own application systems.

1.2 Power Supply Current Data

The graphs and values used to express the power supply current in this document are actual values measured using specific samples. These values are not guaranteed. Also, be aware that power supply current characteristics may differ due to product variations. For guaranteed power supply current values, refer to the electrical specifications section of the hardware user's manual of each V850ES/Jx3-L product.

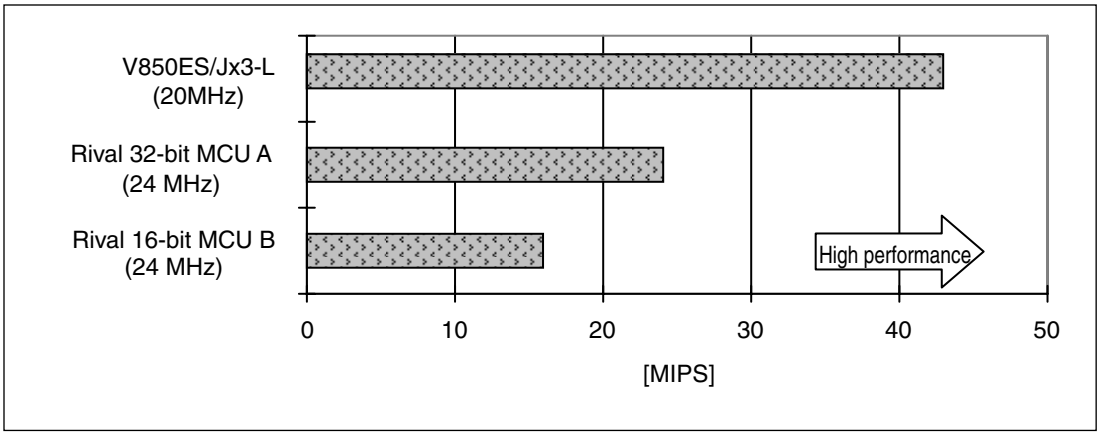
CHAPTER 2 FEATURES OF V850ES/Jx3-L POWER SUPPLY CURRENT

This chapter explains the features of the power supply current in the V850ES/Jx3-L.

2.1 Processing Performance and Power Consumption

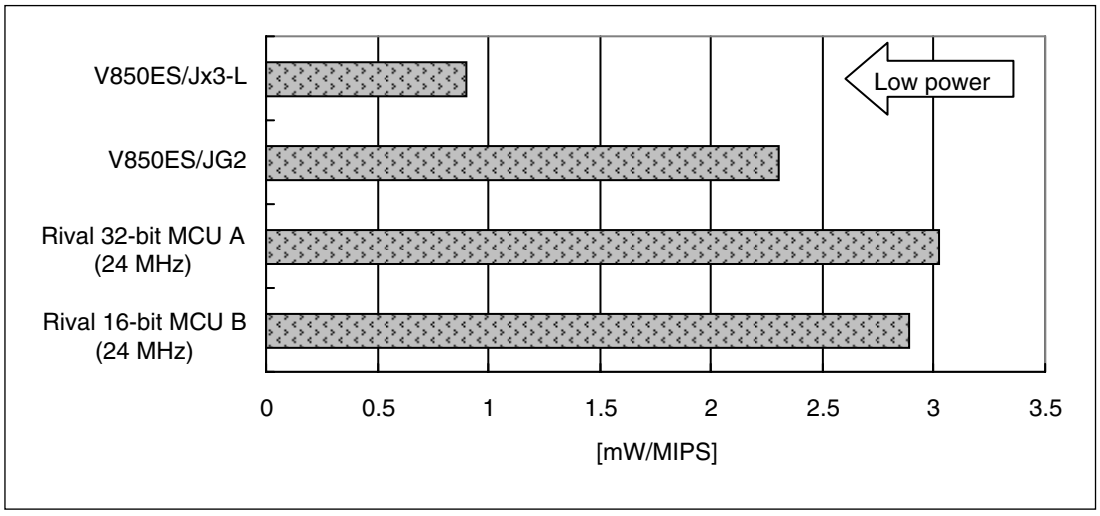
The V850ES/Jx3-L has the processing performance of a 32-bit microcontroller, but with the power efficiency of a 16-bit microcontroller. The V850ES/Jx3-L can realize a performance of 43 MIPS at 20 MHz operation in the Dhrystone 1.1 benchmark program. This is almost twice the level of rival 32-bit microcontrollers (see **Figure 2-1**).

Figure 2-1. Processing Performance [Dhrystone 1.1]



In terms of power consumption, the V850ES/Jx3-L consumes less than half the power of the previous product (V850ES/JG2) per MIPS (see **Figure 2-2**).

Figure 2-2. Power Consumption per MIPS [Dhrystone 1.1]



Remarks 1. Power supply voltage: 3.3 V

2. Power supply current: Catalog value

3. MIPS: Million Instructions Per Second

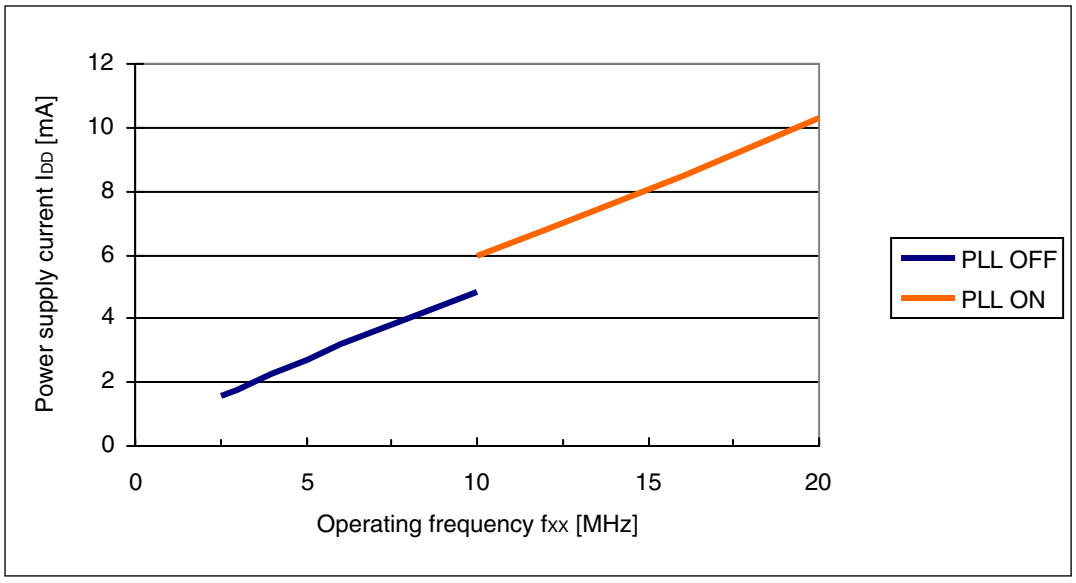
2.2 Operating Frequency and Power Supply Current

When comparing the power of microcontrollers, it is insufficient to simply compare operating frequency vs. current value. This is because the operating frequency used by the microcontroller is determined based on the processing execution time. For example, in the case of a certain microcontroller that must execute processing at 20 MHz in order to satisfy the allowable execution time, it may be possible to satisfy the allowable execution time with a microcontroller operating at 10 MHz if that microcontroller has double the processing performance of the original microcontroller.

The general rule in microcontrollers is that the power supply current increases in proportion to the operating frequency. Therefore, if the operating frequency can be lowered, and the same operations can be executed using a low frequency, the power consumption will also be reduced proportionately. For example, the V850ES/Jx3-L has a processing performance of 11 MIPS (Dhrystone 1.1) even when operating at 5 MHz. This is the same performance as a 16-bit microcontroller operating at 20 MHz. The power supply current in this case is about 2.8 mA.

Figure 2-3 shows the relationship between the operating frequency and the power supply current of the V850ES/Jx3-L.

Figure 2-3. Relationship Between Operating Frequency and Power Supply Current



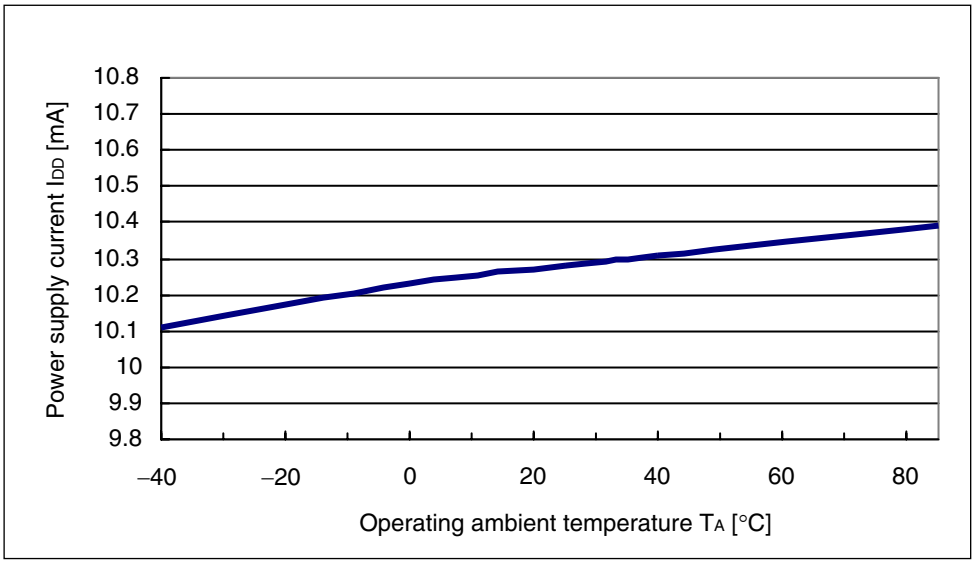
Remark The power supply current is the value under conditions of V_{DD} = EV_{DD} = 3.3 V, T_A = 25°C, with all peripheral functions stopped and when all instructions are executed repeatedly.

2.3 Operating Ambient Temperature and Power Supply Current

The typical (TYP) power supply current value in the electrical specifications is the value when the operating ambient temperature (T_A) is 25°C. The power supply current will change in accordance with the operating ambient temperature (T_A). In modes such as STOP mode especially, the power supply current increases in greater proportion as the operating ambient temperature reaches the high-temperature zone. One effective way to reduce power supply current, therefore, is to restrict the temperature range in which the application system is used.

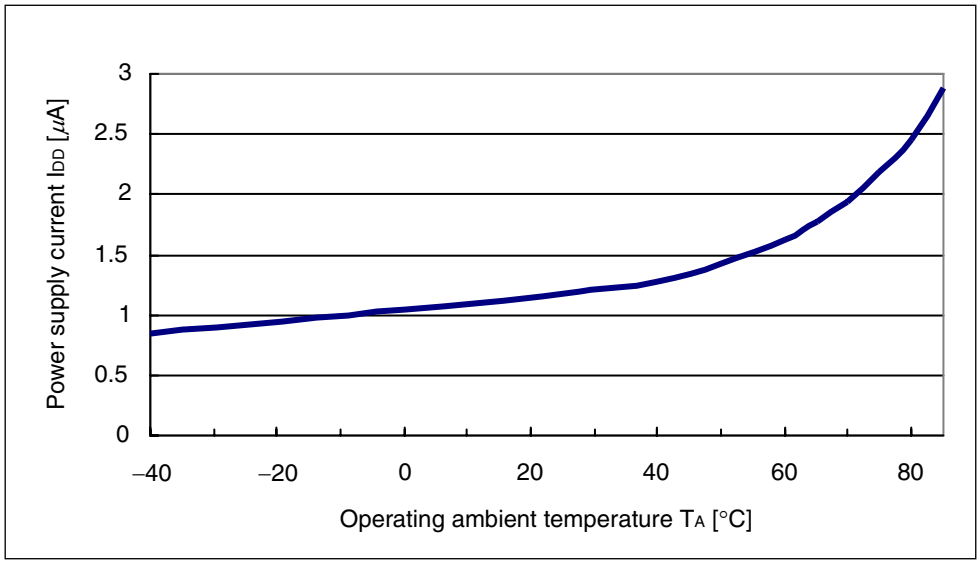
Figures 2-4 and 2-5 show the relationship between the operating ambient temperature and power supply current in normal operation mode and low-voltage STOP mode, respectively.

Figure 2-4. Relationship Between Operating Ambient Temperature and Power Supply Current (Normal Operation Mode)



Remark The power supply current is the value under conditions of V_{DD} = EV_{DD} = 3.3 V, with all peripheral functions stopped and when all instructions are executed repeatedly.

Figure 2-5. Relationship Between Operating Ambient Temperature and Power Supply Current (Low-Voltage STOP Mode)



Remark The power supply current is the value under conditions of V_{DD} = EV_{DD} = 3.3 V, with all peripheral functions stopped, and when the subclock is not being used.

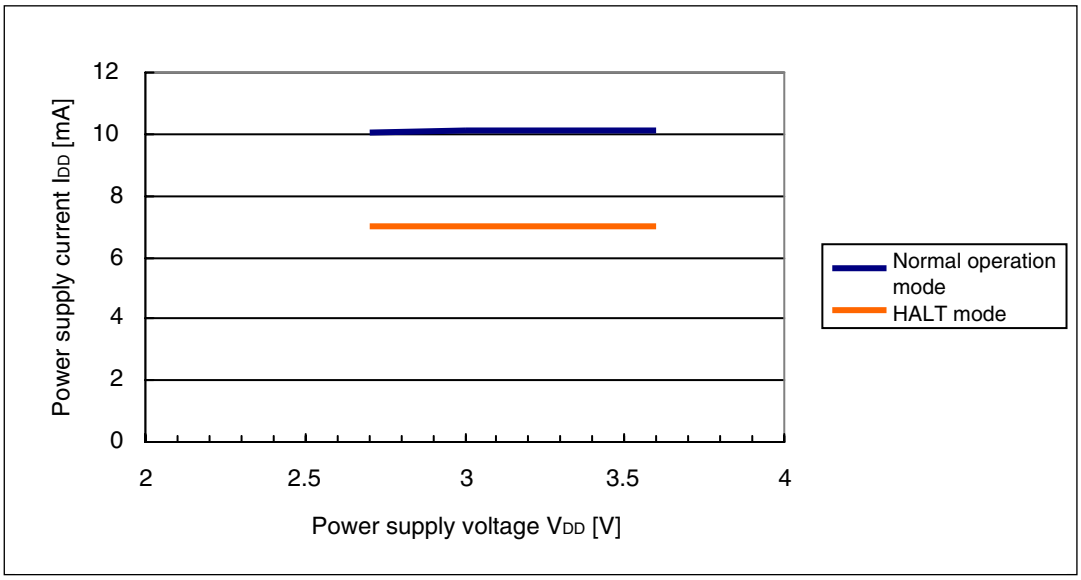
2.4 Power Supply Voltage and Power Supply Current

The V850ES/Jx3-L has an on-chip regulator that operates the internal circuits on a constant voltage. This regulator supplies a stepped down voltage (about 2.5 V; stepped down from the V_{DD} power supply voltage) to the oscillator block and internal logic circuits (except for the A/D converter, D/A converter, and output buffers).

Because the regulator is incorporated on the chip, its current consumption has almost no effect on the V_{DD} power supply voltage.

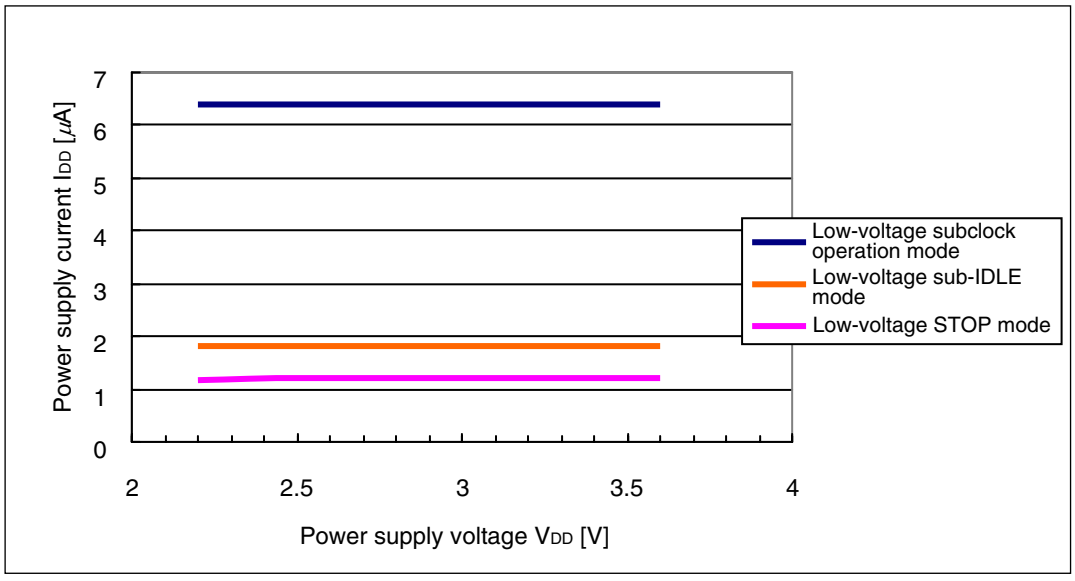
Figures 2-6 and 2-7 show the relationship between the power supply voltage and power supply current at 20 MHz operation and in low-voltage mode, respectively.

Figure 2-6. Relationship Between Power Supply Voltage and Power Supply Current at 20 MHz Operation



Remark The power supply current is the value under conditions of T_A = 25°C, with all peripheral functions stopped, and when all instructions are executed repeatedly in normal operation mode.

Figure 2-7. Relationship Between Power Supply Voltage and Power Supply Current in Low-Voltage Mode



Remark The power supply current is the value under conditions of T_A = 25°C, with all peripheral functions stopped, and when a loop is executed by the JR instruction in low-voltage subclock operation mode. In low-voltage STOP mode, this is the value when the subclock is not being used.

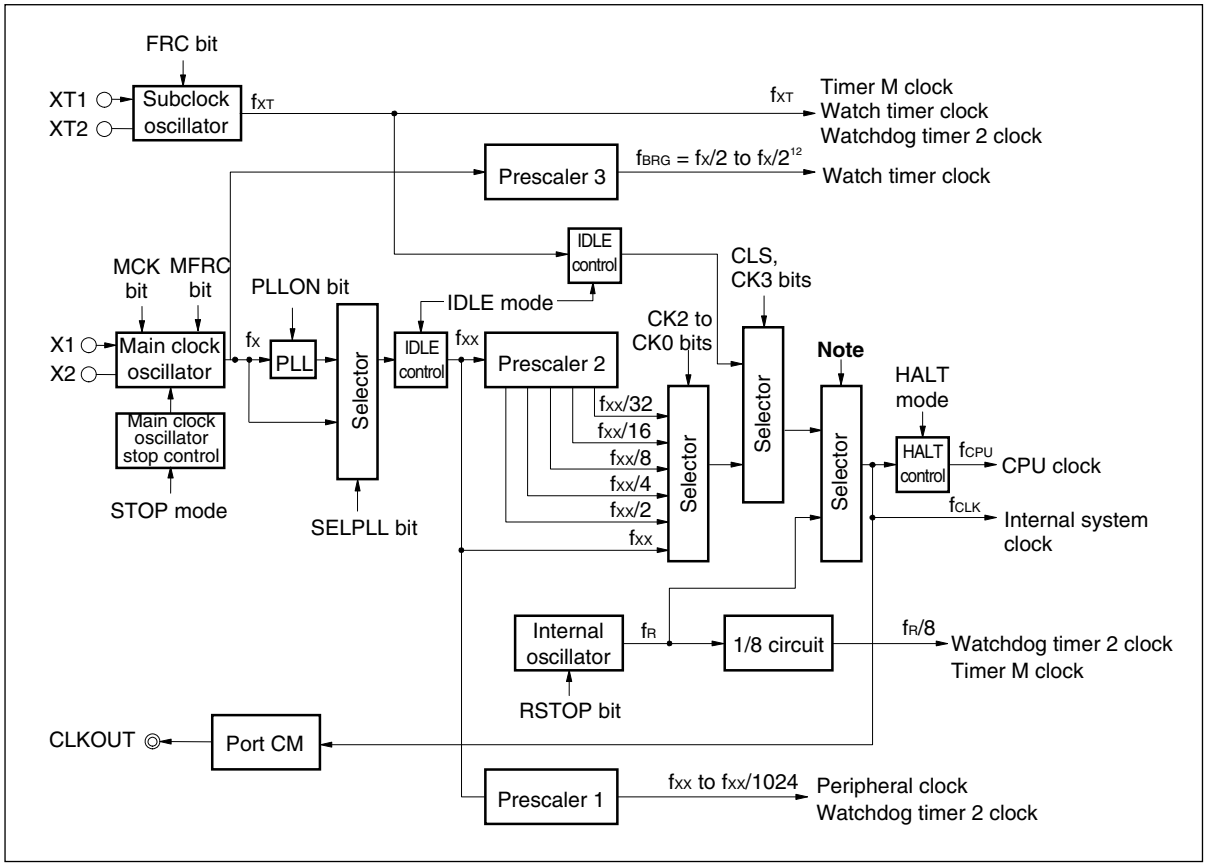
CHAPTER 3 FUNCTIONS USED TO REDUCE POWER SUPPLY CURRENT

This chapter describes the functions used in the V850ES/Jx3-L to reduce power supply current.

3.1 Clock Control

The power supply current can be reduced by selecting the ideal clock and stopping unnecessary clocks and functions. The clock generator used in the V850ES/Jx3-L is shown below.

Figure 3-1. Clock Generator



Note If watchdog timer 2 overflows during the oscillation stabilization period, the internal oscillation clock is selected.

Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency
f_{CLK}: Internal system clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_R: Internal oscillation clock frequency

3.1.1 CPU clock selection

A clock with a selectable divided main clock frequency (f_{XX}) can be used as the CPU clock (f_{CPU}) without changing the frequency of the on-chip peripheral function clock. Selecting a divided clock is effective in reducing the power supply current.

(1) Function details

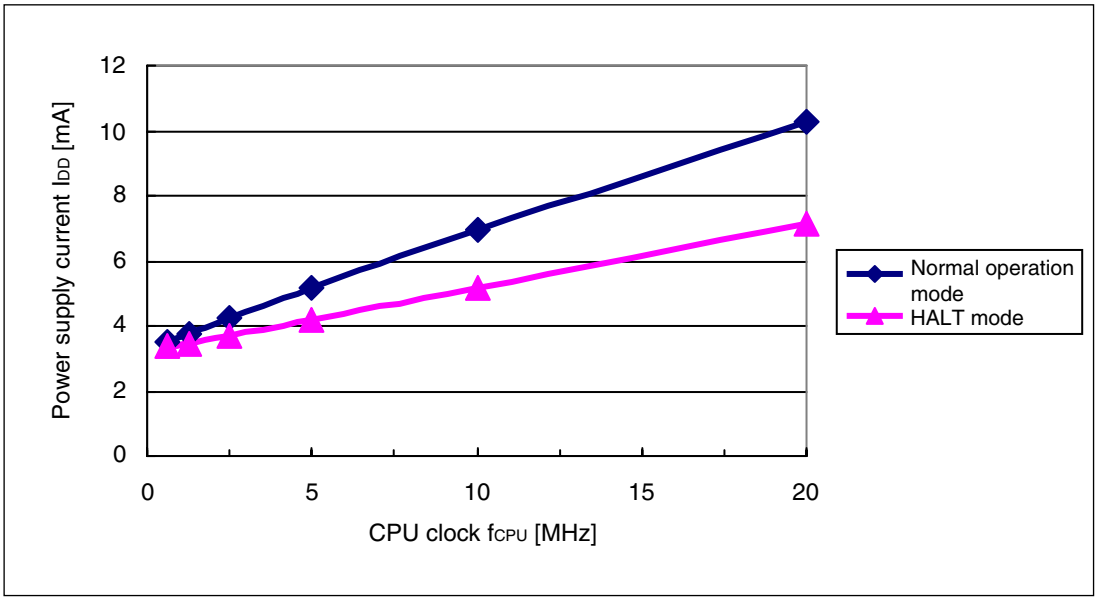
A clock with a divided main clock frequency (f_{XX}) can be used as the CPU clock (f_{CPU}) and internal system clock (f_{CLK}) by setting the CK3 to CK0 bits of the PCC register. The clock at this time has no effect on the peripheral clock supplied via prescaler 1, enabling the power supply current to be reduced without re-setting the on-chip peripheral functions.

This can be an effective way to reduce power supply current in cases such as the following:

- When a high-speed clock is required for the on-chip peripheral functions, but the CPU processing performance can be lowered.
- When a high CPU processing performance is required only for a specific period; otherwise low-speed processing is OK.
- As a substitute for HALT mode (when it is OK to take some time to recover from HALT)

Figure 3-2 shows the relationship between the frequency and power supply current when the CPU clock (f_{CPU}) selection is changed by setting the CK3 to CK0 bits of the PCC register when f_{XX} is 20 MHz.

Figure 3-2. Relationship Between CPU Clock and Power Supply Current



Remark The power supply current is the value under conditions of $V_{DD} = EV_{DD} = 3.3$ V and $T_A = 25°C$, with all peripheral functions stopped and when all instructions are executed repeatedly in normal operation mode.

(2) Processor clock control register (PCC)

This register is used to select the CPU clock (f_{CPU}) and internal system clock (f_{CLK}). The power supply current can be reduced by selecting a low-speed CPU clock.

For details of the PCC register, see the user's manual of the V850ES/Jx3-L product being used.

The PCC register is a special register. Data can be written to this register only in a combination of specific sequences.

Reset sets this register to 03H.

	7	6	5	4	3	2	1	0
PCC	FRC	MCK	MFRC	CLS	CK3	CK2	CK1	CK0

CK3	CK2	CK1	CK0	Clock Selection (f_{CPU}/f_{CLK})
0	0	0	0	f_{XX}
0	0	0	1	$f_{XX}/2$
0	0	1	0	$f_{XX}/4$
0	0	1	1	$f_{XX}/8$ (initial value)
0	1	0	0	$f_{XX}/16$
0	1	0	1	$f_{XX}/32$
0	1	1	X	Setting prohibited
1	0	0	0	Subclock

Remark The CPU clock (f_{CPU}) is used as the CPU operating clock.

The internal system clock (f_{CLK}) is used as the operating clock of the interrupt controller, internal ROM, internal RAM, DMA function, and bus control function.

3.1.2 PLL function

Two clock modes can be selected in the V850ES/Jx3-L: clock-through mode, in which the main clock oscillation frequency (fx) is used unchanged as the main clock frequency (fxx); and PLL mode, in which the PLL function is used to multiply the main clock oscillation frequency (fx) by 4. The power supply current can be reduced by stopping the PLL and operating the system in clock-through mode. The main clock oscillation frequency (fx) and main clock frequency (fxx) that can be used are as follows.

Clock Mode	Main Clock Oscillation Frequency (fx)	Main Clock Frequency (fxx)
Clock-through mode	2.5 to 10 MHz	2.5 to 10 MHz
PLL mode	2.5 to 5 MHz	10 to 20 MHz

(1) Function details

The PLLCTL register can be used to select whether the PLL operates or is stopped, and whether the clock mode is clock-through mode or PLL mode. A PLL lockup time (set by the PLLS register) is required when shifting from the PLL stopped state to the PLL operating state.

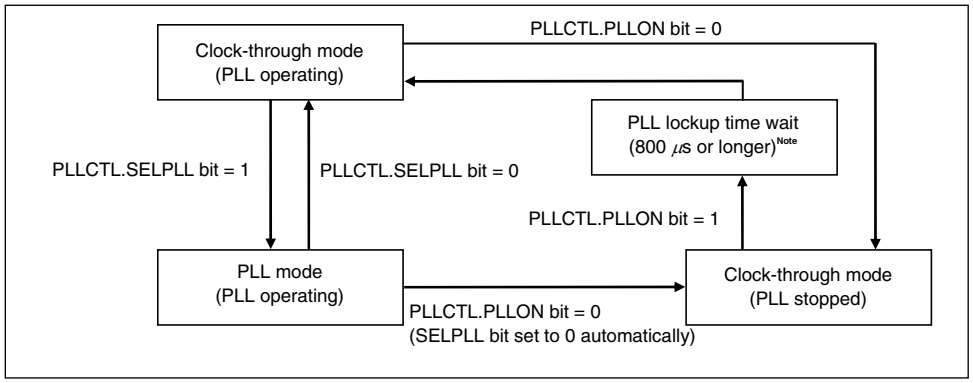
After reset is released, the PLL is in the operating state and the clock mode is clock-though mode. To operate the system in the PLL mode, therefore, the PLL mode must be set (PLLCTL.SELPLL bit = 1). When not using the PLL, the power supply current can be reduced by stopping the PLL (PLLCTL.PLLON bit = 0).

Operating in clock-through mode can be an effective way to reduce power supply current in cases such as the following:

- When the system, including the peripheral functions, can always operate at 10 MHz or lower.
- When a high CPU processing performance is required only for a specific period; otherwise low-speed processing is OK. Also, if the peripheral functions can be stopped/re-set when the clock mode switches between PLL mode and clock-through mode.

There are two ways to switch from PLL mode to clock-through mode: switching to clock-through mode (PLLCTL.SELPLL bit = 0) with the PLL operating (PLLCTL.PLLON bit = 1), and switching with it stopped (PLLCTL.PLLON = 0). Once the PLL is stopped, a PLL lockup time (800 μs or longer) is required when shifting to the PLL operating state. However, by leaving the PLL stopped when it is not being used, the power supply current can be reduced by about 1 mA. Figure 3-3 shows a diagram of the status transitions between the clock-though mode and the PLL mode.

Figure 3-3. Diagram of Status Transitions Between Clock-Through Mode and PLL Mode



Note Set the PLLS register in accordance with the main clock oscillation frequency so that the PLL lockup time is 800 μs or longer.

(2) PLL control register (PLLCTL)

This register is used to select the PLL operation and PLL mode. The power supply current can be reduced by stopping the PLL and operating in clock-through mode.

For details of the PLLCTL register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 01H.

	7	6	5	4	3	2	1	0
PLLCTL	0	0	0	0	0	0	SELPLL	PLLON

SELPLL	Operating clock selection
0	Clock-through mode (initial value)
1	PLL mode

PLLON	PLL operation stop
0	PLL stopped
1	PLL operating (PLL lockup time required)

(3) PLL lockup time specification register (PLLS)

This register is used to select the PLL lockup time required after changing the PLLCTL.PLLON bit from 0 to 1.

For details of the PLLS register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 03H.

	7	6	5	4	3	2	1	0
PLLS	0	0	0	0	0	0	PLLS1	PLLS0

PLLS1	PLLS0	PLL lockup time selection
0	0	$2^{10}/f_X$
0	1	$2^{11}/f_X$
0	0	$2^{12}/f_X$
0	1	$2^{13}/f_X$ (initial value)

Remarks 1. Set this register so that the lockup time is 800 μs or longer.

2. Do not change the setting of the PLLS register during the lockup period.

(4) Lock register (LOCKR)

This register indicates the stabilization state of the PLL frequency. When setting the system to PLL mode (PLLCTL.SELPLL bit = 1), the LOCKR.LOCK bit must first be set to 0.

For details of the LOCKR register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 01H. After the oscillation stabilization time has elapsed following reset release, LOCKR is set to 00H.

	7	6	5	4	3	2	1	0
LOCKR	0	0	0	0	0	0	0	LOCK

LOCK	PLL lock state indication
0	Locked (initial value)
1	Unlocked

[Set conditions]

- Upon system reset (set to 01H by reset and to 00H after oscillation stabilization time elapses following reset release)
- In IDLE2 or STOP mode
- Upon setting of PLL stop (setting of PLLCTL.PLLON bit to 0)
- When CPU operates on subclock and main clock is stopped (when PCC.CK3 bit is set to 1 and then PCC.MCK bit is set to 1)

[Clear conditions]

- When oscillation stabilization time (set by option byte) elapses following reset release
- When oscillation stabilization time (set by OSTS register) elapses following release of IDLE2 or STOP mode (or when IDLE2 or STOP mode is set if the PLL is operating)
- After PLL lockup time (set by PLLS) elapses when PLLCTL.PLLON bit is changed from 0 to 1

3.1.3 Internal oscillator

In the V850ES/Jx3-L, the clock of the internal oscillator can be selected as the clock for watchdog timer 2, timer M and the clock monitor.

When not using these functions, or when not using the internal oscillator's clock for watchdog timer 2 and timer M, the power consumption can be reduced by stopping the internal oscillator.

(1) Function details

The internal oscillator starts operating after reset release. At this time, watchdog timer 2 starts operating on the internal oscillation clock (f_R). When not using watchdog timer 2, stop both the internal oscillator and watchdog timer 2. Also, when operating watchdog timer 2 on another clock (main clock/subclock), stop the internal oscillator after switching the clock. By stopping the internal oscillator, the power supply current can be reduced by about 2 to 5 μA.

The power supply current can be reduced by stopping the internal oscillator in cases such as the following:

- When not using watchdog timer 2 and the clock monitor.
- When operating watchdog timer 2 on the main clock or subclock and at the same time not using the clock monitor.

(2) Internal oscillation mode register (RCM)

This register is used to oscillate and stop the internal oscillator.

For details of the RCM register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 00H.

	7	6	5	4	3	2	1	0
RCM	0	0	0	0	0	0	0	RSTOP

RSTOP	Oscillation/stop of internal oscillator
0	Oscillate internal oscillator
1	Stop internal oscillator

3.1.4 Function to supply/stop clock to peripheral functions

In the V850ES/Jx3-L, the peripheral functions can be operated and stopped by software. The power supply current can be reduced by stopping the operation of peripheral functions not being used.

(1) Function details

The following peripheral functions of the V850ES/Jx3-L can be operated and stopped by using software. After reset is released, the peripheral functions are in the stopped state.

- Timer P (TMP)
- Timer Q (TMQ)
- Timer M (TMM)
- Watch timer
- Real-time output function (RTO)
- A/D converter (A/D)
- D/A converter (D/A)
- Asynchronous serial interface A (UARTA)
- 3-wire variable-length serial I/O (CSIB)
- I^2C bus (I^2C)
- DMA controller (DMA)
- Clock monitor (CLM)
- Low-voltage detector (LVI)

(2) Registers enabling/stopping peripheral function operation

The operation of the peripheral functions can be enabled and stopped by using the following registers and bits.

Peripheral Function	Operation Enable/Stop Control Register	Operation Enable/Stop Control Bit	Stop Setting
TMP	TPnCTL0	TPnCE	0
TMQ	TQ0CTL0	TQ0CE	0
TMM	TM0CTL0	TM0CE	0
Watch timer	WTM	WTM0	0
RTO	RTPC0	RTPOE0	0
A/D	ADA0M0	ADA0CE	0
D/A	DA0M	DA0CEn	0
UARTA	UAnCTL0	UAnPWR	0
CSIB	CBnCTL0	CBnPWR	0
I^2C	IICCn	IICEn	0
DMA	DCHCn	Enn	0
CLM	CLM	CLME	0
LVI	LVIM	LVION	0

3.2 Standby Function

The V850ES/Jx3-L has three operating modes and seven standby modes. The power consumption can be effectively reduced by using the modes in combination and selecting the appropriate mode for the application.

3.2.1 Types of operating and standby modes

The types of operating and standby modes available are shown below.

Mode	Function
Normal operation mode	Mode in which the CPU operates on the main clock.
HALT mode	Mode in which only the CPU operating clock is stopped.
IDLE1 mode	Mode in which the operations of all internal circuits except the oscillator, PLL[Note] and flash memory are stopped.
IDLE2 mode	Mode in which the operations of all internal circuits except the oscillator are stopped. When returning to normal operation mode from IDLE2 mode, regulator, flash memory and PLL setup time (set by the OSTS register) is required.
Subclock operation mode	Mode in which the subclock is used as the internal system clock. If the main clock is stopped, oscillation stabilization time set by the program must be secured when returning to normal operation mode.
Low-voltage subclock operation mode	Mode in which the subclock is used as the internal system clock, and the regulator voltage is lowered. The main clock is stopped.
Sub-IDLE mode	Mode in which the operations of all internal circuits except the oscillator, PLL[Note] and flash memory are stopped in subclock operation mode.
Low-voltage sub-IDLE mode	Mode in which the operations of all internal circuits except the flash memory are stopped in low-voltage subclock operation mode.
STOP mode	Mode in which the operations of all internal circuits except the subclock oscillator are stopped. When returning to normal operation mode, oscillation stabilization time (set by the OSTS register) is required.
Low-voltage STOP mode	Mode in which the operations of all internal circuits except the subclock oscillator are stopped, and the regulator voltage is lowered. When returning to normal operation mode, oscillation stabilization time (set by the OSTS register) is required.

Note In IDLE1 mode and sub-IDLE mode, the PLL retains the state it was in immediately before the mode was shifted. If PLL operations are not required, the PLL should be stopped in order to save power. Note that shifting to IDLE2 mode will automatically stop the PLL.

Figure 3-4 shows a mode status transition diagram and Figure 3-5 shows the power supply current in each mode.

Figure 3-4. Status Transition Diagram

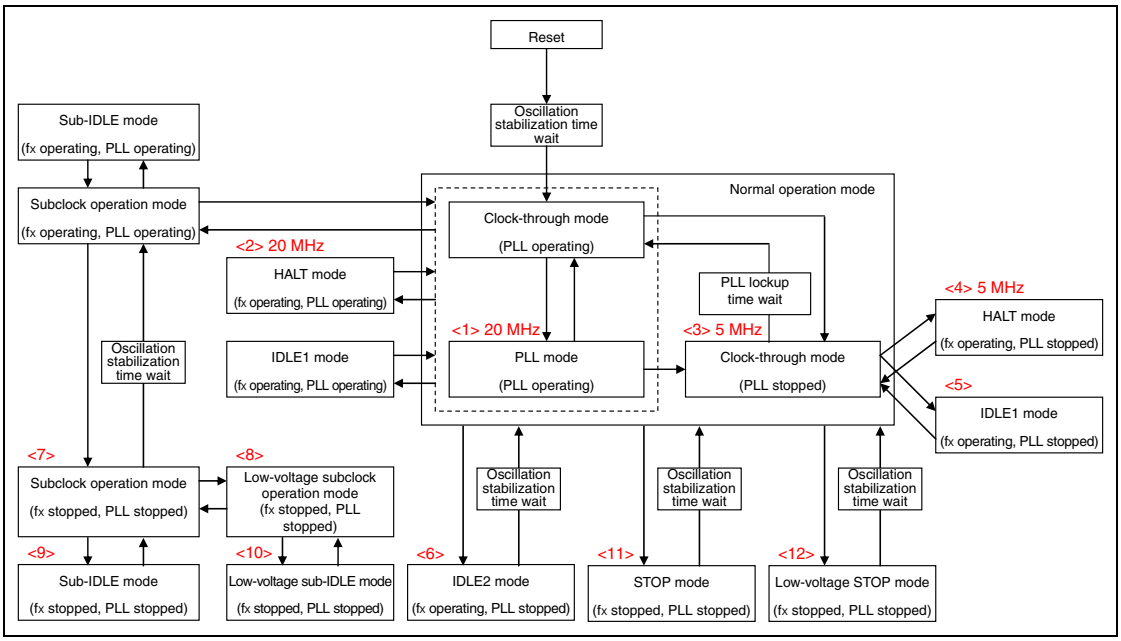
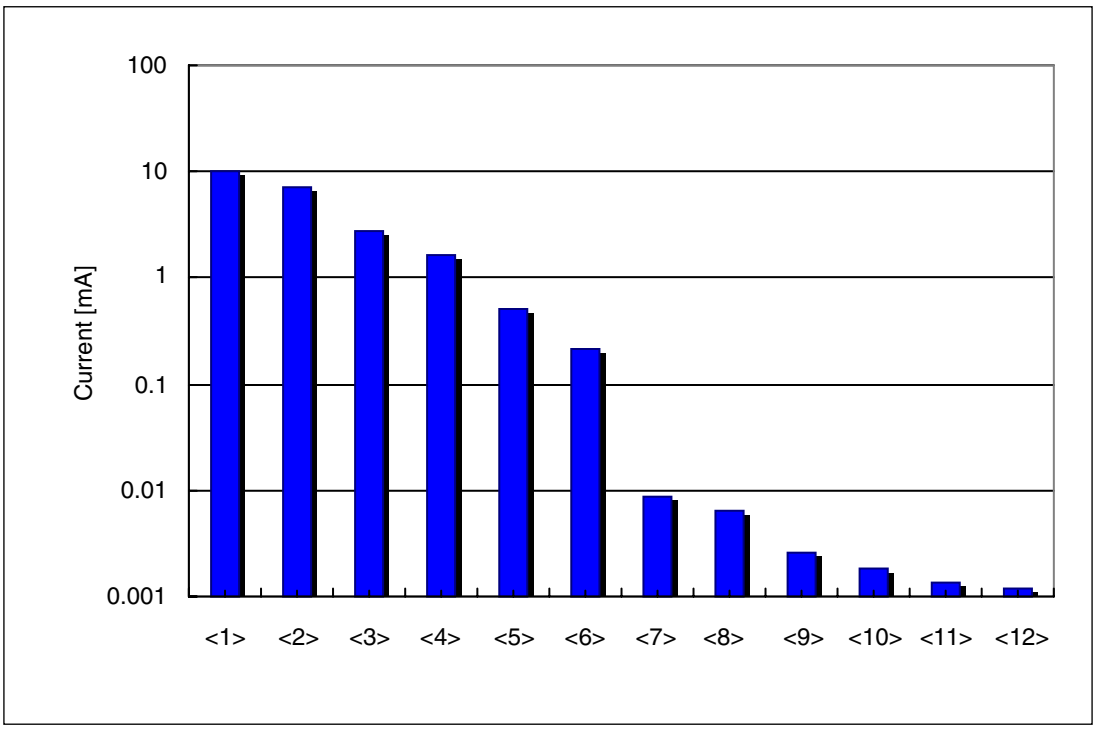


Figure 3-5. Power Supply Current in Each Mode



Remark See **Figure 3-4 Status Transition Diagram** for the definitions of modes <1> to <12> above.

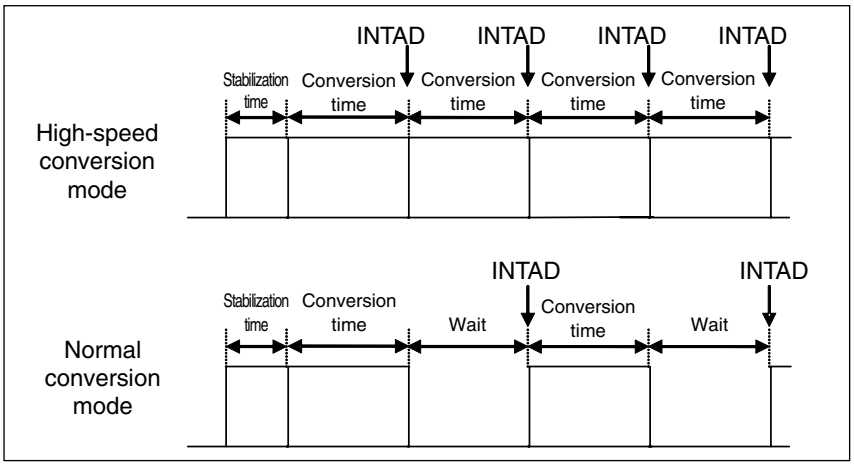
3.3 A/D Converter

The A/D converter has two main conversion modes: normal conversion mode and high-speed conversion mode, and several sub-modes, such as continuous select mode and continuous scan mode. In these latter modes, A/D conversion continues repeatedly until the conversion operation is stopped by a software setting (ADA0M0.ADA0CE bit = 0). When executing A/D conversion continuously like this, setting the normal conversion mode enables a reduction in the average current.

(1) Function details

In normal conversion mode, once A/D conversion has been enabled (ADA0M0.ADA0CE bit = 1) and after the stabilization time has elapsed, A/D conversion starts and continues for the specified conversion time. After conversion is complete, the A/D converter stops operating and the A/D conversion end interrupt request signal (INTAD) is generated after the specified wait time has elapsed. Because conversion operations are stopped during the wait period, the average current can be reduced. Figure 3-6 shows an operational image of high-speed conversion mode and normal conversion mode.

Figure 3-6. Operational Image of High-Speed and Normal Conversion Modes



(2) A/D converter mode register 1 (ADA0M1)

This register is used to specify the conversion time.

For details of the ADA0M1 register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 00H.

	7	6	5	4	3	2	1	0
ADA0M1	ADA0HS1	0	0	0	0	ADA0FR2	ADA0FR1	ADA0FR0

ADA0HS1	Specification of normal conversion mode/high-speed conversion mode
0	Normal conversion mode
1	High-speed conversion mode

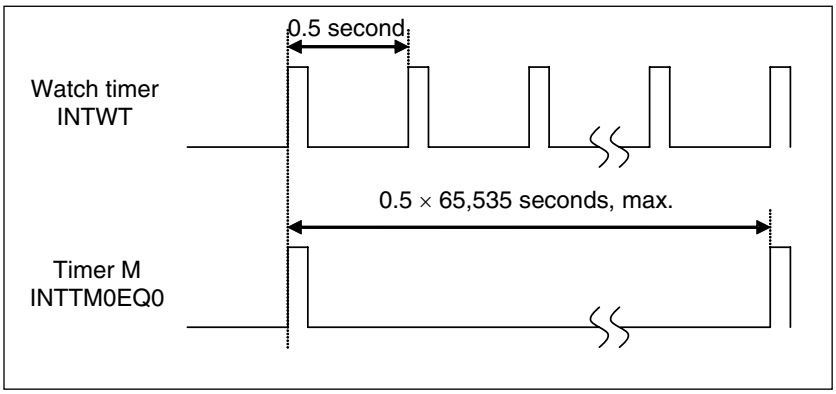
3.4 Watch Timer Function and Timer M

The watch timer generates an interrupt request signal (INTWT) at 0.25-second or 0.5-second time intervals. By using the watch timer in combination with timer M (TMM), the time count processing frequency can be significantly reduced, lowering the power supply current.

(1) Function details

When using the watch timer, the time count must be processed by using an interrupt request signal (INTWT). However, by selecting INTWT as the count clock of timer M (TMM) and processing the time count using timer M's compare match interrupt request signal (INTTM0EQ0), the frequency of processing the time count can be significantly reduced, lowering the power supply current. This is especially effective when the mode is continually switched between sub-IDLE mode and subclock operation mode because only watch-based count operations are executed. Figure 3-7 shows the timing at which the watch timer interrupt request signal (INTWT) and timer M's compare match interrupt request signal (INTTM0EQ0) are generated.

Figure 3-7. Timing of Watch Timer Interrupt and Timer M Interrupt



(2) TMM0 control register 0 (TM0CTL0)

This register is used to control the operations of TMM0 and select the count clock.

For details of the TM0CTL0 register, see the user's manual of the V850ES/Jx3-L product being used.

Reset sets this register to 00H.

	7	6	5	4	3	2	1	0
TM0CTL0	TM0CE	0	0	0	0	TM0CKS2	TM0CKS1	TM0CKS0

TM0CKS2	TM0CKS1	TM0CKS0	Count clock selection
0	0	0	f_{XX} (initial value)
0	0	1	$f_{XX}/2$
0	1	0	$f_{XX}/4$
0	1	1	$f_{XX}/64$
1	0	0	$f_{XX}/512$
1	0	1	INTWT ←Set value
1	1	0	$f_R/8$
1	1	1	f_{XT}

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