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April 1st, 2010 Renesas Electronics Corporation

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DATA SHEET



MOS FIELD EFFECT TRANSISTOR Phase-out/Discontinued 2SK3325

SWITCHING **N-CHANNEL POWER MOS FET INDUSTRIAL USE**

DESCRIPTION

The 2SK3325 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3325	TO-220AB
2SK3325-S	TO-262
2SK3325-ZJ	TO-263

FEATURES

- · Low gate charge: Qg = 22 nC TYP. (VDD = 400 V, VGS = 10 V, ID = 10 A)
- Gate voltage rating: ±30 V
- · Low on-state resistance
- $R_{DS(on)} = 0.85 \Omega MAX. (V_{GS} = 10 V, I_{D} = 5.0 A)$
- · Avalanche capability ratings
- TO-220AB, TO-262, TO-263 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	500	V
Gate to Source Voltage (VDS = 0 V)	VGSS(AC)	±30	V
Drain Current (DC)	D(DC)	±10	Α
Drain Current (pulse) ^{Note1}	D(pulse)	±40	Α
Total Power Dissipation (Tc = 25°C)	Рт	85	W
Total Power Dissipation (TA = 25°C)	Р⊤	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note2	las	10	Α
Single Avalanche Energy Note2	Eas	10.7	mJ



(TO-220AB)

(TO-262)







Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Starting $T_{ch} = 25 \,^{\circ}C$, $V_{DD} = 150 \,^{\circ}V$, $R_G = 25 \,^{\circ}\Omega$, $V_{GS} = 20 \,^{\circ}V \rightarrow 0 \,^{\circ}V$

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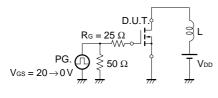
Document No. D14264EJ1V0DS00 (1st edition) Date Published May 2000 NS CP(K) Printed in Japan

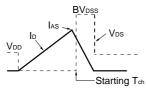
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ELECTRICAL CHARACTERISTICS (TA = 25 °C)

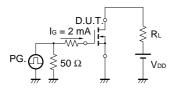
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	IDSS	$V_{DS} = 500 V$, $V_{GS} = 0 V$			100	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
Gate to Source Cut-off Voltage	VGS(off)	$V_{DS} = 10 V, I_{D} = 1 mA$	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 5.0 \text{ A}$	2.0	4.0		S
Drain to Source On-state Resistance	RDS(on)	$V_{GS} = 10 V, I_D = 5.0 A$		0.68	0.85	Ω
Input Capacitance	Ciss	Vbs = 10 V, Vgs = 0 V, f = 1 MHz		1200		pF
Output Capacitance	Coss			190		pF
Reverse Transfer Capacitance	Crss			10		pF
Turn-on Delay Time	td(on)	$V_{DD} = 150 V, I_D = 5.0 A, V_{GS(on)} = 10 V,$		21		ns
Rise Time	tr	$R_G = 10 \Omega$, $R_L = 60 \Omega$		11		ns
Turn-off Delay Time	td(off)			40		ns
Fall Time	tr			9.5		ns
Total Gate Charge	QG	$V_{DD} = 400 V, V_{GS} = 10 V, I_D = 10 A$		22		nC
Gate to Source Charge	QGS			6.5		nC
Gate to Drain Charge	Qgd			7.5		nC
Body Diode Forward Voltage	VF(S-D)	IF = 10 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	$I_F = 10 \text{ A}, \text{ V}_{GS} = 0 \text{ V}, \text{ di/dt} = 50 \text{ A}/\mu \text{s}$		0.5		μs
Reverse Recovery Charge	Qrr			2.6		μC

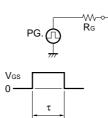
TEST CIRCUIT 1 AVALANCHE CAPABILITY





TEST CIRCUIT 3 GATE CHARGE

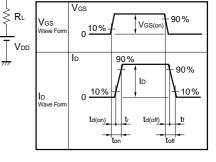




 $\begin{array}{l} \tau = 1 \ \mu s \\ \text{Duty Cycle} \leq 1 \ \% \end{array}$

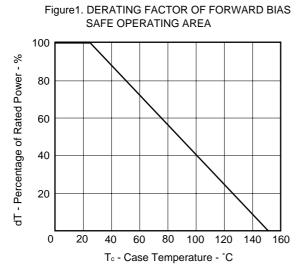
TEST CIRCUIT 2 SWITCHING TIME

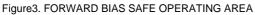
D.U.T.

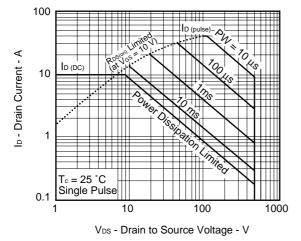


TYPICAL CHARACTERISTICS(TA = 25 °C)

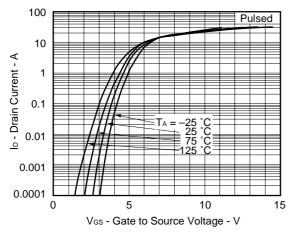
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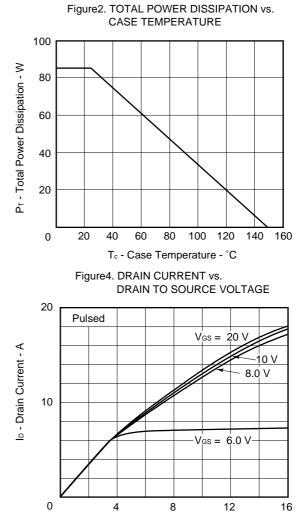






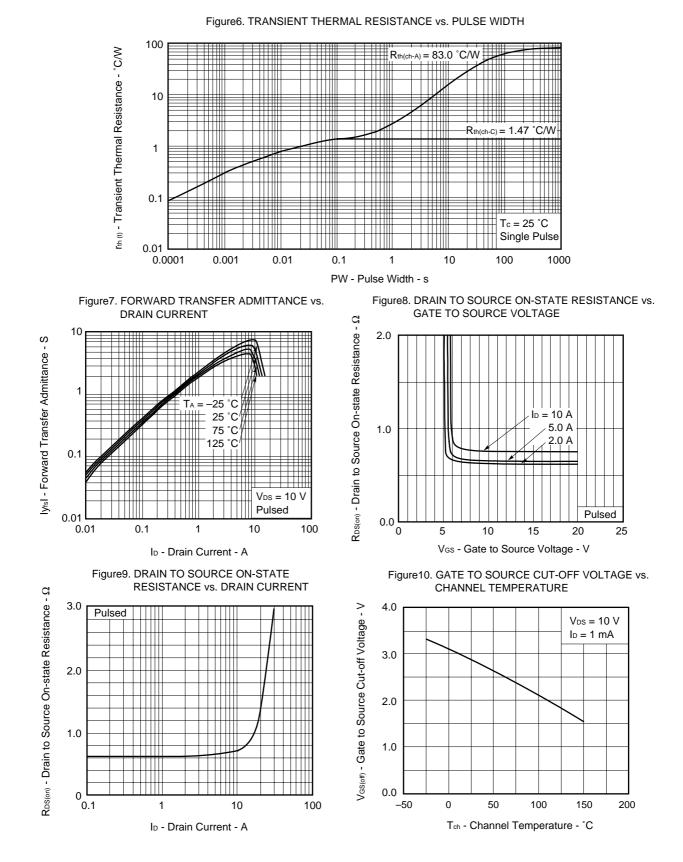






V_{DS} - Drain to Source Voltage - V

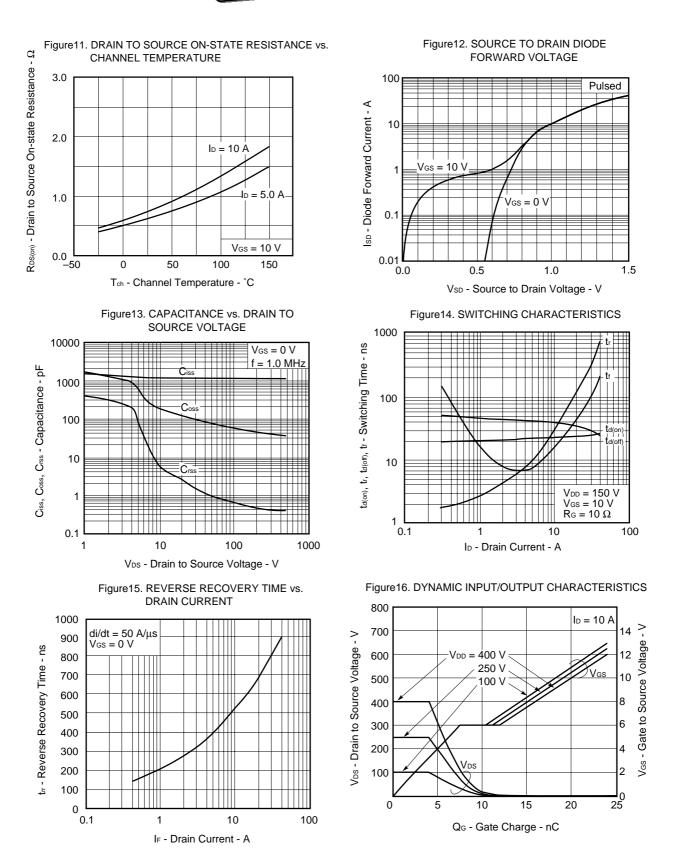
Phase-out/Discontinued



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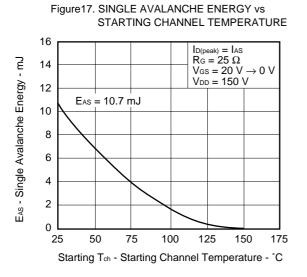
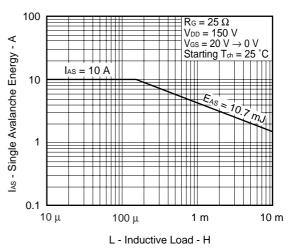


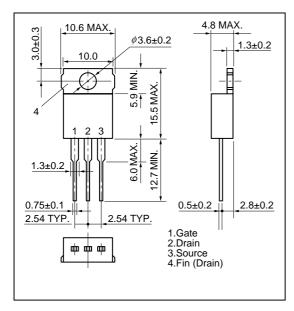
Figure18. SINGLE AVALANCHE ENERGY vs INDUCTIVE LOAD



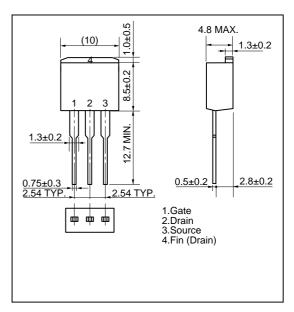
Phase-out/Discontinued

PACKAGE DRAWINGS (Unit : mm)

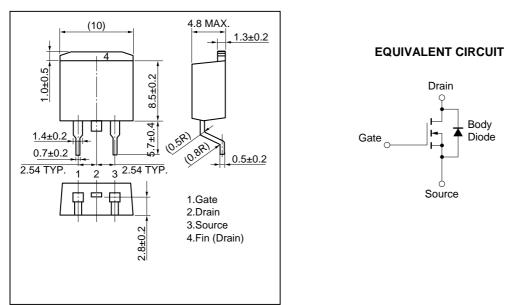
1)TO-220AB (MP-25)



2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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