Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

CK410M Compliant Main Clock

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential PCIEX/PEREQ# selectable pair
- 6 - 0.7V current-mode differential PCIEX pairs
- 1 - 0.7V current-mode differential CPU_ITP/PCIEX selectable pairs
- 1 - 0.7V current-mode differential SATA pair
- 1 - 0.7V current-mode differential LCDCLK/PCIEX/27MHz selectable pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 2 - REF, 14.318MHz

Key Specifications:

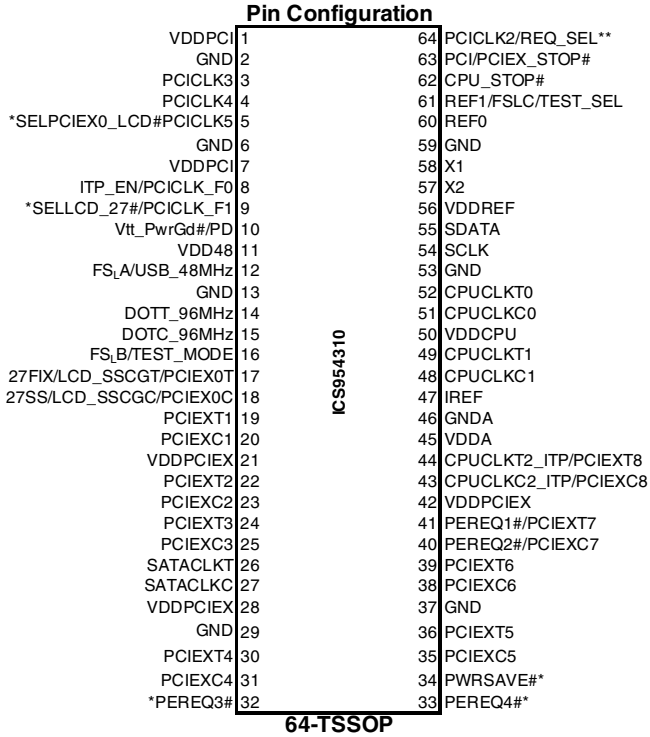
- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 300ppm frequency accuracy on CPU, PCIEX and SATA clocks
- +/- 100ppm frequency accuracy on USB clocks

Features/Benefits:

- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, PCIEX pair in PD for power management.
- PEREQ# pins to support PCIEX power management.
- PWR-SAVE pin for real time power saving.

Pin Configuration

Pin Configuration



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* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Note: Please add an external resister for pull up or down, never rely on an internal resister when the pin is connected to a device It is not recommended to connect dual function (I/O) pins to slots.

Functionality Table

FS_LC	FS_LB	FS_LA	CPU MHz	PCI MHz	PCIEX MHz	Spread %
0	0	0	266.66	33.33	100.00	0.5% Down
0	0	1	133.33	33.33	100.00	0.5% Down
0	1	0	200.00	33.33	100.00	0.5% Down
0	1	1	166.66	33.33	100.00	0.5% Down
1	0	0	333.33	33.33	100.00	0.5% Down
1	0	1	100.00	33.33	100.00	0.5% Down
1	1	0	400.00	33.33	100.00	0.5% Down
1	1	1	200.00	33.33	100.00	0.5% Down

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Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK3	OUT	PCI clock output.
4	PCICLK4	OUT	PCI clock output.
5	*SELPCIEX0_LCD#PCICLK5	I/O	Latched select input for LCDCLK/PCIEX output 0 = LCDCLK, 1 = PCIEX / 3.3V PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
9	*SELLCD_27#/PCICLK_F1	I/O	Free running PCI clock not affected by PCI_STOP#. SELLCD_27#: latched input to select pin functionality 1 = LCDCLK pair 0 = 27MHzSS/27MHzSS# pair
10	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
17	27FIX/LCD_SSCGT/PCIEX0T	OUT	True clock of LCDCLK output / True clock of PCIEXCLK differential pair/27MHz Non-Spread Push-Pull output, selected by SELPCIEX0_LCD# and SELLCD_27#.
18	27SS/LCD_SSCGC/PCIEX0C	OUT	Complementary clock of LCDCLK_SS output / Complementary clock of PCIEXCLK differential pair/27MHz Spreading Push-Pull output, selected by SELPCIEX0_LCD# and SELLCD_27#.
19	PCIEXT1	OUT	True clock of differential PCI_Express pair.
20	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
21	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
22	PCIEXT2	OUT	True clock of differential PCI_Express pair.
23	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
24	PCIEXT3	OUT	True clock of differential PCI_Express pair.
25	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
26	SATACLKT	OUT	True clock of differential SATA pair.
27	SATACLKC	OUT	Complement clock of differential SATA pair.
28	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
29	GND	PWR	Ground pin.
30	PCIEXT4	OUT	True clock of differential PCI_Express pair.
31	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
32	*PEREQ3#	IN	Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled.

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Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
33	PEREQ4#*	IN	Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled.
34	PWRSAVE#*	IN	Active-low input pin used to change frequency to underclocked entries in the ROM table that can be pre-programmed through Byte 6 of the I2c.
35	PCIEXC5	OUT	Complement clock of differential PCI_Express pair.
36	PCIEXT5	OUT	True clock of differential PCI_Express pair.
37	GND	PWR	Ground pin.
38	PCIEXC6	OUT	Complement clock of differential PCI_Express pair.
39	PCIEXT6	OUT	True clock of differential PCI_Express pair.
40	PEREQ2#/PCIEXC7	I/O	Real-time input pin that controls PCIEXCLK outputs that are selected through REQ_SEL. 0 = PCIEXC7, 1 = PECLKQ2#. / Complement clock of differential PCI Express output.
41	PEREQ1#/PCIEXT7	I/O	Real-time input pin that controls PCIEXCLK outputs that are selected through REQ_SEL. 0 = PCIEXT7, 1 = PECLKQ1#. / True clock of differential PCI Express output.
42	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
43	CPUCLKC2_ITP/PCIEXC8	OUT	Complementary clock of CPU_ITP/PCIEX differential pair CPU_ITP/PCIEX output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
44	CPUCLKT2_ITP/PCIEXT8	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair
45	VDDA	PWR	3.3V power for the PLL core.
46	GNDA	PWR	Ground pin for the PLL core.
47	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
48	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
50	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
51	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
53	GND	PWR	Ground pin.
54	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
55	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
56	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
57	X2	OUT	Crystal output, Nominally 14.318MHz
58	X1	IN	Crystal input, Nominally 14.318MHz.
59	GND	PWR	Ground pin.
60	REF0	OUT	14.318 MHz reference clock.
61	REF1/FSLC/TEST_SEL	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
62	CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
63	PCI/PCIEX_STOP#	IN	Stops all PCICLKs and PCIEXCLKs besides the free-running clocks at logic 0 level, when input low
64	PCICLK2/REQ_SEL**	I/O	3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ#

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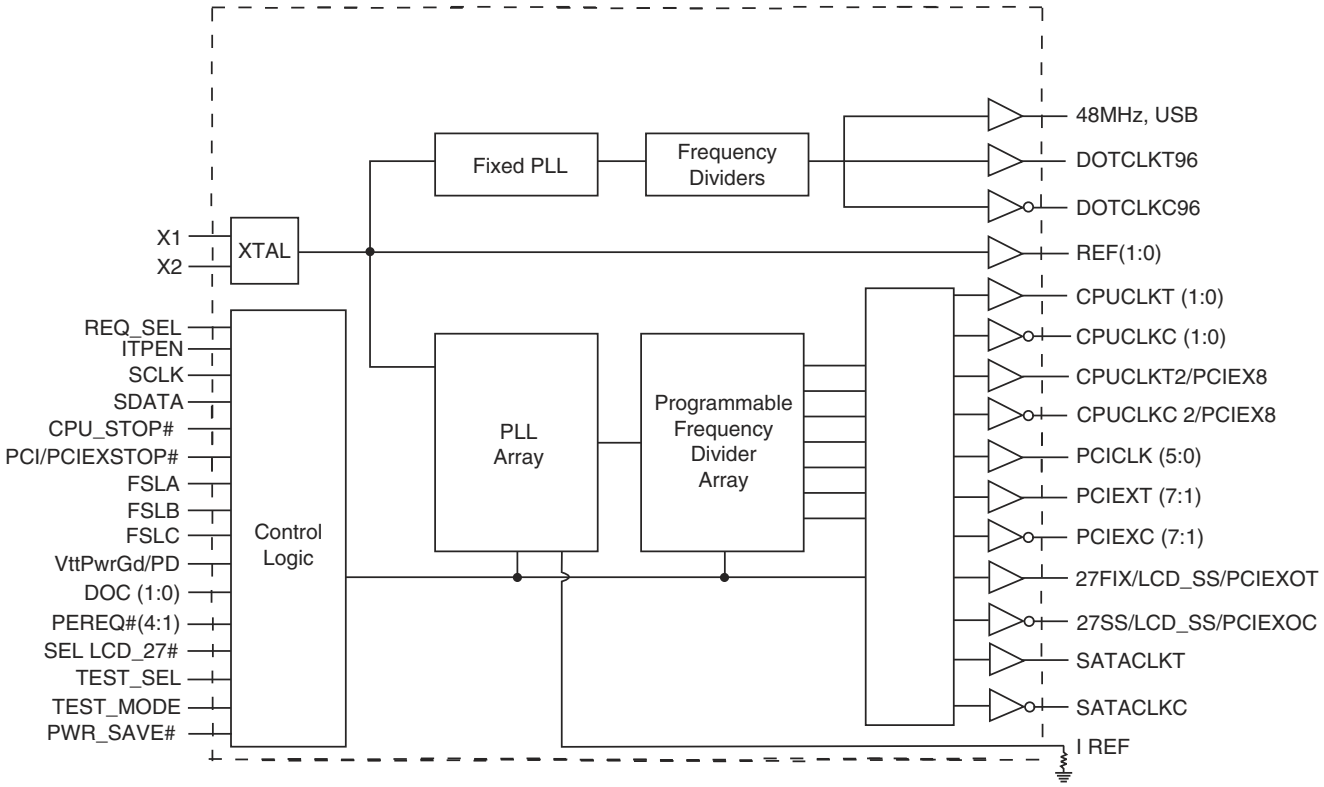
General Description

ICS954310 follows the Intel CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954310** is driven with a 14.318MHz crystal.

Block Diagram



Power Supply

PIN NUMBER		Description
VDD	GND	
1,7	2,6	PCICLK outputs
11	13	48MHz,96Mhz, LCDCLK, Fix Digital, Fix Analog
45	46	Master clock, CPU Analog
21, 28, 42	29, 37	PCIEXT/C outputs
50	53	CPUT/C output
56	59	Xtal, REF

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General I²C serial interface information for the ICS954310

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X (H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Table 1: CPU/PCIEX Frequency Selection Table

FS4	FS3	FS_LC	FS_LB	FS_LA	CPU MHz	PCI MHz	PCIEX MHz	Spread %
0	0	0	0	0	266.66	33.33	100.00	0.5% Down
0	0	0	0	1	133.33	33.33	100.00	0.5% Down
0	0	0	1	0	200.00	33.33	100.00	0.5% Down
0	0	0	1	1	166.66	33.33	100.00	0.5% Down
0	0	1	0	0	333.33	33.33	100.00	0.5% Down
0	0	1	0	1	100.00	33.33	100.00	0.5% Down
0	0	1	1	0	400.00	33.33	100.00	0.5% Down
0	0	1	1	1	200.00	33.33	100.00	0.5% Down
0	1	0	0	0	266.66	33.33	100.00	+/- 0.25 Center
0	1	0	0	1	133.33	33.33	100.00	+/- 0.25 Center
0	1	0	1	0	200.00	33.33	100.00	+/- 0.25 Center
0	1	0	1	1	166.66	33.33	100.00	+/- 0.25 Center
0	1	1	0	0	333.33	33.33	100.00	+/- 0.25 Center
0	1	1	0	1	100.00	33.33	100.00	+/- 0.25 Center
0	1	1	1	0	400.00	33.33	100.00	+/- 0.25 Center
0	1	1	1	1	200.00	33.33	100.00	+/- 0.25 Center
1	0	0	0	0	261.33	32.66	98	+/- 0.25 Center
1	0	0	0	1	130.66	32.66	98	+/- 0.25 Center
1	0	0	1	0	196.00	32.66	98	+/- 0.25 Center
1	0	0	1	1	163.33	32.66	98	+/- 0.25 Center
1	0	1	0	0	253.33	31.66	95	+/- 0.25 Center
1	0	1	0	1	126.66	31.66	95	+/- 0.25 Center
1	0	1	1	0	190.00	31.66	95	+/- 0.25 Center
1	0	1	1	1	158.33	31.66	95	+/- 0.25 Center
1	1	0	0	0	247.99	31.00	93	+/- 0.25 Center
1	1	0	0	1	124.00	31.00	93	+/- 0.25 Center
1	1	0	1	0	186.00	31.00	93	+/- 0.25 Center
1	1	0	1	1	154.99	31.00	93	+/- 0.25 Center
1	1	1	0	0	239.99	30.00	90	+/- 0.25 Center
1	1	1	0	1	120.00	30.00	90	+/- 0.25 Center
1	1	1	1	0	180.00	30.00	90	+/- 0.25 Center
1	1	1	1	1	149.99	30.00	90	+/- 0.25 Center

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Table2: LCDCLK Spread and Frequency Selection Table

SELLCD (27#)	Byte 9b7 SS3	Byte9b6 SS2	Byte 9b5 SS1	Byte 9b4 SS0	Pin 17/18	Spread	
					MHz	%	
0	0	0	0	0	27.00	+/-0.25	Center
0	0	0	0	1	27.00	+/-0.50	Center
0	0	0	1	0	27.00	+/-0.75	Center
0	0	0	1	1	27.00	+/-1.0	Center
0	0	1	0	0	27.00	+/-1.25	Center
0	0	1	0	1	27.00	+/-1.5	Center
0	0	1	1	0	27.00	+/-1.75	Center
0	0	1	1	1	27.00	+/-2	Center
0	1	0	0	0	27.00	-0.5	Down
0	1	0	0	1	27.00	-1	Down
0	1	0	1	0	27.00	-1.25	Down
0	1	0	1	1	27.00	-1.5	Down
0	1	1	0	0	27.00	-1.75	Down
0	1	1	0	1	27.00	-2	Down
0	1	1	1	0	27.00	-2.5	Down
0	1	1	1	1	27.00	-3	Down
1	0	0	0	0	96.00	+/-1.5	Center
1	0	0	0	1	96.00	+/-1.25	Center
1	0	0	1	0	96.00	+/-1.0	Center
1	0	0	1	1	96.00	+/-0.8	Center
1	0	1	0	0	96.00	+/-0.6	Center
1	0	1	0	1	96.00	+/-0.5	Center
1	0	1	1	0	96.00	+/-0.4	Center
1	0	1	1	1	96.00	+/-0.3	Center
1	1	0	0	0	96.00	3	Down
1	1	0	0	1	96.00	2.5	Down
1	1	0	1	0	96.00	2	Down
1	1	0	1	1	96.00	1.75	Down
1	1	1	0	0	96.00	1.5	Down
1	1	1	0	1	96.00	1.25	Down
1	1	1	1	0	96.00	1	Down
1	1	1	1	1	96.00	0.8	Down

Table3: SATA Spread and Frequency Selection Table

SEL_SATA	Byte 16b3 SS3	Byte16b2 SS2	Pin 27/26	Spread	
			MHz	%	
1	0	0	100.00	-0.2	Down
1	0	1	100.00	-0.3	Down
1	1	0	100.00	-0.4	Down
1	1	1	100.00	-0.5	Down

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I2C Table: Output Control Register

Byte 0	Name	Control Function	Type	0	1	PWD
Bit 7	CPUCLK2_ITP/PCIE X8 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 6	PCIEX7 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 5	PCIEX5 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 4	PCIEX4 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 3	PCIEX3 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 2	PCIEX2 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 1	PCIEX1 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 0	LCD/PCIEX0 Enable	Output Enable	RW	Disable (HiZ)	Enable	1

I2C Table: Output Control Register

Byte 1	Name	Control Function	Type	0	1	PWD
Bit 7	PCICLK_4	Output Enable	RW	Disable	Enable	1
Bit 6	DOT_96MHz Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 5	USB_48MHz Enable	Output Enable	RW	Disable	Enable	1
Bit 4	REF1 Enable	Output Enable	RW	Disable	Enable	1
Bit 3	PCIEX6 Enable	Output Enable	RW	Disable	Enable	1
Bit 2	CPUCLK_1 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 1	CPUCLK_0 Enable	Output Enable	RW	Disable (HiZ)	Enable	1
Bit 0	Spread Spectrum Mode	Spread Control for PLL1	RW	SPREAD OFF	SPREAD ON	1

I2C Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD
Bit 7	PCICLK3	Output Enable	RW	Disable	Enable	1
Bit 6	PCICLK2	Output Enable	RW	Disable	Enable	1
Bit 5	PCICLK_F1	Output Enable	RW	Disable	Enable	1
Bit 4	PCICLK_F0	Output Enable	RW	Disable	Enable	1
Bit 3	PCICLK5	Output Enable	RW	Disable	Enable	1
Bit 2	27MHz (Fixed)	Output Enable	RW	Disable	Enable	1
Bit 1	27MHz (SS)	Output Enable	RW	Disable	Enable	1
Bit 0	SATACLK	Output Enable	RW	Disable (HiZ)	Enable	1

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I2C Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD
Bit 7	PCIEX6	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in I2C register to stop PCIEX clocks.	RW	Free-Running	Stoppable	0
Bit 6	PCIEX5		RW	Free-Running	Stoppable	0
Bit 5	PCIEX4		RW	Free-Running	Stoppable	0
Bit 4	SATACLK		RW	Free-Running	Stoppable	0
Bit 3	PCIEX3		RW	Free-Running	Stoppable	0
Bit 2	PCIEX2		RW	Free-Running	Stoppable	0
Bit 1	PCIEX1		RW	Free-Running	Stoppable	0
Bit 0	PCIEX0		RW	Free-Running	Stoppable	0

I2C Table: Output Control Register

Byte 4	Name	Control Function		0	1	PWD
Bit 7	PCIEX7	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 6	DOT_96MHz	Driven in PD	RW	Driven	Hi-Z	0
Bit 5	PCIEX8	Free-Running Control	RW	Free-Running	Stoppable	0
Bit 4	PCICLK_F1	Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCI	RW	Free-Running	Stoppable	0
Bit 3	PCICLK_F0		RW	Free-Running	Stoppable	0
Bit 2	CPUCLK_2/ITP	Allow assertion of CPU_STOP# to stop CPU clocks.	RW	Free-Running	Stoppable	1
Bit 1	CPUCLK_1		RW	Free-Running	Stoppable	1
Bit 0	CPUCLK_0		RW	Free-Running	Stoppable	1

I2C Table: Output Control Register

Byte 5	Name	Control Function		0	1	PWD
Bit 7	PCIEX(8:0)/SATACLK PCI/PCIEX_STOP#	Driven in PCI/PCIEX_STOP#	RW	Driven	Hi-Z	0
Bit 6	CPUCLK2_ITP CPU_STOP# Drive	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 5	CPUCLK_1 CPU_STOP# Drive	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 4	CPUCLK_0 CPU_STOP# Drive	Driven in CPU_STOP#	RW	Driven	Hi-Z	0
Bit 3	PCIEX(8:0)/SATACLK, 96MHz_SS	Driven in PD	RW	Driven	Hi-Z	0
Bit 2	CPUCLK2_ITP PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 1	CPUCLK_1 PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 0	CPUCLK_0 PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0

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I2C Table: Frequency Select Register

Byte 6	Name	Control Function	Type	0	1	PWD
Bit 7	PWRSAVE	PWR_SAVE programming	RW	IIC	PWR_SAVE programming	0
Bit 6	FS4	Frequency Select bit	RW	See Table 1: Frequency Selection Table		0
Bit 5	FS3	Frequency Select bit	RW			0
Bit 4	REF0 STRENGTH	Strength Prog	RW	1X	2X	0
Bit 3	PCI/SRC_STOP#	Stop all PCI and SRC clocks	RW	Outputs Stopped	Outputs Active	1
Bit 2	FSL_C	Frequency Select bit	RW	See Table 1: Frequency Selection Table		latch
Bit 1	FSL_B	Frequency Select bit	RW			latch
Bit 0	FSL_A	Frequency Select bit	RW			latch

I2C Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD
Bit 7	RID3	Revision ID	R	-	-	0
Bit 6	RID2		R	-	-	0
Bit 5	RID1		R	-	-	1
Bit 4	RID0		R	-	-	0
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	001 = ICS	-	0
Bit 0	VID0		R	-	-	1

I2C Table: PEREQ Control Register

Byte 8	Name	Control Function	Type	0	1	PWD
Bit 7	PEREQ2# Control	PCIEX8 is controlled	RW	Not Controlled	Controlled	0
Bit 6	PEREQ2# Control	PCIEX1 is controlled	RW	Not Controlled	Controlled	0
Bit 5	Reserved	Reserved	RW	-	-	1
Bit 4	Reserved	Reserved	RW	-	-	1
Bit 3	Reserved	Reserved	RW	-	-	1
Bit 2	Reserved	Reserved	RW	-	-	1
Bit 1	PEREQ1# Control	PCIEX6 is controlled	RW	Not Controlled	Controlled	0
Bit 0	PEREQ1# Control	PCIEX0 is controlled	RW	Not Controlled	Controlled	0

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I2C Table: LCDCLK and M/N Control Register

Byte 9	Name	Control Function	Type	0	1	PWD
Bit 7	LCDCLK_SS3	Bit S3	RW	See LCDCLK_SS Frequency Select Table 2		0
Bit 6	LCDCLK_SS2	Bit S2	RW			1
Bit 5	LCDCLK_SS1	Bit S1	RW			1
Bit 4	LCDCLK_SS0	Bit S0	RW			1
Bit 3	*SEL SRC_LCDCLK#	Selects SRC or LCD/27MHz on pins 17	R	LCDCLK	PCIEX0	latch
Bit 2	REF 0	Output Enable	RW	Disable	Enable	1
Bit 1	LCDCLK_SS Spread Enable	Enable SS	RW	OFF	ON	1
Bit 0	M/N Enable	PLL M/N Programming Enable	RW	Disable	Enable	0

I2C Table: Byte Count Register

Byte 10	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	X
Bit 6	Reserved	Reserved	RW	-	-	X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	BC4	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 15 = 21 Bytes.		1
Bit 3	BC3		RW			0
Bit 2	BC2		RW			1
Bit 1	BC1		RW			0
Bit 0	BC0		RW			1

I^{2}C Table: PLL1 Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	PWD
Bit 7	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	M Div5	M Divider Programming bits	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

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I²C Table: PLL1 Frequency Control Register

Byte 12	Name	Control Function	Type	0	1	PWD
Bit 7	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	N Div6		RW			X
Bit 5	N Div5		RW			X
Bit 4	N Div4		RW			X
Bit 3	N Div3		RW			X
Bit 2	N Div2		RW			X
Bit 1	N Div1		RW			X
Bit 0	N Div0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 13	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 14	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	R	-	-	0
Bit 6	SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1		X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

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I2C Table: PEREQ Control Register

Byte 15	Name	Control Function	Type	0	1	PWD
Bit 7	PEREQ4# Control	PCIEX7 is controlled	RW	Not Controlled	Controlled	0
Bit 6	PEREQ4# Control	PCIEX5 is controlled	RW	Not Controlled	Controlled	0
Bit 5	PEREQ4# Control	PCIEX3 is controlled	RW	Not Controlled	Controlled	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	PEREQ3# Control	PCIEX4 is controlled	RW	Not Controlled	Controlled	0
Bit 0	PEREQ3# Control	PCIEX2 is controlled	RW	Not Controlled	Controlled	0

I2C Table: SATACLK Control Register

Byte 16	Name	Control Function	Type	0	1	PWD
Bit 7	SEL_SATA	SATACLK Spread Control	RW	PCIEX PLL	SATA PLL	1
Bit 6	SEL_LCD(27#)	Select LCD or 27MHz for pins 17 and 18	RW	27MHz	LCDCLK	latch
Bit 5	PCIEX source	PCIEX comes from	RW	PCIEX PLL	SATA PLL	0
Bit 4	SATA SS ENABLE	SPREAD ENABLE SATA PLL	RW	OFF	ON	1
Bit 3	SATA_SS1	Bit S1	RW	See SATA_SS Frequency Select Table 3		1
Bit 2	SATA_SS0	Bit S0	RW			1
Bit 1	PCI source	PCI comes from	RW	PCIEX PLL	SATA PLL	0
Bit 0	Reserved	Reserved	RW	-	-	1

I^2C Table: PLL2 Frequency Control Register

Byte 17	Name	Control Function	Type	0	1	PWD
Bit 7	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	N Div9	N Divider Prog bit 9	RW			X
Bit 5	M Div5	M Divider Programming bits	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

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I²C Table: PLL2 Frequency Control Register

Byte 18	Name	Control Function	Type	0	1	PWD
Bit 7	N Div7	N Divider Programming b(8:0)	R	The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	N Div6		RW			X
Bit 5	N Div5		RW			X
Bit 4	N Div4		RW			X
Bit 3	N Div3		RW			X
Bit 2	N Div2		RW			X
Bit 1	N Div1		RW			X
Bit 0	N Div0		RW			X

I2C Table: PLL 2 Spread Spectrum Control Register

Byte 19	Name	Control Function	Type	0	1	PWD
Bit 7	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

I2C Table: PLL 2 Spread Spectrum Control Register

Byte 20	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		0
Bit 6	SSP14	Spread Spectrum Programming b(14:8)	RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

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Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	ºC	1
Case Temperature	Tcase	-			115	ºC	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

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Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	$V_{OL} = 0.175V$, $V_{OH} = 0.525V$	175		700	ps	1
Fall Time	t_f	$V_{OH} = 0.525V$ $V_{OL} = 0.175V$	175		700	ps	1
Rise Time Variation	d-t_r	$V_{OL} = 0.175V$, $V_{OH} = 0.525V$			125	ps	1
Fall Time Variation	d-t_f	$V_{OH} = 0.525V$ $V_{OL} = 0.175V$			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%			100	ps	1
Skew	t_{sk4}	CPU(1:0) to CPU2_ITP, V_T = 50%			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}$*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[3] Spread Spectrum is off

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Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	2
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t_{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - DOT_96MHz 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
Absolute min period	Tabsmin	96.00MHz nominal	10.1635			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - 27MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
			-15	0	15		1,2,3
Clock period	T_{period}	27.000MHz output nominal	37.0365	37.0370	37.0376	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4	3.25		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.05	0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29	-73		mA	1
		V_{OH}@MAX = 3.135 V		-10	-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29	72		mA	1
		V_{OL} @ MAX = 0.4 V		27	27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	2.35	4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.83333333	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.86956522	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.5	55	%	1
Jitter	t_{itj}	Long Term (10us)		500	800	ps	1
	t_{jpk-pk}		-250	117.5	250	ps	1
	$t_{jcyc-cyc}$	V_T = 1.5 V		170	500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] At nominal voltage and temperature

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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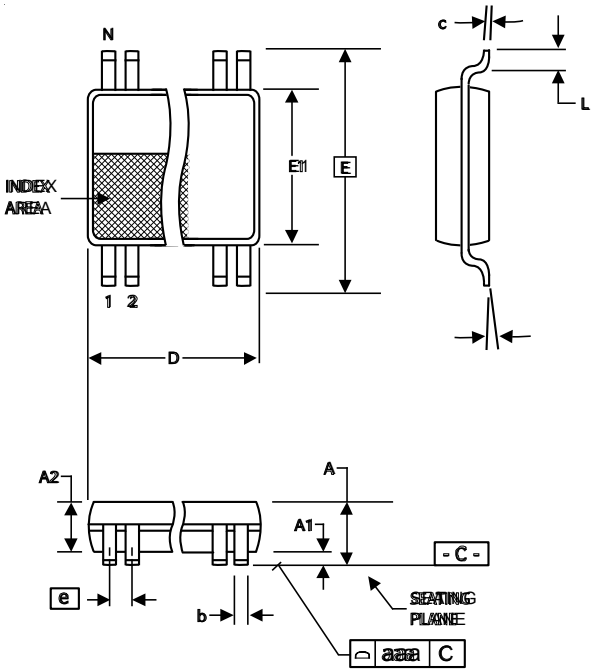

6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

954310yGLF-T

Example:

XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

1043—11/28/05

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