Description

The 9INT31H200 is a 2-output very high-performance HCSL fanout buffer for high performance interconnect applications. It can be used at speeds up to 350MHz and is compliant to the DB200H specification.

Typical Applications

- DB200H
- Ethernet
- PCIe

Output Features

- 2 HCSL differential pairs

Key Specifications

- Qx output-to-output skew across all outputs: 5ps (typical)
- RMS additive phase jitter: 64fs typical (12kHz–20MHz at 156.25MHz)

Features

- Extremely low additive phase jitter; supports DB200H requirements
- 3.3V operation; standard industry power supply
- 2 OE pins (1 for each output); easy control of clocks to CPU sockets
- HCSL-compatible input; supports popular devices
- 1MHz to 350MHz operating frequency; covers all popular Ethernet frequencies
- Space saving 3 × 3 mm 16-QFN; minimal board space

Block Diagram

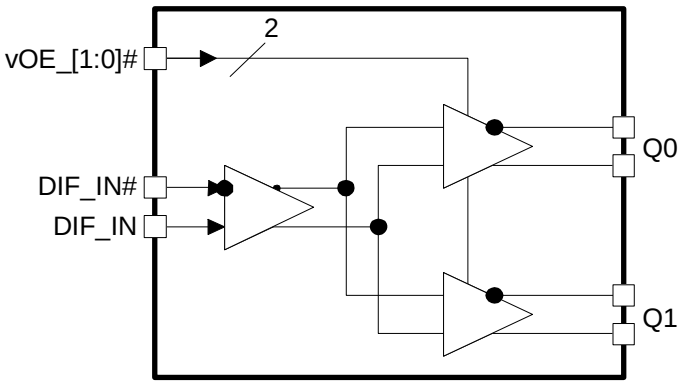


Table 1. Power Management

DIF_IN	OEx# Pin	Qx	nQx
Running	1	Low[1]	Low[1]
Running	0	Running	Running
Not Running	X	X	X

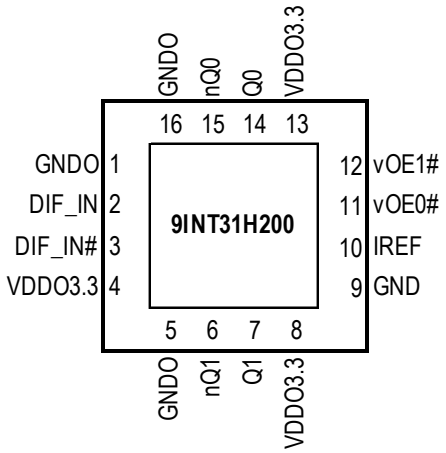
Notes:
1. The outputs are tristated, and the termination networks pulls them low.

Table 2. Power Connections

Pin Number		Description
VDD	GND	
4	1	Input receiver analog
8, 13	5, 9, 16	DIF outputs

Pin Assignments

Figure 1. Pin Assignments for 3 × 3 mm 16-QFN Package – Top View



16-QFN, 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	GNDO	GND	Ground pin for outputs.
2	DIF_IN	IN	HCSL true input.
3	DIF_IN#	IN	HCSL complementary input.
4	VDDO3.3	PWR	Power supply for outputs, nominally 3.3V.
5	GNDO	GND	Ground pin for outputs.
6	nQ1	OUT	Inverting output of differential pair 1.
7	Q1	OUT	Non-inverting output of differential pair 1.
8	VDDO3.3	PWR	Power supply for outputs, nominally 3.3V.
9	GND	GND	Ground pin.
10	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
11	vOE0#	IN	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
12	vOE1#	IN	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs.
13	VDDO3.3	PWR	Power supply for outputs, nominally 3.3V.
14	Q0	OUT	Non-inverting output of differential pair 0.
15	nQ0	OUT	Inverting output of differential pair 0.
16	GNDO	GND	Ground pin for outputs.
17	EPAD	GND	Connect epad to ground.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9INT31H200 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_{AMB} = T_{COM} or T_{IND} unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage - DIF_IN	V_{CROSS}	Crossover voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Current Consumption

T_A = T_{IND}; supply voltage VDDx = 3.3V +/-5% ; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	$I_{DD3.3OP}$	All outputs running at 350MHz C_L = 2pF; Zo = 85Ω.		65	80	mA	-
	$I_{DD3.3STBY}$	1 output running at 350MHz, other output disabled.		50	62	mA	-
	$I_{DD3.3IDLE}$	All outputs stopped, input clock running at 350MHz or stopped.		35	43	mA	-

Electrical Characteristics–Input/Supply/Common Parameters

T_{AMB} = T_{COM} or T_{IND} unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx	Supply voltage	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range (T_{IND})	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	µA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	µA	
Input Frequency	F_{in}	V_{DD} = 3.3 V	1		350	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.1	1.8	ms	1,2
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4	6	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		40	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	2
Trise	t_R	Rise time of control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] DIF_IN input.

Electrical Characteristics–Qx HCSL/LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	1	1.5	2	0.6 - 4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		7	15	20	%	1,4
Voltage High	Vhigh	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	625	681	725	850	mV	
Voltage Low	Vlow		-25	14	50	150		
Max Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).		705	750	1150	mV	
Min Voltage	Vmin		-50	-3		-300		
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	325	349	375	250 - 550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		3.4	20	140	mV	1,6

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Qx Output Duty Cycle, Jitter, and Skew Characteristics

$T_A = T_{IND;}$ supply voltage VDDx = 3.3V +/-5%; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially	-0.5	0	0.5	%	1,2
Skew, Input to Output	t_{PD}	V_T = 50%	2.3	2.6	3.1	ps	1
Skew, Output to Output	t_{sk3}	Across all outputs, V_T = 50%		5	40	ps	1
Jitter, Cycle to cycle additive	$t_{jcyc-cycadd}$	*Additive*		1.1	2	ps	1,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

[3] Measured from differential waveform.

Electrical Characteristics–Additive Phase Jitter

$T_A = T_{IND;}$ supply voltage VDDx = 3.3V +/-5%; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Additive Phase Jitter	t_{jph}	All outputs running at 156.25MHz, 12kHz to 20MHz		64	75	fs (rms)	1,2,3

[1] Applies to all outputs.

[2] Signal source is Wenzel.

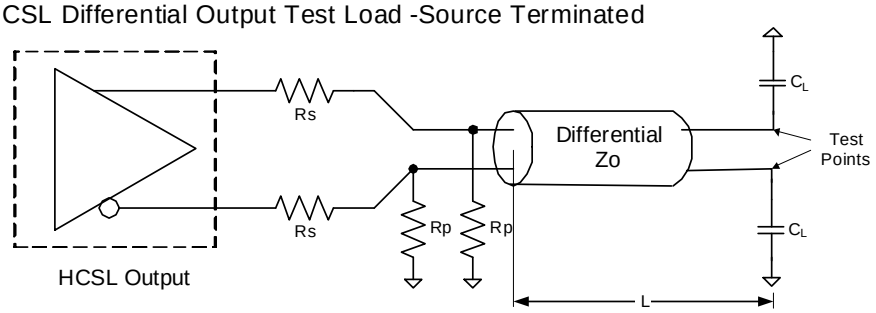
[3] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2].

Test Loads

Differential Output Termination Table

DIF Zo (Ω)	L (in)	C_L (pF)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	5	2	475	33	50
85	5	2	412	27	42.2 or 43.2

HCSL Differential Output Test Load -Source Terminated



Thermal Characteristics

Table 3. Thermal Characteristics [1]

Symbol	Parameter	Typical Value	Units
θ_{JC}	Junction to case	65.8	°C/W
θ_{Jb}	Junction to base	5.1	°C/W
θ_{JA0}	Junction to Air, still air	63.2	°C/W
θ_{JA1}	Junction to Air, 1 m/s air flow	55.9	°C/W
θ_{JA3}	Junction to Air, 3 m/s air flow	51.4	°C/W
θ_{JA5}	Junction to Air, 5 m/s air flow	49.2	°C/W

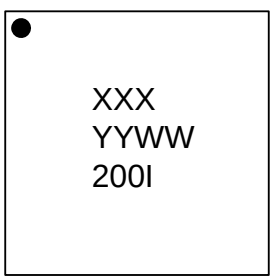
[1] ePad soldered to board.

Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nlnlg16p2

Marking Diagram



1. “XXX” is the last three characters of the Asm lot.
2. “YYWW” is the last digits of the year and week that the part was assembled.
3. Line 3 is the truncated part number.
4. “I” denotes industrial temperature.

Ordering Information

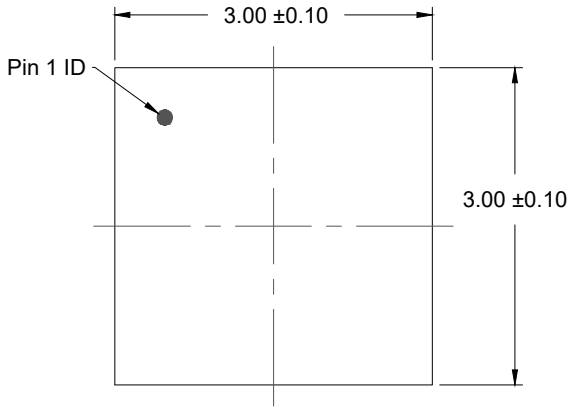
Orderable Part Number	Package	Carrier Type	Temperature
9INT31H200NLGI	3 × 3 mm, 0.5mm pitch 16-QFN	Tray	-40° to +85°C
9INT31H200NLGI8	3 × 3 mm, 0.5mm pitch 16-QFN	Tape and Reel	-40° to +85°C

Revision History

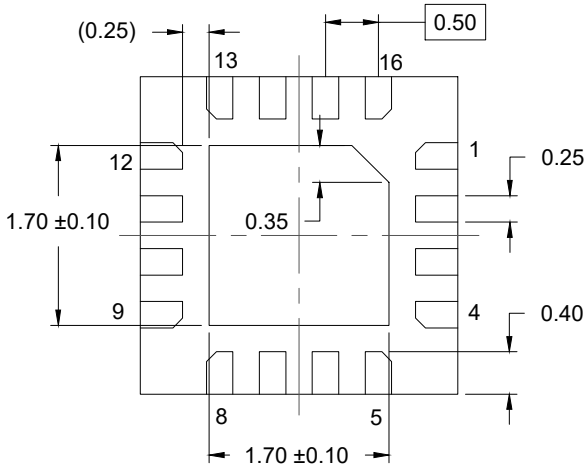
Revision Date	Description of Change
August 9, 2018	Initial release.

Package Outline Drawing

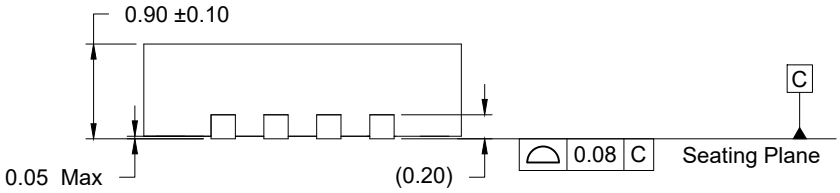
Package Code: NLG16P2
16-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4169-02, Revision: 06, Date Created: Aug 18, 2023



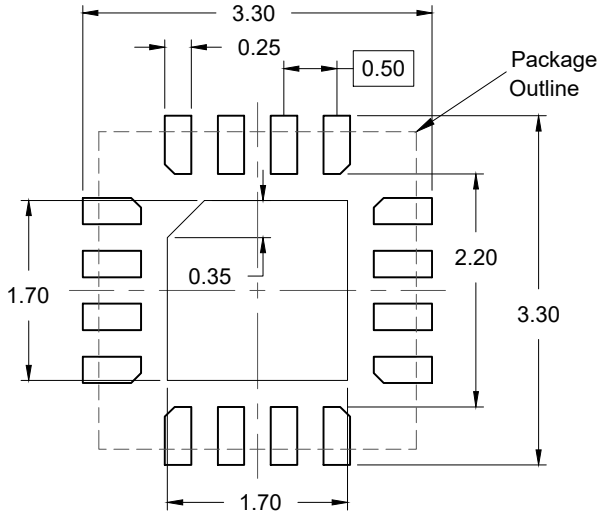
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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