General Description

The 9LRS4206 is a low power CK505-compliant clock specification. This clock synthesizer provides a single chip solution for Intel processors and Intel chipsets. The 9LRS4206 is driven with a 14.318MHz crystal.

Recommended Application

Low Power CK505 Compliant Main Clock

Output Features

- 1 - 0.8V push-pull differential CPU pair
- 1- 0.8V push-pull differential PCIEX pair
- 1 - 0.8V push-pull differential SATA pair
- 1 - 0.8V push-pull differential DOT96 pair
- 1 - USB, 48MHz
- 1 - REF, 14.318MHz

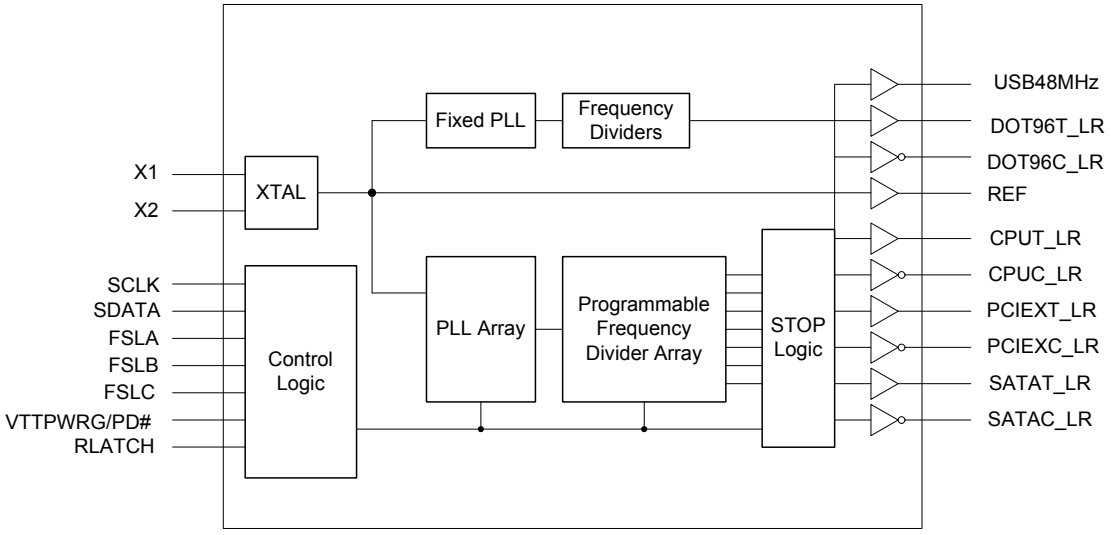
Features/Benefits

- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Low power differential clock outputs (No 50Ω resistor to GND needed)
- Integrated 33Ω series resistor on all differential outputs
- Meets PCIEX Gen2 Specification

Key Specifications

- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- ±100ppm frequency accuracy on CPU, PCIEX and SATA clocks
- ±100ppm frequency accuracy on USB clocks

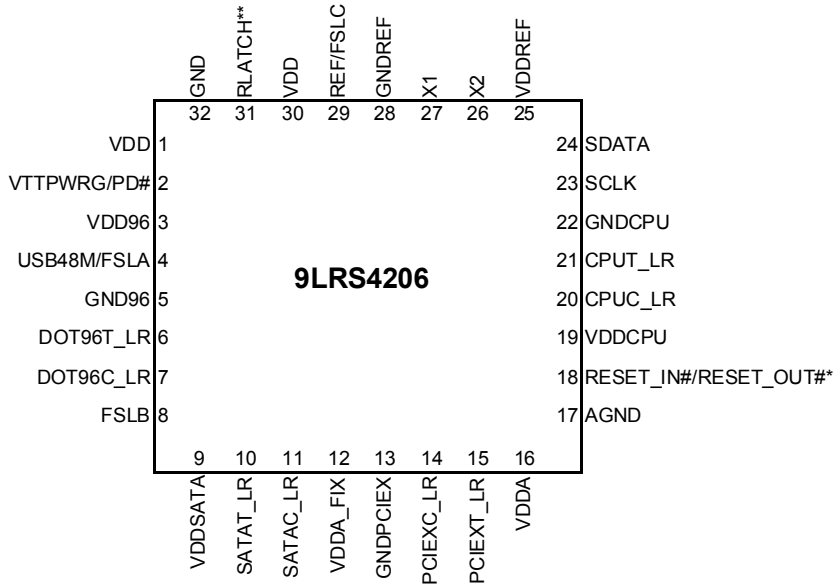
Block Diagram



Preferred drive strengths using CK505 clock sources.
Transmission lines to load do not share series resistors.
Desktop (Zo=50Ω) and mobile (Zo=55Ω) have the same drive strength.

	Number of Loads to Drive	Match Point for N & P Voltage / Current (mA)	Number of Loads Actually Driven.		
			1 Load Rs =	2 Loads Rs=	3 Loads Rs =
D.C.Drive Strength	1	0.56 / 33 (17Ω)	33Ω [39Ω]	-	-
	2	0.92 / 66 (14Ω)	39Ω [43Ω]	22Ω [27Ω]	-
	3	1.15 / 99 (11.6Ω)	43Ω [43Ω]	27Ω [33Ω]	15Ω [22Ω]

Pin Configuration



* Internal Pull-Up Resistor
** Internal Pull-Down Resistor
32-Pin MLF

Functionality Table

FS_LC (B0b2)	FS_LB (B0b1)	FS_LA (B0b0)	CPU MHz	PCIEX MHz	SATA MHz	DOT96 MHz
0	0	1	133.33	100.00	100.00	96.00
1	0	1	100.00	100.00	100.00	96.00

CPU/PCIEX PLL Spread Frequency Selection Table

FS_LC (B0b2)	FS_LB (B0b1)	FS_LA (B0b0)	CPU MHz	PCIEX MHz	SATA MHz	Spread % (B0b5=1)
0	0	1	133.33	100.00	100.00	0.5% Down
1	0	1	100.00	100.00	100.00	0.5% Down

Power Management Table

PD#	SMBus Register OE	CPUT/C	PCIEXT/C	DOT96T/C	SATAT/C	48M	REF
1	Enable	Running	Running	Running	Running	Running	Running
0	Enable	Low	Low	Low	Low	Low	Low
1	**Disable**	Low	Low	Low	Low	Low	Low

9LRS4206 Power Distribution Table

VDD Pin#	GND Pin#	Description
1	5	CPU PLL digital
3	5	48MHz output
9	13	SATACLK output
12	5	Fix PLL analog
16	17	CPU PLL core; PCIEX output; CPU PLL analog
19	22	CPUCLK output
25	28	Fix PLL digital; REF output
30	32	Fix PLL core

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	VTTPWRG/PD#	IN	This active high 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled / Asynchronous active low input pin that is used to power down the device into low power state.
3	VDD96	PWR	Power supply for DOT96 outputs.
4	USB48M/FSLA	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values / Fixed 3.3V 48MHz USB clock output.
5	GND96	PWR	Ground pin for DOT96 outputs.
6	DOT96T_LR	OUT	True clock of DOT 96MHz low power differential output pair with integrated 33ohm series resistor and no 50ohm to GND needed
7	DOT96C_LR	OUT	Complement clock of DOT 96MHz low power differential output pair with integrated 33ohm series resistor and no 50ohm to GND needed
8	FSLB	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
9	VDDSATA	PWR	Power supply for SATA clocks, nominal 3.3V
10	SATAT_LR	OUT	True clock of 0.8V push-pull differential SATA pair with integrated 33ohm series resistor and no 50ohm to GND needed
11	SATAC_LR	OUT	Complement clock of 0.8V push-pull differential SATA pair with integrated 33ohm series resistor and no 50ohm to GND needed
12	VDDA_FIX	PWR	Power supply for FIX PLL Analog, nominal 3.3V.
13	GNDPCIEX	PWR	Ground pin for PCIEX outputs.
14	PCIEXC_LR	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor and no 50ohm to GND needed
15	PCIEXT_LR	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor and no 50ohm to GND needed
16	VDDA	PWR	3.3V power for the PLL core.
17	AGND	PWR	Ground pin for the PLL core.
18	RESET_IN#/RESET_OUT#*	I/O	Real time active low input. When active, SMBus is reset to power up default / Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
19	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
20	CPUC_LR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor and no 50ohm to GND needed
21	CPUT_LR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor and no 50ohm to GND needed
22	GNDCPU	PWR	Ground pin for CPU outputs.
23	SCLK	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
24	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
25	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
26	X2	OUT	Crystal output, Nominally 14.318MHz
27	X1	IN	Crystal input, Nominally 14.318MHz.
28	GNDREF	PWR	Ground for REF outputs.
29	REF/FSLC	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
30	VDD	PWR	Power supply, nominal 3.3V
31	RLATCH**	IN	Asynchronous input pin used in combination with VTTPWRGD signal to determine whether to reset SMBus.
32	GND	PWR	Ground pin.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9LRS4206. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Core/Logic Supply		4.6	V	1,2
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs		4.6	V	1,2,3
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5		V	1,2
Storage Temperature	Ts	-	-65	150	°C	1,2
Case Temperature	Tcase	-		115	°C	1,2
Input ESD protection	ESD prot	Human Body Model	2000		V	1,2

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.
[2] Operation under these conditions is neither implied, nor guaranteed.
[3] Maximum input voltage is not to exceed maximum VDD

Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	
Input High Voltage	V_{IHSE}	Single-ended inputs	2	V_{DD} + 0.3	V	1,4
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3	0.8	V	1,4
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7	VDD+0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1,3
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1,2
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1,2
Operating Supply Current	$I_{DDOP3.3}$	Full Active, C_L = Full load; IDD 3.3V		125	mA	1
Powerdown Current	$I_{DDPD3.3}$	Power down mode, 3.3V Rail		5	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		15	MHz	1
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
	C_{INX}	X1 & X2 pins		6	pF	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.
[2] Signal is required to be monotonic in this region.
[3] Input leakage current does not include inputs with pull-up or pull-down resistors
[4] 3.3V referenced inputs are: RESET_IN, RLATCH, SCLK, SDATA, VTTWRGD inputs if selected.

Electrical Characteristics–SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		100	kHz	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics–Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_PD#	T_{DRPD}	Differential output enable after PD# de-assertion		300	us	1
Tfall_PD#	T_{FALL}	Fall/Rise time of PD# input		5	ns	1
Trise_PD#	T_{RISE}			5	ns	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics–Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	4	V/ns	1,3,4
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	4	V/ns	1,3,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1,2,7
Differential Voltage Swing	V_{SWING}	Single-ended Measurement			mV	1,3
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,2,5,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,2,5,10
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1,2,8
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1,2,9
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] Measurement taken for single ended waveform on a component test board (not in system)

[3] Measurement taken from differential waveform on a component test board. (not in system)

[4] Slew rate emastured through V_swing voltage range centered about differential zero

[5] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[6] Only applies to the differential rising edge (Clock rising, Clock# falling)

[7] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage

[8] The max voltage including overshoot.

[9] The min voltage including undershoot.

[10] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute.

Electrical Characteristics–USB48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,2,6
Clock period	T_{period}	48.00MHz output nominal	20.83125	20.83542	ns	1,4,5
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.48130	21.18540	ns	1,4
CLK High Time	T_{HIGH}		8.216563	11.152	ns	1
CLK Low time	T_{LOW}		7.816563	10.952	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	1
		V_{OH}@MAX = 3.135 V		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	1
		V_{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	2	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	2	V/ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		350	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Peroid and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurment interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz and 48.000000MHz

Electrical Characteristics–REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,2,6
Clock period	T_{period}	14.318MHz output nominal	69.8203	69.8622	ns	1,4,5
Absolute min/max period	T_{abs}	14.318MHz output nominal	69.8203	70.86224	ns	1,4
CLK High Time	T_{HIGH}		29.97543	38.46654	ns	1
CLK Low time	T_{LOW}		29.57543	38.26654	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-33	-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	30	38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1,3
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1,3
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1,4
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V		1000	ps	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=33ohm, CL=5pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]Edge rate in system is measured from 0.8V to 2.0V.

[4] Duty cycle, Peroid and Jitter are measured with respect to 1.5V

[5] The average period over any 1us period of time

[6] Using frequency counter with the measurement interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz and 48.000000MHz

Clock Jitter Specifications - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1,2
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1,2,3
SATA Jitter - Cycle to Cycle	$SATAJ_{C2C}$	Differential Measurement		125	ps	1,2
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1,2
SRC Phase Jitter	$t_{jphasePLL}$	PCIe Gen 1		86	ps (p-p)	1,2
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz		3.0	ps (RMS)	1,4
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		3.1	ps (RMS)	1,4

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=0ohm, CL=2pF

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2] JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded.

[3] Phase jitter requirement: The deisgnated Gen2 outputs will meet the reference clock jitter requiremernts from the PCI Express Gen2 Base Spec. The test is performed on a componnet test board under quiet conditttions with all outputs on.

[4] See http://www.pcisig.com for complete specs

General SMBus Serial Interface Information for the 9LRS4206

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D3_{(H)}$	$D2_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I2C Table: Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	PWD
Bit 7	ROD	Reset on Demand	RW	Disable	Enable	0
Bit 6	Reserved	Reserved	RW	-	-	1
Bit 5	SS_EN	CPU/PCIEX PLL Spread Enable	RW	OFF	ON	1
Bit 4	Reserved	Reserved	RW	-	-	1
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	FSLC	Freq Select Bit 2	RW	See Table 1: CPU/PCIEX PLL Frequency Selection Table		Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

I2C Table: Output Control Register

Byte 1	Name	Control Function	Type	0	1	PWD
Bit 7	DOT96T/C	Output Control	RW	Disable	Enable	1
Bit 6	Reserved	Reserved	RW	-	-	1
Bit 5	RLATCH	RLATCH pin enable bit (Enables pin to be active)	RW	Disable	Enable	1
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	RESET_IN_EN	RESET_IN Enable	RW	Disable	Enable	0
Bit 2	REF Strength	REF Strength Programming	RW	1X	2X	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	CPU/PCIEX PLL MNEN	CPU/PCIEX PLL M/N Enable	RW	Disable	Enable	0

I2C Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD
Bit 7	USB48M	Output Control	RW	Disable	Enable	1
Bit 6	Reserved	Reserved	RW	-	-	1
Bit 5	Reserved	Reserved	RW	-	-	1
Bit 4	Reserved	Reserved	RW	-	-	1
Bit 3	Reserved	Reserved	RW	-	-	1
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	1
Bit 6	Reserved	Reserved	RW	-	-	1
Bit 5	PCIEXT/C	Output Control	RW	Disable	Enable	1
Bit 4	Reserved	Reserved	RW	-	-	1
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	SATAT/C	Output Control	RW	Disable	Enable	1
Bit 0	Reserved	Reserved	RW	-	-	1

I2C Table: Output Control Register

Byte 4	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	1
Bit 6	REF	Output Control	RW	Disable	Enable	1
Bit 5	Reserved	Reserved	RW	-	-	1
Bit 4	CPUT/C	Output Control	RW	Disable	Enable	1
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	1
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

Byte 5 Reserved Register

I2C Table: Output Control Register

Byte 6	Name	Control Function	Type	0	1	PWD
Bit 7	Diff AMP	CPU Differential output Amplitude	RW	00 = 700mV	01 = 900mV	1
Bit 6	Diff AMP	Control	RW	10 = 800mV	11 = 1000mV	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Diff AMP	DOT96 Differential output Amplitude	RW	00 = 700mV	01 = 900mV	1
Bit 2	Diff AMP	Control	RW	10 = 800mV	11 = 1000mV	0
Bit 1	Reserved	Reserved	RW	-	-	1
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD
Bit 7	RID3	Revision ID	R	-	-	0
Bit 6	RID2		R	-	-	0
Bit 5	RID1		R	-	-	0
Bit 4	RID0		R	-	-	0
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	001 = ICS	-	0
Bit 0	VID0		R	-	-	1

I2C Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	PWD
Bit 7	BC7	Byte Count Programming b(7:0)	R	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	BC6		R			0
Bit 5	BC5		R			0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

I2C Table: Watch Dog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	PWD
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 5	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 4	HWD3	WD Hard Alarm Timer Bit 3	RW	These bits represent X*290ms or X*1.16s. The watchdog timer waits before it goes to alarm mode. Default is 15 X 290ms = 4.35s.		1
Bit 3	HWD2	WD Hard Alarm Timer Bit 2	RW			1
Bit 2	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 1	HWD0	WD Hard Alarm Timer Bit 0	RW			1
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: Output Control Register

Byte 10	Name	Control Function	Type	0	1	PWD
Bit 7	Diff AMP	PCIEX Differential output Amplitude	RW	00 = 700mV	01 = 900mV	1
Bit 6	Diff AMP	Control	RW	10 = 800mV	11 = 1000mV	0
Bit 5	Diff AMP	SATACLK Differential output Amplitude	RW	00 = 700mV	01 = 900mV	1
Bit 4	Diff AMP	Control	RW	10 = 800mV	11 = 1000mV	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

Byte 11 Reserved Register

I2C Table: CPU/PCIEX PLL Frequency Control Register

Byte 12	Name	Control Function	Type	0	1	PWD
Bit 7	N Div8	N Divider Programming:	RW	The decimal representation of N Divider in Byte12 will configure the CPU/PCIEX PLL VCO frequency. Default at power up = latch-in or Byte 0 ROM table.		X
Bit 6	N Div7		RW			X
Bit 5	N Div6		RW			X
Bit 4	N Div5		RW			X
Bit 3	N Div4		RW			X
Bit 2	N Div3		RW			X
Bit 1	N Div2		RW			X
Bit 0	N Div1		RW			X

Byte 13 ~ 19 Reserved Registers

I2C Table: Output Control Register

Byte 20	Name	Control Function	Type	0	1	PWD
Bit 7	48MHz Strength	48MHz Strength Control	RW	1X	2X	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	SKIP_ORT	Skip ORT during CPU/SRC PLL M/N Programming	RW	ORT Enabled	ORT Disabled	0
Bit 1	Reserved	Reserved	RW	-	-	X
Bit 0	Reserved	Reserved	RW	-	-	X

I2C Table: Output Control Register

Byte 21	Name	Control Function	Type	0	1	PWD
Bit 7	USB48M	Slew Rate Control	RW	00 = 1.2V/ns	01 = 1.6V/ns	0
Bit 6	USB48M		RW	10 = 2.0V/ns	11 = 2.4V/ns	1
Bit 5	REF	Slew Rate Control	RW	00 = 1.2V/ns	01 = 1.6V/ns	1
Bit 4	REF		RW	10 = 2.0V/ns	11 = 2.4V/ns	1
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	1
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: Synchronization Control Register

Byte 22	Name	Control Function		0	1	PWD
Bit 7	SATA_SSEL	SATACLK Source Select	RW	CPU PLL	FIX PLL	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

Byte 23 ~ 27 Reserved Registers

I2C Table: CPU Output Divider Register

Byte 28	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	X
Bit 6	Reserved	Reserved	RW	-	-	X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	CPUDiv2	CPU Divider Ratio Programming Bits for CPU PLL	RW	000:/2	011:/6	X
Bit 1	CPUDiv1		RW	001:/3	100:/8	X
Bit 0	CPUDiv0		RW	010:/4	101:/12	X

I2C Table: PCIEX Output Divider Register

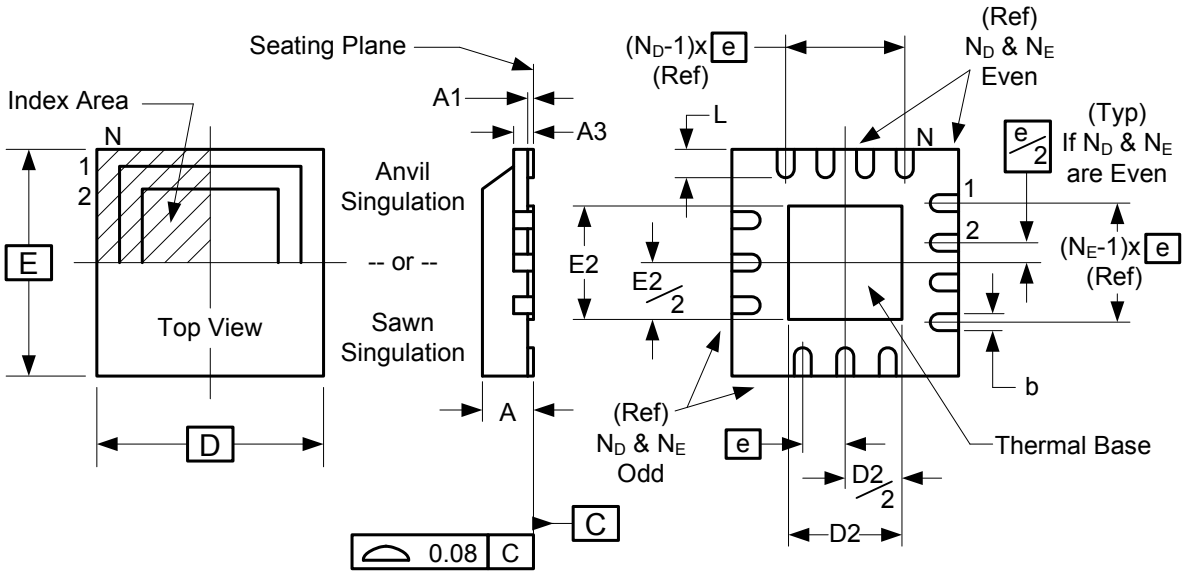
Byte 29	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved	Reserved	RW	-	-	X
Bit 6	Reserved	Reserved	RW	-	-	X
Bit 5	Reserved	Reserved	RW	-	-	X
Bit 4	Reserved	Reserved	RW	-	-	X
Bit 3	Reserved	Reserved	RW	-	-	X
Bit 2	PCIEXDiv2	PCIEX Divider Ratio Programming Bits for PCIEX PLL	RW	000:/4	010:/8	X
Bit 1	PCIEXDiv1		RW	001:/5	011:/10	X
Bit 0	PCIEXDiv0		RW	-	-	X

Marking Diagram

Notes:

1. Due to the package size constrtaints, actual top-side marking may differ from full orderable part number.
2. ###### is the lot number.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. “L” denotes RoHS compliant package.

Package Outline and Package Dimensions (32-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	5.00 x 5.00	
D2 MIN./MAX.	3.0	3.3
E2 MIN./MAX.	3.0	3.3
L MIN./MAX.	0.3	0.5
N	32	
N_D	8	
N_E	8	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9LRS4206AKLF	see page 13	Tubes	32-pin MLF	0 to +70° C
9LRS4206AKLFT		Tape and Reel	32-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Originator	Date	Description of Change
0.1	D.Chan	10/04/10	Initial release.
A	RDW	01/28/14	Moved to final per characterization data.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.