

PMIC for Applications Requiring up to 6 A

General Description

DA9061 is a power management integrated circuit (PMIC) optimized for supplying systems with single- and dual-core processors, I/O, DDR memory, and peripherals. It targets mobile device, medical equipment, IVI systems, and FPGA based applications.

DA9061 features three buck converters providing a total current of 6 A. High efficiency is achieved over a wide load range with PFM mode available for low power or sleep modes. All power switches are integrated, therefore, external Schottky diodes are not required. Furthermore, low-profile inductors can be used with DA9061. The four LDO regulators with programmable output voltage provide up to 300 mA.

Dynamic voltage control (DVC) allows dynamic control of DA9061 supply voltages according to the operating point of the system. It is controlled by writing directly to the registers using the I²C compatible 2-wire interface or the GPIOs.

DA9061 features a programmable power sequencer that handles start-up and shutdown sequences. Power mode transitions can be triggered with software control, GPIOs, or with the on-key. Several types of on-key presses can be detected to trigger different power mode transitions.

An integrated watchdog timer monitors the system.

Five GPIOs are able to perform system functions, including: keypad supervision, application buck, and timing-controlled external regulators/power switches or other ICs.

DA9061 is also available as an automotive AEC-Q100 Grade 2 version.

Key Features

- Input voltage 2.8 V to 5.5 V
- Three buck converters with dynamic voltage control:
 - Buck1: 0.3 V to 1.57 V, 2.5 A
 - Buck2: 0.8 V to 3.34 V, 2 A
 - Buck3: 0.53 V to 1.8 V, 1.5 A
 - 3 MHz switching frequency (enables low profile inductors)
- Four LDO regulators:
 - LDO1: 0.9 V to 3.6 V, 100 mA
 - LDO2, LDO3, LDO4: 0.9 V to 3.6 V, 300 mA
- Programmable power mode sequencer
- System supply and junction temperature monitoring
- Watchdog timer
- Five GPIOs
- -40 °C to +125 °C junction temperature range
- 40-pin QFN, 6 mm × 6 mm package, 0.5 mm pitch
- Automotive AEC-Q100 Grade 2 version available

Applications

- Single and dual core application processors such as ARM Cortex or i.MX6 series
- Entry-level FPGAs
- Automotive infotainment
- Portable industrial and medical devices
- e-book readers

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Block Diagram

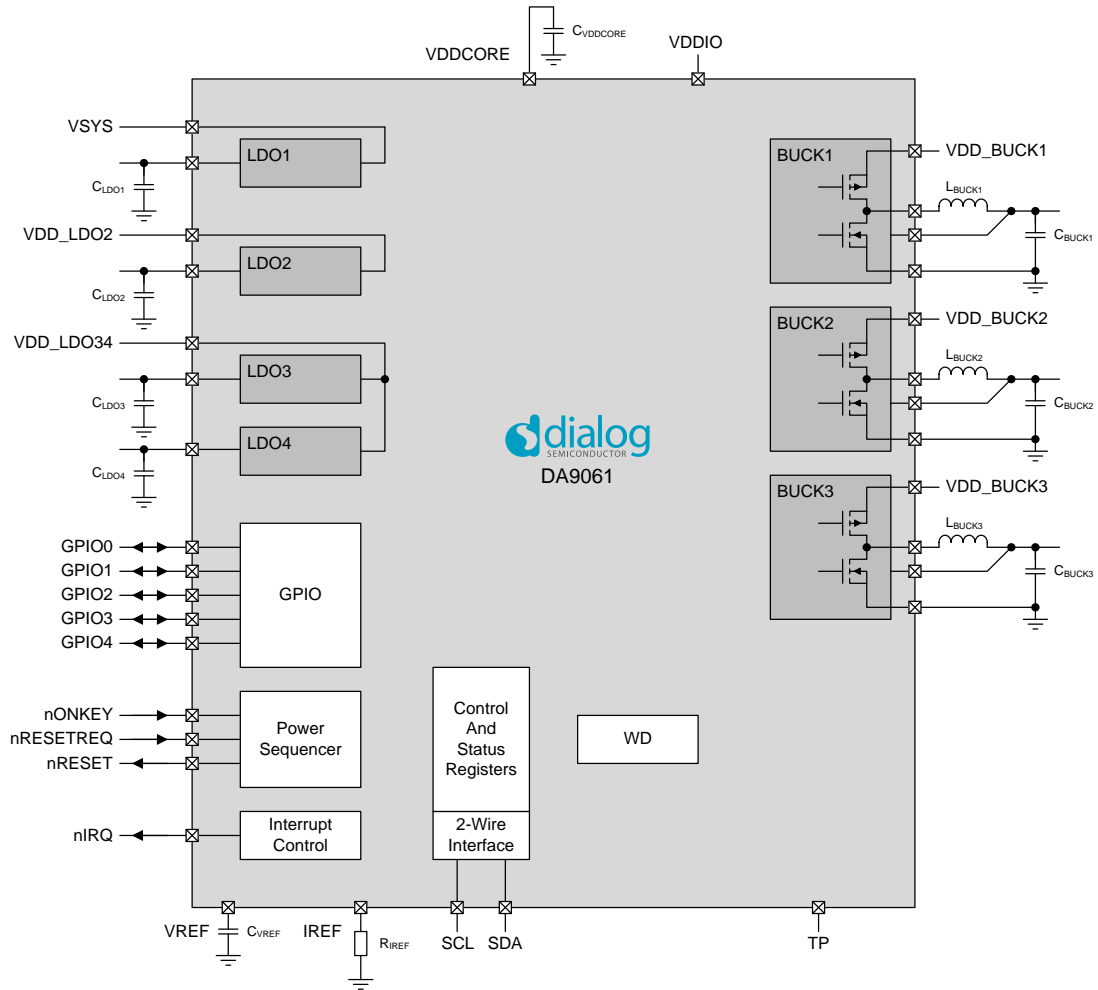


Figure 1: DA9061 Block Diagram

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1 Package Information

1.1 Pin List

Table 1: Pin Description

| Pin No. | Pin Name | Type Table 2 | Description |
|---------|-----------|-----------------|--|
| Paddle | GND | GND | Power grounds of the bucks, digital ground |
| 1 | VLDO1 | AO | LDO1 output voltage |
| 2 | VLDO2 | AO | LDO2 output voltage |
| 3 | VDD_LDO2 | PS | LDO2 supply |
| 4 | IREF | AO | Reference current |
| 5 | VREF | AIO | Reference voltage |
| 6 | NC | | Connect to GND |
| 7 | VSS_ANA | GND | Analog ground |
| 8 | NC | | Connect to GND |
| 9 | VLDO3 | AO | LDO3 output voltage |
| 10 | VDD_LDO34 | PS | LDO3 and LDO4 supply |
| 11 | VLDO4 | AO | LDO4 output voltage |
| 12 | NC | | Do not use. Leave floating |
| 13 | SDA | DIO | Data signal of the 2-wire interface |
| 14 | SCL | DI | Clock signal of the 2-wire interface |
| 15 | nONKEY | DI | Input for power-on key |
| 16 | nRESETREQ | DI | Reset request input |
| 17 | VLX_BUCK3 | AO | Switching node of Buck3 |
| 18 | VDD_BUCK3 | PS | Buck3 supply |
| 19 | VDD_BUCK2 | PS | Buck2 supply |
| 20 | VLX_BUCK2 | AO | Switching node of Buck2 |
| 21 | GPIO0 | DIO | General purpose I/O, WDKICK |
| 22 | GPIO1 | DIO | General purpose I/O |
| 23 | VDDIO | PS | IO supply |
| 24 | VBUCK3 | AI | Voltage feedback of Buck3 |
| 25 | VBUCK2 | AI | Voltage feedback of Buck2 |
| 26 | VBUCK1 | AI | Voltage feedback of Buck1 |
| 27 | NC | | Do not use. Leave floating |
| 28 | GPIO2 | DIO | General purpose I/O, PWR_EN |
| 29 | GPIO3 | DIO | General purpose I/O |
| 30 | GPIO4 | DIO | General purpose I/O, SYS_EN |
| 31 | VLX_BUCK1 | AO | Switching node of Buck1 |
| 32 | VDD_BUCK1 | PS | Buck1 supply |
| 33 | NC | | Connect to GND |

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| Pin No. | Pin Name | Type Table 2 | Description |
|---------|----------|-----------------|------------------------------------|
| 34 | NC | | Do not use. Leave floating |
| 35 | NC | | Do not use. Leave floating |
| 36 | TP | DIO | Test pin |
| 37 | nIRQ | DO | Interrupt signal to host processor |
| 38 | nRESET | DO | Reset output |
| 39 | VDDCORE | AO | Internal supply |
| 40 | VSYS | PS | System supply, LDO1 supply |

Table 2: Pin Type Definition

| Pin type | Description | Pin type | Description |
|----------|----------------------|----------|---------------------|
| DI | Digital Input | AI | Analog Input |
| DO | Digital Output | AO | Analog Output |
| DIO | Digital Input/Output | AIO | Analog Input/Output |
| PS | Power Supply | GND | Ground connection |

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1.2 Package Outline Drawing

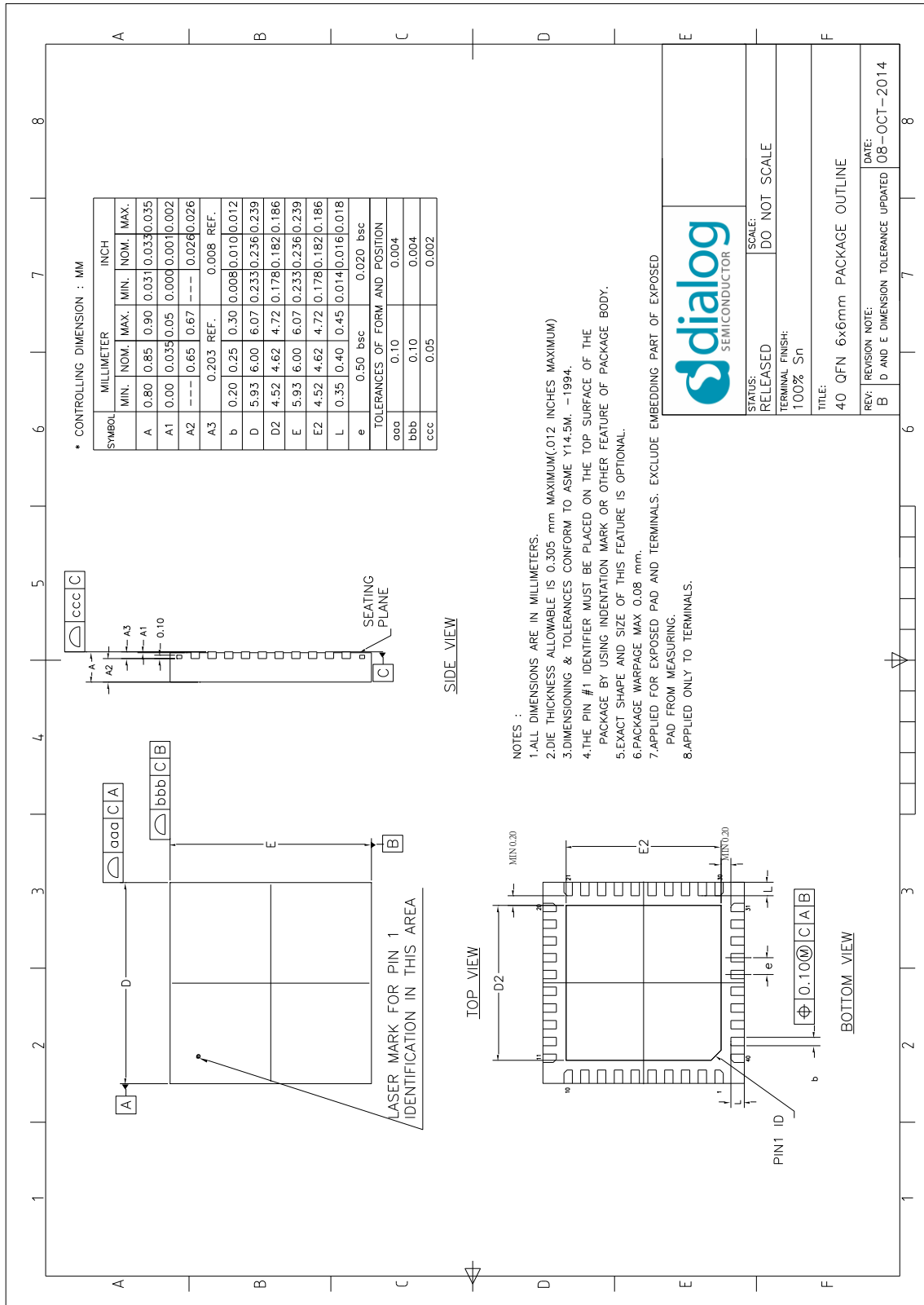


Figure 2: DA9061 Package Outline Drawing

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2 Regulator Overview

Table 3: Regulators

| Regulator | Supplied Pins | Supplied Voltage (V) | Supplied Maximum Current (mA) | External Component | Notes |
|-----------|---------------|----------------------|--------------------------------|---------------------------------------|---|
| Buck1 | VBUCK1 | 0.3 to 1.57 | 2500 Note 1 | 1.0 μ H, 44 μ F/88 μ F | <ul style="list-style-type: none"> GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5, 1.0, 2.0, 4.0] μs) 10 mV steps < 0.7 V PFM mode only |
| Buck2 | VBUCK2 | 0.8 to 3.34 | 2000 Note 2 | 1.0 μ H, 44 μ F/88 μ F | <ul style="list-style-type: none"> GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5, 1.0, 2.0, 4.0] μs) 20 mV steps |
| Buck3 | VBUCK3 | 0.53 to 1.8 | 1500 Note 2 | 1.0 μ H, 44 μ F | <ul style="list-style-type: none"> GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5, 1.0, 2.0, 4.0] μs) 10 mV steps < 0.7 V PFM mode only |
| LDO1 | VLDO1 | 0.9 to 3.6 | 100 | 1.0 μ F | <ul style="list-style-type: none"> Configurable as always-on 50 mV steps Internally supplied from VSYS |
| LDO2 | VLDO2 | 0.9 to 3.6 | 300 | 2.2 μ F | <ul style="list-style-type: none"> Low noise LDO 50 mV steps |
| LDO3 | VLDO3 | 0.9 to 3.6 | 300 | 2.2 μ F | <ul style="list-style-type: none"> Low noise LDO 50 mV steps Common supply with LDO4 |
| LDO4 | VLDO4 | 0.9 to 3.6 | 300 | 2.2 μ F | <ul style="list-style-type: none"> Low noise LDO 50 mV steps Common supply with LDO3 |

Note 1 For short durations, to meet peak current requirements, I_{OUT} for Buck1 can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

Note 2 For short durations, to meet peak current requirements, I_{OUT} for Buck2 and Buck3 can be operated at up to 10 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

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3 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings of the device. Exceeding these ratings may cause permanent damage to the device. Device functionality is only guaranteed under the conditions listed in Sections 4 and 5. Operating the device in conditions exceeding those listed in Sections 4 and 5, but compliant with the absolute maximum ratings listed in Table 4, for extended periods of time may affect device reliability.

Table 4: Absolute Maximum Ratings

| Parameter | Symbol | Note | Min | Typ | Max | Unit |
|----------------------|----------------------|----------------|------|-----|----------------------------------|------|
| Storage temperature | | | -65 | | +150 | °C |
| Junction temperature | T _J | | -40 | | +150 Note 1 | °C |
| Supply voltage | V _{sys} | | -0.3 | | 6.0 | V |
| | V _{BBAT} | | -0.3 | | 3.2 | V |
| | Buck V _{DD} | | -0.3 | | V _{sys} + 0.4 Note 2 | V |
| | V _{TP} | | -0.3 | | 8.0 Note 3 | V |
| | All other pins | | -0.3 | | V _{sys} + 0.3 Note 2 | V |
| ESD protection HBM | V _{ESD_HBM} | | 2000 | | | V |
| ESD protection CDM | V _{ESD_CDM} | Corner pins | 750 | | | V |
| | | All other pins | 500 | | | |

Note 1 See Sections 5.8 and 7.10 for more detail.

Note 2 Voltage must not exceed 5.5 V.

Note 3 Voltage on TP pin should be 0 V except during in-circuit programming.

PMIC for Applications Requiring up to 6 A**4 Recommended Operating Conditions****Table 5: Recommended Operating Conditions**

| Parameter | Symbol | Note | Min | Typ | Max | Unit |
|--------------------------------|----------------|--------|------|-----|------|------|
| Operating junction temperature | T_J | | -40 | | +125 | °C |
| Main supply | V_{SYS} | | 0 | | 5.5 | V |
| Backup supply | V_{BBAT} | | 0 | | 3.15 | V |
| I/O supply | V_{DDIO} | Note 1 | 1.2 | | 3.6 | V |
| TP programming supply | V_{TP_PROG} | Note 2 | 7.25 | 7.5 | 7.75 | V |

Note 1 V_{DDIO} must not exceed V_{SYS} .

Note 2 Voltage on TP pin should be 0 V except during in-circuit programming.

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4.1 Thermal Characteristics

Table 6: QFN Package Ratings

| Parameter | Symbol | Note | Typ | Unit |
|--|-------------------|--|-------|------|
| Thermal resistance junction to ambient | $R_{\theta_{JA}}$ | Note 1 | 20.81 | °C/W |
| Thermal resistance junction to Board | $R_{\theta_{JB}}$ | Note 1 | 5.9 | °C/W |
| Thermal resistance junction to case | $R_{\theta_{JC}}$ | Note 1 | 18.72 | °C/W |
| Maximum power dissipation Note 1 | P_{DISS} | Derating factor above $T_A = 70\text{ °C}$: 48.05 mW/°C | 3120 | mW |

Note 1 Obtained from package thermal simulation, 76 mm x 114 mm x 1.6 mm (JEDEC), 6-layer board, 70 μm thick copper top/bottom layers, 35 μm thick copper inside layers, 49 x 0.2 mm thermal vias beneath the device, natural convection (still air).

4.1.1 Power Derating Curves

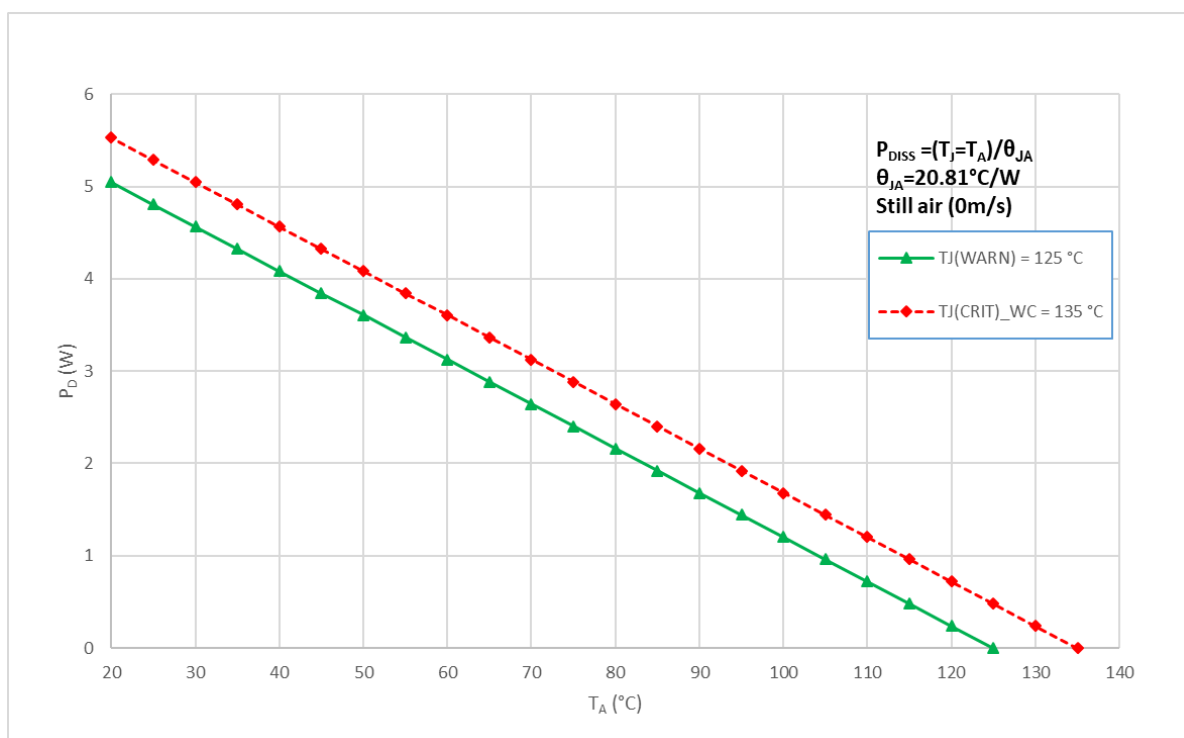


Figure 3: QFN40 Power Derating Curve

Table 7: Typical Temperatures

| | $T_A = 70\text{ °C}$ | $T_A = 85\text{ °C}$ | $T_A = 105\text{ °C}$ |
|-------------------|-----------------------|-----------------------|-----------------------|
| T_{WARN} | $P_D = 3.12\text{ W}$ | $P_D = 1.92\text{ W}$ | $P_D = 0.96\text{ W}$ |
| T_{CRIT} | $P_D = 2.64\text{ W}$ | $P_D = 2.40\text{ W}$ | $P_D = 1.44\text{ W}$ |

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5 Electrical Characteristics

5.1 Digital I/O

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{SYS} = 2.8\text{ V}$ to 5.5 V .

Table 8: Digital I/O Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|----------|--|------------------|-----|------------------|------------|
| Input high voltage (GPIO to GPI4, nRESETREQ) | V_{IH} | VDDCORE mode | 1.0 | | V_{SYS} | V |
| | | VDDIO mode | $0.7 * V_{DDIO}$ | | V_{SYS} | |
| Input low voltage (GPIO to GPI4, nRESETREQ) | V_{IL} | VDDCORE mode | -0.3 | | 0.4 | V |
| | | VDDIO mode $V_{DDIO} \geq 1.5\text{ V}$ | -0.3 | | $0.3 * V_{DDIO}$ | |
| Input high voltage (nONKEY) | V_{IH} | | 1.0 | | V_{SYS} | V |
| Input low voltage (nONKEY) | V_{IL} | | -0.3 | | 0.4 | V |
| Input high voltage (SCL, SDA) | V_{IH} | VDDCORE mode | 1.0 | | V_{SYS} | V |
| | | VDDIO mode | $0.7 * V_{DDIO}$ | | V_{SYS} | |
| Input low voltage (SCL, SDA) | V_{IL} | VDDCORE mode | -0.3 | | 0.4 | V |
| | | VDDIO mode $V_{DDIO} \geq 1.5\text{ V}$ | -0.3 | | $0.3 * V_{DDIO}$ | |
| Output high voltage (GPIO0 to GPIO4, nRESET, nIRQ) | V_{OH} | $I_{OUT} = 1\text{ mA}$ Push-pull mode | $0.7 * V_{DDIO}$ | | | V |
| Output low voltage (GPIO0 to GPIO4, nRESET, nIRQ) | V_{OL} | $I_{OUT} = 1\text{ mA}$ | | | 0.3 | V |
| Output low voltage (SDA) | V_{OL} | $I_{OUT} = 8\text{ mA}$ | | | 0.4 | V |
| | | $I_{OUT} = 3\text{ mA}$ | | | 0.4 | |
| Source current capability (GPIO0 to GPIO4) | I_{OH} | $V_{OUT} = 0.7 * V_{DDIO}$ $V_{DDIO} \geq 1.8\text{ V}$ | | -1 | | mA |
| Sink current capability (GPIO0 to GPIO4) | I_{OL} | $V_{OUT} = 0.3\text{ V}$ | | 1 | | mA |
| Input capacitance (SCL, SDA) | C_{IN} | | | | 10 | pF |
| Pull-down resistance (GPIO0 to GPIO4) | R_{PD} | | 50 | 100 | 250 | k Ω |
| Pull-up resistance (GPIO0 to GPIO4) | R_{PU} | $V_{DDIO} = 1.5\text{ V}$ | 60 | 180 | 310 | k Ω |
| | | $V_{DDIO} = 1.8\text{ V}$ | 45 | 120 | 190 | |
| | | $V_{DDIO} = 3.3\text{ V}$ | 20 | 40 | 60 | |

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5.2 Watchdog

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{SYS} = 2.8\text{ V}$ to 5.5 V .

Table 9: Watchdog Electrical Characteristics

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|-------------------------------|-----------------|----------------------------|-----|-----|-----|---------------|
| Minimum watchdog time | t_{WDMIN} | Internal 25 kHz oscillator | | | 200 | ms |
| Maximum watchdog time | t_{WDMAX} | Internal 25 kHz oscillator | 2.5 | | | s |
| Minimum assert time of WDKICK | $t_{WDKICKMIN}$ | | | 150 | | μs |

5.3 2-Wire Interface

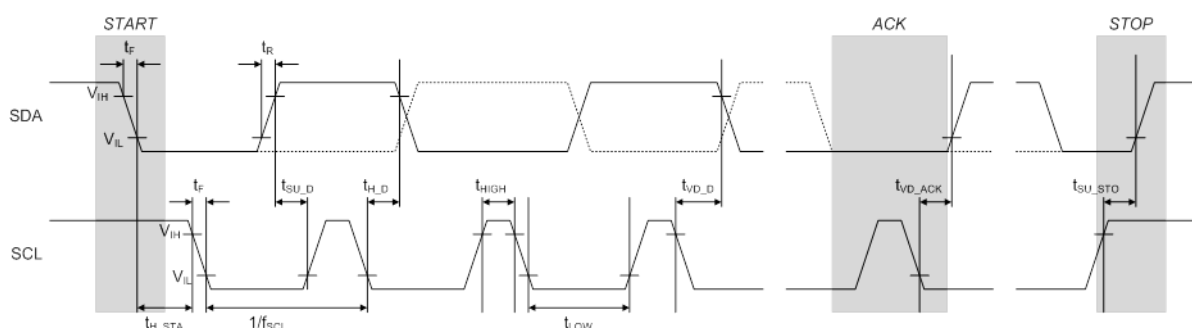


Figure 4: 2-Wire Interface Timing

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{SYS} = 2.8\text{ V}$ to 5.5 V .

Table 10: 2-Wire Interface Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|---------------|--|-----|-----|------|---------------|
| Bus free time STOP to START | t_{BUF} | | 0.5 | | | μs |
| Bus line capacitive load | C_B | | | | 150 | pF |
| Standard/Fast/Fast+ Mode | | | | | | |
| SCL clock frequency | f_{SCL} | $V_{DDIO} \geq 1.5\text{ V}$ Note 1 | 0 | | 1.0 | MHz |
| Start condition set-up time | t_{SU_STA} | | 260 | | | ns |
| Start condition hold time | t_{H_STA} | | 260 | | | ns |
| SCL low time | t_{W_CL} | | 500 | | | ns |
| SCL high time | t_{W_CH} | | 260 | | | ns |
| 2-wire SCL and SDA rise time | t_R | (input requirement) | | | 1000 | ns |
| 2-wire SCL and SDA fall time | t_F | (input requirement) | | | 300 | ns |
| Data set-up time | t_{SU_D} | | 50 | | | ns |
| Data hold-time | t_{H_D} | | 0 | | | ns |
| Data valid time | t_{VD_D} | | | | 450 | ns |
| Data valid time acknowledge | t_{VD_ACK} | | | | 450 | ns |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|---------------------|--|-----|-----|-----|------|
| Stop condition set-up time | t _{SU_STO} | | 260 | | | ns |
| High Speed Mode | | | | | | |
| SCL clock frequency | f _{SCL} | V _{DDIO} ≥ 1.8 V Note 1 | 0 | | 3.4 | MHz |
| Start condition set-up time | t _{SU_STA} | | 160 | | | ns |
| Start condition hold time | t _{H_STA} | | 160 | | | ns |
| SCL low time | t _{W_CL} | | 160 | | | ns |
| SCL high time | t _{W_CH} | | 60 | | | ns |
| 2-wire SCL and SDA rise time | t _R | (input requirement) | | | 160 | ns |
| 2-wire SCL and SDA fall time | t _F | (input requirement) | | | 160 | ns |
| Data set-up time | t _{SU_D} | | 10 | | | ns |
| Data hold-time | t _{H_D} | | 0 | | | ns |
| Stop condition set-up time | t _{SU_STO} | | 160 | | | ns |

Note 1 Minimum clock frequency is 10 kHz if TWOWIRE_TO is enabled.

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5.4 LDOs

5.4.1 LDO1

Unless otherwise noted, the following is valid for $T_J = -40\text{ °C}$ to $+125\text{ °C}$.

Table 11: LDO1 Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-----------------|---|------|-------------------------|------|-------------------|
| Input voltage | V_{DD} | $V_{DD} = V_{SYS}$ (Internally connected) | 2.8 | | 5.5 | V |
| Maximum output current | I_{OUT_MAX} | | 100 | | | mA |
| Output voltage | V_{LDO} | Programmable in 50 mV steps | 0.9 | | 3.6 | V |
| Output accuracy | | $I_{OUT} = I_{OUT_MAX}$ including static line/load regulation | -3% | | +3% | |
| Stabilization capacitor | C_{OUT} | Including voltage and temperature coefficient | -55% | 1.0 | +35% | μF |
| Output capacitor ESR | R_{COUT_ESR} | $f > 1\text{ MHz}$ Including wiring parasitics | 0 | | 300 | $\text{m}\Omega$ |
| Short circuit current | I_{SHORT} | | | 200 | | mA |
| Dropout voltage | $V_{DROPOUT}$ | $V_{LDO} = 3.3\text{ V}$ $I_{OUT} = I_{OUT_MAX}$ | | 100 | 150 | mV |
| Static line regulation | V_{S_LINE} | $V_{DD} = 3.0\text{ V}$ to 5.5 V $I_{OUT} = I_{OUT_MAX}$ | | 5 | 20 | mV |
| Static load regulation | V_{S_LOAD} | $I_{OUT} = 1\text{ mA}$ to I_{OUT_MAX} | | 5 | 20 | mV |
| Line transient response | V_{TR_LINE} | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{OUT_MAX}$ $t_R = t_F = 10\ \mu\text{s}$ | | 5 | 20 | mV |
| Load transient response | V_{TR_LOAD} | $V_{DD} = 3.6\text{ V}$, $V_{LDO} = 3.3\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{OUT_MAX} $t_R = t_F = 1\ \mu\text{s}$ | | 30 | 50 | mV |
| Power supply rejection ratio | PSRR | $V_{DD} = 3.6\text{ V}$ $V_{DD} - V_{LDO} \geq 0.6\text{ V}$ $I_{OUT} = I_{OUT_MAX}/2$ $f = f_{VDD_LDO}$ | | | | |
| | | $f = 10\text{ Hz}$ to 10 kHz | 40 | 60 | | dB |
| Output noise | N | $V_{DD} = 3.6\text{ V}$, $V_{LDO} = 2.8\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{OUT_MAX} $f = 10\text{ Hz}$ to 100 kHz $T_A = 25\text{ °C}$ | | 70 | | $\mu\text{V rms}$ |
| Quiescent current in ON mode | I_{Q_ON} | $T_A = 25\text{ °C}$ | | 9 + 0.9% I_{OUT} | | μA |
| Quiescent current in SLEEP mode | I_{Q_SLEEP} | $T_A = 25\text{ °C}$ | | 1.5 + 1.6% I_{OUT} | | μA |
| Quiescent current in OFF mode | I_{Q_OFF} | $V_{LDO} < 0.5\text{ V}$ $T_A = 25\text{ °C}$ | | | 1 | μA |

PMIC for Applications Requiring up to 6 A

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------|------------------|---|-----|-----|-----|------|
| Turn-on time | t _{ON} | 10 % to 90 % | | | 350 | μs |
| | | SLEEP mode | | | 450 | |
| Turn-off time | t _{OFF} | 90 % to 10% Pull-down enabled | | | 1 | ms |
| Pull-down resistance in OFF mode | R _{OFF} | VLDO = 0.5 V Can be disabled via LDO1_PD_DIS | | 50 | | Ω |

5.4.2 LDO2, LDO3, LDO4

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 °C.

Table 12: LDO2, LDO3, LDO4 Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|-----------------------|---|----------------|----------------|------|------|
| Input voltage | V _{DD} | V _{DD} = V _{SYS} | 2.8 | | 5.5 | V |
| | | Supplied from buck converter | 1.5 | | | |
| Maximum output current | I _{OUT_MAX} | V _{DD} ≥ 1.8 V (I _{OUT} = I _{OUT_MAX} /3, V _{DD} < 1.8 V) | 300 | | | mA |
| Output voltage | V _{LDO} | Programmable in 50 mV steps | 0.9 | | 3.6 | V |
| Output accuracy | | I _{OUT} = I _{OUT_MAX} Including static line/load regulation | -3% | | +3% | |
| Stabilization capacitor | C _{OUT} | Including voltage and temperature coefficient | -55% | 2.2 | +35% | μF |
| Output capacitor ESR | R _{COUT_ESR} | f > 1 MHz Including wiring parasitics | 0 | | 300 | mΩ |
| Short circuit current | I _{SHORT} | | | 600 | | mA |
| Dropout voltage | V _{DROPOUT} | I _{OUT} = I _{OUT_MAX} (V _{DD} < 1.8 V, I _{OUT} = I _{OUT_MAX} /3) Note 1 | | 100 | 150 | mV |
| Static line regulation | V _{S_LINE} | V _{DD} = 3.0 V to 5.5 V I _{OUT} = I _{OUT_MAX} | | 5 | 20 | mV |
| Static load regulation | V _{S_LOAD} | I _{OUT} = 1 mA to I _{OUT_MAX} | | 5 | 20 | mV |
| Line transient response | V _{TR_LINE} | V _{DD} = 3.0 V to 3.6 V I _{OUT} = I _{OUT_MAX} t _r = t _f = 10 μs | | 5 | 20 | mV |
| Load transient response | V _{TR_LOAD} | V _{DD} = 3.6 V, V _{LDO} = 3.3 V I _{OUT} = 1 mA to I _{OUT_MAX} t _r = t _f = 1 μs | | 30 | 50 | mV |
| Power supply rejection ratio | PSRR | V _{DD} = 3.6 V V _{DD} - V _{LDO} ≥ 0.6 V I _{OUT} = I _{OUT_MAX} /2 f = f _{VDD_LDO} | | | | |
| | | f = 10 Hz to 1 kHz f = 1 kHz to 10 kHz f = 10 kHz to 100 kHz | 70 60 40 | 80 70 50 | | dB |

PMIC for Applications Requiring up to 6 A

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------------------------|----------------------|--|-----|-------------------------------|-----|--------|
| Output noise | N | V _{DD} = 3.6 V V _{LDO} = 2.8 V I _{OUT} = 5 mA to I _{OUT_MAX} f = 10 Hz to 100 kHz | | 50 | | μV rms |
| Quiescent current in ON mode | I _{Q_ON} | T _A = 25 °C | | 9 + 0.34% I _{OUT} | | μA |
| Quiescent current in SLEEP mode | I _{Q_SLEEP} | T _A = 25 °C | | 2 + 0.7% I _{OUT} | | μA |
| Quiescent current in OFF mode | I _{Q_OFF} | V _{LDO} < 0.5 V T _A = 25 °C | | | 1 | μA |
| Turn-on time | T _{ON} | 10 % to 90 % | | | 200 | μs |
| | | SLEEP mode | | | 300 | |
| Turn-off time | T _{OFF} | 90 % to 10 % Pull-down enabled | | | 1 | ms |
| Pull-down resistance in OFF mode | R _{OFF} | V _{LDO} = 0.5 V Can be disabled via LDO<x>_PD_DIS | | 50 | | Ω |

Note 1 At V_{DD} = 1.8 V, the dropout voltage at I_{OUT_MAX} increases by 70%.

5.4.3 LDOCORE

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 °C, V_{SYS} = 2.8 V to 5.5 V.

Table 13: LDOCORE Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-------------------------|-----------------------|---|------|-----|------|------|
| Output voltage | V _{DDCORE} | Note 1 | 2.45 | 2.5 | 2.55 | V |
| | | RESET mode | | 2.2 | | V |
| Stabilization capacitor | C _{OUT} | Including voltage and temperature coefficient | -55% | 2.2 | +35% | μF |
| Output capacitor ESR | R _{COUT_ESR} | f > 1 MHz including wiring parasitics | 0 | | 300 | mΩ |
| Dropout voltage | V _{DROPOUT} | Note 2 | | 50 | 100 | mV |

Note 1 Setting V_{DD_FAULT_LOWER} ≥ 2.65 V avoids LDOCORE dropout, see Section 5.7.

Note 2 The LDOCORE supply, V_{SYS}, must be maintained above V_{DDCORE} + V_{DROPOUT}

NOTE

LDOCORE is only used to supply internal circuits.

PMIC for Applications Requiring up to 6 A

5.5 Buck Converters

5.5.1 Buck1

Unless otherwise noted, the following is valid for $T_J = -40\text{ °C}$ to $+125\text{ °C}$.

Table 14: Buck1 Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------|--|------|--------|------|------------------|
| Input voltage | V_{DD} | $V_{DD} = V_{SYS}$ | 2.8 | | 5.5 | V |
| Output capacitor | C_{OUT} | Half-current mode including voltage and temperature coefficient | -50% | 2 * 22 | +30% | μF |
| | | Full-current mode including voltage and temperature coefficient | | 2 * 47 | | |
| Output capacitor ESR | R_{COUT_ESR} | $C_{OUT} = 2 * 22\ \mu\text{F}$ $f > 100\ \text{kHz}$ Including wiring parasitics | | 15 | 50 | $\text{m}\Omega$ |
| | | $C_{OUT} = 2 * 47\ \mu\text{F}$ $f > 100\ \text{kHz}$ Including wiring parasitics | | 7.5 | 25 | |
| Inductor value | L_{BUCK} | Including current and temperature dependence | 0.7 | 1.0 | 1.3 | μH |
| Inductor resistance | R_{L_DCR} | | | 55 | 100 | $\text{m}\Omega$ |
| PWM Mode | | | | | | |
| Output voltage | V_{BUCK} | Programmable in 10 mV steps Note 1 | 0.3 | | 1.57 | V |
| Output voltage accuracy | V_{BUCK_ACC} | $V_{DD} = 4.2\ \text{V}$, $V_{BUCK} = 1.03\ \text{V}$ Excluding static line/load regulation and voltage ripple $T_A = 25\text{ °C}$ | -1% | | +1% | |
| | | Including static line/load regulation and voltage ripple Note 2 | -3% | | +3% | |
| Transient load regulation | V_{TR_LOAD} | $V_{DD} = 3.6\ \text{V}$, $V_{BUCK} = 1.15\ \text{V}$ $I_{OUT} = 200\ \text{mA}$ to $1000\ \text{mA}$ $di/dt = 3\ \text{A}/\mu\text{s}$ $L = 1\ \mu\text{H}$ | | 30 | 45 | mV |
| Transient line regulation | V_{TR_LINE} | $V_{DD} = 3.0\ \text{V}$ to $3.6\ \text{V}$ $I_{OUT} = 500\ \text{mA}$ $t_R = t_F = 10\ \mu\text{s}$ | | 0.2 | 3 | mV |
| Output current | I_{OUT} | Half-current mode | | | 1250 | mA |
| | | Full-current mode Note 3 | | | 2500 | |
| Current limit | I_{LIM} | Half-current mode controlled in BUCK<x>_ILIM in 100 mA steps | 700 | | 2200 | mA |
| | | Full-current mode controlled in BUCK<x>_ILIM in 200 mA steps | 1400 | | 4400 | |
| Current limit accuracy | I_{LIM_ACC} | | -20% | | 20% | |

PMIC for Applications Requiring up to 6 A

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|---|------|------|------|------|
| Quiescent current in OFF mode | I _{Q_OFF} | | | | 1 | μA |
| Quiescent current in PWM mode | I _{Q_ON} | Half-current mode V _{DD} = 3.6 V I _{OUT} = 0 mA T _A = 25 °C | | 9 | | mA |
| | | Full-current mode V _{DD} = 3.6 V I _{OUT} = 0 mA T _A = 25 °C | | 11 | | |
| Switching frequency Note 4 | f | OSC_FRQ = 0000 | 2.85 | 3 | 3.15 | MHz |
| Switching duty cycle | DC | | 14% | | 83% | |
| Turn-on time | t _{ON} | V _{BUCK} = 1.15 V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 μs BUCK<x>_ILIM = 1500 mA | | 0.37 | 1.2 | ms |
| Output pull-down resistance | R _{PD} | V _{BUCK} = 0.5 V Disabled via BUCK<x>_PD_DIS | | 100 | 200 | Ω |
| PMOS ON resistance | R _{PMOS} | Half-current mode Including pin and routing V _{DD} = 3.6 V | | 160 | | mΩ |
| | | Full-current mode Including pin and routing V _{DD} = 3.6 V | | 80 | | |
| NMOS ON resistance | R _{NMOS} | Half-current mode Including pin and routing V _{DD} = 3.6 V | | 60 | | mΩ |
| | | Full-current mode Including pin and routing V _{DD} = 3.6 V | | 30 | | |
| PFM mode | | | | | | |
| Output voltage | V _{BUCK_PFM} | Programmable in 10 mV steps | 0.3 | | 1.57 | V |
| Mode transition current threshold (PFM to PWM) in AUTO mode Note 5 | I _{AUTO_THR} | V _{DD} = 3.6 V V _{BUCK} = 1.15 V R _{TRACK} ≈ 45 mΩ including bondwire, PCB, and inductor ESR | | 400 | | mA |
| Output current | I _{OUT_PFM} | Forced PFM mode | | | 300 | mA |
| Current limit | I _{LIM_PFM} | | | 1000 | | mA |
| Quiescent current | I _{Q_PFM} | Forced PFM mode I _{OUT} = 0 mA | | 27 | 32 | μA |
| | | AUTO mode I _{OUT} = 0 mA | | 35 | 42 | |
| Mode transition time | t _{AUTO} | AUTO mode | | 6 | | μs |

Note 1 If control BUCK<x>_MODE = 10 (Synchronous) then the buck operates in PFM mode for V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>_MODE = 00.

Note 2 Minimum tolerance 35 mV.

Note 3 For short durations, to meet peak current requirements, I_{OUT} for Buck1 can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

PMIC for Applications Requiring up to 6 A

Note 4 Generated from internal 6 MHz oscillator and can be adjusted by $\pm 10\%$ via control OSC_FRQ, see Section 7.12.

Note 5 Auto-mode is not recommended for new designs, see Section 7.7.6.

5.5.2 Buck2

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$.

Table 15: Buck2 Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------|---|------|----------|--------------------------------|------------------|
| Input voltage | V_{DD} | $V_{DD} = V_{SYS}$ $I_{OUT} \leq 1.5\text{ A}$ | 2.8 | | 5.5 | V |
| | | $V_{DD} = V_{SYS}$ $I_{OUT} > 1.5\text{ A}$ | 3.3 | | 5.5 | |
| Output capacitor | C_{OUT} | $I_{OUT} \leq 1.5\text{ A}$ Including voltage and temperature coefficient | -50% | $2 * 22$ | +30% | μF |
| | | $I_{OUT} > 1.5\text{ A}$ Including voltage and temperature coefficient | -50% | $2 * 47$ | +30% | |
| Output capacitor ESR | R_{COUT_ESR} | $C_{OUT} = 2 * 22\text{ }\mu\text{F}$ $f > 100\text{ kHz}$ Including wiring parasitics | | 15 | 50 | $\text{m}\Omega$ |
| | | $C_{OUT} = 2 * 47\text{ }\mu\text{F}$ $f > 100\text{ kHz}$ Including wiring parasitics | | 7.5 | 25 | |
| Inductor value | L_{BUCK} | Including current and temperature dependence | 0.7 | 1.0 | 1.3 | μH |
| Inductor resistance | R_{L_DCR} | | | 55 | 100 | $\text{m}\Omega$ |
| PWM Mode | | | | | | |
| Output voltage | V_{BUCK} | Programmable in 20 mV steps | 0.8 | | 3.34 Note 1 | V |
| Output voltage accuracy | V_{BUCK_ACC} | Including static line and load regulation and voltage ripple Note 2 | -3% | | +3% | |
| Transient load regulation | V_{TR_LOAD} | $V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 1.8\text{ V}$ $I_{OUT} = 200\text{ mA}$ to 1000 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 1\text{ }\mu\text{H}$ | | 30 | 45 | mV |
| | | $V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 1.8\text{ V}$ $I_{OUT} = 200\text{ mA}$ to 2000 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 1\text{ }\mu\text{H}$ | | 60 | 90 | |
| | | $V_{DD} = 5.0\text{ V}$, $V_{BUCK} = 3.34\text{ V}$ $I_{OUT} = 200\text{ mA}$ to 2000 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 1\text{ }\mu\text{H}$ | | 60 | 90 | |
| Transient line regulation | V_{TR_LINE} | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 500\text{ mA}$ $t_R = t_F = 10\text{ }\mu\text{s}$ | | 0.2 | 3 | mV |
| Output current | I_{OUT} | $V_{DD} - V_{BUCK} \geq 1.25\text{ V}$ Note 3 | | | 2000 | mA |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------|--|------|------|------|---------------|
| | | $V_{DD} - V_{BUCK} \geq 1.00 \text{ V}$ | | | 1250 | |
| | | $V_{DD} - V_{BUCK} \geq 0.75 \text{ V}$ | | | 900 | |
| Current limit | I_{LIM} | Controlled in BUCK2_ILIM in 100 mA steps | 1700 | | 3200 | mA |
| Current limit accuracy | I_{LIM_ACC} | | -20% | | 20% | |
| Quiescent current in OFF mode | I_{Q_OFF} | | | | 1 | μA |
| Quiescent current in PWM mode | I_{Q_ON} | $I_{OUT} = 0 \text{ mA}$ $T_A = 25 \text{ }^\circ\text{C}$ | | 9 | | mA |
| Switching frequency Note 4 | f | OSC_FRQ = 0000 | 2.85 | 3 | 3.15 | MHz |
| Switching duty cycle | D | | 15% | | 90% | |
| Turn-on time | t_{ON} | $V_{BUCK} = 1.80 \text{ V}$ BUCK_SLOWSTART = disabled SLEW_RATE = 20 mV/2 μs BUCK2_ILIM = 2500 mA | | 0.44 | 1.5 | ms |
| Output pull-down resistance | R_{PD} | $V_{BUCK} = 0.5 \text{ V}$ Disabled via BUCK2_PD_DIS | | 100 | 200 | Ω |
| PMOS ON resistance | R_{PMOS} | Including pin and routing $V_{DD} = 3.6 \text{ V}$ | | 150 | | m Ω |
| NMOS ON resistance | R_{NMOS} | Including pin and routing $V_{DD} = 3.6 \text{ V}$ | | 60 | | m Ω |
| PFM mode | | | | | | |
| Output voltage | V_{BUCK_PFM} | Programmable in 20 mV steps | 0.8 | | 3.34 | V |
| Mode transition current threshold (PFM to PWM) in AUTO mode Note 5 | I_{AUTO_THR} | $V_{DD} = 3.6 \text{ V}$ $V_{BUCK} = 1.8 \text{ V}$ $R_{TRACK} \sim 45 \text{ m}\Omega$ Including bondwire, PCB, and inductor ESR | | 400 | | mA |
| Output current | I_{OUT_PFM} | Forced PFM mode | | | 300 | mA |
| Current limit | I_{LIM_PFM} | | | 1000 | | mA |
| Quiescent current | I_{Q_PFM} | Forced PFM mode, $I_{OUT} = 0 \text{ mA}$ | | 22 | 25 | μA |
| | | AUTO mode, $I_{OUT} = 0 \text{ mA}$ | | 30 | 35 | |
| Mode transition time | t_{AUTO} | AUTO mode | | 6 | | μs |

Note 1 Maximum output is $V_{DD} - 0.7 \text{ V}$

Note 2 Minimum tolerance 35 mV

Note 3 For short durations, to meet peak current requirements, I_{OUT} for Buck2 can be operated at up to 10 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

Note 4 Generated from internal 6 MHz oscillator and can be adjusted by $\pm 10 \%$ via register OSC_FRQ, see Section [7.12](#).

Note 5 Auto-mode is not recommended for new designs, see Section [7.7.6](#).

PMIC for Applications Requiring up to 6 A

5.5.3 Buck3

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

Table 16: Buck3 Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------|--|------|--------|------|------------------|
| Input voltage | V_{DD} | $V_{DD} = V_{SYS}$ | 2.8 | | 5.5 | V |
| Output capacitor | C_{OUT} | Including voltage and temperature coefficient | -50% | 2 * 22 | +30% | μF |
| Output capacitor ESR | R_{COUT_ESR} | $f > 100\text{ kHz}$ Including wiring parasitics | | 15 | 50 | $\text{m}\Omega$ |
| Inductor value | L_{BUCK} | Including current and temperature dependence | 0.7 | 1.0 | 1.3 | μH |
| Inductor resistance | R_{L_DCR} | | | 55 | 100 | $\text{m}\Omega$ |
| PWM Mode | | | | | | |
| Output voltage | V_{BUCK} | Programmable in 10 mV steps Note 1 | 0.7 | | 1.8 | V |
| Output voltage accuracy | V_{BUCK_ACC} | Including static line/load regulation and voltage ripple Note 2 | -3% | | +3% | |
| Transient load regulation | V_{TR_LOAD} | $V_{DD} = 3.6\text{ V}$ $V_{BUCK} = 1.35\text{ V}$ $I_{OUT} = 200\text{ mA}$ to 1000 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 1\text{ }\mu\text{H}$ | | 25 | 40 | mV |
| | | $V_{DD} = 3.6\text{ V}$ $V_{BUCK} = 1.35\text{ V}$ $I_{OUT} = 200\text{ mA}$ to 1500 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 1\text{ }\mu\text{H}$ | | 40 | 60 | mV |
| Transient line regulation | V_{TR_LINE} | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 500\text{ mA}$ $t_R = t_F = 10\text{ }\mu\text{s}$ | | 0.2 | 3 | mV |
| Output current | I_{OUT} | $V_{DD} - V_{BUCK} \geq 1.25\text{ V}$ Note 3 | | | 1500 | mA |
| | | $V_{DD} - V_{BUCK} \geq 1.00\text{ V}$ | | | 1250 | |
| Current limit | I_{LIM} | Controlled in BUCK3_ILIM in 100 mA steps | 700 | | 2200 | mA |
| Current limit accuracy | I_{LIM_ACC} | $I_{LIM} = 700\text{ mA}$ to 1400 mA | -15 | | +25 | % |
| | | $I_{LIM} = 1400\text{ mA}$ to 2200 mA | -10 | | +15 | |
| Quiescent current in OFF mode | I_{Q_OFF} | | | | 1 | μA |
| Quiescent current in PWM mode | I_{Q_ON} | $I_{OUT} = 0\text{ mA}$ $T_A = 25\text{ }^{\circ}\text{C}$ | | 9 | | mA |
| Switching frequency Note 4 | f | OSC_FRQ = 0000 | 2.85 | 3 | 3.15 | MHz |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|--|------|------|-----|------|
| Switching duty cycle | D | | 14 | | 83 | % |
| Turn-on time | t _{ON} | V _{BUCK} = 1.35 V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 μs BUCK3_ILIM = 1500 mA | | 0.39 | 1.2 | ms |
| Output pull-down resistance | R _{PD} | V _{BUCK} = 0.5 V Disabled via BUCK3_PD_DIS | | 100 | 200 | Ω |
| PMOS ON resistance | R _{PMOS} | Including pin and routing V _{DD} = 3.6 V | | 150 | | mΩ |
| NMOS ON resistance | R _{NMOS} | Including pin and routing V _{DD} = 3.6 V | | 60 | | mΩ |
| PFM mode | | | | | | |
| Output voltage | V _{BUCK_PFM} | Programmable in 10 mV steps. | 0.53 | | 1.8 | V |
| Mode transition current threshold (PFM to PWM) in AUTO mode Note 5 | I _{AUTO_THR} | V _{DD} = 3.6 V V _{BUCK} = 1.35 V R _{TRACK} ≈ 45 mΩ Including bondwire, PCB, inductor ESR | | 400 | | mA |
| Output current | I _{OUT_PFM} | | | | 300 | mA |
| Current limit | I _{LIM_PFM} | | | 1000 | | mA |
| Quiescent current | I _{Q_PFM} | Forced PFM mode I _{OUT} = 0 mA | | 22 | 25 | μA |
| | | AUTO mode I _{OUT} = 0 mA | | 30 | 35 | |
| Mode transition time | t _{AUTO} | AUTO mode | | 6 | | μs |

Note 1 If register BUCK3_MODE = 10 (synchronous) then the buck operates in PFM mode for V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK3_MODE = 00.

Note 2 Minimum tolerance 35 mV.

Note 3 For short durations, to meet peak current requirements, I_{OUT} for Buck3 can be operated at up to 10 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

Note 4 Generated from internal 6 MHz oscillator and can be adjusted by ±10% via control OSC_FRQ, see Section [7.12](#).

Note 5 Auto-mode is not recommended for new designs, see Section [7.7.6](#).

5.6 Internal Oscillator

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 °C, V_{SYS} = 2.8 V to 5.5 V.

Table 17: Internal Oscillator Electrical Characteristics

| Parameter | Symbol | Test conditions | Min | Typ | Max | Unit |
|----------------------|------------------|-----------------|-----|-----|-----|------|
| Oscillator frequency | f _{OSC} | OSC_FRQ = 0000 | 5.7 | 6 | 6.3 | MHz |

Note 1 Oscillator frequency can be further adjusted by about ±10%, see Section [7.12](#).

PMIC for Applications Requiring up to 6 A

5.7 System Supply Voltage Supervision

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{\text{SYS}} = 2.8\text{ V}$ to 5.5 V .

Table 18: System Supply Voltage Supervision Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|-----------------|-----|---|------|---------------|
| Under-voltage lockout lower threshold | $V_{\text{POR_LOWER}}$ | | | 2.0 | | V |
| Under-voltage lockout upper threshold | $V_{\text{POR_UPPER}}$ | | | 2.3 | | V |
| V_{SYS} under-voltage lower threshold | $V_{\text{DD_FAULT_LOWER}}$ Note 1 | | 2.5 | 2.8 | 3.25 | V |
| V_{SYS} under-voltage lower threshold accuracy | $V_{\text{SYS_LOWER}}$ | | -2% | | +2% | |
| V_{SYS} hysteresis | $V_{\text{DD_FAULT_HYS}}$ Note 2 | | 100 | 200 | 450 | mV |
| V_{SYS} upper threshold | $V_{\text{DD_FAULT_UPPER}}$ | | -2% | $V_{\text{DD_FAULT_LOWER}} + V_{\text{DD_FAULT_HYS}}$ | +2% | |
| Reference voltage | V_{REF} | | -1% | 1.2 | +1% | V |
| V_{REF} decoupling capacitor | C_{VREF} | | | 2.2 | | μF |
| Reference current resistor | R_{IREF} | | -1% | 200 | +1% | k Ω |

Note 1 Can be set in 50 mV steps via control $V_{\text{DD_FAULT_ADJ}}$ in register CONFIG_B , setting $V_{\text{DD_FAULT_LOWER}} \geq 2.65\text{ V}$ avoids LDOCORE dropout, see Section 5.4.3.

Note 2 Can be set in 50 mV steps via control $V_{\text{DD_HYST_ADJ}}$ in register CONFIG_B .

5.8 Junction Temperature Supervision

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{\text{SYS}} = 2.8\text{ V}$ to 5.5 V .

Table 19: Junction Temperature Supervision Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|-------------------|-----------------|-----|-----|-----|------------------|
| POR temperature threshold Note 1 | T_{POR} | Note 2 | 145 | 150 | 155 | $^\circ\text{C}$ |
| Critical temperature threshold Note 1 | T_{CRIT} | Note 2 | 135 | 140 | 145 | $^\circ\text{C}$ |
| Warning temperature threshold Note 1 | T_{WARN} | Note 2 | 120 | 125 | 130 | $^\circ\text{C}$ |

Note 1 See section 7.10.

Note 2 Thermal thresholds are non-overlapping.

PMIC for Applications Requiring up to 6 A**5.9 Current Consumption**

Unless otherwise noted, the following is valid for $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{SYS} = 2.8\text{ V}$ to 5.5 V .

Table 20: Current Consumption Electrical Characteristics

| Operating mode | Symbol | Test Conditions | V_{SYS} (Typ) | Unit |
|----------------|-------------|--|-----------------|---------------|
| POWERDOWN mode | I_{DDPD} | $V_{SYS} > 3.0\text{ V}$ LDOCORE enabled Bucks and LDOs disabled | 40 | μA |
| ACTIVE mode | I_{DDACT} | Bucks and LDOs enabled | 400 | μA |

6 Typical Characteristics

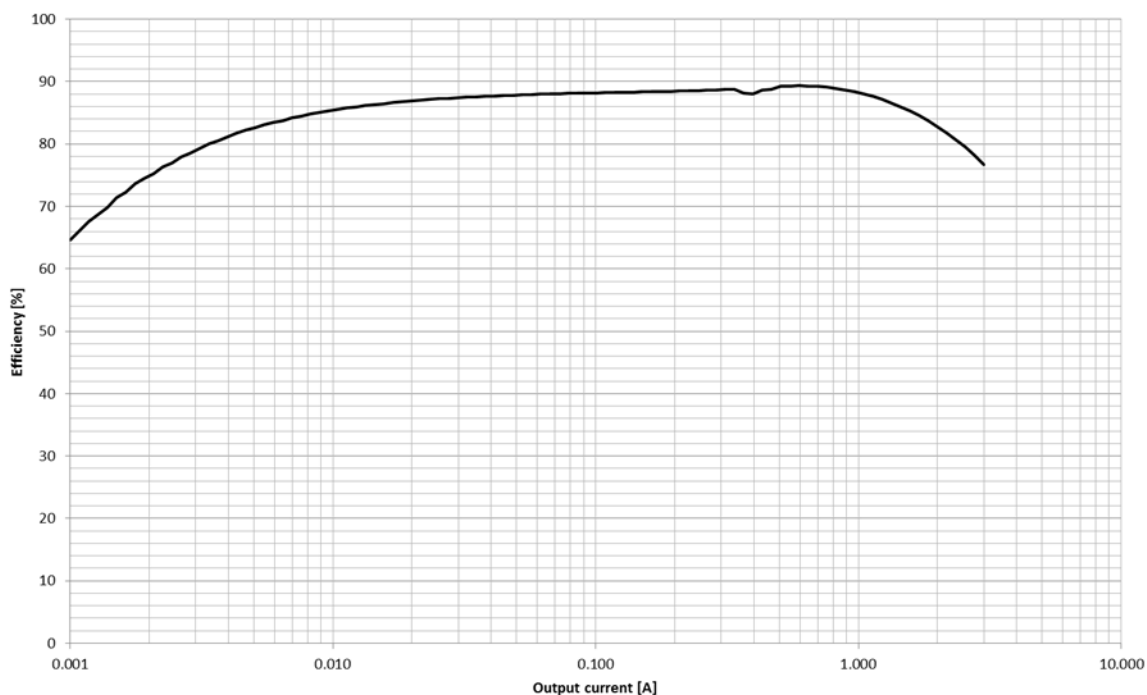


Figure 5: Buck1 Efficiency in AUTO Mode ($V_{IN} = 3.60\text{ V}$, $V_{OUT} = 1.15\text{ V}$)

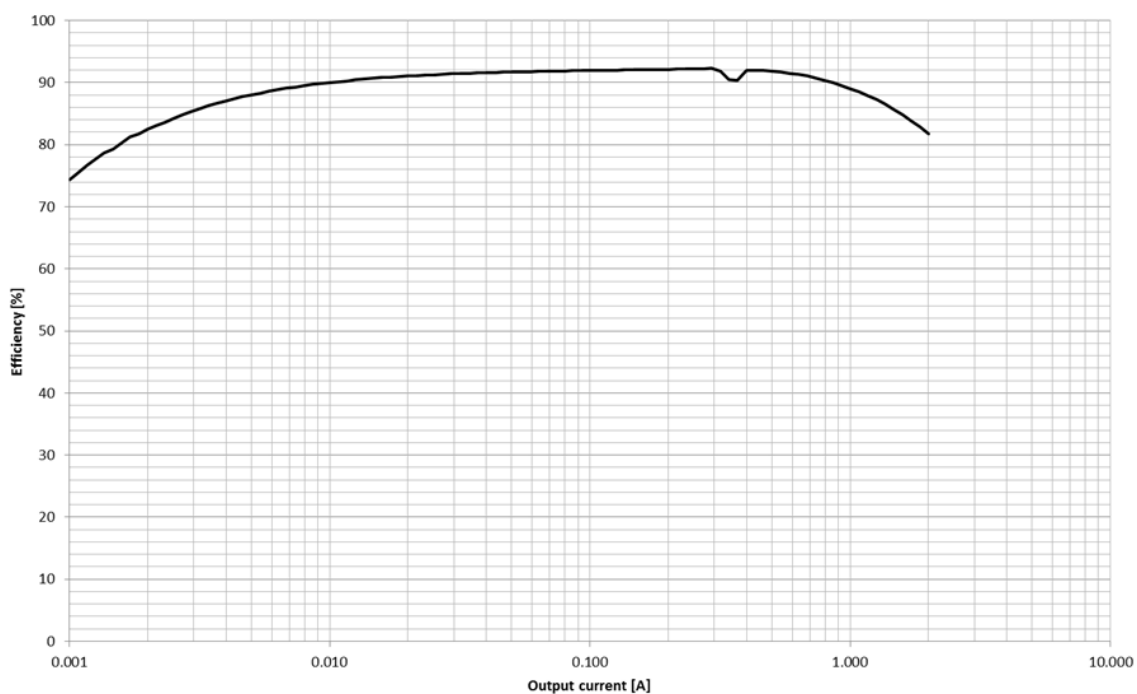


Figure 6: Buck2 Efficiency in AUTO Mode ($V_{IN} = 3.60\text{ V}$, $V_{OUT} = 1.80\text{ V}$)

PMIC for Applications Requiring up to 6 A

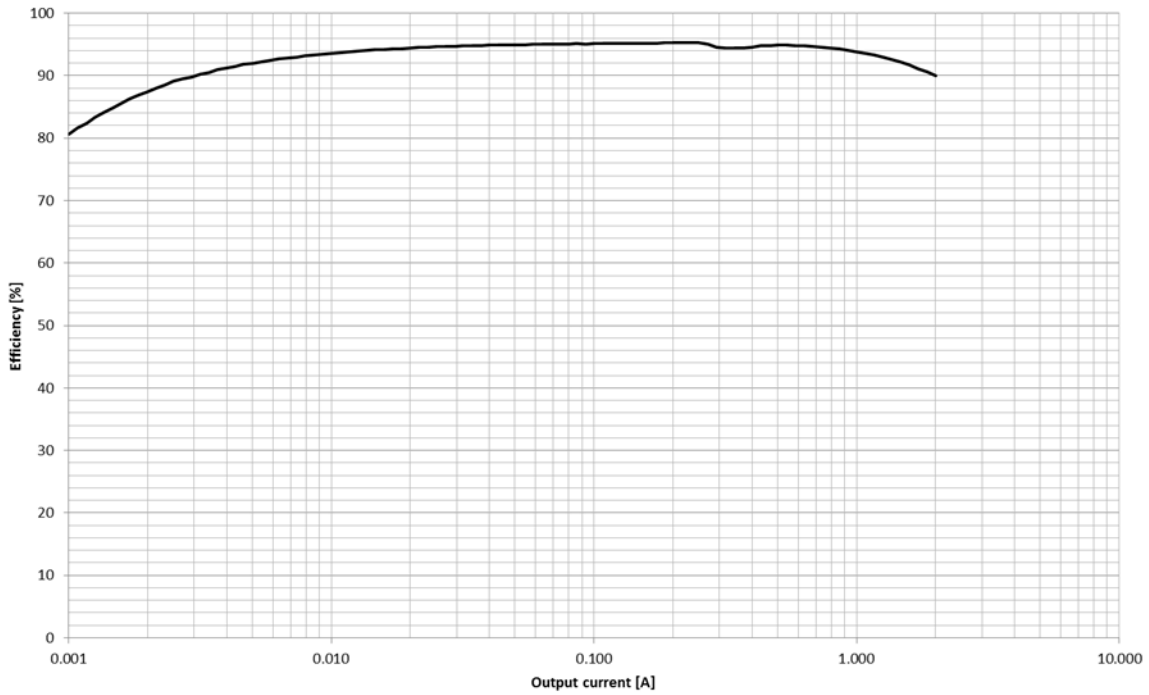


Figure 7: Buck2 Efficiency in AUTO Mode ($V_{IN} = 5.00\text{ V}$, $V_{OUT} = 3.34\text{ V}$)

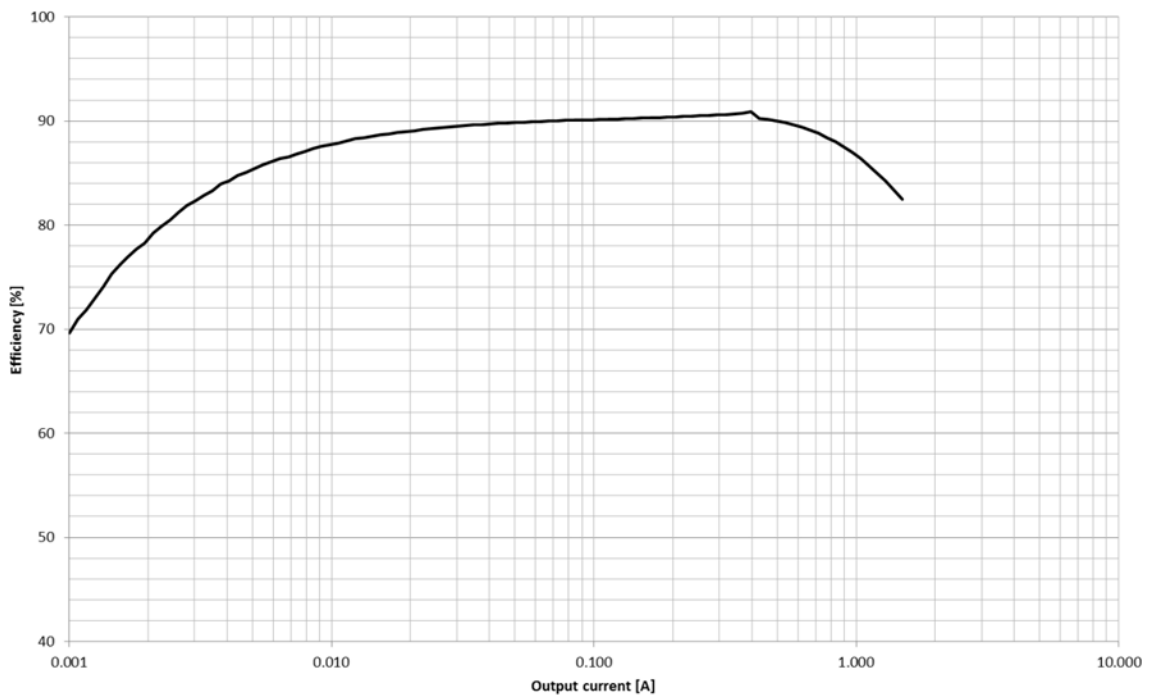


Figure 8: Buck3 Efficiency in AUTO Mode ($V_{IN} = 3.60\text{ V}$, $V_{OUT} = 1.35\text{ V}$)

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7 Functional Description

7.1 Control Signals

Each of the input signals described below feature a debounce filter. They share a common debounce time control (DEBOUNCING).

7.1.1 nONKEY

nONKEY is an edge-sensitive signal that controls the power mode of DA9061. Both falling and rising edges are detected and the time between the edges is measured. This enables different lengths of key press detection. The detection circuitry is enabled in all power modes of the device.

The status of the signal after debouncing can be read from NONKEY (reg. STATUS_A). The mask bit M_NONKEY prevents interrupt and wakeup events that would normally be caused by an nONKEY event.

nONKEY has four modes of operation, see [Table 21](#), which can be selected by NONKEY_PIN. NONKEY_LOCK controls the wakeup event generation of the nONKEY. If NONKEY_LOCK is asserted (depends on NONKEY_PIN), a short nONKEY press (shorter than KEY_DELAY) will not generate a wakeup.

Table 21: nONKEY Functions

| nONKEY_PIN | Function |
|------------|---|
| 00 | An event (E_nONKEY) is generated when nONKEY is asserted. If not masked, the event causes an interrupt. A wakeup is triggered if the device is in POWERDOWN mode. |
| 01 | A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge. If the signal stays asserted and the timer reaches the programmed value, an event is generated and nONKEY_LOCK is asserted. |
| 10 | A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge. If the signal stays asserted and the timer reaches the programmed value, an event is generated, nONKEY_LOCK is asserted, and a power-down sequence is triggered by automatically clearing SYSTEM_EN. |
| 11 | A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge, SYSTEM_EN is cleared, and STANDBY is asserted. If the signal stays asserted and the timer reaches the programmed value, an event is generated, nONKEY_LOCK is asserted, and SYSTEM_EN and STANDBY are cleared. |

Whenever nONKEY_LOCK is asserted, a long key press (longer than the time programmed in KEY_DELAY) is required to wakeup from POWERDOWN mode. If the wakeup is also desired after a short key press, nONKEY_LOCK has to be cleared before entering the POWERDOWN mode.

7.1.2 nRESETREQ

nRESETREQ is an active-low reset request that causes DA9061 to enter RESET mode. The transition to the RESET mode is handled by the power sequencer and it can be sped up by setting the HOST_SD_MODE bit. Before entering the RESET mode, a fault log bit is set (nRESETREQ) and nRESET is asserted.

nRESETREQ should be tied to an always-on rail that is supplied in all modes of the DA9061 such as VSYS. It is not recommended to tie nRESETREQ to any of the regulator outputs.

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7.1.3 nRESET

nRESET is an active-low reset output intended for resetting the host processor of the system. The signal can be configured as either push-pull or open drain output (PM_O_TYPE).

nRESET is always asserted upon a cold boot from the no-power mode. It is always asserted at the beginning of a shutdown sequence to the RESET mode. nRESET may also be asserted at the beginning of the sequence to the POWERDOWN mode, if configured in control NRES_MODE.

De-assertion of nRESET is controlled by a reset timer. After being asserted, nRESET remains low until the reset timer, which was started from the selected trigger signal, expires. The reset timer trigger can be selected via RESET_EVENT and set to one of the following: an external signal triggering the wakeup (EXT_WAKEUP), an internal signal indicating the end of the first power-up sub-sequence (SYS_UP), an internal signal indicating the end of the second power-up sub-sequence (PWR_UP), or the transition of DA9061 from reset to POWERDOWN mode. The expiry time can be configured via RESET_TIMER from 1 ms to 1 s. If RESET_TIMER is set to 0 ms, nRESET is de-asserted immediately after the trigger selected with RESET_EVENT.

7.1.4 nIRQ

nIRQ is a level-sensitive interrupt signal. It can be configured either as a push-pull or an open drain output (selected via PM_O_TYPE). The polarity of nIRQ can be selected with IRQ_TYPE.

nIRQ is asserted when an unmasked event has occurred. The nIRQ will not be released until all event registers have been cleared. New events that occur while reading an event register are saved until the event register is cleared, ensuring that the host processor captures them. The same will happen to all events occurring when the power sequencer is in transition.

7.2 2-Wire Interface

The 2-wire interface provides access to the control and status registers. The interface supports operations compatible to the standard, fast, fast-plus, and high-speed modes of the I²C bus specification Rev. 3. Communication on the 2-wire bus is always between two devices; one acting as the master and the other as the slave. The DA9061 only operates as a slave. The default address is 0xB0, this is configurable via OTP, see IF_BASE_ADDR. I²C addresses are stated as 8-bit addresses including R/W bit; for example, 0xB0 is the 8-bit address equivalent to the 7-bit address 0x58 plus the R/W bit = 0 (Write).

SCL transmits 2-wire clock data and SDA transmits the bidirectional data. The 2-wire interface is open-drain supporting multiple devices on one line. The bus lines have to be pulled high by an external pull-up resistor (2 kΩ to 20 kΩ). The attached devices drive the bus lines low by connecting them to ground. As a result, two devices can drive the bus simultaneously without conflict. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the DA9061 internal clock signals. DA9061 stays within the described host clock speed limitations and does not initiate clock slow-down. An automatic interface reset is triggered when the clock signal ceases toggling for >35 ms (controlled in TWOWIRE_TO).

When the SDA is stuck, the bus clears after receiving nine clock pulses. Operation in high-speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable slope-control. The high-speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. The DA9061 does not make use of clock stretching and delivers read data without delay up to 3.4 MHz.

Alternatively, the interface can be configured to use high-speed mode continuously via PM_IF_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus and limits the attachable bus slaves to compatible devices.

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7.2.1 Register Map Paging

The 2-wire interface has direct access to two pages of the DA9061 register map (up to 256 addresses). The register at address zero on each page is used as a page control register (the LSB of control PAGE is ignored). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 is selected using control REVERT. Unless REVERT was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

DA9061 also offers an alternative way to access register pages which avoids writing explicitly to PAGE. DA9061 responds to multiple consecutive slave addresses and updates PAGE automatically based on the slave address. For example, when $IF_BASE_ADDR[7:4] = 0xB$ the slave address changes PAGE as follows:

Slave address = $0xB0 \Rightarrow$ PAGE = $0x00$

Slave address = $0xB2 \Rightarrow$ PAGE = $0x02$

7.2.2 Details of the 2-Wire Protocol

All data is transmitted across the 2-wire bus in 8-bit groups. To send a bit, the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL stores the SDA bit in the receiver's shift register.

A 2-byte serial protocol is used: one address byte and one data byte. Data and address transfer transmits the MSB first for both read and write operations. All transmissions begin with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in high state. The START and STOP conditions are illustrated in [Figure 9](#).

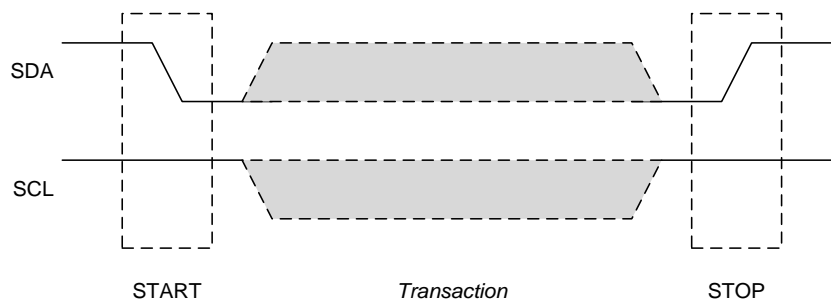


Figure 9: Timing of the START and STOP Conditions

DA9061 monitors the 2-wire bus for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with A in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. DA9061 responds to all bytes with an ACK. A register write operation is illustrated in [Figure 10](#).

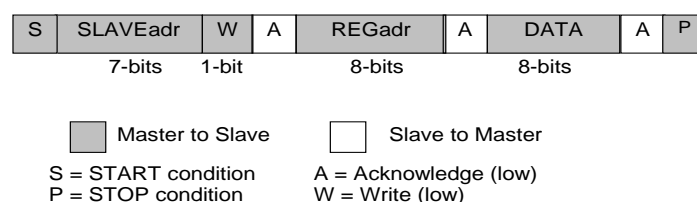


Figure 10: Byte Write Operation

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When the host reads register data the DA9061 first has to access the target register address with write access and then with read access and a repeated START, or alternatively a second START, condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition, see [Figure 11](#).

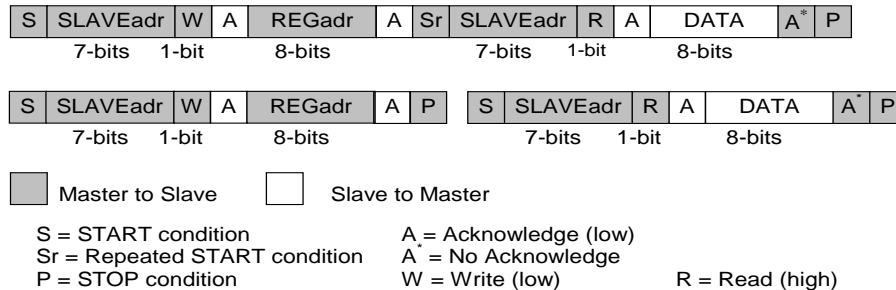


Figure 11: Examples of Byte Read Operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see [Figure 12](#). The 2-wire control block then increments the address pointer to the next register address and sends the data to the master. The data bytes are read continuously until the master sends a NACK followed by a subsequent STOP condition directly after receiving the data. If a non-existent 2-wire address is read out then the DA9061 will return code zero.

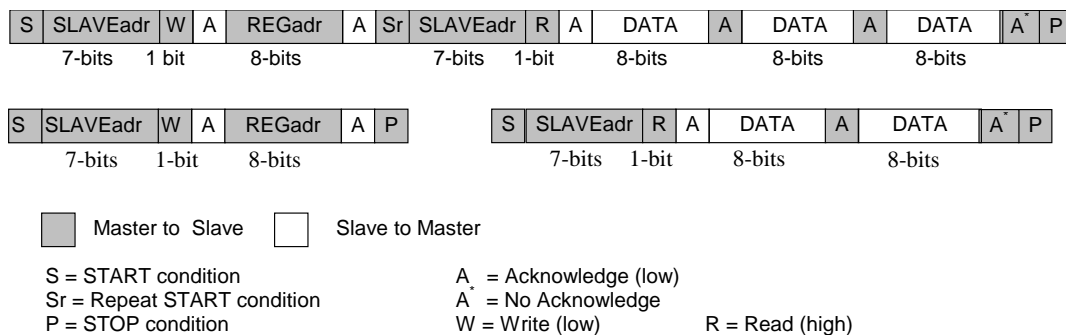


Figure 12: 2-Wire Page Read

The slave address after the repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes after sending the register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in [Figure 13](#).

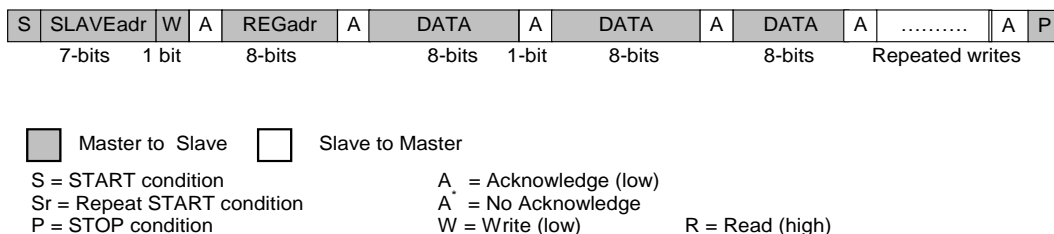


Figure 13: 2-Wire Page Write

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Table 22: GPIO Functions

| GPIO<x>_PIN | Function | GPIO<x>_MODE | GPIO<x>_TYPE | GPIO<x>_WKUP_MODE | GPIO<x>_WEN |
|-------------|--------------------|-----------------------------------|---------------------------------|---|---|
| 0 | Alternate function | No effect | No effect | No effect | No effect |
| 1 | GPI | 0: Debounce off 1: Debounce on | 0: Active low 1: Active high | 0: Edge-sensitive wakeup 1: Level-sensitive wakeup | 0: Wakeup disabled 1: Wakeup enabled |
| 2 | GPO Open drain | 0: Output low 1: Output high | No effect | No effect | No effect |
| 3 | GPO Push-pull | 0: Output low 1: Output high | No effect | No effect | No effect |

7.3.1 GPI Functionality

When configured as a GPI, the polarity of the input can be selected with GPIO<x>_TYPE. A debouncing filter can be applied on the input signals with a configurable debouncing time (control DEBOUNCING). An event is generated at the active edge of the input. The active edge is determined by the signal polarity configured in GPIO<x>_TYPE. The event can be further configured to generate a wakeup via GPIO<x>_WKUP_MODE and GPIO<x>_WEN. An internal pull-down can be activated for the inputs in GPIO<x>_PUPD.

A level sensitive wakeup event can also be configured for each GPI via GPIO<x>_WKUP_MODE and GPIO<x>_WEN. The functionality of the level-sensitive wakeup is described in [Table 25](#).

7.3.1.1 Regulator Control

GPIO1, GPIO2, and GPIO3 can be used for controlling DA9061 regulators. When configured as GPIs, they can be used to enable regulators or select between their two output voltage settings.

As seen in [Figure 15](#), the regulator control is branched after the GPIO<x>_TYPE control allowing active edge delegation for the regulator control. Finally, the functionality for the GPI is selected with the regulator controls BUCK<x>_GPI, LDO<x>_GPI, VBUCK<x>_GPI, and VLDO<x>_GPI.

One GPI can be used to control the same function on multiple regulators simultaneously. When a regulator is controlled by a GPI, the same function (on/off or voltage selection) can no longer be controlled by the power supply sequencer. The regulator still responds normally to register writes to the control bit.

Enable/Disable Control

A GPI is used for enabling/disabling regulators when it is selected in one of the BUCK<x>_GPI or LDO<x>_GPI controls. A passive to active transition sets the regulator enable bit (BUCK<x>_EN, LDO<x>_EN), and an active to passive transition clears it.

Output Voltage Control

A GPI is used for the output voltage selection when it is selected in one of the VBUCK<x>_GPI or VLDO<x>_GPI controls. A passive to active transition sets the voltage selection bit (VBUCK<x>_SEL, VLDO<x>_SEL), and an active to passive edge clears it.

7.3.1.2 Sequencer WAIT_STEP

GPIO3 can be used for the WAIT_STEP functionality. The power sequencer can be programmed to wait for either a rising or falling edge of the WAIT_STEP input, see [Section 7.9.5](#). The active edge is selected from GPIO<x>_TYPE.

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7.3.2 GPO Functionality

The outputs can be configured as push-pull or open drain outputs, see [Table 22](#). An internal pull-up can be enabled/disabled from GPIO<x>_PUPD (open drain mode). The GPIO<x>_MODE settings can control the output state.

Instead of controlling the output with GPIO<x>_MODE, a selection of alternatives is available in the GPIO<x>_OUT controls. These include: the forwarding function, see [Section 7.3.4](#), the power supply sequencer, see [Section 7.9](#), and the status of the supply voltage supervision (nVDD_FAULT). When the GPIO is configured as an output and GPIO<x>_OUT is set to 0x0, the GPIO<x>_MODE determines the state of the output.

7.3.2.1 nVDD_FAULT

nVDD_FAULT gives the status of the system supply monitoring, see [Section 7.11](#). The assertion of nVDD_FAULT indicates that the main supply input voltage has been low ($V_{SYS} < V_{DD_FAULT_LOWER}$) for more than 100 ms and informs the host processor that the power will shut down. It can be configured to drive a GPO from the GPIO<x>_OUT controls. The driver type (push-pull, open-drain) selection and pull-up resistor control function normally. The GPIO<x>_MODE can be used to invert the incoming nVDD_FAULT signal.

7.3.3 Alternate Functions

GPIO0, GPIO2, and GPIO4 can be used for alternate functions. These are digital control signals that do not employ the debouncing, event detection, or interrupt generation functions. Only the input buffer of the GPIO block is employed. The alternate functions of DA9061 are listed in [Table 23](#) and described in the following subsections. A debouncing filter can be applied also on the alternate functions with a configurable debouncing time (register DEBOUNCING).

Table 23: GPIO Alternate Input Functions

| GPIO | Alternate Function | Description |
|-------|--------------------|--------------------------|
| GPIO0 | WDKICK | Watchdog kick or disable |
| GPIO1 | - | |
| GPIO2 | PWR_EN | Power mode control |
| GPIO3 | - | |
| GPIO4 | SYS_EN | Power mode control |

7.3.3.1 SYS_EN

SYS_EN (pin GPIO4) controls the SYSTEM_EN bit and thereby the power mode of DA9061. It is part of the power supply sequencer functionality described in [Section 7.9](#). SYS_EN is an edge-sensitive signal and its polarity can be chosen in the GPIO4_TYPE control.

Asserting SYS_EN causes an interrupt (E_GPIx) and a wakeup event. De-asserting SYS_EN triggers a power-down sequence but no interrupt.

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7.3.3.2 PWR_EN

PWR_EN (pin GPIO2) controls the POWER_EN bit and thereby the power mode of DA9061. It is part of the power supply sequencer functionality described in Section 7.9. PWR_EN is an edge-sensitive signal and its polarity can be chosen in the GPIO2_TYPE control. A wakeup event can be generated after assertion of PWR_EN if so configured in GPIO2_WEN.

7.3.3.3 WDKICK

A rising edge of the WDKICK signal resets the watchdog counter. The polarity of the signal can be chosen in the GPIO0_TYPE control. If the signal is kept asserted, the watchdog is disabled as the counter is not incremented (WDG_MODE), see Section 7.13.

7.3.4 GPIO Forwarding

GPIO forwarding works between GPIOs 0, 1, 2, and 3. Any of these GPIOs can be routed directly to GPIO0, 1, and 3 after debouncing. Forwarding is one of the options for the GPIO<x>_OUT control.

7.4 Dynamic Voltage Control

All of DA9061's buck converters can be controlled in several ways to achieve Dynamic Voltage Control (DVC). The buck converters feature a voltage ramping feature that enables smooth transition from one voltage setting to another.

All output voltages can be controlled with software via the 2-wire interface (VBUCK<x>_A). The 2-wire interface is operational when the device is in ACTIVE mode.

7.5 Regulator Voltage A and B Selection

In addition, all regulators feature A and B settings which can be programmed with different voltages (VBUCK<x>_A, VBUCK<x>_B), one of which is chosen according to the operating mode of the system (VBUCK<x>_SEL, VLDO<x>_SEL). In addition to the output voltage, the A and B settings include a bit to force the regulator into SLEEP mode which reduces the quiescent current.

The selection between the A and B settings can be done either with software via the 2-wire interface or by the power sequencer, see Section 7.9. Furthermore, each regulator can be enabled with a GPI pin, see Section 7.3.1.1, and the selection between the A and B settings done with another GPI.

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7.6 LDOs

All LDOs employ Dialog Semiconductor's **Smart Mirror™** dynamic biasing technology, see [Figure 16](#), which maintains high performance over a wide range of operating conditions and a power saving mode (SLEEP mode) to minimize the quiescent current during very low output current. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is maintained across the full operating current range however quiescent current consumption is scaled to demand improved efficiency when current demand is low.

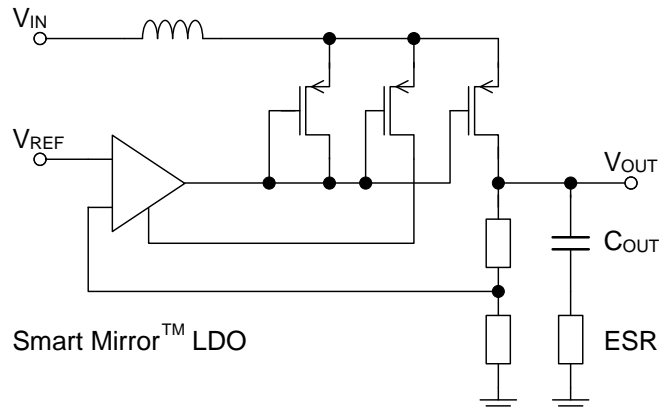


Figure 16: Smart Mirror Voltage Regulator

7.6.1 Control

The LDOs can be enabled by writing directly to a control bit (LDO<x>_EN), controlling it via a GPI, see [Section 7.3.1.1](#), or assigning it to a power sequencer step, see [Section 7.9.3](#). Each LDO features two voltage control registers (VLDO<x>_A/VLDO<x>_B) that allow two output voltage pre-configurations. The active setting can then be selected either with a control bit (VLDO<x>_SEL), via a GPI, see [Section 7.3.1.1](#), or automatically based on the DA9061 power mode. The SLEEP mode of the LDOs can be linked to either the A or B setting (LDO<x>_SL_A/LDO<x>_SL_B). Therefore, the LDO will switch to SLEEP mode when the setting is active.

LDO1 differs from the other LDOs because it can be configured as an always-on regulator. This means that it is also enabled in RESET mode, see [Section 7.8.2](#).

7.6.2 Current Limit

Each LDO provides over-current detection. The current limit is fixed for each LDO based on their current capability. If any of the LDOs' current limit is exceeded for longer than 10 ms, an event, E_LDO_LIM, is triggered. The status of the limit comparator can be observed from LDO<x>_ILIM (reg. STATUS_D). If an LDO's current limit is exceeded for longer than 200 ms, the LDO is automatically disabled. This shutdown feature can be disabled by clearing the LDO_SD control. Once disabled due to an over-current, the LDO must be re-enabled by one of the sources described in [Section 7.6.1](#).

7.6.3 Output Pull-Down

When over-voltage ($1.06 * VLDO<x>$) occurs, the voltage regulators enable an internal load to discharge the output back to its configured voltage. This feature can be disabled in LDO<x>_PD_DIS.

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7.7 Switching Regulators

DA9061 includes four step-down switching regulators operating at 3 MHz. All switching regulators employ a synchronous topology with an internal NFET, thus eliminating the need for an external Schottky diode. The output voltage can be set in 10 mV steps (20 mV steps for Buck2) and the regulation accuracy is $\pm 3\%$ over the whole operating temperature range. Static line and load regulation are also considered in this accuracy.

The switching frequency (3 MHz) is high enough to warrant the use of a small 1.0 μH inductor. The programming of the converter current limit depends on the coil parameters, as illustrated in [Table 24](#).

Table 24: Buck Current Limit

| Min. ISAT (mA) | Frequency (MHz) | Buck Current Limit (mA) |
|----------------|-----------------|-------------------------|
| 1750 | 3 | 1500 |
| 1460 | 3 | 1200 |
| 1180 | 3 | 950 |
| 940 | 3 | 750 |

7.7.1 Control

The buck can be enabled manually by writing directly to a control register, with an external signal connected to GPI, see [Section 7.3.1.1](#), or by assigning it to a power sequencer step, see [Section 7.9.3](#). Each buck converter features two voltage control registers (VBUCK<x>_A/VBUCK<x>_B) which can be programmed with two different voltages. The active setting can then be selected via a control bit (VBUCK<x>_SEL), via a GPI, see [Section 7.3.1.1](#), or automatically based on the power mode of DA9061.

7.7.2 Output Voltage Slewing

To limit in-rush current from the input supply, the buck converters can achieve a new output voltage with controlled ramping. Ramping is achieved by stepping through all the VBUCK values between the old and new settings, at a rate defined by SLEW_RATE. The actual output slew rate, in $\text{mV}/\mu\text{s}$, for a particular buck converter is then defined by the minimum voltage step of that buck and the common step time programmed in SLEW_RATE. During PFM mode, the negative slew rate is load dependent and might be lower than the one mentioned above. An event E_DVC_RDY is triggered when all buck converters have reached their target voltage.

7.7.3 Soft-Start

The buck converter supports two options for starting up. The normal start-up option ramps up the power rail as fast as possible, typically within 1 ms. This implies a high in-rush current. The slow start-up is selected by setting BUCK_SLOWSTART, which increases the start-up time and limits the input current.

7.7.4 Active Discharge

When switching off a buck converter the output rail can be actively discharged. This feature is enabled by setting BUCK_ACTV_DISCHRG. The discharge is implemented by ramping down the output voltage using DVC.

7.7.5 Peak Current Limit

All buck converters feature a programmable current limit (BUCK<x>_ILIM). The current limit protects the inductor and the pass devices from excessive current. If the current limit is exceeded, the buck continues to run normally but the duty cycle is limited.

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7.7.6 Operating Mode

The operating mode of each converter can be set via the buck control (BUCK<x>_MODE) to synchronous (PWM), sleep (PFM), or auto. In auto mode the buck converter switches between PWM and PFM depending on the load current. The current consumption during PWM operation is 10 mA and drops to <math><1 \mu\text{A}</math> in shutdown.

| Note |
|---|
| It is not recommended that the Auto mode transition feature is used under certain operating conditions. Customers wishing to use the Auto mode transition feature should first check with their Dialog FAE. |

In addition, the buck mode can be controlled with the A and B setting. If BUCK<x>_SL_B is set, the buck is forced to SLEEP mode when the B setting is active. Similarly, if BUCK<x>_SL_A is set, the buck is forced to SLEEP mode when the A setting is active.

7.7.7 Half-Current Mode

Buck1 can operate in half-current mode where the quiescent current is reduced by disabling half of the pass devices. As the name implies, enabling this option halves the output current, and therefore, this feature is valuable in applications where quiescent current is critical and full current is not needed. This feature is controlled with BUCK1_FCM. If the bit is asserted (BUCK1_FCM = 1), the buck is in full-current mode and the full current is available. If the bit is de-asserted, the buck is in half-current mode. Operating the buck in full-current mode requires twice as much output capacitance (2 x 47 μF) as the half-current mode (2 x 22 μF).

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7.8 Power Modes

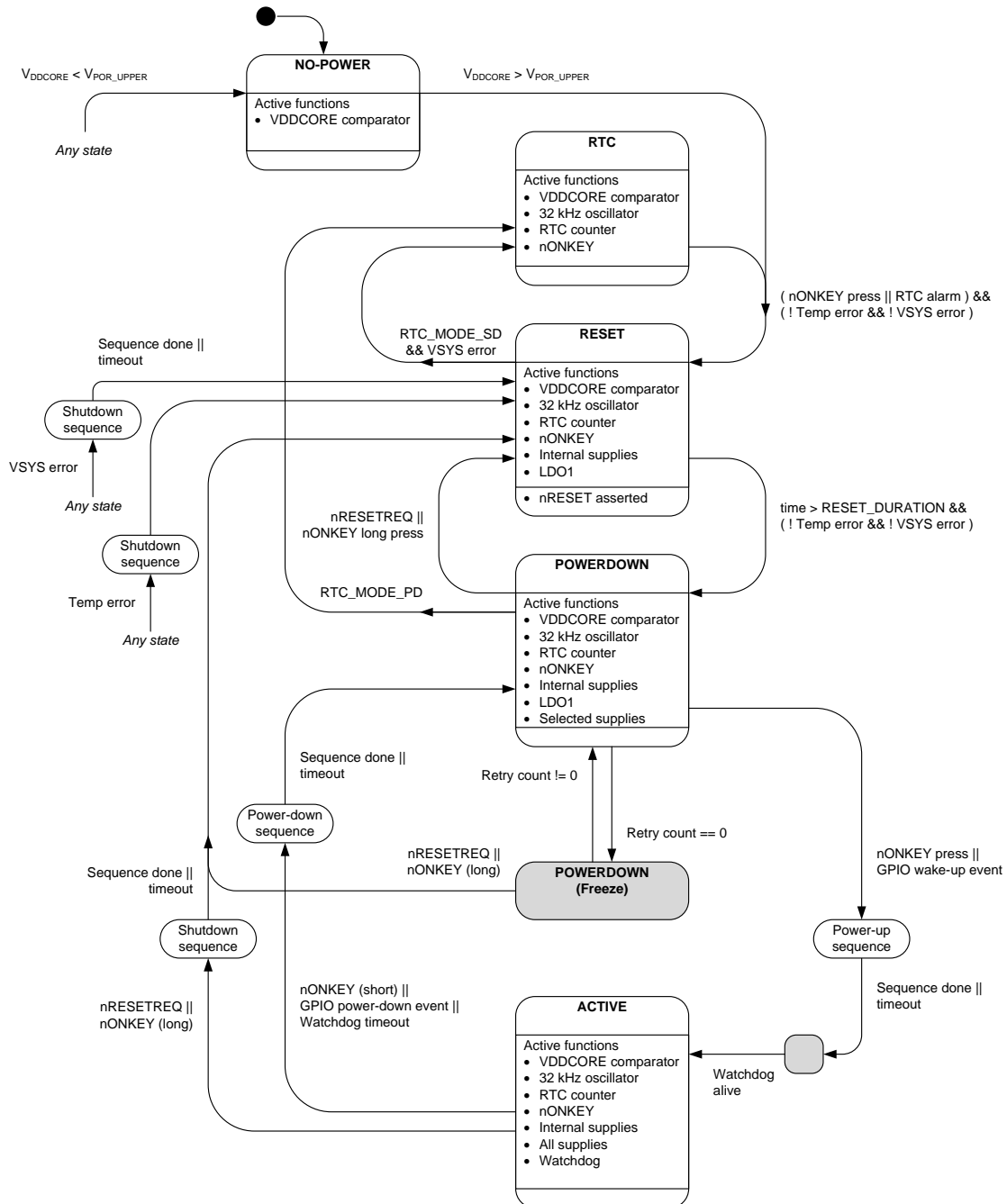


Figure 17: DA9061 Power Modes (State Transition Conditions Follow C-Language Syntax)

7.8.1 NO-POWER Mode

The NO-POWER mode is initial state when powering up the DA9061 for the first time. When the system supply rises above a threshold, DA9061 enters RESET mode.

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7.8.2 RESET Mode

In RESET mode, the internal supplies, and LDO1 (if configured as an always-on supply) are enabled. All other DA9061 supplies are disabled.

DA9061 is in RESET mode whenever a complete application shutdown is required. RESET mode can be triggered by the user, a host processor, or an internal event.

RESET mode can be triggered by the user:

- from a long press of nONKEY (interruptible by host) defined by control SHUT_DELAY
- by pressing a reset switch that is connected to port nRESETREQ (non-interruptible)

RESET mode can be forced from the host processor (non-interruptible):

- by asserting nRESETREQ (falling edge)
- by writing to control SHUTDOWN

DA9061 error conditions that force RESET mode (non-interruptible) are:

- no WATCHDOG write (WDKICK signal assertion) from the host inside the watchdog time window (if watchdog was enabled)
- an under-voltage detected on VSYS ($V_{SYS} < V_{DD_FAULT_LOWER}$)
- an internal junction over-temperature

With the INT_SD_MODE, HOST_SD_MODE and KEY_SD_MODE controls, the shutdown sequences from internal fault, host or user triggered, are individually configured to either implement the reverse timing of the power-up sequence or transfer immediately to the RESET mode by skipping any delay from sequencer or dummy slot timers. For the host to determine the reason for the reset a FAULT_LOG register stores the root cause (either KEY_RESET or NRESETREQ). The host processor resets this register by writing asserted bits with 1.

KEY_SD_MODE = 1 triggers a complete power on reset (POR) (instead of entering RESET mode) after the related keys are pressed extendedly.

If an OTP read is aborted, DA9061 enters RESET mode without an asserted bit inside register FAULT_LOG.

A shutdown sequence to RESET mode will start with the assertion of the nRESET port. After the sequencer completes the power down sequence (sequencer position 0), DA9061 continues to RESET mode with only the following active circuits: LDOCORE (at reduced output voltage 2.2 V), control interfaces and GPIOs, BCD counter, band-gap and over-temperature/VSYS comparators. All regulators, except for LDO1, are automatically disabled to avoid battery drainage. As described in Section 7.1.3, nRESET is always asserted at the beginning of a shutdown sequence to RESET mode, and remains asserted when DA9061 is in RESET mode.

When entering RESET mode, all user and system events are cleared. The DA9061's register configuration will be re-loaded from OTP when leaving the RESET mode (with the exception of control AUTO_BOOT in case of a VDD_START fault).

FAULT_LOG, GP_ID_10 to GP_ID_19 and other non-OTP loaded registers will not be changed when leaving the RESET mode.

Some reset conditions such as writing a 1 to control SHUTDOWN, a watchdog error, or a junction over-temperature will be automatically cleared. Other reset triggers such as asserting nRESETREQ, need to be released to proceed from RESET to POWERDOWN mode. If the application requires regulators to discharge completely before a power-up sequence, a minimum duration of the RESET mode can be selected via RESET_DURATION.

The RESET_DURATION only applies when a PMIC is powered down through the RESET state, such as a result of a SHUTDOWN command, nRESETREQ, or VSYS under-voltage fault. The RESET_DURATION does not apply to a PMIC cold-boot.

If the reset was initiated by a long nONKEY press, initially only KEY_RESET is set and the nIRQ port will be asserted. KEY_RESET signals the host that a shutdown sequence is started. If the host does not then clear KEY_RESET within 1 s by writing a 1 to the related bit in register FAULT_LOG, the

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shutdown sequence will complete. When the reset condition has disappeared, DA9061 requires a supply ($V_{SYS} > V_{DD_FAULT_UPPER}$) that provides enough power to start-up from the POWERDOWN mode.

7.8.3 POWERDOWN Mode

The POWERDOWN mode is a low-power state where most of the regulators are disabled. The transition from active to POWERDOWN mode (and vice versa) is handled by the programmable sequencer. Entry to POWERDOWN mode from ACTIVE mode is triggered by the de-assertion of SYSTEM_EN (either via SYS_EN or register access) or by a short press of nONKEY. The POWERDOWN mode is also passed during start-up and shutdown to RESET mode sequences.

In POWERDOWN mode the internal supplies are enabled, and the control interface and GPIOs are operational.

The power state machine features a retry counter that limits the number of transitions from POWERDOWN to ACTIVE under certain conditions. A watchdog timeout triggers POWERDOWN mode entry, but it does not necessarily clear the conditions that trigger a transition back to the ACTIVE mode. This could cause an endless loop between the ACTIVE and POWERDOWN modes. Therefore, after each watchdog timeout the retry counter is decremented, and after the retry counter reaches zero, DA9061 blocks all wakeup events and stays in POWERDOWN mode. This freeze function can be regarded as a substate of the POWERDOWN mode that is undetectable from outside the DA9061.

Table 25 describes the state transitions with a level-sensitive wakeup and the freeze function.

Table 25: State Transitions with a Level-Sensitive (LS) GPI

| Current state | LS GPI | SYS_EN | PWR_EN | Freeze Note 1 | Next state |
|---------------|--------|--------|--------|------------------|------------|
| POWERDOWN | x | x | x | 1 | POWERDOWN |
| POWERDOWN | 0 | 0 | x | 0 | POWERDOWN |
| POWERDOWN | x | 1 | 0 | 0 | SYSTEM |
| POWERDOWN | x | 1 | 1 | 0 | ACTIVE |
| POWERDOWN | 1 | x | 0 | 0 | SYSTEM |
| POWERDOWN | 1 | x | 1 | 0 | ACTIVE |
| SYSTEM | 0 | 0 | x | x | POWERDOWN |
| SYSTEM | x | 1 | 0 | x | SYSTEM |
| SYSTEM | x | 1 | 1 | x | ACTIVE |
| SYSTEM | 1 | x | 0 | x | SYSTEM |
| SYSTEM | 1 | x | 1 | x | ACTIVE |
| ACTIVE | 0 | 0 | x | x | POWERDOWN |
| ACTIVE | x | 1 | 0 | x | SYSTEM |
| ACTIVE | x | 1 | 1 | x | ACTIVE |
| ACTIVE | 1 | x | 0 | x | SYSTEM |
| ACTIVE | 1 | x | 1 | x | ACTIVE |

Note 1 In this table, Freeze represents the result of the comparison $retry\ count = 0$.

The following events will reset the retry counter and release the state machine from the freeze state:

- De-assertion of all blocked level-sensitive wakeup conditions
- Entry to the RESET mode (over-temperature error, nRESETREQ or long press of nONKEY)

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The freeze operation is illustrated in Figure 18. Once the freeze state is cleared, DA9061 continues operating normally. The freeze function can be enabled in the FREEZE_EN register and the number of retries triggering the freeze can be configured in NFREEZE.

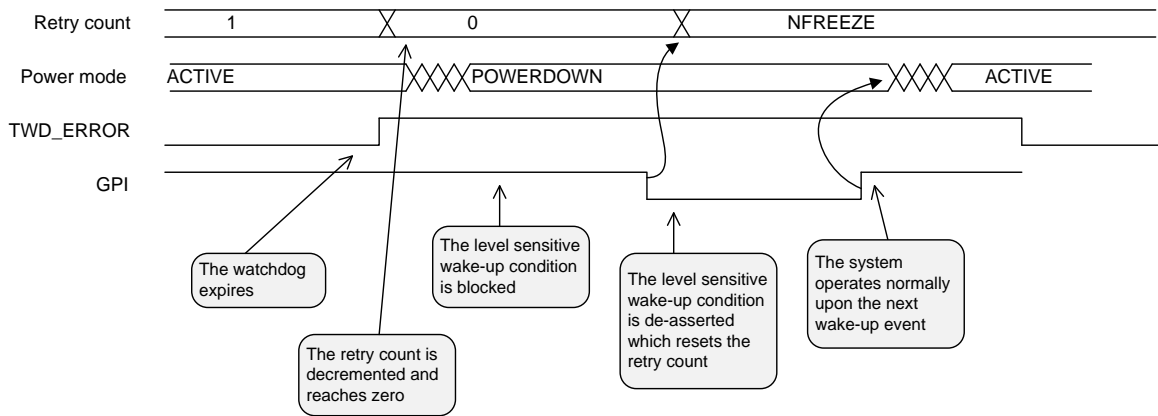


Figure 18: Freeze Function

7.8.4 Power-Up, Power-Down, and Shutdown Sequences

The power-up, power-down, and shutdown sequences, see Figure 17, are handled by the power supply sequencer, see Section 7.9. All power-up sequences are identical, and the power-down sequences mirror the power-up sequences.

The shutdown sequences are also identical to the power-down sequence, but after reaching POWERDOWN mode, the state machine automatically proceeds to RESET mode. The shutdown sequences caused by an internal error or nRESETREQ can be sped up from the INT_SD_MODE and HOST_SD_MODE controls: see Section 7.8.2.

7.8.5 ACTIVE Mode

In the ACTIVE mode, all supplies and functions are active. The transition from POWERDOWN to ACTIVE mode is handled by the programmable sequencer. DA9061 enters ACTIVE mode after the sequence has completed and the watchdog is enabled (if configured to use watchdog).

Status information can be read from the host processor via the 2-wire interface and DA9061 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ).

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7.9 Power Supply Sequencer

DA9061 features a programmable Power Supply Sequencer that handles the system power-up, power-down, and shutdown sequences. The sequencer has a step-up counter, a timer that controls the step period, and a set of comparators that trigger power-on/off events at specific steps of the counter. The structure of the sequencer is depicted in Figure 19.

The sequencer is composed of 16 steps, and the step time can be programmed between 32 μ s and 8.192 ms. The sequencer will step until it reaches a programmable maximum value (MAX_COUNT), whereupon an interrupt is issued. At each step, the sequencer will enable all the functions that are pointing to that particular step.

The power-up and -down sequences cannot be configured separately. When DA9061 is powering down, the sequencer will execute whatever was configured for the power-up sequence but in reverse order. Supplies can also be configured to stay on in POWERDOWN mode. In this case, the sequencer does not disable the regulator but switches to its B-configuration, see Section 7.5.

If any pointer is programmed to a step higher than MAX_COUNT, the function is no longer controlled by the sequencer. Only the regulator control pointers (LDO<x>_STEP, BUCK<x>_STEP) are allowed to point to step 0. Setting any other pointer to step 0, effectively disables that function.

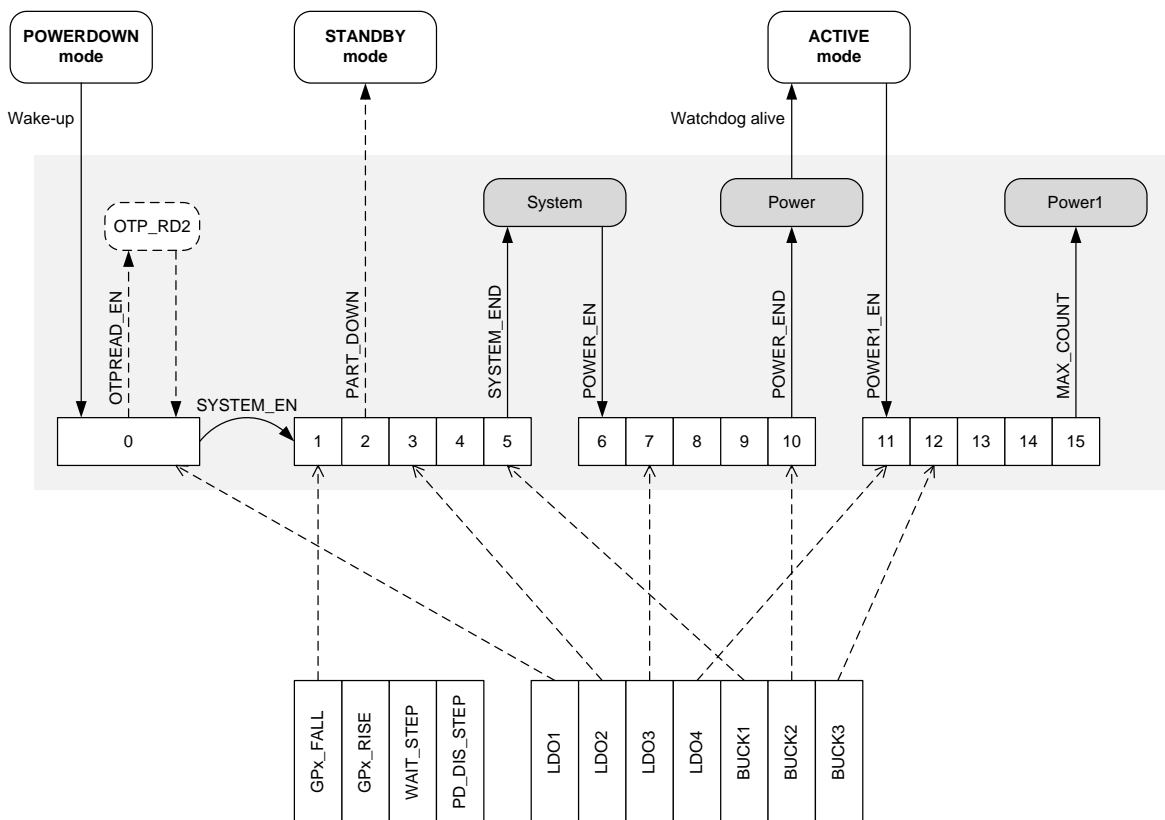


Figure 19: Structure of the Power Supply Sequencer

NOTE

STANDBY mode can only be reached on power-down, not power-up.

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7.9.1 Programmable Slot Delays

The delay between the slots of a sequence is controlled via the programmable value of SEQ_TIME in register SEQ_TIMER. This has a default delay of 128 μ s per slot (min. 32 μ s, max. 8 ms). The delay time between individual supplies can be extended by leaving a consecutive slot(s) with no IDs pointing to it: these are dummy slots. The dummy slots have an independent delay configured by SEQ_DUMMY. These delay times, in register SEQ_TIMER, are (re-)loaded from OTP every time domain SYSTEM begins to power-up. These slot delays also apply to Slot 0.

7.9.2 Sub-Sequences

As illustrated in Figure 19, the sequencer is partitioned into three sub-sequences. These three sub-sequences can be used to define three power modes for the target application and to move between them in a controlled sequence as a response to control signals or register writes.

The first sub-sequence starts from step 0 and ends at a step defined by the SYSTEM_END pointer. After the power-up is triggered, DA9061 performs a partial OTP read (OTP_RD2) if OTPREAD_EN is set. It then waits for control SYSTEM_EN to trigger the first sub-sequence. If SYSTEM_EN is already set in the OTP the first sub-sequence starts automatically after the power-up trigger. Alternatively, SYSTEM_EN can be asserted through the SYS_EN input. When the sequencer reaches the SYSTEM_END step the first sub-sequence is completed and the sequencer starts waiting for control POWER_EN to trigger the second sub-sequence. If POWER_EN is already set in the OTP, the sequencer does not stop after the first sub-sequence. Alternatively, POWER_EN can be asserted through the PWR_EN input or via a register access.

The second sub-sequence starts from the step following SYSTEM_END and stops at a step defined by the POWER_END pointer. When the sequencer reaches the POWER_END step (and the watchdog is active), DA9061 enters ACTIVE mode. The final sub-sequence is triggered by asserting POWER1_EN via a register write. The third sub-sequence starts from the step following POWER_END and stops at a step defined by the MAX_COUNT pointer. If MAX_COUNT points to an earlier step than SYSTEM_END or POWER_END the remaining steps of the sequencer are disabled.

The power-down sequences are executed in reverse order to the power-up sequences. If the power-down sequence is triggered from the ACTIVE mode by de-asserting POWER_EN, the sequencer stops after reversing to the SYSTEM_END step. However, if the power-down sequence is triggered by de-asserting SYSTEM_EN, the sequencer does not stop and reverses back to step 0. Furthermore, if the power-down sequence is triggered by a watchdog timeout, the sequencer reverses to step 0 immediately.

A partial power-down can be achieved by setting control STANDBY. This makes the sequencer stop at the step pointed to by the PART_DOWN pointer. The next power-up will then start from the PART_DOWN step, instead of step 0. The PART_DOWN pointer has to point to a step smaller than the SYSTEM_END pointer.

7.9.3 Regulator Control

Each of DA9061's buck converters and LDOs can be assigned to any of the sequencer steps. In general, when the sequencer reaches a step to which a regulator is assigned, that regulator is enabled by the sequencer. Likewise, when the sequencer reaches the same step on the way down, the regulator is disabled. Multiple supplies can point to the same counter step, however, enabling multiple regulators in the same slot can lead to increased in-rush currents.

In the simplest scheme, the sequencer enables regulators during a power-up, and disables them during a power-down. This functionality is achieved by setting BUCK<x>_AUTO/LDO<x>_AUTO and clearing BUCK<x>_CONF/LDO<x>_CONF. Alternatively, the sequencer can be configured to keep the regulator enabled, but switch between the A and B settings in ACTIVE and POWERDOWN modes. The functionality of the BUCK<x>_AUTO/LDO<x>_AUTO and BUCK<x>_CONF/LDO<x>_CONF controls is summarized in Table 26.

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Table 26: Regulator Control Functionality of the Power Supply Sequencer

| Power-Up (Sequencer Direction Up) | | | | | | |
|---------------------------------------|------|-------------------------|-----|------------------------|-----|---|
| AUTO | CONF | POWERDOWN Mode (Before) | | ACTIVE Mode (After) | | Sequencer Functionality |
| | | EN | SEL | EN | SEL | |
| 0 | 0 | x | x | 0 | 0 | The regulator is disabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated. |
| x | 1 | x | x | 1 | 0 | The regulator is enabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated. |
| 1 | x | x | x | 1 | 0 | |
| Power-Down (Sequencer Direction Down) | | | | | | |
| AUTO | CONF | ACTIVE Mode (Before) | | POWERDOWN Mode (After) | | |
| | | EN | SEL | EN | SEL | |
| x | 0 | x | x | 0 | 0 | The regulator is disabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated. |
| x | 1 | x | x | 1 | 1 | The regulator stays enabled but it is switched to the B-setting (VBUCK<x>_B/VLDO<x>_B). |

Step 0 of the sequencer has a special meaning. If control DEF_SUPPLY is set, the sequencer treats all regulators pointing to step 0 as default supplies. This means that the regulators are enabled automatically when entering the POWERDOWN mode. Regulators assigned to other steps are only enabled after a wakeup condition occurs. Apart from this, step 0 acts the same as steps 1 to 15. If control DEF_SUPPLY = 0, step 0 of the sequencer does not have any affect.

As mentioned in Section 7.6.1, LDO1 can be programmed as an always-on supply. This is achieved by setting controls DEF_SUPPLY, LDO1_CONF, and LDO1_EN in the OTP. In normal operation, when the sequencer moves between ACTIVE and POWERDOWN modes, LDO1 behaves as presented in Table 26. However, if DA9061 moves to the RESET mode, this configuration keeps LDO1 enabled. This is not the case for any other regulator.

7.9.4 GPO Control

Any GPO can be asserted or de-asserted in a sequencer step (GP_RISE<x>_STEP, GP_FALL<x>_STEP). The GPO control is summarized in Table 27. If a GPO is controlled by the sequencer, it is driven to its inactive state when DA9061 is in RESET mode. The GPIO control only works in sequencer steps greater than zero.

Table 27: GPO Control Functionality of the Power Supply Sequencer

| GPIO<x>_MODE | GPO State After Reset | Sequencer Direction | Previous GPO state | GPO Transition at GP_RISE<x> | GPO Transition at GP_FALL<x> |
|-----------------|-----------------------|---------------------|--------------------|------------------------------|------------------------------|
| 0 (active low) | High | Up | High | High to low | - |
| | | | Low | - | Low to high |
| | | Down | High | - | High to low |
| | | | Low | Low to high | - |
| 1 (active high) | Low | Up | High | - | High to low |
| | | | Low | Low to high | - |
| | | Down | High | High to low | - |
| | | | Low | - | Low to high |

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7.9.5 Wait Step

One of the sequencer steps (any step greater than zero) can be configured as a wait step, in which the sequencer stays until an event is detected in the GPI3 input, see Section 7.3.1.2.

NOTE

The E_GPI3 event has to be cleared after the power-up sequence completes. Otherwise, the wait step in the next power-up sequence will be ineffective.

The wait step features an optional 500 ms timeout, which can be used when the wait event never occurs. If the timeout occurs, the steps following the wait step are not executed and a shutdown sequence to RESET mode is triggered. The shutdown reason is signalled with the WAIT_SHUT bit. Alternatively, the wait step can be used as a configurable delay in the sequence (WAIT_MODE, WAIT_TIME).

7.9.6 Power-Down Disable

The PD_DIS_STEP pointer can be used to define a step in the power-up sequence above which a group of functions will be enabled. The functions concerned can be controlled in the PD_DIS register. Similarly, in the power-down sequence, the same groups of functions will be disabled when the sequencer proceeds below the PD_DIS_STEP.

7.10 Junction Temperature Supervision

To protect DA9061 from damage due to excessive power dissipation, the junction temperature is continuously monitored. The monitoring is split into three thresholds T_{WARN} (125 °C), T_{CRIT} (140 °C), and T_{POR} (150 °C).

If the junction temperature rises above the first threshold (T_{WARN}), the event E_TEMP (in register EVENT_B) is asserted. If the event is not masked, this will issue an interrupt. This first level of temperature supervision is intended for non-invasive temperature control, where the necessary measures for cooling the system down are left to the host software.

If the junction temperature increases even further and crosses the second threshold (T_{CRIT}) the temperature error flag TEMP_CRIT (in register FAULT_LOG) is issued and a shutdown sequence to RESET mode is triggered, see Section 7.8.2. The nRESET output is asserted at the beginning of the shutdown sequence. Therefore, the second level of the temperature supervision does not rely on the host software to take counter-measures. The fault flag can be evaluated by the application after the next power up.

There is also a third temperature threshold (T_{POR}) which causes DA9061 to enter RESET mode without any sequencing and stop all functions. This prevents possible permanent damage due to fast temperature increases.

7.11 System Supply Voltage Supervision

Two comparators supervise the system supply V_{SYS}. One is monitoring the under-voltage level (V_{DD_FAULT_LOWER}) and the other is indicating a good system supply (V_{DD_FAULT_UPPER}). The V_{DD_FAULT_LOWER} threshold is OTP configurable and can be set via the VDD_FAULT_ADJ control from 2.5 V to 3.25 V in 50 mV steps. The V_{DD_FAULT_UPPER} threshold is also OTP configurable and can be set via the VDD_HYST_ADJ control from 100 mV to 450 mV higher than the V_{DD_FAULT_LOWER} threshold.

V_{SYS} dropping below the V_{DD_FAULT_UPPER} threshold asserts the event E_VDD_WARN (in register EVENT_B). If the event is not masked, this will issue an interrupt, which can be used by the host processor as an indication to decrease its activity.

If V_{SYS} drops below V_{DD_FAULT_LOWER} for more than 100 ms, the supply error flag VDD_FAULT (in register FAULT_LOG) is asserted and a shutdown sequence to RESET mode is triggered, see Section 7.8.2. The nRESET output is asserted at the beginning of the shutdown sequence. The status can also be reported using a dedicated nVDD_FAULT signal, see Section 7.3.2.1.

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7.12 Internal Oscillator

An internal oscillator provides a nominal 6.0 MHz clock that is divided to 3.0 MHz for the buck converters. The frequency of the internal oscillator is adjusted during the initial start-up sequence of DA9061 to within 5 % of the nominal 6.0 MHz.

Some applications require that the software is able to modify the oscillator frequency at runtime, for example to avoid interference effects caused by harmonics of the buck converter operating frequency. This can be achieved by writing a non-zero value to control OSC_FRQ. This control is a signed 4-bit value where each step changes the frequency by about 1.33 %, which gives a range from -10.65 % (-8) to +9.33 % (+7).

The tolerance of this frequency will affect most absolute timer values and PWM repetition rates.

7.13 Watchdog

The watchdog provides system monitoring functionality. A watchdog timeout triggers shutdown to POWERDOWN mode, signalled in register FAULT_LOG. The watchdog can also be configured to control a secondary reset output in addition to nRESET. This requires that one of the GPIOs is configured as a GPO, controlled by the sequencer. The assertion/de-assertion is used as a reset, and the GPIO is configured as a sequencer controlled GPO. This way, after the watchdog triggers the power-down, the reset output is asserted by the sequencer during the power-down sequence.

Once enabled, the watchdog cannot be stopped and it runs in ACTIVE mode (this feature can be bypassed with an OTP configuration). The source clock of the watchdog is the internally generated slow frequency clock.

After a cold boot, the watchdog is activated when entering ACTIVE mode. This first watchdog kick is required for DA9061 to move to the ACTIVE mode after a cold boot, as illustrated in [Figure 17](#). After the watchdog is activated, the host must kick the watchdog periodically within the watchdog period programmed with the TWDSCALE control. An interrupt can be generated to warn the host processor of the watchdog timeout. The time for the warning interrupt is half of the watchdog period.

The kick can be done by a register write to control WATCHDOG (reg. CONTROL_F) or with the GPIO0 pin configured as a WDKICK input. With control WDG_MODE = 1, the behavior of the WDKICK input is modified so that either a pulse or a permanently asserted input prevents a watchdog timeout. In this mode the parameter tWDMIN is not applicable.

If the host processor fails to feed the watchdog, DA9061 asserts a fault bit and enters POWERDOWN mode. The watchdog timeout can also be configured to assert a reset output. This requires that one of the GPIOs is configured as a reset output and assigned to a power sequencer step, see [Section 7.9](#).

After each watchdog timeout a retry counter is decremented. If the retry counter reaches zero, DA9061 will stay in POWERDOWN mode, as described in [Section 7.8.3](#). The number of allowed retries can be programmed in the NFREEZE control.

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8 Register Map

8.1 Register Page Control

The device register map is larger than the address range directly addressable from the host interface. The page control register provides the higher address bits and control for using the paging mechanism. There are several copies of this register, one per host interface. These copies are mirrored to addresses 0x080, 0x100 and 0x180.

8.2 Overview

Table 28 provides a summary of the registers. A description of each register is provided in [Appendix A: Register Descriptions](#).

Table 28: Register Summary

| Address | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|--------------------------------------|----------------|----------------|-------------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|--|
| Page Control | | | | | | | | | | |
| 0x000 | PAGE_CON | REVERT | WRITE_MODE | PAGE | | | | | | |
| Power Manager Control and Monitoring | | | | | | | | | | |
| 0x001 | STATUS_A | Reserved | | | | DVC_BUSY | Reserved | NONKEY | | |
| 0x002 | STATUS_B | Reserved | | | GPI4 | GPI3 | GPI2 | GPI1 | GPI0 | |
| 0x004 | STATUS_D | Reserved | | | | LDO4_ILIM | LDO3_ILIM | LDO2_ILIM | LDO1_ILIM | |
| 0x005 | FAULT_LOG | WAIT_SHUT | NRESETREQ | KEY_RESET | TEMP_CRIT | VDD_START | VDD_FAULT | POR | TWD_ERROR | |
| IRQ Events | | | | | | | | | | |
| 0x006 | EVENT_A | Reserved | EVENTS_C | EVENTS_B | E_SEQ_RDY | E_WDG_WARN | Reserved | Reserved | E_NONKEY | |
| 0x007 | EVENT_B | E_VDD_WARN | Reserved | E_DVC_RDY | Reserved | E_LDO_LIM | Reserved | E_TEMP | Reserved | |
| 0x008 | EVENT_C | Reserved | | | E_GPI4 | E_GPI3 | E_GPI2 | E_GPI1 | E_GPI0 | |
| IRQ Masks | | | | | | | | | | |
| 0x00A | IRQ_MASK_A | Reserved | | | M_SEQ_RDY | M_WDG_WARN | Reserved | Reserved | M_NONKEY | |
| 0x00B | IRQ_MASK_B | M_VDD_WARN | Reserved | M_DVC_RDY | Reserved | M_LDO_LIM | Reserved | M_TEMP | Reserved | |
| 0x00C | IRQ_MASK_C | Reserved | | | M_GPI4 | M_GPI3 | M_GPI2 | M_GPI1 | M_GPI0 | |
| System Control | | | | | | | | | | |
| 0x00E | CONTROL_A | Reserved | M_POWER1_EN | M_POWER_EN | M_SYSTEM_EN | STANDBY | POWER1_EN | POWER_EN | SYSTEM_EN | |
| 0x00F | CONTROL_B | BUCK_SLOWSTART | NFREEZE | nONKEY_LOCK | | NRES_MODE | FREEZE_EN | WATCHDOG_PD | Reserved | |
| 0x010 | CONTROL_C | DEF_SUPPLY | SLEW_RATE | OTPREAD_EN | | AUTO_BOOT | DEBOUNCING | | | |
| 0x011 | CONTROL_D | Reserved | | | | | TWDSCALE | | | |
| 0x012 | CONTROL_E | V_LOCK | Reserved | | | Reserved | Reserved | Reserved | Reserved | |
| 0x013 | CONTROL_F | Reserved | | | | | WAKE_UP | SHUTDOWN | WATCHDOG | |
| 0x014 | PD_DIS | PMCONT_DIS | Reserved | BBAT_DIS | CLDR_PAUSE | Reserved | PMIF_DIS | Reserved | GPI_DIS | |
| GPIO Control | | | | | | | | | | |
| 0x015 | GPIO_0_1 | GPIO1_WEN | GPIO1_TYPE | GPIO1_PIN | | GPIO0_WEN | GPIO0_TYPE | GPIO0_PIN | | |
| 0x016 | GPIO_2_3 | GPIO3_WEN | GPIO3_TYPE | GPIO3_PIN | | GPIO2_WEN | GPIO2_TYPE | GPIO2_PIN | | |
| 0x017 | GPIO_4 | Reserved | | | | GPIO4_WEN | GPIO4_TYPE | GPIO4_PIN | | |
| 0x01C | GPIO_WKUP_MODE | Reserved | | | GPIO4_WKUP_MODE | GPIO3_WKUP_MODE | GPIO2_WKUP_MODE | GPIO1_WKUP_MODE | GPIO0_WKUP_MODE | |
| 0x01D | GPIO_MODE0_4 | Reserved | | | GPIO4_MODE | GPIO3_MODE | GPIO2_MODE | GPIO1_MODE | GPIO0_MODE | |
| 0x01E | GPIO_OUT0_2 | GPIO2_OUT | | GPIO1_OUT | | | GPIO0_OUT | | | |
| 0x01F | GPIO_OUT3_4 | Reserved | | | GPIO4_OUT | | GPIO3_OUT | | | |
| Power Supply Control | | | | | | | | | | |
| 0x021 | BUCK1_CONT | Reserved | VBUCK1_GPI | | Reserved | BUCK1_CONF | BUCK1_GPI | | BUCK1_EN | |
| 0x022 | BUCK3_CONT | Reserved | VBUCK3_GPI | | Reserved | BUCK3_CONF | BUCK3_GPI | | BUCK3_EN | |

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| Address | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------------------------|-------------|---------------|--------------|--------------|---------------|---------------|------------|----------|------------|--|
| 0x024 | BUCK2_CONT | Reserved | VBUCK2_GPI | | Reserved | BUCK2_CONF | BUCK2_GPI | | BUCK2_EN | |
| 0x026 | LDO1_CONT | LDO1_CONF | VLDO1_GPI | | Reserved | LDO1_PD_DIS | LDO1_GPI | | LDO1_EN | |
| 0x027 | LDO2_CONT | LDO2_CONF | VLDO2_GPI | | Reserved | LDO2_PD_DIS | LDO2_GPI | | LDO2_EN | |
| 0x028 | LDO3_CONT | LDO3_CONF | VLDO3_GPI | | Reserved | LDO3_PD_DIS | LDO3_GPI | | LDO3_EN | |
| 0x029 | LDO4_CONT | LDO4_CONF | VLDO4_GPI | | Reserved | LDO4_PD_DIS | LDO4_GPI | | LDO4_EN | |
| 0x032 | DVC_1 | VLDO4_SEL | VLDO3_SEL | VLDO2_SEL | VLDO1_SEL | VBUCK2_SEL | VBUCK3_SEL | Reserved | VBUCK1_SEL | |
| Power Sequencer | | | | | | | | | | |
| 0x081 | SEQ | NXT_SEQ_START | | | SEQ_POINTER | | | | | |
| 0x082 | SEQ_TIMER | SEQ_DUMMY | | | SEQ_TIME | | | | | |
| 0x083 | ID_2_1 | LDO2_STEP | | | LDO1_STEP | | | | | |
| 0x084 | ID_4_3 | LDO4_STEP | | | LDO3_STEP | | | | | |
| 0x088 | ID_12_11 | PD_DIS_STEP | | | Reserved | | | | | |
| 0x089 | ID_14_13 | Reserved | | | BUCK1_STEP | | | | | |
| 0x08A | ID_16_15 | BUCK2_STEP | | | BUCK3_STEP | | | | | |
| 0x08D | ID_22_21 | GP_FALL1_STEP | | | GP_RISE1_STEP | | | | | |
| 0x08E | ID_24_23 | GP_FALL2_STEP | | | GP_RISE2_STEP | | | | | |
| 0x08F | ID_26_25 | GP_FALL3_STEP | | | GP_RISE3_STEP | | | | | |
| 0x090 | ID_28_27 | GP_FALL4_STEP | | | GP_RISE4_STEP | | | | | |
| 0x091 | ID_30_29 | GP_FALL5_STEP | | | GP_RISE5_STEP | | | | | |
| 0x092 | ID_32_31 | Reserved | | | WAIT_STEP | | | | | |
| 0x095 | SEQ_A | POWER_END | | | SYSTEM_END | | | | | |
| 0x096 | SEQ_B | PART_DOWN | | | MAX_COUNT | | | | | |
| 0x097 | WAIT | WAIT_DIR | | TIME_OUT | WAIT_MODE | WAIT_TIME | | | | |
| 0x099 | RESET | RESET_EVENT | | RESET_TIMER | | | | | | |
| Power Supply Control | | | | | | | | | | |
| 0x09A | BUCK_ILIM_A | Reserved | | | | BUCK2_ILIM | | | | |
| 0x09B | BUCK_ILIM_B | Reserved | | | | BUCK3_ILIM | | | | |
| 0x09C | BUCK_ILIM_C | Reserved | | | | BUCK1_ILIM | | | | |
| 0x09E | BUCK1_CFG | BUCK1_MODE | | BUCK1_PD_DIS | Reserved | | | | Reserved | |
| 0x09F | BUCK3_CFG | BUCK3_MODE | | BUCK3_PD_DIS | Reserved | Reserved | Reserved | | | |
| 0x0A0 | BUCK2_CFG | BUCK2_MODE | | BUCK2_PD_DIS | Reserved | | | | | |
| 0x0A4 | VBUCK1_A | BUCK1_SL_A | VBUCK1_A | | | | | | | |
| 0x0A5 | VBUCK3_A | BUCK3_SL_A | VBUCK3_A | | | | | | | |
| 0x0A7 | VBUCK2_A | BUCK2_SL_A | VBUCK2_A | | | | | | | |
| 0x0A9 | VLDO1_A | LDO1_SL_A | Reserved | VLDO1_A | | | | | | |
| 0x0AA | VLDO2_A | LDO2_SL_A | Reserved | VLDO2_A | | | | | | |
| 0x0AB | VLDO3_A | LDO3_SL_A | Reserved | VLDO3_A | | | | | | |
| 0x0AC | VLDO4_A | LDO4_SL_A | Reserved | VLDO4_A | | | | | | |
| 0x0B5 | VBUCK1_B | BUCK1_SL_B | VBUCK1_B | | | | | | | |
| 0x0B6 | VBUCK3_B | BUCK3_SL_B | VBUCK3_B | | | | | | | |
| 0x0B8 | VBUCK2_B | BUCK2_SL_B | VBUCK2_B | | | | | | | |
| 0x0BA | VLDO1_B | LDO1_SL_B | Reserved | VLDO1_B | | | | | | |
| 0x0BB | VLDO2_B | LDO2_SL_B | Reserved | VLDO2_B | | | | | | |
| 0x0BC | VLDO3_B | LDO3_SL_B | Reserved | VLDO3_B | | | | | | |
| 0x0BD | VLDO4_B | LDO4_SL_B | Reserved | VLDO4_B | | | | | | |
| Customer Trim and Configuration | | | | | | | | | | |
| 0x105 | INTERFACE | IF_BASE_ADDR | | | Reserved | | | | | |
| 0x106 | CONFIG_A | Reserved | PM_IF_HSM | PM_IF_FMP | PM_IF_V | IRQ_TYPE | PM_O_TYPE | Reserved | PM_I_V | |
| 0x107 | CONFIG_B | Reserved | VDD_HYST_ADJ | | | VDD_FAULT_ADJ | | | | |

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| Address | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|--------------------------|-------------|------------|---------------|----------------|---------------|---------------|--------------------|------------|------------|--|
| 0x108 | CONFIG_C | Reserved | BUCK2_CLK_INV | Reserved | BUCK3_CLK_INV | BUCK1_CLK_INV | BUCK_ACTV_DISC_HRG | Reserved | | |
| 0x109 | CONFIG_D | Reserved | | FORCE_RESET | Reserved | | SYSTEM_EN_RD | NIRQ_MODE | GPLV | |
| 0x10A | CONFIG_E | Reserved | | | BUCK2_AUTO | Reserved | BUCK3_AUTO | Reserved | BUCK1_AUTO | |
| 0x10C | CONFIG_G | Reserved | | | | LDO4_AUTO | LDO3_AUTO | LDO2_AUTO | LDO1_AUTO | |
| 0x10D | CONFIG_H | Reserved | BUCK1_FCM | Reserved | Reserved | Reserved | Reserved | | | |
| 0x10E | CONFIG_I | LDO_SD | INT_SD_MODE | HOST_SD_MODE | KEY_SD_MODE | WATCHDOG_S D | nONKEY_SD | NONKEY_PIN | | |
| 0x10F | CONFIG_J | IF_RESET | TWOWIRE_TO | RESET_DURATION | | SHUT_DELAY | | KEY_DELAY | | |
| 0x110 | CONFIG_K | Reserved | | | GPIO4_PUPD | GPIO3_PUPD | GPIO2_PUPD | GPIO1_PUPD | GPIO0_PUPD | |
| 0x112 | CONFIG_M | OSC_FRQ | | | | WDG_MODE | Reserved | Reserved | Reserved | |
| Customer Device Specific | | | | | | | | | | |
| 0x121 | GP_ID_0 | GP_0 | | | | | | | | |
| 0x122 | GP_ID_1 | GP_1 | | | | | | | | |
| 0x123 | GP_ID_2 | GP_2 | | | | | | | | |
| 0x124 | GP_ID_3 | GP_3 | | | | | | | | |
| 0x125 | GP_ID_4 | GP_4 | | | | | | | | |
| 0x126 | GP_ID_5 | GP_5 | | | | | | | | |
| 0x127 | GP_ID_6 | GP_6 | | | | | | | | |
| 0x128 | GP_ID_7 | GP_7 | | | | | | | | |
| 0x129 | GP_ID_8 | GP_8 | | | | | | | | |
| 0x12A | GP_ID_9 | GP_9 | | | | | | | | |
| 0x12B | GP_ID_10 | GP_10 | | | | | | | | |
| 0x12C | GP_ID_11 | GP_11 | | | | | | | | |
| 0x12D | GP_ID_12 | GP_12 | | | | | | | | |
| 0x12E | GP_ID_13 | GP_13 | | | | | | | | |
| 0x12F | GP_ID_14 | GP_14 | | | | | | | | |
| 0x130 | GP_ID_15 | GP_15 | | | | | | | | |
| 0x131 | GP_ID_16 | GP_16 | | | | | | | | |
| 0x132 | GP_ID_17 | GP_17 | | | | | | | | |
| 0x133 | GP_ID_18 | GP_18 | | | | | | | | |
| 0x134 | GP_ID_19 | GP_19 | | | | | | | | |
| 0x181 | DEVICE_ID | DEV_ID | | | | | | | | |
| 0x182 | VARIANT_ID | MRC | | | | VRC | | | | |
| 0x183 | CUSTOMER_ID | CUST_ID | | | | | | | | |
| 0x184 | CONFIG_ID | CONFIG_REV | | | | | | | | |

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9 Application Information

9.1 Component Selection

The following recommended components are examples selected from requirements of a typical application. The final component selection will be dependent on the specific application. The electrical characteristics (for example, supported voltage/current range) have to be cross-checked and component types may need to be adapted from the individual needs of the target circuitry.

9.1.1 Resistors

Table 29: Recommended Resistors

| Pin | Value | Tol. | Size (mm) | Rating (mW) | Part |
|------|--------|------|-----------|-------------|------------------------|
| IREF | 200 kΩ | ±1% | 1005 | 100 | Panasonic ERJ2RKF2003x |

9.1.2 Capacitors

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially ones with high capacitance and small size, the DC bias characteristic has to be taken into account.

On the VSYS main supply rail, a minimum distributed capacitance of 40 μF (actual capacitance after voltage and temperature derating) is required.

Buck input capacitors should be within 1.5 mm distance from the supply pin, and the output capacitor should be close to the inductor.

Table 30: Recommended Capacitors

| Pin | Value | Tol. (%) | Size (mm) | Height (mm) | Temp. Char. | Rating (V) | Part |
|-------------------------------|-----------|----------|-----------|-------------|-------------|------------|---------------------|
| VLDO1 | 1 μF | ±10 | 1005 | 0.55 | X5R | 10 | GRM155R61A105KE15 |
| VLDOx | 2.2 μF | ±20 | 1005 | 0.55 | X5R | 10 | GRM155R60J225ME95# |
| VBUCK2 IOUT ≤ 1.5 A | 2 x 22 μF | ±20 | 2012 | 0.95 | X5R | 6.3 | GRM219R60J226M*** |
| | | ±20 | 1005 | 0.5 | X5R | 4.0 | CL05A226MR5NZNC |
| VBUCK2 IOUT > 1.5 A | 2 x 47 μF | ±20 | 2012 | 0.95 | X5R | 4.0 | GRM219R60G476M*** |
| | | ±20 | 1608 | 0.8 | X5R | 4.0 | CL10A476MR8NZN |
| VBUCK3 | 2 x 22 μF | ±20 | 1608 | 1 | X5R | 6.3 | GRM188R60J226MEA0 |
| | | ±20 | 1005 | 0.5 | X5R | 4.0 | CL05A226MR5NZNC |
| VBUCK1 (half-current mode) | 2 x 22 μF | ±20 | 1608 | 1 | X5R | 6.3 | GRM188R60J226MEA0 |
| | | ±20 | 1005 | 0.5 | X5R | 4.0 | CL05A226MR5NZNC |
| VBUCK1 (full-current mode) | 2 x 47 μF | ±20 | 2012 | 0.95 | X5R | 4.0 | GRM219R60G476M***61 |
| | | ±20 | 1608 | 0.8 | X5R | 4.0 | CL10A476MR8NZN |
| VSYS | 1 x 1 μF | ±10 | 1005 | 0.5 | X5R | 10 | GRM155R61A105KE15D |
| VDD_BUCKx | 2 x 22 μF | ±20 | 2012 | 1.25 | X5R | 10 | LMK212BJ226MG-T |
| | 4 x 10 μF | ±20 | 1005 | 0.5 | X5R | 10 | GRM155R61A106ME21 |
| VDD_LDO2 | 1 x 1 μF | ±10 | 1005 | 0.5 | X5R | 10 | GRM155R61A105KE15D |
| VDD_LDO34 | 1 x 1 μF | ±10 | 1005 | 0.5 | X5R | 10 | GRM155R61A105KE15D |
| VDDCORE | 2.2 μF | ±20 | 1005 | 0.55 | X5R | 6.3 | GRM155R60J225ME95# |

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| Pin | Value | Tol. (%) | Size (mm) | Height (mm) | Temp. Char. | Rating (V) | Part |
|------|--------|----------|-----------|-------------|-------------|------------|-------------------|
| VREF | 220 nF | ±15% | 1005 | 0.5 | X5R | 16 | GRM155R71C224KA12 |

9.1.3 Inductors

Inductors should be selected based upon the following parameters:

- I_{SAT} specifies the current causing a reduction in the inductance by a specific amount, typically 30 %
- I_{RMS} specifies the current causing a temperature rise of a specific amount
- DC resistance (DCR) is critical for converter efficiency and should be therefore minimized.
- ESR at the buck switching frequency is critical to converter efficiency in PFM mode and should be therefore minimized.

Inductance is given in [Table 31](#).

Table 31: Recommended Inductors

| Buck | Value | I_{SAT} (A) | I_{RMS} (A) | DCR (Typ. mΩ) | Size (W×L×H mm) | Part |
|---|-------|---------------|---------------|-------------------------|-----------------|---------------------------------|
| Buck1 (half-current mode), Buck2, Buck3 | 1 μH | 2.7 | 2.3 | 55 | 2.0×1.6×1.0 | Toko 1285AS-H-1R0M |
| | | 2.65 | 2.45 | 60 | 2.0×1.6×1.0 | Tayo Yuden MAKK2016T1R0M |
| | | 2.9 | 2.2 | 60 | 2.0×1.6×1.0 | TDK TFM201610A-1R0M |
| Buck1 (full-current mode) | 1 μH | 3.4 | 3 | 60 | 2.5×2.0×1.0 | Toko1269AS-H-1R0M |
| | | 3.6 | 3.1 | 45 | 2.5×2.0×1.2 | Tayo Yuden MAMK2520T1R0M |
| | | 3.8 | 3.5 | 45 | 2.5×2.0×1.2 | Toko 1239AS-H-1R0M |
| | | 3.9 | 3.1 | 48 | 3.2×2.5×1.0 | Toko1276AS-H-1R0M |
| | | 4.7 | 4.1 | 35 | 2.5×2.0×1.2 | TDK TFM252012ALMA1R0MT AA |
| | | 3.35 | 2.5 | 52 | 3.0×3.0×1.2 | Cyntec PST031B-1R0MS |
| | | 4.9 | 7.9 | 18.5 | 3.5×3.5×1.5 | Coilcraft XGL3515-102ME |
| 8.8 | 12 | 8.2 | 4.0×4.0×2.1 | Coilcraft XGL4020-102ME | | |

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9.2 PCB Layout

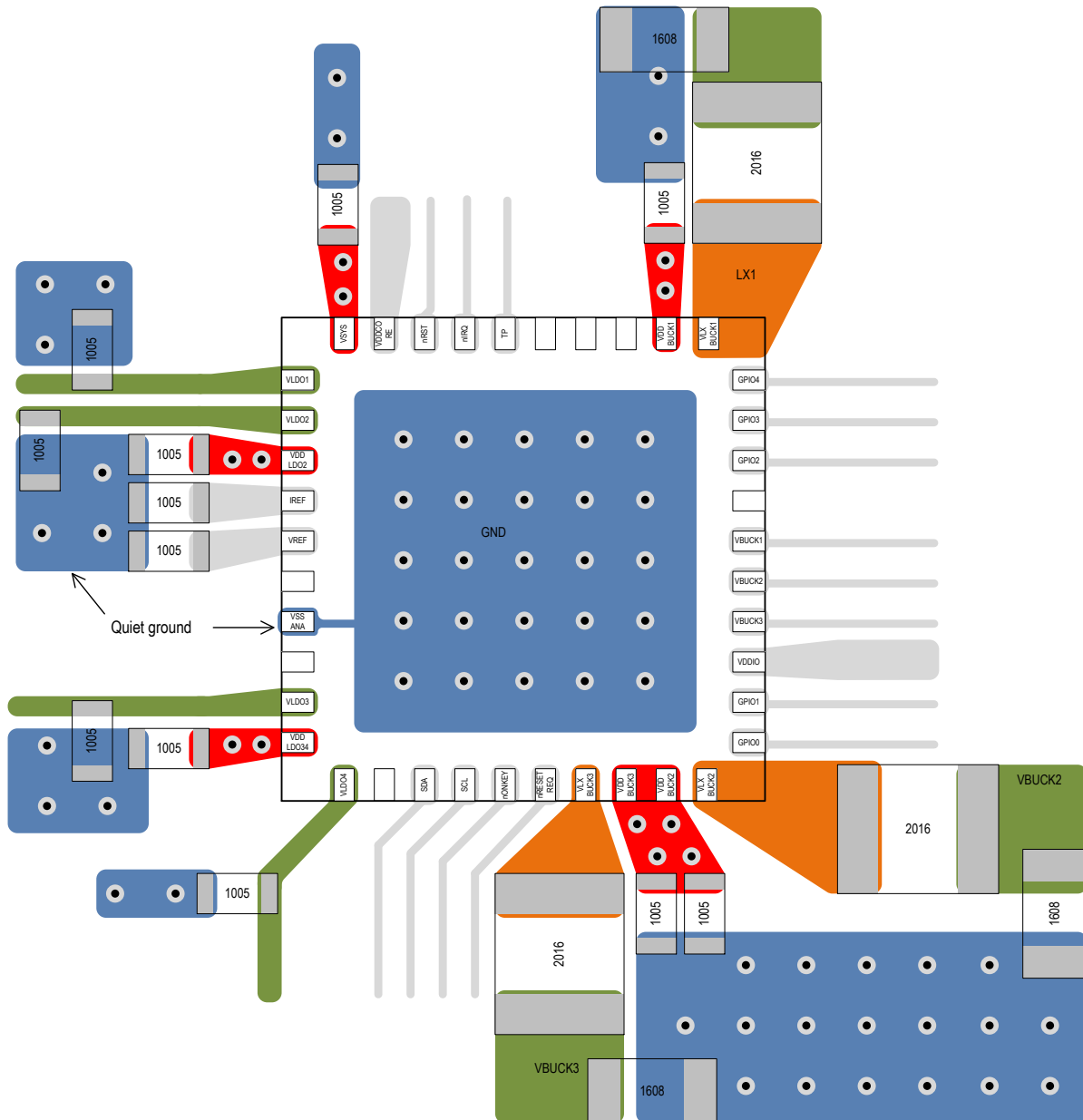


Figure 20: PCB Layout for DA9061

9.2.1 General Recommendations

Appropriate trace width and quantity of vias should be used for all power supply paths.

Too high trace resistances can prevent the system from achieving the best performance, for example, the efficiency and the current ratings of switching converters might be degraded. Furthermore, the PCB may be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.

Special care must be taken with the DA9061 pad connections. The traces connecting the pads should be of the same width as the pads and they should become wider as soon as possible.

It is recommended to create a separate quiet ground to which the VREF capacitor, IREF resistor, and the crystal capacitors are connected. The PCB layout should ensure these component grounds are kept quiet, that is, they should be separated from the main ground return path for the noisy power

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ground. The quiet ground can then be connected to the main ground at the paddle, as shown in [Figure 20](#).

All traces carrying high discontinuous currents should be kept as short as possible.

Noise sensitive analog signals, such as feedback lines or crystal connections, should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation or shielding with quiet signals or ground traces.

9.2.2 LDOs and Switched Mode Supplies

The placement of the distributed capacitors on the VSYS rail must ensure that all VDD inputs and VSYS are connected to a bypass capacitor close to the pad. It is recommended placing at least two 1 μ F capacitors close to the VDD_LDOx pads and at least one 10 μ F close to the VDD_BUCKx pads.

Using a local power plane underneath the device for VSYS might be considered.

Transient current loops in the area of the switching converters should be minimized.

The common references (IREF, VREF) should be placed close to the device and cross-coupling to any noisy digital or analog trace must be avoided.

Output capacitors of the LDOs can be placed close to the input pins of the supplied devices (remote from the DA9061).

Care must be taken with trace routing to ensure that no current is carried on feedback lines of the buck output voltages (VBUCK<x>).

The inductor placement is less critical since parasitic inductances have negligible effect.

9.2.3 Optimizing Thermal Performance

DA9061 features a ground paddle which should be connected with as many vias as possible to the PCB's main ground plane in order to achieve good thermal performance.

Solder mask openings for the landing pads must be arranged to prohibit solder flowing into vias.

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10 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. The “xx” represents a placeholder for the specific OTP variant. For details and availability, please consult Dialog’s [website](#) or your local sales representative.

Table 32: Ordering Information

| Part Number | Package (mm) | Package Description | MOQ |
|--|--------------------|---------------------|-----------------|
| Consumer / Industrial: 25 °C production testing | | | |
| DA9061-xxAM1 | QFN40, 6 mm x 6 mm | Tray, 490 pcs | 14 Trays - 6860 |
| DA9061-xxAM2, Note 1 | QFN40, 6 mm x 6 mm | T&R, 4000 pcs | |
| DA9061-xxAMC | QFN40, 6 mm x 6 mm | T&R, 1100 pcs | 6 Reels, - 6600 |

Note 1 Large reel sizes are no longer supported, contact sales for further information

11 Package Marking

| Package Marking | | |
|--|-----------------|----------------------------|
| A1 Corner > | Marking Content | Format |
| 1st | | Orientation |
| 2nd | | Logo |
| 3rd | | Part No. |
| 4th | | OTP/Silicon Version/Option |
| 5th | | Date Code |
| Date Code Format: yy = Year, ww = Week, zzzz = Traceability | | |
| xx identifies the OTP Variant, vv may be used to show the silicon version. | | |
| -A and -AT optionally indicate the Automotive and Automotive high temp test options. | | |

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Appendix A Register Descriptions

This appendix describes the registers summarized in Section 8. In the following tables, if the description does not explicitly list behaviors for 0 and 1, then the description applies to 1 only.

A.1 PAGE 0

A.1.1 Page Control

Table 33: PAGE_CON (0x000)

| Field | Bit | Type | Description |
|-----------------|-----|------|---|
| REVERT | 7:7 | R/W | 0: PAGE switches the register page until rewritten. 1: PAGE reverts to 0 after one access. |
| WRITE_MODE | 6:6 | R/W | 2-wire sequential write style. 0: Write data to consecutive addresses 1: Write data to random addresses using address/data pairs |
| <i>Reserved</i> | 5:2 | R/W | <i>Reserved</i> |
| PAGE | 1:0 | R/W | The top 2 bits of the register address. 00: Selects register space 0x00 to 0x7F 01: Selects register space 0x80 to 0xFF 10: Selects register space 0x100 to 0x17F 11: Selects register space 0x180 to 0x1FF |

The device register map is larger than the address range directly addressable from the host interface. The page control register provides the higher address bits and control for using the paging mechanism. There are several copies of this register which are mirrored to addresses 0x080, 0x100 and 0x180.

A.1.2 Power Manager Control and Monitoring

Table 34: STATUS_A (0x001)

| Field | Bit | Type | Description |
|----------|-----|------|--|
| Reserved | 7:3 | R | Reserved |
| DVC_BUSY | 2:2 | R | One or more DVC capable supplies are ramping |
| Reserved | 1:1 | R | Reserved |
| NONKEY | 0:0 | R | |

Table 35: STATUS_B (0x002)

| Field | Bit | Type | Description |
|----------|-----|------|-------------|
| Reserved | 7:5 | R | Reserved |
| GPI4 | 4:4 | R | GPI4 level |
| GPI3 | 3:3 | R | GPI3 level |
| GPI2 | 2:2 | R | GPI2 level |
| GPI1 | 1:1 | R | GPI1 level |
| GPI0 | 0:0 | R | GPI0 level |

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Table 36: STATUS_D (0x004)

| Field | Bit | Type | Description |
|-----------|-----|------|-----------------------------|
| Reserved | 7:4 | R | Reserved |
| LDO4_ILIM | 3:3 | R | LDO4 over-current indicator |
| LDO3_ILIM | 2:2 | R | LDO3 over-current indicator |
| LDO2_ILIM | 1:1 | R | LDO2 over-current indicator |
| LDO1_ILIM | 0:0 | R | LDO1 over-current indicator |

Table 37: FAULT_LOG (0x005)

| Field | Bit | Type | Description |
|-----------|-----|-----------------------------|---|
| WAIT_SHUT | 7:7 | R Note 1 | Power-down due to sequencer WAIT_STEP timeout, see Section 7.9.5. |
| NRESETREQ | 6:6 | R Note 1 | Power-down due to nRESETREQ pin or control SHUTDOWN. |
| KEY_RESET | 5:5 | R Note 1 | Power-down due to nONKEY. |
| TEMP_CRIT | 4:4 | R Note 1 | Junction over-temperature |
| VDD_START | 3:3 | R Note 1 | Power-down due to VSYS under-voltage before or within 16 s after release of nRESET. |
| VDD_FAULT | 2:2 | R Note 1 | Power-down due to VSYS under-voltage ($V_{SYS} < V_{DD_FAULT_LOWER}$) |
| POR | 1:1 | R Note 1 | DA9061 starts up from NO-POWER. |
| TWD_ERROR | 0:0 | R Note 1 | Watchdog timeout |

Note 1 Cleared from the host by writing back the read value.

A.1.3 IRQ Events

Table 38: EVENT_A (0x006)

| Field | Bit | Type | Description |
|------------|-----|-----------------------------|--------------------------------------|
| Reserved | 7:7 | R | Reserved |
| EVENTS_C | 6:6 | R | Event in register EVENT_C is active. |
| EVENTS_B | 5:5 | R | Event in register EVENT_B is active. |
| E_SEQ_RDY | 4:4 | R Note 1 | Sequencer reached final position. |
| E_WDG_WARN | 3:3 | R Note 1 | Watchdog timeout warning |
| Reserved | 2:1 | | Reserved |
| E_NONKEY | 0:0 | R Note 1 | nONKEY event |

Note 1 Cleared from the host by writing back the read value.

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Table 39: EVENT_B (0x007)

| Field | Bit | Type | Description |
|------------|-----|-----------------------------|---|
| E_VDD_WARN | 7:7 | R Note 1 | VSYS under-voltage ($V_{SYS} \leq V_{DD_FAULT_UPPER}$). |
| Reserved | 6:6 | R | Reserved |
| E_DVC_RDY | 5:5 | R Note 1 | All supplies have finished DVC ramping. |
| Reserved | 4:4 | R | Reserved |
| E_LDO_LIM | 3:3 | R Note 1 | Any LDO over-current |
| Reserved | 2:2 | R | Reserved |
| E_TEMP | 1:1 | R Note 1 | Junction over-temperature ($T_J > T_{WARN}$) |
| Reserved | 0:0 | | Reserved |

Note 1 Cleared from the host by writing back the read value.

Table 40: EVENT_C (0x008)

| Field | Bit | Type | Description |
|----------|-----|-----------------------------|-------------|
| Reserved | 7:5 | R | Reserved |
| E_GPI4 | 4:4 | R Note 1 | GPI4 event |
| E_GPI3 | 3:3 | R Note 1 | GPI3 event |
| E_GPI2 | 2:2 | R Note 1 | GPI2 event |
| E_GPI1 | 1:1 | R Note 1 | GPI1 event |
| E_GPI0 | 0:0 | R Note 1 | GPI0event |

Note 1 Cleared from the host by writing back the read value.

A.1.4 IRQ Masks

Table 41: IRQ_MASK_A (0x00A)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:5 | | Reserved |
| M_SEQ_RDY | 4:4 | R/W | IRQ mask for sequencer final position indication (E_SEQ_RDY) |
| M_WDG_WARN | 3:3 | R/W | IRQ mask for watchdog timeout warning (E_WDG_WARN) |
| Reserved | 2:1 | | Reserved |
| M_NONKEY | 0:0 | R/W | IRQ mask for nONKEY event (E_NONKEY) |

Table 42: IRQ_MASK_B (0x00B)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| M_VDD_WARN | 7:7 | R/W | IRQ mask for under-voltage event (E_VDD_WARN) $V_{SYS} < V_{DD_FAULT_UPPER}$ |

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| | | | |
|-----------|-----|-----|---|
| Reserved | 6:6 | | Reserved |
| M_DVC_RDY | 5:5 | R/W | All supplies have finished DVC ramping. |
| Reserved | 4:4 | | Reserved |
| M_LDO_LIM | 3:3 | R/W | IRQ mask for LDO over-current event (E_LDO_LIM) |
| Reserved | 2:2 | | Reserved |
| M_TEMP | 1:1 | R/W | IRQ mask for junction over-temperature event (E_TEMP) |
| Reserved | 0:0 | | Reserved |

Table 43: IRQ_MASK_C (0x00C)

| Field | Bit | Type | Description |
|----------|-----|------|----------------------------------|
| Reserved | 7:5 | | Reserved |
| M_GPI4 | 4:4 | R/W | IRQ mask for GPI4 event (E_GPI4) |
| M_GPI3 | 3:3 | R/W | IRQ mask for GPI3 event (E_GPI3) |
| M_GPI2 | 2:2 | R/W | IRQ mask for GPI2 event (E_GPI2) |
| M_GPI1 | 1:1 | R/W | IRQ mask for GPI1 event (E_GPI1) |
| M_GPI0 | 0:0 | R/W | IRQ mask for GPI0 event (E_GPI0) |

A.1.5 System Control

Table 44: CONTROL_A (0x00E)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| Reserved | 7:7 | | Reserved |
| M_POWER1_EN | 6:6 | R/W | Write mask for POWER1_EN |
| M_POWER_EN | 5:5 | R/W | Write mask for POWER_EN |
| M_SYSTEM_EN | 4:4 | R/W | Write mask for SYSTEM_EN |
| STANDBY | 3:3 | R/W | Clearing control SYSTEM_EN or releasing SYS_EN (GPIO4 alternate function) or a long press of nONKEY will: 0: Power-down to slot 0. 1: Power-down as far as defined by the PART_DOWN pointer. |
| POWER1_EN | 2:2 | R/W | Target status of power domain POWER1. Bus write masked with M_POWER1_EN. |
| POWER_EN | 1:1 | R/W | Target status of power domain POWER. Bus write masked with M_POWER_EN. |
| SYSTEM_EN | 0:0 | R/W | Target status of power domain SYSTEM. Bus write masked with M_SYSTEM_EN. |

Table 45: CONTROL_B (0x00F)

| Field | Bit | Type | Description |
|----------------|-----|------|---|
| BUCK_SLOWSTART | 7:7 | R/W | Enable buck slow start (reduced inrush current; increased start-up time). |
| NFREEZE | 6:5 | R/W | Block all wakeups after NFREEZE watchdog restart trials. |
| nONKEY_LOCK | 4:4 | R/W | 0: normal POWERDOWN mode 1: Power-down controlled by KEY_DELAY |

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| | | | |
|-------------|-----|-----|---|
| NRES_MODE | 3:3 | R/W | If powering down / up: 0: Keep nRESET not asserted 1: Assert / clear nRESET when entering / leaving POWERDOWN |
| FREEZE_EN | 2:2 | R/W | Enable watchdog restart limit NFREEZE. |
| WATCHDOG_PD | 1:1 | R/W | Watchdog timer is on (1) / off (0) in POWERDOWN mode. |
| Reserved | 0:0 | | Reserved |

Table 46: CONTROL_C (0x010)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| DEF_SUPPLY | 7:7 | R/W | 1: OTP enables / disables all supplies (except LDOCORE) when sequencer enters slot 0. |
| SLEW_RATE | 6:5 | R/W | Buck DVC slew rate step width [10 mV/step (20 mV/step for Buck2)] 00: 4 μ s for Buck1, Buck3; 8 μ s for Buck2 01: 2 μ s for Buck1, Buck3; 4 μ s for Buck2 10: 1 μ s for Buck1, Buck3; 2 μ s for Buck2 11: 0.5 μ s for Buck1, Buck3; 1 μ s for Buck2 |
| OTPREAD_EN | 4:4 | R/W | When leaving POWERDOWN mode supplies are configured from OTP. |
| AUTO_BOOT | 3:3 | R/W | After progressing from RESET mode the sequencer... 0: ... requires a wakeup event to start-up. 1: ... starts up automatically. |
| DEBOUNCING | 2:0 | R/W | GPI, nONKEY and nRESETREQ debounce time 000: no debouncing 001: 0.1 ms 010: 1.0 ms 011: 10.24 ms 100: 51.2 ms 101: 256 ms 110: 512 ms 111: 1024 ms |

Table 47: CONTROL_D (0x011)

| Field | Bit | Type | Description |
|----------|-----|------|--|
| Reserved | 7:3 | | Reserved |
| TWDSCALE | 2:0 | R/W | Watchdog timeout scaling 0: Watchdog disabled Other: Timeout = 2.048 * 2 ^(TWDSCALE-1) s |

Table 48: CONTROL_E (0x012)

| Field | Bit | Type | Description |
|----------|-----|------|---|
| V_LOCK | 7:7 | R/W | Prevent host from writing to registers 0x81 - 0x120 except 0x100. |
| Reserved | 6:0 | | Reserved |

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Table 49: CONTROL_F (0x013)

| Field | Bit | Type | Description |
|----------|-----|------|---|
| Reserved | 7:3 | | Reserved |
| WAKE_UP | 2:2 | R/W | Wake-up from POWERDOWN mode. Cleared automatically. |
| SHUTDOWN | 1:1 | R/W | Power down to RESET mode. Cleared automatically. |
| WATCHDOG | 0:0 | R/W | Reset watchdog timer. Cleared automatically. |

Table 50: PD_DIS (0x014)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| PMCONT_DIS | 7:7 | R/W | Disable SYS_EN, PWR_EN and PWR1_EN in POWERDOWN mode. |
| Reserved | 6:5 | | Reserved |
| CLDR_PAUSE | 4:4 | R/W | Disable calendar update in POWERDOWN mode. |
| Reserved | 3:3 | | Reserved |
| PMIF_DIS | 2:2 | R/W | Disable 2-wire interface in POWERDOWN mode. |
| Reserved | 1:1 | | Reserved |
| GPI_DIS | 0:0 | R/W | Disable E_GPI<x> events in POWERDOWN mode. |

A.1.6 GPIO Control

Table 51: GPIO_0_1 (0x015)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| GPIO1_WEN | 7:7 | R/W | 0: Passive-to-active transition triggers wakeup. 1: No wakeup |
| GPIO1_TYPE | 6:6 | R/W | GPI: active high (1) / low (0) |
| GPIO1_PIN | 5:4 | R/W | Function of GPIO1 pin (see GPIO1_OUT if output) 00: Reserved 01: Input (opt. regul. HW ctrl.) 10: Output (open-drain) 11: Output (push-pull) |
| GPIO0_WEN | 3:3 | R/W | 0: Passive-to-active transition triggers wakeup. 1: No wakeup |
| GPIO0_TYPE | 2:2 | R/W | GPI: active high (1) / low (0) |
| GPIO0_PIN | 1:0 | R/W | Function of GPIO0 pin (see GPIO0_OUT if output) 00: Watchdog trigger input 01: Input 10: Output (open-drain) 11: Output (push-pull) |

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Table 52: GPIO_2_3 (0x016)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| GPIO3_WEN | 7:7 | R/W | 0: Passive-to-active transition triggers wakeup. 1: No wakeup |
| GPIO3_TYPE | 6:6 | R/W | GPI: active high (1) / low (0) |
| GPIO3_PIN | 5:4 | R/W | Function of GPIO3 pin (see GPIO3_OUT if output) 00: Reserved 01: Input (opt. regul. HW ctrl.) 10: Output (open-drain) 11: Output (push-pull) |
| GPIO2_WEN | 3:3 | R/W | 0: Passive-to-active transition triggers wakeup. 1: No wakeup |
| GPIO2_TYPE | 2:2 | R/W | GPI: active high (1) / low (0) |
| GPIO2_PIN | 1:0 | R/W | Function of GPIO2 pin (see GPIO2_OUT if output) 00: GPI as PWR_EN 01: Input (opt. regul. HW ctrl.) 10: Output (open-drain) 11: nVDD_FAULT (push-pull) |

Table 53: GPIO_4 (0x017)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| Reserved | 7:4 | | Reserved |
| GPIO4_WEN | 3:3 | R/W | 0: Passive-to-active transition triggers wakeup. 1: No wakeup |
| GPIO4_TYPE | 2:2 | R/W | GPI: active high (1) / low (0) |
| GPIO4_PIN | 1:0 | R/W | Function of GPIO pad (see GPIO4_OUT if output) 00: GPI as SYS_EN 01: Input 10: Output (open-drain) 11: Output (push-pull) |

Table 54: GPIO_WKUP_MODE (0x01C)

| Field | Bit | Type | Description |
|-----------------|-----|------|--|
| Reserved | 7:5 | | Reserved |
| GPIO4_WKUP_MODE | 4:4 | R/W | GPI4 wakeup is edge (0) / level (1) sensitive. |
| GPIO3_WKUP_MODE | 3:3 | R/W | GPI3 wakeup is edge (0) / level (1) sensitive. |
| GPIO2_WKUP_MODE | 2:2 | R/W | GPI2 wakeup is edge (0) / level (1) sensitive. |
| GPIO1_WKUP_MODE | 1:1 | R/W | GPI1 wakeup is edge (0) / level (1) sensitive. |
| GPIO0_WKUP_MODE | 0:0 | R/W | GPI0 wakeup is edge (0) / level (1) sensitive. |

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Table 55: GPIO_MODE0_4 (0x01D)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:5 | | Reserved |
| GPIO4_MODE | 4:4 | R/W | Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1) |
| GPIO3_MODE | 3:3 | R/W | Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1) |
| GPIO2_MODE | 2:2 | R/W | Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1) |
| GPIO1_MODE | 1:1 | R/W | Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1) |
| GPIO0_MODE | 0:0 | R/W | Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1) |

Table 56: GPIO_OUT0_2 (0x01E)

| Field | Bit | Type | Description |
|-----------|-----|------|---|
| GPIO2_OUT | 7:6 | R/W | GPIO output function 00: Static value according GPIO2_MODE 01: nVDD_FAULT 10: Reserved 11: Sequencer controlled |
| GPIO1_OUT | 5:3 | R/W | GPIO output function 000: Static value according GPIO1_MODE 001: nVDD_FAULT 010: Reserved 011: Sequencer controlled 100: Forward GPIO 101: Reserved 110: Forward GPI2 111: Forward GPI3 |
| GPIO0_OUT | 2:0 | R/W | GPIO output function 000: Static value according GPIO0_MODE 001: nVDD_FAULT 010: Reserved 011: Sequencer controlled 100: Reserved 101: Forward GPI1 110: Forward GPI2 111: Forward GPI3 |

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Table 57: GPIO_OUT3_4 (0x01F)

| Field | Bit | Type | Description |
|-----------|-----|------|---|
| Reserved | 7:5 | | Reserved |
| GPIO4_OUT | 4:3 | R/W | GPIO output function 00: Static value according GPIO4_MODE 01: nVDD_FAULT 10: Reserved 11: Sequencer controlled |
| GPIO3_OUT | 2:0 | R/W | GPIO output function 000: Static value according GPIO3_MODE 001: nVDD_FAULT 010: Reserved 011: Sequencer controlled 100: Forward GPIO 101: Forward GPI1 110: Forward GPI2 111: Reserved |

A.1.7 Power Supply Control

Table 58: BUCK1_CONT (0x021)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:7 | | Reserved |
| VBUCK1_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VBUCK1_A, active to passive: VBUCK1_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| BUCK1_CONF | 3:3 | R/W | Default supply, or sequenced and on in POWERDOWN |
| BUCK1_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| BUCK1_EN | 0:0 | R/W | Disable (0) / enable (1) the buck (dependent on on/off priority order) |

Table 59: BUCK3_CONT (0x022)

| Field | Bit | Type | Description |
|----------|-----|------|-------------|
| Reserved | 7:7 | | Reserved |

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| Field | Bit | Type | Description |
|------------|-----|------|--|
| VBUCK3_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VBUCK3_A, active to passive: VBUCK3_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| BUCK3_CONF | 3:3 | R/W | Default supply, or sequenced and on in POWERDOWN |
| BUCK3_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| BUCK3_EN | 0:0 | R/W | Disable (0) / enable (1) the buck (dependent on on/off priority order) |

Table 60: BUCK2_CONT (0x024)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:7 | | Reserved |
| VBUCK2_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VBUCK2_A, active to passive: VBUCK2_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| BUCK2_CONF | 3:3 | R/W | Default supply, or sequenced and on in POWERDOWN |
| BUCK2_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| BUCK2_EN | 0:0 | R/W | Disable (0) / enable (1) the buck (dependent on on/off priority order) |

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Table 61: LDO1_CONT (0x026)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| LDO1_CONF | 7:7 | R/W | Default supply, or sequenced and on in POWERDOWN |
| VLDO1_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VLDO1_A, active to passive: VLDO1_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| LDO1_PD_DIS | 3:3 | R/W | 0: Pull-down resistor enabled when the LDO is off 1: Pull-down resistor disabled when the LDO is off |
| LDO1_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| LDO1_EN | 0:0 | R/W | Disable (0) / enable (1) the LDO (dependent on on/off priority order) |

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Table 62: LDO2_CONT (0x027)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| LDO2_CONF | 7:7 | R/W | Default supply, or sequenced and on in POWERDOWN |
| VLDO2_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VLDO2_A, active to passive: VLDO2_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| LDO2_PD_DIS | 3:3 | R/W | 0: Pull-down resistor enabled when the LDO is off 1: Pull-down resistor disabled when the LDO is off |
| LDO2_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| LDO2_EN | 0:0 | R/W | Disable (0) / enable (1) the LDO (dependent on on/off priority order) |

Table 63: LDO3_CONT (0x028)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| LDO3_CONF | 7:7 | R/W | Default supply, or sequenced and on in POWERDOWN |
| VLDO3_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VLDO3_A, active to passive: VLDO3_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| LDO3_PD_DIS | 3:3 | R/W | 0: Pull-down resistor enabled when the LDO is off 1: Pull-down resistor disabled when the LDO is off |
| LDO3_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, active to passive: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| LDO3_EN | 0:0 | R/W | Disable (0) / enable (1) the LDO (dependent on on/off priority order) |

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Table 64: LDO4_CONT (0x029)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| LDO4_CONF | 7:7 | R/W | Default supply, or sequenced and on in POWERDOWN |
| VLDO4_GPI | 6:5 | R/W | Voltage controlling GPI (passive to active transition: VLDO4_A, active to passive: VLDO4_B) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| Reserved | 4:4 | | Reserved |
| LDO4_PD_DIS | 3:3 | R/W | 0: Pull-down resistor enabled when the LDO is off 1: Pull-down resistor disabled when the LDO is off |
| LDO4_GPI | 2:1 | R/W | Enabling GPI (passive to active transition: enable, act. to pas.: disable) 00: Sequencer controlled 01: Select GPI1 10: Select GPI2 11: Select GPI3 |
| LDO4_EN | 0:0 | R/W | Disable (0) / enable (1) the LDO (dependent on on/off priority order) |

Table 65: DVC_1 (0x032)

| Field | Bit | Type | Description |
|------------|-----|------|-------------------------------------|
| VLDO4_SEL | 7:7 | R/W | Select VLDO4_A (0) / VLDO4_B (1). |
| VLDO3_SEL | 6:6 | R/W | Select VLDO3_A (0) / VLDO3_B (1). |
| VLDO2_SEL | 5:5 | R/W | Select VLDO2_A (0) / VLDO2_B (1). |
| VLDO1_SEL | 4:4 | R/W | Select VLDO1_A (0) / VLDO1_B (1). |
| VBUCK2_SEL | 3:3 | R/W | Select VBUCK2_A (0) / VBUCK2_B (1). |
| VBUCK3_SEL | 2:2 | R/W | Select VBUCK3_A (0) / VBUCK3_B (1). |
| Reserved | 1:1 | | Reserved |
| VBUCK1_SEL | 0:0 | R/W | Select VBUCK1_A (0) / VBUCK1_B (1). |

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A.2.1 Power Sequencer

Table 66: SEQ (0x081)

| Field | Bit | Type | Description |
|-------------|-----|------|---------------------------------|
| Reserved | 7:4 | R/W | Reserved |
| SEQ_POINTER | 3:0 | R | Actual power sequencer position |

Table 67: SEQ_TIMER (0x082)

| Field | Bit | Type | Description |
|-----------|-----|------|---|
| SEQ_DUMMY | 7:4 | R/W | Waiting time for power sequencer slots which do not have an associated power supply. 0000: 32 μ s 0001: 64 μ s 0010: 96 μ s 0011: 128 μ s 0100: 160 μ s 0101: 192 μ s 0110: 224 μ s 0111: 256 μ s 1000: 288 μ s 1001: 384 μ s 1010: 448 μ s 1011: 512 μ s 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms |
| SEQ_TIME | 3:0 | R/W | Length of each sequencer time slot 0000: 32 μ s 0001: 64 μ s 0010: 96 μ s 0011: 128 μ s 0100: 160 μ s 0101: 192 μ s 0110: 224 μ s 0111: 256 μ s 1000: 288 μ s 1001: 384 μ s 1010: 448 μ s 1011: 512 μ s 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms |

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Table 68: ID_2_1 (0x083)

| Field | Bit | Type | Description |
|-----------|-----|------|-------------------------|
| LDO2_STEP | 7:4 | R/W | Sequencer step for LDO2 |
| LDO1_STEP | 3:0 | R/W | Sequencer step for LDO1 |

Table 69: ID_4_3 (0x084)

| Field | Bit | Type | Description |
|-----------|-----|------|-------------------------|
| LDO4_STEP | 7:4 | R/W | Sequencer step for LDO4 |
| LDO3_STEP | 3:0 | R/W | Sequencer step for LDO3 |

Table 70: ID_12_11 (0x088)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| PD_DIS_STEP | 7:4 | R/W | Sequencer step for PD_DIS register functionality |
| Reserved | 3:0 | R/W | Reserved |

Table 71: ID_14_13 (0x089)

| Field | Bit | Type | Description |
|------------|-----|------|--------------------------|
| Reserved | 7:4 | R/W | Reserved |
| BUCK1_STEP | 3:0 | R/W | Sequencer step for Buck1 |

Table 72: ID_16_15 (0x08A)

| Field | Bit | Type | Description |
|------------|-----|------|--------------------------|
| BUCK2_STEP | 7:4 | R/W | Sequencer step for Buck2 |
| BUCK3_STEP | 3:0 | R/W | Sequencer step for Buck3 |

Table 73: ID_22_21 (0x08D)

| Field | Bit | Type | Description |
|---------------|-----|------|----------------------------------|
| GP_FALL1_STEP | 7:4 | R/W | Sequencer step to de-assert GPO0 |
| GP_RISE0_STEP | 3:0 | R/W | Sequencer step to assert GPO0 |

Table 74: ID_24_23 (0x08E)

| Field | Bit | Type | Description |
|---------------|-----|------|----------------------------------|
| GP_FALL2_STEP | 7:4 | R/W | Sequencer step to de-assert GPO1 |
| GP_RISE2_STEP | 3:0 | R/W | Sequencer step to assert GPO1 |

Table 75: ID_26_25 (0x08F)

| Field | Bit | Type | Description |
|---------------|-----|------|----------------------------------|
| GP_FALL3_STEP | 7:4 | R/W | Sequencer step to de-assert GPO2 |
| GP_RISE3_STEP | 3:0 | R/W | Sequencer step to assert GPO2 |

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Table 76: ID_28_27 (0x090)

| Field | Bit | Type | Description |
|---------------|-----|------|----------------------------------|
| GP_FALL4_STEP | 7:4 | R/W | Sequencer step to de-assert GPO3 |
| GP_RISE4_STEP | 3:0 | R/W | Sequencer step to assert GPO3 |

Table 77: ID_30_29 (0x091)

| Field | Bit | Type | Description |
|---------------|-----|------|----------------------------------|
| GP_FALL5_STEP | 7:4 | R/W | Sequencer step to de-assert GPO4 |
| GP_RISE5_STEP | 3:0 | R/W | Sequencer step to assert GPO4 |

Table 78: ID_32_31 (0x092)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| Reserved | 7:4 | R/W | Reserved |
| WAIT_STEP | 3:0 | R/W | Sequencer step for WAIT register functionality |

Table 79: SEQ_A (0x095)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| POWER_END | 7:4 | R/W | End of POWER power domain in the sequencer SYSTEM_END <= POWER_END <= MAX_COUNT must be true. |
| SYSTEM_END | 3:0 | R/W | End of SYSTEM power domain in the sequencer PART_DOWN <= SYSTEM_END <= POWER_END must be true. |

Table 80: SEQ_B (0x096)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| PART_DOWN | 7:4 | R/W | Sequencer slot to stop at, when going down into STANDBY state. 1 <= PART_DOWN <= SYSTEM_END must be true. |
| MAX_COUNT | 3:0 | R/W | End of POWER1 power domain in the sequencer POWER_END <= MAX_COUNT must be true. |

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Table 81: WAIT (0x097)

| Field | Bit | Type | Description |
|-----------|-----|------|---|
| WAIT_DIR | 7:6 | R/W | <p>WAIT_STEP power sequence selection</p> <p>00: Do not wait during WAIT_STEP of power sequencer except for normal slot time.</p> <p>01: Wait during up sequence.</p> <p>10: Wait during down sequence.</p> <p>11: Wait during up and down sequence.</p> |
| TIME_OUT | 5:5 | R/W | <p>Timeout when WAIT_MODE = 0</p> <p>0: no timeout when waiting for external signal (GPIO3).</p> <p>1: 500 ms timeout when waiting for external signal (GPIO3).</p> |
| WAIT_MODE | 4:4 | R/W | <p>0: Wait for external signal (GPIO3) to be active.</p> <p>1: Start timer and wait for expiration.</p> |
| WAIT_TIME | 3:0 | R/W | <p>Wait timer during WAIT STEP of power sequencer ($\pm 10\%$)</p> <p>0000: Do not wait during WAIT_STEP of power sequencer except for normal slot time.</p> <p>0001: 512 μs</p> <p>0010: 1.0 ms</p> <p>0011: 2.0 ms</p> <p>0100: 4.1 ms</p> <p>0101: 8.2 ms</p> <p>0110: 16.4 ms</p> <p>0111: 32.8 ms</p> <p>1000: 65.5 ms</p> <p>1001: 128 ms</p> <p>1010: 256 ms</p> <p>1011: 512 ms</p> <p>1100: 1.0 s</p> <p>1101: 2.0 s</p> <p>1110: 4.1 s</p> <p>1111: 8.2 s</p> |

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Table 82: RESET (0x099)

| Field | Bit | Type | Description |
|-------------|-----|------|--|
| RESET_EVENT | 7:6 | R/W | Reset timer started by: 00: EXT_WAKEUP 01: SYS_UP (register control or pin) 10: PWR_UP (register control or pin) 11: Leaving PMIC RESET mode |
| RESET_TIMER | 5:0 | R/W | 0: Release nRESET immediately after the event selected by RESET_EVENT. 1 - 31: 1.024 ms * RESET_TIMER 32-63: 1.024 ms * 32 * (RESET_TIMER-31) |

A.2.2 Power Supply Control

Table 83: BUCK_ILIM_A (0x09A)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:4 | | Reserved |
| BUCK2_ILIM | 3:0 | R/W | Buck2 current limit = (1700 + BUCK2_ILIM * 100) mA |

Table 84: BUCK_ILIM_B (0x09B)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| Reserved | 7:4 | R/W | Reserved |
| BUCK3_ILIM | 3:0 | R/W | Buck3 current limit = (700 + BUCK3_ILIM * 100) mA |

Table 85: BUCK_ILIM_C (0x09C)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| Reserved | 7:4 | R/W | Reserved |
| BUCK1_ILIM | 3:0 | R/W | Buck1 current limit = (1400 + BUCK1_ILIM * 200) mA In half-current mode the limit is internally halved. |

Table 86: BUCK1_CFG (0x09E)

| Field | Bit | Type | Description |
|--------------|-----|------|--|
| BUCK1_MODE | 7:6 | R/W | Controls the mode of the buck: 00: Controlled by BUCK1_SL_A and BUCK1_SL_B 01: Sleep (PFM) 10: Synchronous (PWM) 11: Automatic |
| BUCK1_PD_DIS | 5:5 | R/W | Disable pull-down resistor when disabled. |
| Reserved | 4:1 | R/W | Reserved |
| Reserved | 0:0 | R/W | Reserved |

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Table 87: BUCK3_CFG (0x09F)

| Field | Bit | Type | Description |
|--------------|-----|------|--|
| BUCK3_MODE | 7:6 | R/W | Controls the mode of the buck: 00: Controlled by BUCK3_SL_A and BUCK3_SL_B 01: Sleep (PFM) 10: Synchronous (PWM) 11: Automatic |
| BUCK3_PD_DIS | 5:5 | R/W | Disable pull-down resistor when disabled. |
| Reserved | 4:0 | R/W | |

Table 88: BUCK2_CFG (0x0A0)

| Field | Bit | Type | Description |
|--------------|-----|------|--|
| BUCK2_MODE | 7:6 | R/W | Controls the mode of the buck: 00: Controlled by BUCK3_SL_A and BUCK3_SL_B 01: Sleep (PFM) 10: Synchronous (PWM) 11: Automatic |
| BUCK2_PD_DIS | 5:5 | R/W | Disable pull-down resistor when disabled. |
| Reserved | 4:0 | R/W | Reserved |

Table 89: VBUCK1_A (0x0A4)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK1_SL_A | 7:7 | R/W | This control is only effective when BUCK1_MODE = 0 0: forced to synchronous mode (PWM) when A setting is active. 1: forced to sleep mode (PFM) when A setting is active. |
| VBUCK1_A | 6:0 | R/W | From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV |

Table 90: VBUCK3_A (0x0A5)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK3_SL_A | 7:7 | R/W | This control is only effective when BUCK3_MODE = 0 0: forced to synchronous mode (PWM) when A setting is active. 1: forced to sleep mode (PFM) when A setting is active. |
| VBUCK3_A | 6:0 | R/W | From 0.53 V (0x00) to 1.8 V (0x7F) in steps of 10 mV |

Table 91: VBUCK2_A (0x0A7)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK2_SL_A | 7:7 | R/W | This control is only effective when BUCK2_MODE = 0 0: forced to synchronous mode (PWM) when A setting is active. 1: forced to sleep mode (PFM) when A setting is active. |
| VBUCK2_A | 6:0 | R/W | From 0.80 V (0x00) to 3.34 V (0x7F) in steps of 20 mV |

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Table 92: VLDO1_A (0x0A9)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO1_SL_A | 7:7 | R/W | Force LDO sleep mode if VLDO1_A is active. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO1_A | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 93: VLDO2_A (0x0AA)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO2_SL_A | 7:7 | R/W | Force LDO sleep mode if VLDO2_A is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO2_A | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 94: VLDO3_A (0x0AB)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO3_SL_A | 7:7 | R/W | Force LDO sleep mode if VLDO3_A is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO3_A | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 95: VLDO4_A (0x0AC)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO4_SL_A | 7:7 | R/W | Force LDO sleep mode if VLDO4_A is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO4_A | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 96: VBUCK1_B (0x0B5)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK1_SL_B | 7:7 | R/W | This control is only effective when BUCK1_MODE = 0 0: forced to synchronous mode (PWM) when B setting is active. 1: forced to sleep mode (PFM) when B setting is active. |
| VBUCK1_B | 6:0 | R/W | From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV |

Table 97: VBUCK3_B (0x0B6)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK3_SL_B | 7:7 | R/W | This control is only effective when BUCK3_MODE = 0 0: forced to synchronous mode (PWM) when B setting is active. 1: forced to sleep mode (PFM) when B setting is active. |
| VBUCK3_B | 6:0 | R/W | From 0.53 V (0x00) to 1.8 V (0x7F) in steps of 10 mV |

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Table 98: VBUCK2_B (0x0B8)

| Field | Bit | Type | Description |
|------------|-----|------|--|
| BUCK2_SL_B | 7:7 | R/W | This control is only effective when BUCK2_MODE = 0 0: forced to synchronous mode (PWM) when B setting is active. 1: forced to sleep mode (PFM) when B setting is active. |
| VBUCK2_B | 6:0 | R/W | From 0.80 V (0x00) to 3.34 V (0x7F) in steps of 20 mV |

Table 99: VLDO1_B (0x0BA)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO1_SL_B | 7:7 | R/W | Force LDO sleep mode when B setting is active. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO1_B | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 100: VLDO2_B (0x0BB)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO2_SL_B | 7:7 | R/W | Force LDO sleep mode if VLDO2_B is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO2_B | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 101: VLDO3_B (0x0BC)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO3_SL_B | 7:7 | R/W | Force LDO sleep mode if VLDO3_B is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO3_B | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

Table 102: VLDO4_B (0x0BD)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| LDO4_SL_B | 7:7 | R/W | Force LDO sleep mode if VLDO4_B is selected. |
| Reserved | 6:6 | R/W | Reserved |
| VLDO4_B | 5:0 | R/W | From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V |

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A.3.1 Customer Trim and Configuration

Table 103: INTERFACE (0x105)

| Field | Bit | Type | Description |
|--------------|-----|-----------------------------|---|
| IF_BASE_ADDR | 7:4 | R Note 1 | 2-wire slave address MSBs. The LSBs of the slave address are "000". The complete slave address is then IF_BASE_ADDR * 23. However, the device also responds to IF_BASE_ADDR * 23+1. |
| Reserved | 3:0 | | Reserved |

Note 1 The interface configuration can be written/modified only for unmarked samples which do not have the control OTP_APPS_LOCK asserted/fused.

Table 104: CONFIG_A (0x106)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| Reserved | 7:7 | R | Reserved |
| PM_IF_HSM | 6:6 | R/W | 2-wire interface permanently in high speed mode. |
| PM_IF_FMP | 5:5 | R/W | 2-wire interface selects fast-mode+ timings. |
| PM_IF_V | 4:4 | R/W | 2-wire supplied from VDDCORE (0) / VDDIO (1). |
| IRQ_TYPE | 3:3 | R/W | nIRQ is active low (0) / high (1). |
| PM_O_TYPE | 2:2 | R/W | nRESET and nIRQ are push pull (0) / open-drain (1). |
| Reserved | 1:1 | R/W | Reserved |
| PM_I_V | 0:0 | R/W | nRESETREQ, SYS_EN, PWR_EN and KEEPACT supplied from VDDCORE (0) / VDDIO (1). |

Table 105: CONFIG_B (0x107)

| Field | Bit | Type | Description |
|---------------|-----|------|--|
| Reserved | 7:7 | R/W | Reserved |
| VDD_HYST_ADJ | 6:4 | R/W | nVDD_FAULT comparator hysteresis from 100 mV (0x0) to 450 mV (0x7) in 50 mV steps. |
| VDD_FAULT_ADJ | 3:0 | R/W | nVDD_FAULT comparator level from 2.5 V (0x0) to 3.25 V (0xF) in 50 mV steps. |

Table 106: CONFIG_C (0x108)

| Field | Bit | Type | Description |
|-------------------|-----|------|--|
| Reserved | 7:7 | R/W | Reserved |
| BUCK2_CLK_INV | 6:6 | R/W | Invert Buck2 clock polarity. |
| Reserved | 5:5 | R/W | Reserved |
| BUCK3_CLK_INV | 4:4 | R/W | Invert Buck3 clock polarity. |
| BUCK1_CLK_INV | 3:3 | R/W | Invert Buck1 clock polarity. |
| BUCK_ACTV_DISCHRG | 2:2 | R/W | Enable active discharging of buck rails. |
| Reserved | 1:0 | R/W | Reserved |

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Table 107: CONFIG_D (0x109)

| Field | Bit | Type | Description |
|--------------|-----|------|---|
| Reserved | 7:6 | R/W | Reserved |
| FORCE_RESET | 5:5 | R/W | Keep nRESET always asserted |
| Reserved | 4:3 | R/W | Reserved |
| SYSTEM_EN_RD | 2:2 | R/W | Suppress loading SYSTEM_EN during OTP_RD2 |
| NIRQ_MODE | 1:1 | R/W | nIRQ will be asserted from events during POWERDOWN ... |
| GPI_V | 0:0 | R/W | GPIs, except power manager controls, supplied from VDDCORE (0) / VDDIO (1). |

Table 108: CONFIG_E (0x10A)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| Reserved | 7:5 | R/W | Reserved |
| BUCK2_AUTO | 4:4 | R/W | Enable and select VBUCK2_A when powering up |
| Reserved | 3:3 | R/W | Reserved |
| BUCK3_AUTO | 2:2 | R/W | Enable and select VBUCK3_A when powering up |
| Reserved | 1:1 | R/W | Reserved |
| BUCK1_AUTO | 0:0 | R/W | Enable and select VBUCK1_A when powering up |

Table 109: CONFIG_G (0x10C)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| Reserved | 7:4 | R/W | Reserved |
| LDO4_AUTO | 3:3 | R/W | Enable and select VLDO4_A when powering up |
| LDO3_AUTO | 2:2 | R/W | Enable and select VLDO3_A when powering up |
| LDO2_AUTO | 1:1 | R/W | Enable and select VLDO2_A when powering up |
| LDO1_AUTO | 0:0 | R/W | Enable and select VLDO1_A when powering up |

Table 110: CONFIG_H (0x10D)

| Field | Bit | Type | Description |
|-----------|-----|------|--|
| Reserved | 7:7 | R/W | Reserved |
| BUCK1_FCM | 6:6 | R/W | Buck full-current mode (double pass device and current limit). |
| Reserved | 5:0 | R/W | Reserved |

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Table 111: CONFIG_I (0x10E)

| Field | Bit | Type | Description |
|--------------|-----|------|--|
| LDO_SD | 7:7 | R/W | Enable switching off an LDO if an over-current is detected longer than 200 ms. |
| INT_SD_MODE | 6:6 | R/W | Skip sequencer and dummy slots on shutdown from internal fault. |
| HOST_SD_MODE | 5:5 | R/W | Skip sequencer and dummy slots on shutdown from SHUTDOWN or nRESETREQ. |
| KEY_SD_MODE | 4:4 | R/W | Enable power-on reset on shutdown from nONKEY. |
| WATCHDOG_SD | 3:3 | R/W | Enable shutdown instead of power-down on watchdog timeout. |
| nONKEY_SD | 2:2 | R/W | Enable shutdown via long press of nONKEY. |
| NONKEY_PIN | 1:0 | R/W | nONKEY function, see Section 7.11 |

Table 112: CONFIG_J (0x10F)

| Field | Bit | Type | Description |
|----------------|-----|------|--|
| IF_RESET | 7:7 | R/W | Enable host interface reset via nRESETREQ pin |
| TWOWIRE_TO | 6:6 | R/W | Enable 35 ms timeout for 2-wire interfaces |
| RESET_DURATION | 5:4 | R/W | Minimum RESET mode duration: 00: 22 ms 01: 100 ms 10: 500 ms 11: 1 s |
| SHUT_DELAY | 3:2 | R/W | Shut down delay (+ KEY_DELAY) for nONKEY |
| KEY_DELAY | 1:0 | R/W | nONKEY locking threshold |

Table 113: CONFIG_K (0x110)

| Field | Bit | Type | Description |
|------------|-----|------|---|
| Reserved | 7:5 | R/W | Reserved |
| GPIO4_PUPD | 4:4 | R/W | GPI: pull-down enabled open-drain GPO: pull-up enabled |
| GPIO3_PUPD | 3:3 | R/W | GPI: pull-down enabled open-drain GPO: pull-up enabled |
| GPIO2_PUPD | 2:2 | R/W | GPI: pull-down enabled open drain GPO: pull-up enabled |
| GPIO1_PUPD | 1:1 | R/W | GPI: pull-down enabled open-drain GPO: pull-up enabled |
| GPIO0_PUPD | 0:0 | R/W | GPI: pull-down enabled open-drain GPO: pull-up enabled |

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Table 114: CONFIG_M (0x112)

| Field | Bit | Type | Description |
|----------|-----|------|--|
| OSC_FRQ | 7:4 | R/W | Adjust internal oscillator frequency: 1000: -10.67 % ... 1111: -1.33 % 0000: 0.00 % 0001: +1.33 % ... 0111: +9.33 % |
| WDG_MODE | 3:3 | R/W | Activate watchdog halt operation mode |
| Reserved | 2:0 | R/W | Reserved |

A.3.2 Customer Device Specific

Table 115: GP_ID_0 (0x121)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_0 | 7:0 | R/W | General purpose register Note 1 |

Note 1 Initial value at start-up is the OTP ini file version number.

Table 116: GP_ID_1 (0x122)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_1 | 7:0 | R/W | General purpose register |

Table 117: GP_ID_2 (0x123)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_2 | 7:0 | R/W | General purpose register |

Table 118: GP_ID_3 (0x124)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_3 | 7:0 | R/W | General purpose register |

Table 119: GP_ID_4 (0x125)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_4 | 7:0 | R/W | General purpose register |

Table 120: GP_ID_5 (0x126)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_5 | 7:0 | R/W | General purpose register |

Table 121: GP_ID_6 (0x127)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_6 | 7:0 | R/W | General purpose register |

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Table 122: GP_ID_7 (0x128)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_7 | 7:0 | R/W | General purpose register |

Table 123: GP_ID_8 (0x129)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_8 | 7:0 | R/W | General purpose register |

Table 124: GP_ID_9 (0x12A)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------------|
| GP_9 | 7:0 | R/W | General purpose register |

Table 125: GP_ID_10 (0x12B)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_10 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 126: GP_ID_11 (0x12C)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_11 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 127: GP_ID_12 (0x12D)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_12 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 128: GP_ID_13 (0x12E)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_13 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 129: GP_ID_14 (0x12F)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_14 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 130: GP_ID_15 (0x130)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_15 | 7:0 | R/W | General purpose register Note 1 |

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Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 131: GP_ID_16 (0x131)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_16 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 132: GP_ID_17 (0x132)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_17 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 133: GP_ID_18 (0x133)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_18 | 7:0 | R/W | General purpose register Note 1 |

Note 1 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

Table 134: GP_ID_19 (0x134)

| Field | Bit | Type | Description |
|-------|-----|------|---|
| GP_19 | 7:0 | R/W | General purpose register Note 2 |

Note 2 The value is persistent through a warm reset such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F.

PMIC for Applications Requiring up to 6 A**A.4 PAGE 3****A.4.1 Device Identification****Table 135: DEVICE_ID (0x181)**

| Field | Bit | Type | Description |
|--------|-----|------|-------------|
| DEV_ID | 7:0 | R | Device ID |

Table 136: VARIANT_ID (0x182)

| Field | Bit | Type | Description |
|-------|-----|------|--------------------|
| MRC | 7:4 | R | Mask revision code |
| VRC | 3:0 | R/W | Chip variant code |

Table 137: CUSTOMER_ID (0x183)

| Field | Bit | Type | Description |
|---------|-----|------|-------------|
| CUST_ID | 7:0 | R | Customer ID |

Table 138: CONFIG_ID (0x184)

| Field | Bit | Type | Description |
|------------|-----|------|-----------------------|
| CONFIG_REV | 7:0 | R | OTP settings revision |

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Status Definitions

| Revision | Datasheet Status | Product Status | Definition |
|----------|------------------|----------------|--|
| 1.<n> | Target | Development | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice. |
| 2.<n> | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
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