ISL71010B50

Ultra Low Noise, 5V Precision Voltage Reference

Description

The ISL71010B50 is an ultra low noise, high DC accuracy precision voltage reference, with a wide input voltage range from 7.0V to 30V. The ISL71010B50 uses the dielectrically isolated PR40 process to achieve 4.2µV_{P-P} noise at 0.1Hz to 10Hz with an initial voltage accuracy of ±0.05%.

The ISL71010B50 offers a 5.0V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld SOIC package.

The ISL71010B50 is ideal for high-end instrumentation, data acquisition, and processing applications requiring high DC precision where low noise performance is critical.

Applications

- Low Earth Orbit (LEO)
- High altitude avionics
- Precision instruments
- Data acquisition systems for space applications
- Strain and pressure gauges for space applications
- Active sources for sensors

Features

- Reference output voltage: 5.0V ±0.05%
- Accuracy over temperature/radiation: ±0.15%
- Output voltage noise: 4.2µV_{P-P} typical (0.1Hz to 10Hz)
- Supply current: 930µA (typical)
- Temperature coefficient: 10ppm/°C (maximum)
- Output current capability: 20mA
- Line regulation: 20ppm/V (maximum)
- Load regulation: 17ppm/mA (maximum)
- NiPdAu-Ag lead finish (Sn Free)
- Dielectrically isolated PR40 process
- Operating temperature range: -55°C to +125°C
- Passes NASA Low Outgassing Specifications
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤10mrad(Si)/s)
  - ISL71010BM30B50Z: 30krad(Si)
  - ISL71010BM50B50Z: 50krad(Si)
- SEE Characterization
  - No DSEE for V_{IN} = 39V at 43MeV·cm^2/mg
  - V_{OUT} SET shorter than 160µs and -300mV ≤ ΔV_{OUT} ≤ 500mV at 28MeV·cm^2/mg

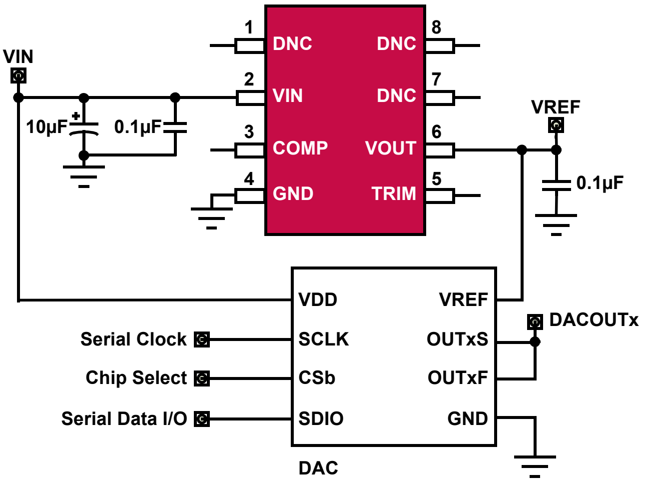


Figure 1. ISL71010B50 Typical Application Diagram

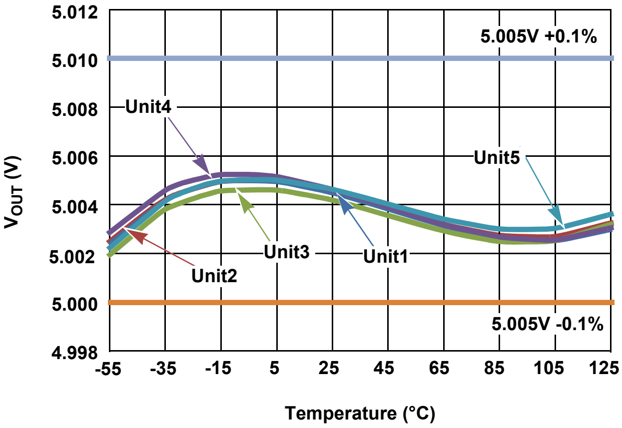


Figure 2. V_{OUT} vs Temperature

Contents

1. Overview

1.1 Functional Block Diagram

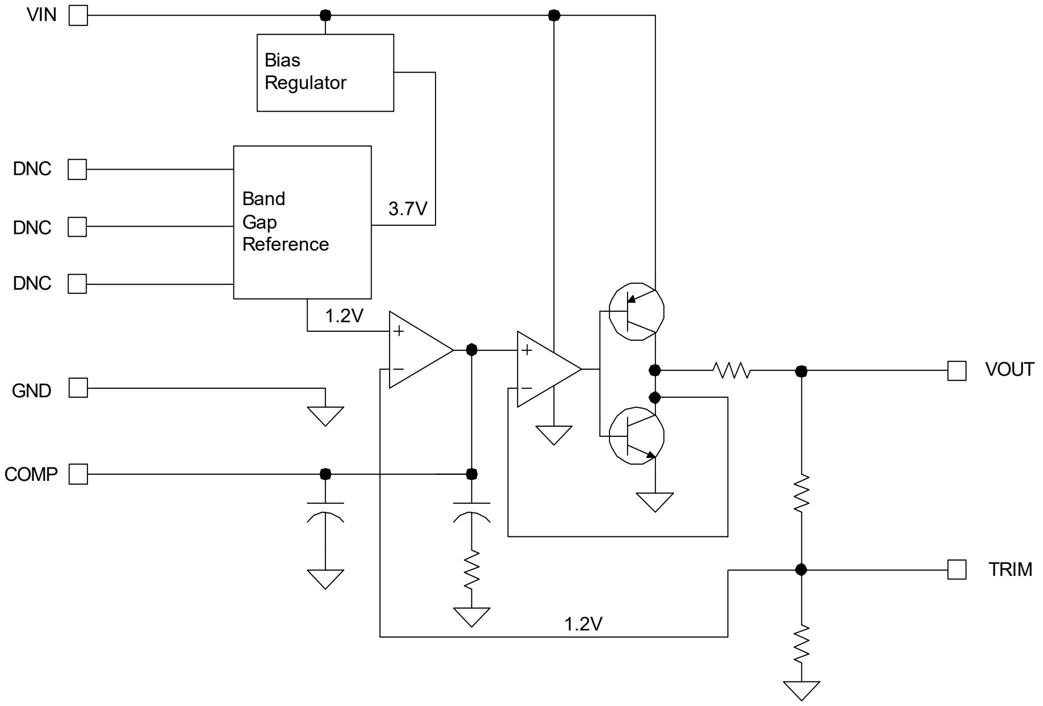


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

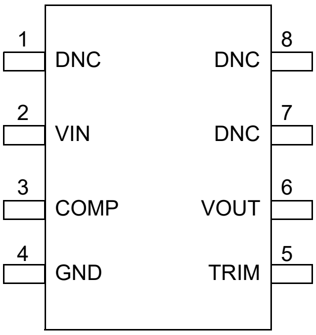
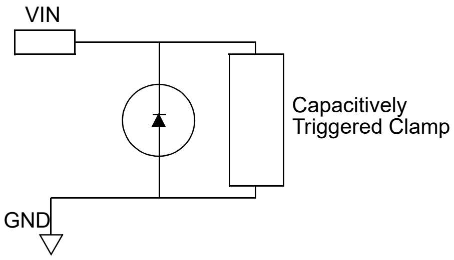


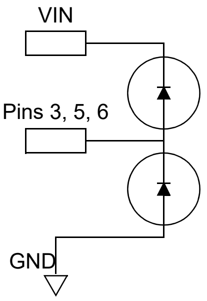
Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

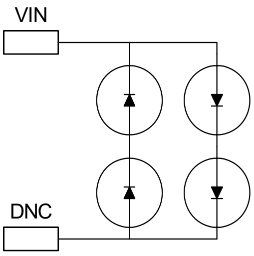
Pin Number	Pin Name	ESD Circuit	Description
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection
3	COMP	2	Compensation and noise reduction capacitor
4	GND	1	Ground connection.
5	TRIM	2	Voltage reference trim input
6	VOUT	2	Voltage reference output



ESD Circuit 1



ESD Circuit 2



ESD Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Max Voltage			
V_{IN} to GND	-0.5	+40	V
V_{OUT} to GND (10s)	-0.5	V_{OUT} + 0.5	V
Voltage on any Pin to Ground	-0.5	+V_{OUT} + 0.5	V
Voltage on DNC pins	No connections permitted to these pins		
Input Voltage Slew Rate (Max)	-	0.1	**V/µs**
Human Body Model (Tested per JS-001-2014)	-	3	kV
Machine Model (Tested per JESD22-A115-C)	-	200	V
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Latch-up (Tested per JESD-78E; Class 2, Level A, at +125°C)	-	±100	mA

3.2 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Results meet NASA low outgassing requirements of “Total Mass Lost” of <1% and “Collected Volatile Condensible Material” of <0.1%.

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	110	°C/W
		θ_{JC}[2]	Junction to case	60	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Continuous Power Dissipation (T_A = +125°C)		217	mW
Maximum Junction Temperature (T_{JMAX})		+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{IN}	7.0	+30	V
Temperature Range	-55	+125	°C

3.5 Electrical Specifications

V_{IN} = 10V, I_{OUT} = 0mA, C_{OUT} = 0.1µF, COMP = 1nF unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71010BM30B50Z); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71010BM50B50Z).**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Output Voltage	V_{OUT}	V_{IN} = 10V	-	5.0	-	V
V_{OUT} Accuracy	V_{OA}	V_{OUT} = 5.0V[2], T_A = +25°C	-0.05	-	+0.05	%
		V_{OUT} = 5.0V[2], T_A = -55°C to +125°C	**-0.15**	-	**+0.15**	%
		V_{OUT} = 5.0V[2], T_A = +25°C, 30krad(Si)	-0.15	-	+0.15	%
		V_{OUT} = 5.0V[2], T_A = +25°C, 50krad(Si)	-0.20	-	+0.20	%
Output Voltage Temperature Coefficient[3]	TC V_{OUT}	-	-	-	10	ppm/°C
Input Voltage Range	V_{IN}	V_{OUT} = 5.0V	7	-	**30**	V
Supply Current	I_{IN}	-	-	0.930	**1.33**	mA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 7V to 30V, V_{OUT} = 5.0V	-	8	**20**	ppm/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA	-	2.5	**17**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA	-	2.5	**17**	ppm/mA
Dropout Voltage[4]	V_D	V_{OUT} = 5.0V at 10mA	-	1.1	**1.7**	V
Short-Circuit Current	I_{SC+}	T_A = +25°C, V_{OUT} tied to GND	-	54	75	mA
Short-Circuit Current	I_{SC-}	T_A = +25°C, V_{OUT} tied to V_{IN}	-100	-60	-	mA
Turn-On Settling Time	t_R	90% of final value, C_L = 1.0µF, C_C = Open	-	150	-	µs
Ripple Rejection		f = 120Hz	-	90	-	dB
Output Voltage Noise	e_{np-p}	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 5.0V	-	4.2	-	μV_{P-P}
Broadband Voltage Noise	V_n	10Hz ≤ f ≤ 1kHz, V_{OUT} = 5.0V	-	3.2	-	μV_{RMS}
Noise Voltage Density	e_n	f = 1kHz, V_{OUT} = 5.0V	-	100	-	nV/√Hz
Long Term Stability	$\Delta V_{OUT}/\Delta t$	T_A = +25°C	-	20	-	ppm

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Post-reflow drift for the ISL71010B50 devices can exceed 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The system engineer must take this into account when considering the reference voltage after assembly.
3. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C. See Specifying Temperature Coefficient (Box Method) for more information.
4. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = Nominal at T_A = +25°C.

4. Typical Performance Curves

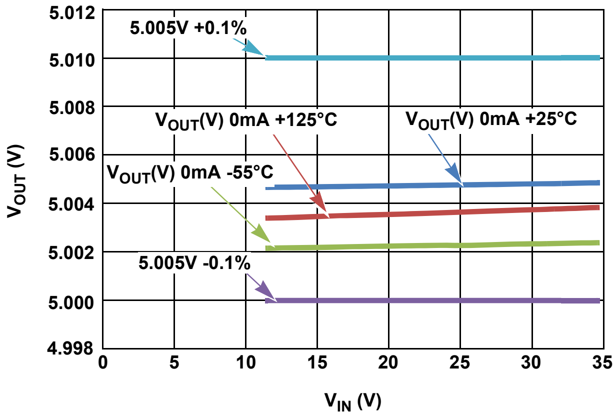


Figure 5. V_{OUT} Accuracy Over Temperature

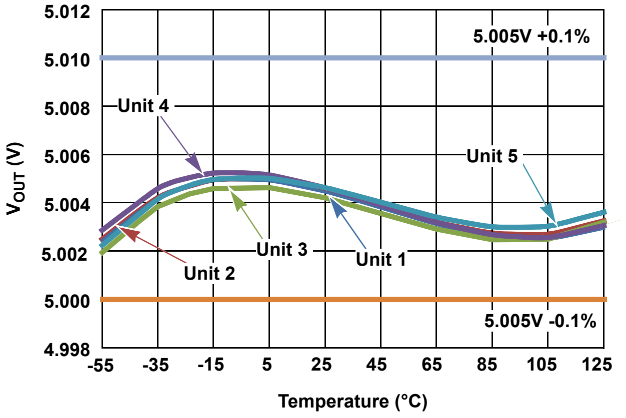


Figure 6. 5.005V V_{OUT} Limits Plot

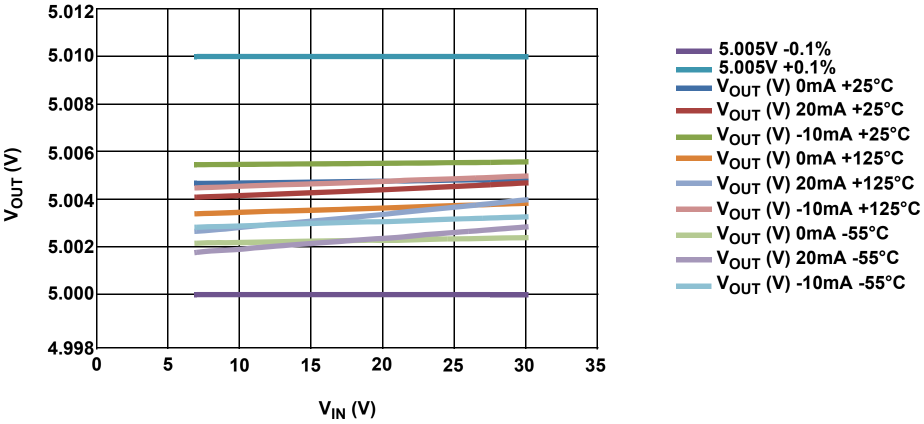


Figure 7. V_{OUT} vs V_{IN} AT 0mA, 20mA, and -10mA

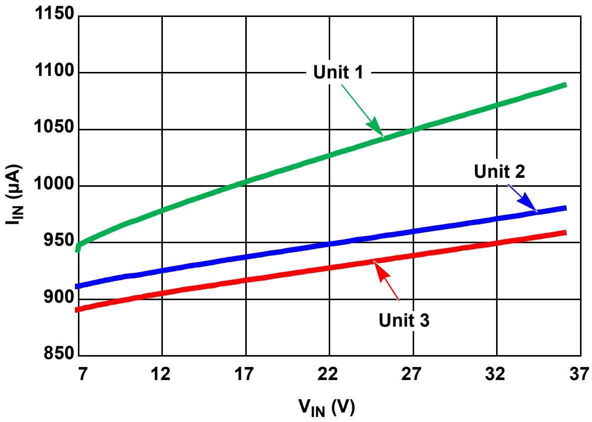


Figure 8. I_{IN} vs V_{IN}, Three Units

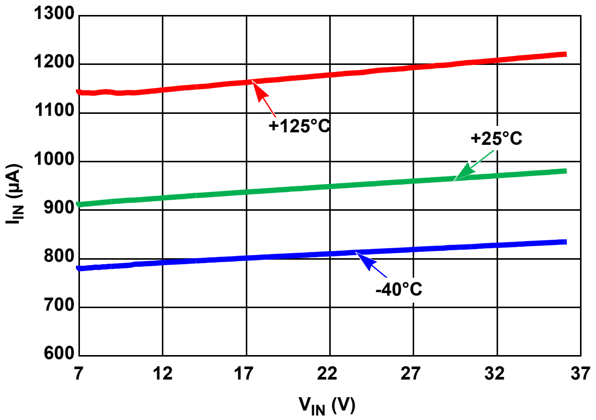


Figure 9. I_{IN} vs V_{IN}, Three Temperatures

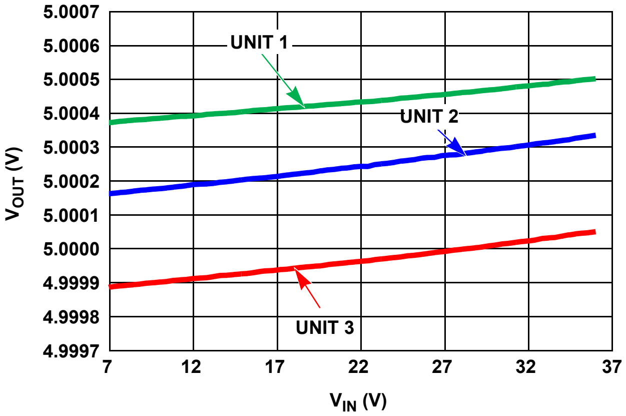


Figure 10. Line Regulation, Three Units

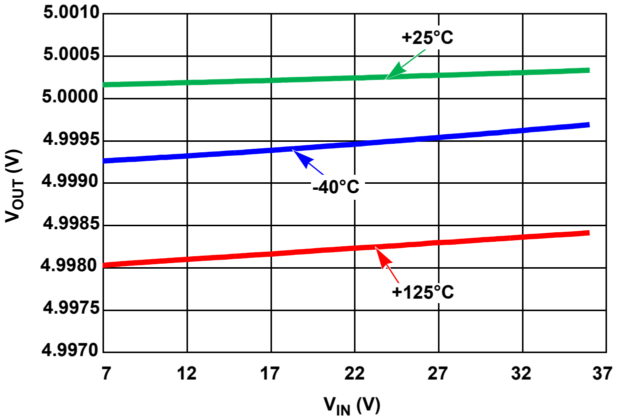


Figure 11. Line Regulation, Three Temperatures

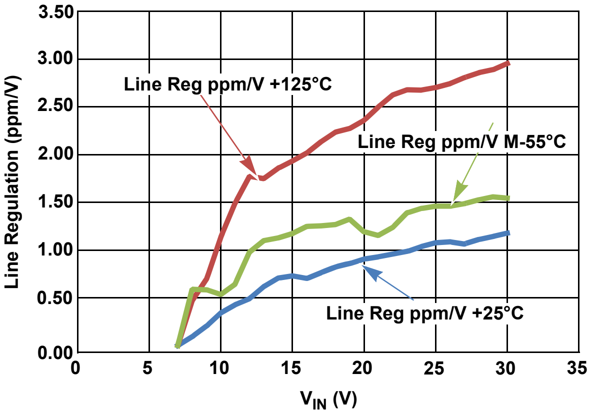


Figure 12. Line Regulation Over Temperature

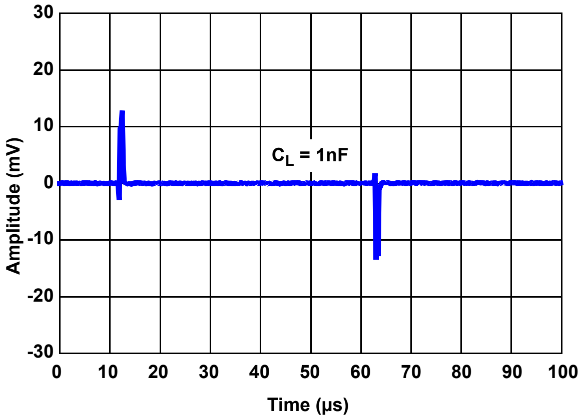


Figure 13. Line Transient with 1nF LOAD ($\Delta V_{IN} = \pm500mV$)

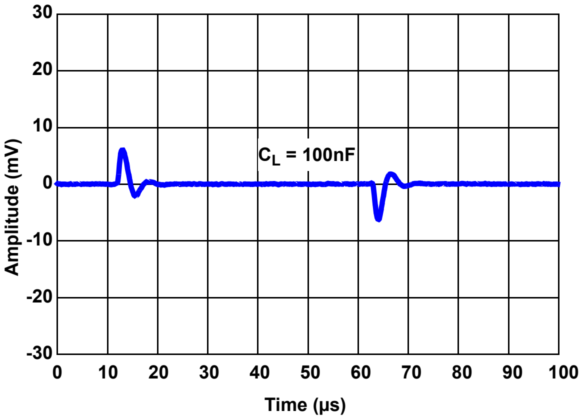


Figure 14. Line Transient with 100nF LOAD ($\Delta V_{IN} = \pm500mV$)

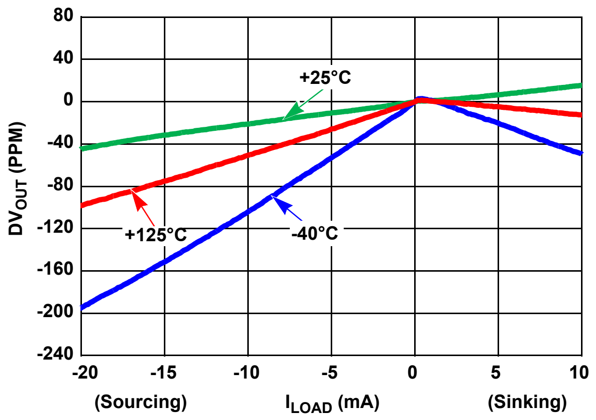


Figure 15. Load Regulation, Three Temperatures

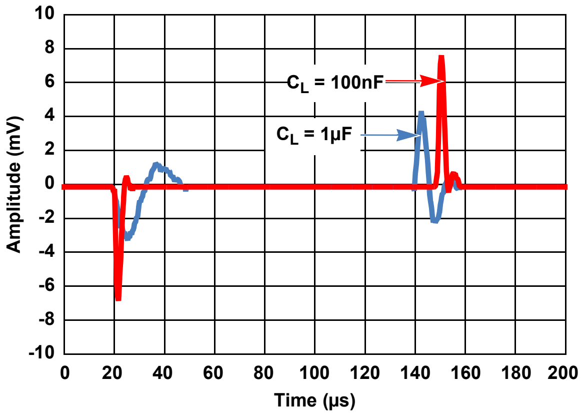


Figure 16. Load Transient (ΔI_{LOAD} = ±1mA)

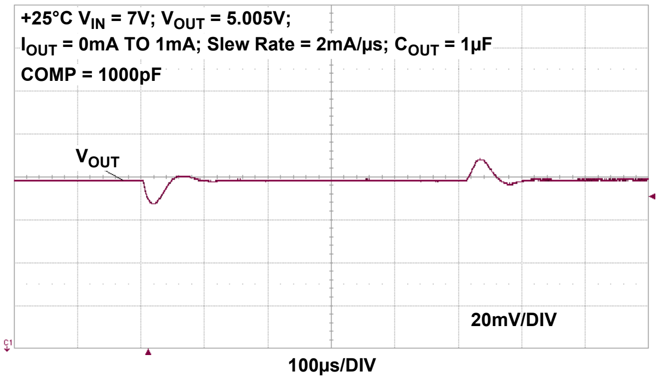


Figure 17. Load Transient (0mA to 1mA)

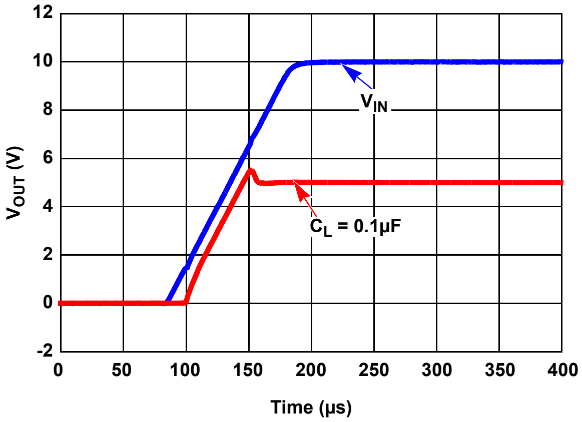


Figure 18. Turn-On Time with 0.1µF

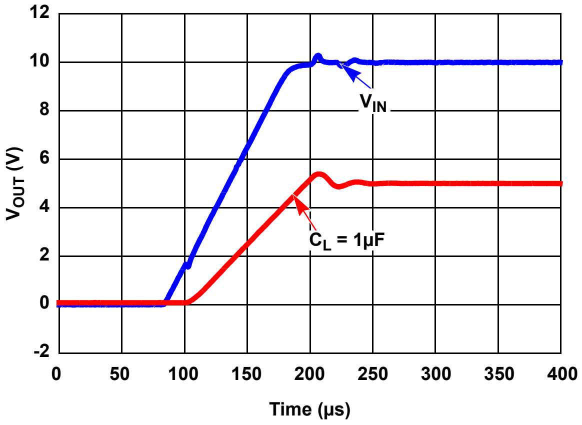


Figure 19. Turn-On Time with 1µF

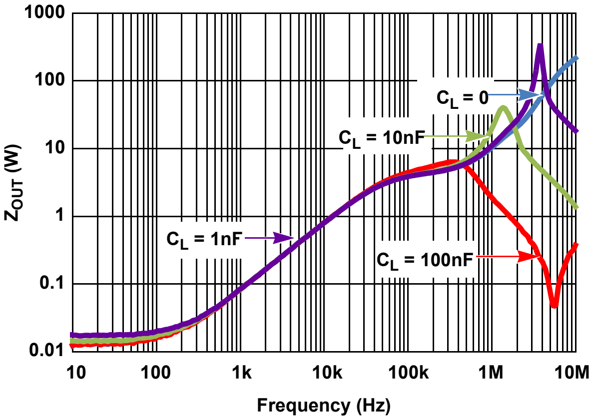


Figure 20. Z_{OUT} vs Frequency

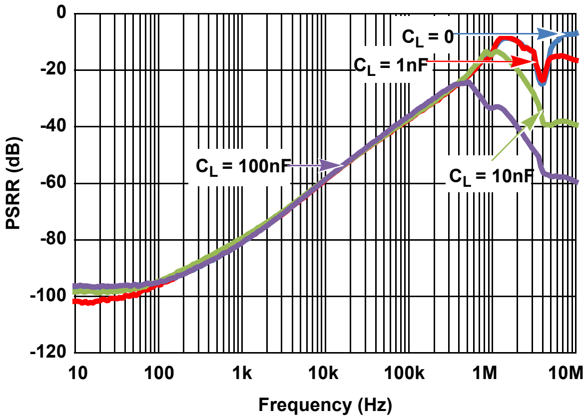


Figure 21. PSRR at Different Capacitive Loads

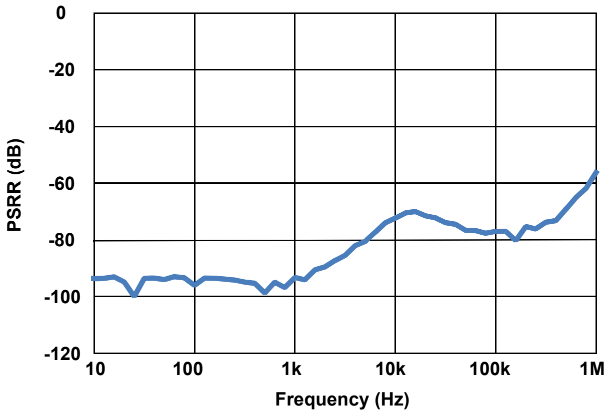


Figure 22. PSRR (+25°C, V_{IN} = 7V, V_{OUT} = 5.005V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1.0µF, COMP = 1nF, V_{SIG} = 300mV_{P-P})

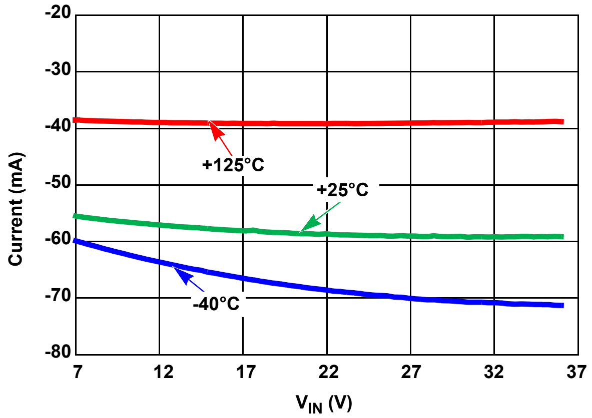


Figure 23. Short-Circuit to GND

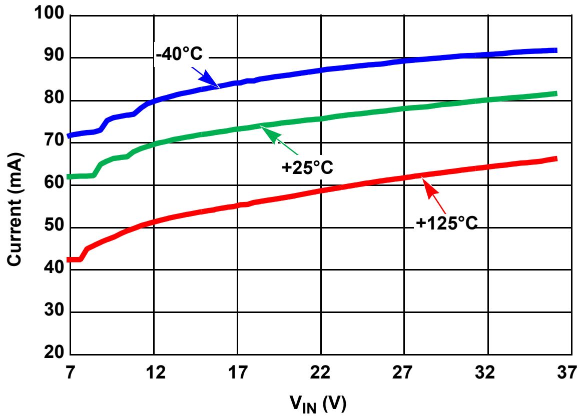


Figure 24. Short-Circuit to V_{IN}

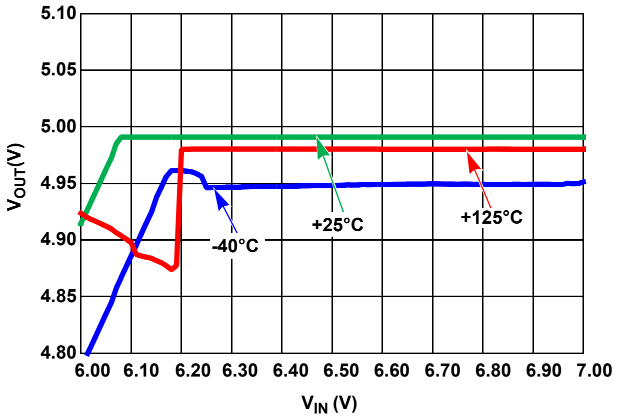


Figure 25. Dropout with -10mA Load

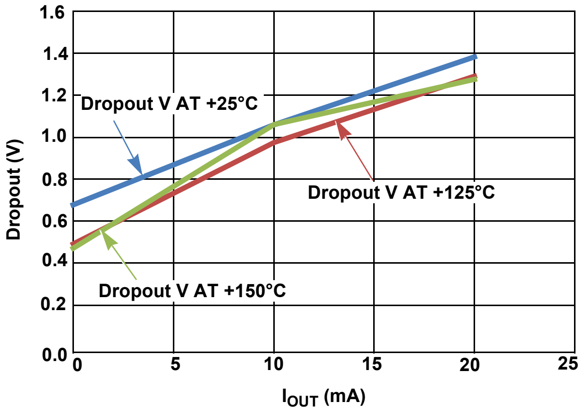


Figure 26. Dropout Voltage for 5.005V

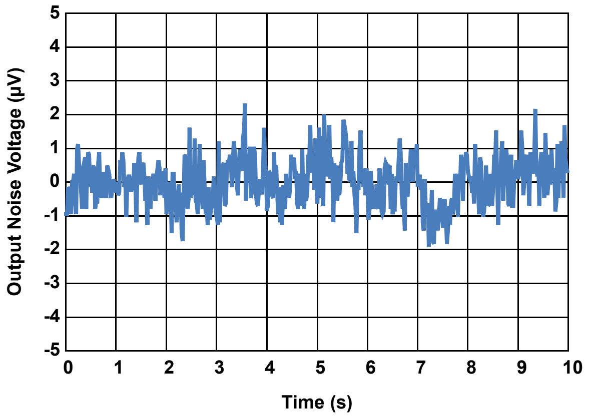


Figure 27. V_{OUT} vs Noise, 0.1Hz to 10Hz

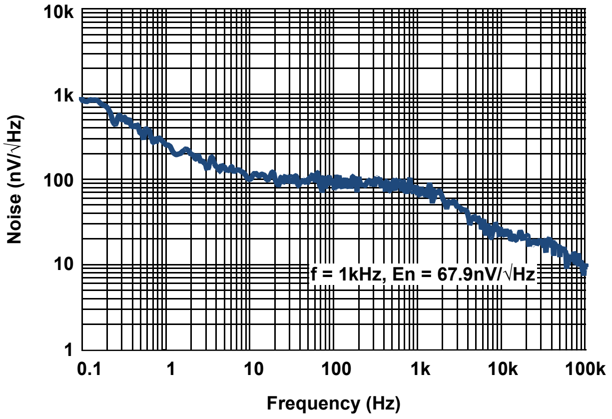


Figure 28. Noise Density vs Frequency (V_{IN} = 7.1V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1µF, COMP = 1nF)

5. Applications Information

5.1 Bandgap Precision Reference

The ISL71010B50 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

5.2 Board Mounting Considerations

For applications requiring the highest accuracy, the board mounting location should be considered. The device uses a plastic SOIC package, which subjects the die to mild stresses when the Printed Circuit Board (PCB) is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of degrade the reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

5.3 Board Assembly Considerations

Some PCB assembly precautions are necessary. Normal output voltage shifts of 100µV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PCBs. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

5.4 Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 4.2µV_{P-P} (V_{OUT} = 5.0V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately 3.2µV_{RMS}, with 1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added, but will result in only marginal improvements in output noise and transient response.

5.5 Turn-On Time

Normal turn-on time is typically 250µs. The circuit designer must take this into account when looking at power-up delays or sequencing.

5.6 Specifying Temperature Coefficient (Box Method)

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures. Divide the total variation ($V_{HIGH} – V_{LOW}$) by the temperature extremes of measurement ($T_{HIGH} – T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

5.7 Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value using the trim terminal. The trim terminal is the negative feedback divider point of the output operational amplifier. The voltage at the TRIM pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference.

The suggested method to adjust the output is to connect a 1MΩ external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100kΩ resistance and with outer terminals that connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. The TRIM pin should not have any capacitor tied to its output. Also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments do not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

5.8 Output Stage

The output stage of the device has a push pull configuration with a high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA.

5.9 Use of COMP Capacitors

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from COMP pin to GND. See Table 1 for recommended values of the COMP capacitor.

Table 1. COMP Capacitor Recommended Values

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

6. Radiation Tolerance

The ISL71010B50 is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device’s response to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL71010B50 is not guaranteed through radiation lot acceptance testing. The ISL71010BM30B50 is radiation lot acceptance tested (RLAT) to 30krad(Si), and the ISL71010BM50B50 is RLAT to 50krad(Si).

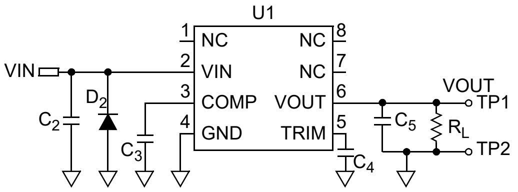
6.1 Total Ionizing Dose (TID) Testing

6.1.1 Introduction

This test was conducted to determine the sensitivity of the part to the total dose environment. Testing was performed on two separate sample sets. For the first sample set, test downpoints were 0krad(Si), 10krad(Si), and 30krad(Si). The second sample set was irradiated to 50krad(Si).

Total dose testing was performed using a Hopewell Designs N40 panoramic ^{60}Co irradiator. The irradiations were performed at 10mrad(Si)/s. A PbAl box was used to shield the test fixture and devices under test against low energy secondary gamma radiation.

The characterization matrix of the first sample set consisted of four samples irradiated under bias and four samples irradiated with all pins grounded. The characterization matrix of the second sample set consisted of seven samples irradiated under bias and seven samples irradiated with all pins grounded. Four control units were used to ensure repeatable data. Two different wafers were used. The bias configuration is shown in Figure 29.



PARTS:
V_{IN} = +36V ±10%
R_1 = 3.86k, 1%, 1W
R_2 = 470, 1%, 1W
R_L = 5k, 1%, 1⁄4W

C_2 = 0.1µF, 50V, 10%, X7R
C_3, C_4 = 0.01µF, 50V, 10%, X7R
C_5 = 0.1µF, 10V, 10%, X7R

Figure 29. Irradiation Bias Configuration and Power Supply Sequencing for the ISL71010B50

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE), with data logging at each down point. Downpoint electrical testing was performed at room temperature.

6.1.2 Results

Table 2 summarizes the attributes data.

Table 2. ISL71010B50 Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Down Point	Pass[1]	Rejects
10	Figure 29	4	Pre-rad	4	0
			10krad(Si)	4	0
			30krad(Si)	4	0
		7	50krad(Si)	7	0
10	Grounded	4	Pre-rad	4	0
			10krad(Si)	4	0
			30krad(Si)	4	0
		7	50krad(Si)	7	0

[1] A Pass indicates a device that passes all datasheet specification limits.

The plots in Figure 30 through Figure 35 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions. All parts showed excellent stability over irradiation.

Table 3 shows the average of the key parameters with respect to total dose in tabular form.

6.1.3 Data Plots

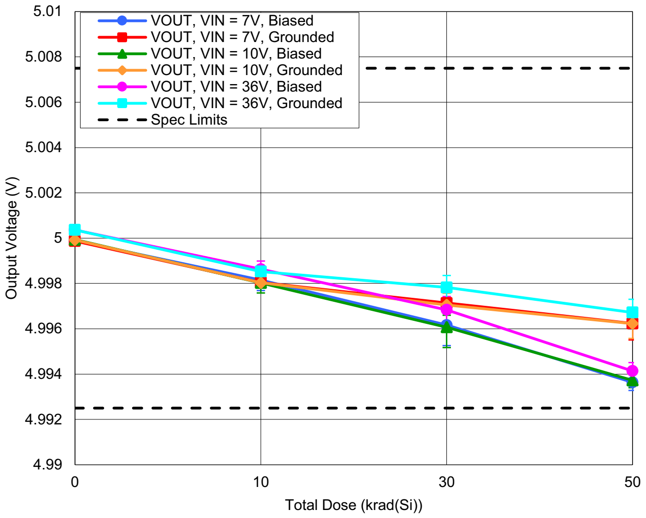


Figure 30. VREF Output Voltage vs TID

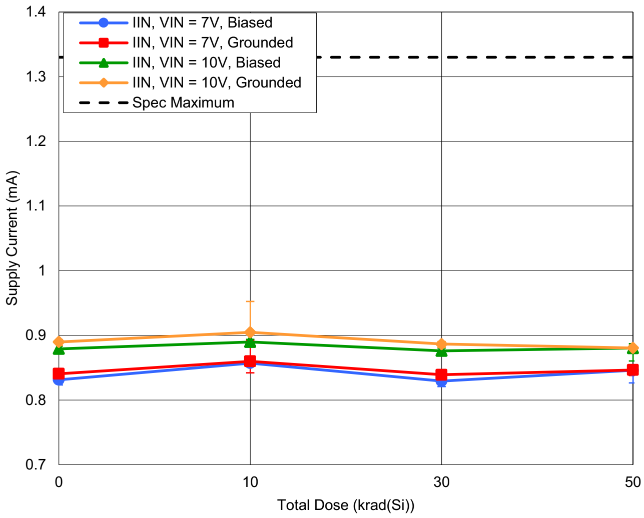


Figure 31. Supply Current vs TID

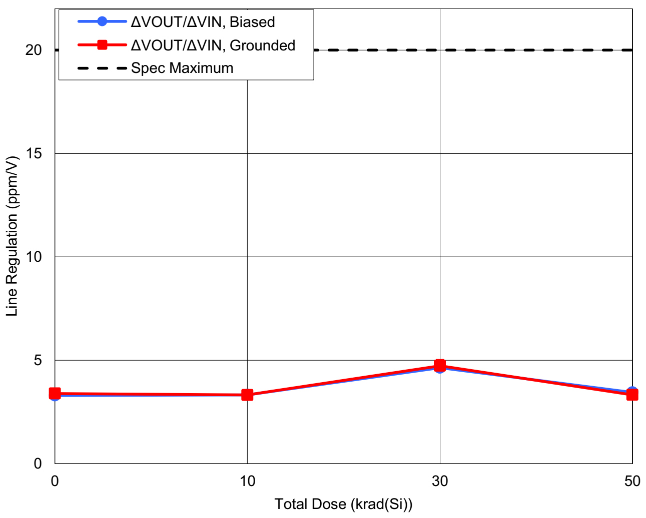


Figure 32. Line Regulation vs TID

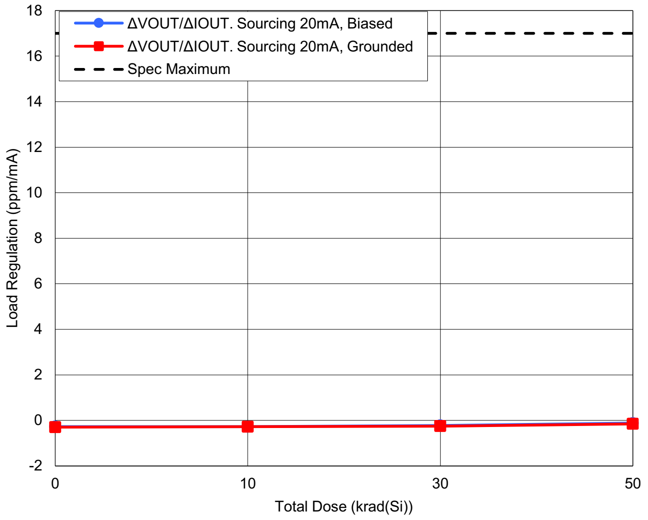


Figure 33. Load Regulation 20mA Sourcing vs TID

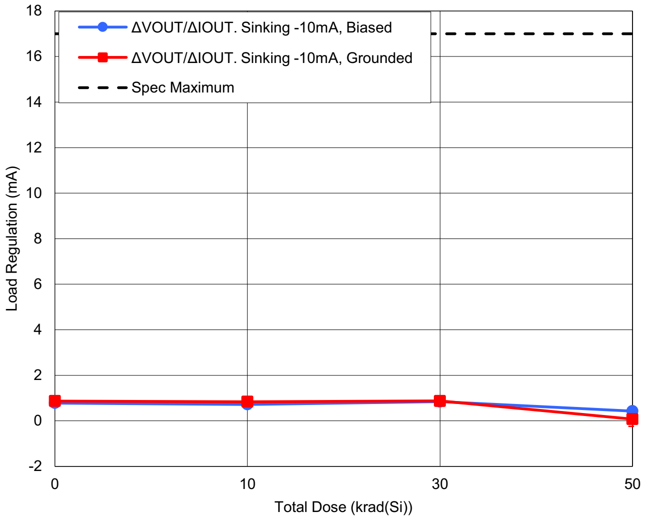


Figure 34. Load Regulation -10mA Sinking vs TID

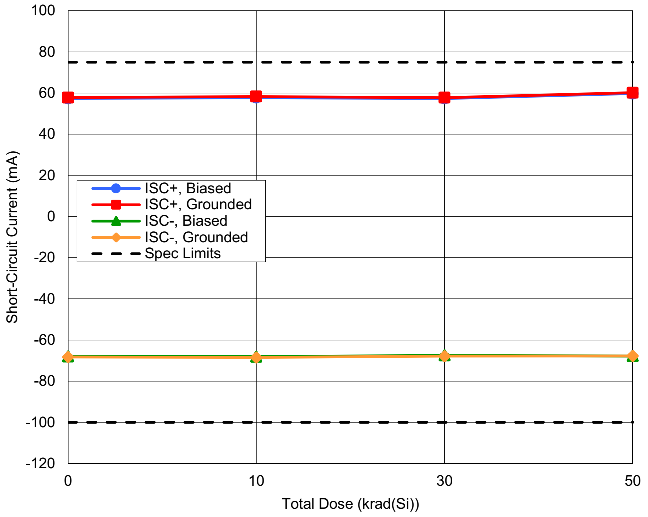


Figure 35. Short-Circuit Current vs TID

6.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all down points. Variables data for selected parameters is presented in Figure 30 through Figure 35. No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

Table 3. ISL71010B50 Response of Key Parameters vs TID

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Output Voltage	V_{OUT}	V_{IN} = 10V	Bias	4.999938	4.998027	4.996072	4.993725	V
			Grounded	4.999922	4.998032	4.997056	4.996227	
		V_{IN} = 7V	Bias	4.999885	4.998147	4.996166	4.993636	
			Grounded	4.999873	4.998045	4.997138	4.996235	
		V_{IN} = 36V	Bias	5.000362	4.99863	4.99684	4.994136	
			Grounded	5.000366	4.998528	4.997825	4.996719	

Table 3. ISL71010B50 Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Supply Current	I_{IN}	V_{IN} = 7V	Bias	0.831391	0.85709	0.829327	0.846038	mA
			Grounded	0.840696	0.859878	0.839203	0.84651	
		V_{IN} = 10V	Bias	0.879245	0.889788	0.876051	0.880307	
			Grounded	0.889907	0.90476	0.886532	0.880486	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4V to 30V, V_{OUT} = 2.5V	Bias	3.295899	3.327616	4.641101	3.446307	ppm/V
			Grounded	3.395929	3.326168	4.734789	3.332438	
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	20mA Sourcing	Bias	-0.27145	-0.27352	-0.22263	-0.11585	ppm/mA
			Grounded	-0.29523	-0.27458	-0.25169	-0.15318	
		-10mA Sinking	Bias	0.78336	0.720432	0.843916	0.428049	
			Grounded	0.86987	0.840889	0.877108	0.076316	
Short-Circuit Current	I_{SC+}	V_{OUT} = GND	Bias	57.37025	57.72532	57.32021	59.76282	mA
			Grounded	57.80417	58.30301	57.73128	60.18774	
	I_{SC-}	V_{OUT} = V_{IN}	Bias	-68.0334	-68.0907	-67.4924	-67.7959	
			Grounded	-68.2972	-68.4802	-67.8589	-67.7662	

6.2 Single Event Effects Testing

6.2.1 Introduction

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the ISL71010B50 SEE testing.

6.2.2 SEE Test Setup

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility.

A schematic of the ISL71010B50 SEE test circuit is shown in Figure 40. The test circuit is configured to accept an input voltage from 7V to 30V and generate the 5.0V nominal output voltage. The output current of the reference was adjusted using fixed load resistors on a test board. The output capacitor, C_4, and the compensation capacitor C_2 were 0.1µF and 10nF, respectively.

Digital multimeters were used to monitor input voltage (V_{IN}), output voltage (V_{OUT}), and input current (I_{IN}). A LeCroy waveRunner digital oscilloscope was used to monitor, capture, and store key signal waveforms. The scope was configured to trigger with V_{OUT} signal levels of ±50mV.

6.2.3 SEB Testing Results

For the SEB tests, conditions were selected to maximize the electrical and thermal stresses on the Device Under Test (DUT), thus insuring worst-case conditions. The input voltage (V_{IN}) was initially set to 35V and then increased in 1V increments. The capacitors were set to C_{OUT} = 0.1µF and C_{COMP} = 1nF. SEB testing was conducted with the ISL71010B25. Output current (I_{OUT}) was set to 20mA which is the maximum recommended current rating for load regulation of the device. Case temperature was maintained at +125ºC by controlling the current flowing into a resistor heater bonded to the underside of the DUT. Four DUTs were irradiated with Ag ions at a normal incident angle, resulting in an effective LET of 43MeV•cm^2/mg.

The failure criterion for destructive SEE was an increase in operating input current (I_{IN}) greater than 5% measured at 20mA output current. I_{IN} is defined as the total current drawn by the device. Failed devices were not further irradiated.

From a design perspective, the ISL71010B25 and the ISL71010B50 are exactly the same in silicon. The output voltages, even though they are different values, are produced the same way and trimmed through a resistor ladder network. All the parts are built in the same process and are functionally equivalent. Therefore, the ISL71010B25 SEB results are applicable to the ISL71010B50.

Four parts passed irradiation to 1x10^7 ions/cm^2 with 43MeV•cm^2/mg at 39V and +125ºC case temperature.

6.2.4 Single Event Transient (SET) Testing

SET testing was done on four samples of the ISL71010B50, which were irradiated at room temperature at LETs of 2.7MeV•cm^2/mg and 28MeV•cm^2/mg to observe SET performance. Samples were separately tested to V_{IN} of 7V and 30V. The parts were configured with a 0.1µF output capacitor, 10nF compensation capacitor, and a 20mA load current to set up the worst conditions for negative going transients. Table 4 shows the SET summary giving the cross section for each input voltage and LET level.

Figure 36 through Figure 39 represent output waveform responses of the DUTs at the respective bias conditions and LET levels. The plots are composites of all the transients captured on the scope.

The SET exhibited by the ISL71010B50 fall into two basic categories; fast negative spike and slow negative ramp. The fast spikes can be as large as 500mV for LET 28 and V_{IN} = 30V. Under the same conditions, the slow (20µs) negative ramp can reach 300mV. The slow ramp disturbances can take significantly over 160µs to recover. Even at LET = 8.5MeV•cm^2/mg (Figure 36 and Figure 37), there are SET of approximately 200mV.

Table 4. SET Summary of Fully Functional ISL71010B50

Supply Voltage (V)[1]	LET (MeV•cm^2/mg)	Fluence (Particles/cm^2)	Events (±50mV)	Events CS (cm^2)
7	8.5	8.00E+06	375	4.69E-05
30	8.5	8.00E+06	442	5.53E-05
7	28	8.00E+06	743	9.29E-05
30	28	8.00E+06	1073	1.34E-04

1. Samples at 7.0V and 30V input voltage. trigger level for the output voltage SET to ±50mV.

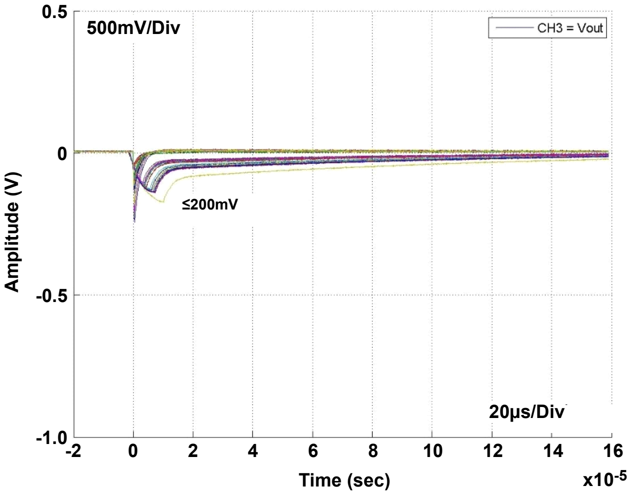


Figure 36. Composite SET Plot for ISL71010B50 at LET 8.5 V_{IN} = 7V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

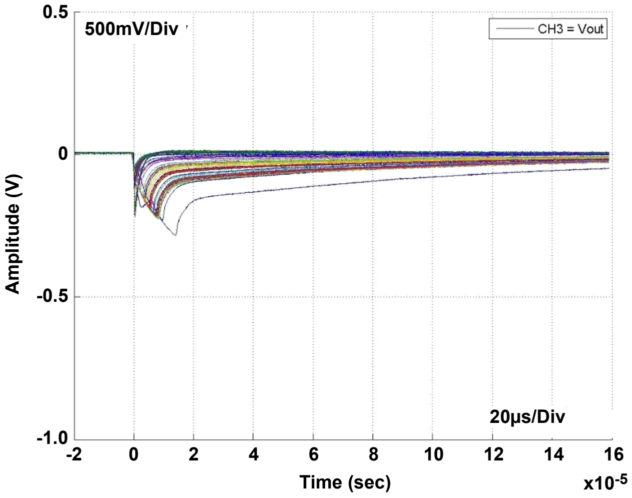


Figure 37. Composite SET Plot for ISL71010B50 at LET 8.5 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

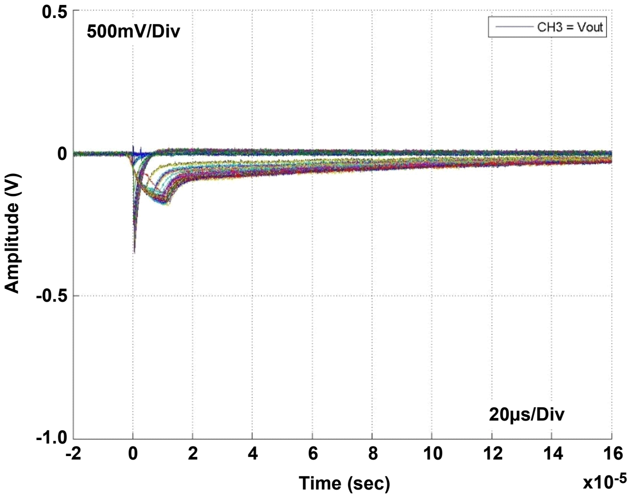


Figure 38. Composite SET Plot for ISL71010B50 at LET 28 V_{IN} = 7V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

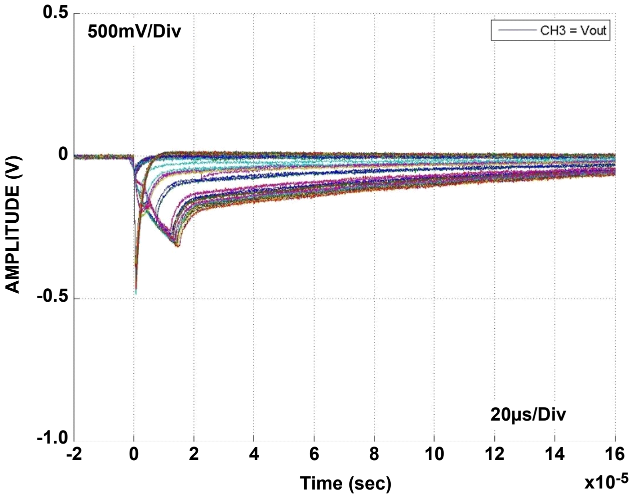


Figure 39. Composite SET Plot for ISL71010B50 at LET 28 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

7. Conclusion

SEE testing has demonstrated that the ISL71010B50 is not susceptible to Single Event Burnout (SEB) at an LET of 43MeV•cm^2/mg with an input voltage of 39V and a load current of 20mA. This represents conditions that are over 30% above the recommended input voltage of 30V and 100% of the load regulation drive capability of the IC (20mA).

SET testing demonstrated that all transients are negative and the higher the LET level the greater the magnitude of the negative transient. At LET = 28MeV•cm^2/mg and V_{IN} = 30V with C_{OUT} = 0.10µF, showed a 500mV fast negative transient and a 300mV slow (20us) negative transient during an SET event. The slow transient can take over 160µs to recovery. At LET = 8.5MeV•cm^2/mg there are SET of approximately 200mV.

A larger C_{OUT} capacitance value will suppress the SET magnitude but the SET disturbance duration will stretch out. Capacitor selection represents a compromise between SET magnitude and recovery duration.

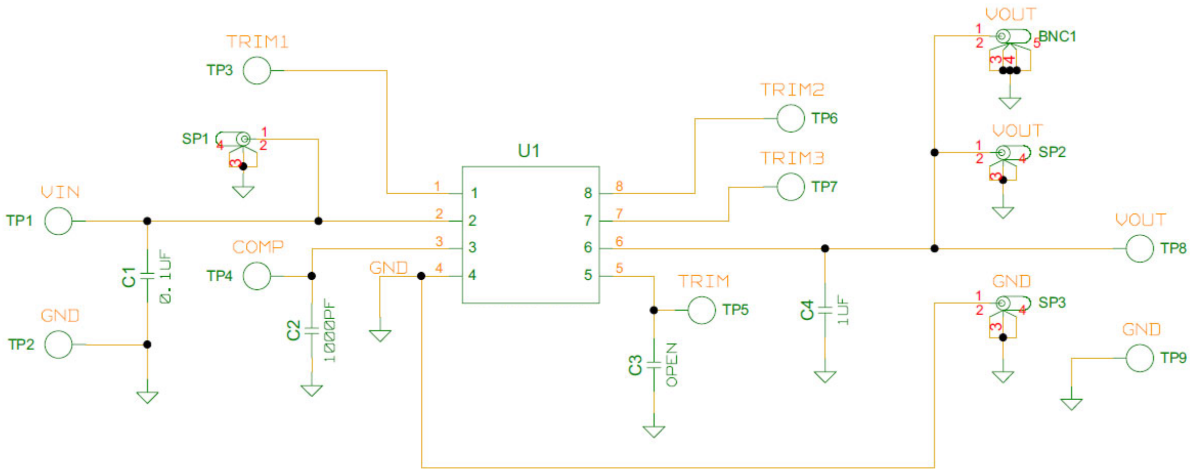


Figure 40. SEE Testing Schematic for the ISL71010B50

8. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

9. Ordering Information

Part Number[1] [2]	Part Marking	Radiation Lot Acceptance Testing	V_{OUT} Option (V)	Accuracy (%) T_A = 25°C	Tempco (ppm/°C)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type [3]	Temp Range
ISL71010BMB50Z	71010 BMZ50	N/A	5.0	±0.05	10	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71010BMB50Z-TK								Reel, 1k	
ISL71010BM30B50Z	71010 BMZ50	30krad(Si)	5.0	±0.15	10	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71010BM30B50Z-TK								Reel, 1k	
ISL71010BM50B50Z	71010 BMZ50	50krad(Si)	5.0	±0.20	10	8 Ld SOIC	M8.15	Tube	-55 to +125°C
ISL71010BM50B50Z-TK								Reel, 1k	
ISL71010BM50EV1Z	Evaluation Board								

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71010B50 device page. For more information about MSL, refer to TB363.
3. See TB347 for details about reel specifications.

10. Revision History

Rev.	Date	Description
1.01	Aug 12, 2025	Applied latest template. Updated Radiation bullets. Updated Radiation Tolerance sections. Updated POD M8.15 to the latest version. Updated Ordering Information table.
1.00	Apr 12, 2018	Added Outgassing Feature bullet. Updated Ordering information by adding -TK part to table and updated Note 1. Added Outgassing specification information. Removed About Intersil and updated disclaimer.
0.00	Sep 29, 2017	Initial release

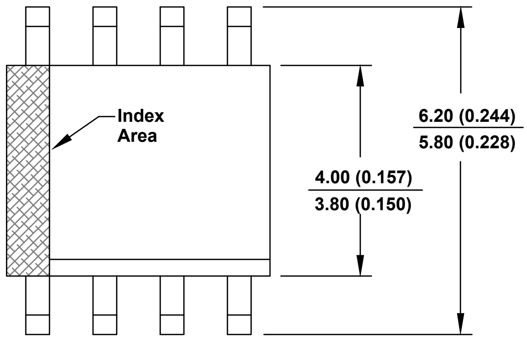
Package Outline Drawing

M8.15

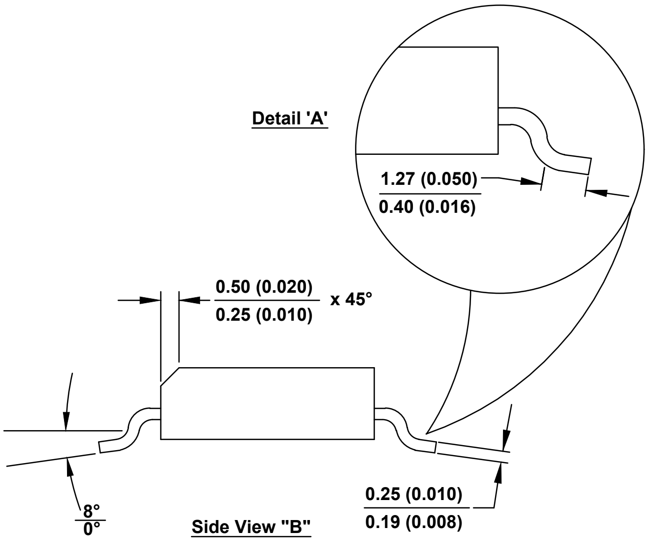
GS0008AC

8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch

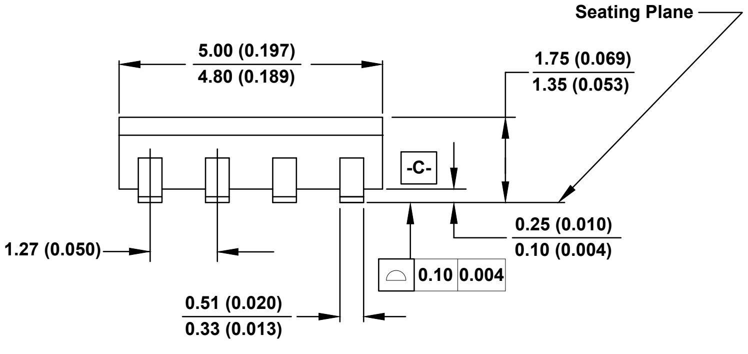
Rev08, Jul 7, 2025



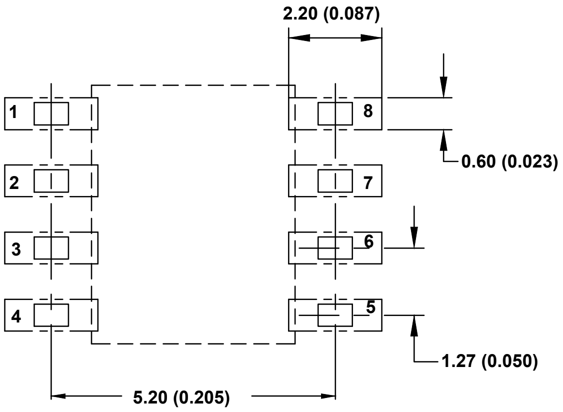
Top View



Side View "B"



Side View "A"



Typical Recommended Land Pattern

Notes:

1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2025 Renesas Electronics Corporation. All rights reserved.