RAA210610

15A, 54V Single-Channel DC/DC Step-Down Power Module

The RAA210610 power module is a single-channel, synchronous step-down, non-isolated complete power supply, capable of delivering up to 15A of continuous current. Operating from a single 7V to 54V wide input power rail and integrating the controller, power inductor, and MOSFETs, the RAA210610 requires only a few external components to operate and is optimized for space constrained applications.

The RAA210610 offers an adjustable output voltage range of 0.6V to 42V with better than 1.5% accuracy over line, load, and temperature. It achieves up to 97.6% efficiency and provides fast transient response and excellent loop stability. The operating frequency can also be synchronized with an external clock signal. The RAA210610 implements a selectable Pulse Skipping Mode (PSM) with Diode Emulation Mode (DEM) to improve light-load efficiency for battery related applications. A programmable soft-start reduces the inrush current from the input supply while a dedicated enable pin and power-good flag allow for easy system power rails sequencing with voltage tracking capability. Input Undervoltage Lockout (UVLO), over-temperature, programmable overcurrent, output overvoltage, and output pre-bias start-up protections ensure safe operations under abnormal operating conditions. The RAA210610 is available in a compact RoHS compliant thermally-enhanced 19mmx13mmx5.3mm HDA package.

Related Literature

For a full list of related documents, visit our website:

- RAA210610 device page

Features

- Up to 15A single-channel complete power supply
  - Integrates controller, MOSFETs, and inductor
- 7V to 54V wide input voltage range
- Adjustable output voltage
  - 0.6V to 42V wide output voltage range
  - ±1.5% accuracy over line, load, and temperature
  - Up to 97.6% efficiency
- 300kHz to 2MHz adjustable PWM operations
  - External synchronization up to 1MHz
  - Selectable light-load PSM/DEM efficiency mode
- Enable pin and power-good flag
- Programmable soft-start or voltage tracking
- Complete protection
  - UVLO, programmable overcurrent, overvoltage, and over-temperature
  - Prebias output start-up
- Compact RoHS compliant 19mmx13mmx5.3mm HDA package

Applications

- Telecom, Industrial, and medical equipment
- Point-of-load conversions
- Aftermarket automotive

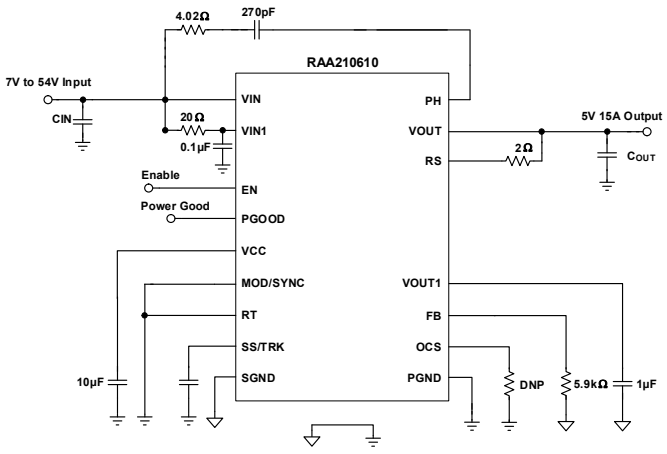


Figure 1. Typical Application Circuit

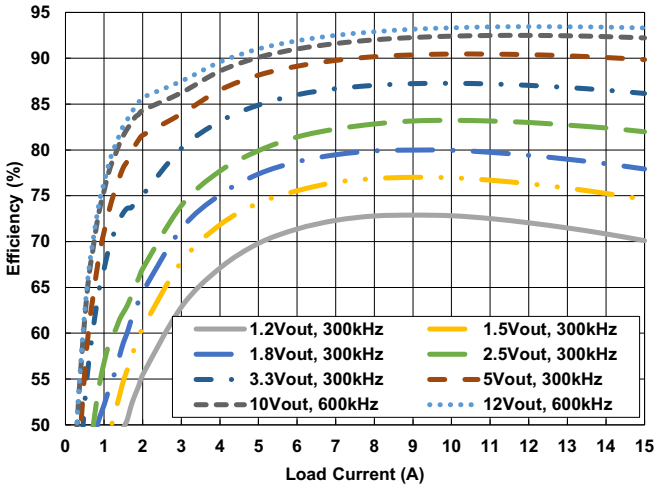


Figure 2. V_{IN} = 48V

Contents

1. Overview

1.1 Typical Application Circuits

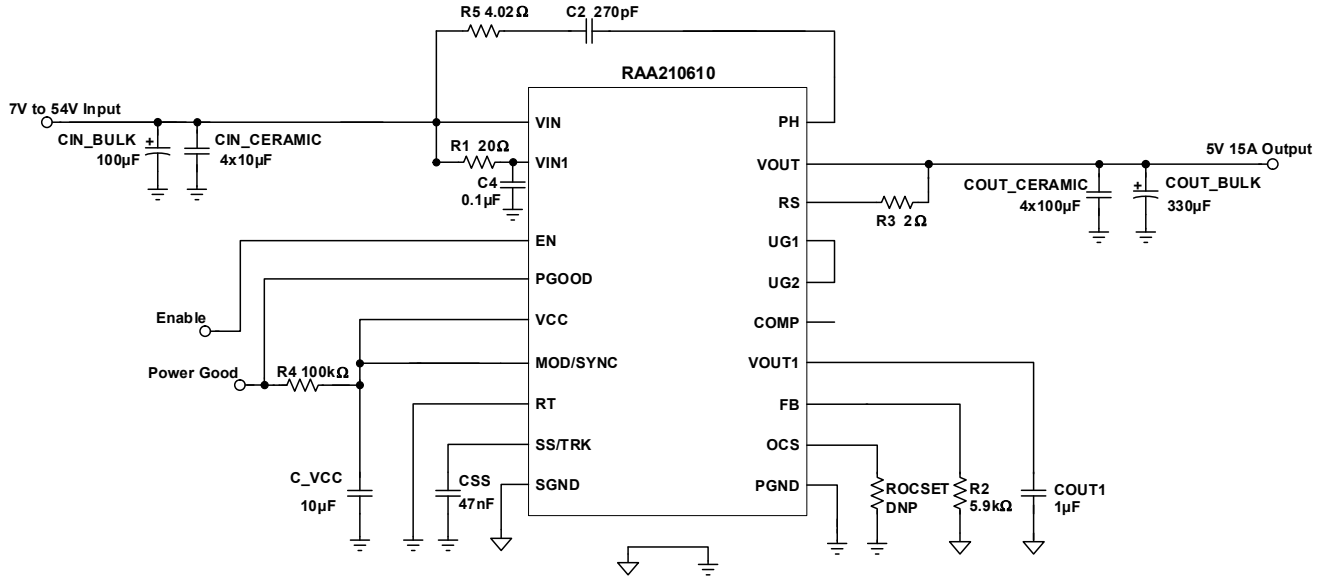


Figure 3. V_{OUT} = 5V, f_{SW} = 300kHz, DEM Mode, t_{SS} = 15ms

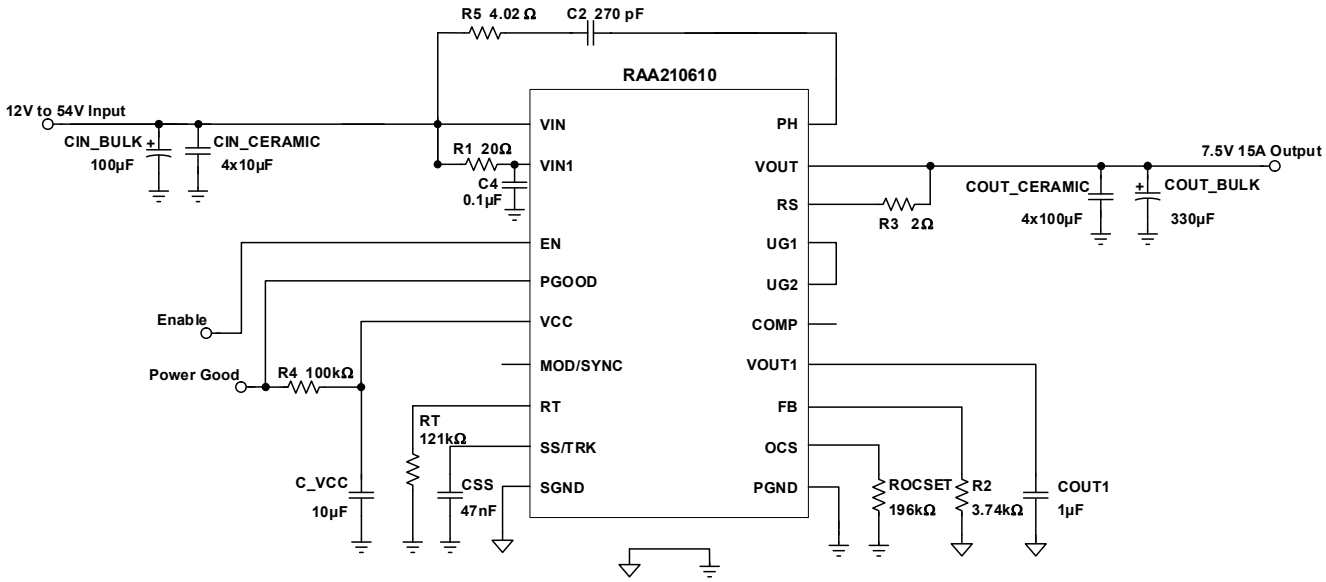


Figure 4. V_{OUT} = 7.5V, f_{SW} = 400kHz, PWM/CCM Mode, t_{SS} = 15ms

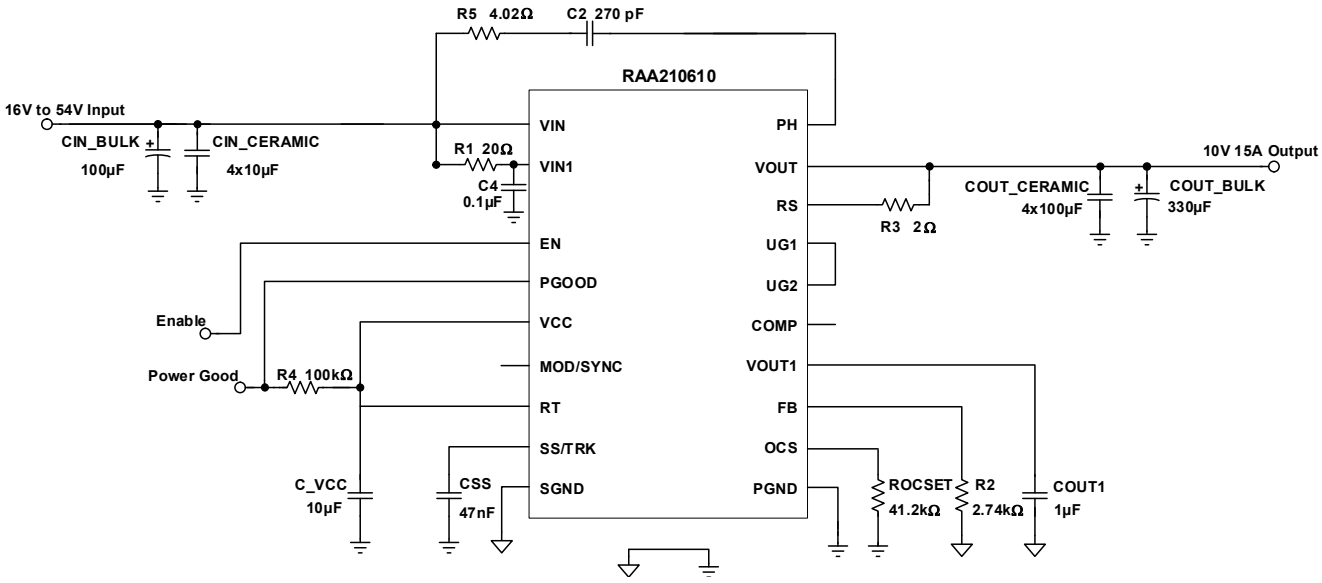


Figure 5. V_{OUT} = 10V, f_{SW} = 600kHz, PWM/CCM Mode, t_{SS} = 15ms

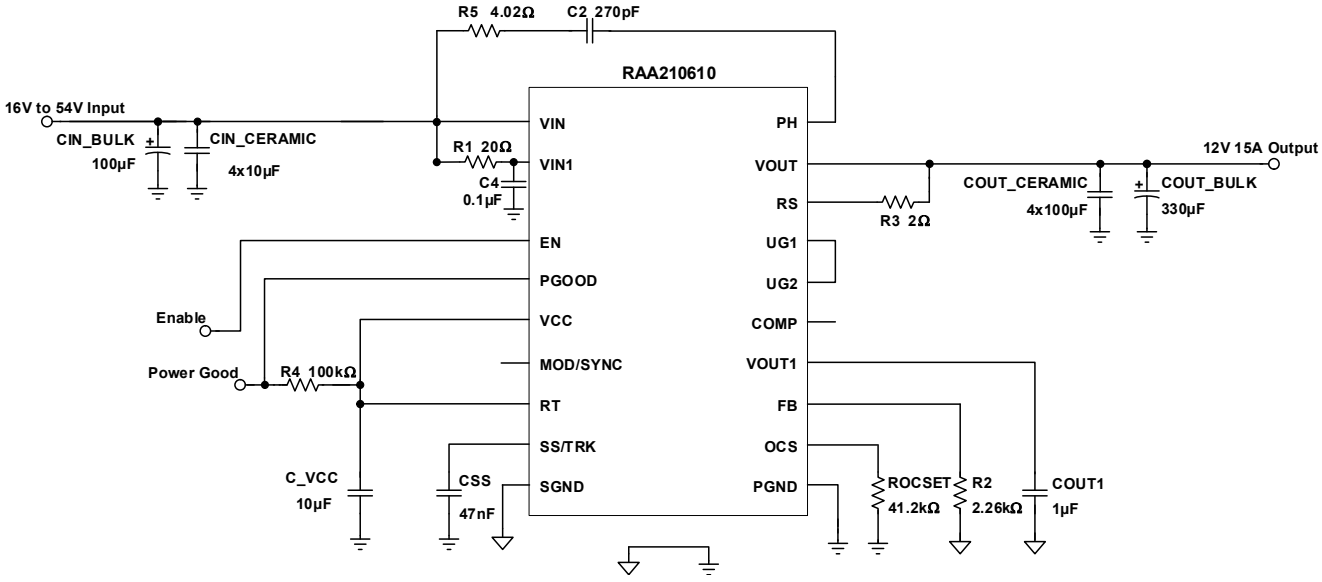


Figure 6. V_{OUT} = 12V, f_{SW} = 600kHz, PWM/CCM Mode, t_{SS} = 15ms

1.2 Block Diagram

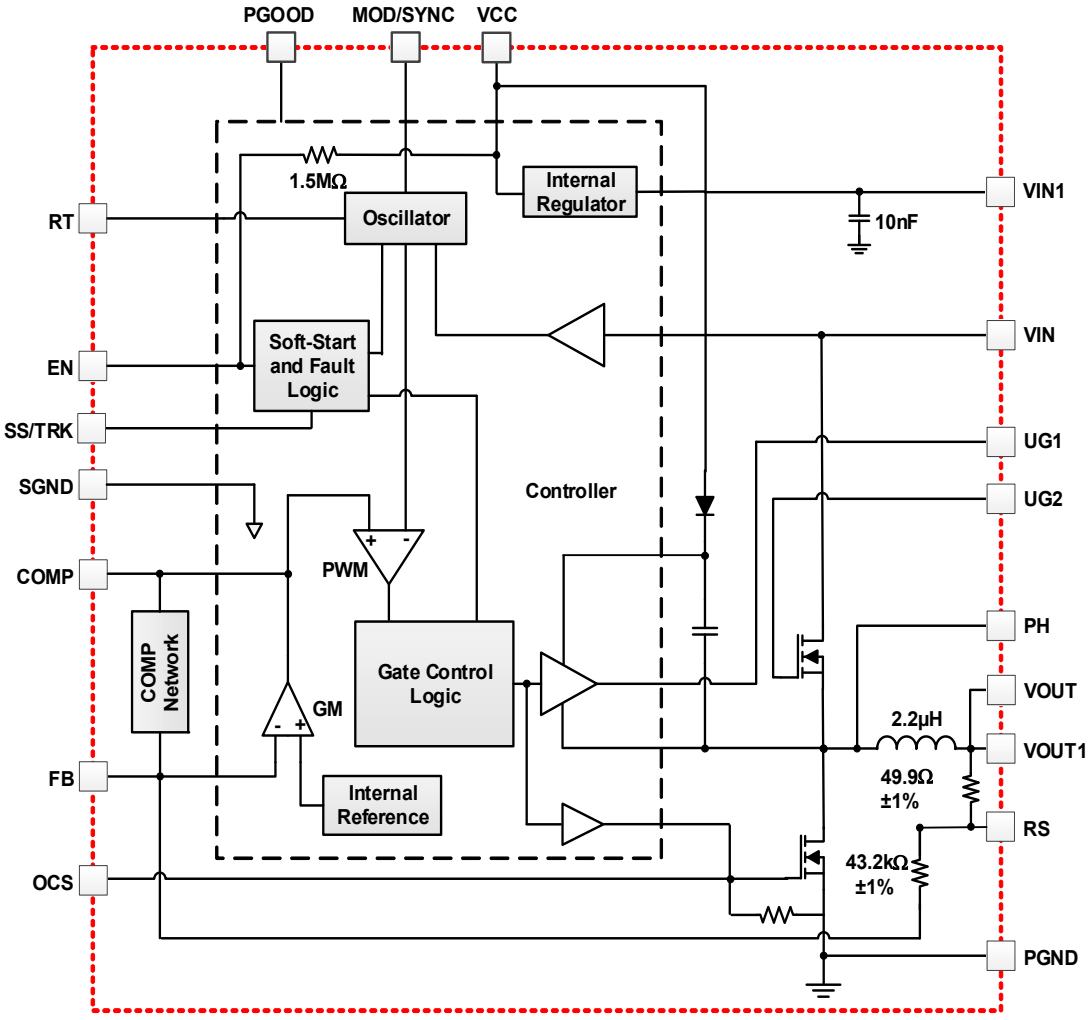


Figure 7. Block Diagram

1.3 Ordering Information

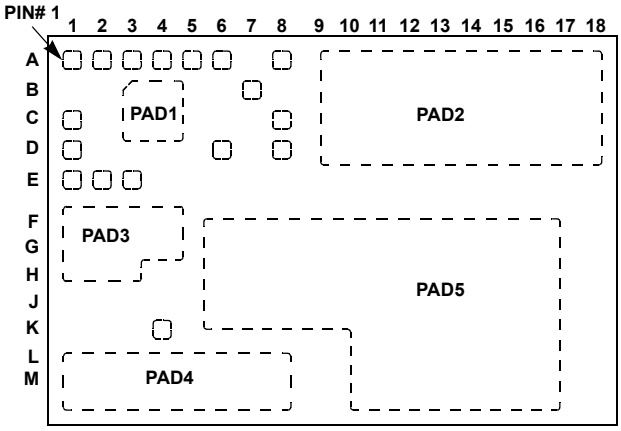
Part Number (Notes 2, 3)	Part Marking	Junction Temperature (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2106104GLG#AD0	RAA2106104	-40 to +125	-	19x13 HDA	Y22.19x13
RAA2106104GLG#HD0	RAA2106104	-40 to +125	350	19x13 HDA	Y22.19x13
RAA2106104GLG#MD0	RAA2106104	-40 to +125	100	19x13 HDA	Y22.19x13
RTKA210610DE0000BU	Evaluation Board				

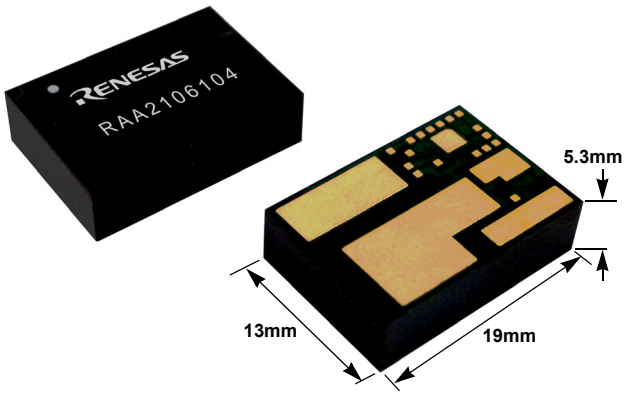
Notes:

1. See TB347 for details about reel specifications.
2. These plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the RAA210610 device page. For information about MSL, see TB363.

1.4 Pin Configuration

22 Ld 19x13 HDA
Top View





1.5 Pin Descriptions

Pin Number	Pin Name	Function
PAD1	SGND	Signal ground. The small-signal ground is common to all control circuitry and all voltage levels are measured with respect to this pin. Tie SGND to a solid low noise GND plane. See "Layout Considerations" on page 28 and Figure 47 on page 29 for details.
PAD2	VOUT	Regulated power module output. Apply the output load between this pin and PGND. An external resistor on the FB pin sets the output voltage in a range of 0.6V to 42V. See "Derating" on page 18 for maximum load current at various output voltages.
PAD3	PGND	Power ground. This pin is connected to the source of the low-side MOSFET inside the module. Connect it to the (-) terminals of the external input capacitors and output capacitors.
PAD4	VIN	Power input. Connect this pin directly to an input rail in a range of 7V to 54V. Connect input ceramic capacitors between this pin and PGND as close as possible to the module.
PAD5	PH	Phase node connection. This pin is connected to the junction source of the high-side MOSFET, output filter inductor, and drain of the low-side MOSFET. A 4.02Ω 1206 resistor and a 270pF X7R 100V 0603 capacitor in series from PH to VIN (see Figures 3 through 6) are required for a switching frequency of 600kHz and a 54V input. See "Layout Considerations" on page 28 for details.
A1	COMP	Voltage error amplifier output. Internal compensation networks are implemented to stabilize the system and achieve optimal transient response across the full range of input and output operating conditions. Leave this pin floating.
A2	SS/TRK	Soft-start/tracking pin. Connecting a capacitor from this pin to power ground sets the soft-start output voltage ramp rate. For tracking control, an external supply rail applied to this pin with a resistor divider is tracked by the output voltage. Leave this pin floating to enable a soft-start time of 1.5ms. See "Tracking Operation" on page 23.
A3	RT	Switching frequency selection. Connect to PGND to set the operating frequency to 300kHz. Connect to VCC or float this pin to set the operating frequency to 600kHz. Connect a resistor from RT to PGND to program the switching frequency. See "Switching Frequency Selection" on page 21.
A4	PGOOD	Open-drain, power-good output. The PGOOD signal is asserted when the output voltage is within ±12.5% of the nominal set output voltage and de-asserted when the output voltage is outside of the stated range or the EN pin is pulled low.
A5	MOD/SYNC	Light-load mode selection/synchronization input. Connect to VCC to enable light load PSM/DEM mode with pulse skipping at light loads. Connect to power ground or leave floating to enable constant frequency PWM/CCM mode. Connect to external clock to synchronize the internal switching operations to an external clock. The module operates in PWM/CCM mode at light-load when synchronized with an external clock.

Pin Number	Pin Name	Function
A6, A8	EN	Enable inputs. Connect to logic high level or leave floating to enable the device. An internal pull-up resistor allows for self enable operations on application of VIN. Connect to logic low level or SGND to disable the device. Connect these two pins together externally through a PCB trace.
B7	VIN1	This pin should be tied to the input rail through a 20Ω 0603 resistor. It provides power to the internal linear drive circuitry and is also used by the feed-forward controller to adjust the amplitude of the PWM sawtooth. Decouple with a 0.1µF ceramic capacitor placed close to this pin.
C1	FB	Feedback input. Connect a resistor between this pin and SGND to adjust the output voltage. See "Output Voltage Programming" on page 21.
D1	RS	Output voltage remote sense feedback. Connect to the positive output regulation point. To achieve best regulation performance, connect a 2Ω resistor between the RS pin and the point of load. Use an internal 49.9Ω resistor connected between the RS pin and the VOUT1 pin to inject a small signal for loop gain measurements.
D6	UG1	High-side MOSFET gate driver output. Connect this pin to UG2 externally through a PCB trace.
K4	UG2	Pin connected to the gate of high-side MOSFET. Connect this pin to UG1 externally through a PCB trace.
E1	VOUT1	Power module output. Connect a 1µF ceramic decoupling capacitor between this pin and SGND.
E2	OCS	Low-side MOSFET gate driver output and OC set pin. Use a resistor between this pin and power ground to set the overcurrent threshold. Inside the module, a 19.1kΩ resistor is connected between this pin and PGND. An external resistor in parallel with the internal 19.1kΩ resistor can be used to reduce the overcurrent threshold. See "Overcurrent Protection (OCP)" on page 26 for more details.
E3	VCC	5V internal linear regulator output. This output supplies bias for the controller, the low-side gate driver and the internal boot circuitry for the high-side gate driver. Decouple with a 10µF ceramic capacitor placed close to the pin to power ground. Do not allow the voltage at VCC to exceed VIN at any time.
C8, D8	NC	No connection. Do not connect these pins.

Table 1. RAA210610 Design Guide Matrix (See Figures 3 Through 6)

Case	V_{IN} (V)	V_{OUT} (V)	R2 (kΩ)	C_{IN} (Bulk) (µF)	C_{IN} (Ceramic) (µF)	C_{OUT} (Bulk) (µF)	C_{OUT} (Ceramic) (µF)	Freq (kHz)	RT (kΩ)	ROCSET (kΩ)	C_7 (pF)	R5 (Package) (Note 4)
1	12	0.8	130	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
2	12	0.9	86.6	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
3	12	1	64.9	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
4	12	1.2	43.2	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
5	12	1.8	21.5	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
6	12	2.5	13.7	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
7	12	3.3	9.53	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0402
9	24	0.9	86.6	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
10	24	1	64.9	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
11	24	1.2	43.2	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
12	24	1.8	21.5	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
13	24	2.5	13.7	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
14	24	3.3	9.53	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
15	24	5	5.90	1x100	4x10	1x330	4x100	300	PGND	DNP	Open	0603
16	36	1.5	28.7	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
17	36	1.8	21.5	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
18	36	2.5	13.7	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
19	36	3.3	9.53	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0603
20	36	5	5.90	1x100	4x10	1x330	4x100	300	PGND	DNP	Open	0603

Table 1. RAA210610 Design Guide Matrix (See Figures 3 Through 6) (Continued)

Case	V_{IN} (V)	V_{OUT} (V)	R2 (kΩ)	C_{IN} (Bulk) (µF)	C_{IN} (Ceramic) (µF)	C_{OUT} (Bulk) (µF)	C_{OUT} (Ceramic) (µF)	Freq (kHz)	RT (kΩ)	ROCSET (kΩ)	C_7 (pF)	R5 (Package) (Note 4)
21	36	7.5	3.74	1x100	4x10	1x330	4x100	400	105	196	Open	0603
22	48	2.5	13.7	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0805
23	48	3.3	9.53	1x100	4x10	1x470	4x100	300	PGND	DNP	Open	0805
24	48	5	5.90	1x100	4x10	1x330	4x100	300	PGND	DNP	Open	0805
25	48	7.5	3.74	1x100	4x10	1x330	4x100	400	105	196	Open	0805
26	48	10	2.74	1x100	4x10	1x330	4x100	600	Open	41.2	Open	1206
27	48	12	2.26	1x100	4x10	1x330	4x100	600	Open	41.2	Open	1206

Note:
4. See "Layout Considerations" on page 28 for more details about package selection size for R5.

Table 2. Recommended Input/Output Capacitor

Vendor	Value	Part Number
Nichicon, Input Bulk	100µF, 63V	UUX1J101MNL1GS
Murata, Input Ceramic	10µF, 100V, 1210, X7S	GRM32EC72A106KE05L
Taiyo Yuden, Output Ceramic	100uF, 16V, 1210, X5R	EMK325ABJ107MM-P
Panasonic, Output Bulk	470µF, 6.3V	6TPF470MAH
KEMET, Output Bulk	330µF, 16V	T521X337M016ATE025
KEMET	270pF, 100V, C0G	C0402C271J1GAC7867

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to PGND	-0.3	+5.9	V
VIN to PGND	-0.3	+56	V
VIN1 to PGND	-0.3	+56	V
EN, FB, COMP to SGND	-0.3	V_{CC} + 0.3	V
VOUT to PGND	-0.3	+48	V
VOUT1 to SGND	-0.3	+48	V
RS to PGND	-0.3	+48	V
UG1 to PHASE	-0.3	V_{CC} + 0.3	V
UG2 to PHASE	-20	+20	V
OCS to PGND	-0.3	V_{CC} + 0.3	V
RT, PGOOD, SS/TRK, MOD/SYNC to PGND	-0.3	V_{CC} + 0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	1.4		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class II, Level A, +125°C)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
22 Ld HDA Package (Notes 5, 6)	11.7	1.9

Notes:

5. θ_{JA} is measured in free air with the module mounted on a 4-layer thermal test board 4.5x3 inch in size with significant coverage of 2oz Cu on all layers, with numerous vias.
6. For θ_{JC}, the case temperature location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VIN to GND	7	54	V
Output Voltage, V_{OUT}	0.6	42	V
Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

Unless otherwise noted, typical specifications are measured at V_{IN} = 7V to 54V, V_{OUT} = 5V, C_V_{CC} = 10µF, T_A = +25°C. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min Note 11	Typ	Max Note 11	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		**7**		**54**	V
Module Input Current						
Shutdown Current Note 7	I_{VINQ}	EN = 0 PGOOD is floating V_{IN} = 48V		5	**10**	µA
Operating Current (PSM/DEM) Note 8	I_{VINOP}	MOD/SYNC = V_{CC} PGOOD is floating V_{IN} = 48V		2.5	**5**	mA
V_{CC} Supply Note 9						
Internal LDO Output Voltage	V_{CC}	V_{IN} = 48V, I_L = 0mA	**4.85**	5.10	**5.40**	V
		V_{IN} > 7V, I_L = 75mA	**4.75**	5.05		V
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	V_{VCC} = 0V, V_{IN} = 12V		120		mA
Output Regulation						
Output Continuous Current Range	I_{OUT}		**0**		**15**	A
Output Voltage Range Note 10	V_{OUT_RANGE}		**0.6**		**42.0**	V
Output Voltage Set-Point Accuracy	V_{OUT_ACCY}	Total variation with line, load, and temperature (-40°C ≤ T_J ≤ +125°C)	**-1.5**		**1.5**	%
Line Regulation	$\Delta V_{OUT}/V_{OUT\_SET}$	V_{IN} from 7V to 54V, I_{OUT} = 0A		0.125		%
Load Regulation	$\Delta V_{OUT}/V_{OUT\_SET}$	From 0A to 15A, V_{IN} = 48V		0.15		%
Output Ripple Voltage	$V_{OUT(AC)}$	V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 15A, 4x100µF ceramic capacitor and 1x330µF POSCAP		45		mV_{P-P}
Dynamic Characteristics						
Voltage Change of Positive Load Step	V_{OUT_DP}	Current slew rate = 2.5A/µs, V_{IN} = 48V, 4x100µF ceramic capacitor and 1x330µF POSCAP V_{OUT} = 5V, I_{OUT} = 0A to 7.5A		60		mV
Voltage Change of Negative Load Step	V_{OUT_DN}	Current slew rate = 2.5A/µs, V_{IN} = 48V, 4x100µF ceramic capacitor and 1x330µF POSCAP V_{OUT} = 5V, I_{OUT} = 7.5A to 0A		60		mV
Undervoltage Lockout						
Undervoltage Lockout, Rising	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on V_{CC}	**3.70**	3.90	**4.20**	V
Undervoltage Lockout, Falling	$V_{UVLOTHF}$	V_{IN} voltage, 0mA on V_{CC}	**3.35**	3.50	**3.85**	V
EN Threshold						
EN Rise Threshold	V_{ENSS_THR}	V_{IN} = 12V	**1.25**	1.60	**1.95**	V
EN Fall Threshold	V_{ENSS_THF}	V_{IN} = 12V	**1.05**	1.25	**1.55**	V
EN Hysteresis	V_{ENSS_HYST}	V_{IN} = 12V	**180**	350	**500**	mV
Soft-Start Current						
SS/TRK Soft-Start Charge Current	I_{SS}	SS/TRK = 0V		2		µA
Default Internal Minimum Soft-Starting						
Default Internal Output Ramping Time	t_{SS_MIN}	SS/TRK open		1.5		ms

Unless otherwise noted, typical specifications are measured at V_{IN} = 7V to 54V, V_{OUT} = 5V, C_V_{CC} = 10µF, T_A = +25°C. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min Note 11	Typ	Max Note 11	Unit
Power-Good Monitors						
PGOOD Upper Threshold	V_{PGOV}		**109.0**	112.5	**115.0**	%
PGOOD Lower Threshold	V_{PGUV}		**85.0**	87.5	**92.0**	%
PGOOD Low-Level Voltage	V_{PGLOW}	I_SINK = 2mA			**0.35**	V
PGOOD Leakage Current	I_{PGLKG}	PGOOD = 5V		20	**150**	nA
PGOOD Timing						
V_{OUT} Rising Threshold to PGOOD Rising Note 12	t_{PGR}			1.1	**5**	ms
V_{OUT} Falling Threshold to PGOOD Falling	t_{PGF}			75		µs
Reference Section						
Internal Reference Voltage	V_{REF}			0.600		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	-0.75		+0.75	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
FB Bias Current	I_{FBLKG}		**-40**	0	**40**	nA
PWM Controller Error Amplifiers						
Input Common-Mode Range		V_{IN} = 12V	0		V_{CC} - 2	V
DC Gain		V_{IN} = 12V		88		dB
Gain-BW Product	GBW	V_{IN} = 12V		8		MHz
Slew Rate	SR	V_{IN} = 12V		2.0		V/µs
COMP V_{OL}		V_{IN} = 12V		0.4		V
COMP V_{OH}		V_{IN} = 12V		2.6		V
COMP Sink Current Note 13		V_{COMP} = 2.5V		30		mA
COMP Source Current Note 13		V_{COMP} = 2.5V		20		mA
PWM Regulator						
Minimum Off-Time Note 13	t_{OFF_MIN}			308		ns
Minimum On-Time Note 13	t_{ON_MIN}			40		ns
Peak-to-Peak Sawtooth Amplitude	DV_{RAMP}	V_{IN} = 20V		1.0		V
		V_{IN} = 12V		0.6		V
Ramp Offset				1.0		V
Switching Frequency						
Switching Frequency	f_{SW}	RT PIN connect to PGND	**250**	300	**350**	kHz
		RT PIN connect to V_{CC} or FLOAT	**515**	600	**645**	kHz
		R_T = 36kΩ	**890**	1050	**1195**	kHz
		R_T = 16.5kΩ	**1650**	2000	**2375**	kHz
R_T Voltage	V_{RT}	R_T = 36kΩ		770		mV
Synchronization						
SYNC Synchronization Range Note 13	F_{SYNC}	R_T = 0Ω	**354**		**1000**	kHz
Diode Emulation Mode Detection						
MOD/SYNC Threshold High Note 13	$V_{MODETHH}$		**1.1**	1.6	**2.1**	V
MOD/SYNC Hysteresis Note 13	$V_{MODEHYST}$			200		mV
Diode Emulation Phase Threshold Note 14	V_{CROSS}	V_{IN} = 12V		-3		mV

Unless otherwise noted, typical specifications are measured at V_{IN} = 7V to 54V, V_{OUT} = 5V, C_V_{CC} = 10µF, T_A = +25°C. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min Note 11	Typ	Max Note 11	Unit
Overvoltage Protection						
OVP Threshold	V_{OVTH}		**116**	121	**127**	%
Overcurrent Protection						
OCP Threshold Note 15	I_{OCTH}	R_{OCSET} resistor open, at +125°C junction		18.3		A
Over-Temperature						
Over-Temperature Shutdown (Controller Junction Temperature)	T_{OT-TH}			150		°C
Over-Temperature Hysteresis	T_{OT-HYS}			15		°C

Notes:

7. This is the total shutdown current.
8. Operating current is the supply current consumed when the module operates at PSM/DEM mode.
9. In normal operation, in which the module is supplied with voltage on the VIN pin, the VCC pin provides a 5V output capable of sourcing 75mA (minimum).
10. Maximum limit 100% production tested up to 5V.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. Controller is independently tested prior to module assembly.
12. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t_{PGR} increases close to its maximum limit 5ms.
13. Compliance to limits is assured by characterization and design.
14. Threshold voltage at PHASE pin for turning off the bottom MOSFET during PSM/DEM.
15. V_{IN} = 48V, V_{OUT} = 5V at 125°C junction.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: T_A = +25°C, no air flow, PWM/CCM mode. Typical values are used unless otherwise noted.

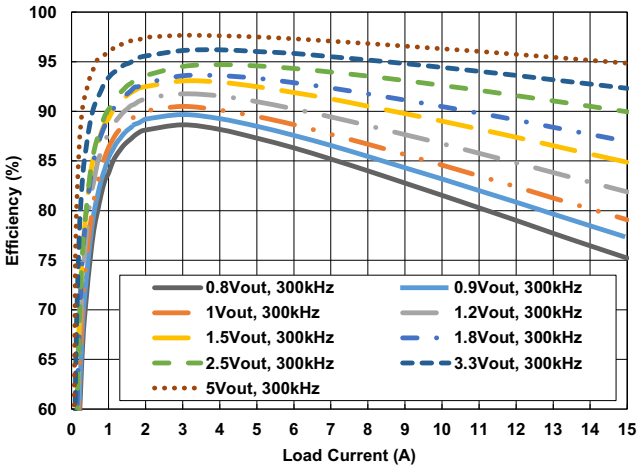


Figure 8. V_{IN} = 7V

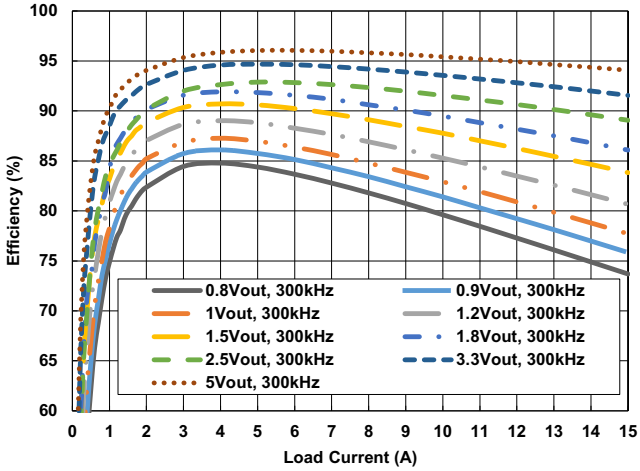


Figure 9. V_{IN} = 12V

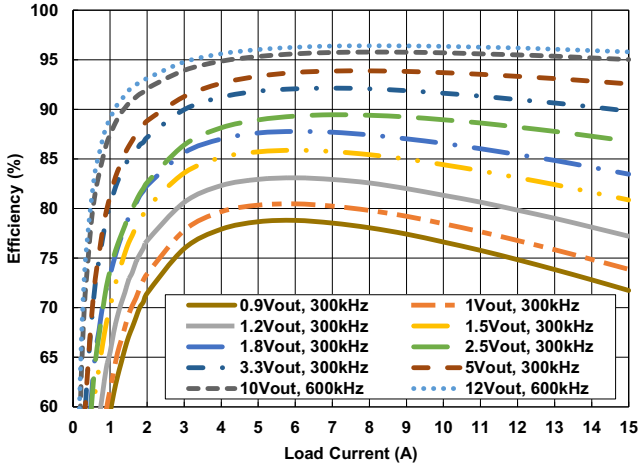


Figure 10. V_{IN} = 24V

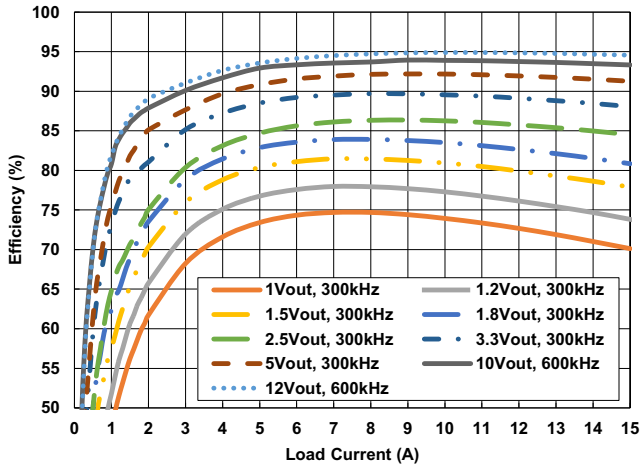


Figure 11. V_{IN} = 36V

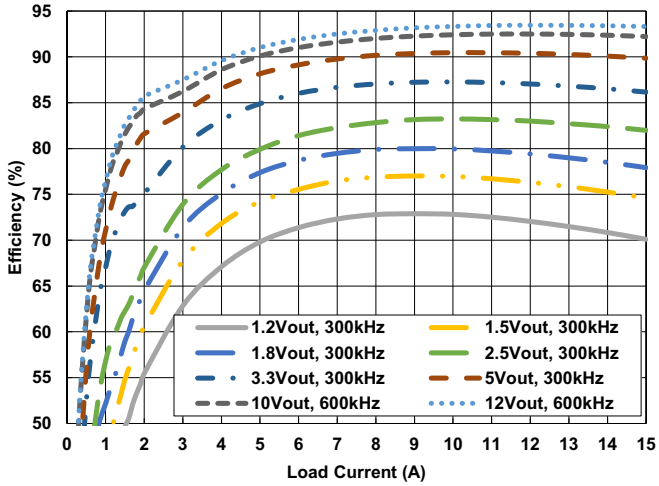


Figure 12. V_{IN} = 48V

3.2 Output Voltage Ripple

Operating condition: T_A = +25°C, no air flow. V_{IN} = 48V, PWM/CCM mode. Typical values are used unless otherwise noted.

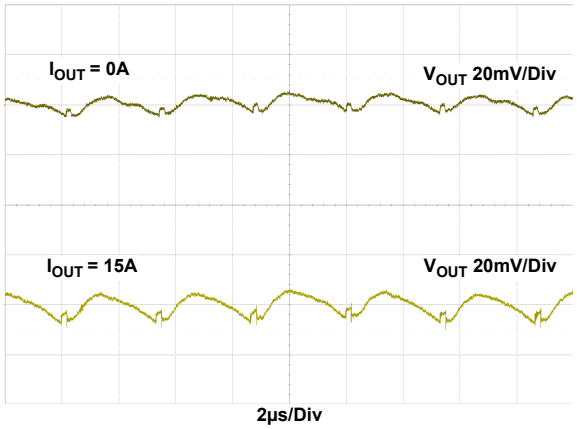


Figure 13. Output Ripple, V_{OUT} = 2.5V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

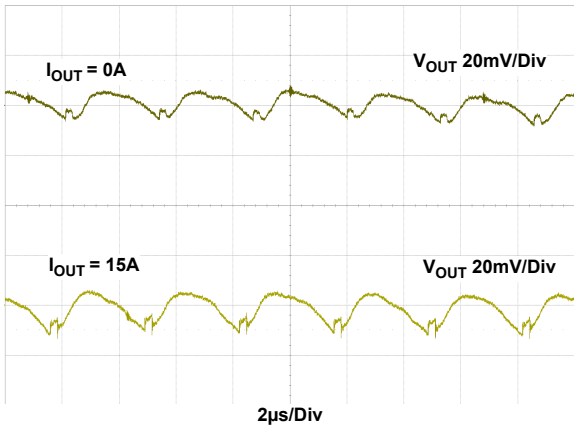


Figure 14. Output Ripple, V_{OUT} = 3.3V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

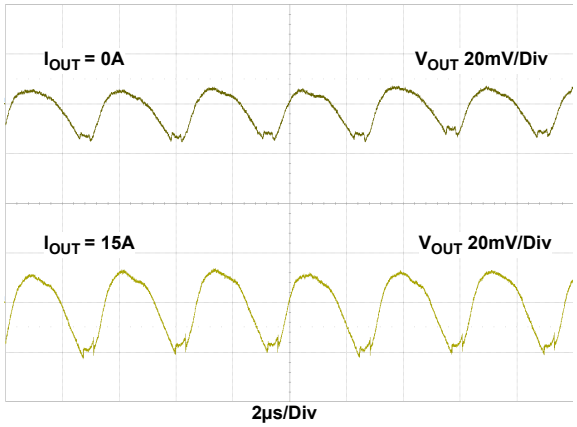


Figure 15. Output Ripple, V_{OUT} = 5V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

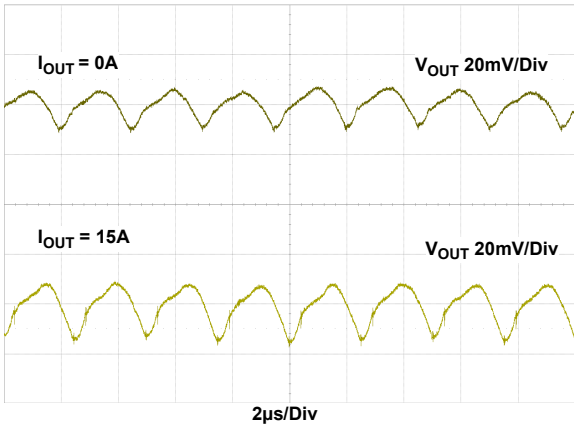


Figure 16. Output Ripple, V_{OUT} = 7.5V, f_{SW} = 400kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

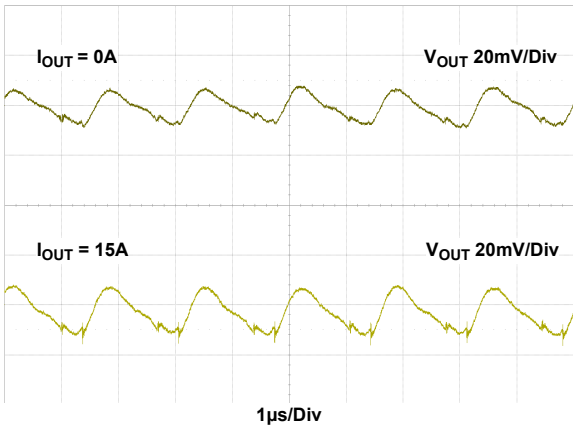


Figure 17. Output Ripple, V_{OUT} = 10V, f_{SW} = 600kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

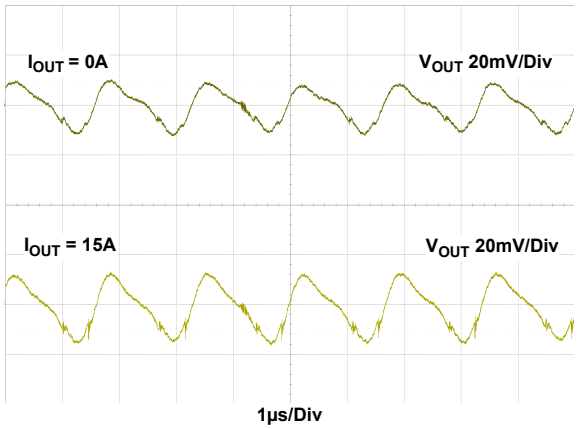


Figure 18. Output Ripple, V_{OUT} = 12V, f_{SW} = 600kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

3.3 Load Transient Response Performance

Operating condition: T_A = +25°C, no air flow. V_{IN} = 48V, PWMCCM mode, 0A - 7.5A, 2.5A/µs step load. Typical values are used unless otherwise noted.

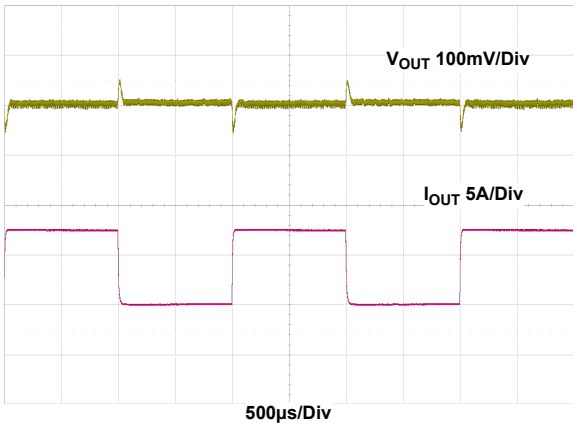


Figure 19. V_{OUT} = 2.5V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

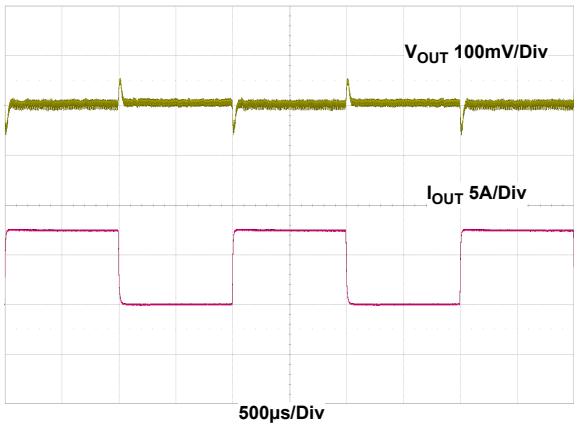


Figure 20. V_{OUT} = 3.3V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x470µF POSCAP

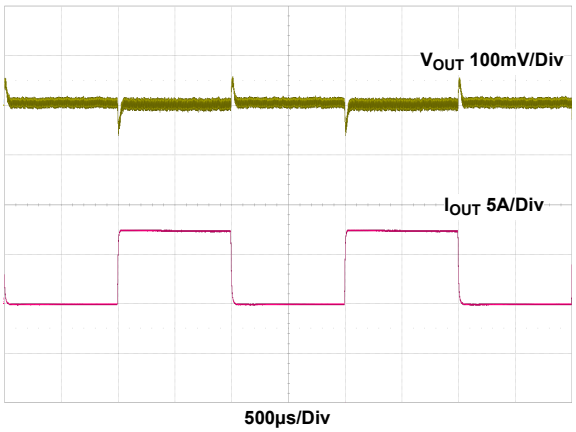


Figure 21. V_{OUT} = 5V, f_{SW} = 300kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

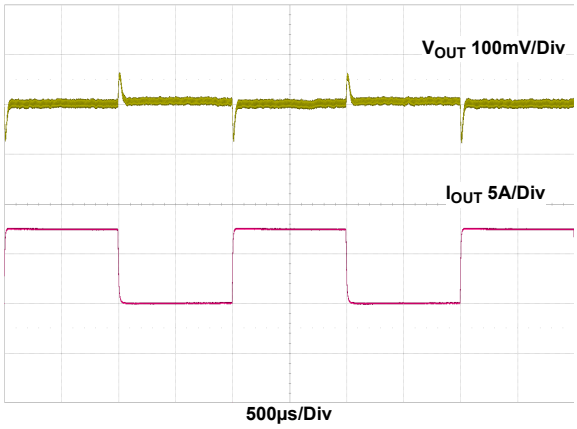


Figure 22. V_{OUT} = 7.5V, f_{SW} = 400kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

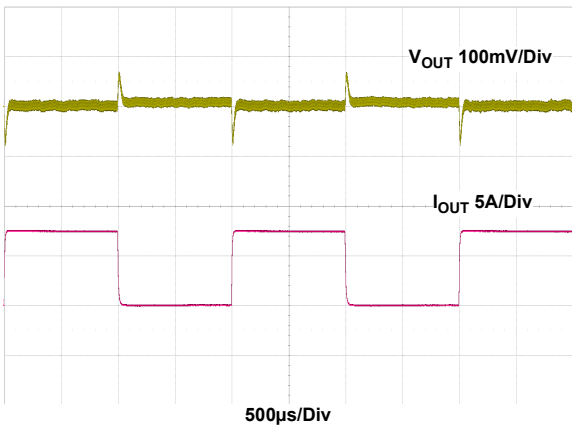


Figure 23. V_{OUT} = 10V, f_{SW} = 600kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

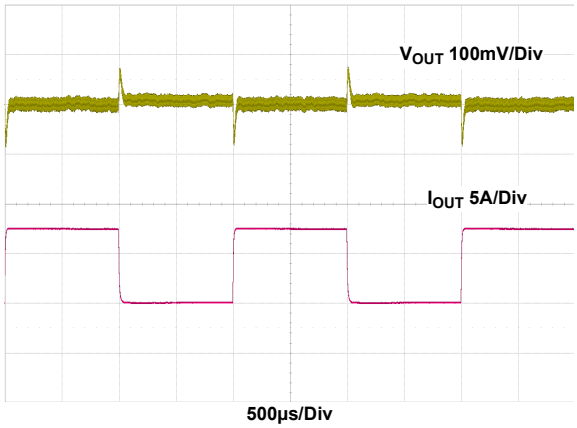


Figure 24. V_{OUT} = 12V, f_{SW} = 600kHz, C_{OUT} = 4x100µF Ceramic + 1x330µF POSCAP

3.4 Start-Up Waveforms

Operating condition: T_A = +25°C, no air flow. V_{IN} = 48V, f_{SW} = 300kHz, C_{OUT} = 4x100µF CERAMIC + 1x330µF POSCAP, PWM/CCM mode. Typical values are used unless otherwise noted.

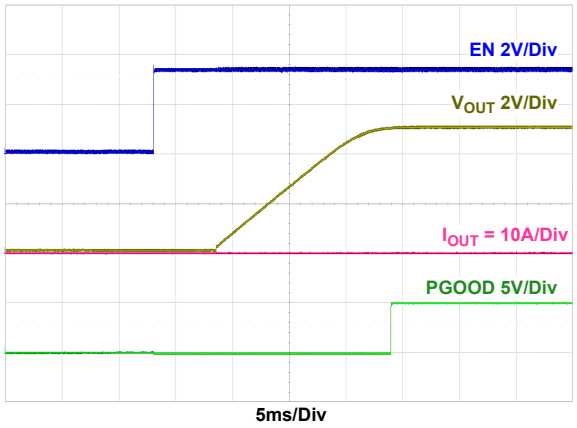


Figure 25. Start-Up Waveforms; V_{OUT} = 5V, I_{OUT} = 0A

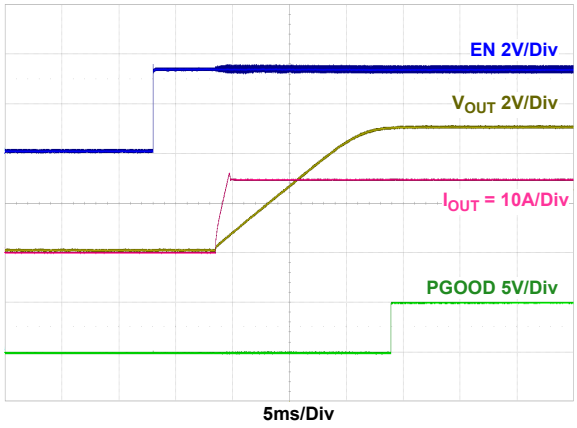


Figure 26. Start-Up Waveforms; V_{OUT} = 5V, I_{OUT} = 15A

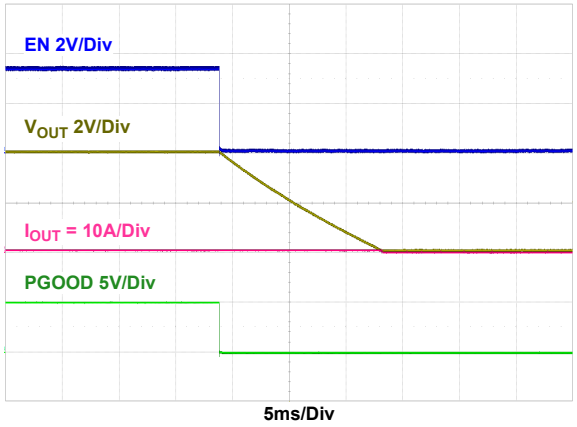


Figure 27. Shutdown Waveforms; V_{OUT} = 5V, I_{OUT} = 0.5A

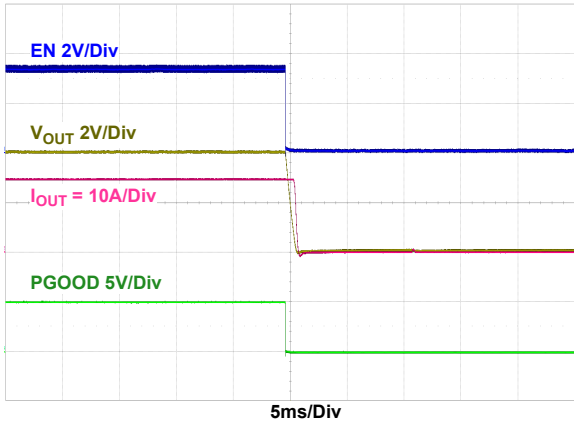


Figure 28. Shutdown Waveforms; V_{OUT} = 5V, I_{OUT} = 15A

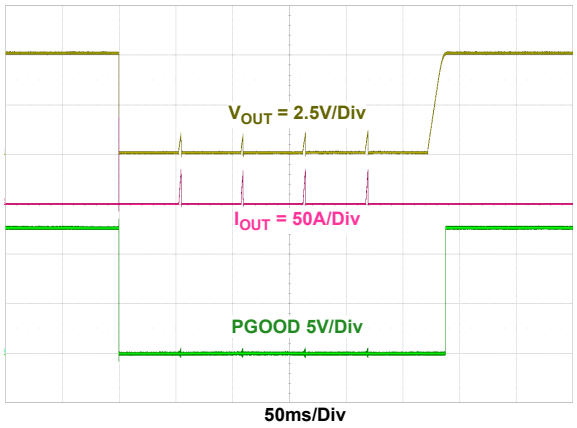


Figure 29. OCP Response; Output Short-Circuited from No Load to Ground and Released, V_{OUT} = 5V, I_{OUT} = 0A

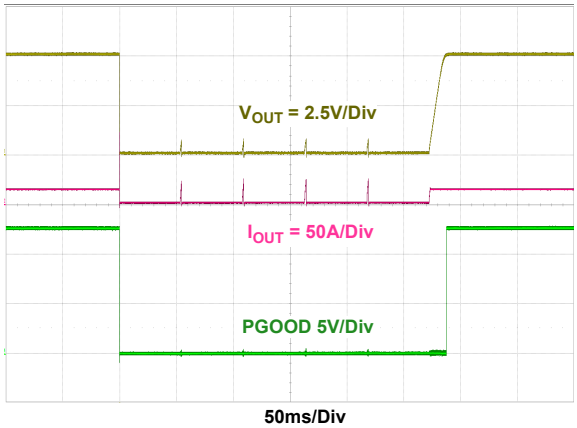


Figure 30. OCP Response; Output Short-Circuited from 15A to Ground and Released, V_{OUT} = 5V, I_{OUT} = 15A

3.5 Derating

Operating condition: V_{IN} = 48V. All of the following curves were plotted at T_J = +125°C.

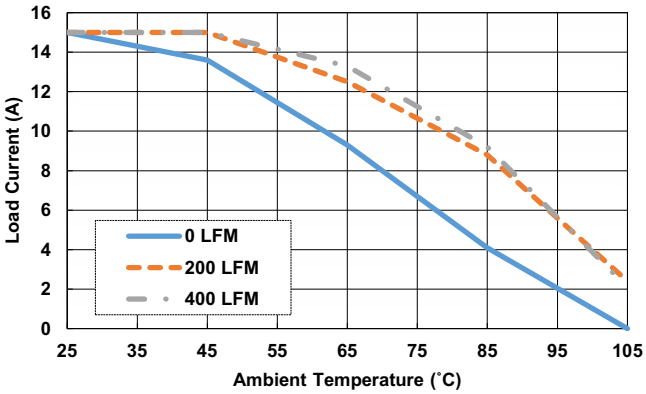


Figure 31. PWM/CCM Mode, V_{OUT} = 2.5V, f_{SW} = 300kHz

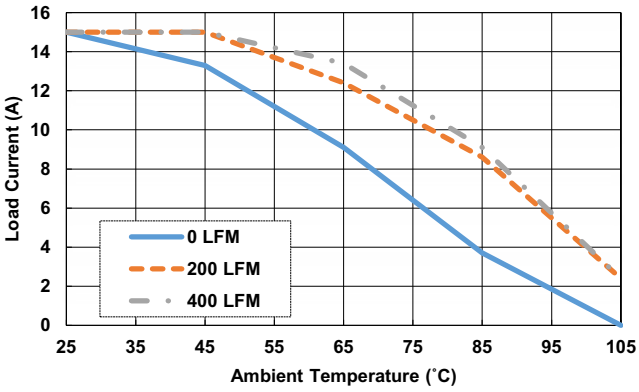


Figure 32. PWM/CCM Mode, V_{OUT} = 3.3V, f_{SW} = 300kHz

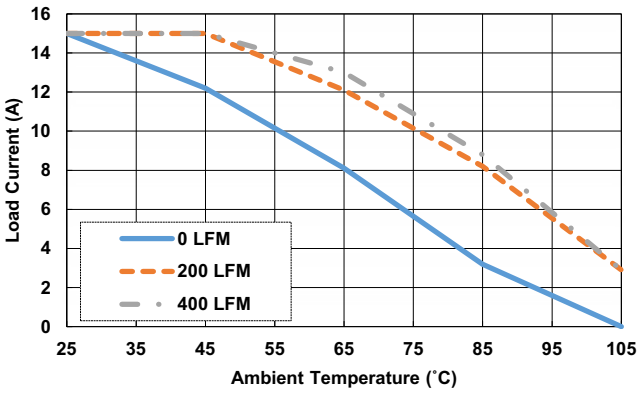


Figure 33. PWM/CCM Mode, V_{OUT} = 5V, f_{SW} = 300kHz

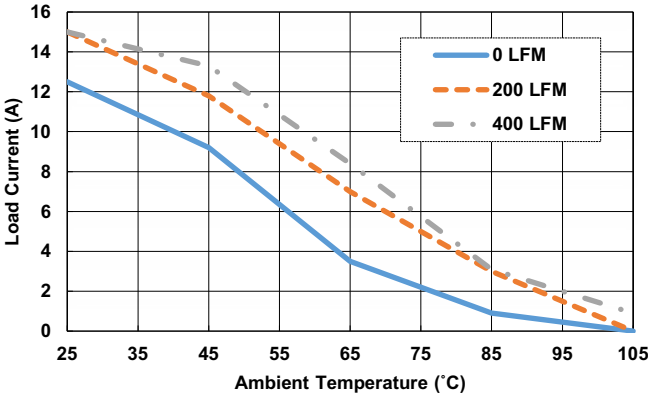


Figure 34. PWM/CCM Mode, V_{OUT} = 7.5V, f_{SW} = 400kHz

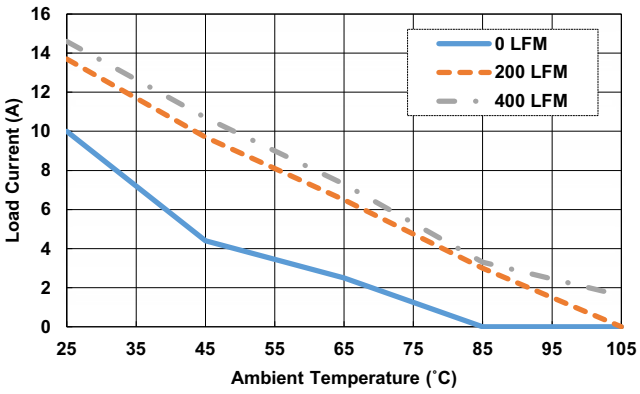


Figure 35. PWM/CCM Mode, V_{OUT} = 10V, f_{SW} = 600kHz

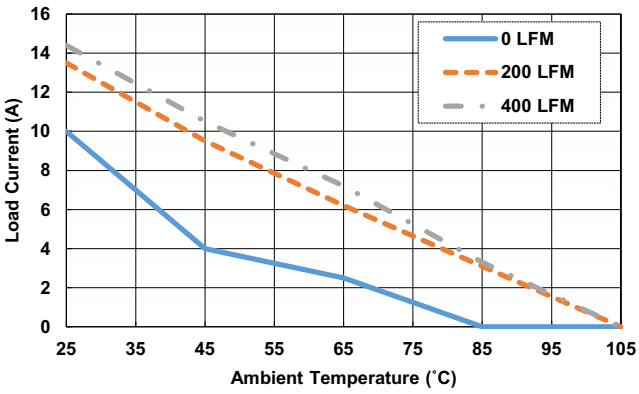


Figure 36. PWM/CCM Mode, V_{OUT} = 12V, f_{SW} = 600kHz

4. Functional Description

4.1 Internal 5V Linear Regulator (V_{CC})

An internal low dropout regulator powers all RAA210610 internal circuitry, allowing the module to operate from a single, wide-input voltage rail from 7V to 54V. For proper operation, decouple the output of this internal LDO (VCC) to power ground with a 10µF capacitor positioned as close as possible to the pin. No other circuitry should be connected to VCC.

4.2 Enable

The RAA210610 is enabled or disabled by driving the EN pin high or low, respectively. When the EN pin voltage reaches 1.6V, the RAA210610 internal circuit is initialized. Pulling the EN low disables all internal circuitry to achieve a low standby current and discharges the SS/TRK pin to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$.

4.3 Self-Enable Operation

Connect an internal pull-up resistor from EN to VCC to allow self-enabling operation. Leaving the EN pin floating enables the RAA210610 as soon as V_{IN} reaches the UVLO threshold, at which point the soft-start circuitry is activated as shown in Figure 37.

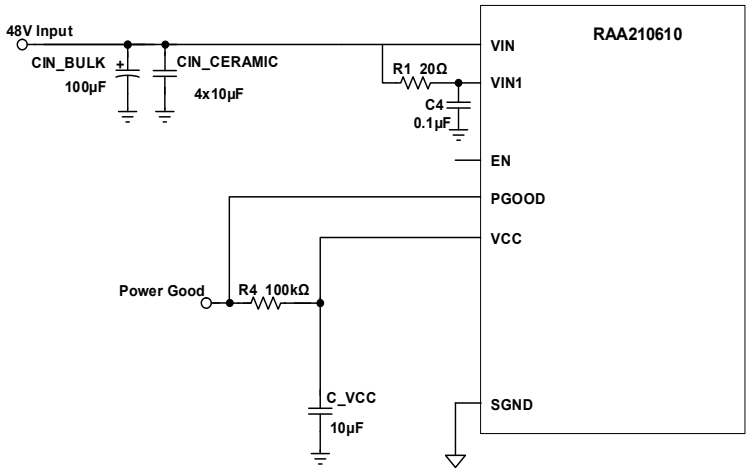


Figure 37. Self-Enable Operation

For operations in which the RAA210610 is required to turn on at a specific input voltage level, external circuitry must be implemented to control the voltage applied on the EN pin through a resistor divider. An optional zener (D1 as shown in Figure 38) may also be required to maintain the EN voltage within the recommended operating conditions.

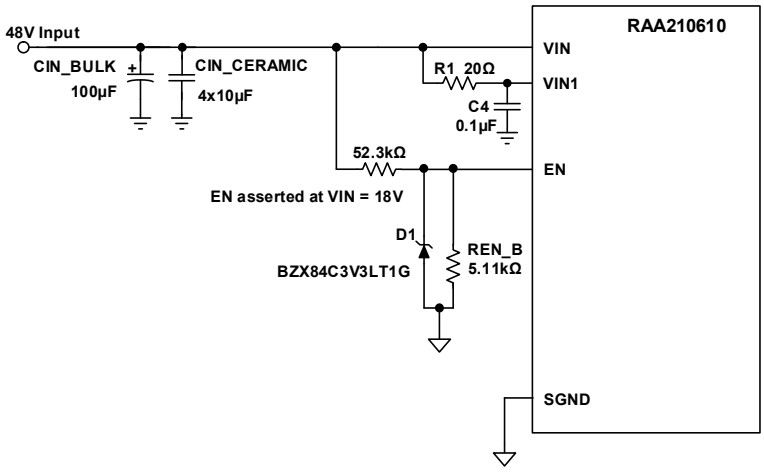


Figure 38. Self-Enable Operation at Minimum 18V_{IN}

4.4 Power-Good Indicator

The power-good signal can be used to monitor the status of the output voltage for undervoltage and overvoltage conditions. This open-drain, PGOOD output is asserted whenever the output voltage is within ±12.5% of the selected target value. This voltage is measured through the feedback resistive divider and therefore is referenced to the internal 0.6V reference. The PGOOD assertion occurs after a 1.1ms blanking delay when the output voltage reaches the regulation window. PGOOD is deasserted without any delay when an output undervoltage or overvoltage is detected or when EN is pulled low.

4.5 Prebiased Power-Up

The RAA210610 can soft-start with a prebiased output. The output voltage is not pulled down during prebiased startup. PWM operations initiate only when the soft-start ramp reaches the prebiased voltage times the resistive divider ratio. Overvoltage protection is active during soft-start operations.

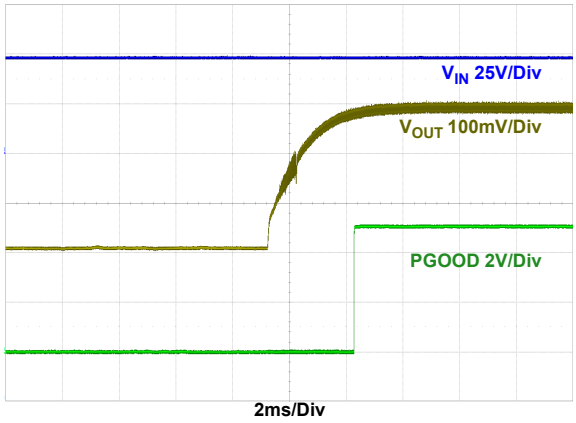


Figure 39. Prebiased Power-Up Waveform, Prebiased Voltage = 4.7V, V_{OUT} = 5V, I_{OUT} = No Load

4.6 PWM/CCM Mode

Tie the MOD/SYNC pin to power ground or leave it floating to select PWM/CCM operation mode. In this mode, the RAA210610 operates at a constant frequency at all load currents. While this mode provides lower conversion efficiency at light current load, it can sometimes be required for applications sensitive to electromagnetic interferences.

4.7 PSM/DEM Light-Load Efficiency Mode

Tie the MOD/SYNC pin to VCC to select the PSM/DEM enhanced light-load efficiency operation mode. In this mode, the RAA210610 operates in high-efficiency Diode Emulation Mode (DEM) and Pulse Skipping Mode (PSM) at light-load conditions. The inductor current is not allowed to reverse (discontinuous operation) while at very light loads, and the RAA210610 enters the pulse skipping function. Although this mode provides increased conversion efficiency at light load, it also increases the output ripple voltage and operates at a non-constant frequency.

4.8 Gate Control Logic Optimization

The RAA210610 implements a specific proprietary MOSFET gate control logic that optimizes the performance across a wide range of operating conditions. This circuitry provides adaptive dead time control by monitoring the real gate waveforms of both the high-side and low-side MOSFETs. A shoot-through control logic provides a 16ns dead time to ensure that both the high-side and low-side MOSFETs do not turn on simultaneously and cause a shoot-through condition.

5. Application Information

5.1 Output Voltage Programming

The RAA210610 supports an adjustable output voltage range of 0.6V to 42V. A single resistor, R_2, placed from FB to SGND sets the output voltage according to Equation 1.

$$R_2 = \frac{(R_1 \times 0.6)}{(V_{OUT} - 0.6)} \quad \text{(EQ. 1)}$$

where R_1 = fixed high-side resistor value of 43.2kΩ ±1% tolerance inside the module and R_2 = resistor connected from FB to SGND in kΩ.

Use Table 3 to select the value of resistor R_2 for typical output voltages. For maximum output voltage accuracy, R_2 should be selected with a tolerance of 0.1% or better.

Table 3. Typical Output Voltage Resistor Settings

V_{OUT} (V)	R_2
0.6	Open
0.8	130kΩ
0.85	104kΩ
0.90	86.6kΩ
0.95	74.1kΩ
1.0	64.9kΩ
1.1	51.7kΩ
1.2	43.2kΩ
1.5	28.7kΩ
1.8	21.5kΩ
2.5	13.7kΩ
3.3	9.53kΩ
5	5.90kΩ
7.5	3.74kΩ
10	2.74kΩ
12	2.26kΩ
20	1.33kΩ
32	0.825kΩ

5.2 Switching Frequency Selection

The switching frequency of the RAA210610 is programmable from 300kHz to 2MHz typical and is set by a resistor connected from the RT pin to power ground according to Equation 2:

$$R_T = \left(\frac{39.2}{f_{SW}} - 1.96\right) k\Omega \quad \text{(EQ. 2)}$$

where f_{SW} is the switching frequency in MHz.

The switching frequency can be set to 300kHz when the RT pin is tied to ground. The switching frequency can be increased to 600kHz if the RT pin is tied to VCC or left floating. Switching frequency selection is a trade-off between efficiency, output voltage ripple, and load transient response requirements. Typically, a low switching frequency improves efficiency by reducing MOSFET switching losses while a high switching frequency improves

the output voltage ripple and transient response in conjunction with the value and type of the output capacitance. Use the frequency setting curve shown in Figure 40 to select the correct value for the resistor R_T.

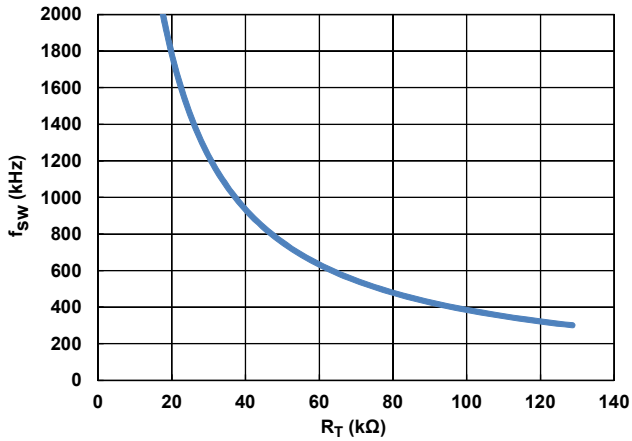


Figure 40. R_T vs Switching Frequency f_{SW}

5.3 External Frequency Synchronization

The RAA210610 can be synchronized to an external clock applied on the MOD/SYNC pin. The external clock should be a square pulse waveform with a frequency in the range of 354kHz - 1MHz. The programmed frequency of the RAA210610 module, which is set by the resistor connected to the RT pin should be lower than the external clock frequency. The duty cycle of the external clock should be within 30% to 70% (typically 50%), while the amplitude should be in the range of 3V to 5V.

To ensure proper operation, the external clock frequency must be at least 18% higher than the programmed default frequency of the module. Disable the module before turning off the external clock. When frequency synchronization is in effect, the RAA210610 operates in forced PWM/CCM mode across all loads.

5.4 Soft-Start Operation

The RAA210610 provides soft-start operations for applications in which inrush current needs to be reduced during startup. A soft-start capacitor placed between the SS/TRK pin and power ground adjusts the soft-start output voltage ramp rate. The typical soft-start time is based on the soft-start capacitor value and set according to Equation 3:

$$t_{SS} = 0.6V\left(\frac{C_{SS}}{2}\right) \quad \text{(EQ. 3)}$$

where C_{SS} is in nF and t_{SS} in ms.

Use the soft-start time setting curve shown in Figure 41 to select the correct value for the capacitor C_{SS}. When the soft-start time set by external C_{SS} or tracking is less than 1.5ms, an internal soft-start circuitry of 1.5ms takes over the soft-start function. Furthermore, overvoltage protection is active during soft-starting operation.

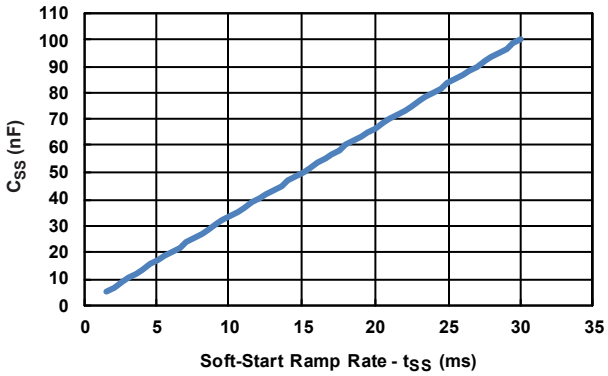


Figure 41. C_{SS} vs t_{SS}

5.5 Tracking Operation

The RAA210610 can be configured to track an external supply, either coincidently or ratiometrically. To implement this functionality, a tracking resistor divider is connected between the external supply output (master rail) and ground. The center point of this resistor divider is connected to the SS/TRK pin of RAA210610 as shown in Figure 42.

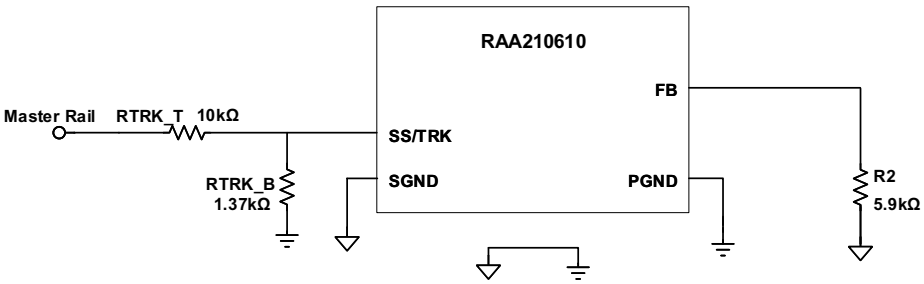


Figure 42. RAA210610 V_{OUT} = 5V - Master Rail Coincidental Tracking - Divider Ratio of 10:1.37 (R_1/R_2)

Coincident tracking is achieved when both the master rail and the RAA210610 output rail reach their respective regulation voltage levels with the same slope. As shown in Figure 43, the master rail and the RAA210610 output rail reach regulation at two different times. Coincident tracking can be achieved by setting the external resistor divider ratio (RTRK_T/RTRK_B) equal to the feedback resistor divider ratio (R_1/R_2) of the RAA210610. Use Table 3 on page 21 to select the appropriate resistor value for different output voltages.

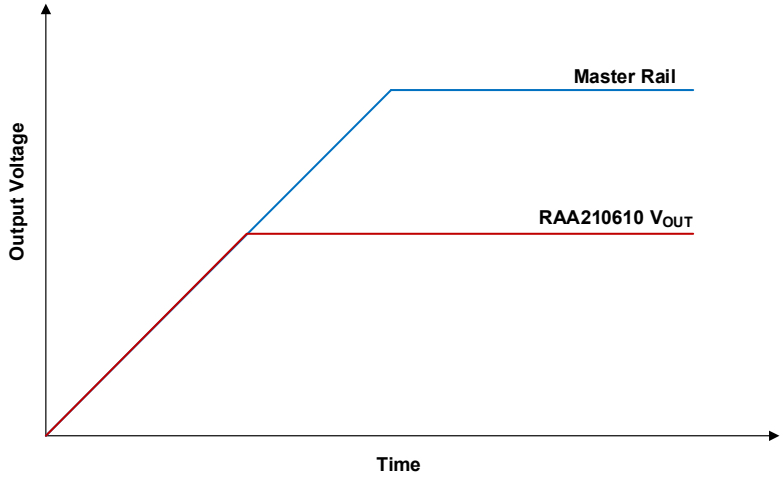


Figure 43. Master Rail Coincidental Tracking

Ratiometric tracking is achieved when the master rail and the RAA210610 output rail both reach their final regulation value at the same time but with different slopes, as shown in Figure 44 on page 24. Use Equation 4 to calculate the resistor divider ratio (RTRK_T/RTRK_B) to implement ratiometric tracking.

$$V_{Master\ rail} \times \frac{RTRK\_B}{RTRK\_B + RTRK\_T} = 0.6 \quad \text{(EQ. 4)}$$

When the voltage at the SS/TRK pin reaches ~550mV, the output voltage is decided by the internal reference of the RAA210610 controller. In addition, the tracking resistor divider of the master rail should include resistors of values less than 10kΩ to minimize the impact of the 2µA soft-start current on the tracking function.

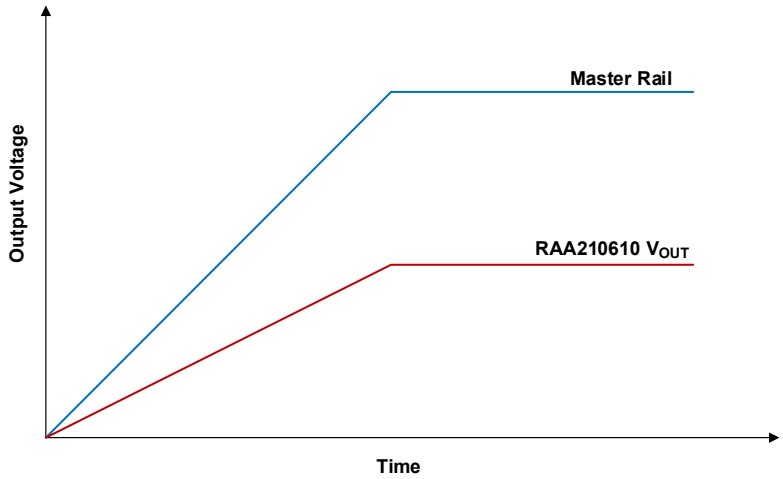


Figure 44. Ratiometric Tracking of Master Rail

5.6 Input Voltage Range

The RAA210610 is designed to operate from a single wide input supply ranging from 7V DC to 54V DC. Limitations on the minimum on-time and minimum off-time required by the RAA210610 limit the minimum and maximum conversion ratios, or duty cycles, supported. By extension, the supported input voltage range for a selected output voltage and selected operating frequency can be effectively reduced.

The maximum input voltage is limited by the minimum on-time ($t_{ON(min)}$), ON-resistance of both the high-side and low-side MOSFETs ($r_{DS(ON)}$), series resistance of the inductor (R_L), and the load current (I_{OUT}) as shown in Equation 5.

$$V_{IN(max)} \leq \left(\frac{V_{OUT} + I_{OUT} \times (r_{DS(ON)} + R_L)}{t_{ON(min)} \times f_{SW}}\right) \quad \text{(EQ. 5)}$$

where $t_{ON(min)}$ = 40ns typically in PWM/CCM mode and f_{SW} is the switching frequency in Hz. $r_{DS(ON)}$ = 7.4mΩ typically and 9.4mΩ maximum. R_L = 6.7mΩ typically and 7mΩ maximum.

Likewise, the minimum input voltage is limited by the minimum off-time ($t_{OFF(min)}$) as shown in Equation 6.

$$V_{IN(min)} \geq \left(\frac{V_{OUT} + I_{OUT} \times (r_{DS(ON)} + R_L)}{1 - t_{OFF(min)} \times f_{SW}}\right) \quad \text{(EQ. 6)}$$

where $t_{OFF(min)}$ = 308ns typically.

5.7 Input Capacitor Selection

The important parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC_{RMS} input current varies with the load given in Equation 7:

$$I_{RMS} = \sqrt{D(1-D)} \cdot I_{OUT} \quad \text{(EQ. 7)}$$

where D is duty cycle of the PWM.

The maximum RMS current supplied by the input capacitance occurs at $V_{IN} = 2 \times V_{OUT}$, D = 50% as shown in Equation 8:

$$I_{RMS} = \frac{1}{2} \cdot I_{OUT} \quad \text{(EQ. 8)}$$

See the capacitor vendor to check the RMS current rating. **Note:** The current rating is decided by the ambient temperature or temperature rise. Each 1210 size 10µF low ESR capacitor is typically sufficient for 2A to 3A RMS ripple current.

Use a mix of input bypass capacitors to control the voltage stress across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the MOSFETs to suppress the voltage induced in the parasitic circuit impedances.

Solid tantalum capacitors can be used; however, use caution with regard to the capacitor surge current rating. These capacitors must be able to handle the surge current at power-up.

5.8 Output Capacitor Selection

The RAA210610 is designed for low output voltage ripple. In general, select output capacitors to meet the dynamic regulation requirements including ripple voltage and load transients. These requirements can be met with bulk output capacitors that have adequately low ESR and ESL.

High frequency capacitors initially supply the transient current and slow the slew rate of load transient seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR and ESL and voltage rating requirements, as well as actual capacitance requirements.

Place high frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low ESR/ESL components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low ESR capacitors intended for switching regulator applications for the bulk capacitors. In most cases, multiple small case electrolytic capacitors perform better than a single large case capacitor.

In conclusion, the output capacitors must meet the following criteria:

- They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.

The recommended output capacitor value for the RAA210610 is between 400µF and 1000µF. See Tables 1 and 2 on page 9 for more capacitor information. All ceramic capacitors are possible with loop analysis to ensure stability.

6. Protection Circuits

6.1 Undervoltage Lockout (UVLO)

The RAA210610 includes UVLO protection, which keeps the module in a reset condition until a proper operating voltage is applied. The UVLO protection also shuts down the RAA210610 if the operating voltage drops below a predefined value. When assertion of the UVLO state occurs, the module is completely disabled. PGOOD is valid and is deasserted.

6.2 Overcurrent Protection (OCP)

The RAA210610 uses the ON-resistance ($r_{DS(ON)}$) of the low-side MOSFET to monitor the current in the converter. The sensed voltage drop across the drain-to-source of the MOSFET is compared to a threshold voltage set by the resistor (R_{OCSET}) connected from the OCS pin to ground. Because $r_{DS(ON)}$ is higher at hot temperatures and lower at cold temperatures, the OCP setpoint at room and cold temperatures is higher than the OCP setpoint at hot temperatures.

For applications involving less than 15A load, Renesas recommends further reducing the OCP setpoint to improve the system reliability. Use Equation 9 to calculate the value of the OCP set resistor.

$$R_{OCSET} = \frac{(19.1 \cdot R_{Nom} \cdot (I_O / 15))}{(R_{Nom} \cdot (1 - (I_O / 15)) + 19.1)} k\Omega \quad \text{(EQ. 9)}$$

where

- I_O = Desired full load current (A)
- R_{OCSET} = Resistor connected to the OCS pin (kΩ)
- R_{Nom} = R_{OCSET} resistor to ensure 15A full load operation (kΩ)
- R_{OCSET} values for ensuring 15A full load operation:
  - 20MΩ for 5V output and below (simulating a Do Not Populate (DNP) condition)
  - 196kΩ for 7.5V output
  - 41.2kΩ for 10V and 12V output

Take the OCP setpoint at 12V output voltage and 7.5A load current for example. R_{Nom} = 41.2kΩ at 12V output voltage and I_O = 7.5A. According to Equation 9, R_{OCSET} = 10kΩ.

In Equation 9 the typical load current to hit OCP at +120°C is set to around 20% higher than the desired full load current. The 20% margin is due to the controller OCP and the MOSFET $r_{DS(ON)}$ tolerance.

If an overcurrent is detected, the high-side MOSFET remains off and the low-side MOSFET remains on until the next cycle. As a result, the converter skips a pulse. When the overload condition is removed, the converter resumes normal operation. If an overcurrent is detected for two consecutive clock cycles, the module enters Hiccup mode by turning off the gate driver and entering soft-start. The RAA210610 stays off for 50ms before trying to restart and continues to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start, so ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

When OCP is triggered, the SS/TRK pin is pulled to ground by an internal MOSFET for hiccup restart. When configured to track another voltage rail, the SS/TRK pin rises up much faster than the internal minimum soft-start ramp. The voltage reference is then clamped to the internal minimum soft-start ramp. Thus, smooth soft-start hiccup is achieved even with the tracking function.

6.3 Overvoltage Protection (OVP)

The overvoltage set point is set at 121% of the nominal output voltage set by the feedback resistors. If an overvoltage event occurs, the module attempts to bring the output voltage back into regulation by keeping the high-side MOSFET turned off and the low-side MOSFET turned on. If the overvoltage condition is corrected and

the output voltage returns to 110% of the nominal output voltage, both high-side and low-side MOSFETs turn off until the output voltage drops to the nominal voltage to start work in normal PWM switching.

6.4 Over-Temperature Protection (OTP)

The module incorporates an over-temperature protection circuit that shuts down the module when a die temperature of +150°C is reached. Normal operation resumes when the die temperature drops below +145°C through the initiation of a full soft-start cycle. During OTP shutdown, the module consumes only 100µA current. When the module is disabled, the thermal protection is inactive. This helps achieve a very low shutdown current of 5µA.

7. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an RAA210610 based DC/DC converter. The RAA210610 switches at a very high frequency. Therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. The peak gate drive current also rises significantly in an extremely short time. Current transition speed from one MOSFET to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device overvoltage stress and ringing. Careful component selection and proper PCB layout minimize the magnitude of these voltage spikes.

7.1 Layout Considerations

1. Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND, as close to the module as possible. The loop formed by the input capacitor, VIN pad, and PGND must be as small as possible to minimize the high frequency noise. Place the output capacitors close to the load. Use short, wide copper planes to connect the output capacitors to the load to avoid any parasitic inductances and resistances. A layout example is shown in Figures 45 and 46 on page 29.
2. Use large copper planes to minimize conduction loss and thermal stress for VIN, VOUT, and PGND. Use enough vias to connect the power planes in different layers.
3. Use full ground planes in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Renesas recommends using slots (as shown in Figure 47 on page 29) to ensure that the switching current avoids the SGND pad of the module. Use as much GND plane as possible for the layer directly above the bottom layer (containing components such as input caps and output caps). Use the top and bottom layer to route the EN, VCC, and PGOOD signals.
4. For a switching frequency of 300kHz and a 54V input, connect a 4.02Ω 0805 resistor and a 270pF 100V X7R 0603 capacitor in series from PH to VIN. Derate the resistor size for switching frequencies higher than 300kHz. Calculate the power dissipated in resistor R5 (P_{cal}) by using the formula $C \times V^2 \times f$, where:
   a. C = 270pF
   b. V = input voltage
   c. f = frequency of operation
   For derating purposes, the nominal power handling capability of the resistor package size should be at least $P_{cal}/0.65$. The 65% derating is derived from the resistor operation at +100°C ambient temperature. Use a standard thick film chip resistor datasheet to find the correct resistor package size for different switching frequencies and input voltage.
5. Make sure that UG1 and UG2 (D6 and K4) are connected externally through a PCB trace. Make a similar connection for the two EN pins (A6 and A8). See "Pin Configuration" on page 7 and "Pin Descriptions" on page 7.
6. Use a remote sensing trace to connect to the VOUT+ of load to achieve a tight output voltage regulation. Route the remote sense trace underneath the GND layer and avoid routing the sense lines near noisy planes such as the PHASE node. Place a 2Ω resistor close to the RS pin to damp the noise on the traces.
7. To avoid ground bouncing issues, place the VIN return and the VOUT return diagonally opposite to each other. This ensures that the switching noise generated by the power-train has minimal effect on the controller operation.
8. Do not unnecessarily oversize the copper islands for the PHASE node. Because the phase nodes are subjected to very high dv/dt voltages, the parasitic capacitor formed between these islands and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE node plane.
9. Place the VCC bypass capacitor underneath the VCC pin and connect its ground to the PGND pad. Connect the low-side feedback resistor and the decoupling cap for VOUT1 to the SGND pad.

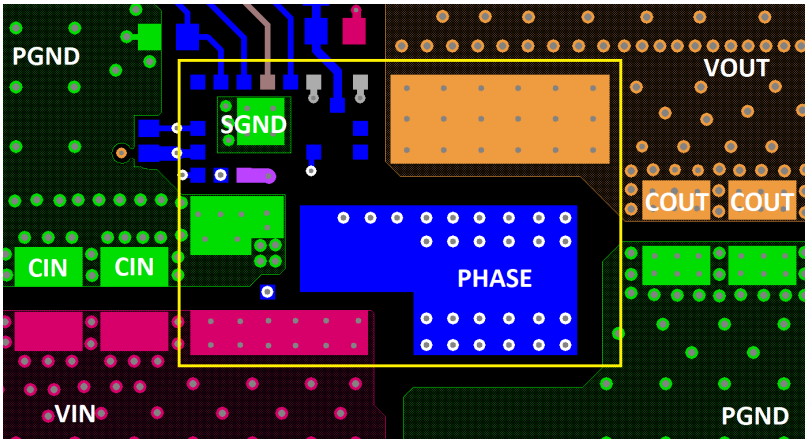


Figure 45. Layout Example - Top Layer

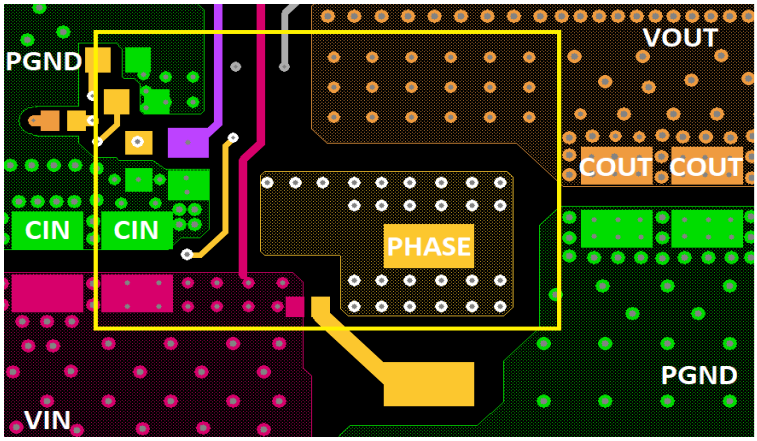


Figure 46. Layout Example - Bottom Layer

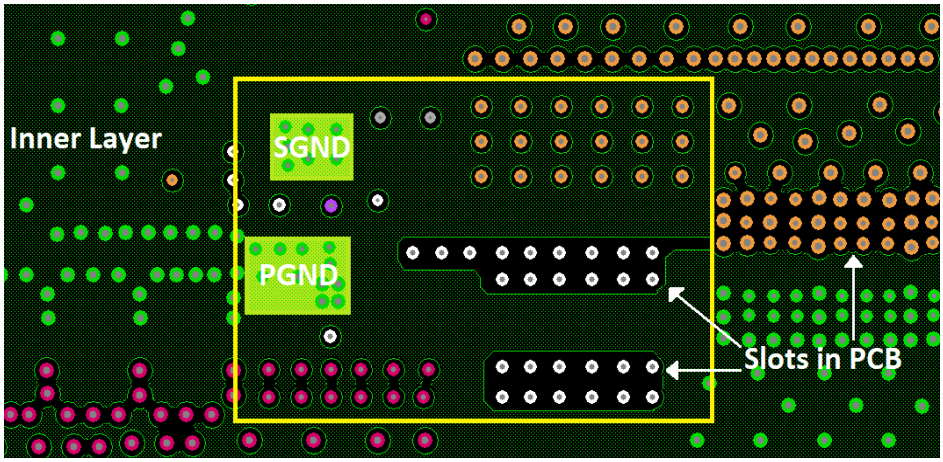


Figure 47. Layout Example - SGND is Connected to PGND Through Internal Layer

7.2 Thermal Considerations

Experimental power loss curves, along with θ_{JA} from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining temperature below the maximum junction temperature of +125°C. In applications in which the system parameters and layout are different from the evaluation board, the customer can adjust the margin of safety. All derating curves are obtained from the tests on a 4-layer thermal test board 4.5x3 inches in size. See TB379 for more details. In the actual application, other heat sources and design margins should be considered.

8. Package Description

The RAA210610 uses the High Density Array no-lead package (HDA). This kind of package has advantages such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210610 contains several types of devices, including resistors, capacitors, MOSFETs, inductors, and control ICs. The RAA210610 is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi-component assembly is overmolded with polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern design, and typical stencil pattern design are shown in the Package Outline Drawing starting on page 33. The module has a small size of 19mmx13mmx5.3mm.

8.1 PCB Layout Pattern Design

The bottom of the RAA210610 is a lead-frame footprint that is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on page 36 and page 37. The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50% to 80% of the available module I/O area.

8.2 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as more vias are added. Use as many vias as practical for the thermal land size and your board design rules allow.

8.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown on page 34 and page 35. Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

8.4 Reflow Parameters

Due to the low mount height of the HDA, No Clean Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile in Figure 48 is provided as a guideline to be customized for varying manufacturing practices and applications.

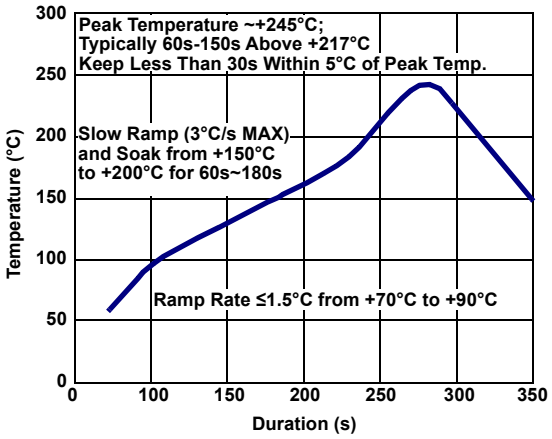


Figure 48. Typical Reflow Profile

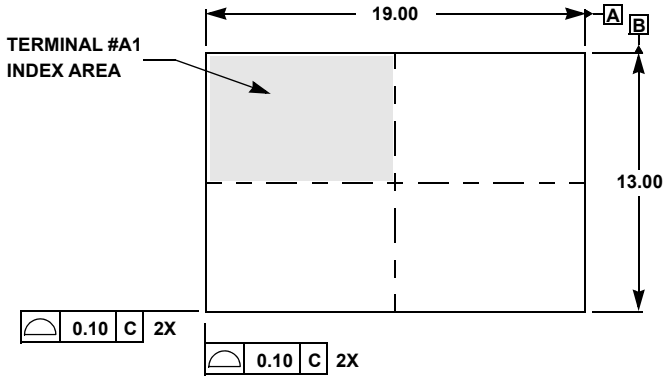
9. Revision History

Rev.	Date	Description
2.00	Feb.2.21	In the Abs Max Rating section changed the maximum values from 16V to 48V for the VOUT to PGND, VOUT1 to SGND, and RS to PGND parameters.
1.03	Jun.19.20	Updated the descriptions for Equations 5 (page 24) and 9 (page 26).
1.02	Mar.19.20	Updated Figures 1, 3, 4, 5, 6, 37 and 38. Updated VIN1, OCS, and RT pin descriptions. Updated Table 1. Updated Abs Max Parameter names.
1.01	Jan.16.20	Added Figure 34.
1.00	Dec.17.19	Initial release

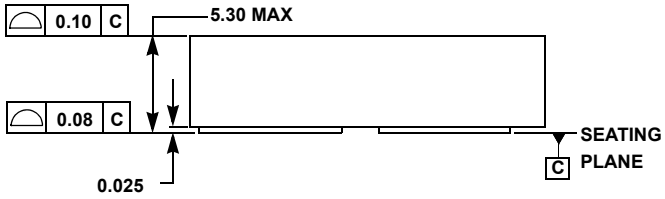
10. Package Outline Drawing

For the most recent package outline drawing, see Y22.19x13.

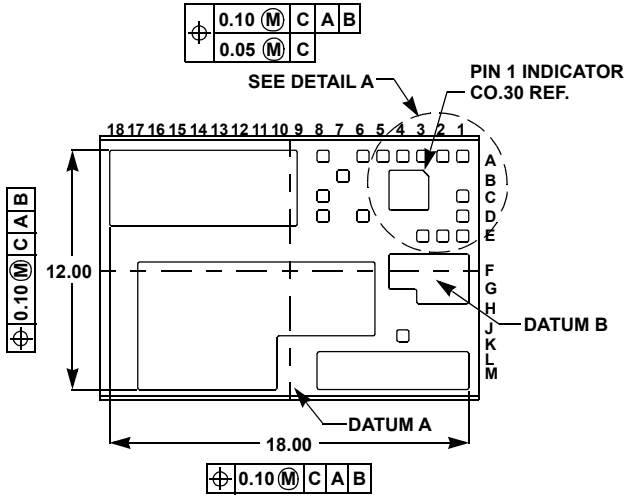
Y22.19x13
22 I/O 19mmx13mmx5.30mm HDA MODULE
Rev 1, 11/16



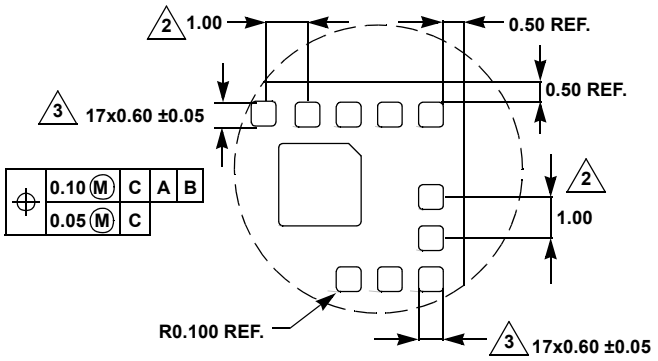
TOP VIEW



SIDE VIEW



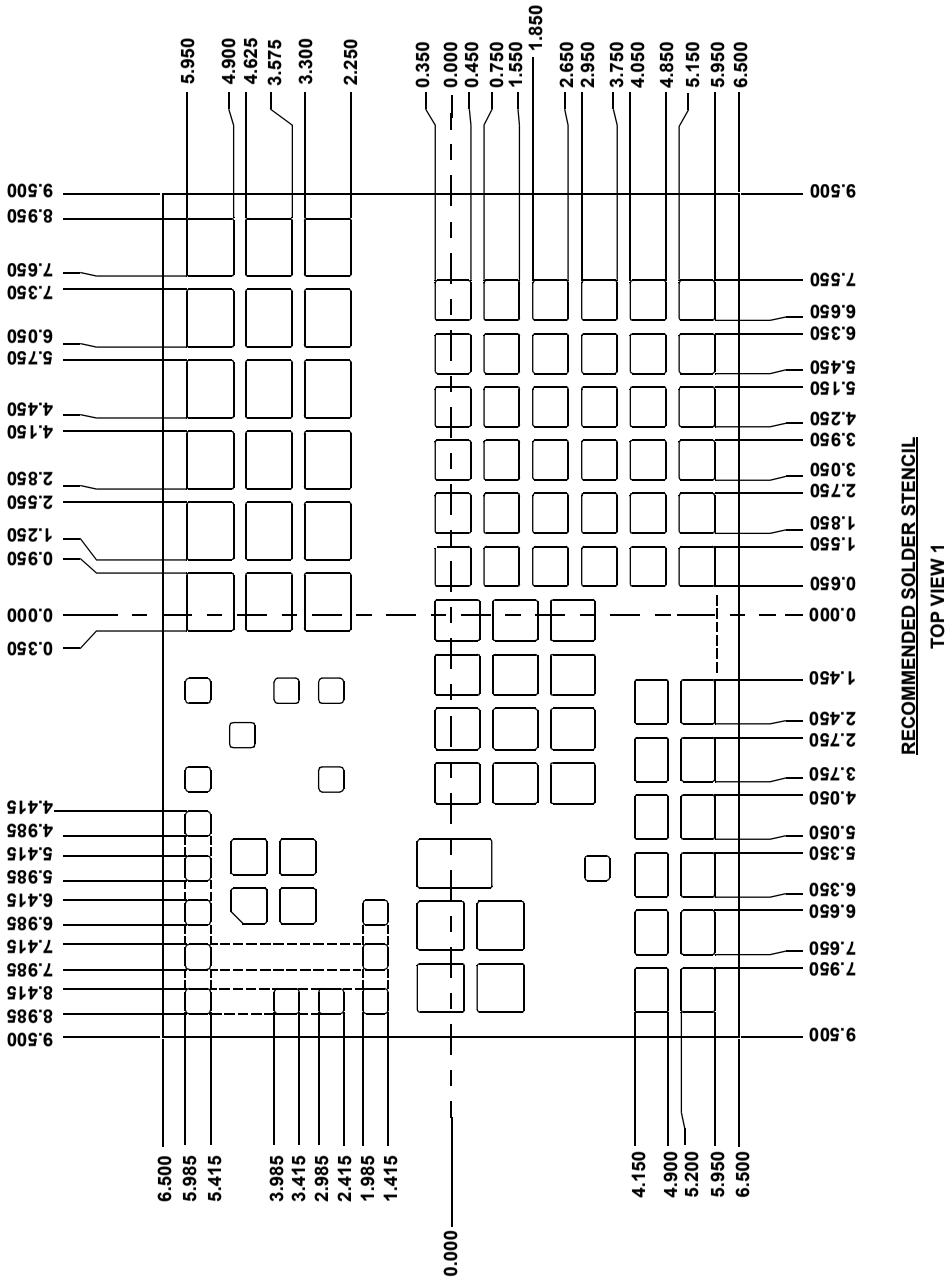
BOTTOM VIEW

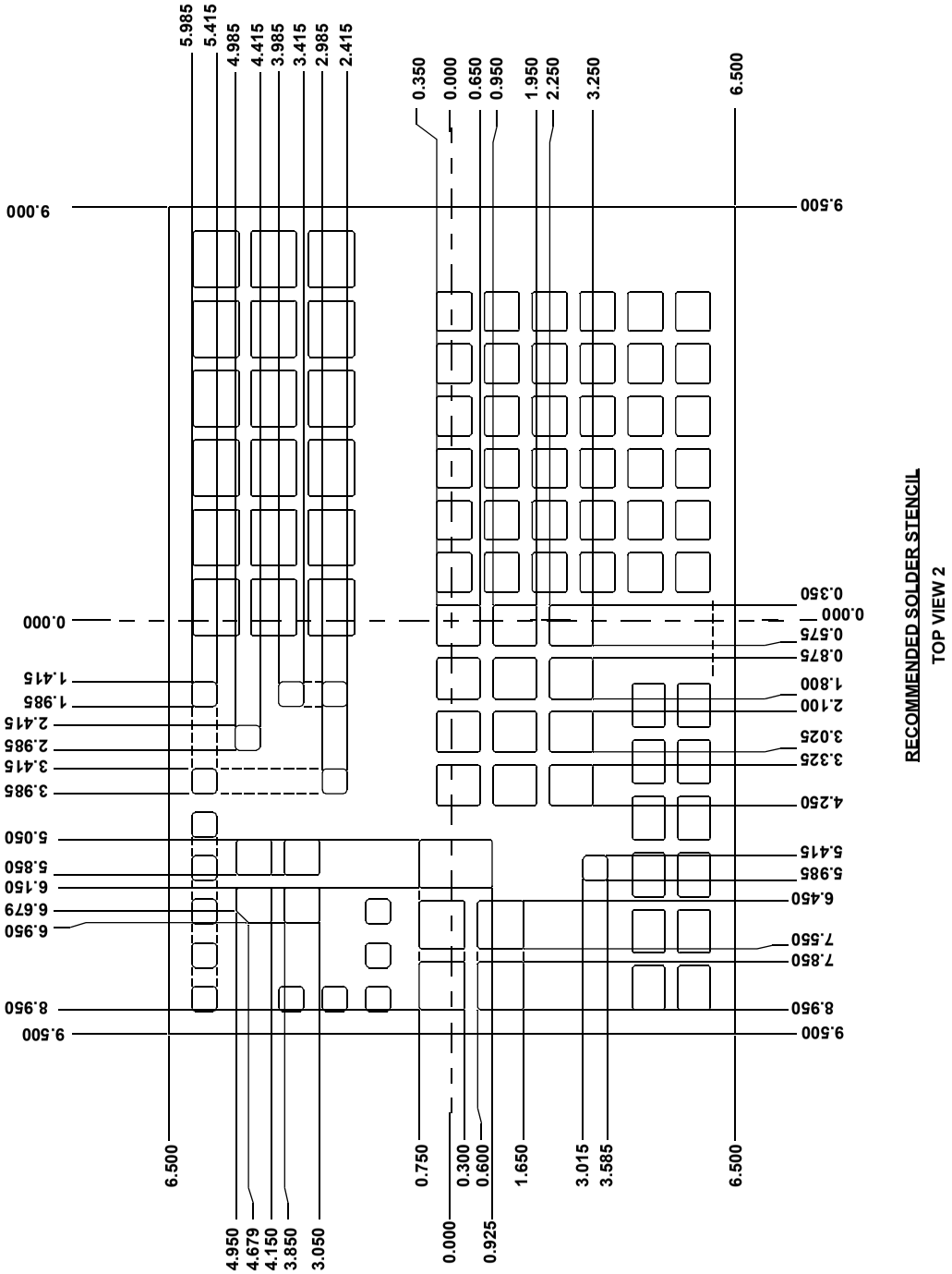


DETAIL A
(SCALE 2:1)

NOTES:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 17 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension is ±0.1mm.


RECOMMENDED SOLDER STENCIL
TOP VIEW 1


RECOMMENDED SOLDER STENCIL
TOP VIEW 2
9.000
0.000
1.415
1.985
2.415
2.985
3.415
3.985
5.050
5.850
6.150
6.679
6.950
8.950
9.500
5.985
5.415
4.985
4.415
3.985
3.415
2.985
2.415
0.350
0.000
0.650
0.950
1.950
2.250
3.250
6.500
9.500
0.350
0.000
0.575
0.875
1.800
2.100
3.025
3.325
4.250
5.415
5.985
6.450
7.550
7.850
8.950
9.500
6.500
4.950
4.679
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3.850
3.050
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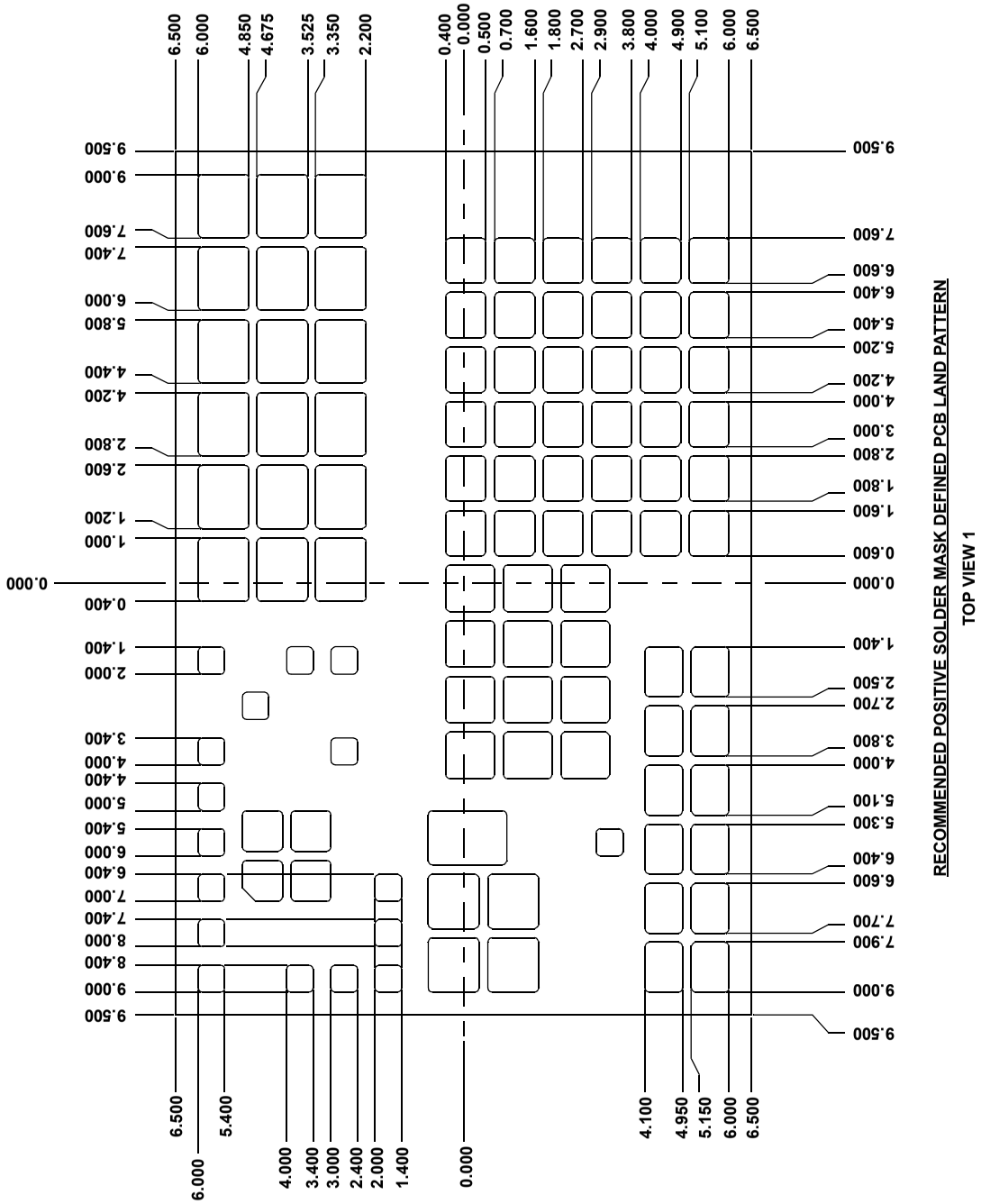
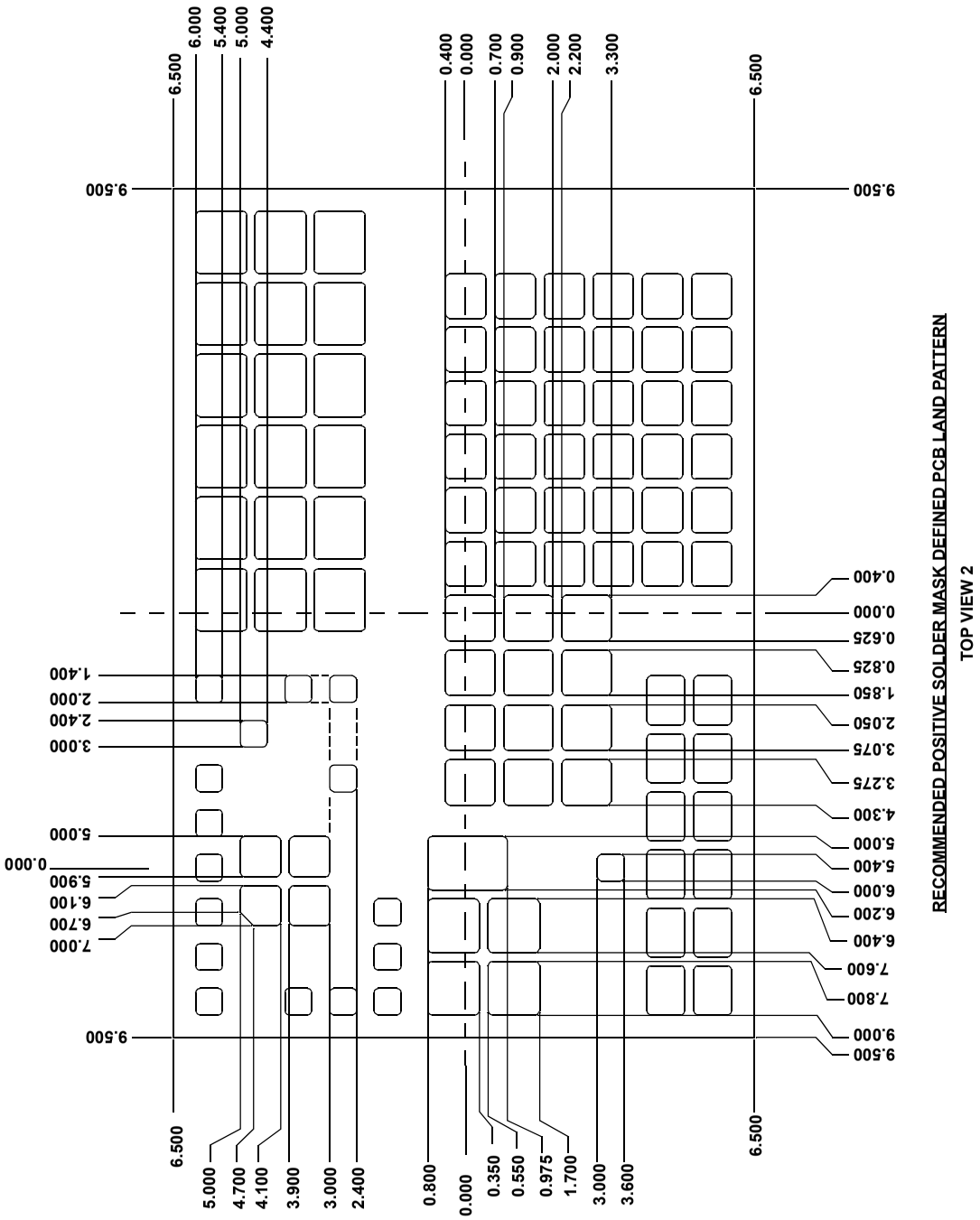
0.600
1.650
3.015
3.585
6.500


RECOMMENDED POSITIVE SOLDER MASK DEFINED PCB LAND PATTERN
TOP VIEW 1


RECOMMENDED POSITIVE SOLDER MASK DEFINED PCB LAND PATTERN
TOP VIEW 2
6.500
6.000
5.400
5.000
4.400
0.400
0.000
0.700
0.900
2.000
2.200
3.300
6.500
9.500
9.500
0.400
0.000
0.625
0.825
1.850
2.050
3.075
3.275
4.300
5.000
5.400
6.000
6.200
6.400
7.600
7.800
9.000
9.500
1.400
2.000
2.400
3.000
5.000
0.000
5.900
6.100
6.700
7.000
9.500
6.500
5.000
4.700
4.100
3.900
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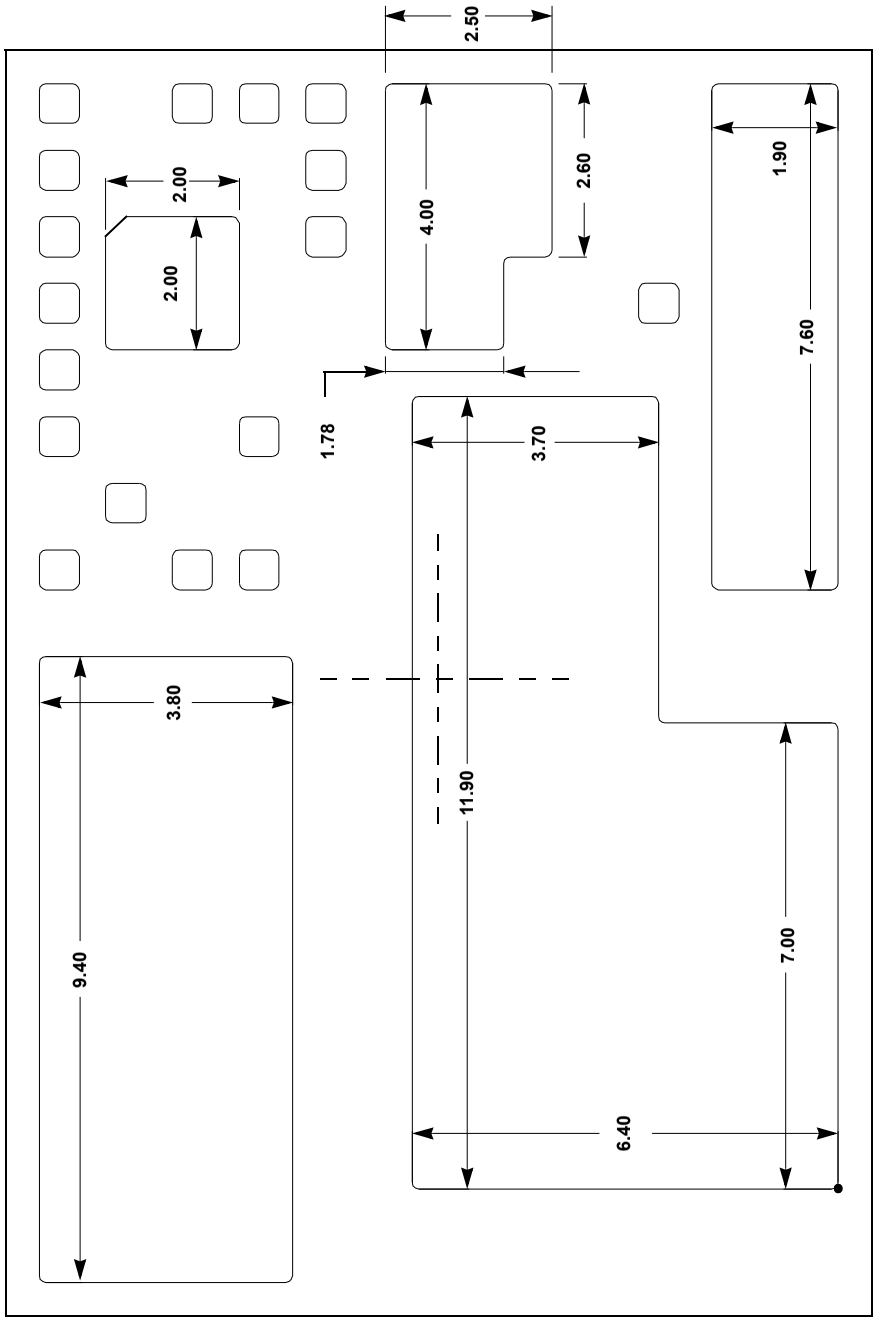
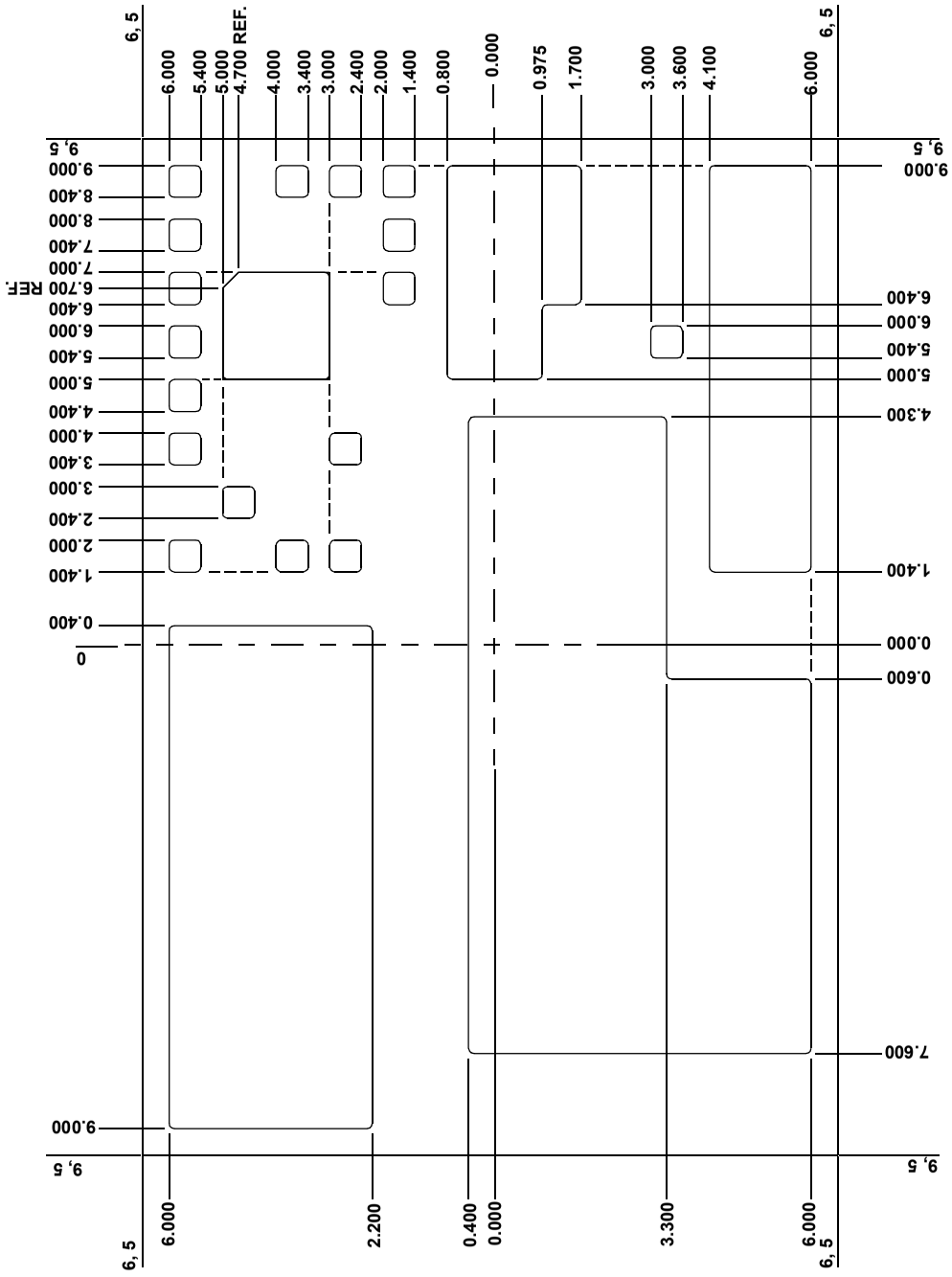
0.350
0.550
0.975
1.700
3.000
3.600
6.500


2.50
2.00
2.00
4.00
2.60
1.90
7.60
1.78
3.70
3.80
11.90
9.40
7.00
6.40
SIZE DETAILS FOR THE 5 EXPOSED PADS



TERMINAL AND PAD EDGE DETAILS
(BOTTOM VIEW)

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