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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR $\mu PA1819$

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA1819 is a switching device that can be driven directly by a 4.0 V power source.

This device features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power management of notebook computers and so on.

FEATURES

- 4.0 V drive available
- Low on-state resistance $R_{DS(on)1} = 12 \ m\Omega \ MAX. \ (V_{GS} = -10 \ V, \ I_{D} = -6.0 \ A)$ $R_{DS(on)2} = 18.5 \ m\Omega \ MAX. \ (V_{GS} = -4.5 \ V, \ I_{D} = -6.0 \ A)$ $R_{DS(on)3} = 22 \ m\Omega \ MAX. \ (V_{GS} = -4.0 \ V, \ I_{D} = -6.0 \ A)$
- Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1819GR-9JG	Power TSSOP8

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage ($V_{GS} = 0 V$)	VDSS	-30	V	EQUI
Gate to Source Voltage (Vbs = 0 V)	Vgss	∓20	V	
Drain Current (DC) (T _A = 25°C)	ID(DC)	∓12	А	
Drain Current (pulse) ^{Note1}	D(pulse)	∓48	А	
Total Power Dissipation Note2	Ρτ	2.0	W	Gate
Channel Temperature	Tch	150	°C	Gate
Storage Temperature	Tstg	–55 to +150	°C	Prote

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

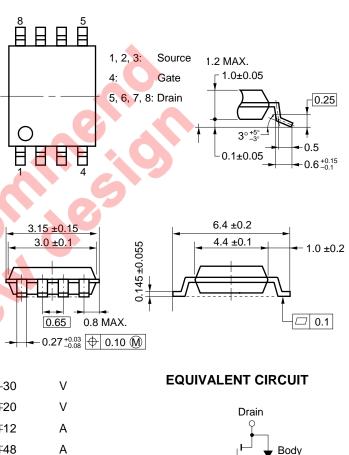
- 2. Mounted on ceramic substrate of 5000 mm² x 1.1 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Diode

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Source



Gate Protection

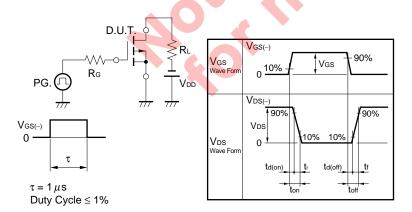
Diode

PACKAGE DRAWING (Unit: mm)

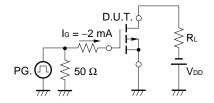
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -30 V$, $V_{GS} = 0 V$			-1.0	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			∓10	μA
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 V$, $I_D = -1.0 mA$	-1.0	-2.0	-2.5	V
Forward Transfer Admittance	y₁s	$V_{DS} = -10 V$, $I_D = -6.0 A$	11	23		S
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = -10 \text{ V}, \text{ ID} = -6.0 \text{ A}$		9.8	12	mΩ
	RDS(on)2	$V_{GS} = -4.5 V$, $I_D = -6.0 A$		13.9	18.5	mΩ
	RDS(on)3	$V_{GS} = -4.0 \text{ V}, \text{ Id} = -6.0 \text{ A}$		16.4	22	mΩ
Input Capacitance	Ciss	$V_{DS} = -10 V$		2430		pF
Output Capacitance	Coss	$V_{GS} = 0 V$		690		pF
Reverse Transfer Capacitance	Crss	f = 1.0 MHz		420		pF
Turn-on Delay Time	td(on)	Vdd = -15 V, Id = -6.0 A	*	19		ns
Rise Time	tr	Vgs = -10 V		17		ns
Turn-off Delay Time	td(off)	Rg = 10 Ω		160		ns
Fall Time	tr			160		ns
Total Gate Charge	QG	VDD = -24 V		45		nC
Gate to Source Charge	QGS	V _{GS} = -10 V		5.5		nC
Gate to Drain Charge	Qgd	Ib = -12 A		15		nC
Body Diode Forward Voltage	VF(S-D)	IF = 12 A, Vgs = 0 V		0.83		V
Reverse Recovery Time	trr	IF = 12 A, VGs = 0 V		50		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		40		nC

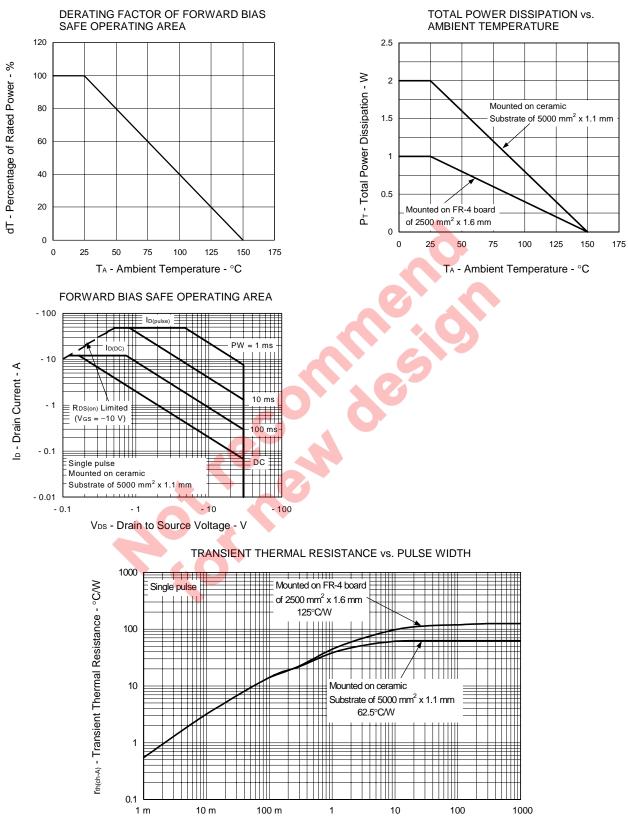
TEST CIRCUIT 1 SWITCHING TIME



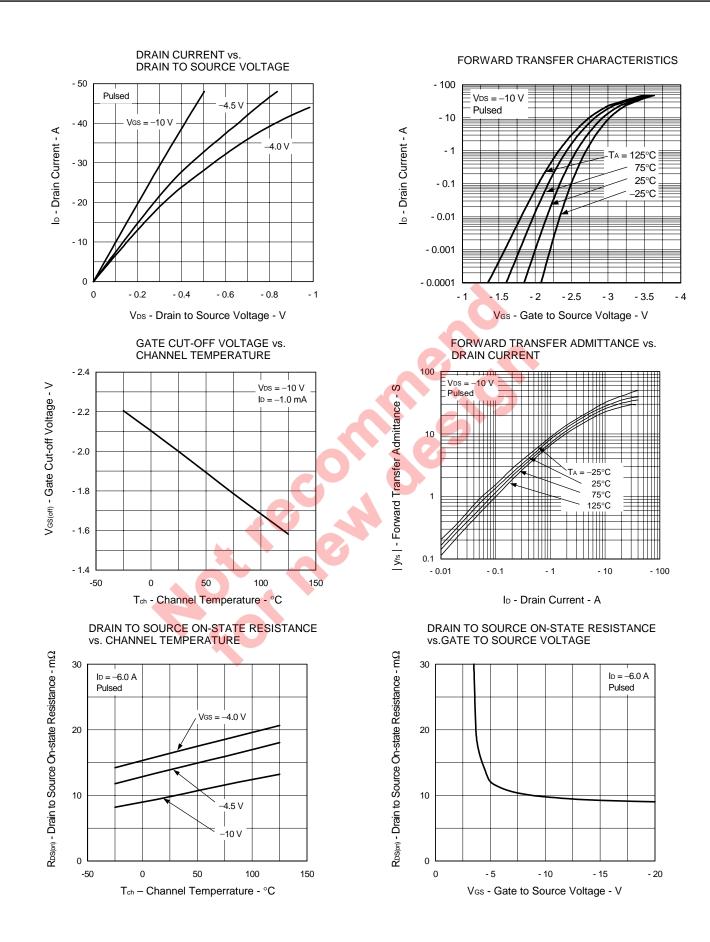
TEST CIRCUIT 2 GATE CHARGE



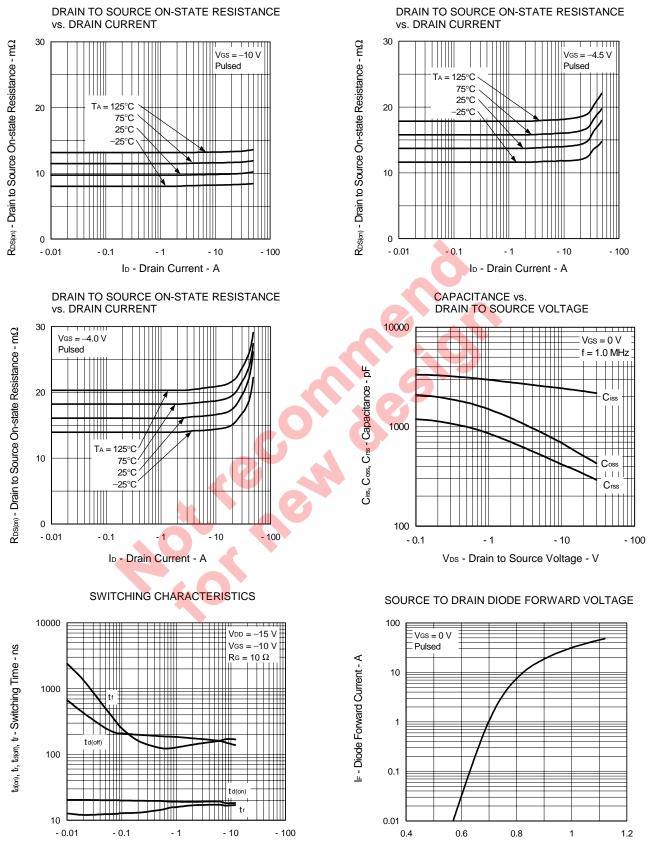
TYPICAL CHARACTERISTICS (TA = 25°C)



PW - Pulse Width - s



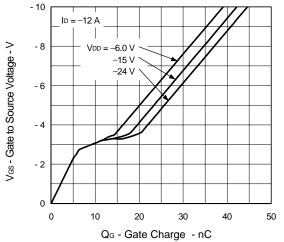
NEC



VF(S-D) - Source to Drain Voltage - V

ID - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



De - Gate Charge - nC

[MEMO]



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