NEC

MOS INTEGRATED CIRCUIT

μPD16742

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256 GRAY SCALES)

★ The μPD16742 is a source driver for TFT-LCDs capable of dealing with displays with 256 gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ-corrected by an internal D/A converter and 11 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. The D/A converter, which incorporates a digital offset circuit, is suitable for an LCD panel in which liquid crystal transmittance in positive and negative polarities is different. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, this driver is applicable to SXGA and XGA-standard TFT-LCD panels.

FEATURES

- CMOS level input
- 384-output channel
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 11 external power modules and a D/A converter (C-DAC)
- ★ • Output dynamic range V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- ★ • Logic Part Power Supply Voltage (V_{DD1}) : 3.3 ± 0.3 V
- ★ • Driver Part Power Supply Voltage (V_{DD2}) : 9.0 ± 0.5 V
- High-speed data transfer: $f_{MAX.}$ = 65 MHz (internal data transfer speed when operating at V_{DD1} = 3.0 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- ★ • Output voltage polarity reverse is possible (POLA)
- ★ • Input data reverse function is incorporated (POLB (O/E))
- Output offset for different eight values can be controlled by offset signals (three signals)

ORDERING INFORMATION

Part Number	Package
μPD16742N-×××	TCP (TAB package)

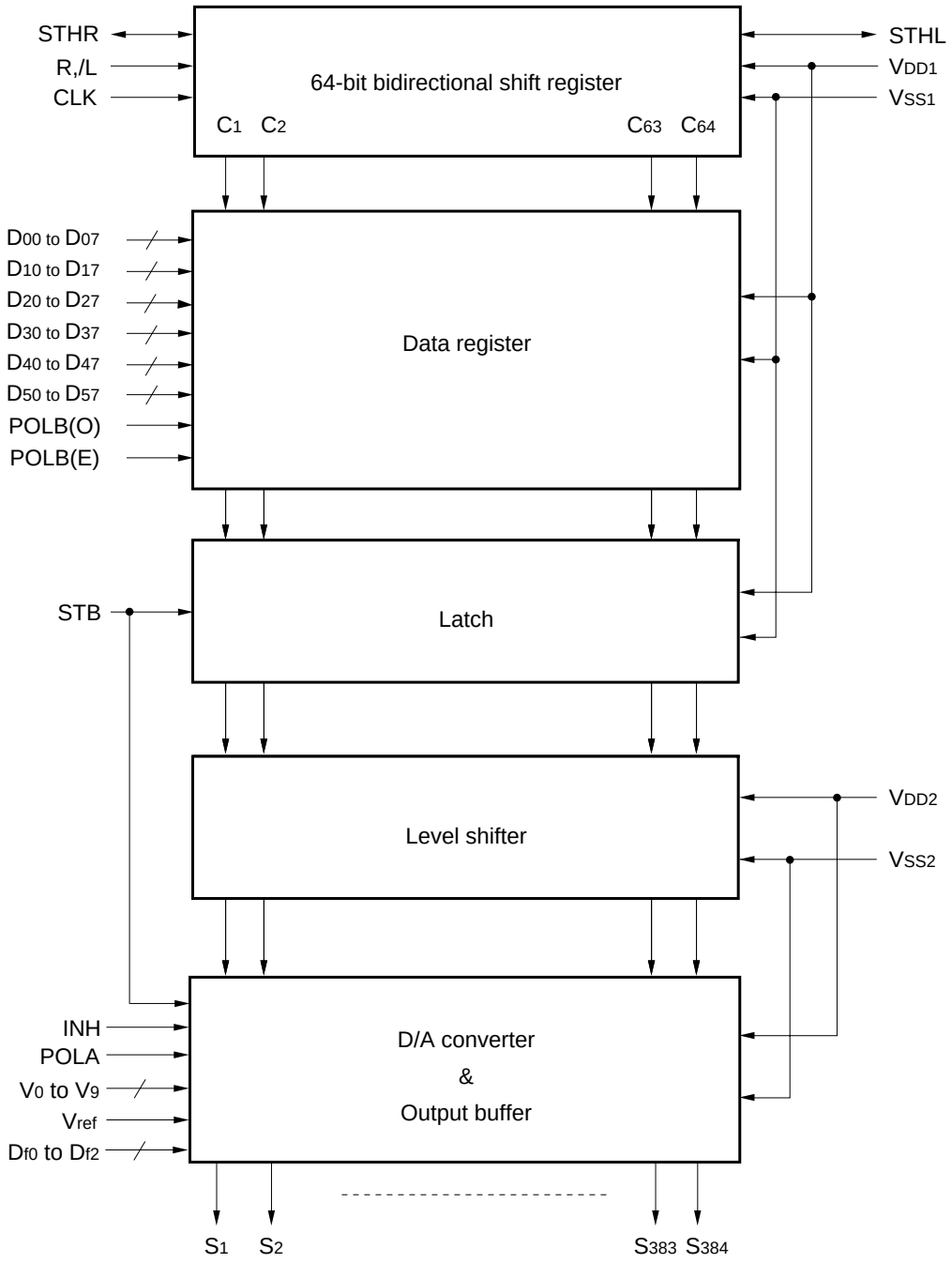
The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. S13325EJ6V0PM00 (6th edition)
Date Published January 1999 NS CP(K)
Printed in Japan

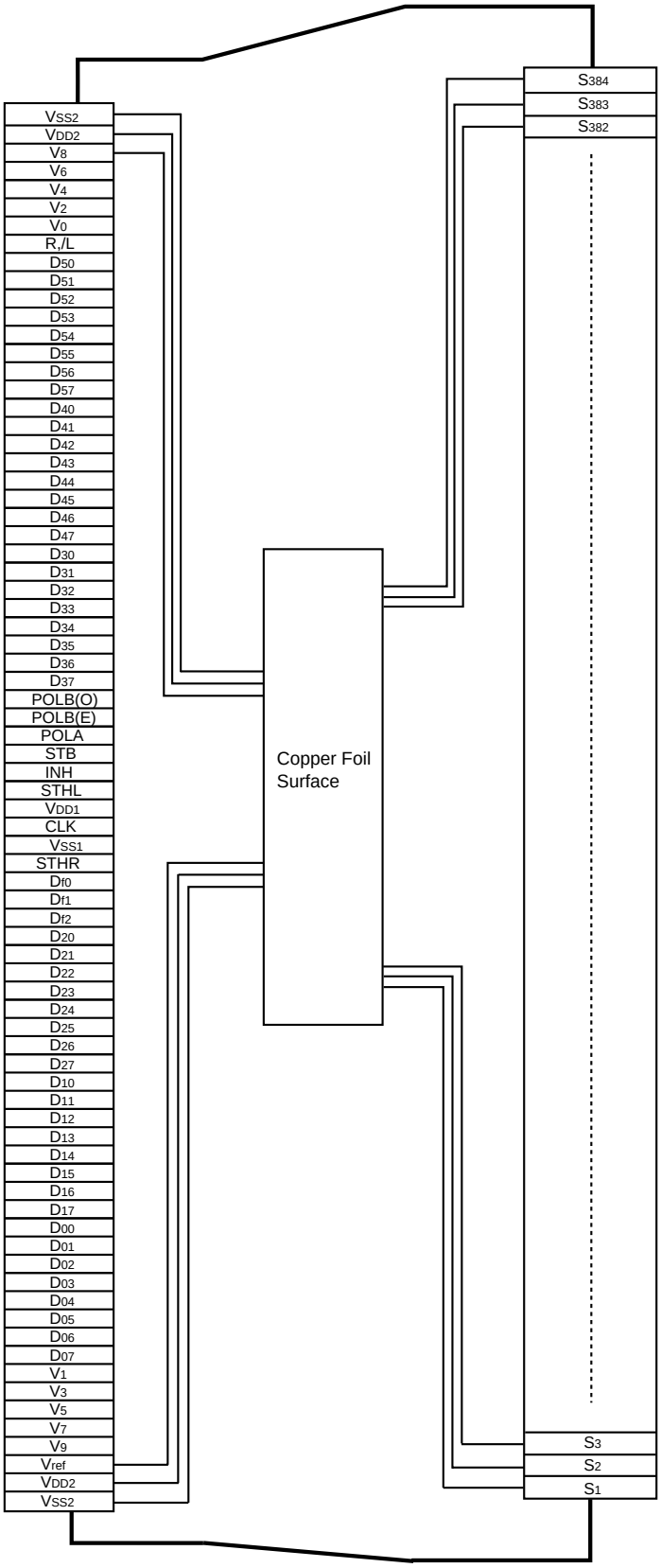
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16742N-×××)



Caution This figure does not specify the TCP package.

3. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 256-gray-scale analog voltage is output.
D_{00} to D_{07}	Display data input	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). 8-bit input : D_{X0}: LSB, D_{X7}: MSB
D_{10} to D_{17}		
D_{20} to D_{27}		
D_{30} to D_{37}		
D_{40} to D_{47}		
D_{50} to D_{57}		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H (Right shift) : STHR (input) → S_1 → S_{384} → STHL (output) R,/L = L (Left shift) : STHL (input) → S_{384} → S_1 → STHR (output)
STHR	Right shift start pulse input/output	Start pulse I/O pin at cascade connection. The display data is acquired when the high level is read at the rising edge of CLK. Right shift : STHR is input. STHL is output. Left shift : STHL is input. STHR is output.
STHL	Left shift start pulse input/output	
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. Start pulse high level is read at rising edge of CLK, start to load the display data from next rising edge of CLK. Also, after start pulse input and CLK input 66 pulses, it stops to load the display data and it makes contents of shift register clear at rising edge of STB.
STB	Latch input	After the contents of data register is transferred to a latch at a rising edge and is cleared, operation of analog output voltage for output voltage is started.
INH	Inhibit input	At the falling edge complete calculation of analog output voltage, and output the voltage appointed by display data.
POLA	Polarity input	This signal is read at the rising edge of latch signal and determines the output voltage polarity to reference voltage of each output pin. POLA = L : Pins with even number are negative output. Pins with odd number are positive output. POLA = H : Pins with even number are positive output. Pins with odd number are negative output.
POLB(O) POLB(E)	Data inversion	By inputting a switching signal to this pin, this pin enables the data whose polarity is reversed to be read. POLB(O) and POLB(E) are a data reverse control pin for D_{0X} – D_{2X} and D_{3X} – D_{5X}, respectively. POLB(O/E) = H : Acquires with displayed data reversed POLB(O/E) = L : Acquires raw displayed data
V_{ref}	Reference power supply	This terminal is the input reference power supply need to calculation output. Please refer to **5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE.**

(2/2)

Pin Symbol	Pin Name	Description
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. $V_{ref} - 0.1\ V \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1\ V$ $V_{ref} - 0.1\ V \geq V_9 \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0 \geq V_{SS2} + 0.1\ V$ During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level.
D_{f0} to D_{f2}	Offset control	This pin determines offset voltage. For the offset voltage for each input data, refer to **9. OFFSET VOLTAGE**.
V_{DD1}	Logic power supply	3.3 V ± 0.3 V
V_{DD2}	Driver power supply	9.0 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

4. CAUTION

(1) The power start sequence must be V_{DD1} → logic input (Hi or Low) → V_{DD2} → V_{ref} → V_0 to V_9 in that order. Reverse this sequence to shut down. Be sure to observe this power sequence even during a transition period.

(2) To stabilize the supply voltage, please be sure to insert each 0.1μF,0.47μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01μF is also advised between the γ- corrected power supply terminals (V_0 to V_9) and V_{SS2}.

(3) We recommend to use Operational Amplifier to lower input impedance of "γ-corrected voltage" and " γ-corrected reference power supply " input terminal .
Please input this terminal stabilized voltage . In case of input high impedance switching signals , applied voltage to this terminal is getting to instability , and may not be correctly displayed.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

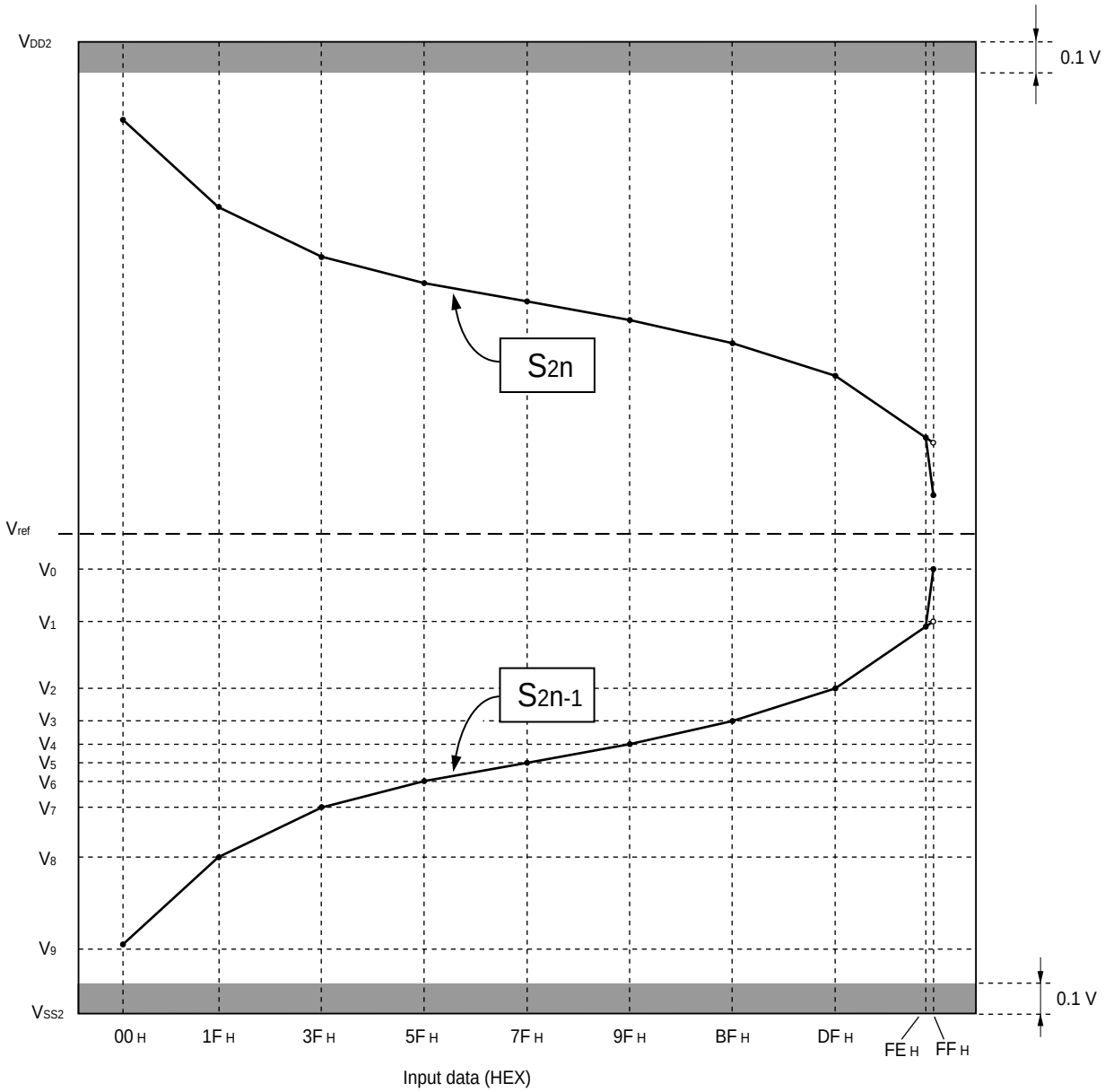
5.1 Calculation of output voltage in 8-bit input

(V_{ref} – 0.1 V ≥ V_0 ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 ≥ V_6 ≥ V_7 ≥ V_8 ≥ V_9 ≥ V_{SS2} + 0.1 V)

Gray Scale	Binary	Input Data								Output Voltage	Output Voltage
		D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	S_{2n} (POLA=H), S_{2n-1} (POLA=L)	S_{2n-1}(POLA=H),S_{2n}(POLA=L)
0	00_H	0	0	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_8+(V_9-V_8) \times 31/32\}$	$V_8+(V_9-V_8) \times 31/32$
1	01_H	0	0	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_8+(V_9-V_8) \times 30/32\}$	$V_8+(V_9-V_8) \times 30/32$
⋮	⋮									⋮	⋮
30	$1E_H$	0	0	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_8+(V_9-V_8) \times 1/32\}$	$V_8+(V_9-V_8) \times 1/32$
31	$1F_H$	0	0	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_8$	V_8
32	20_H	0	0	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_7+(V_8-V_7) \times 31/32\}$	$V_7+(V_8-V_7) \times 31/32$
33	21_H	0	0	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_7+(V_8-V_7) \times 30/32\}$	$V_7+(V_8-V_7) \times 30/32$
⋮	⋮									⋮	⋮
62	$3E_H$	0	0	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_7+(V_8-V_7) \times 1/32\}$	$V_7+(V_8-V_7) \times 1/32$
63	$3F_H$	0	0	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_7$	V_7
64	40_H	0	1	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_6+(V_7-V_6) \times 31/32\}$	$V_6+(V_7-V_6) \times 31/32$
65	41_H	0	1	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_6+(V_7-V_6) \times 30/32\}$	$V_6+(V_7-V_6) \times 30/32$
⋮	⋮									⋮	⋮
94	$5E_H$	0	1	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_6+(V_7-V_6) \times 1/32\}$	$V_6+(V_7-V_6) \times 1/32$
95	$5F_H$	0	1	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_6$	V_6
96	60_H	0	1	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_5+(V_6-V_5) \times 31/32\}$	$V_5+(V_6-V_5) \times 31/32$
97	61_H	0	1	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_5+(V_6-V_5) \times 30/32\}$	$V_5+(V_6-V_5) \times 30/32$
⋮	⋮									⋮	⋮
126	$7E_H$	0	1	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_5+(V_6-V_5) \times 1/32\}$	$V_5+(V_6-V_5) \times 1/32$
127	$7F_H$	0	1	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_5$	V_5
128	80_H	1	0	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_4+(V_5-V_4) \times 31/32\}$	$V_4+(V_5-V_4) \times 31/32$
129	81_H	1	0	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_4+(V_5-V_4) \times 30/32\}$	$V_4+(V_5-V_4) \times 30/32$
⋮	⋮									⋮	⋮
158	$9E_H$	1	0	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_4+(V_5-V_4) \times 1/32\}$	$V_4+(V_5-V_4) \times 1/32$
159	$9F_H$	1	0	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_4$	V_4
160	$A0_H$	1	0	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_3+(V_4-V_3) \times 31/32\}$	$V_3+(V_4-V_3) \times 31/32$
161	$A1_H$	1	0	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_3+(V_4-V_3) \times 30/32\}$	$V_3+(V_4-V_3) \times 30/32$
⋮	⋮									⋮	⋮
190	BE_H	1	0	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_3+(V_4-V_3) \times 1/32\}$	$V_3+(V_4-V_3) \times 1/32$
191	BF_H	1	0	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_3$	V_3
192	$C0_H$	1	1	0	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_2+(V_3-V_2) \times 31/32\}$	$V_2+(V_3-V_2) \times 31/32$
193	$C1_H$	1	1	0	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_2+(V_3-V_2) \times 30/32\}$	$V_2+(V_3-V_2) \times 30/32$
⋮	⋮									⋮	⋮
222	DE_H	1	1	0	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_2+(V_3-V_2) \times 1/32\}$	$V_2+(V_3-V_2) \times 1/32$
223	DF_H	1	1	0	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_2$	V_2
224	$E0_H$	1	1	1	0	0	0	0	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_1+(V_2-V_1) \times 31/32\}$	$V_1+(V_2-V_1) \times 31/32$
225	$E1_H$	1	1	1	0	0	0	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_1+(V_2-V_1) \times 30/32\}$	$V_1+(V_2-V_1) \times 30/32$
⋮	⋮									⋮	⋮
254	FE_H	1	1	1	1	1	1	1	0	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times \{V_1+(V_2-V_1) \times 1/32\}$	$V_1+(V_2-V_1) \times 1/32$
255	FF_H	1	1	1	1	1	1	1	1	$(4+\alpha)/\alpha \times V_{ref}-4/\alpha \times V_0$	V_0

5.2 Curved line of output voltage

(POLA = H, α = 4, V_{ref} – 0.1 V ≥ V_0 ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5 ≥ V_6 ≥ V_7 ≥ V_8 ≥ V_9 ≥ V_{SS2} + 0.1 V)



6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

The reference power supply of the D/A converter is made up of a capacitance ladder circuit, which minimizes current flow into the γ- corrected power supply pins. However, in the LCD driver of previous R-DAC systems the resistance ratio between the γ- corrected power supply pins was set to be identical to the γ- corrected voltage ratio used for an actual LCD panel. Such a function is not available in this product. Therefore, γ- corrected voltage directly becomes D/A converter reference power voltage in the IC. Determine γ- corrected voltage based on the data of γ characteristics of a LCD panel described in **5. RELATIONS BETWEEN INPUT DATA AND OUTPUT VOLTAGE**.

7. INPUT FORMAT OF DISPLAY DATA

Data format : 8 bits × 2 RGBs (6 dots)
Input width : 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

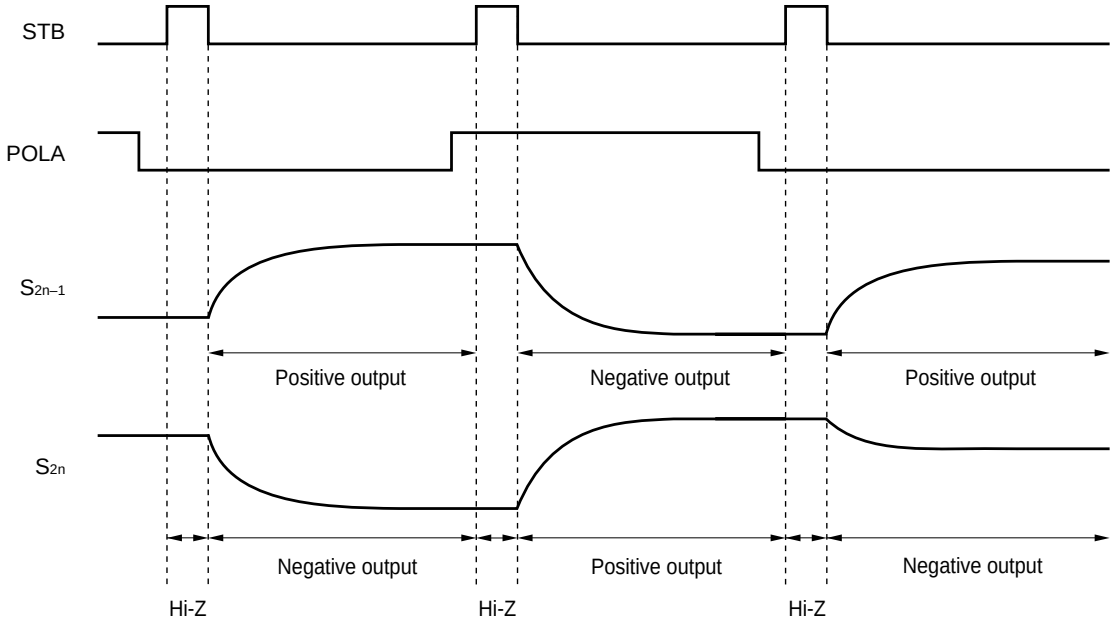
Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	···	D_{40} to D_{47}	D_{50} to D_{57}

(2) R,/L = L (Left shift)

Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	···	D_{40} to D_{47}	D_{50} to D_{57}

8. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output buffer consists of an operational amplifier circuit that does not perform recharge operation. Therefore, driver output current I_{VOH} is the charging current to the LCD, and I_{VOL} is the discharging current.



9. OFFSET VOLTAGE

Determine the coefficient α of V_{OUT} based on the offset control pins (D_{f0} – D_{f2}). Relationship between input data and α are listed as follows.

D_{f0}	D_{f1}	D_{f2}	α
0	0	0	4.0
1	0	0	4.4
0	1	0	4.6
1	1	0	4.8
0	0	1	5.0
1	0	1	5.2
0	1	1	5.4
1	1	1	5.6

Remark $V_{OUT} = (4+\alpha) / \alpha \times V_{ref} - 4/\alpha \times \{V_m+(V_m+1-V_m) \times n/32\}$

10. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = +25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Part Power Supply Voltage	V_{DD1}	–0.5 to + 6.0	V
Driver Part power Supply Voltage	V_{DD2}	–0.5 to + 10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	8.5	9.0	9.5	V
Driver Part Output Voltage Range	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
γ-Corrected Voltage	V_0 to V_9	V_{SS2} + 0.1		V_{ref} – 0.1	V
γ-Corrected Reference Power Supply	V_{ref}		0.5 V_{DD2}	5.5	V
Maximum Clock Frequency	$f_{max.}$	65			MHz

Electrical Specifications (T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 9.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH}	CLK,STB,R,/L,INH,POLA,POLB, D_{00} to D_{07}, D_{10} to D_{17}, D_{20} to D_{27}, D_{30} to D_{37}, D_{40} to D_{47}, D_{50} to D_{57}, D_{f0} to D_{f2}	0.7 V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
Input Leak Current	I_{IL}		–1.0		+1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = –1.0 mA	V_{DD1} – 0.5			V
Low-level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = +1.0 mA			V_{SS1} +0.5	V
Driver Output Current (V_{DD2} = 9.0 V)	I_{VOH}	V_{DD1} = 3.3 V , INH = 0 V V_{OUT} = 8.4 V , V_O = 8.9 V		–0.18	–0.1	mA
	I_{VOL}	V_{DD1} = 3.3 V , INH = 0 V V_{OUT} = 0.6 V , V_O = 0.1 V	0.06	0.13		mA
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V , V_{DD2} = 9.0 V V_{OUT} = 0.5 / 3.0 / 5.0 / 8.0 V		±10	±20	mV
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1} = 3.3 V,with no load		7	20	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2} = 9.0 V, with no load		8	16	mA

Remarks1. V_{OUT} indicates application voltage to output pins. V_0 indicates output voltage to output pins.

2. For logic part dynamic current consumption, the TYP. value is based on the condition while the screen is displayed in entirely dark or entirely light and the MAX. value is based on the condition while the screen is displayed in chess board pattern.

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 9.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

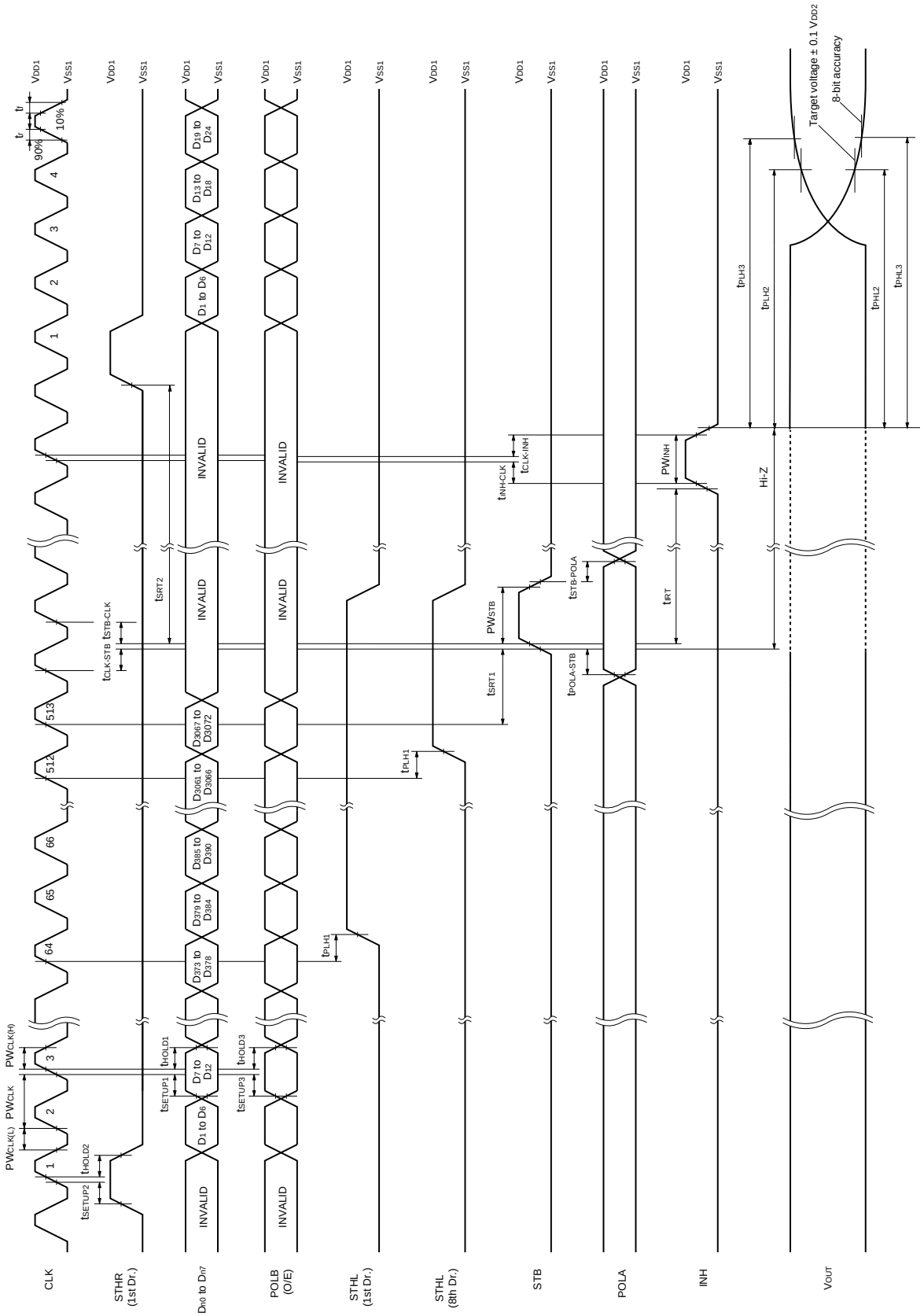
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF, CLK → STHL (STHR)		2		15	ns
Driver Output Delay Time	t_{PLH2}	V_{DD2} = 9.0V,	V_O = 0.1 V → 8.9 V		4.0	(T.B.D.)	μs
	t_{PLH3}	R_L = 5.0 kΩ,			8.5	(T.B.D.)	μs
	t_{PHL2}	C_L = 70 pF,	V_O = 8.9 V → 0.1 V		4.0	(T.B.D.)	μs
	t_{PHL3}				8.5	(T.B.D.)	μs
Input Capacitance	C_{I1}	T_A = +25°C , STHR (STHL)			10	15	pF
	C_{I2}	T_A = +25°C, V_0 to V_9,V_{ref}			900		pF
	C_{I3}	T_A = +25°C, STHR(STHL), V_0 to V_9, Except V_{ref}			5	10	pF

Timing Requirement

(T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 9.0 V ±0.5 V ,V_{SS1} = V_{SS2} = 0 V)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Clock Pulse Width	PW_{CLK}		15			ns
	Clock Pulse High Period	$PW_{CLK(H)}$		3			ns
	Clock Pulse Low Period	$PW_{CLK(L)}$		3			ns
	STB Pulse Width	PW_{STB}		1			CLK
	INH Pulse Width	PW_{INH}		1			CLK
	Data Setup Time	t_{SETUP1}		2			ns
	Data Hold Time	t_{HOLD1}		2			ns
	Start Pulse Setup Time	t_{SETUP2}		2			ns
	Start Pulse Hold Time	t_{HOLD2}		2			ns
	POLB Setup Time	t_{SETUP3}		2			ns
	POLB Hold Time	t_{HOLD3}		2			ns
	STB Pulse Rise Timing	t_{SRT1}		1			CLK
	Start Pulse Rise Timing	t_{SRT2}		1			CLK
	INH Rise Timing	t_{IRT}		1			μs
★	CLK-INH Time	$t_{CLK-INH}$	CLK↑→INH↓	4			ns
★	INH-CLK Time	$t_{INH-CLK}$	INH↑→CLK↑	4			ns
★	POLA-STB Time	$t_{POLA-STB}$	POLA↑or↓→STB↑	4			ns
★	STB-POLA Time	$t_{STB-POLA}$	STB↓→POLA↑or↓	4			ns
★	CLK-STB Time	$t_{CLK-STB}$	CLK↑→STB↑	4			ns
★	STB-CLK Time	$t_{STB-CLK}$	STB↑→CLK↑	4			ns

★ 11. SWITCHING CHARACTERISTICS WAVEFORM (In case of XGA drive)



Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

12. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16742.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

μPD16742N-×××: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2 : time 3 to 5 secs. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2 : time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

- **The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.**
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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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