

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 8-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The μPD78070A is a limited-function product from which the internal ROM of the μPD78078 subseries has been removed. Through interchangeable external ROM, program maintenance can be performed easily. Besides a high-speed, high-performance CPU, this microcontroller has an internal RAM, I/O ports, 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

Detailed information about product features and specifications can be found in the following documents. Be sure to read the following documents before starting design.

μPD78070A, 78070AY User's Manual: U10200E

78K/0 Series User's Manual – Instructions: IEU-1372

### FEATURES

- Internal high-capacity RAM
  - Internal high-speed RAM : 1024 bytes
  - Buffer RAM: 32 bytes
- Two packages
  - 100-pin plastic QFP (fine pitch) (14 x 14 mm)
  - 100-pin plastic QFP (14 x 20 mm)
- External memory expansion space : 64 Kbytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 61 (N-ch open-drain : 8)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
  - 3-wire/SBI/2-wire mode : 1 channel
  - 3-wire mode : 1 channel
  - 3-wire/UART mode : 1 channel
- Timer : 7 channels
- Power supply voltage : V<sub>DD</sub> = 2.7 to 5.5 V

### APPLICATIONS

CD-ROM driver, printer, PPC, etc.

### ORDERING INFORMATION

Part Number	Package
μPD78070AGC-7EA	100-pin plastic QFP (Fine pitch) (14 × 14 mm, Resin thickness 1.45 mm)
μPD78070AGF-3BA	100-pin plastic QFP (14 × 20 mm, Resin thickness 2.7 mm)

The information in this document is subject to change without notice.

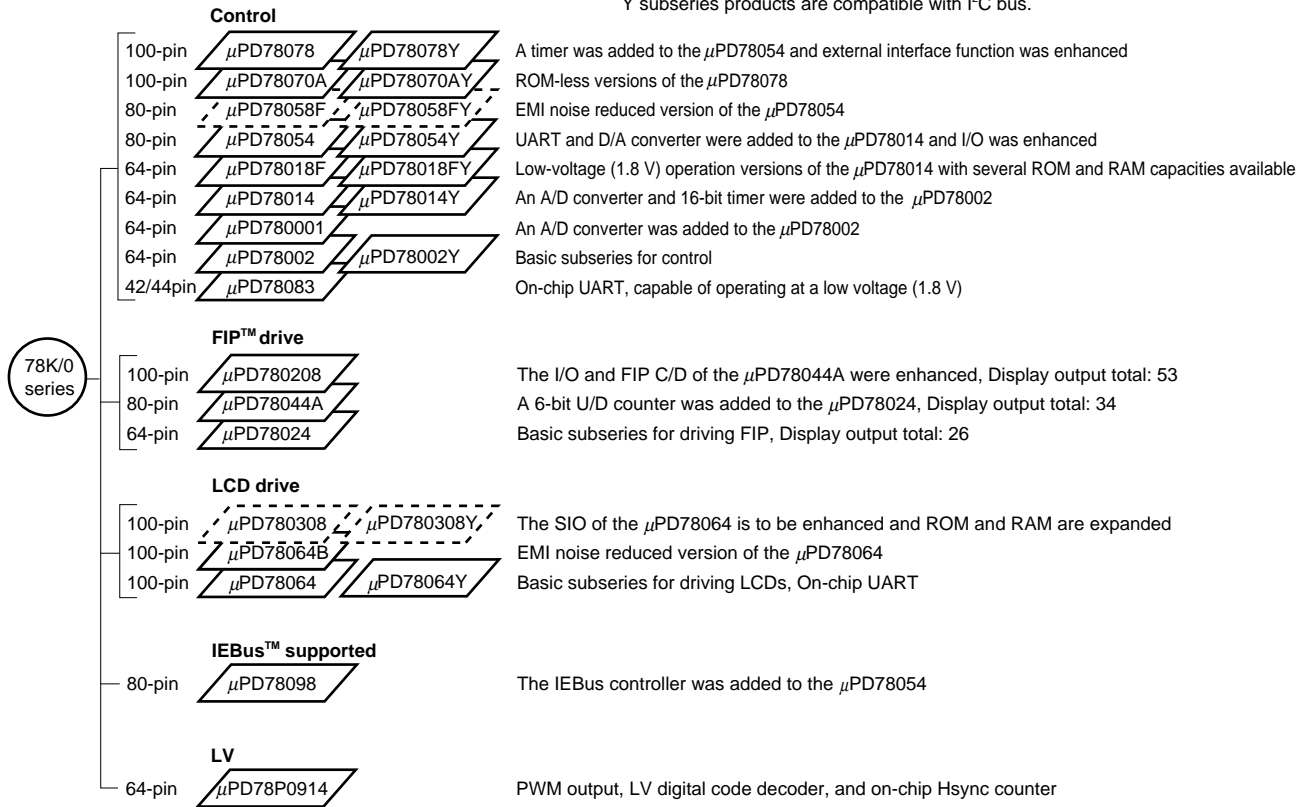
The mark ★ shows major revised points.

### 78K/0 Series Development

The following shows the 78K/0 series products development. Subseries names are shown inside frames.



Y subseries products are compatible with I<sup>2</sup>C bus.



The following table lists the main functional differences between subseries products.

Function Subseries name		ROM capacity	Timer				8-bit	8-bit	Serial Interface	I/O	V <sub>DD</sub> MIN. Value	External Expansion	
			8-bit	16-bit	Watch	WDT	A/D	D/A					
Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	Available	
	μPD78070A	–								61			2.7 V
	μPD78058F	48 K-60 K	2ch	–	–	–	–	–	2ch	69	2.0 V	–	
	μPD78054	16 K-60 K								53			1.8 V
	μPD78018F	8 K-60 K							53	2.7 V			
	μPD78014	8 K-32 K	–	–	–	–	–	–	1ch	39	–	–	
	μPD780001	8 K								53			Available
	μPD78002	8 K-16 K								8ch			1ch (UART: 1ch)
μPD78083	–	–	–	–	–	–	–	–	–	–	–		
FIP driving	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	74	2.7 V	–	
	μPD78044A	16 K-40 K								68			
	μPD78024	24 K-32 K								54			
LCD driving	μPD780308	48 K-60 K	2ch	1ch	1ch	1ch	8ch	–	3ch (UART: 1ch)	57	1.8 V	–	
	μPD78064B	32 K							2ch (UART: 1ch)	2.0 V			
	μPD78064	16 K-32 K							–	–			
IEBus supported	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	Available	
LV	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	2ch	54	4.5 V	Available	

**FUNCTION DESCRIPTION**

Item		Function
Internal memory	ROM	Not provided
	Internal high-speed RAM	1024 bytes
	Buffer RAM	32 bytes
Memory space		64 Kbytes
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time setting function
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz)
	When subsystem clock is selected	122 μs (@ 32.768 kHz)
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, Boolean operation)</li> <li>• BCD adjust, etc.</li> </ul>
I/O ports		Total : 61 <ul style="list-style-type: none"> <li>• CMOS input : 2</li> <li>• CMOS I/O : 51</li> <li>• N-ch open-drain I/O : 8</li> </ul>
A/D converter		• 8-bit resolution × 8 channels
D/A converter		• 8-bit resolution × 2 channels
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire/SBI/2-wire bus mode selectable: 1 channel</li> <li>• 3-wire mode (on-chip max. 32-byte automatic data transmit/receive function): 1 channel</li> <li>• 3-wire/UART mode selectable: 1 channel</li> </ul>
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter: 1 channel</li> <li>• 8-bit timer/event counter: 4 channels</li> <li>• Watch timer: 1 channel</li> <li>• Watchdog timer: 1 channel</li> </ul>
Timer output		5 (14-bit PWM output × 1, 8-bit PWM output × 2)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@ 5.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@ 5.0-MHz operation with main system clock)
Vectored interrupts	Maskable interrupts	Internal : 15, external : 7
	Non-maskable interrupts	Internal : 1
	Software interrupts	Internal : 1
Test input		Internal : 1
Power supply voltage		V <sub>DD</sub> = 2.7 to 5.5 V
Package		<ul style="list-style-type: none"> <li>• 100-pin plastic QFP (Fine pitch) (14 × 14 mm, Resin thickness 1.45 mm)</li> <li>• 100-pin plastic QFP (14 × 20 mm, Resin thickness 2.7 mm)</li> </ul>

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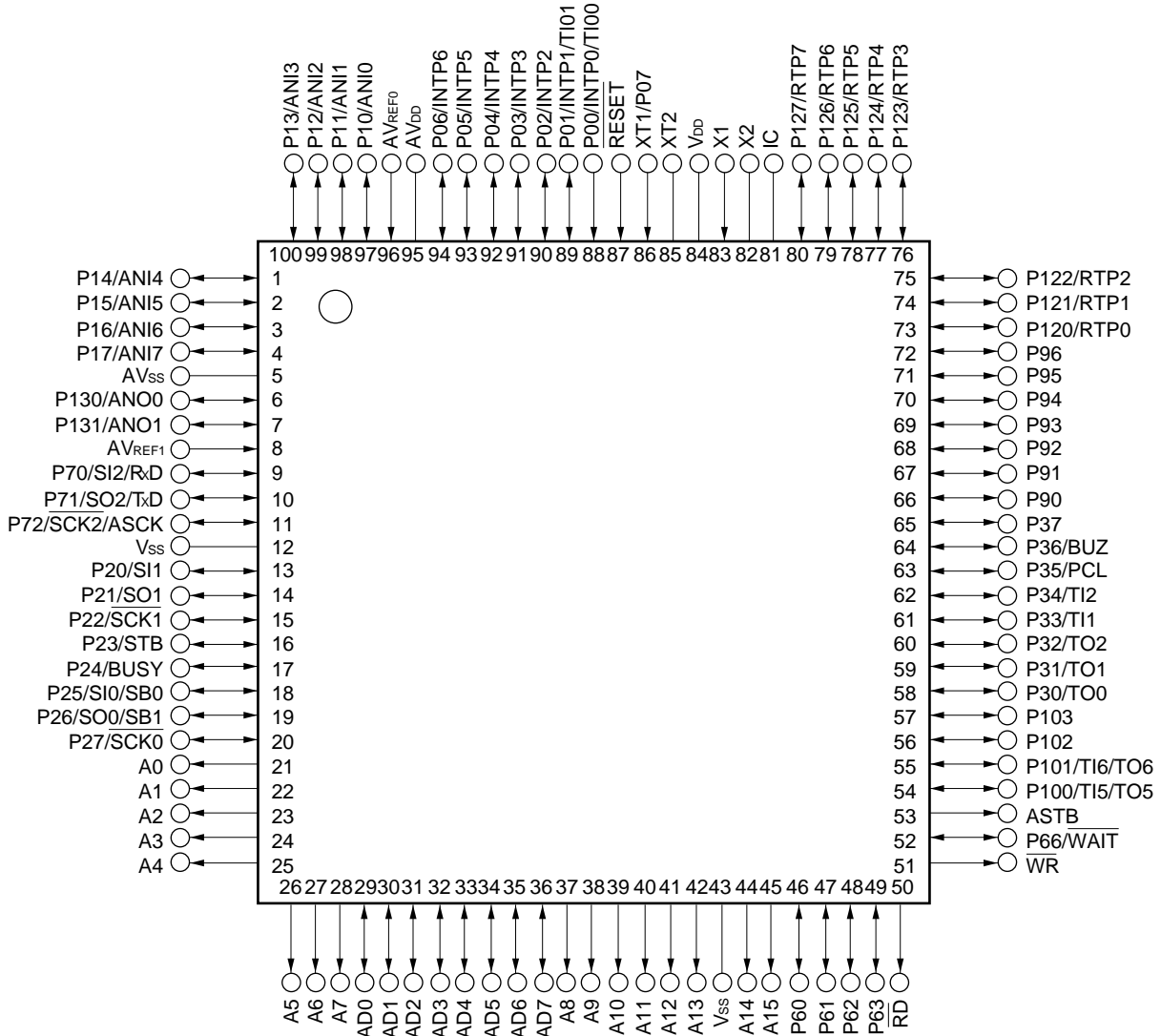
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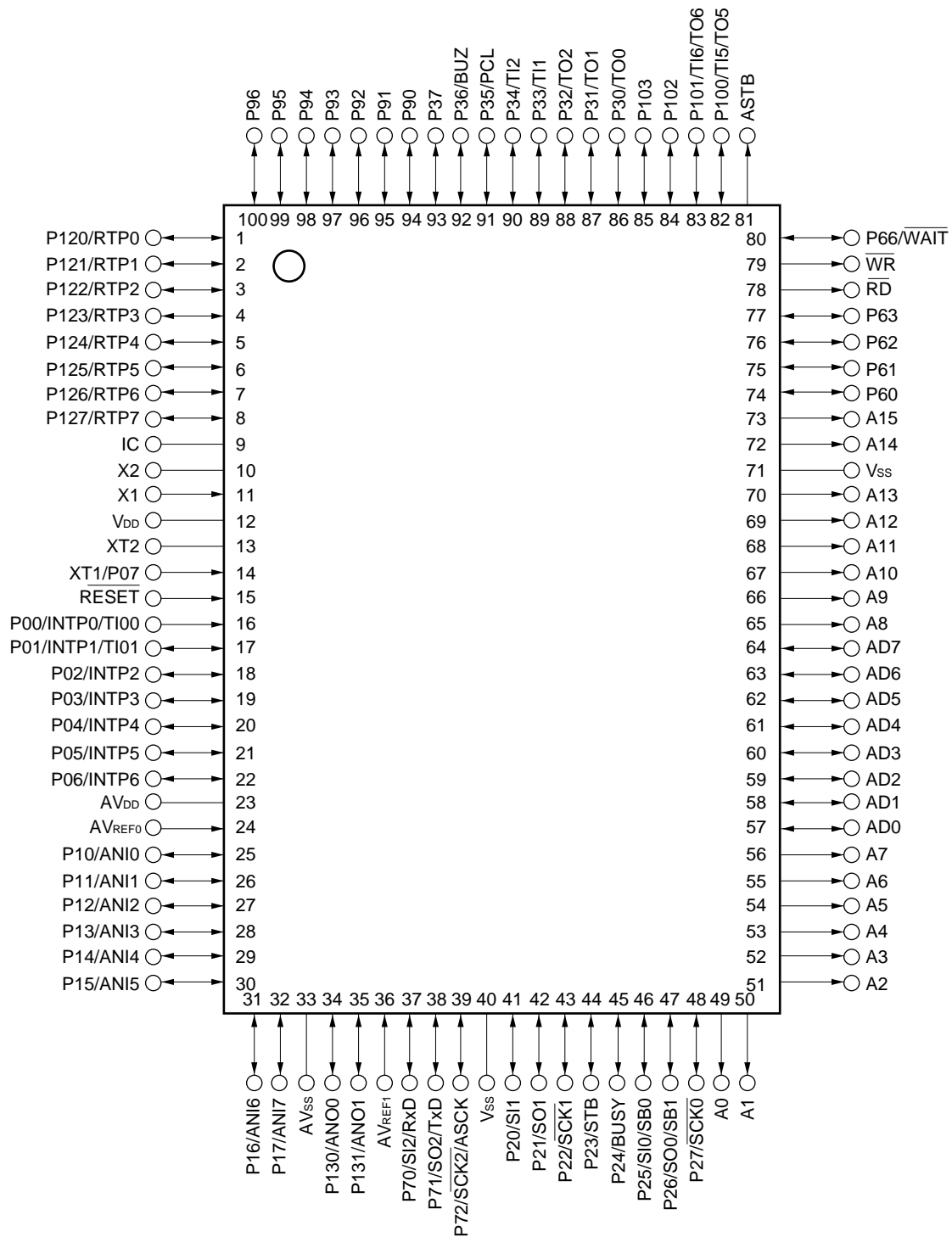
1. PIN CONFIGURATION (Top View)

- 100-pin plastic QFP (Fine pitch) (14 × 14 mm)  
μPD78070AGC-7EA



- Cautions**
1. Connect IC (Internally Connected) pin directly to V<sub>SS</sub>.
  2. Connect AV<sub>DD</sub> pin to V<sub>DD</sub>.
  3. Connect AV<sub>SS</sub> pin to V<sub>SS</sub>.

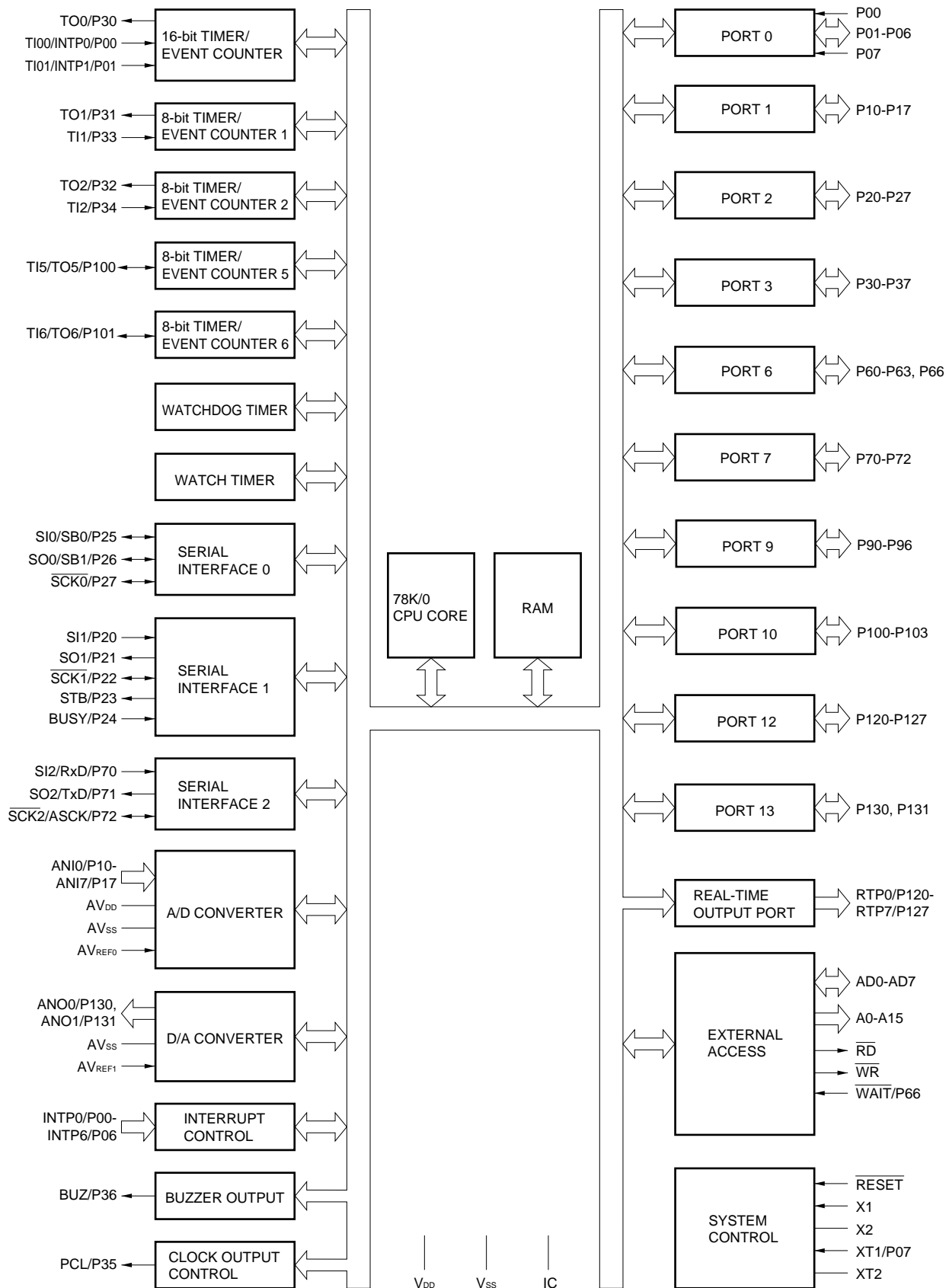
- 100-pin plastic QFP (14 × 20 mm)  
μPD78070AGF-3BA



- Cautions**
1. Connect IC (Internally Connected) pin directly to V<sub>SS</sub>.
  2. Connect AV<sub>DD</sub> pin to V<sub>DD</sub>.
  3. Connect AV<sub>SS</sub> pin to V<sub>SS</sub>.

P00-P07	: Port0	PCL	: Programmable Clock
P10-P17	: Port1	BUZ	: Buzzer Clock
P20-P27	: Port2	STB	: Strobe
P30-P37	: Port3	BUSY	: Busy
P60-P63, P66	: Port6	AD0-AD7	: Address/Data Bus
P70-P72	: Port7	A0-A15	: Address Bus
P90-P96	: Port9	$\overline{RD}$	: Read Strobe
P100-P103	: Port10	$\overline{WR}$	: Write Strobe
P120-P127	: Port12	$\overline{WAIT}$	: Wait
P130, P131	: Port13	ASTB	: Address Strobe
RTP0-RTP7	: Real-time Output Port	X1, X2	: Crystal (Main System Clock)
INTP0-INTP6	: Interrupt from Peripherals	XT1, XT2	: Crystal (Subsystem Clock)
TI00, TI01	: Timer Input	$\overline{RESET}$	: Reset
TI1, TI2, TI5, TI6	: Timer Input	ANI0-ANI7	: Analog Input
TO0-TO2, TO5, TO6	: Timer Output	ANO0, ANO1	: Analog Output
SB0, SB1	: Serial Bus	AV <sub>DD</sub>	: Analog Power Supply
SI0-SI2	: Serial Input	AV <sub>SS</sub>	: Analog Ground
SO0-SO2	: Serial Output	AV <sub>REF0</sub> , AV <sub>REF1</sub>	: Analog Reference Voltage
$\overline{SCK0}$ - $\overline{SCK2}$	: Serial Clock	V <sub>DD</sub>	: Power Supply
RxD	: Receive Data	V <sub>SS</sub>	: Ground
TxD	: Transmit Data	IC	: Internally Connected
ASCK	: Asynchronous Serial Clock		

2. BLOCK DIAGRAM



### 3. PIN FUNCTIONS

#### 3.1 Port Pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function	
P00	Input	Port 0	Input only.	Input	INTP0/TI00
P01	Input/output	8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 <sup>Note1</sup>	Input		Input only.	Input	XT1
P10-P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. <sup>Note2</sup>		Input	ANI0-ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					SCK1
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

- Notes**
1. When using the P07/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the on-chip feedback resistor of the subsystem clock oscillator.
  2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog inputs, their on-chip pull-up resistors are automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P60	Input/output	Port 6 5-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. LED can be driven directly.	Input	—
P61					
P62		When used as an input port, on-chip pull-up resistor can be used by software.	WAIT		
P63					
P66					
P70	Input/output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	SI2/RxD	
P71				SO2/TxD	
P72				SCK2/ASCK	
P90	Input/output	Port 9 7-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port.	Input	—
P91					
P92		When used as an input port, on-chip pull-up resistor can be used by software.			
P93					
P94					
P95					
P96					
P100	Input/output	Port 10 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	TI5/TO5	
P101				TI6/TO6	
P102, P103				—	
P120-P127	Input/output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	RTP0-RTP7	
P130, P131	Input/output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	ANO0, ANO1	

3.2 Non-port Pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/Output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
SCK0	Input/Output	Serial interface serial clock input/output.	Input	P27
SCK1				P22
SCK2				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TI5		External count clock input to 8-bit timer (TM5).		P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO0		Output		16-bit timer output (also used for 14-bit PWM output).
TO1	8-bit timer output.		P31	
TO2			P32	
TO5	8-bit timer output (also used for 8-bit PWM output).		P100/TI5	
TO6			P101/TI6	
PCL	Output		Clock output (for main system clock, subsystem clock trimming).	Input

3.2 Non-port Pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
BUZ	Output	Buzzer output.	Input	P36
RTP0-RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120-P127
AD0-AD7	Input/Output	Data bus for external memory.	Input	—
A0-A15	Output	Address bus for external memory.	Input	—
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	—
$\overline{WR}$		External memory write operation strobe signal output.		—
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV <sub>REF0</sub>	Input	A/D converter reference voltage input.	—	—
AV <sub>REF1</sub>	Input	D/A converter reference voltage input.	—	—
AV <sub>DD</sub>	—	A/D converter analog power supply. Connected to V <sub>DD</sub> .	—	—
AV <sub>SS</sub>	—	A/D converter ground potential. Connected to V <sub>SS</sub> .	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V <sub>DD</sub>	—	Positive power supply.	—	—
V <sub>SS</sub>	—	Ground potential.	—	—
IC	—	Internal connection. Connected directly to V <sub>SS</sub> .	—	—

**3.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

**Table 3-1. Types of Pin Input/Output Circuits (1/2)**

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection of Unused Pins
P00/INTP0/TI00	2	Input	Connect to V <sub>SS</sub> .
P01/INTP1/TI01	8-A	Input/Output	Independently connect to V <sub>SS</sub> via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V <sub>DD</sub> .
P10/ANI0-P17/ANI7	11	Input/Output	Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/SCK $\bar{1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/SCK $\bar{0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P60-P63		13-C	Input/Output
P66/ $\overline{\text{WAIT}}$	5-A	Input/Output	Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.

★

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection of Unused Pins
P70/SI2/RxD	8-A	Input/Output	Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.
P71/SO2/TxD	5-A		
P72/SCK2/ASCK	8-A		
P90-P93	13-C	Input/Output	Independently connect to V <sub>DD</sub> via a resistor.
P94-P96	5-A	Input/Output	Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.
P100/TI5/TO5	8-A		
P101/TI6/TO6	5-A		
P102, P103			
P120/RTP0-P127/RTP7			
P130/ANO0, P131/ANO1	12-A	Input/Output	Independently connect to V <sub>SS</sub> via a resistor.
AD0-AD7	5-E	Input/Output	Independently connect to V <sub>DD</sub> via a resistor.
A0-A15	5-A	Output	Leave open.
$\overline{RD}$			
$\overline{WR}$			
ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV <sub>REF0</sub>	—		Connect to V <sub>SS</sub> .
AV <sub>REF1</sub>			Connect to V <sub>DD</sub> .
AV <sub>DD</sub>			
AV <sub>SS</sub>			Connect to V <sub>SS</sub> .
IC			Connect directly to V <sub>SS</sub> .

Figure 3-1. Pin Input/Output Circuits (1/2)

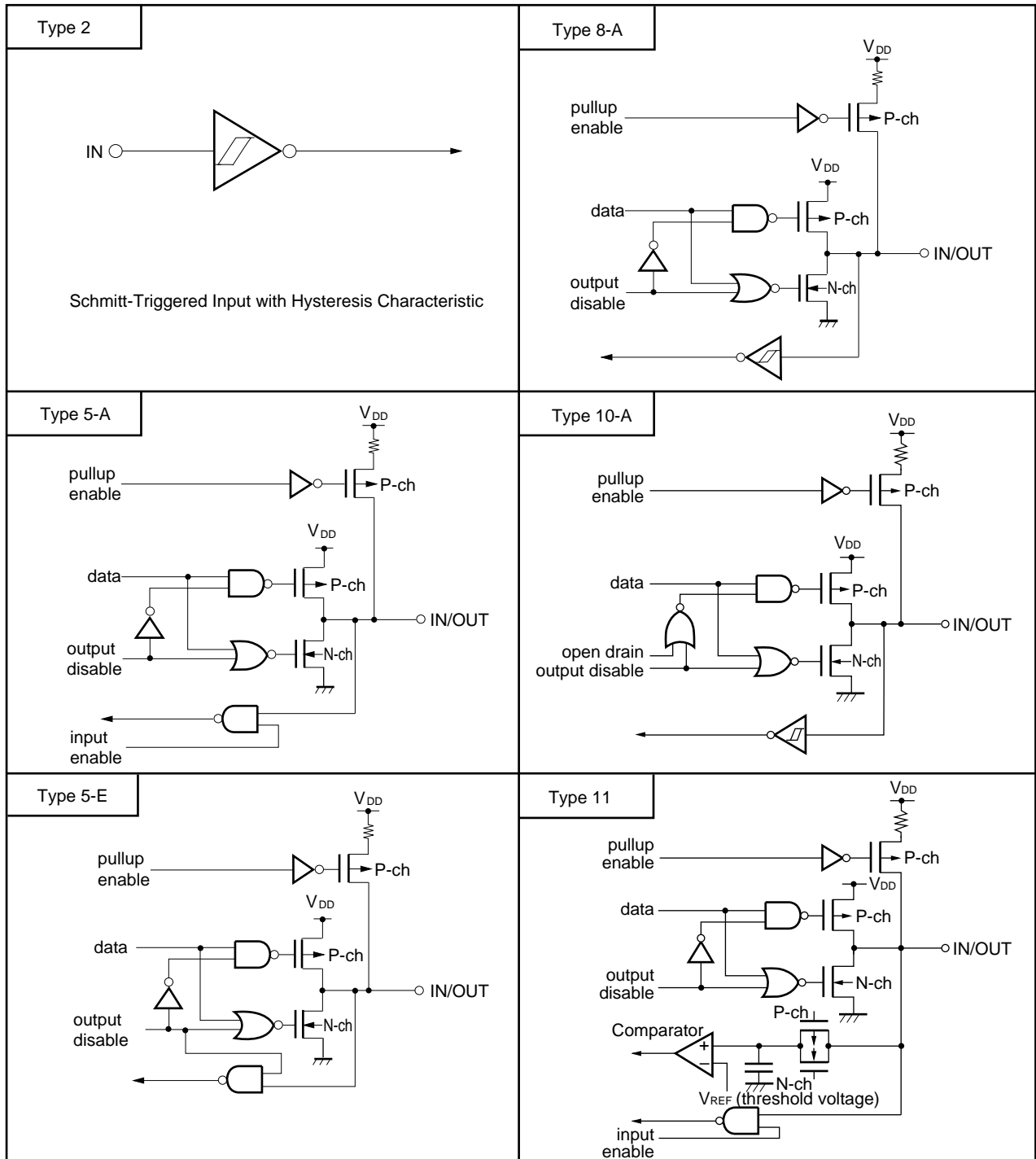
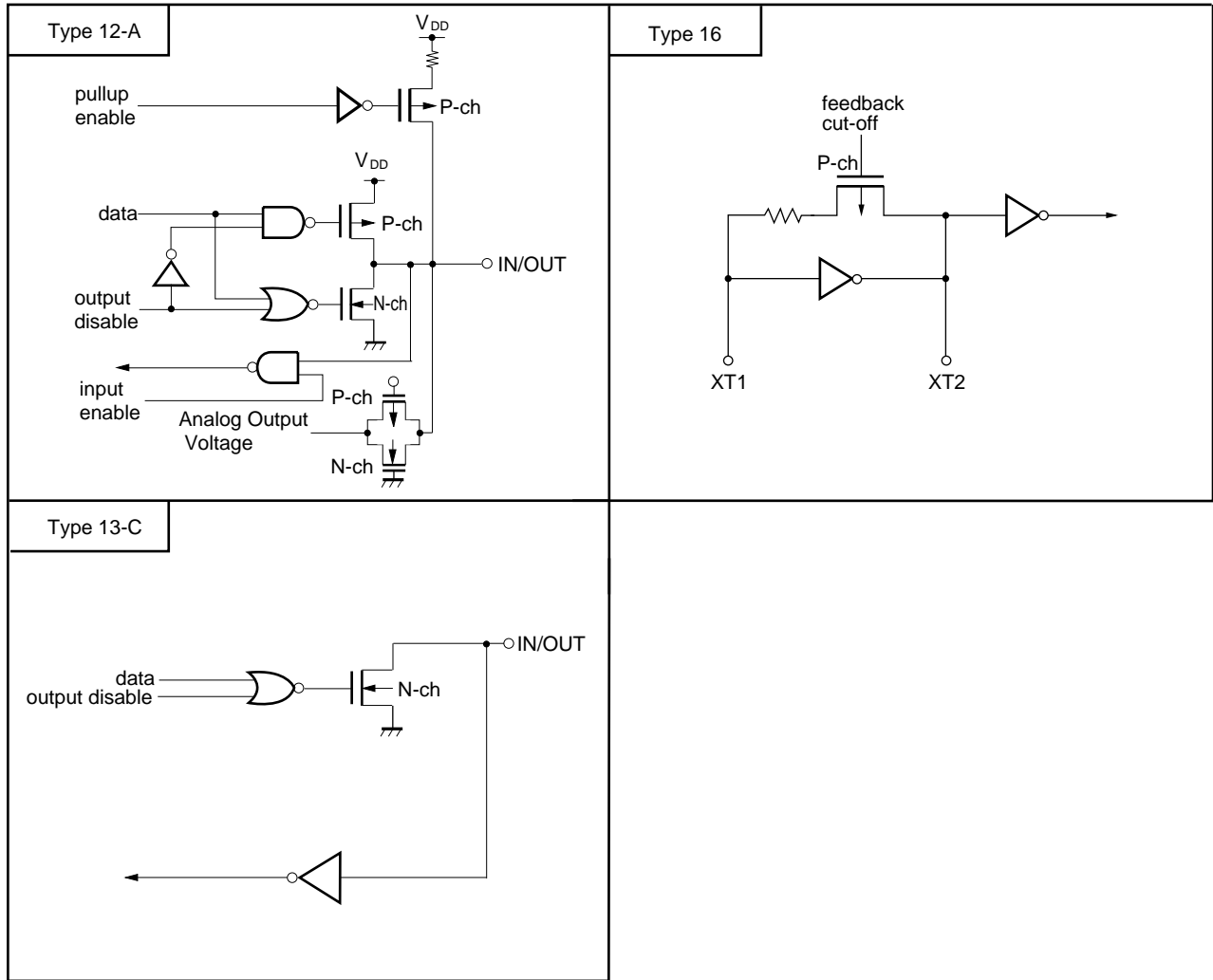


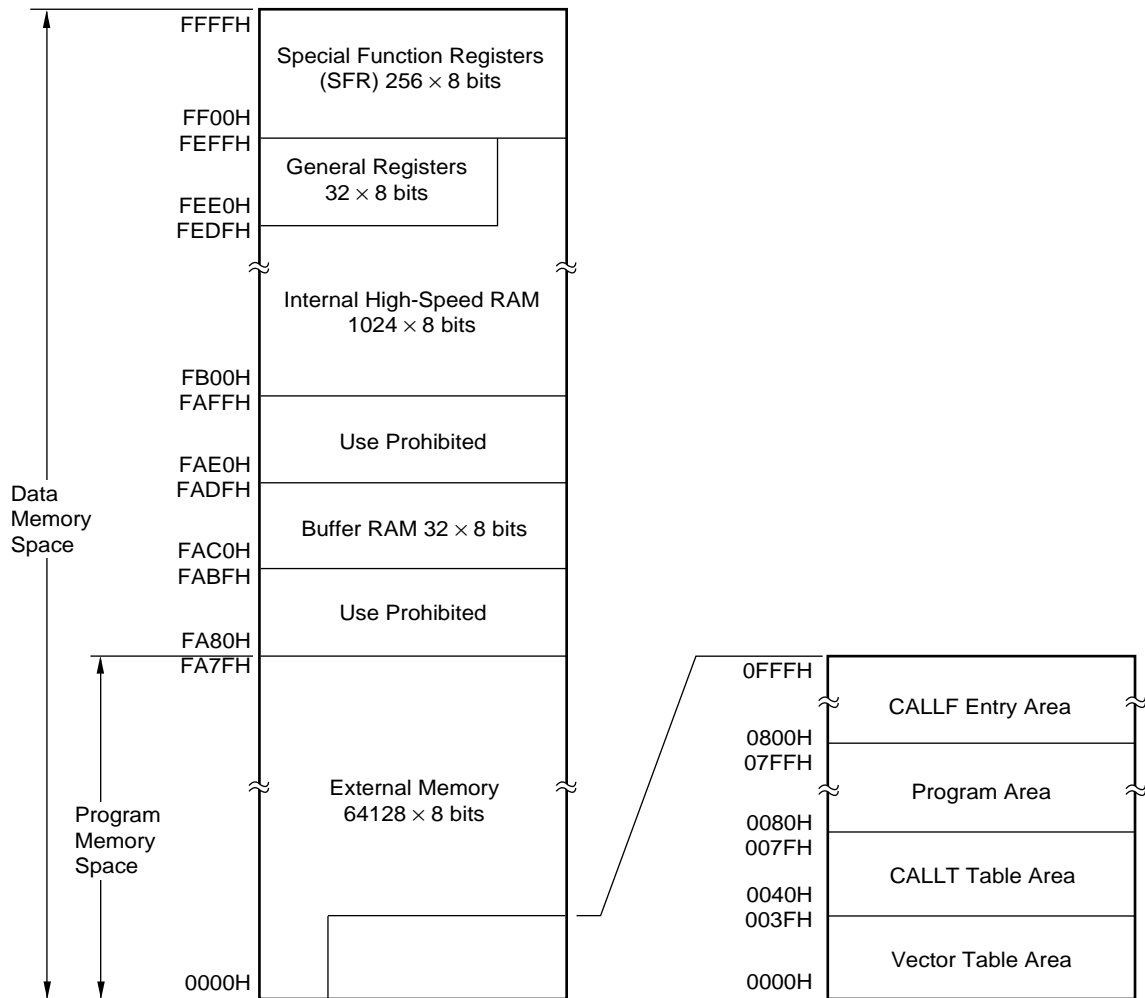
Figure 3-1. Pin Input/Output Circuits (2/2)



### 4. MEMORY SPACE

The memory map of the μPD78070A is shown in Figure 4-1.

**Figure 4-1. Memory Map**



## 5. PERIPHERAL HARDWARE FUNCTIONS

### 5.1 Ports

Input/output ports are classified into three types.

• CMOS inputs (P00, P07)	: 2
• CMOS input/outputs (P01-P06, Port 1-3, P66, Port 7, P94-P96, Port 10, Port 12, Port 13)	: 51
• N-ch open-drain input/outputs (P60-P63, P90-P93)	: 8
<hr/> Total	: 61

**Table 5-1. Functions of Ports**

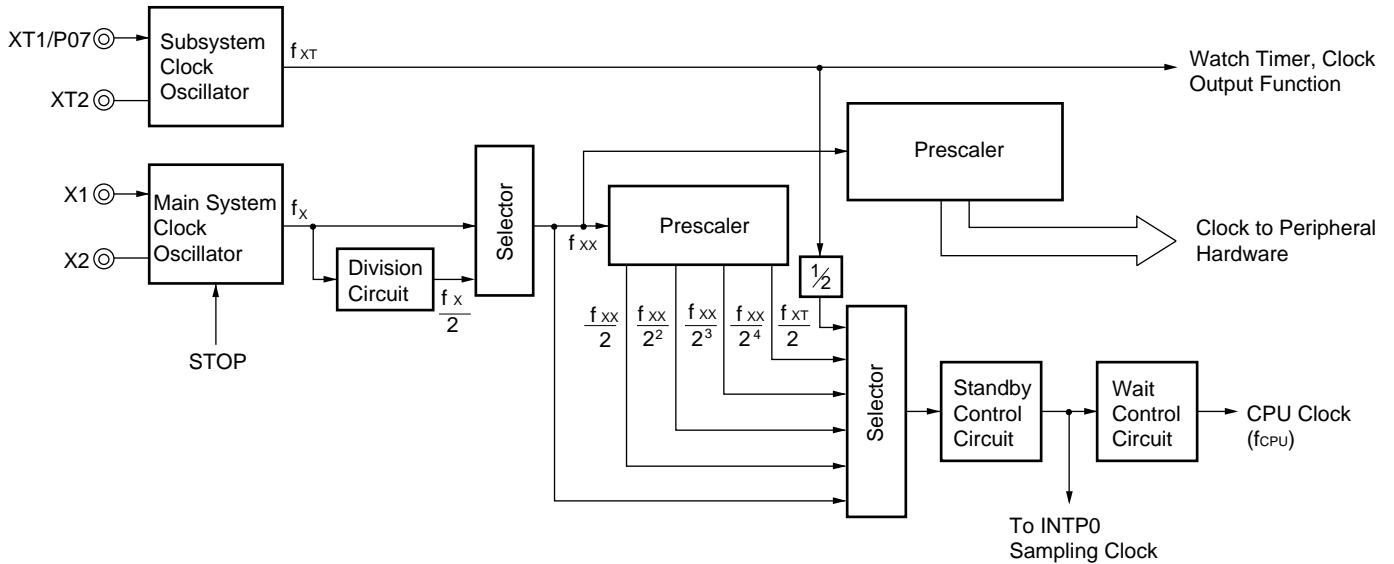
Port Name	Pin Name	Function
Port 0	P00, P07	Input only.
	P01-P06	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 1	P10-P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 2	P20-P27	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 3	P30-P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 6	P60-P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. LED can be driven directly.
	P66	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 7	P70-P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 9	P90-P93	N-ch open-drain input/output port. Input/output can be specified bit-wise.
	P94-P96	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 10	P100-P103	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 12	P120-P127	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 13	P130, P131	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.

**5.2 Clock Generator**

There are two kinds of clock generators: main system and subsystem clock generators. It is possible to change the instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

**Figure 5-1. Clock Generator Block Diagram**



5.3 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 4 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter 1, 2	8-bit Timer/ Event Counter 5, 6	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	2 channels	—	—
Function	Timer output	1 output	2 outputs	2 outputs	—	—
	PWM output	1 output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—	—
	Square wave output	1 output	2 outputs	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—	—
	Interrupt request	2	2	2	1	1
	Test input	—	—	—	1	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

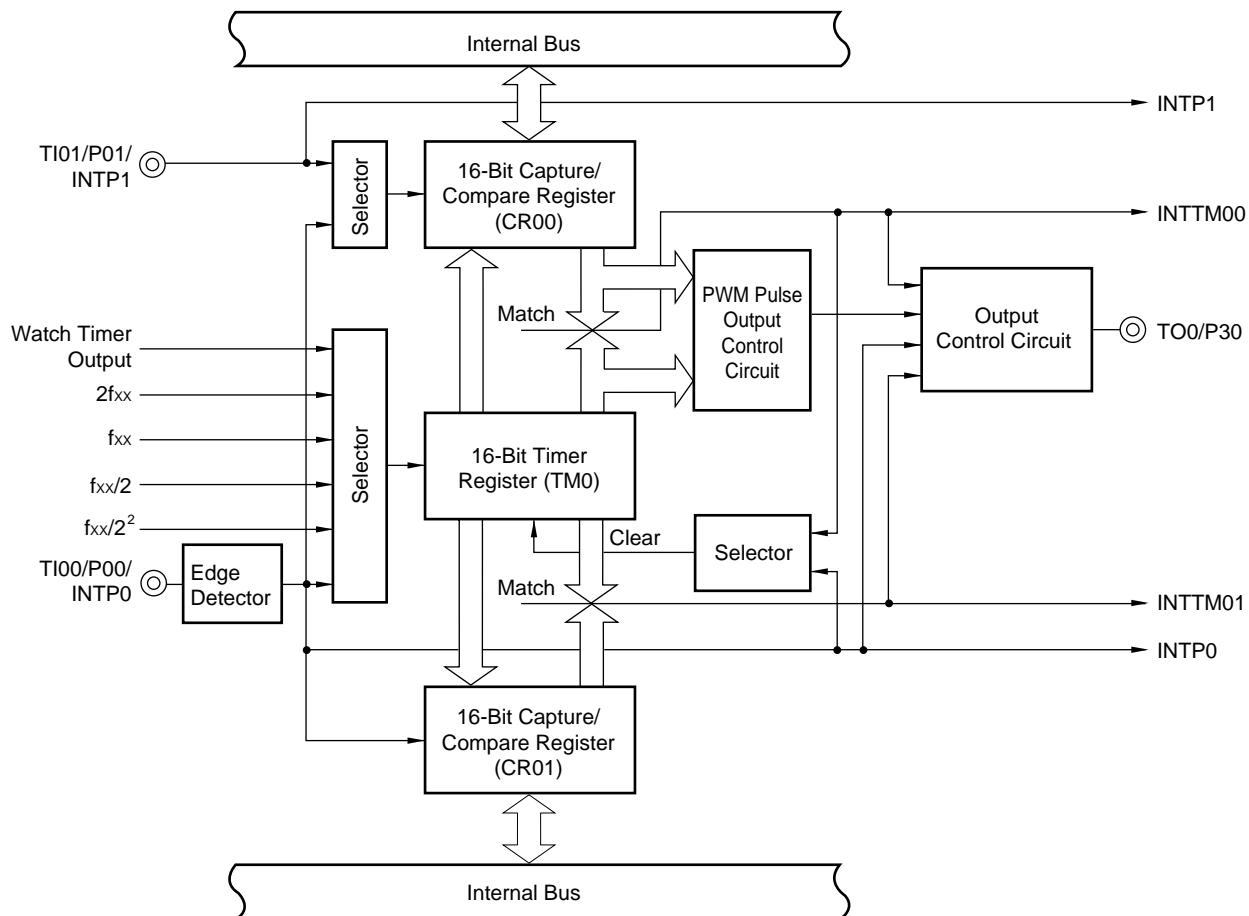


Figure 5-3. 8-Bit Timer/Event Counter 1, 2 Block Diagram

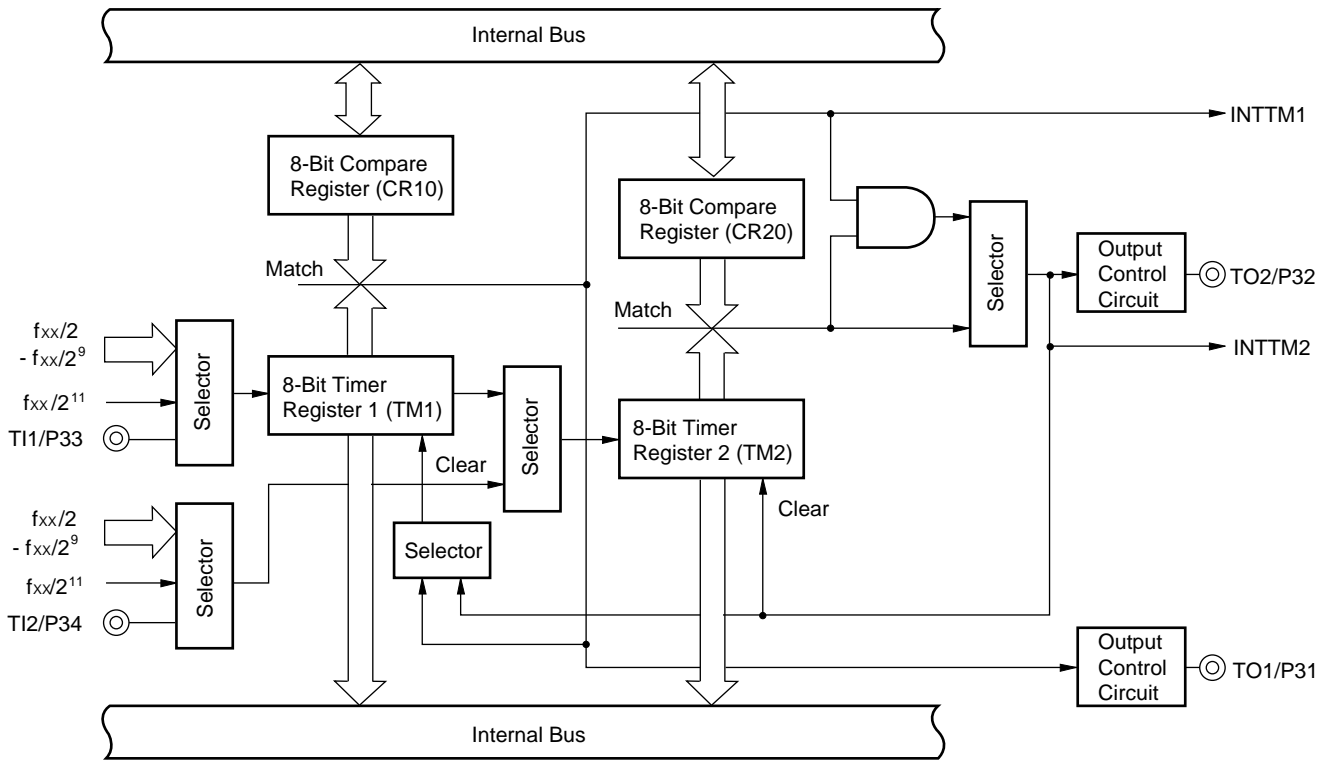
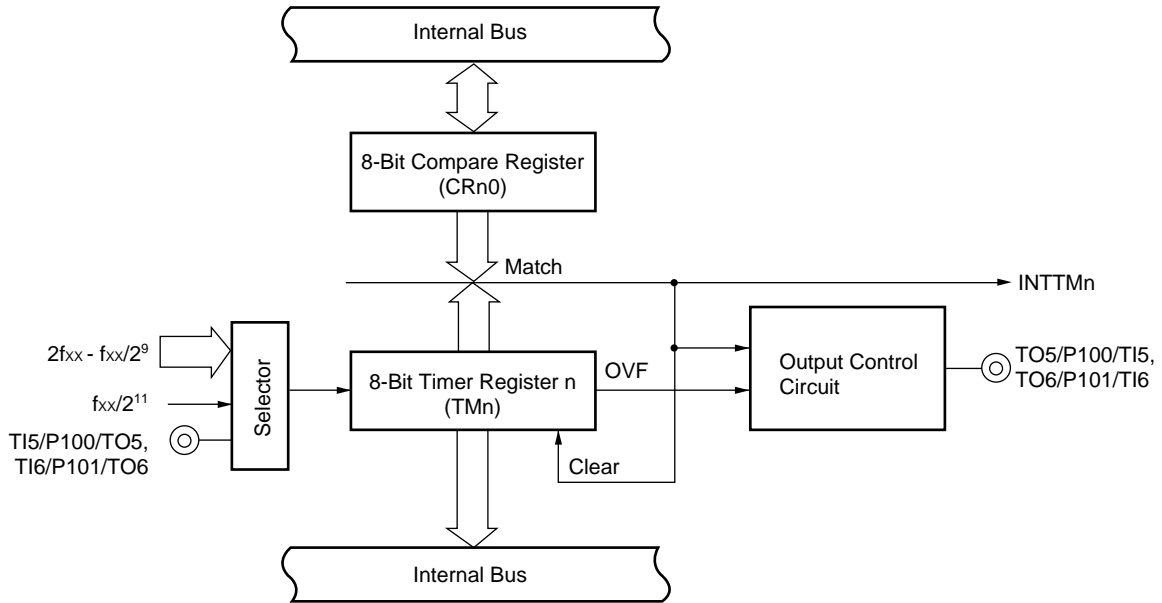


Figure 5-4. 8-Bit Timer/Event Counter 5, 6 Block Diagram



n = 5, 6

Figure 5-5. Watch Timer Block Diagram

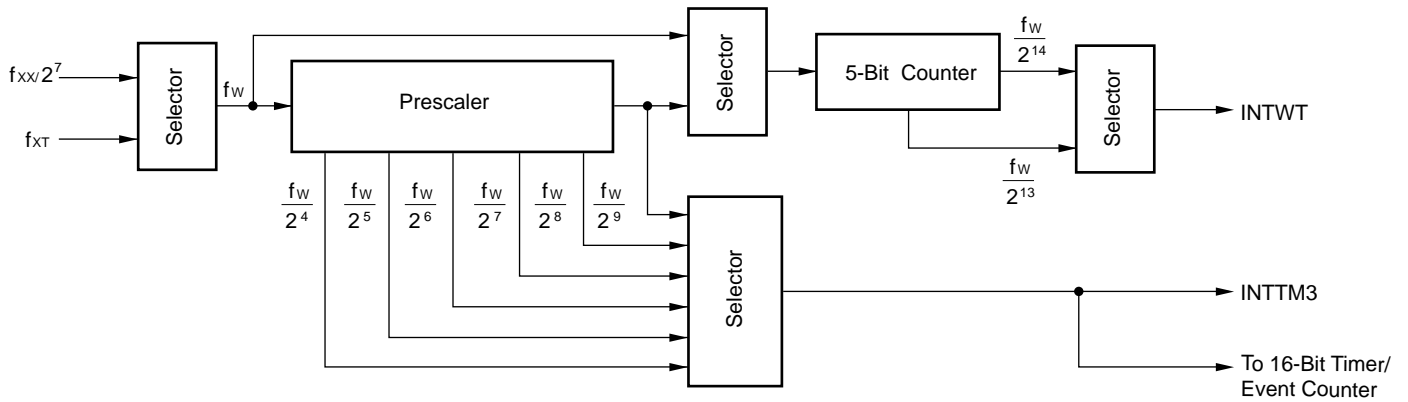
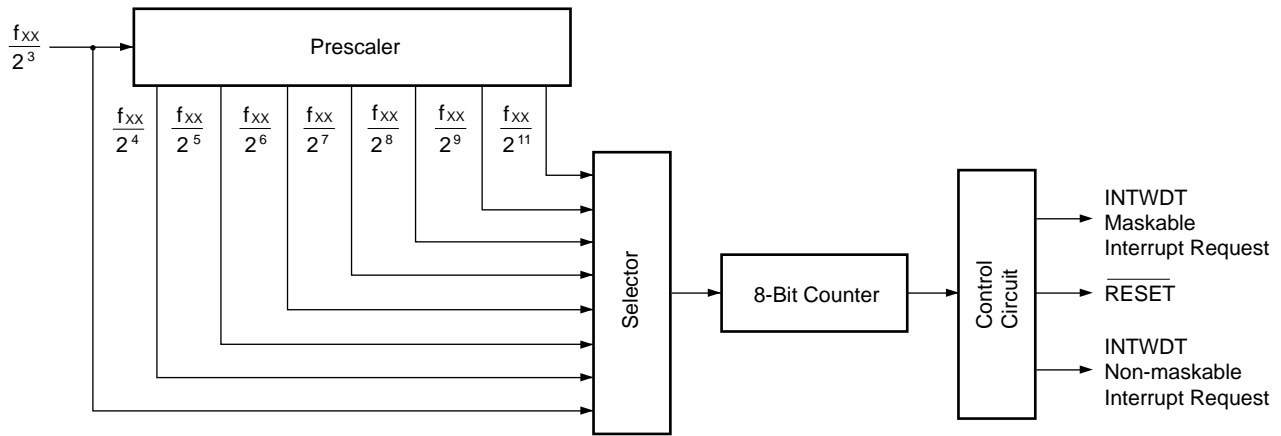


Figure 5-6. Watchdog Timer Block Diagram

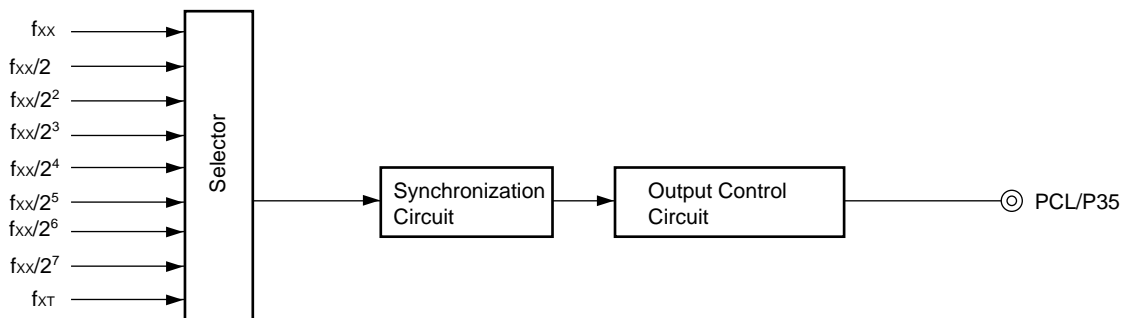


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)
- 32.768 kHz (at subsystem clock frequency of 32.768 kHz)

Figure 5-7. Clock Output Control Circuit Block Diagram

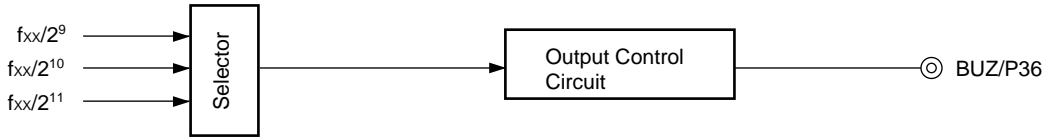


**5.5 Buzzer Output Control Circuit**

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

**Figure 5-8. Buzzer Output Control Circuit Block Diagram**



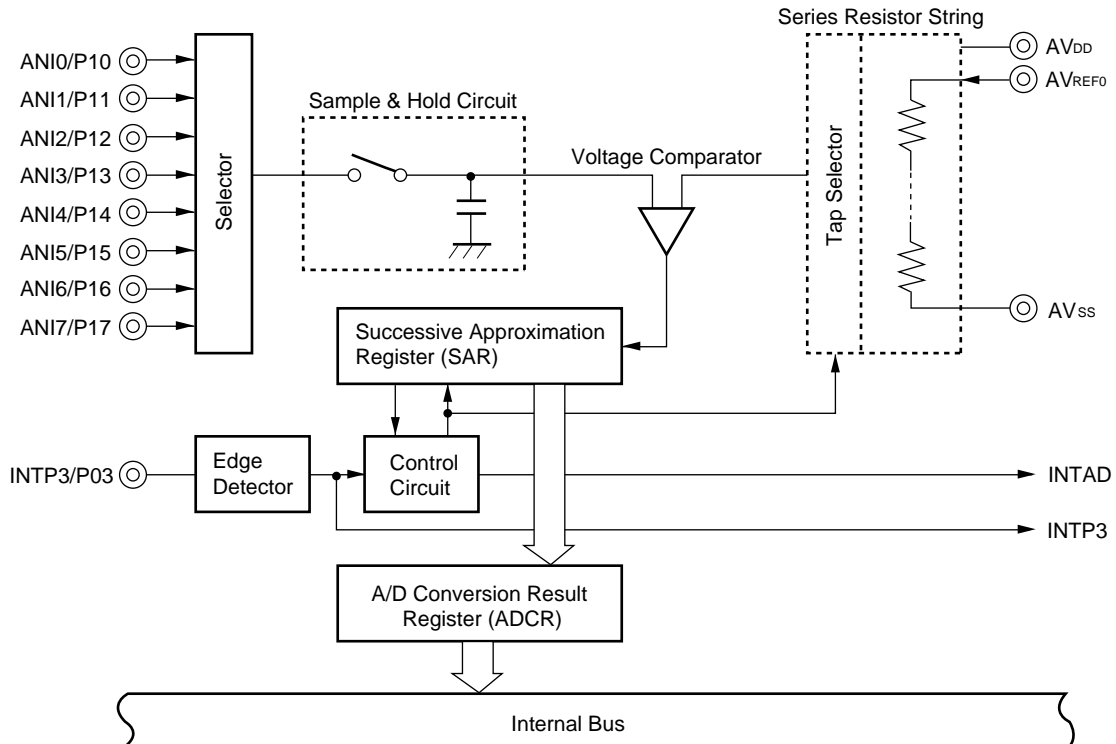
**5.6 A/D Converter**

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

**Figure 5-9. A/D Converter Block Diagram**

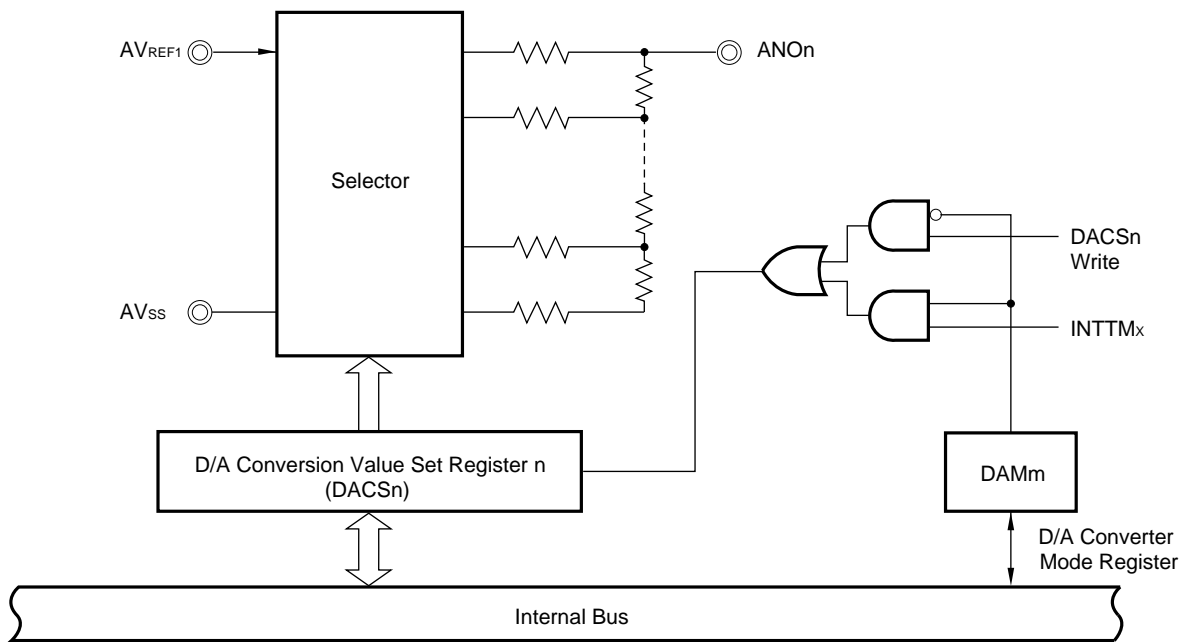


**5.7 D/A Converter**

The D/A converter consists of two 8-bit resolution channels.

The conversion method is the R-2R resistor ladder method.

Figure 5-10. D/A Converter Block Diagram



n = 0, 1  
 m = 4, 5  
 x = 1, 2

5.8 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	○ (MSB/LSB first bit switching possible)	○ (MSB/LSB first bit switching possible)	○ (MSB/LSB first bit switching possible)
3-wire serial I/O mode with automatic data transmit/receive function	—	○ (MSB/LSB first bit switching possible)	—
2-wire serial I/O mode	○ (MSB first)	—	—
Serial bus interface (SBI) mode	○ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	○ (On-chip dedicated baud rate generator)

Figure 5-11. Serial Interface Channel 0 Block Diagram

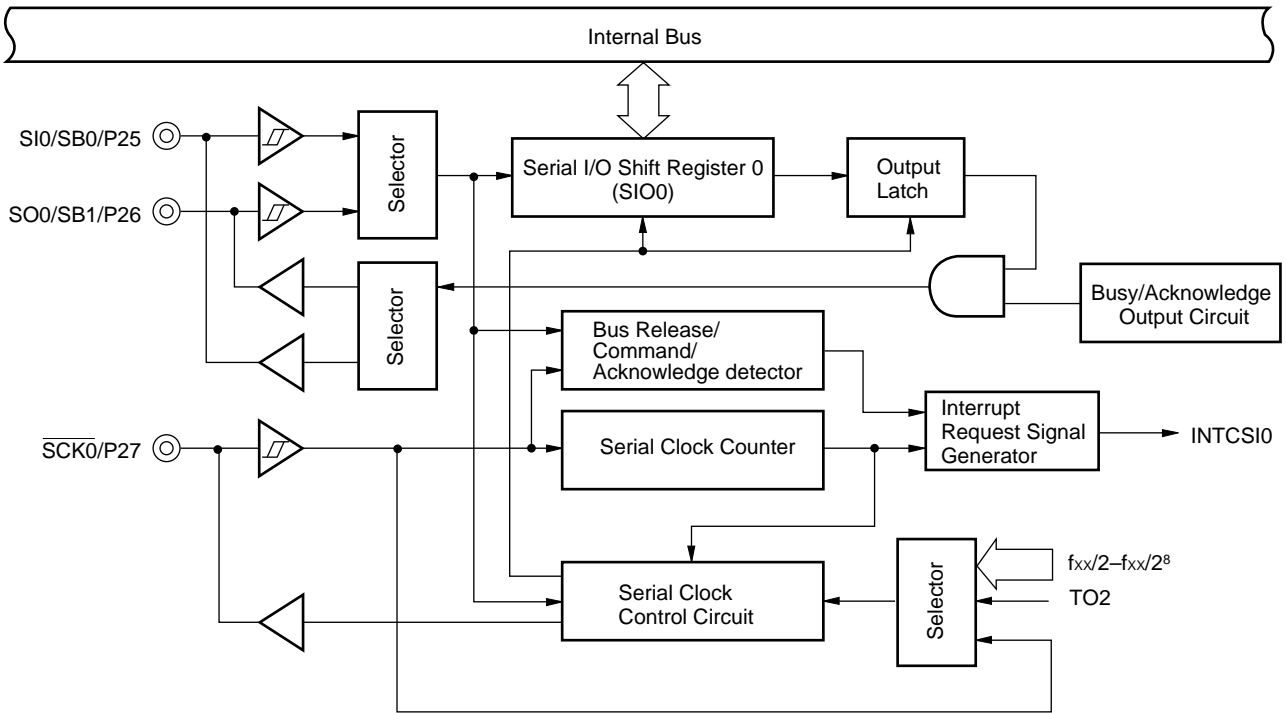


Figure 5-12. Serial Interface Channel 1 Block Diagram

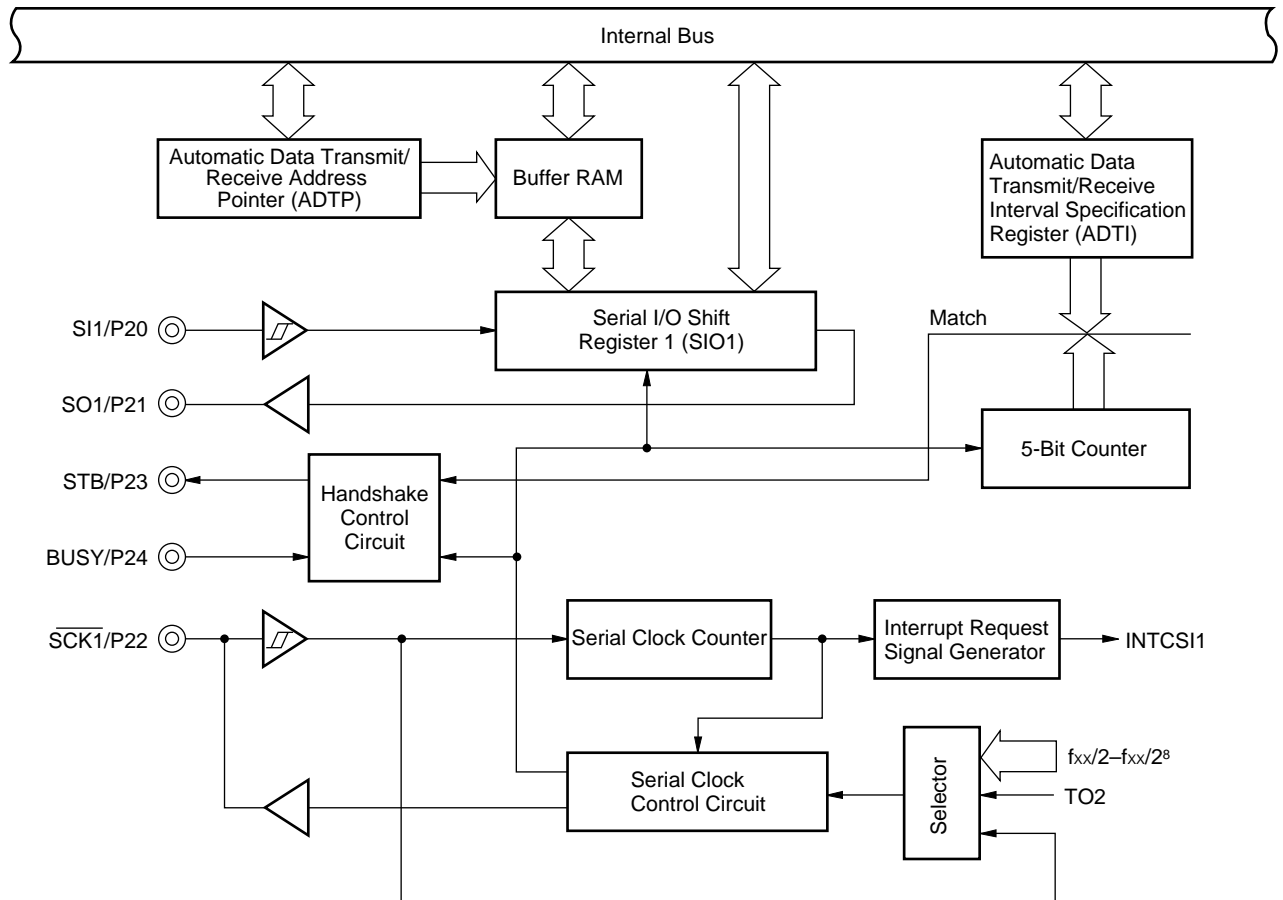
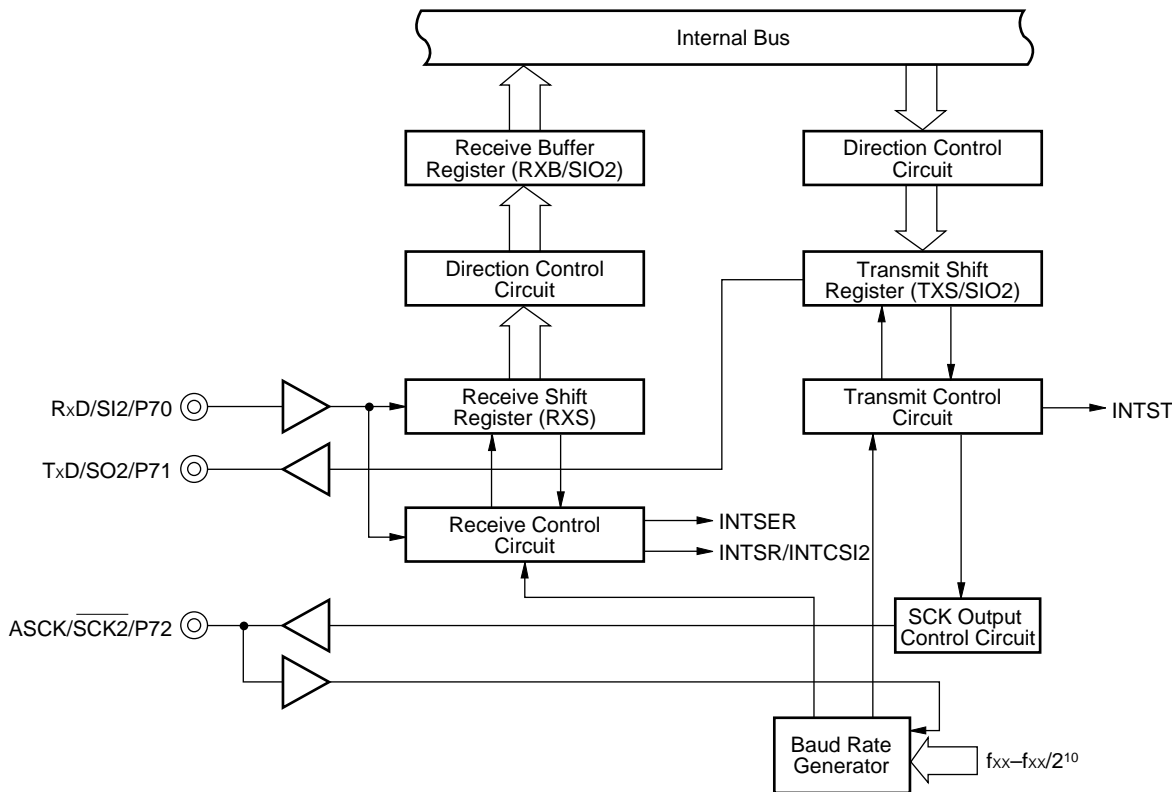


Figure 5-13. Serial Interface Channel 2 Block Diagram

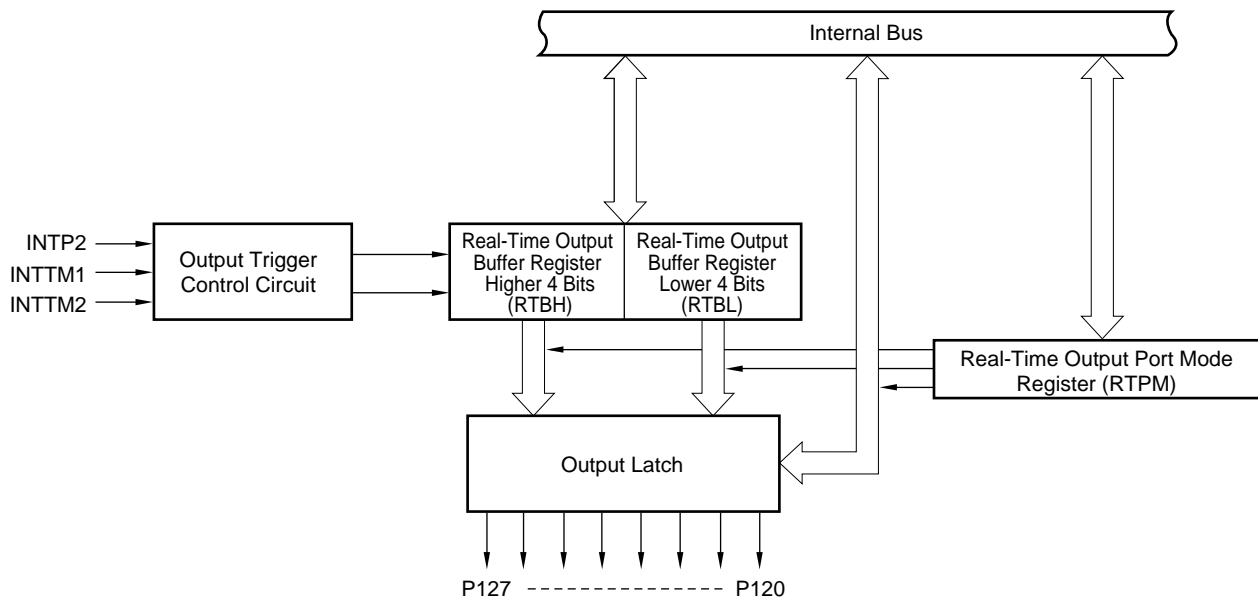


5.9 Real-Time Output Port

Data set previously in the real-time output buffer is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is a real-time output function. Pins used to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motors, etc.

Figure 5-14. Real-Time Output Port Block Diagram



## 6. INTERRUPT FUNCTIONS AND TEST FUNCTION

### 6.1 Interrupt Functions

A total of 24 interrupt functions are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupts : 22
- Software interrupt : 1

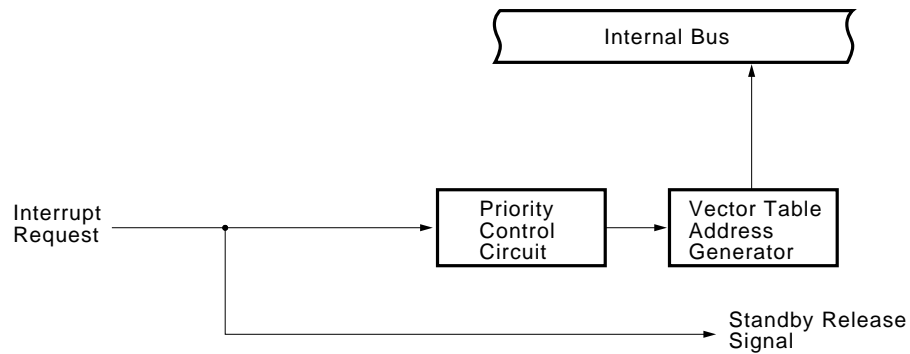
**Table 6-1. List of Interrupt Sources**

Interrupt Type	Default Priority <sup>Note1</sup>	Interrupt Source		Internal/ External	Vector Table Address	Basic Structure Type <sup>Note2</sup>
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0			Completion of serial interface channel 0 transfer	Internal
	9	INTCSI1	Completion of serial interface channel 1 transfer	0016H		
	10	INTSER	Occurrence of serial interface channel 2 UART reception error	0018H		
	11	INTSR	Completion of serial interface channel 2 UART reception	001AH		
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	12	INTST	Completion of serial interface channel 2 UART transmission	001CH		
	13	INTTM3	Reference time interval signal from watch timer	001EH		
	14	INTTM00	Generation of matching signal of 16-bit timer register and capture/compare register (CR00)	0020H		
	15	INTTM01	Generation of matching signal of 16-bit timer register and capture/compare register (CR01)	0022H		
	16	INTTM1	Generation of matching signal of 8-bit timer/event counter 1	0024H		
	17	INTTM2	Generation of matching signal of 8-bit timer/event counter 2	0026H		
	18	INTAD	Completion of A/D conversion	0028H		
	19	INTTM5	Generation of matching signal of 8-bit timer/event counter 5	002AH		
	20	INTTM6	Generation of matching signal of 8-bit timer/event counter 6	002CH		
Software	—	BRK	Execution of BRK instruction	Internal	003EH	(E)

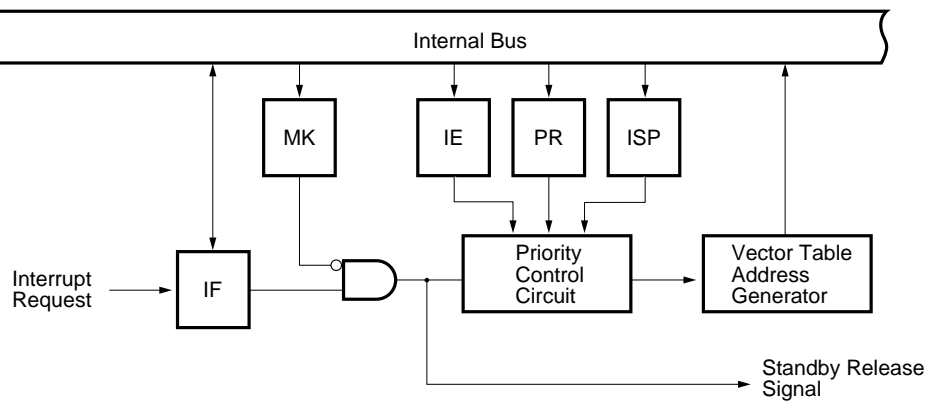
- Notes**
1. Default priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest priority and 20 is the lowest priority.
  2. Basic structure types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

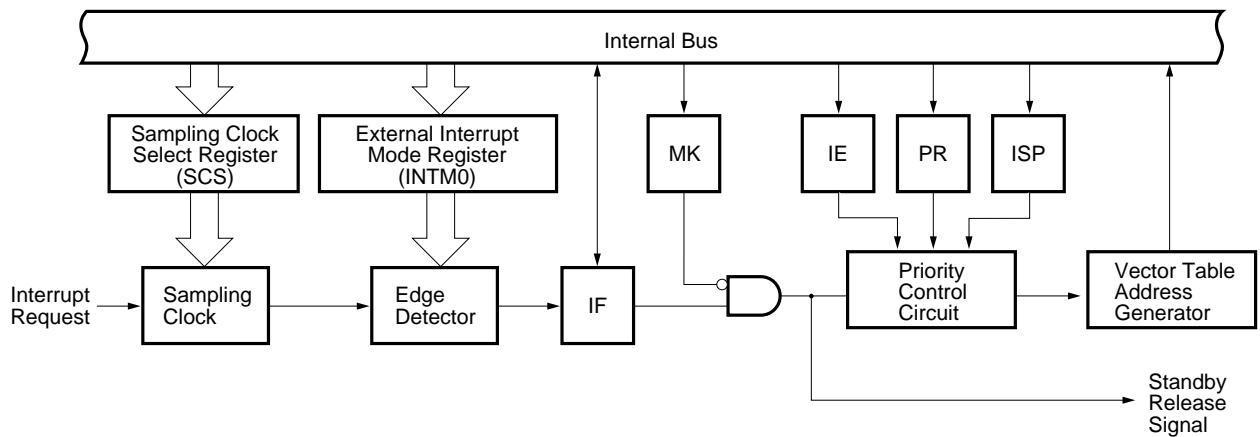
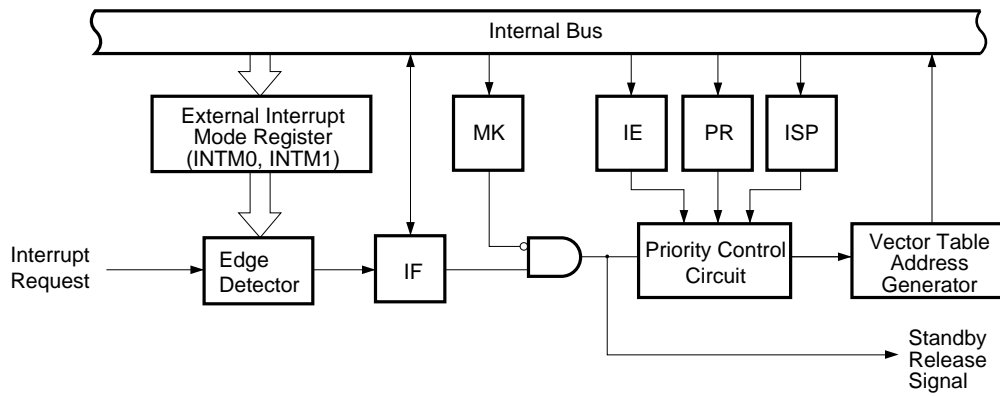
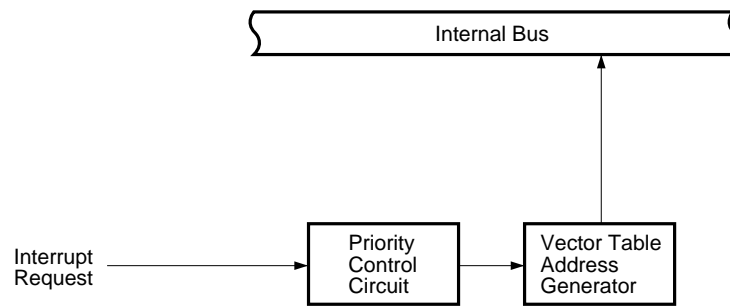


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTPO)



(E) Software interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

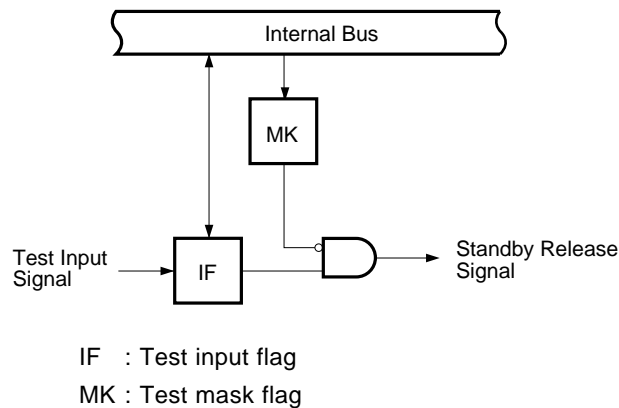
6.2 Test Function

Table 6-2 shows the test function available.

Table 6-2. Test Input Source

Test Input Source		Internal/
Name	Trigger	External
INTWT	Overflow of watch timer	Internal

Figure 6-2. Basic Configuration of Test Function



## 7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the RAM and SFR. The μPD78070A is a ROM-less product, and therefore requires the connection of external ROM. Connect external devices using an independent address bus and data bus.

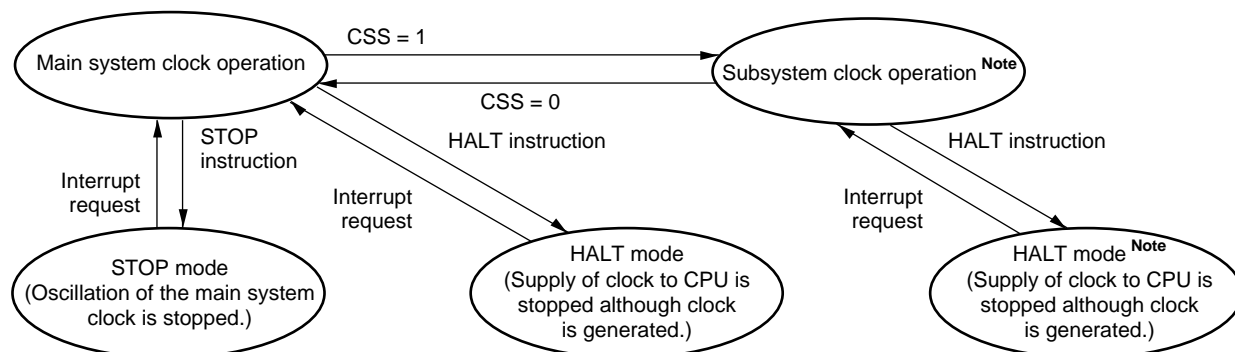
## 8. STANDBY FUNCTION

The standby function is designed to reduce current consumption.

It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 8-1. Standby Function



**Note** Current consumption is reduced by shutting off the main system clock. If the CPU is operating on the subsystem clock, shut off the main system clock by setting bit 7 (MCC) of the processor clock control register (PCC). You cannot use a STOP instruction.

**Caution** When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

## 9. RESET FUNCTION

There are the following two reset methods.

- External reset input by  $\overline{\text{RESET}}$  pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	\$saddr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											

Note Except r = A

2nd Operand 1st Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	\$addr16	1	None
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#word	AX	rp <sup>Note</sup>	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW <sup>Note</sup>						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

**Note** Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	laddr16	laddr11	[addr5]	\$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			78125	bps
					39063	bps

(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t <sub>KCY13</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t <sub>KH13</sub> , t <sub>KL13</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			39063	bps
					19531	bps
ASCK rise, fall time	t <sub>R13</sub> , t <sub>F13</sub>				160	ns

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

Parameter	Symbol	Test Conditions	Ratings	Unit	
Supply voltage	V <sub>DD</sub>		−0.3 to +7.0	V	
	AV <sub>DD</sub>		−0.3 to V <sub>DD</sub> +0.3	V	
	AV <sub>REF0</sub>		−0.3 to V <sub>DD</sub> +0.3	V	
	AV <sub>REF1</sub>		−0.3 to V <sub>DD</sub> +0.3	V	
	AV <sub>SS</sub>		−0.3 to +0.3	V	
Input voltage	V <sub>I1</sub>	P00-P07, P10-P17, P20-P27, P30-P37, P66, P70-P72, P94-P96, P100-P103, P120-P127, P130, P131, AD0-AD7, X1, X2, XT2, $\overline{\text{RESET}}$	−0.3 to V <sub>DD</sub> +0.3	V	
	V <sub>I2</sub>	P60-P63, P90-P93	N-ch open-drain	−0.3 to V <sub>DD</sub> +0.3	
Output voltage	V <sub>O</sub>		−0.3 to V <sub>DD</sub> +0.3	V	
Analog input voltage	V <sub>AN</sub>	P10-P17	Analog input pins	AV <sub>SS</sub> − 0.3 to AV <sub>REF0</sub> + 0.3	
Output current, high	I <sub>OH</sub>	Per pin		−10	mA
		Total for P30-P37, P60-P63, P66, P90-P96, P100-P103, P120-P127, A14, A15, $\overline{\text{RD}}$ , $\overline{\text{WR}}$ , ASTB		−15	mA
		Total for P01-P06, P10-P17, P20-P27, P70-P72, P130, P131, AD0-AD7, A0-A13		−15	mA
Output current, low	I <sub>OL</sub> <sup>Note</sup>	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for A8-A13	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P60-P63, A14, A15	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P30-P37, P66, P90-P96, P100-P103, P120-P127, $\overline{\text{RD}}$ , $\overline{\text{WR}}$ , ASTB	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P20-P27, AD0-AD7, A0-A7	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01-P06, P10-P17, P70-P72, P130, P131	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T <sub>A</sub>		−40 to +85	°C	
Storage temperature	T <sub>stg</sub>		−65 to +150	°C	

**Note** The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

**Caution** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**Capacitance** ( $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{IN}$	$f = 1\text{ MHz}$ , Unmeasured pins returned to 0 V.			15	pF
Output capacitance	$C_{OUT}$				15	pF
I/O capacitance	$C_{IO}$				15	pF

**Main System Clock Oscillator Characteristics** ( $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ to }5.5\text{ V}$ )

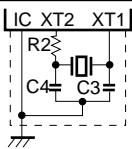
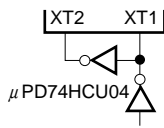
Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency ( $f_x$ ) <sup>Note1</sup>	$V_{DD} = \text{Oscillation voltage range}$	1.0		5.0	MHz
		Oscillation stabilization time <sup>Note2</sup>	After $V_{DD}$ came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency ( $f_x$ ) <sup>Note1</sup>		1.0		5.0	MHz
		Oscillation stabilization time <sup>Note2</sup>	$V_{DD} = 4.5\text{ to }5.5\text{ V}$			10 30	ms
External clock		X1 input frequency ( $f_x$ ) <sup>Note1</sup>		1.0		5.0	MHz
		X1 input high- and low-level widths ( $t_{XH}$ , $t_{XL}$ )		85		500	ns

- Notes 1.** Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.  
**2.** Time required for oscillation to stabilize after a reset or the STOP mode has been released.

**Cautions 1.** When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
  - Do not cross the wiring over other signal lines.
  - Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
  - Always keep the ground point of the capacitor of the oscillation circuit at the same potential as  $V_{SS}$ .
  - Do not connect the power source to a ground pattern through which a high current flows.
  - Do not extract signals from the oscillation circuit.
- 2.** When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

**Subsystem Clock Oscillator Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency ( $f_{XT}$ ) <sup>Note1</sup>		32	32.768	35	kHz
		Oscillation stabilization time <sup>Note2</sup>	$V_{DD} = 4.5$ to $5.5$ V		1.2	2	s
External clock		XT1 input frequency ( $f_{XT}$ ) <sup>Note1</sup>		32		100	kHz
		XT1 input high-, low-level widths ( $t_{XTH}$ , $t_{XTL}$ )		5		15	μs

- Notes**
1. Only the oscillator characteristics are shown. For the instruction execution time, refer to AC Characteristics.
  2. Time required for oscillation to stabilize after  $V_{DD}$  reaches the minimum value of the oscillation voltage range.

**Cautions**

1. When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- Keep the wiring length as short as possible.
  - Do not cross the wiring over other signal lines.
  - Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
  - Always keep the ground point of the capacitor of the oscillation circuit at the same potential as  $V_{SS}$ .
  - Do not connect the power source pattern through which a high current flows.
  - Do not extract signals from the oscillation circuit.
2. The amplification factor of the subsystem clock oscillator is designed to be low to reduce the current consumption and therefore, the subsystem clock oscillator is influenced by noise more easily than the main system clock oscillator. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH1</sub>	P10-P17, P21, P23, P30-P32, P35-P37, P66, P71, P94-P96, P102, P103, P120-P127, P130, P131, AD0-AD7	0.7V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH2</sub>	P00-P06, P20, P22, P24-P27, P33, P34, P70, P72, P100, P101, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH3</sub>	P60-P63, P90-P93 (N-ch open-drain)	0.7V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH4</sub>	X1, X2	V <sub>DD</sub> -0.5		V <sub>DD</sub>	V	
	V <sub>IH5</sub>	XT1/P07, XT2	V <sub>DD</sub> = 4.5 to 5.5 V	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
			0.9V <sub>DD</sub>		V <sub>DD</sub>	V	
Input voltage, low	V <sub>IL1</sub>	P10-P17, P21, P23, P30-P32, P35-P37, P66, P71, P94-P96, P102, P103, P120-P127, P130, P131, AD0-AD7	0		0.3V <sub>DD</sub>	V	
	V <sub>IL2</sub>	P00-P06, P20, P22, P24-P27, P33, P34, P70, P72, P100, P101, RESET	0		0.2V <sub>DD</sub>	V	
	V <sub>IL3</sub>	P60-P63, P90-P93 (N-ch open-drain)	V <sub>DD</sub> = 4.5 to 5.5 V	0		0.3V <sub>DD</sub>	V
				0		0.2V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2	0		0.4	V	
V <sub>IL5</sub>	XT1/P07, XT2	V <sub>DD</sub> = 4.5 to 5.5 V	0		0.2V <sub>DD</sub>	V	
			0		0.1V <sub>DD</sub>	V	
Output voltage, high	V <sub>OH</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = -1 mA	V <sub>DD</sub> -1.0			V	
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> -0.5			V	
Output voltage, low	V <sub>OL1</sub>	P60-P63	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 15 mA	0.4	2.0	V	
		P01-P06, P10-P17, P20-P27, P30-P37, P66, P70-P72, P90-P96, P100-P103, P120-P127, P130, P131, AD0-AD7, A0-A15, RD, WR, ASTB	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 1.6 mA		0.4	V	
	V <sub>OL2</sub>	SB0, SB1, SCK0	V <sub>DD</sub> = 4.5 to 5.5 V, Open-drain, pulled up (R = 1 k $\Omega$ )		0.2V <sub>DD</sub>	V	
	V <sub>OL3</sub>	I <sub>OL</sub> = 400 μA			0.5	V	

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	P00-P06, P10-P17, P20-P27, P30-P37, P60-P63, P66, P70-P72, P90-P96, P100-P103, P120- P127, P130, P131, AD0-AD7, $\overline{\text{RESET}}$			3	μA
	I <sub>LIH2</sub>		X1, X2, XT1/P07, XT2			20	μA
Input leakage current, low	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	P00-P06, P10-P17, P20-P27, P30-P37, P60-P63, P66, P70-P72, P90-P96, P100-P103, P120- P127, P130, P131, AD0-AD7, $\overline{\text{RESET}}$			-3	μA
	I <sub>LIL2</sub>		X1, X2, XT1/P07, XT2			-20	μA
Output leakage current, high	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub>				3	μA
Output leakage current, low	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V				-3	μA
Software pull-up resistor	R	V <sub>IN</sub> = 0 V, P01-P06, P10- P17, P20-P27, P30-P37, P66, P70-P72, P94-P96, P100-P103, P120-P127, P130, P131	V <sub>DD</sub> = 4.5 to 5.5 V	15	40	90	k Ω
				20		500	k Ω

**Remark** Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note1</sup>	I <sub>DD1</sub>	5.0-MHz crystal oscillation operating mode ( $f_{xx} = 2.5$ MHz) <sup>Note2</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$ <sup>Note5</sup>		4.5	13.5	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <sup>Note6</sup>		0.7	2.1	mA
		5.0-MHz crystal oscillation operating mode ( $f_{xx} = 5.0$ MHz) <sup>Note3</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$ <sup>Note5</sup>		8.0	24.0	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <sup>Note6</sup>		0.9	2.7	mA
	I <sub>DD2</sub>	5.0-MHz crystal oscillation HALT mode ( $f_{xx} = 2.5$ MHz) <sup>Note2</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$ <sup>Note5</sup>		1.4	4.2	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <sup>Note6</sup>		0.5	1.5	mA
		5.0-MHz crystal oscillation HALT mode ( $f_{xx} = 5.0$ MHz) <sup>Note3</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$ <sup>Note5</sup>		1.6	4.8	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <sup>Note6</sup>		0.65	1.95	mA
	I <sub>DD3</sub>	32.768-kHz crystal oscillation operating mode <sup>Note4</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$		60	120	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		32	64	μA
	I <sub>DD4</sub>	32.768-kHz crystal oscillation operating mode <sup>Note4</sup>	$V_{DD} = 5.0\text{ V} \pm 10\%$		25	55	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		5	15	μA
I <sub>DD5</sub>	XT1 = $V_{DD}$ STOP mode Feedback resistor used	$V_{DD} = 5.0\text{ V} \pm 10\%$		1	30	μA	
		$V_{DD} = 3.0\text{ V} \pm 10\%$		0.5	10	μA	
I <sub>DD6</sub>	XT1 = $V_{DD}$ STOP mode Feedback resistor not used	$V_{DD} = 5.0\text{ V} \pm 10\%$		0.1	30	μA	
		$V_{DD} = 3.0\text{ V} \pm 10\%$		0.05	10	μA	

**Notes 1.** Not including  $AV_{REF0}$ ,  $AV_{REF1}$  and  $AV_{DD}$  currents or port currents (including current flowing into on-chip pull-up resistors).

2.  $f_{xx} = f_x/2$  operation (when oscillation mode selection register (OSMS) is set to 00H).
3.  $f_{xx} = f_x$  operation (when OSMS is set to 01H).
4. When the main system clock is stopped.
5. High-speed mode operation (when processor clock control register (PCC) is set to 00H).
6. Low-speed mode operation (when PCC is set to 04H).

**Remark**  $f_{xx}$  : Main system clock frequency ( $f_x$  or  $f_x/2$ )  
 $f_x$  : Main system clock oscillation frequency

AC Characteristics

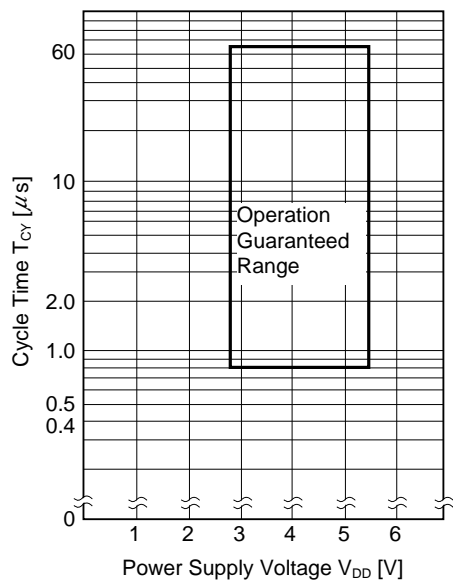
(1) Basic Operation (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	T <sub>CY</sub>	Operating on main system clock	f <sub>XX</sub> = f <sub>X</sub> /2 <sup>Note1</sup>	0.8		64	μs
			f <sub>XX</sub> = f <sub>X</sub> <sup>Note2</sup>	V <sub>DD</sub> = 3.5 to 5.5 V	0.4		32
		Operating on subsystem clock		0.8		32	μs
		Operating on subsystem clock		40	122	125	μs
TI00 input high-/low-level widths	t <sub>TIH00</sub> ,	V <sub>DD</sub> = 3.5 to 5.5 V		2f <sub>sam</sub> +0.1 <sup>Note3</sup>		μs	
	t <sub>TIL00</sub>			2f <sub>sam</sub> +0.2 <sup>Note3</sup>		μs	
TI01 input high-/low-level widths	t <sub>TIH01</sub> , t <sub>TIL01</sub>		10			μs	
TI1, TI2, TI5, TI6 input frequency	f <sub>TI1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V		0	4	MHz	
				0	275	kHz	
TI1, TI2, TI5, TI6 input high-/low-level widths	t <sub>TIH1</sub> , t <sub>TIL1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V		100		ns	
				1.8		μs	
Interrupt input high-/low-level widths	t <sub>INTH</sub> , t <sub>INTL</sub>	INTP0	V <sub>DD</sub> = 3.5 to 5.5 V		2f <sub>sam</sub> +0.1 <sup>Note3</sup>	μs	
					2f <sub>sam</sub> +0.2 <sup>Note3</sup>	μs	
		INTP1-INTP6		10		μs	
RESET low-level width	t <sub>RSL</sub>		10		μs		

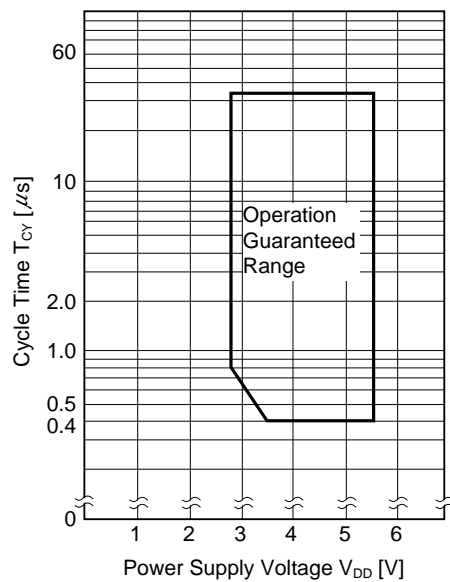
- Notes**
1. When oscillation mode selection register (OSMS) is set to 00H.
  2. When OSMS is set to 01H.
  3. f<sub>sam</sub> can be selected as f<sub>xx</sub>/2<sup>N</sup>, f<sub>xx</sub>/32, f<sub>xx</sub>/64 or f<sub>xx</sub>/128 (N = 0-4) by bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register.

**Remark** f<sub>xx</sub> : Main system clock frequency (f<sub>x</sub> or f<sub>x</sub>/2)  
 f<sub>x</sub> : Main system clock oscillation frequency

**T<sub>CY</sub> vs V<sub>DD</sub>**  
**(Main System Clock f<sub>xx</sub> = f<sub>x</sub>/2 Operation)**



**T<sub>CY</sub> vs V<sub>DD</sub>**  
**(Main System Clock f<sub>xx</sub> = f<sub>x</sub> Operation)**



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.85t <sub>cY</sub> - 50		ns
Address setup time	t <sub>ADS</sub>		0.85t <sub>cY</sub> - 50		ns
Address hold time	t <sub>ADH</sub>		50		ns
Address → Data input time	t <sub>ADD1</sub>			(2.85 + 2n) t <sub>cY</sub> - 80	ns
	t <sub>ADD2</sub>			(4 + 2n) t <sub>cY</sub> - 100	ns
RD ↓ → Data input time	t <sub>RDD1</sub>			(2 + 2n) t <sub>cY</sub> - 100	ns
	t <sub>RDD2</sub>			(2.85 + 2n) t <sub>cY</sub> - 100	ns
Read data hold time	t <sub>RDH</sub>		0		ns
RD low-level width	t <sub>RDL1</sub>		(2 + 2n) t <sub>cY</sub> - 60		ns
	t <sub>RDL2</sub>		(2.85 + 2n) t <sub>cY</sub> - 60		ns
RD ↓ → WAIT ↓ input time	t <sub>RDWT1</sub>			0.85t <sub>cY</sub> - 50	ns
	t <sub>RDWT2</sub>			2t <sub>cY</sub> - 60	ns
WR ↓ → WAIT ↓ input time	t <sub>WRWT</sub>			2t <sub>cY</sub> - 60	ns
WAIT low-level width	t <sub>WTL</sub>		(1.15 + 2n) t <sub>cY</sub>	(2 + 2n) t <sub>cY</sub>	ns
Write data setup time	t <sub>WDS</sub>		(2.85 + 2n) t <sub>cY</sub> - 100		ns
Write data hold time	t <sub>WDH</sub>		20		ns
WR low-level width	t <sub>WRL</sub>		(2.85 + 2n) t <sub>cY</sub> - 60		ns
ASTB ↓ → RD ↓ delay time	t <sub>ASTRD</sub>		25		ns
ASTB ↓ → WR ↓ delay time	t <sub>ASTWR</sub>		0.85t <sub>cY</sub> + 20		ns
In external fetch RD ↑ → ASTB ↑ delay time	t <sub>RDAST</sub>		0.85t <sub>cY</sub> - 10	1.15t <sub>cY</sub> + 20	ns
In external fetch RD ↑ → address hold time	t <sub>RDADH</sub>		0.85t <sub>cY</sub> - 50	1.15t <sub>cY</sub> + 50	ns
RD ↑ → write data output time	t <sub>RDWD</sub>		40		ns
WR ↓ → write data output time	t <sub>WRWD</sub>		0	50	ns
WR ↑ → address hold time	t <sub>WRADH</sub>		0.85t <sub>cY</sub>	1.15t <sub>cY</sub> + 40	ns
WAIT ↑ → RD ↑ delay time	t <sub>WTRD</sub>		1.15t <sub>cY</sub> + 40	3.15t <sub>cY</sub> + 40	ns
WAIT ↑ → WR ↑ delay time	t <sub>WTWR</sub>		1.15t <sub>cY</sub> + 30	3.15t <sub>cY</sub> + 30	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
  2. PCC2-PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
  3. t<sub>cY</sub> = T<sub>cY</sub>/4
  4. n indicates the number of waits.

(b) Except When MCS = 1, PCC2 to PCC0 = 000B (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		t <sub>cy</sub> - 80		ns
Address setup time	t <sub>ADS</sub>		t <sub>cy</sub> - 80		ns
Address hold time	t <sub>ADH</sub>		0.4t <sub>cy</sub> - 10		ns
Address → Data input time	t <sub>ADD1</sub>			(3 + 2n) t <sub>cy</sub> - 160	ns
	t <sub>ADD2</sub>			(4 + 2n) t <sub>cy</sub> - 200	ns
RD ↓ → Data input time	t <sub>RDD1</sub>			(1.4 + 2n) t <sub>cy</sub> - 70	ns
	t <sub>RDD2</sub>			(2.4 + 2n) t <sub>cy</sub> - 70	ns
Read data hold time	t <sub>RDH</sub>		0		ns
RD low-level width	t <sub>RDL1</sub>		(1.4 + 2n) t <sub>cy</sub> - 20		ns
	t <sub>RDL2</sub>		(2.4 + 2n) t <sub>cy</sub> - 20		ns
RD ↓ → WAIT ↓ input time	t <sub>RDWT1</sub>			t <sub>cy</sub> - 100	ns
	t <sub>RDWT2</sub>			2t <sub>cy</sub> - 100	ns
WR ↓ → WAIT ↓ input time	t <sub>WRWT</sub>			2t <sub>cy</sub> - 100	ns
WAIT low-level width	t <sub>WTL</sub>		(1 + 2n) t <sub>cy</sub>	(2 + 2n) t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		(2.4 + 2n) t <sub>cy</sub> - 60		ns
Write data hold time	t <sub>WDH</sub>		20		ns
WR low-level width	t <sub>WRL</sub>		(2.4 + 2n) t <sub>cy</sub> - 20		ns
ASTB ↓ → RD ↓ delay time	t <sub>ASTRD</sub>		0.4t <sub>cy</sub> - 30		ns
ASTB ↓ → WR ↓ delay time	t <sub>ASTWR</sub>		1.4t <sub>cy</sub> - 30		ns
In external fetch RD ↑ → ASTB ↑ delay time	t <sub>RDAST</sub>		t <sub>cy</sub> - 10	t <sub>cy</sub> + 20	ns
In external fetch RD ↑ → address hold time	t <sub>RDADH</sub>		t <sub>cy</sub> - 50	t <sub>cy</sub> + 50	ns
RD ↑ → write data output time	t <sub>RDWD</sub>		0.4t <sub>cy</sub> - 20		ns
WR ↓ → write data output time	t <sub>WRWD</sub>		0	60	ns
WR ↑ → address hold time	t <sub>WRADH</sub>		t <sub>cy</sub>	t <sub>cy</sub> + 60	ns
WAIT ↑ → RD ↑ delay time	t <sub>WTRD</sub>		0.6t <sub>cy</sub> + 180	2.6t <sub>cy</sub> + 180	ns
WAIT ↑ → WR ↑ delay time	t <sub>WTWR</sub>		0.6t <sub>cy</sub> + 120	2.6t <sub>cy</sub> + 120	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
  2. PCC2-PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
  3. t<sub>cy</sub> = T<sub>cy</sub>/4
  4. n indicates the number of waits.

(3) Serial Interface (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 2.7 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{\text{SCK0}}$ high-/low-level width	t <sub>KH1</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY1</sub> /2-50			ns
	t <sub>KL1</sub>		t <sub>KCY1</sub> /2-100			ns
SIO setup time (to $\overline{\text{SCK0}}$ ↑)	t <sub>SIK1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	100			ns
			150			ns
SIO hold time (from $\overline{\text{SCK0}}$ ↑)	t <sub>KS1</sub>		400			ns
$\overline{\text{SCK0}}$ ↓ → SO0 output delay time	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the  $\overline{\text{SCK0}}$ , SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY2</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{\text{SCK0}}$ high-/low-level width	t <sub>KH2</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
	t <sub>KL2</sub>		800			ns
SIO setup time (to $\overline{\text{SCK0}}$ ↑)	t <sub>SIK2</sub>		100			ns
SIO hold time (from $\overline{\text{SCK0}}$ ↑)	t <sub>KS2</sub>		400			ns
$\overline{\text{SCK0}}$ ↓ → SO0 output delay time	t <sub>KSO2</sub>	C = 100 pF <sup>Note</sup>			300	ns
$\overline{\text{SCK0}}$ rise, fall time	t <sub>R2</sub> , t <sub>F2</sub>				160	ns

**Note** C is the SO0 output line load capacitance.

(iii) SBI mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY3}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH3}}, t_{\text{KL3}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY3}}/2-50$			ns
			$t_{\text{KCY3}}/2-150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	$t_{\text{SIK3}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	$t_{\text{KSI3}}$		$t_{\text{KCY3}}/2$			ns
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	$t_{\text{KSO4}}$	R = 1 kΩ, C = 100 pF <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$		250	ns
				0		1000
$\overline{\text{SCK0}}$ ↑ → SB0, SB1 ↓	$t_{\text{KSB}}$		$t_{\text{KCY3}}$			ns
SB0, SB1 ↓ → $\overline{\text{SCK0}}$ ↓	$t_{\text{SBK}}$		$t_{\text{KCY3}}$			ns
SB0, SB1 high-level width	$t_{\text{SBH}}$		$t_{\text{KCY3}}$			ns
SB0, SB1 low-level width	$t_{\text{SBL}}$		$t_{\text{KCY3}}$			ns

**Note** R and C are the  $\overline{\text{SCK0}}$ , SB0, SB1 output line load resistance and load capacitance.

(iv) SBI mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY4}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH4}}, t_{\text{KL4}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
			1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	$t_{\text{SIK4}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	$t_{\text{KSI4}}$		$t_{\text{KCY4}}/2$			ns
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	$t_{\text{KSO4}}$	R = 1 kΩ, C = 100 pF <sup>Note</sup>	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$		300	ns
				0		1000
$\overline{\text{SCK0}}$ ↑ → SB0, SB1 ↓	$t_{\text{KSB}}$		$t_{\text{KCY4}}$			ns
SB0, SB1 ↓ → $\overline{\text{SCK0}}$ ↓	$t_{\text{SBK}}$		$t_{\text{KCY4}}$			ns
SB0, SB1 high-level width	$t_{\text{SBH}}$		$t_{\text{KCY4}}$			ns
SB0, SB1 low-level width	$t_{\text{SBL}}$		$t_{\text{KCY4}}$			ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R4}}, t_{\text{F4}}$				160	ns

**Note** R and C are the SB0, SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	$t_{\text{CY5}}$	R = 1 kΩ, C = 100 pF <sup>Note</sup>	1600			ns	
$\overline{\text{SCK0}}$ high-level width	$t_{\text{KH5}}$		$t_{\text{CY5}}/2-160$			ns	
$\overline{\text{SCK0}}$ low-level width	$t_{\text{KL5}}$		$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{CY5}}/2-50$			ns
				$t_{\text{CY5}}/2-100$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	$t_{\text{SIK5}}$		$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	$t_{\text{KSI5}}$			600			ns
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	$t_{\text{KSO5}}$		0		300	ns	

**Note** R and C are the  $\overline{\text{SCK0}}$ , SB0, SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	$t_{\text{CY6}}$		1600			ns	
$\overline{\text{SCK0}}$ high-level width	$t_{\text{KH6}}$		650			ns	
$\overline{\text{SCK0}}$ low-level width	$t_{\text{KL6}}$		800			ns	
SB0, SB1 setup time (to $\overline{\text{SCK0}}$ ↑)	$t_{\text{SIK6}}$		100			ns	
SB0, SB1 hold time (from $\overline{\text{SCK0}}$ ↑)	$t_{\text{KSI6}}$		$t_{\text{CY6}}/2$			ns	
$\overline{\text{SCK0}}$ ↓ → SB0, SB1 output delay time	$t_{\text{KSO6}}$	R = 1 kΩ,	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	0		300	ns
		C = 100 pF <sup>Note</sup>		0		500	ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R6}}, t_{\text{F6}}$				160	ns	

**Note** R and C are the SB0, SB1 output line load resistance and load capacitance.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ( $\overline{\text{SCK1}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY7}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH7}}, t_{\text{KL7}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY7}}/2-50$			ns
			$t_{\text{KCY7}}/2-100$			ns
S11 setup time (to $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK7}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
S11 hold time (from $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI7}}$		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	$t_{\text{KSO7}}$	$C = 100 \text{ pF}$ <sup>Note</sup>			300	ns

**Note** C is the  $\overline{\text{SCK1}}$ , SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK1}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY8}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH8}}, t_{\text{KL8}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
			800			ns
S11 setup time (to $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK8}}$		100			ns
S11 hold time (from $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI8}}$		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	$t_{\text{KSO8}}$	$C = 100 \text{ pF}$ <sup>Note</sup>			300	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{r8}}, t_{\text{f8}}$				160	ns

**Note** C is the SO1 output line load capacitance.

(iii) 3-wire serial I/O mode with automatic transmission/reception function ( $\overline{\text{SCK1}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY9}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH9}}$ ,	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY9}}/2-50$			ns
	$t_{\text{KL9}}$		$t_{\text{KCY9}}/2-100$			ns
SI1 setup time (to $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK9}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (from $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI9}}$		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	$t_{\text{KSO9}}$	$C = 100 \text{ pF}$ <sup>Note</sup>			300	ns
$\overline{\text{SCK1}}$ ↑ → STB ↑	$t_{\text{SBD}}$		$t_{\text{KCY9}}/2-100$		$t_{\text{KCY9}}/2+100$	ns
Strobe signal high-level width	$t_{\text{SBW}}$		$t_{\text{KCY9}}-30$		$t_{\text{KCY9}}+30$	ns
Busy signal setup time (to busy signal detection timing)	$t_{\text{BYS}}$		100			ns
Busy signal hold time (from busy signal detection timing)	$t_{\text{BYH}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
Busy inactive → $\overline{\text{SCK1}}$ ↓	$t_{\text{SPS}}$				$2t_{\text{KCY9}}$	ns

**Note** C is the  $\overline{\text{SCK1}}$ , SO1 output line load capacitance.

(iv) 3-wire serial I/O mode with automatic transmission/reception function ( $\overline{\text{SCK1}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY10}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	800			ns
			1600			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH10}}$ ,	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	400			ns
	$t_{\text{KL10}}$		800			ns
SI1 setup time (to $\overline{\text{SCK1}}$ ↑)	$t_{\text{SIK10}}$		100			ns
SI1 hold time (from $\overline{\text{SCK1}}$ ↑)	$t_{\text{KSI10}}$		400			ns
$\overline{\text{SCK1}}$ ↓ → SO1 output delay time	$t_{\text{KSO10}}$	$C = 100 \text{ pF}$ <sup>Note</sup>			300	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R10}}, t_{\text{F10}}$				160	ns

**Note** C is the SO1 output line load capacitance.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ( $\overline{\text{SCK2}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK2 cycle time	t <sub>KCY11</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
SCK2 high-/low-level width	t <sub>KH11</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY11</sub> /2-50			ns
	t <sub>KL11</sub>		t <sub>KCY11</sub> /2-100			ns
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t <sub>SIK11</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t <sub>KSI11</sub>		400			ns
SCK2 ↓ → SO2 output delay time	t <sub>KSO11</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the  $\overline{\text{SCK2}}$ , SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK2}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK2 cycle time	t <sub>KCY12</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
SCK2 high-/low-level width	t <sub>KH12</sub> ,	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
	t <sub>KL12</sub>		800			ns
SI2 setup time (to $\overline{\text{SCK2}}$ ↑)	t <sub>SIK12</sub>		100			ns
SI2 hold time (from $\overline{\text{SCK2}}$ ↑)	t <sub>KSI12</sub>		400			ns
$\overline{\text{SCK2}}$ ↓ → SO2 output delay time	t <sub>KSO12</sub>	C = 100 pF <sup>Note</sup>			300	ns
SCK2 rise, fall time	t <sub>R12</sub> ,				160	ns
	t <sub>F12</sub>					

**Note** C is the SO2 output line load capacitance.

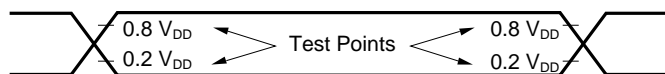
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			78125	bps
					39063	bps

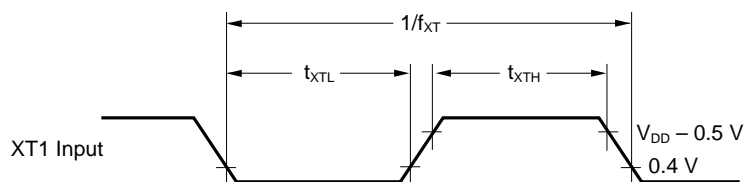
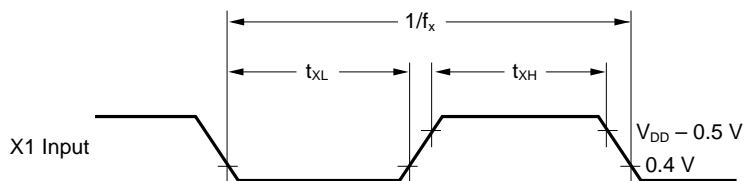
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t <sub>KCY13</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t <sub>KH13</sub> , t <sub>KL13</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V <sub>DD</sub> = 4.5 to 5.5 V			39063	bps
					19531	bps
ASCK rise, fall time	t <sub>R13</sub> , t <sub>F13</sub>				160	ns

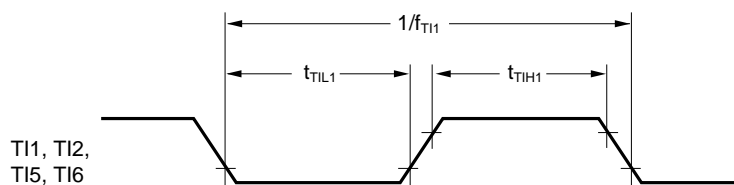
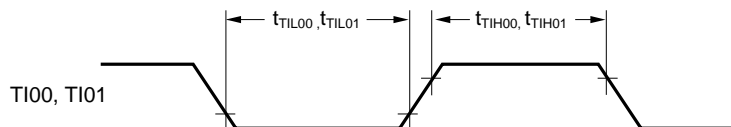
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

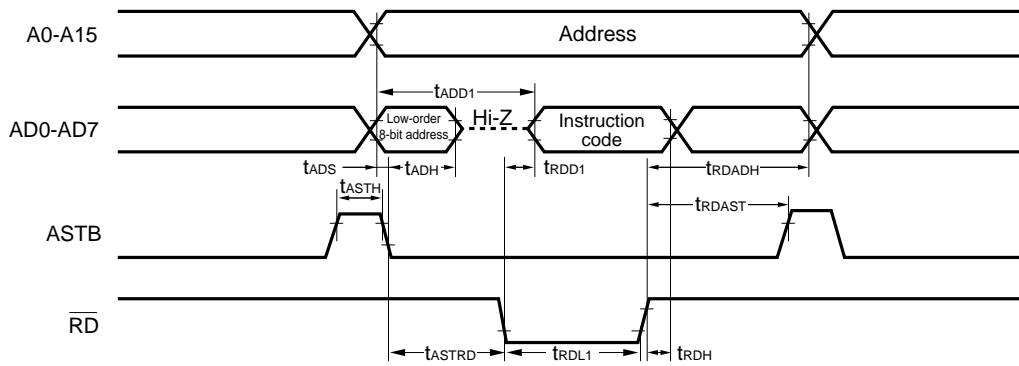


TI Timing

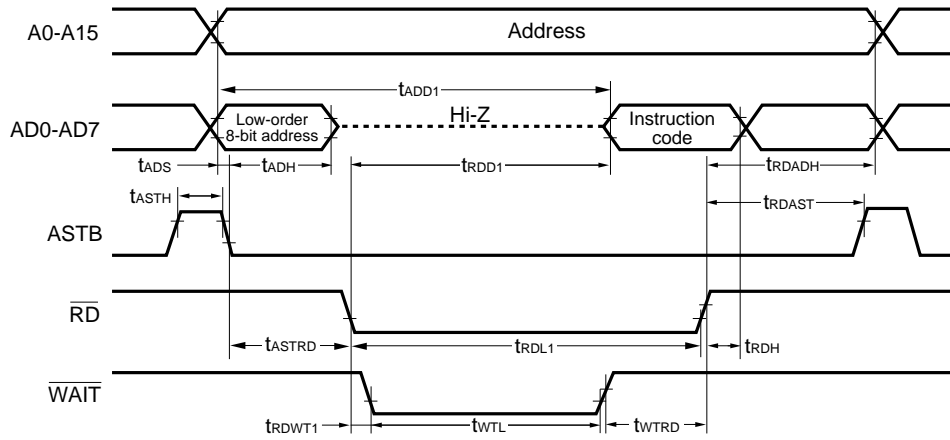


Read/Write Operation

External fetch (no wait):



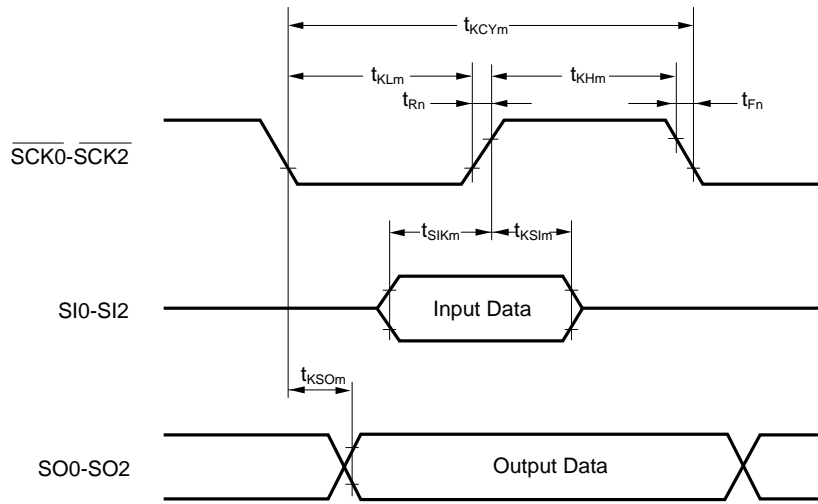
External fetch (wait insertion):





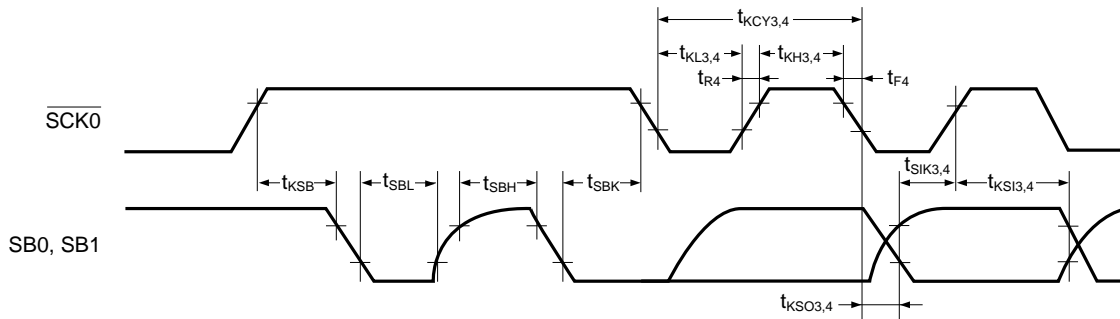
**Serial Transfer Timing**

**3-wire serial I/O mode:**

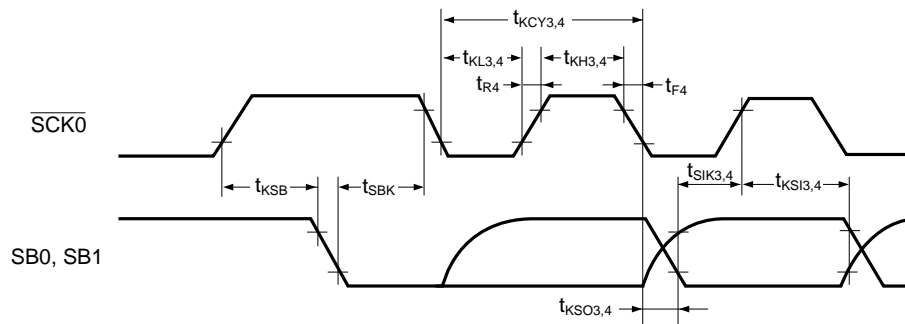


**Remark**  $m = 1, 2, 7, 8, 11, 12$   
 $n = 2, 8, 12$

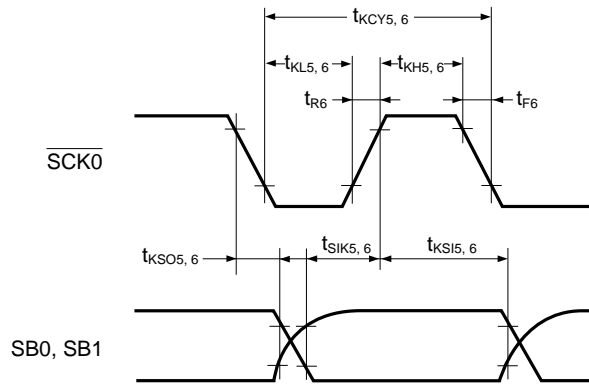
**SBI mode (bus release signal transfer):**



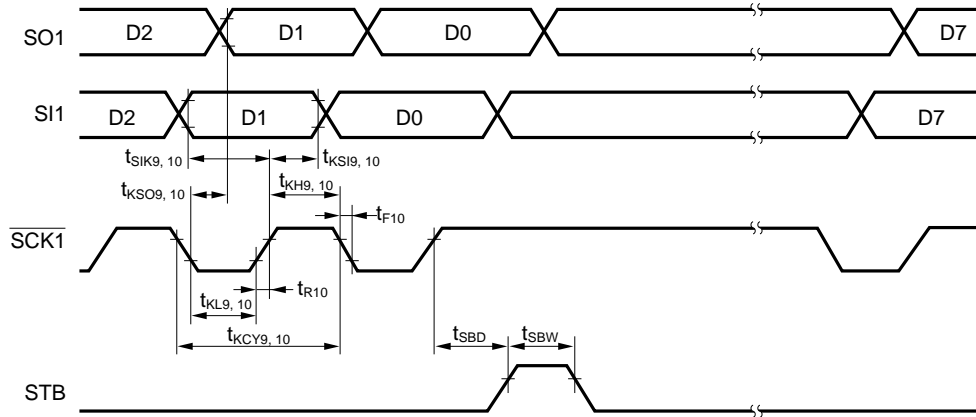
**SBI mode (command signal transfer):**



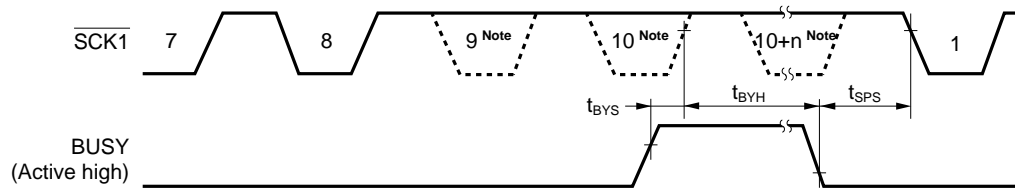
**2-wire serial I/O mode:**



**3-wire serial I/O mode with automatic transmission/reception function:**

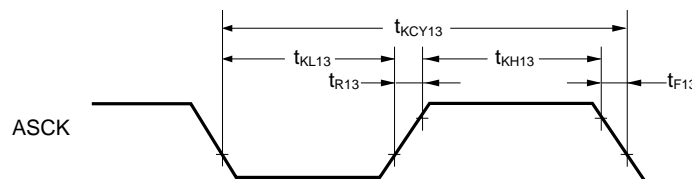


**3-wire serial I/O mode with automatic transmission/reception function (busy processing):**



**Note** The signal is not actually low here, but is represented in this way to show the timing.

**UART mode (external clock input):**



**A/D Converter Characteristics** ( $T_A = -40$  to  $+85$  °C,  $AV_{DD} = V_{DD} = 2.7$  to  $5.5$  V,  $AV_{SS} = V_{SS} = 0$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error <sup>Note</sup>		$2.7\text{ V} - AV_{REF0} - AV_{DD}$			0.6	%
Conversion time	$t_{CONV}$		19.1		200	μs
Sampling time	$t_{SAMP}$		$12/f_{xx}$			μs
Analog input voltage	$V_{IAN}$		$AV_{SS}$		$AV_{REF0}$	V
Reference voltage	$AV_{REF0}$		2.7		$AV_{DD}$	V
$AV_{REF0}-AV_{SS}$ resistance	$RA_{IREF0}$		4	14		kΩ

**Note** Excluding quantization error ( $\pm 1/2$  LSB). Shown as a percentage of the full scale value.

**Remark**  $f_{xx}$ : Main system clock frequency ( $f_x$  or  $f_x/2$ )

$f_x$ : Main system clock oscillation frequency

**D/A Converter Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V,  $AV_{SS} = V_{SS} = 0$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Total error		$R = 2\text{ M}\Omega$ <sup>Note1</sup>			1.2	%
		$R = 4\text{ M}\Omega$ <sup>Note1</sup>			0.8	%
		$R = 10\text{ M}\Omega$ <sup>Note1</sup>			0.6	%
Settling time		$C = 30\text{ pF}$ <sup>Note1</sup>	$4.5\text{ V} - AV_{REF1} - 5.5\text{ V}$		10	μs
			$2.7\text{ V} - AV_{REF1} < 4.5\text{ V}$		15	μs
Output resistor	$R_o$	<b>Note2</b>		10		kΩ
Analog reference voltage	$AV_{REF1}$		2.7		$V_{DD}$	V
$AV_{REF1}-AV_{SS}$ resistance	$RA_{IREF1}$	$DACS0, DACS1 = 55H$ <sup>Note2</sup>	4	8		kΩ

**Notes** 1. R and C are the D/A converter output pin load resistance and load capacitance.

2. Value for one D/A converter channel.

**Remark**  $DACS0, DACS1$ : D/A conversion value setting registers 0, 1.

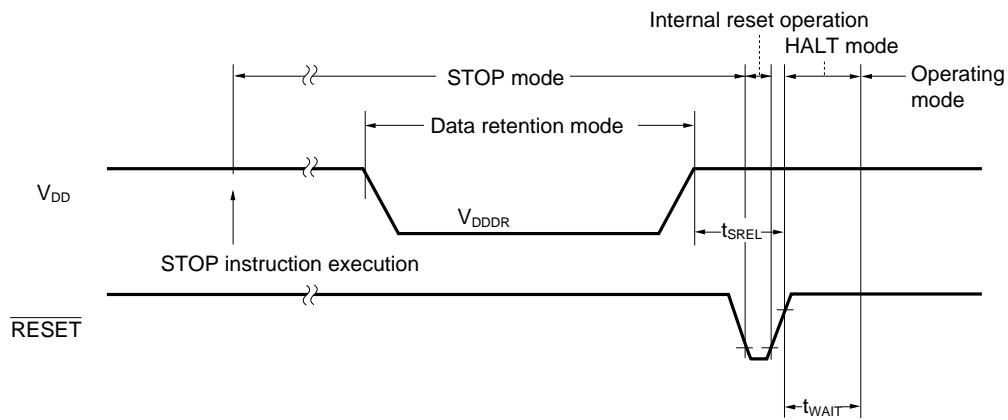
**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics** ( $T_A = -40$  to  $+85$  °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.8		5.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 1.8$ V When subsystem clock stopped and feedback resistor disconnected		0.1	10	μA
Release signal setup time	$t_{SREL}$		0			μs
Oscillation stabilization wait time	$t_{WAIT}$	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		Note		ms

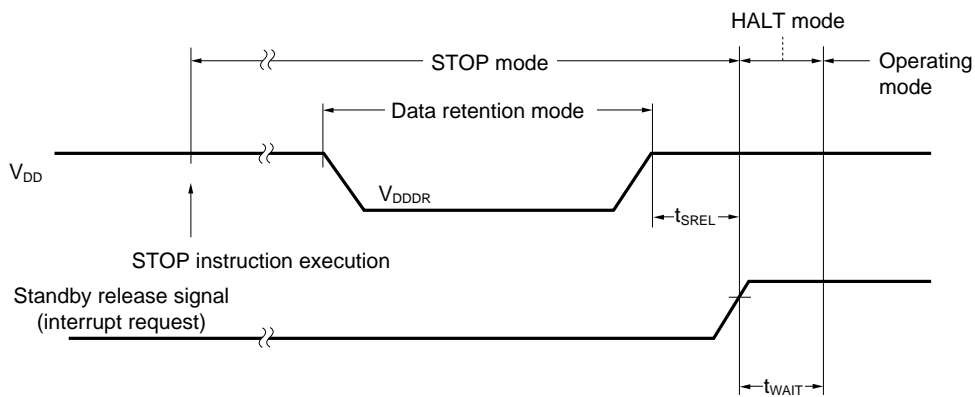
**Note**  $2^{12}/f_{xx}$  or  $2^{14}/f_{xx}-2^{17}/f_{xx}$  can be selected by bit 0-bit 2 (OSTS0-OSTS2) of oscillation stabilization time selection register (OSTS).

**Remark**  $f_{xx}$ : Main system clock frequency ( $f_x$  or  $f_x/2$ )  
 $f_x$ : Main system clock oscillation frequency

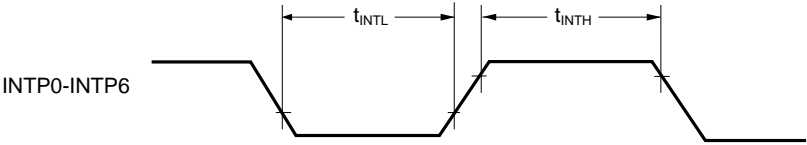
**Data Retention Timing (STOP mode released by  $\overline{RESET}$ )**



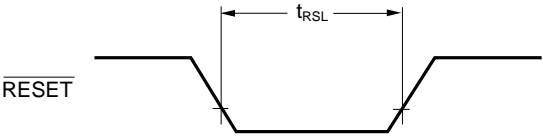
**Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)**



Interrupt Input Timing

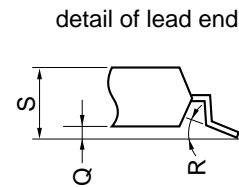
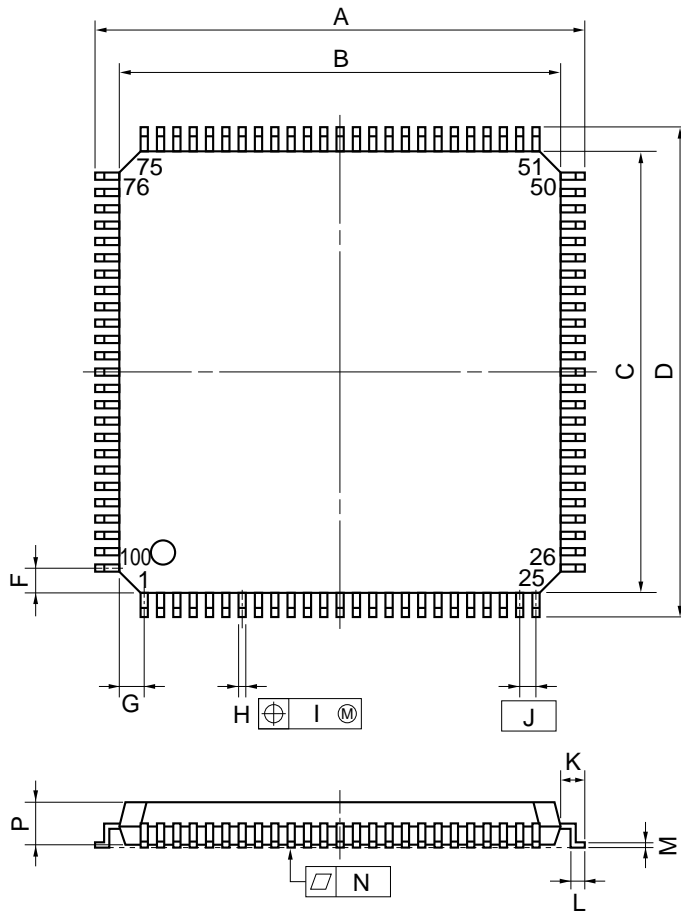


RESET Input Timing



12. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



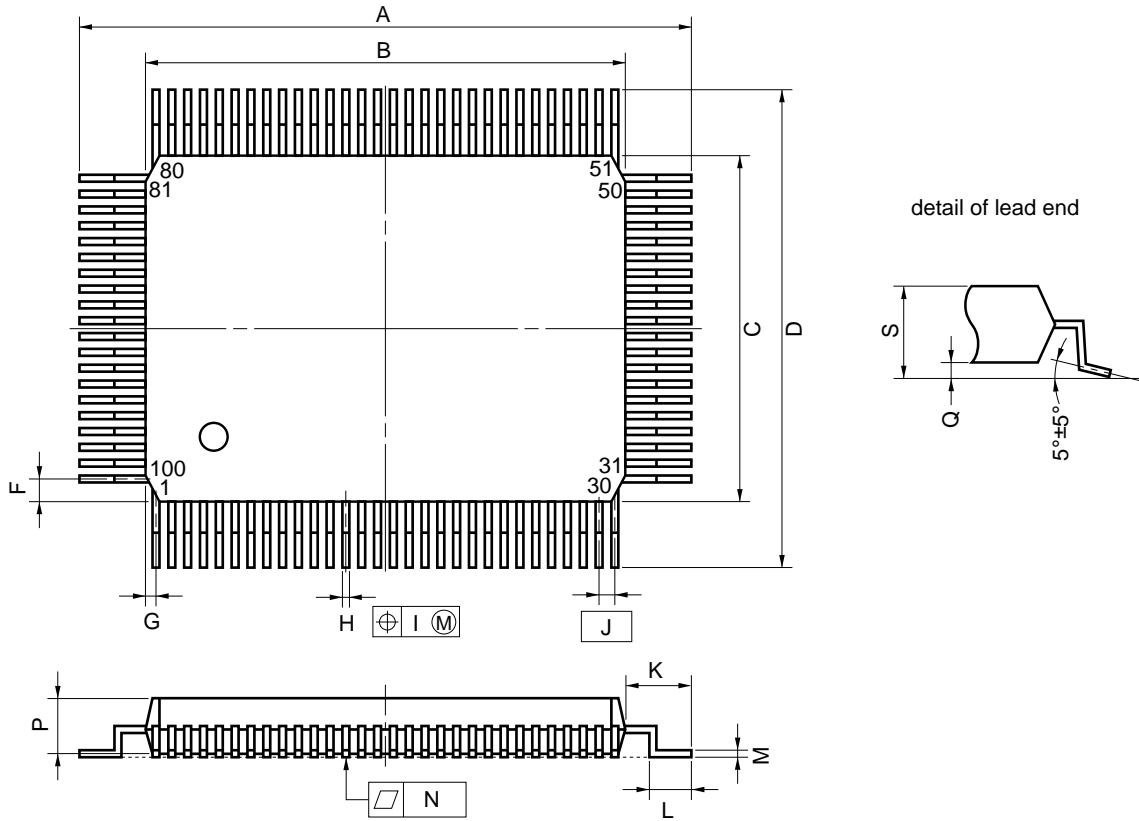
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	0.22 <sup>+0.05</sup> <sub>-0.04</sub>	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 <sup>+0.009</sup> <sub>-0.008</sub>
L	0.5±0.2	0.020 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>	0.007 <sup>+0.001</sup> <sub>-0.003</sub>
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

100 PIN PLASTIC QFP (14 × 20)



**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P100GF-65-3BA1-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

13. RECOMMENDED SOLDERING CONDITIONS



It is recommended that the μPD78070A be soldered under the following conditions. For details on the recommended soldering conditions, refer to information document "Semiconductor Device Mounting Technology Manual" (C10535E).

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 13-1. Soldering Conditions for Surface Mount Devices (1/2)

(1) μPD78070AGC-7EA: 100-pin plastic QFP (Fine pitch) (14 × 14 mm, resin thickness 1.45 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days <sup>Note</sup> (10 hours pre-baking is required at 125 °C afterwards) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-107-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days <sup>Note</sup> (10 hours pre-baking is required at 125 °C afterwards) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per device side)	—

**Note** Exposure limit before soldering after the dry pack package is opened. Storage conditions: 25 °C and relative humidity at 65% or less.

**Caution** Do not use different soldering methods together (except for partial heating method).

**Table 13-1. Soldering Conditions for Surface Mount Devices (2/2)**

**(2) μPD78070AGF-3BA: 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per device side)	—

**Caution Do not use different soldering methods together (except for partial heating method).**

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to support development of systems using the μPD78070AY.

### Language Processing Software

RA78K/0 <small>Note 1, 2, 3, 4</small>	Assembler package common to the 78K/0 series
CC78K/0 <small>Note 1, 2, 3, 4</small>	C compiler package common to the 78K/0 series
DF78078 <small>Note 1, 2, 3, 4</small>	Device file common to the μPD78078 subseries
CC78K/0-L <small>Note 1, 2, 3, 4</small>	C compiler library source file common to the 78K/0 series

### Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 series	
IE-78000-R-A <small>Note 8</small>	In-circuit emulator common to the 78K/0 series (for the integrated debugger)	★
IE-78000-R-BK	Break board common to the 78K/0 series	
IE-78078-R-EM	Emulation board common to the μPD78078 subseries	
EP-78064GC-R EP-78064GF-R	Emulation probe common to the μPD78064 subseries	
EV-9500GC-100	Adapter mounted on the user system board prepared for 100-pin plastic QFP	
EV-9200GF-100	Socket mounted on the user system board prepared for 100-pin plastic QFP	
SM78K0 <small>Note 5, 6, 7</small>	System simulator common to the 78K/0 series	
ID78K0 <small>Note 4, 5, 6, 7, 8</small>	Integrated debugger for the IE-78000-R-A	★
SD78K/0 <small>Note 1, 2</small>	Screen debugger for the IE-78000-R	
DF78078 <small>Note 1, 2, 5, 6, 7</small>	Device file common to the μPD78078 subseries	

### Real-Time OS

RX78K/0 <small>Note 1, 2, 3, 4</small>	Real-time OS used for the 78K/0 series
MX78K0 <small>Note 1, 2, 3, 4</small>	OS used for the 78K/0 series

**Notes** 1. Based on PC-9800 series (MS-DOS™)

2. Based on IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS™)

3. Based on HP9000 series 300™ (HP-UX™)

4. Based on HP9000 series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)

5. Based on PC-9800 series (MS-DOS + Windows™)

6. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)

7. Based on NEWS™ (NEWS-OS™)

8. Under development

**Remarks** 1. Please refer to the **78K/0 Series Selection Guide (IF-1185)** for information on third party development tools.

2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0 and RX78K/0 in combination with the DF78078.

**Fuzzy Inference Development Support System**

FE9000 <sup>Note1</sup> /FE9200 <sup>Note2</sup>	Fuzzy knowledge data creation tool
FT9080 <sup>Note1</sup> /FT9085 <sup>Note3</sup>	Translator
FI78K0 <sup>Note 1, 3</sup>	Fuzzy inference module
FD78K0 <sup>Note 1, 3</sup>	Fuzzy inference debugger

**Notes** 1. Based on PC-9800 series (MS-DOS)

2. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)

3. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS)

**Remark** Please refer to the **78K/0 Series Selection Guide (IF-1185)** for information on third party development tools.

## APPENDIX B. RELATED DOCUMENTS

## Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD78070A, 78070AY User's Manual	IEU-907	U10200E
78K/0 Series User's Manual—Instructions	IEU-849	IEU-1372
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78070AY Special Function Register Table	U10133J	—

## Documents Related to Development Tools

Document Name	Document No.		
	Japanese	English	
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note know-how	Programming	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		U10775J	EEU-1504
EP-78064		EEU-934	EEU-1522
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External parts user open interface specification	U10092J	U10092E
SD78K/0 Screen Debugger	Introduction	EEU-852	—
PC-9800 Series (MS-DOS) Based	Reference	U10952J	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Based	Reference	EEU-993	EEU-1413

**Caution** The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

**Documents Related to Embedded Software (User's Manual)**

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
78K/0 Series OS MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System	Fuzzy Inference Debugger	EEU-921	EEU-1458

**Other Documents**

Document Name		Document No.	
		Japanese	English
Package Manual		IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
NEC Semiconductor Device Quality Grades		IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System		IEM-5068	—
Electrostatic Discharge (ESD) Test		MEM-539	—
Semiconductor Device Quality Assurance Guide		MEI-603	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –		MEI-604	—

**Caution** The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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NEC devices are classified into the following three quality grades:

“Standard”, “Special”, and “Specific”. The Specific quality grade applies only to devices developed based on a customer designated “quality assurance program” for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in “Standard” unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.