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RENESAS

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MOS INTEGRATED CIRCUIT

μPD78E9860, 78E9861

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD78E9860 and μPD78E9861 are μPD789860, 789861 Subseries products in the 78K/0S Series.

The μPD78E9860 and μPD78E9861 incorporate EEPROM™ in place of the internal ROM of the μPD789860 and μPD789861, respectively.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789860, 789861 Subseries User's Manual: To be prepared
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Pin compatible with mask ROM product (except V_{PP} pin)
- On-chip EEPROM as program memory: 4 KB
- On-chip EEPROM that can be read/written by program in RAM area: 32 bytes
- On-chip high-speed RAM: 256 bytes
- System clock oscillator
  - μPD78E9860: Crystal/ceramic oscillator
  - μPD78E9861: RC oscillator (externally attached resistor and capacitor)
- Minimum instruction execution time
  - μPD78E9860: 0.4 μs/1.6 μs (@ f_X = 5.0 MHz operation)
  - μPD78E9861: 2.0 μs/8.0 μs (@ f_{CC} = 1.0 MHz operation)
- I/O ports: 14
- Timer: 3 channels
  - 8-bit timer/event counter: 1 channel
  - 8-bit timer: 1 channel
  - Watchdog timer: 1 channel
- On-chip power-on-clear circuit
- On-chip bit sequential buffer
- Power supply voltage: V_{DD} = 1.8 to 3.6 V

APPLICATIONS

Keyless entry and other automotive electrical equipment

In this preliminary product information, the oscillation frequency of the crystal/ceramic oscillator (μPD78E9860) is described as f_X and the oscillation frequency of the RC oscillator (μPD78E9861) is described as f_{CC}.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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Date Published May 2000 NS CP(K)

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD78E9860MC-5A4	20-pin plastic SSOP (7.62 mm (300))
μPD78E9861MC-5A4	20-pin plastic SSOP (7.62 mm (300))

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production (solid box)

Products under development (dashed box)

Y Subseries products support SMB.

78K0/S Series

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789026 with added subsystem clock
42-/44-pin	μPD789026	μPD789014 with enhanced timer, increased ROM, RAM capacity
28-pin	μPD789014	On-chip UART and capable of low voltage (1.8 V) operation

Small-scale package, general-purpose applications and A/D converter

44-pin	μPD789177	μPD789177Y	μPD789167 with enhanced A/D converter
44-pin	μPD789167	μPD789167Y	μPD789104A with enhanced timer
30-pin	μPD789156		μPD789146 with enhanced A/D converter
30-pin	μPD789146		μPD789104A with added EEPROM
30-pin	μPD789134A		μPD789124A with enhanced A/D converter
30-pin	μPD789124A		RC oscillation version of the μPD789104A
30-pin	μPD789114A		μPD789104A with enhanced A/D converter
30-pin	μPD789104A		μPD789026 with added A/D converter and multiplier

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART

LCD Drive

80-pin	μPD789417A	μPD789407A with enhanced A/D converter
80-pin	μPD789407A	μPD789456 with enhanced I/O
64-pin	μPD789456	μPD789446 with enhanced A/D converter
64-pin	μPD789446	μPD789426 with enhanced display output
64-pin	μPD789436	μPD789426 with enhanced A/D converter
64-pin	μPD789426	μPD789306 with added A/D converter
64-pin	μPD789316	RC oscillation version of the μPD789306
64-pin	μPD789306	Basic Subseries for LCD drive

Dot LCD Drive

144-pin	μPD789835	Segment/common outputs: 96
88-pin	μPD789830	Segments: 40, commons: 16

ASSP

64-pin	μPD789467	μPD789327 with added A/D converter
64-pin	μPD789327	For remote controller, on-chip LCD controller/driver
44-pin	μPD789800	For PC keyboard, on-chip USB function
44-pin	μPD789840	For keypad, on-chip POC
20-pin	μPD789861	RC oscillation version of the μPD789860
20-pin	μPD789860	For keyless entry, on-chip POC and key return circuit

The major functional differences among the subseries are listed below.

Subseries Name	Function	ROM Capacity	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART: 1 ch)	34	1.8 V	—
	μPD789026	4 K to 16 K			—							
	μPD789014	2 K to 4 K	2 ch	—						22		
Small-scale package, general-purpose applications and A/D function	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch		—	8 ch	1 ch (UART: 1 ch)	31		—
	μPD789167						8 ch	—				
	μPD789156	8 K to 16 K	1 ch		—		—	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	—				
	μPD789134A	2 K to 8 K					—	4 ch				RC oscillation version
	μPD789124A						4 ch	—				
	μPD789114A						—	4 ch				—
	μPD789104A						4 ch	—				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	—	1 ch (UART: 1 ch)	30	4.0 V	—
LCD drive	μPD789417A	12 K to 24 K	3 ch	1 ch	1 ch	1 ch	—	7 ch	1 ch (UART: 1 ch)	43	1.8 V	—
	μPD789407A						7 ch	—				
	μPD789456	12 K to 16 K	2 ch				—	6 ch		30		
	μPD789446						6 ch	—				
	μPD789436						—	6 ch		40		
	μPD789426						6 ch	—				
	μPD789316	8 K to 16 K					—		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											—
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	—	1 ch	1 ch	2 ch	—	1 ch	27	1.8 V	—
	μPD789830	24 K	1 ch	1 ch			—		1 ch (UART: 1 ch)	30	2.7 V	
ASSP	μPD789467	4 K to 24 K	2 ch	—	1 ch	1 ch	1 ch	—	—	18	1.8 V	On-chip LCD
	μPD789327		3 ch				—		1 ch			
	μPD789800	8 K	2 ch		—	1 ch	—		2 ch (USB: 1 ch)	31	4.0 V	—
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					—		—	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

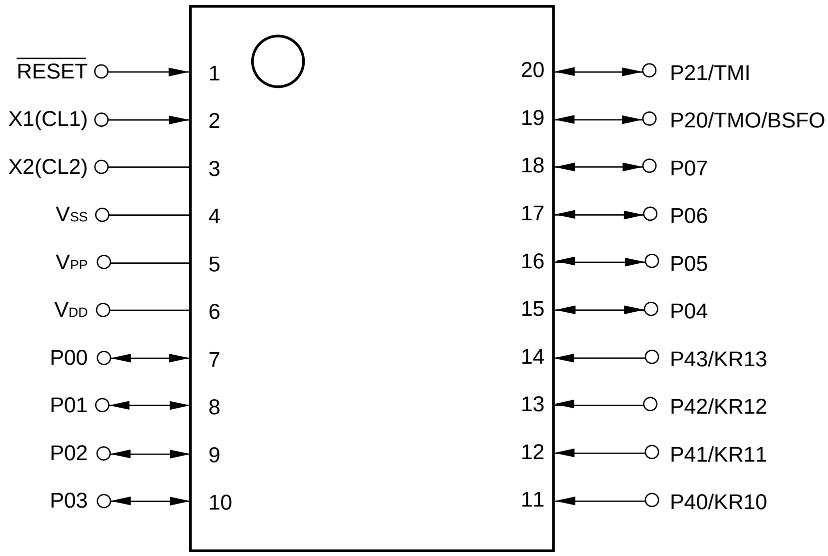
OVERVIEW OF FUNCTIONS

Item \ Part Number			μPD78E9860	μPD78E9861
Internal memory	Program memory	EEPROM	4 KB	
	Data memory	High-speed RAM	128 bytes	
		EEPROM	32 bytes	
Oscillator			Ceramic/crystal oscillator	RC oscillator
Minimum instruction execution time			0.4 μs/1.6 μs (@ f_X = 5.0 MHz operation)	2.0 μs/8.0 μs (@ f_{CC} = 1.0 MHz operation)
General-purpose registers			8 bits × 8 registers	
Instruction set			• 16-bit operation	
			• Bit manipulation (set, reset, test) etc.	
I/O ports			Total: 14 CMOS I/O: 10 CMOS input: 4	
Timer			• 8-bit timer/event counter: 1 channel • 8-bit timer: 1 channel • Watchdog timer: 1 channel	
Power-on-clear circuit	POC circuit		Generates internal reset signal according to comparison of detection voltage to power supply voltage	
	LVI circuit		Generates interrupt request signal according to comparison of detection voltage to power supply voltage	
Bit sequence buffer			8 bits × 8 bits = 16 bits	
Key return function			Generates key return signal according to falling edge detection	
Vectored interrupt sources	Maskable		Internal: 5	
	Non-maskable		Internal: 1, External: 1	
Power supply voltage			V_{DD} = 1.8 to 3.6 V	
Operating ambient temperature			T_A = –40 to +85°C	
Package			20-pin plastic SSOP (7.62 mm (300))	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

★ • 20-pin plastic SSOP (7.62 mm (300))
μPD78E9860MC-5A4
μPD78E9861MC-5A4

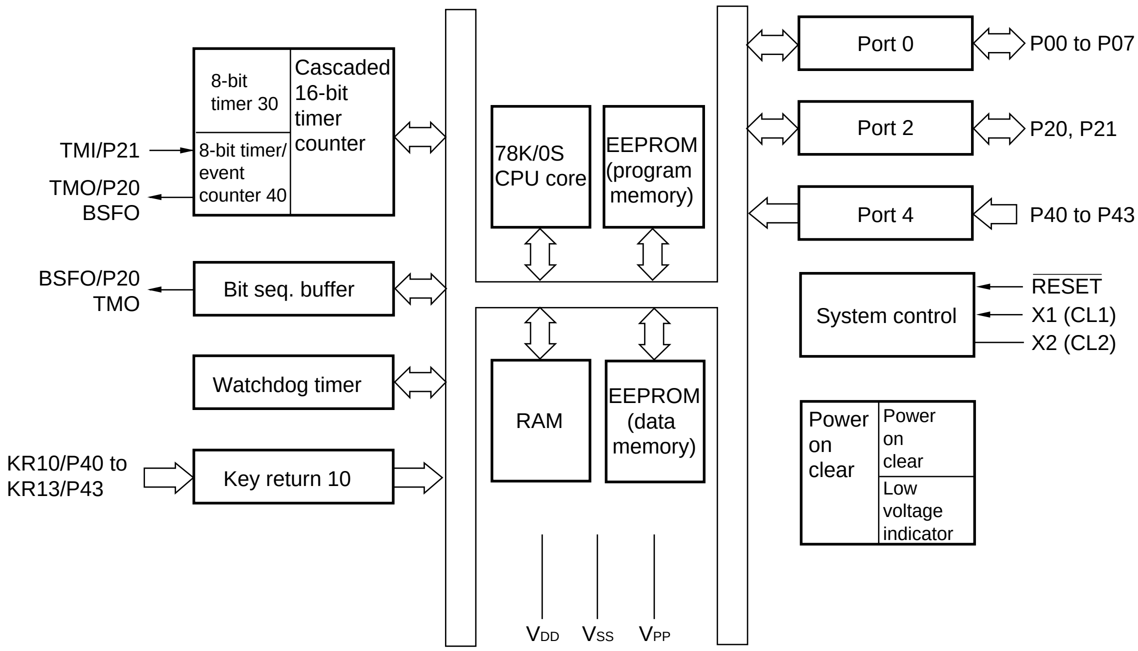


Caution Connect the V_{PP} pin directly to V_{SS}.

Remark Pin connections in parentheses apply to the μPD78E9861.

BSFO:	Bit Sequential Buffer Output	TMI:	Timer Input
CL1, CL2:	RC Oscillator	TMO:	Timer Output
KR10 to KR13:	Key Return	V_{DD}:	Power Supply
P00 to P07:	Port 0	V_{PP}:	Programming Power Supply
P20, P21:	Port 2	V_{SS}:	Ground
P40 to P43:	Port 4	X1, X2:	Crystal/Ceramic Oscillator
$\overline{\text{RESET}}$:	Reset		

2. BLOCK DIAGRAM



Remark Items in parentheses apply to the μPD78E9861.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	Input	—
P20	I/O	Port 2 2-bit I/O port Input/output can be specified in 1-bit units.	Input	TMO/BSFO
P21				TM1
P40 to P43	Input	Port 4 4-bit input-only port	Input	KR10 to KR13

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
TMI	Input	8-bit timer (TM40) input	Input	P21
TMO	Output	8-bit timer (TM40) output	Input	P20/BSFO
BSFO	Output	Bit sequential buffer (BSF10) output	Input	P20/TMO
KR10 to KR13	Input	Key return input	Input	P40 to P43
X1 Note 1	Input	Connecting ceramic/crystal resonator for system clock oscillation	—	—
X2 Note 1	—		—	—
CL1 Note 2	Input	Connecting resistor (R) and capacitor (C) for system clock oscillation	—	—
CL2 Note 2	—		—	—
$\overline{\text{RESET}}$	Input	System reset input	Input	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
V_{PP}	—	EEPROM programming mode setting. High-voltage application during programming write/verify. In normal operation mode, connect directly to V_{SS}.	—	—

Notes 1. μPD78E9860 only.

2. μPD78E9861 only.

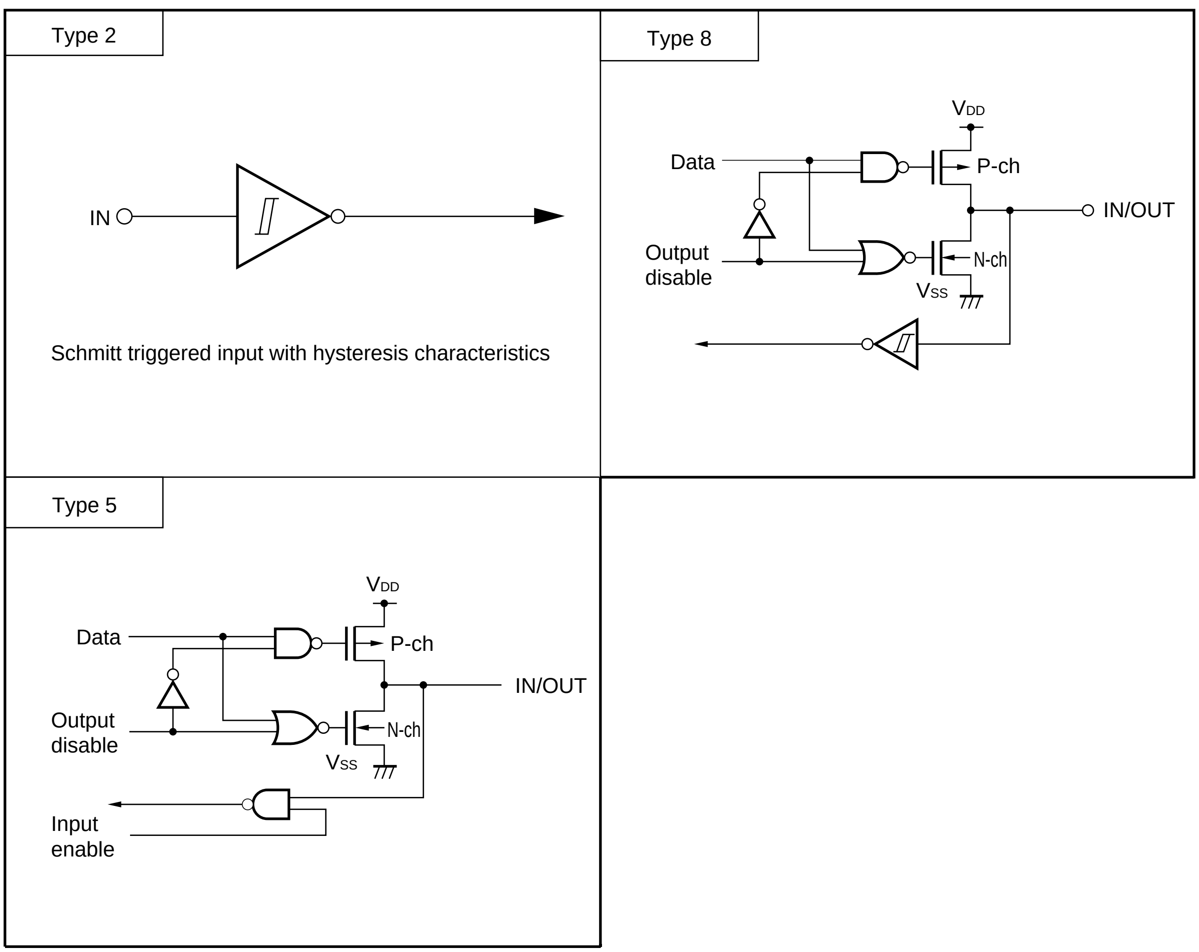
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type for each pin and recommended connections of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits and Recommended Connection of Unused Pins

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P20/TMO/BSFO	8		
P21/TMI			
P40/KR10 to P43/KR13	2		Connect directly to V_{DD} or V_{SS}.
$\overline{\text{RESET}}$			—
V_{PP}	—	—	Connect directly to V_{SS}.

Figure 3-1. Pin Input/Output Circuits

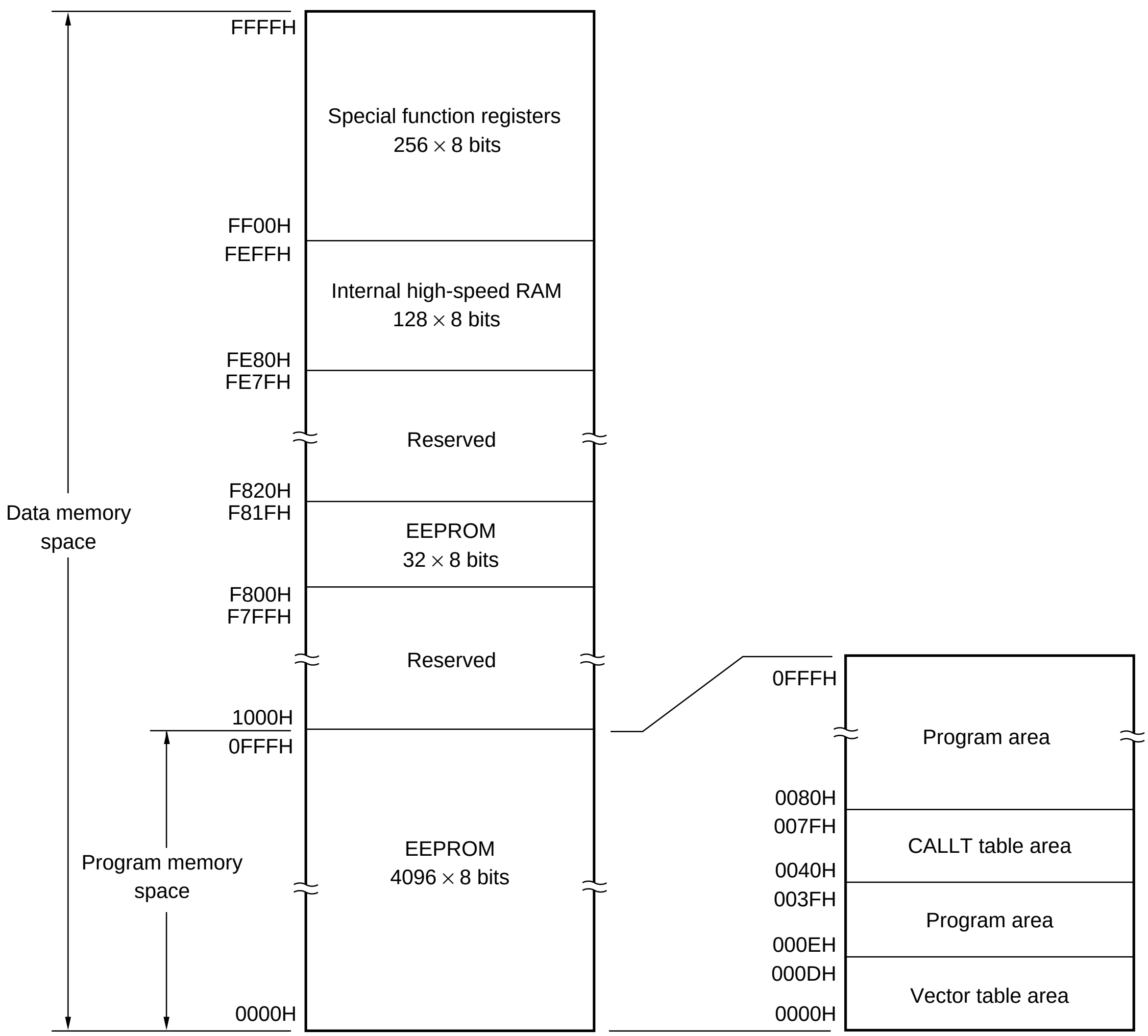


4. CPU ARCHITECTURE

4.1 Memory Space

The μPD78E9860 and μPD78E9861 can each access a 64 KB memory space. Figure 4-1 shows the memory map.

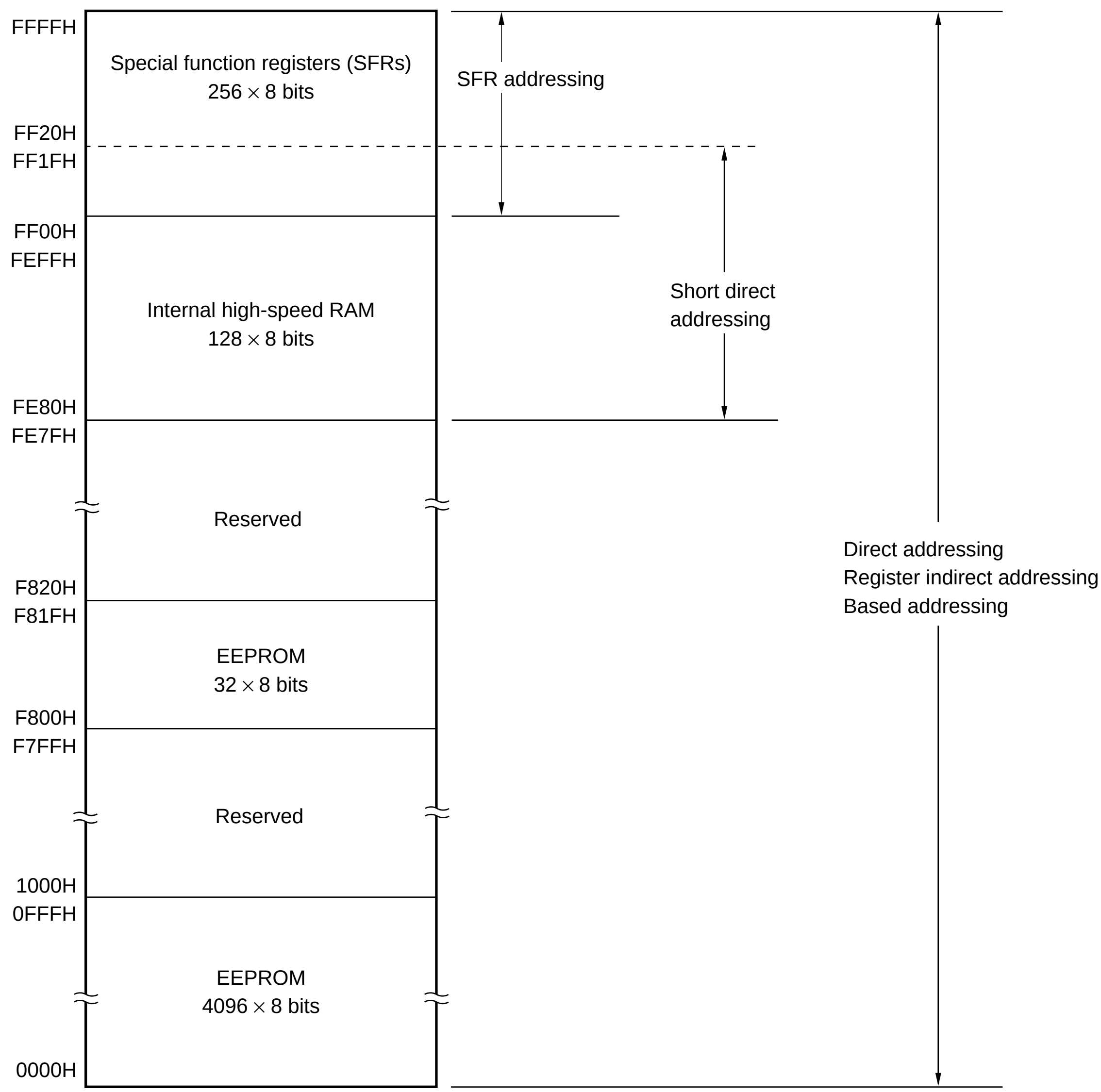
Figure 4-1. Memory Map



4.2 Data Memory Addressing

The μPD78E9860 and μPD78E9861 provide ample addressing modes that take into account the manipulation of memory. Addressing peculiar to the special function registers (SFRs) and other functions is possible in on-chip data memory areas (FE80H to FFFFH) in particular. Figure 4-2 shows data memory addressing.

Figure 4-2. Data Memory Addressing



4.3 Processor Registers

4.3.1 Control registers

(1) Program counter (PC)

The program counter is a 16-bit register that maintains address information about the program to be executed next.

Figure 4-3. Configuration of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register that shows the status of the CPU in terms of the results of instruction execution.

Figure 4-4. Configuration of Program Status Word

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

(a) Interrupt enable flag (IE)

The interrupt enable flag is a flag that controls CPU interrupt request acknowledgement operations.

(b) Zero flag (Z)

The zero flag is a flag that is set (1) when the result of an operation is zero and that is reset (0) otherwise.

(c) Auxiliary carry flag (AC)

The auxiliary carry flag is a flag that is set (1) when there is a carry from bit 3 or a borrow to bit 3 as a result of an operation and that is reset (0) otherwise.

(d) Carry flag (CY)

The carry flag is a flag that stores an overflow or underflow when an addition or subtraction instruction is executed.

(3) Stack pointer (SP)

The stack pointer is a 16-bit register that maintains the starting address of the stack area of memory. Only the internal high-speed RAM area (FE80H to FEFFH) can be set as the stack area.

Figure 4-5. Configuration of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Caution Because stack pointer contents become undefined when $\overline{\text{RESET}}$ input, be sure to initialize the SP before executing an instruction.

4.3.2 General-purpose registers

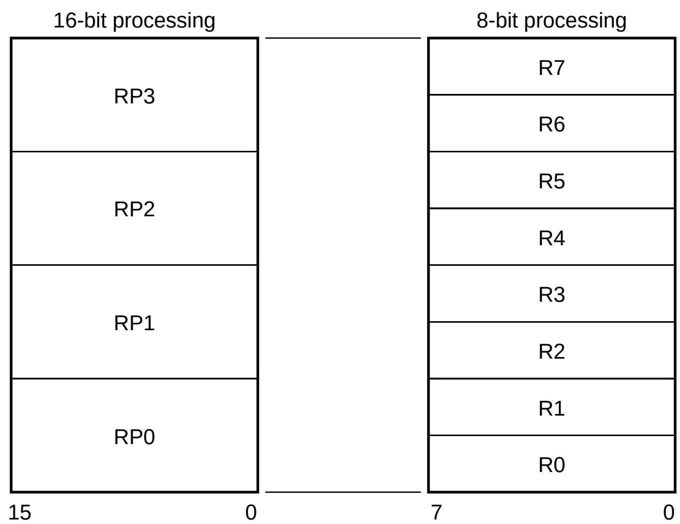
The general-purpose registers consist of eight 8-bit registers (X, A, C, B, E, D, L, H).

Besides each register being usable as an 8-bit register, it is possible to pair two 8-bit registers and use them as a 16-bit register (AX, BC, DE, HL).

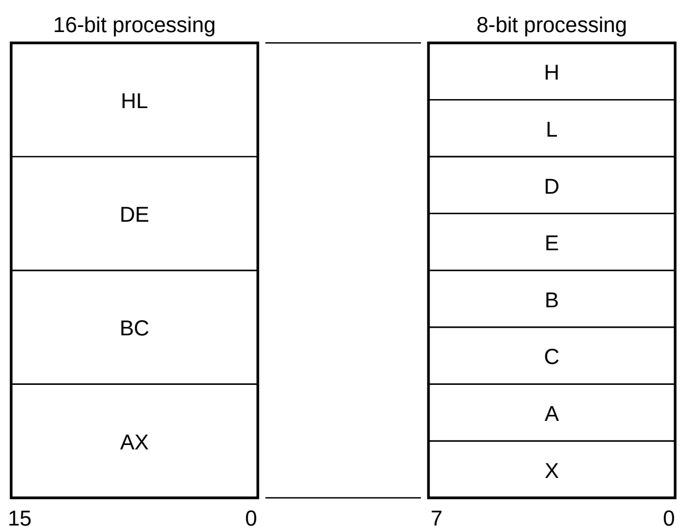
Moreover, in addition to function names (X, A, C, B, E, D, L, H, AX, BC, DE, HL), general-purpose registers can also be described using absolute names (R0 to R7 and RP0 to RP3).

Figure 4-6. Configuration of General-Purpose Registers

(a) Absolute names



(b) Function names



4.3.3 Special function registers (SFRs)

The special function registers are registers such as peripheral hardware mode registers and control registers that have special functions. They are mapped to the 256-byte space from FF00H to FFFFH.

Note that bits whose names are reserved words in the RA78K/0S or defined in the header file sfrbit.h in the CC78K0S have their bit number encircled in each register format. Refer to each register format in **6. PERIPHERAL HARDWARE FUNCTIONS**.

Table 4-1. List of Special Function Registers

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Unit for Manipulation			After Reset
				1 bit	8 bits	16 bits	
FF00H	Port 0	P0	R/W	√	√	—	00H
FF02H	Port 2	P2		√	√	—	
FF04H	Port 4	P4	R	√	√	—	
FF10H	Bit sequential buffer 10 data register L	BSFRL10	W	—	√	√ Note 1	Undefined
FF11H	Bit sequential buffer 10 data register H	BSFRH10		—	√		
FF20H	Port mode register 0	PM0	R/W	√	√	—	FFH
FF22H	Port mode register 2	PM2		√	√	—	
★ FF42H	Timer clock select register 2	TCL2		—	√	—	00H
FF50H	8-bit timer compare register 30	CR30	W	—	√	—	Undefined
FF51H	8-bit timer counter 30	TM30	R	—	√	—	00H
FF52H	8-bit timer mode control register 30	TMC30	R/W	√	√	—	
FF53H	8-bit timer compare register 40	CR40	W	—	√	—	Undefined
FF54H	8-bit compare register H40	CRH40		—	√	—	
FF55H	8-bit timer counter 40	TM40	R	—	√	—	00H
FF56H	8-bit timer mode control register 40	TMC40	R/W	√	√	—	
FF57H	Carrier generator output control register 40	TCA40	W	—	√	—	
FF60H	Bit sequential buffer output control register 10	BSFC10	R/W	√	√	—	
FFD8H	EEPROM write control register 10	EEWC10		√	√	—	08H
FFDDH	Power-on-clear register 1	POCF1		√	√	—	00H Note 2
FFDEH	Low-voltage detection register 1	LVIF1		√	√	—	00H
FFDFH	Low-voltage detection level selection register 1	LVIS1		√	√	—	
FFE0H	Interrupt request flag register 0	IF0		√	√	—	
FFE4H	Interrupt mask flag register 0	MK0		√	√	—	FFH
FFF9H	Watchdog timer mode register	WDTM		√	√	—	00H
FFFAH	Oscillation stabilization time selection register Note 3	OSTS		—	√	—	04H
FFFBH	Processor clock control register	PCC		√	√	—	02H

Notes 1. Specify address FF10H directly for 16-bit access.

2. This value is 04H only after a power-on-clear reset.

3. μPD78E9860 only.

5. EEPROM (DATA MEMORY)

5.1 EEPROM Functions

Besides internal high-speed RAM, the μPD78E9860 and μPD78E9861 have 32 × 8 bits of electrically erasable PROM (EEPROM) on-chip as data memory and 4096 × 8 bits of EEPROM as program memory.

This section describes the EEPROM used as data memory (for EEPROM used as program memory, refer to **10. EEPROM (PROGRAM MEMORY)**).

Unlike normal RAM, EEPROM can maintain its contents even if its power supply is cut. In addition, unlike EPROM, its electrical contents can be erased without using ultraviolet rays.

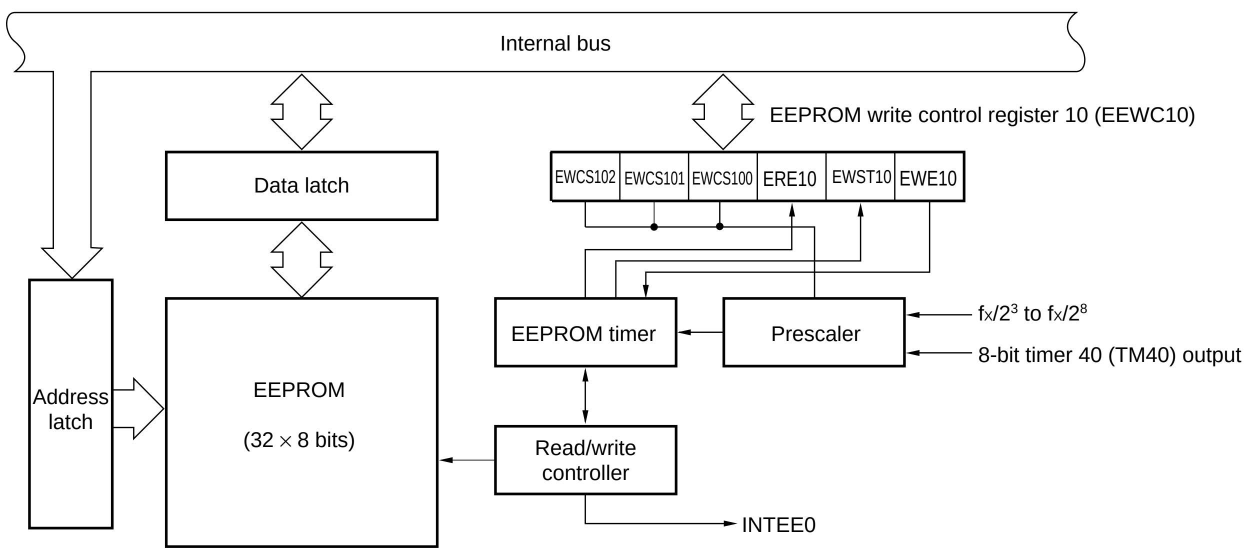
EEPROM operations are performed using 8-bit memory manipulation instructions.

5.2 EEPROM Configuration

EEPROM consists of the EEPROM itself and a control section.

The control section consists of EEPROM write control register 10 (EEWC10) which controls EEPROM writing and a part that detects the termination of writing and generates an interrupt request signal (INTEE0).

Figure 5-1. EEPROM Block Diagram



5.3 Register That Controls EEPROM

EEPROM is controlled by EEPROM write control register 10 (EEWC10).

EEWC10 is the register that sets the EEPROM count clock selection, and EEPROM write control.

Set EEWC10 using 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 08H.

Figure 5-2 shows the format of EEPROM write control register 10. Tables 5-1 and 5-2 show EEPROM write times.

Figure 5-2. Format of EEPROM Write Control Register 10

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
EEWC10	0	EWCS102	EWCS101	EWCS100	1	ERE10	EWST10	EWE10	FFD8H	08H	R/W[Note]

EWCS102	EWCS101	EWCS100	EEPROM timer count clock selection	
			When operating at f_X = 5.0 MHz	When operating at f_{CC} = 1.0 MHz
0	0	0	$f_X/2^3$ (625 kHz)	$f_{CC}/2^3$ (125 kHz)
0	0	1	$f_X/2^4$ (313 kHz)	$f_{CC}/2^4$ (62.5 kHz)
0	1	0	$f_X/2^5$ (156 kHz)	$f_{CC}/2^5$ (31.3 kHz)
0	1	1	$f_X/2^6$ (78.1 kHz)	$f_{CC}/2^6$ (15.6 kHz)
1	0	0	$f_X/2^7$ (39.1 kHz)	$f_{CC}/2^7$ (7.81 kHz)
1	0	1	$f_X/2^8$ (19.5 kHz)	$f_{CC}/2^8$ (3.91 kHz)
1	1	0	Output of 8-bit timer 40	
1	1	1	Setting prohibited	

ERE10	EWE10	Write	Read	Remarks
0	0	Disabled	Disabled	EEPROM is in standby state (low power consumption mode)
0	1	Setting prohibited		
1	0	Disabled	Enabled	
1	1	Enabled	Enabled	

EWST10	EEPROM write status flag
0	Not writing to EEPROM (EEPROM can be read or written. However, writing is disabled if EWE10 = 0.)
1	Writing to EEPROM (EEPROM cannot be read or written.)

Note Bit 1 is read only.

Caution Be sure to set bit 3 to 1 and bit 7 to 0.

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. f_{CC}: System clock oscillation frequency (RC oscillation)

Table 5-1. EEPROM Write Time (When Operating at f_X = 5.0 MHz)

EWCS102	EWCS101	EWCS100	EEPROM Timer Count Clock	EEPROM Data Write Time[Note 1]
0	0	0	$f_X/2^3$ (625 kHz)	$2^3/f_X \times 145$ (setting prohibited)[Note 2]
0	0	1	$f_X/2^4$ (313 kHz)	$2^4/f_X \times 145$ (setting prohibited)[Note 2]
0	1	0	$f_X/2^5$ (156 kHz)	$2^5/f_X \times 145$ (setting prohibited)[Note 2]
0	1	1	$f_X/2^6$ (78.1 kHz)	$2^6/f_X \times 145$ (setting prohibited)[Note 2]
1	0	0	$f_X/2^7$ (39.1 kHz)	$2^7/f_X \times 145$ (3.71 ms)
1	0	1	$f_X/2^8$ (19.5 kHz)	$2^8/f_X \times 145$ (setting prohibited)[Note 2]
1	1	0	Output of 8-bit timer 40	(Output of 8-bit timer 40) × 145
1	1	1	Setting prohibited	

Notes 1. Be sure to set the EEPROM write time within the range of 3.3 to 6.6 ms.
The spec values of EEPROM write time are target values in the product development stage. Since they may change after evaluation, be sure to refer to the data sheet created after evaluation when designing.

2. Setting is prohibited because the condition that an EEPROM write time must be between 3.3 and 6.6 ms is not satisfied.

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)

Table 5-2. EEPROM Write Time (When Operating at f_{CC} = 1.0 MHz)

EWCS102	EWCS101	EWCS100	EEPROM Timer Count Clock	EEPROM Data Write Time[Note 1]
0	0	0	$f_{CC}/2^3$ (12.5 kHz)	$2^3/f_{CC} \times 145$ (setting prohibited)[Note 2]
0	0	1	$f_{CC}/2^4$ (62.5 kHz)	$2^4/f_{CC} \times 145$ (setting prohibited)[Note 2]
0	1	0	$f_{CC}/2^5$ (31.3 kHz)	$2^5/f_{CC} \times 145$ (4.64 ms)
0	1	1	$f_{CC}/2^6$ (15.6 kHz)	$2^6/f_{CC} \times 145$ (setting prohibited)[Note 2]
1	0	0	$f_{CC}/2^7$ (7.81 kHz)	$2^7/f_{CC} \times 145$ (setting prohibited)[Note 2]
1	0	1	$f_{CC}/2^8$ (3.91 kHz)	$2^8/f_{CC} \times 145$ (setting prohibited)[Note 2]
1	1	0	Output of 8-bit timer 40	(Output of 8-bit timer 40) × 145
1	1	1	Setting prohibited	

Notes 1. Be sure to set the EEPROM write time within the range of 3.3 to 6.6 ms.
The spec values of EEPROM write time are target values in the product development stage. Since they may change after evaluation, be sure to refer to the data sheet created after evaluation when designing.

2. Setting is prohibited because the condition that an EEPROM write time must be between 3.3 and 6.6 ms is not satisfied.

Remark f_{CC}: System clock oscillation frequency (RC oscillation)

5.4 Cautions for EEPROM Writing

The following cautions pertain to writing to EEPROM.

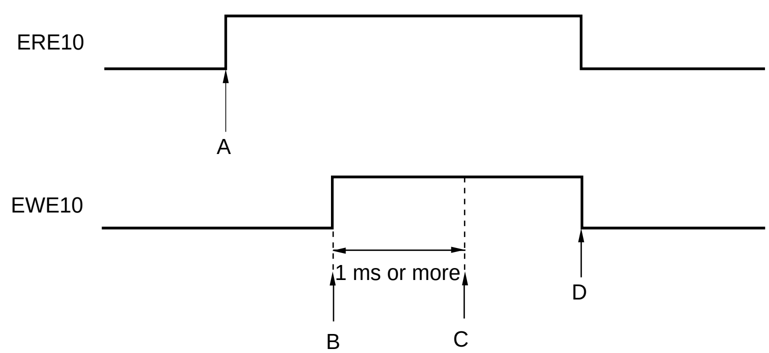
(1) When fetching an instruction from EEPROM or stopping the system clock oscillator, be sure to do so after setting EEPROM to write-disabled (EWE10 = 0).

(2) Set the count clock in a state in which the selected clock is operating (oscillating). If the selected count clock is stopped, there is no transition to the state in which writing is possible even if the clock operation is subsequently started and EEPROM is set to write-enabled (EWE10 = 1).

(3) Be sure to set the EEPROM write time within the range of 3.3 to 6.6 ms.

(4) When setting ERE10 and EWE10, be sure to use the following procedure. If you set these using other than the following procedure, there is no transition to the state in which writing to EEPROM is possible.

<1> Set ERE10 to 1 (In a state in which EWE10 = 0)
<2> Set EWE10 to 1 (In a state in which ERE10 = 1)
<3> Wait 1 ms or more using software
<4> Shift to state in which writing to EEPROM is possible



A (ERE10 = 1): Transition to state in which reading is possible
B (EWE10 = 1): Set count clock before this point.
C: Transition to state in which writing is possible
D: When ERE10 is cleared (ERE10 = 0), EWE10 is also cleared (EWE10 = 0).
Reading or writing is not possible in this state.

(5) When performing a write to EEPROM, execute it after confirming that EWST10 = 0.
If a write is executed to EEPROM when EWST10 = 1, the instruction is ignored.

(6) Do not execute the following operations while writing to EEPROM, as execution will cause the EEPROM cell value at that address to become undefined.

- Turn off the power
- Execute a reset
- Set ERE10 to 0
- Set EWE10 to 0
- Switch the EEPROM timer count clock

(7) Do not execute the following operation while writing to EEPROM after selecting system clock division for the EEPROM timer count clock, as execution will cause the EEPROM cell value at that address to become undefined.

- Execute a STOP instruction

(8) Do not execute the following operations while writing to EEPROM after selecting 8-bit timer 40 (TM40) output for the EEPROM timer count clock, as execution will cause the EEPROM cell value at that address to become undefined.

- Execute a STOP instruction
- Stop TM40 timer output
- Stop TM40 operation

(9) Do not execute the following operations while writing to or reading from EEPROM, as execution will cause the EEPROM data read next to become undefined, and a CPU runaway could result.

- Set ERE10 to 0
- Execute a write to EEPROM

(10) When not writing to or reading from EEPROM, it is possible to enter low-power consumption mode by setting ERE10 to 0. In the ERE10 = 1 state, a current of about 0.27 mA (V_{DD} = 3.6 V) is always flowing. If an instruction to read from EEPROM is then executed, a further 0.9 mA current will flow, increasing the total current flow at this time to approximately 1.17 mA (V_{DD} = 3.6 V).
In the ERE10 = 1, EWE10 = 1 state, a current of about 0.3 mA (V_{DD} = 3.6 V) is always flowing. If an instruction to write to EEPROM is then executed, a further 0.7 mA current will flow, and if an instruction to read from EEPROM is executed, a further 0.9 mA current will flow, increasing the total current flow at this time to approximately 1.0 mA (V_{DD} = 3.6 V) for the former case and 1.2 mA for the latter (refer to **EEPROM Characteristics** in **12. ELECTRICAL SPECIFICATIONS** for details).

(11) Execution of a STOP instruction causes an automatic change to low-power consumption mode, regardless of the ERE10 and EWE10 settings. The states of ERE10 and EWE10 at the time are maintained. During the wait time following STOP mode release, a current of approximately 300 μA (V_{DD} = 3.6 V) flows.
Executing a HALT instruction does not change the mode to low-power consumption mode.

6. PERIPHERAL HARDWARE FUNCTIONS

6.1 Ports

6.1.1 Port functions

The μPD78E9860 and μPD78E9861 are provided with the ports shown in Table 6-1, by which many kinds of control are possible. Moreover, these have a variety of alternate functions besides their functions as digital input/output ports. Refer to **3. PIN FUNCTIONS** for details of the alternate functions.

Table 6-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units.
Port 2	P20, P21	I/O port. Input/output can be specified in 1-bit units.
Port 4	P40 to P43	Input-only port.

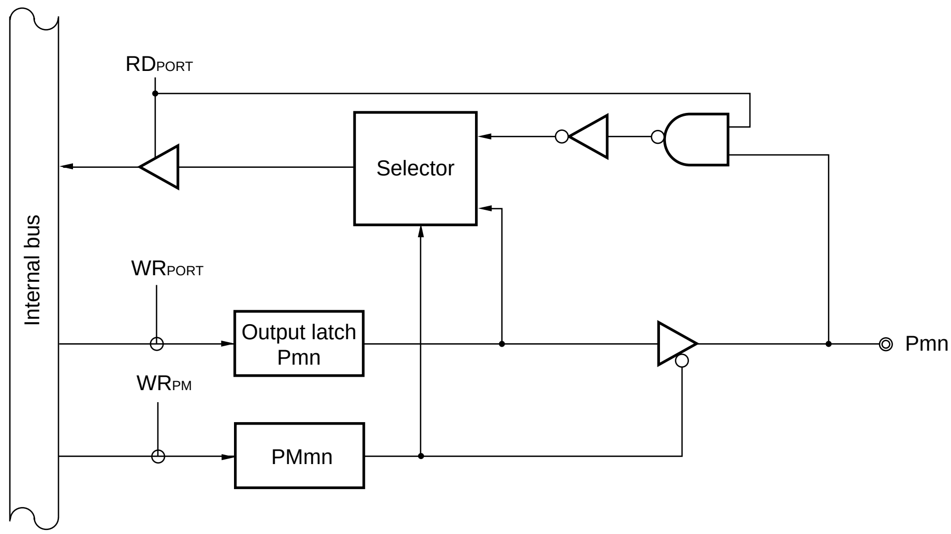
6.1.2 Port Configuration

A port consists of the following hardware.

Table 6-2. Port Configuration

Item	Configuration
Control register	Port mode register (PMm: m = 0, 2)
Port	Total: 14 (CMOS input/output: 10, CMOS input: 4)

Figure 6-1. Basic Configuration of CMOS Port



Caution Figure 6-1 is the basic configuration of a CMOS I/O port. The configuration varies according to the functions of alternate-function pins.

Remark PMmn: Bit n of port mode register m (m = 0, 2 n = 0 to 7)
Pmn: Bit n of port m
RD: Port read signal
WR: Port write signal

6.1.3 Registers that control port functions

A port is controlled using the following registers.

- Port mode registers (PM0, PM2)

(1) Port mode registers (PM0, PM2)

The port mode registers are registers that set the port to input or output in 1-bit units.

Each port mode register can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

When using a port pin as an alternate-function pin, set the port mode registers and output latch as shown in Table 6-3.

Figure 6-2. Port Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM2	1	1	1	1	1	1	PM21	PM20	FF22H	FFH	R/W

PMmn	Selection of Pmn pin input/output mode (m = 0, 2 n = 0 to 7)
0	Output mode (Output buffer on)
1	Input mode (Output buffer off)

Table 6-3. Port Mode Register and Output Latch Settings When Using Alternate Functions

Pin Name	Alternate Function		PM××	P××
	Name	I/O		
P20	TMO	Output	0	0
	BSFO	Output	0	0
P21	TMI	Input	1	×

Remark ×: don't care

PM××: Port mode register

P××: Port output latch

6.2 Clock Generator (μPD78E9860)

The clock generator specifications differ for the μPD78E9860 and μPD78E9861. When using the μPD78E9861, refer to **6.3 Clock Generator (μPD78E9861)**.

6.2.1 Clock generator functions

The clock generator is a circuit that generates the clocks that are provided to the CPU and peripheral hardware.

- System clock oscillator (ceramic/crystal oscillation)
  Oscillates at frequency from 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction.

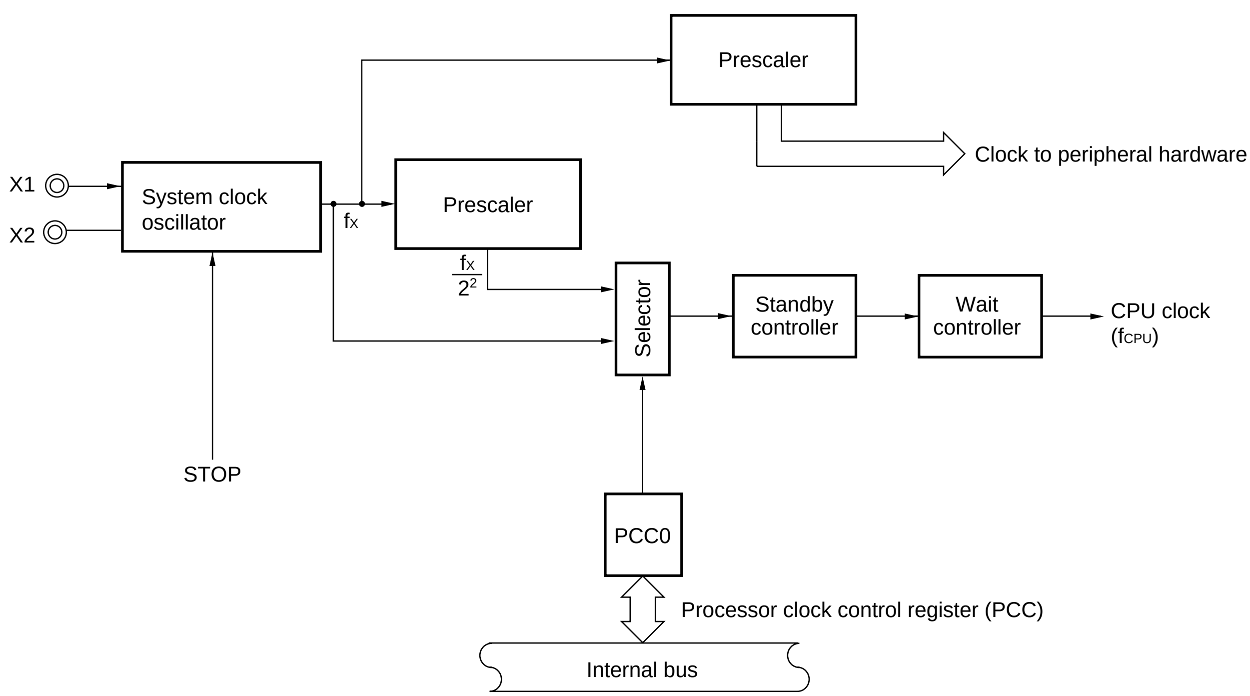
6.2.2 Configuration of clock generator

The clock generator consists of the following hardware.

Table 6-4. Configuration of Clock Generator

Item	Configuration
Control register	Processor clock control register (PCC)
Oscillator	System clock oscillator

Figure 6-3. Clock Generator Block Diagram



6.2.3 Register that controls clock generator

The clock generator is controlled by the following register.

- Processor clock control register (PCC)

(1) Processor clock control register (PCC)

The processor clock control register is a register that sets the CPU clock selection and division ratio.

PCC can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 02H.

Figure 6-4. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	0	0	0	0	0	0	PCC0	0	FFFBH	02H	R/W

PCC0	CPU clock (f_{CPU}) selection
0	f_X (0.2 μs)
1	$f_X/2^2$ (0.8 μs)

Caution Be sure to set bits 0 and 2 to 7 to 0.

Remarks **1.** f_X: System clock oscillation frequency (ceramic/crystal oscillator)

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

3. Minimum instruction execution time: 2 f_{CPU}

- 0.4 μs when f_{CPU} = 0.2 μs
- 1.6 μs when f_{CPU} = 0.8 μs

6.3 Clock Generator (μPD78E9861)

6.3.1 Clock generator functions

The clock generator is a circuit that generates the clocks that are provided to the CPU and peripheral hardware.

- System clock oscillator (RC oscillation)
  Oscillates at a frequency of 1.0 MHz ±15%. Oscillation can be stopped by executing the STOP instruction.

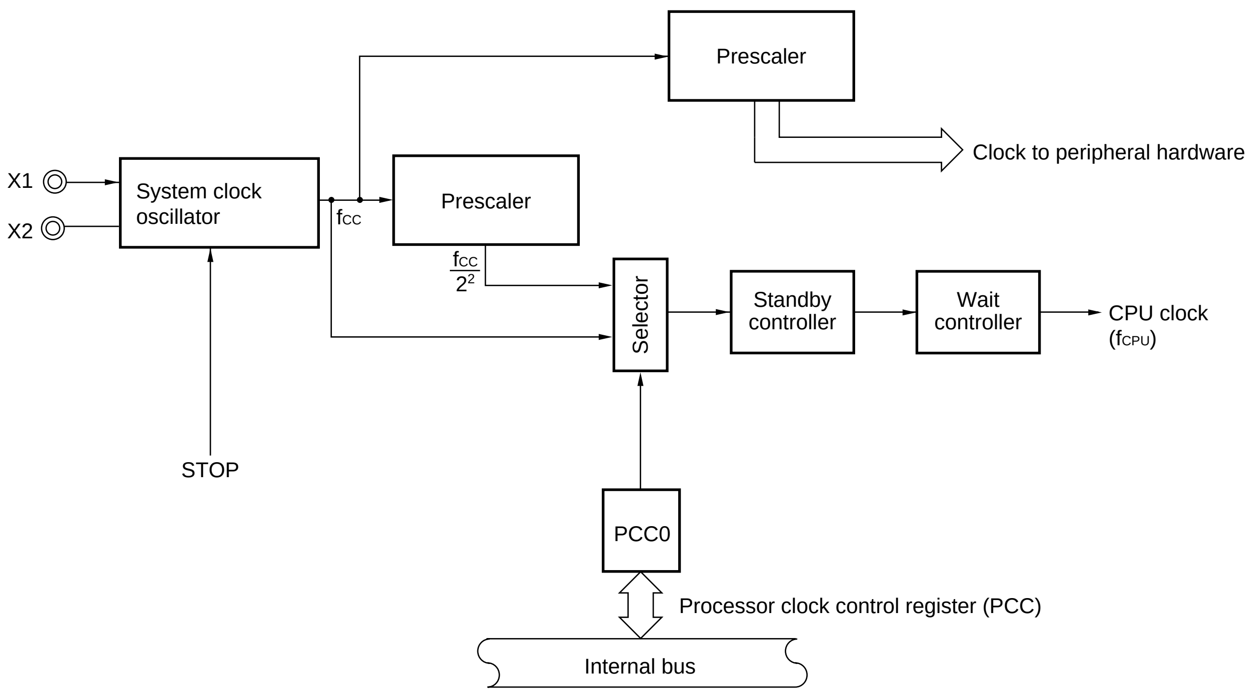
6.3.2 Configuration of clock generator

The clock generator consists of the following hardware.

Table 6-5. Configuration of Clock Generator

Item	Configuration
Control register	Processor clock control register (PCC)
Oscillator	System clock oscillator

Figure 6-5. Clock Generator Block Diagram



6.3.3 Register that controls clock generator

The clock generator is controlled by the following register.

- Processor clock control register (PCC)

(1) Processor clock control register (PCC)

The processor clock control register is a register that sets the CPU clock selection and division ratio.

PCC can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 02H.

Figure 6-6. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	0	0	0	0	0	0	PCC0	0	FFFBH	02H	R/W

PCC0	CPU clock (f_{CPU}) selection
0	f_{CC} (1.0 μs)
1	$f_{CC}/2^2$ (4.0 μs)

Caution Be sure to set bits 0 and 2 to 7 to 0.

Remarks

1. f_{CC}: System clock oscillation frequency (RC oscillation)

2. The parenthesized values apply to operation at f_{CC} = 1.0 MHz.

3. Minimum instruction execution time: 2 f_{CPU}

- 2.0 μs when f_{CPU} = 1.0 μs
- 8.0 μs when f_{CPU} = 4.0 μs

6.4 8-Bit Timer/Event Counter

6.4.1 8-bit timer/event counter functions

The μPD78E9860 and 78E9861 have on chip an 8-bit timer (Timer 30) (1 channel) and an 8-bit timer/event counter (Timer 40) (1 channel). The operation modes shown in the table below are possible by means of mode register settings.

Table 6-6. Mode List

Mode \ Channel	Timer 30	Timer 40
8-bit timer counter mode (discrete mode)	√	√
16-bit timer counter mode (cascade connection mode)	√	
Carrier generator mode	√	
PWM output mode	×	√

(1) 8-bit timer counter mode (discrete mode)

The following functions can be used.

- 8-bit resolution interval timer
- 8-bit resolution external event timer (Timer 40 only)
- 8-bit resolution square wave output (Timer 40 only)

(2) 16-bit timer counter mode (cascade connection mode)

Operates as a 16-bit timer/event counter due to cascade connection.
The following functions can be used.

- 16-bit resolution interval timer
- 16-bit resolution external event counter
- 16-bit resolution square wave output

(3) Carrier generator mode

In this mode, the carrier clock generated by timer 40 is output in the cycle set by timer 30.

(4) PWM output mode

Outputs a pulse of an arbitrary duty factor set by timer 40.

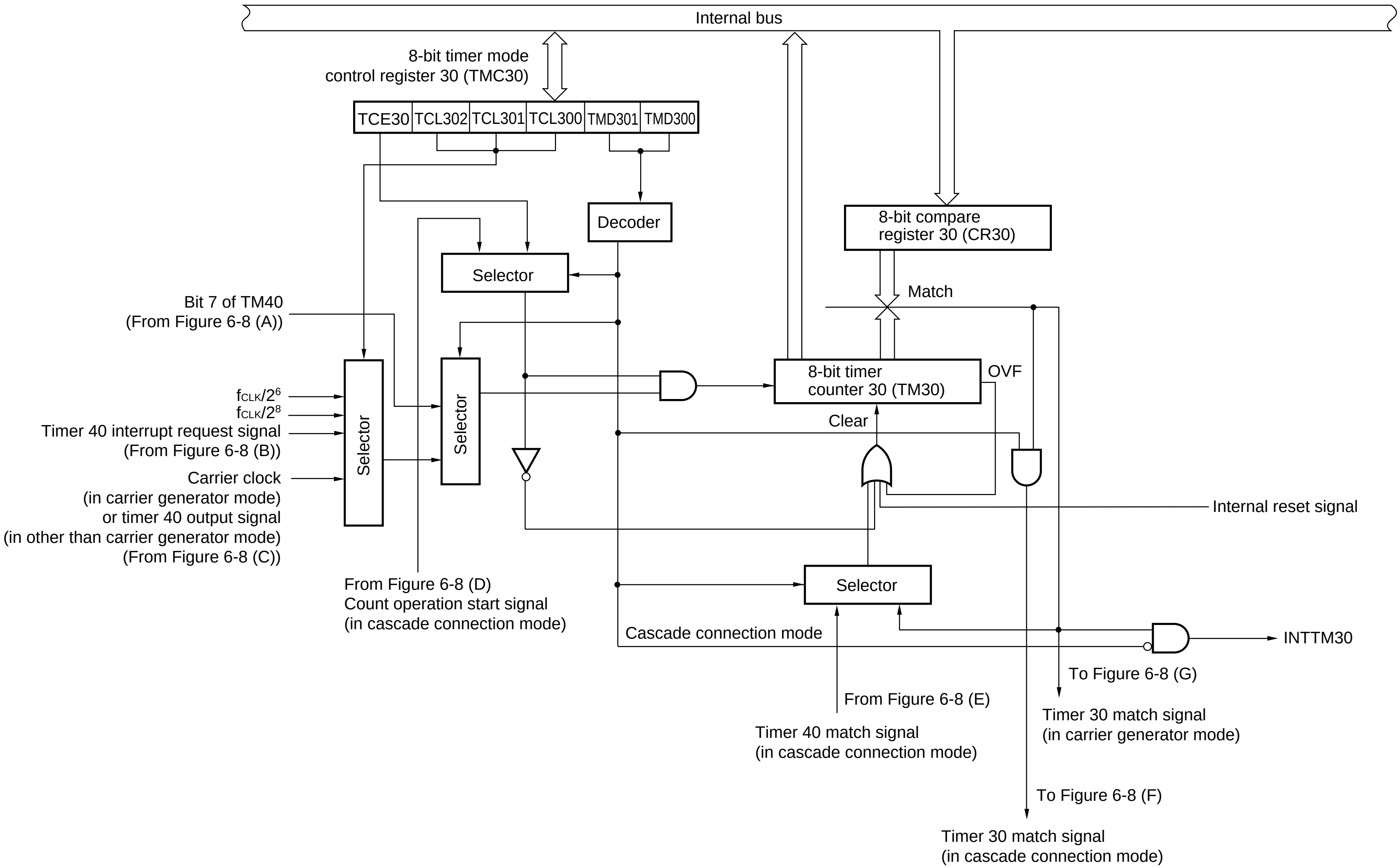
6.4.2 8-bit timer/event counter configuration

The 8-bit timer/event counter consists of the following hardware.

Table 6-7. Configuration of 8-Bit Timer/Event Counter

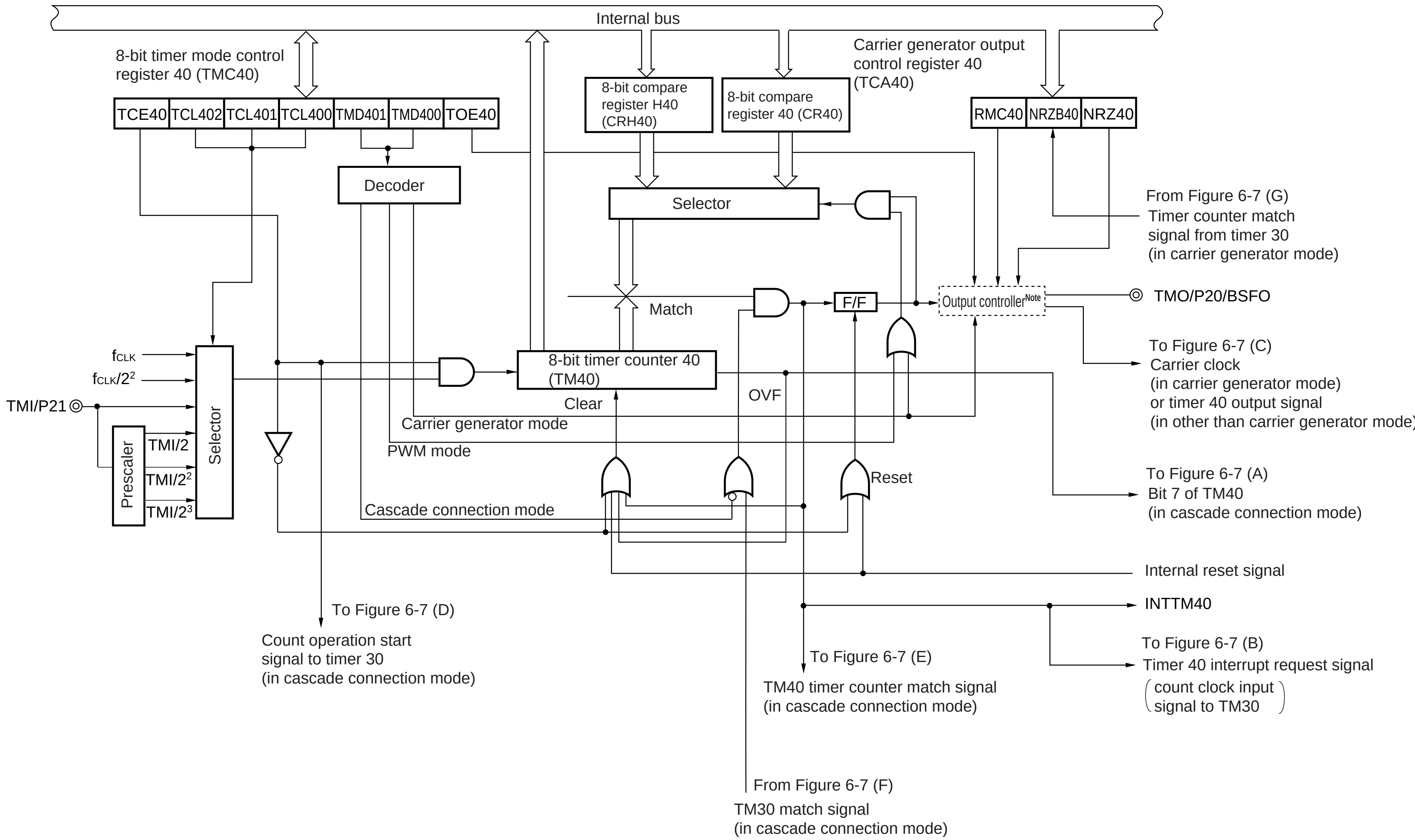
Item	Configuration
Timer counter	8 bits × 2 (TM30, TM40)
Registers	Compare registers: 8 bits × 3 (CR30, CR40, CRH40)
Timer output	1 (TMO)
Control registers	8-bit timer mode control register 30 (TMC30) 8-bit timer mode control register 40 (TMC 40) Carrier generator output control register 40 (TCA40) Port mode register 2 (PM2)

Figure 6-7. Timer 30 Block Diagram



Remark f_{CLK}: f_X or f_{CC}

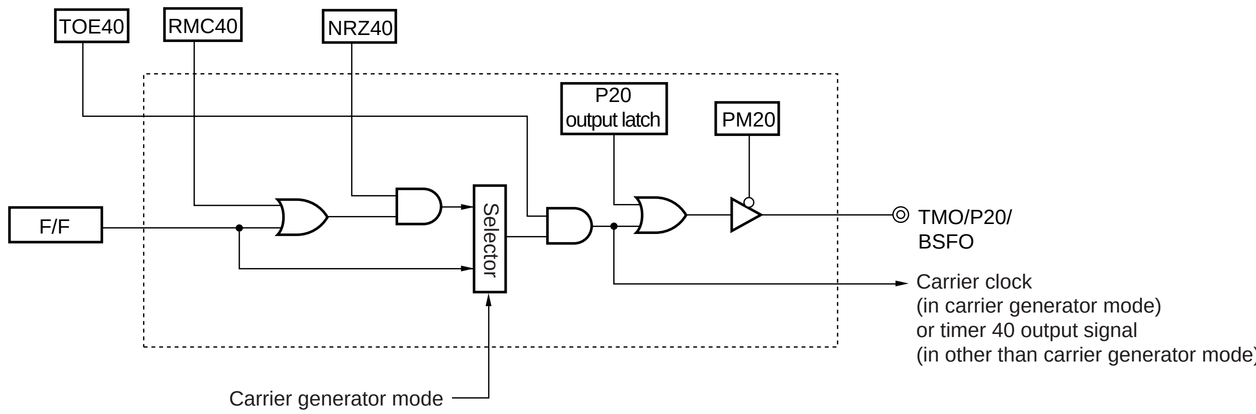
Figure 6-8. Timer 40 Block Diagram



Note For details, refer to Figure 6-9.

Remark f_{CLK}: f_X or f_{CC}

Figure 6-9. Block Diagram of Output Controller (Timer 40)



(1) 8-bit compare register 30 (CR30)

This register is an 8-bit register that always compares the count value of 8-bit timer register 30 (TM30) with the value set in CR30 and generates an interrupt request (INTTM30) if they match.

CR30 can be set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

Caution CR30 cannot be used in carrier generator mode or PWM output mode.

(2) 8-bit compare register 40 (CR40)

This register is an 8-bit register that always compares the count value of 8-bit timer register 40 (TM40) with the value set in CR40 and generates an interrupt request (INTTM40) if they match. In addition, when cascade-connected to TM30 and used as a 16-bit timer/event counter, an interrupt request (INTTM40) is generated only if TM30 matches with CR30 and TM40 matches with CR40 simultaneously (INTTM30 is not generated).

CR40 can be set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(3) 8-bit compare register H40 (CRH40)

In carrier generator mode or PWM output mode, writing a CRH40 value sets the width of high level timer output.

CRH40 can be set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(4) 8-bit timer counters 30 and 40 (TM30, TM40)

These 8-bit registers count pulse counts.

Each of TM30 and TM40 can be read using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to 00H.

The conditions under which TM30 and TM40 are cleared to 00H are shown next.

(a) Discrete mode

(i) TM30

- Reset
- Clearing of TCE30 (bit 7 of 8-bit timer mode control register 30 (TMC30)) to 0
- Match of TM30 and CR30
- TM30 count value overflow

(ii) TM40

- Reset
- Clearing of TCE40 (bit 7 of 8-bit timer mode control register 40 (TMC40)) to 0
- Match of TM40 and CR40
- TM40 count value overflow

(b) Cascade connection mode (TM30, TM40 simultaneously cleared to 00H)

- Reset
- Clearing of the TCE40 flag to 0
- Simultaneous match of TM30 with CR30 and TM40 with CR40
- TM30 and TM40 count values overflow simultaneously

(c) Carrier generator/PWM output mode (TM40 only)

- Reset
- Clearing of the TCE40 flag to 0
- Match of TM40 and CR40
- Match of TM40 and CRH40
- TM40 count value overflow

6.4.3 Registers that control 8-bit timer/event counter

The 8-bit timer/event counter is controlled by the following three registers.

- 8-bit timer mode control register 30 (TMC30)
- 8-bit timer mode control register 40 (TMC40)
- Carrier generator output control register 40 (TCA40)
- Port mode register 2 (PM2)

(1) 8-bit timer mode control register 30 (TMC30)

8-bit timer mode control register 30 (TMC30) is the register that controls the setting of the timer 30 count clock and the setting of the operating mode.

TMC30 can be set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

★ **Figure 6-10. Format of 8-Bit Timer Mode Control Register 30**

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
TMC30	TCE30	0	TCL302	TCL301	TCL300	TMD301	TMD300	0	FF52H	00H	R/W

TCE30	TM30 count operation control[Note 1]
0	Clears TM30 count value and halt operation
1	Starts count operation

TCL302	TCL301	TCL300	Selection of timer 30 count clock	
			When operating at f_X = 5.0 MHz	When operating at f_{CC} = 1.0 MHz
0	0	0	$f_X/2^6$ (78.1 kHz)	$f_{CC}/2^6$ (15.6 kHz)
0	0	1	$f_X/2^8$ (19.5 kHz)	$f_{CC}/2^8$ (3.91 kHz)
0	1	0	Timer 40 match signal	
0	1	1	Carrier clock (in carrier generator mode) or timer 40 output signal (in other than carrier generator mode)	
Other than above			Setting prohibited	

TMD301	TMD300	TMD401	TMD400	Selection of timer 30, timer 40 operating mode[Note 2]
0	0	0	0	Discrete mode
0	1	0	1	Cascade connection mode
0	0	1	1	Carrier generator mode
0	0	1	0	PWM output mode
Other than above				Setting prohibited

Notes 1. In cascade connection mode, since count operations are controlled by TCE40 (bit 7 of TMC40), TCE30 is ignored even if it is set.

2. The selection of operating mode is made by combining the two registers TMC30 and TMC40.

Cautions 1. Be sure to set bits 0 and 4 to 0.

2. In cascade connection mode, timer 40 output signal is forcibly selected for count clock.

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. f_{CC}: System clock oscillation frequency (RC oscillation)

(2) 8-bit timer mode control register 40 (TMC40)

8-bit timer mode control register 40 (TMC40) is the register that controls the setting of the timer 40 count clock and the setting of the operating mode.

TMC40 can be set using a 1-bit or 8-bit memory manipulation instruction.

RESET input sets this register to 00H.

★ **Figure 6-11. Format of 8-Bit Timer Mode Control Register 40**

Symbol	<7>	6	5	4	3	2	1	<0>	Address	After reset	R/W
TMC40	TCE40	0	TCL402	TCL401	TCL400	TMD401	TMD400	TOE40	FF56H	00H	R/W

TCE40	TM40 count operation control[Note 1]
0	Clears TM40 count value and halt operation (in cascade connection mode, the TM30 count value is simultaneously cleared as well.)
1	Starts count operation (in cascade connection mode, the TM30 count operation is simultaneously started as well.)

TCL402	TCL401	TCL400	Selection of timer 40 count clock	
			When operating at f_X = 5.0 MHz	When operating at f_{CC} = 1.0 MHz
0	0	0	f_X (5.0 MHz)	f_{CC} (1.0 MHz)
0	0	1	$f_X/2^2$ (1.25 MHz)	$f_{CC}/2^2$ (250 MHz)
0	1	0	f_{TMI}	
0	1	1	$f_{TMI}/2$	
1	0	0	$f_{TMI}/2^2$	
1	0	1	$f_{TMI}/2^3$	

TMD301	TMD300	TMD401	TMD400	Selection of timer 30, timer 40 operating mode[Note 2]
0	0	0	0	Discrete mode
0	1	0	1	Cascade connection mode
0	0	1	1	Carrier generator mode
0	0	1	0	PWM output mode
Other than above				Setting prohibited

TCE40	Timer output control
0	Output disabled
1	Output enabled (port mode)

Notes 1. In cascade connection mode, since count operations are controlled by TCE40 (bit 7 of TMC40), TCE30 is ignored even if it is set.

2. The selection of operating mode is made by combining the two registers TMC30 and TMC40.

Remarks. 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. f_{CC}: System clock oscillation frequency (RC oscillation)

3. f_{TMI}: External clock input from TMI/P21 pin

(3) Carrier generator output control register 40 (TCA40)

This register is used to set the timer output data in the carrier generator mode.

TCA40 is set using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-12. Format of Carrier Generator Output Control Register 40

★

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
TCA40	0	0	0	0	0	RMC40	NRZB40	NRZ40	FF6AH	00H	W

RMC40	Remote controller output control
0	When NRZ40 = 1, a carrier pulse is output to the TMO/P20/BSFO pin
1	When NRZ40 = 1, a high level is output to the TMO/P20/BSFO pin

NRZB40	This bit stores the data that NRZ40 will output next. Data is transferred to NRZ40 upon the generation of a timer 30 match signal.

NRZ40	No return, zero data
0	A low level is output (the carrier clock is stopped)
1	A carrier pulse is output

Caution TCA40 cannot be set using a 1-bit memory manipulation instruction. Be sure to set this register using an 8-bit memory manipulation instruction.

(4) Port mode register 2 (PM2)

This register sets port 2 to input/output in 1-bit units.

When using the P20/TMO/BSFO pin as a timer output, set the PM20 and P20 output latch to 0.

PM2 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to FFH.

Figure 6-13. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	1	1	1	1	1	PM21	PM20	FF22H	FFH	R/W

PM21	P20 pin input/output mode
0	Output mode (output buffer on)
1	Input mode (output buffer off)

6.5 Watchdog Timer

6.5.1 Watchdog timer functions

The watchdog timer has the following functions.

(1) Watchdog timer

Detects program runaway. When runaway is detected, a non-maskable interrupt or $\overline{\text{RESET}}$ can be generated.

(2) Interval timer

Generates an interrupt at an arbitrary preset time interval.

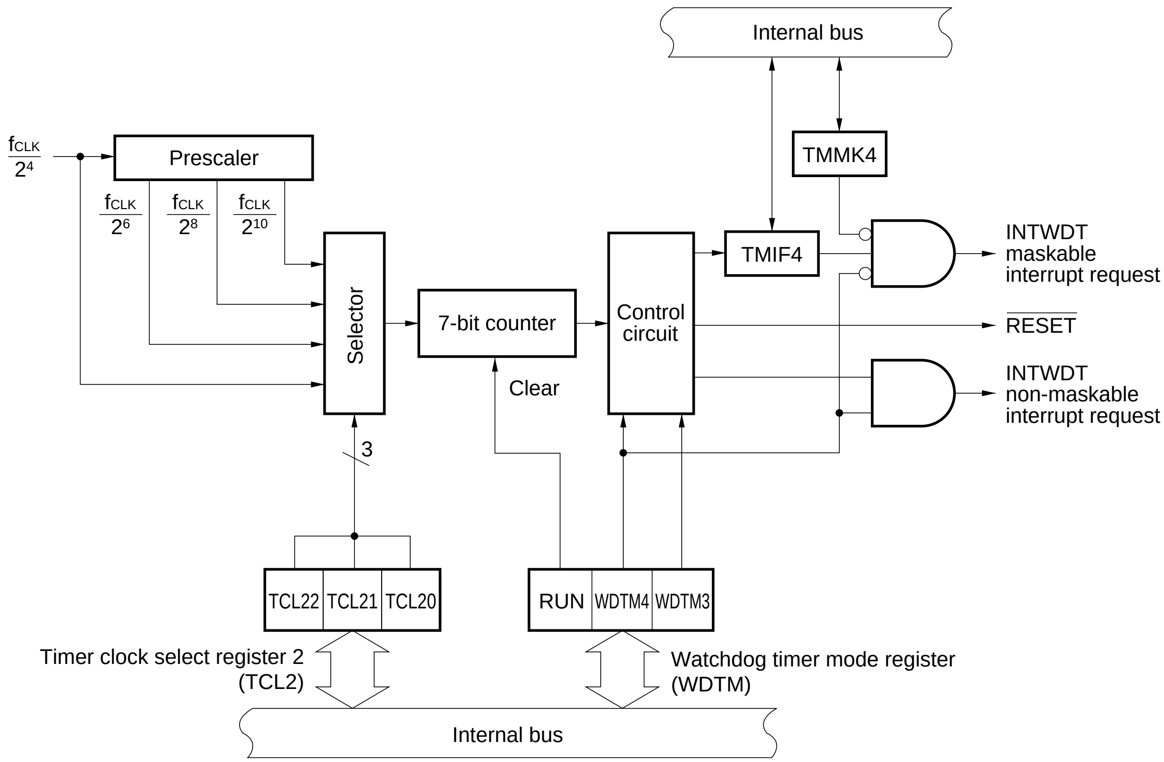
6.5.2 Configuration of watchdog timer

The watchdog timer consists of the following hardware. Figure 6-13 shows watchdog timer block diagram.

Table 6-8. Configuration of Watchdog Timer

Item	Configuration
★ Control register	Timer clock select register 2 (TCL2) Watchdog timer mode register (WDTM)

★ **Figure 6-14. Watchdog Timer Block Diagram**



Remark f_{CLK}: f_X or f_{CC}

6.5.3 Register that controls watchdog timer

The watchdog timer is controlled by the following two registers.

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

★ **(1) Timer clock select register 2 (TCL2)**

This register sets the watchdog timer count clock.

TCL2 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears this register TCL2 to 00H.

Figure 6-15. Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
TCL2	0	0	0	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Watchdog timer count clock selection		interval time	
			At f_X = 5.0 MHz operation	At f_{CC} = 1.0 MHz operation	At f_X = 5.0 MHz operation	At f_{CC} = 1.0 MHz operation
0	0	0	$f_X/2^4$ (312.5 kHz)	$f_{CC}/2^4$ (62.5 kHz)	$2^{11}/f_X$ (410 μs)	$2^{11}/f_{CC}$ (2.05 ms)
0	1	0	$f_X/2^6$ (78.1 kHz)	$f_{CC}/2^6$ (15.6 kHz)	$2^{13}/f_X$ (1.64 ms)	$2^{13}/f_{CC}$ (8.19 ms)
1	0	0	$f_X/2^8$ (19.5 kHz)	$f_{CC}/2^8$ (3.91 kHz)	$2^{15}/f_X$ (6.55 ms)	$2^{15}/f_{CC}$ (32.8 ms)
1	1	0	$f_X/2^{10}$ (4.88 kHz)	$f_{CC}/2^{10}$ (977 Hz)	$2^{17}/f_X$ (26.2 ms)	$2^{17}/f_{CC}$ (131.1 ms)
Other than above			Setting prohibited			

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. f_{CC}: System clock oscillation frequency (RC oscillation)

(2) Watchdog timer mode register (WDTM)

This register sets the watchdog timer operating mode and enables or disables counting.

WDTM can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-16. Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Selection of watchdog timer operation[Note 1]
0	Count stop
1	Counter is cleared and then counting starts

WDTM4	WDTM3	Selection of watchdog timer operating mode[Note 2]
0	0	Operation stop
0	1	Interval timer mode (maskable interrupt generated if overflow occurs)[Note 3]
1	0	Watchdog timer mode 1 (non-maskable interrupt generated if overflow occurs)
1	1	Watchdog timer mode 2 (reset operation started if overflow occurs)

Notes 1. Once RUN is set (1), it cannot be cleared (0) by software. Therefore, once a count it is started cannot be stopped by $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 are set (1), they cannot only be cleared (0) by software.

3. Operation as an interval timer starts at the time that RUN is set to 1.

Cautions 1. When the watchdog timer is cleared by setting RUN to 1, the actual overflow time is at most 0.8% shorter than the time set using timer clock selection register 2.

2. When using watchdog timer mode 1 or 2, set WDTM4 to 1 after confirming that TMIF4 (bit 0 of interrupt request flag register 0 (IF0)) is 0. If watchdog timer mode 1 or 2 is selected when TMIF4 is 1, a non-maskable interrupt occurs at the same time as writing terminates.

6.6 Power-on-Clear Circuits

6.6.1 Power-on-clear circuit functions

The power-on-clear circuits include the following two circuits, which have the following function.

(1) Power-on-clear (POC) circuit

- Compares the detection voltage (V_{POC}) with the power supply voltage (V_{DD}) and generates an internal reset signal if $V_{DD} < V_{POC}$.
- This circuit can operate even in STOP mode.

(2) Low-voltage detection (LVI) circuit

- Compares the detection voltage (V_{LVI}) to the power supply voltage (V_{DD}) and generates an interrupt request signal (INTLVI1) if $V_{DD} < V_{LVI}$.
- Eight levels of detection voltage can be selected using software.
- This circuit stops operation in STOP mode.

6.6.2 Configuration of power-on-clear circuit

Figures 6-17 and 6-18 show the block diagrams of the power-on-clear circuits.

Figure 6-17. Block Diagram of Power-on-Clear Circuit

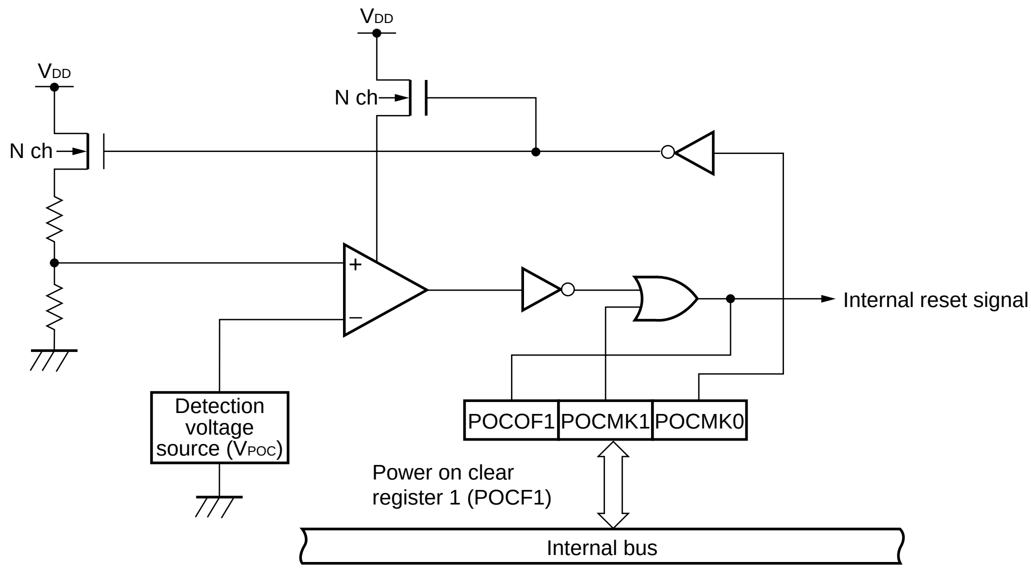
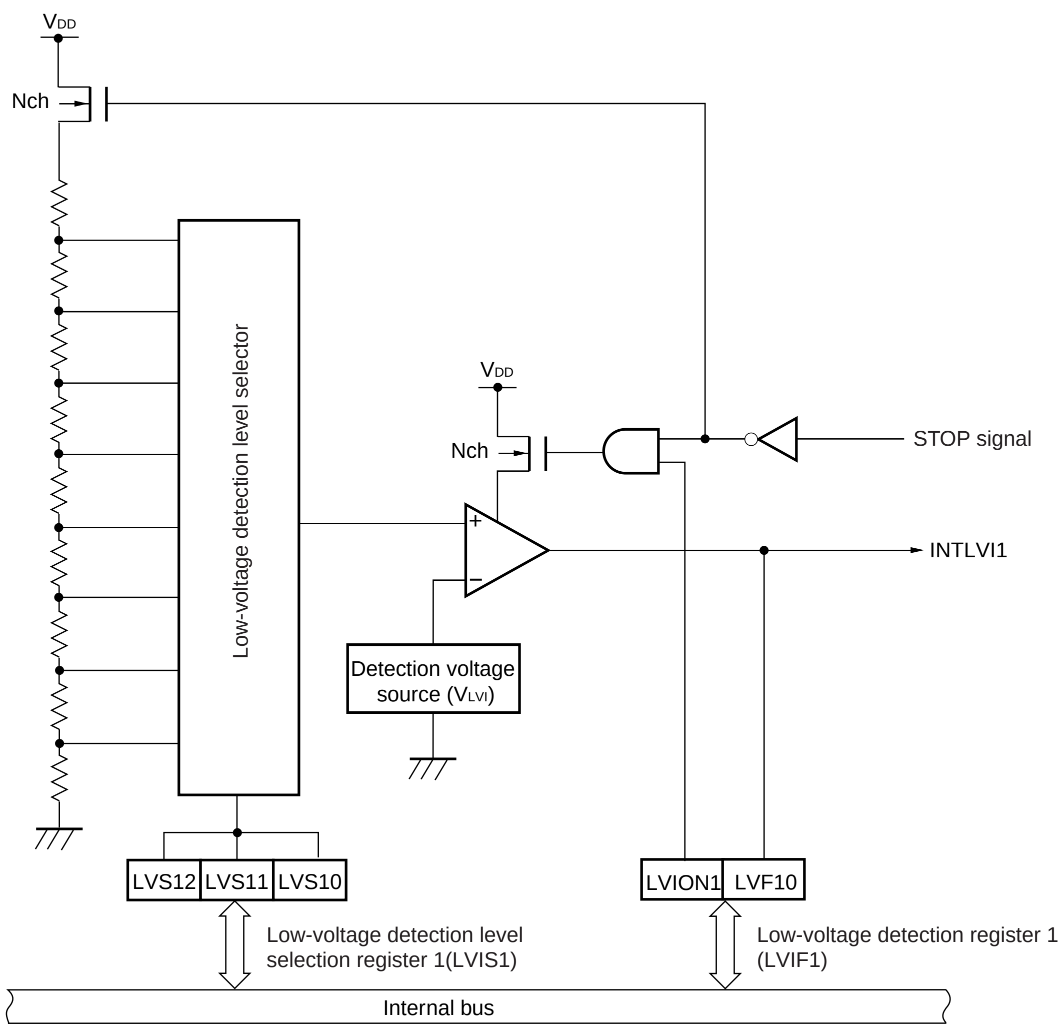


Figure 6-18. Block Diagram of Low-Voltage Detection Circuit



6.6.3 Registers that control power-on-clear circuits

The following three registers control the power-on-clear circuits.

- Power-on-clear register 1 (POCF1)
- Low-voltage detection register 1 (LVIF1)
- Low-voltage detection level selection register 1 (LVIS1)

(1) Power on clear register 1 (POCF1)

This register controls POC circuit operation.

POCF1 can be set using a 1-bit or 8-bit memory manipulation instruction.

Figure 6-19. Format of Power-on-Clear Register 1

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
POCF1	0	0	0	0	0	POCOF1	POCMK1	POCMK0	FFDDH	00H[Note]	R/W

POCOF1	POC output detection flag
0	Non-generation of reset signal by POC or in cleared state due to a write operation to POCF1
1	Generation of reset signal by POC

POCMK1	POC reset control
0	Generation of reset signal by POC enabled
1	Generation of reset signal by POC disabled

POCMK0	POC operation control
0	POC operating
1	POC halted

Note This value is 04H only after a power-on-clear reset.

(2) Low-voltage detection register 1 (LVIF1)

This register controls the operation of the LVI circuit.

LVIF1 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-20. Format of Low-Voltage Detection Register 1

Symbol	<7>	6	5	4	3	2	1	<0>	Address	After reset	R/W
LVIF1	LVION1	0	0	0	0	0	0	LVF10	FFDEH	00H	R/W[Note]

LVION1	LVI operation enable flag
0	LVI disabled
1	LVI enabled

LVF10	LVI output detection flag
0	Power supply voltage (V_{DD}) > LVI detection voltage (V_{LVI}) or operation disabled
1	$V_{DD} < V_{LVI}$

Note Bit 0 is read only.

Caution When the LVI circuit enters STOP mode, it is automatically turned off (low-current consumption mode). When STOP mode is released, it necessary to wait about 2 ms for the operation of the LVI circuit to stabilize. Because it is possible for an interrupt request signal to be generated in this stabilization period, be sure to disable any interrupts by setting LVIMK1 (bit 3 of interrupt mask flag register 0 (MK0)) (LVIMK1 = 1) before setting the STOP mode.

The program example is shown below.

Example After setting the STOP mode, an interrupt is enabled following the elapse of the operation stabilization time (for RC oscillation).

```
      SET1   LVIMK1
      STOP
      MOV    A, #0BCH
WAIT:
      DEC    A        ]  10 clocks
      BNZ    $WAIT

      CLR1   LVIIF1
      CLR1   LVIMK1
```

Because the required operation stabilization time following the release of STOP mode is $2^7/f_{CC}$ = 128 μs (when f_{CC} = 1 MHz operation), it is necessary to make the program wait for 2 ms – 128 μs (approx. 1880 μs). When the CPU clock is 1 μs (when f_{CC} = 1 MHz operation), secure the wait time by making the program loop 188 times.

Caution In the case of a ceramic/crystal oscillator, because the oscillation stabilization time following release of STOP mode is 2 ms or more, the above program wait is unnecessary.

(3) Low-voltage detection level selection register 1 (LVIS1)

This register selects the level of the detection voltage (V_{LVI}).

LVIS1 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-21. Format of Low-Voltage Detection Level Selection Register 1

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
LVIS1	0	0	0	0	0	LVS12	LVS11	LVS10	FFDFH	00H	R/W

LVS12	LVS11	LVS10	Selection of detection voltage (V_{LVI}) level[Note]
0	0	0	V_{LVI0}
0	0	1	V_{LVI1}
0	1	0	V_{LVI2}
0	1	1	V_{LVI3}
1	0	0	V_{LVI4}
1	0	1	V_{LVI5}
1	1	0	V_{LVI6}
1	1	1	V_{LVI7}

Note Refer to **12. ELECTRICAL SPECIFICATIONS** for detection voltage specifications.

Caution When changing the detection voltage level (V_{LVI}), an operation stabilization time of about 2 ms is required in order for the LVI output to stabilize. Do not, therefore, set the LVI circuit to operation-enable until the operation has stabilized.

6.7 Bit Sequential Buffer

6.7.1 Functions of bit sequential buffer

The μPD78E9860 and μPD78E9861 have an on-chip bit sequential buffer of 8 bits × 8 bits = 16 bits.
The functions of the bit sequential buffer are shown below.

- If the value of the bit sequential buffer 10 data register (BSFRL10, BSFRH10) is shifted 1 bit to the lower side, the LSB can be output to the port at the same time.
- It is possible to write to BSFRL10 and BSFRH10 using an 8-bit or 16-bit manipulation instruction.
- Overwriting is enabled during a shift operation on the higher 8 bits only (the period in which shift clock is low level).

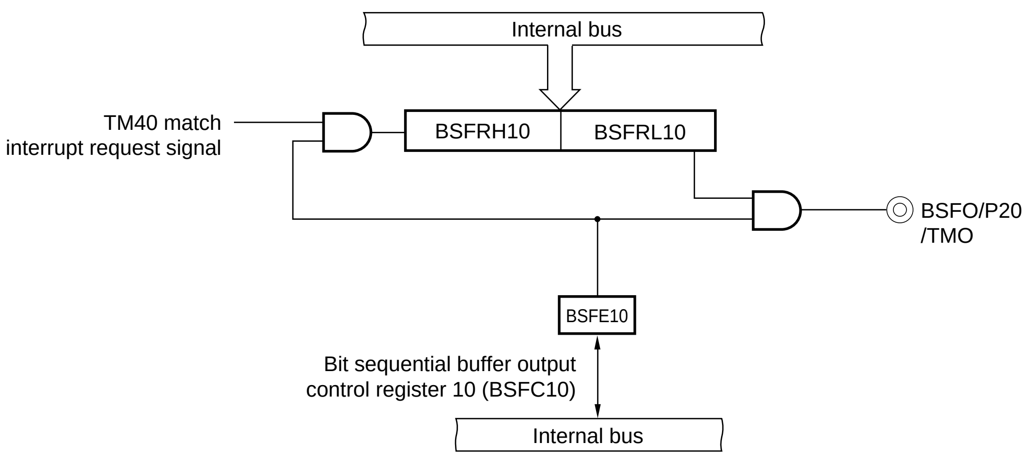
6.7.2 Configuration of bit sequential buffer

The bit sequential buffer consists of the following hardware.

Table 6-9. Configuration of Bit Sequential Buffer

Item	Configuration
Data register	Bit sequential buffer: 8 bits × 8 bits = 16 bits
Control register	Bit sequential buffer output control register 10 (BSFC10)

Figure 6-22. Block Diagram of Bit Sequential Buffer



6.7.3 Register that controls the bit sequential buffer

The following register controls the bit sequential buffer.

- Bit sequential buffer output control register 10 (BSFC10)

(1) Bit sequential buffer output control register 10 (BSFC10)

This register controls the operation of the bit sequential buffer.

BSFC10 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 6-23. Format of Bit Sequential Buffer Output Control Register 10

Symbol	7	6	5	4	3	2	1	<0>	Address	After reset	R/W
BSFC10	0	0	0	0	0	0	0	BSFE10	FF60H	00H	R/W

BSFE10	Bit sequential buffer operation control
0	Operation disabled
1	Operation enabled

6.8 Key Return Circuit

6.8.1 Function of key return circuit

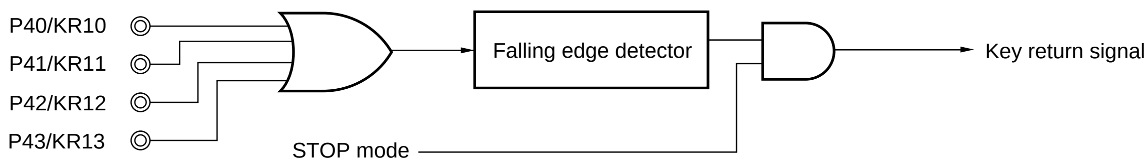
In STOP mode, this circuit generates a key return interrupt by inputting a P40/KR10 to P43/KR13 falling edge.
It can be used in judging the cause of a STOP mode release in software.

Caution The key return interrupt is a non-maskable interrupt that is effective only in STOP mode. In addition, P40/KR10 to P43/KR13 key input cannot be performed by mask control.

6.8.2 Configuration of key return circuit

Figure 6-24 shows the block diagram of the key return circuit.

Figure 6-24. Block Diagram of Key Return Circuit



7. INTERRUPT FUNCTIONS

7.1 Types of Interrupt Functions

The following two types of interrupt functions are available.

(1) Non-maskable interrupts

A non-maskable interrupt is an interrupt that is accepted unconditionally even in a state in which interrupts are disabled. In addition, it is not subject to interrupt priority control and has a greater priority than all other interrupt requests.
A non-maskable interrupt generates the standby release signal.
Non-maskable interrupts have 1 internal interrupt source and 1 external interrupt source.

(2) Maskable interrupts

A maskable interrupt is an interrupt that is mask controlled. The order of priority when multiple interrupt requests are generated at the same time is determined as shown in Table 7-1.
A maskable interrupt generates the standby release signal.
Maskable interrupts have 5 internal interrupt sources.

7.2 Sources and Configuration of Interrupts

There are a total of seven sources of interrupts for non-maskable interrupts and maskable interrupts combined (see Table 7-1).

Table 7-1. List of Interrupt Sources

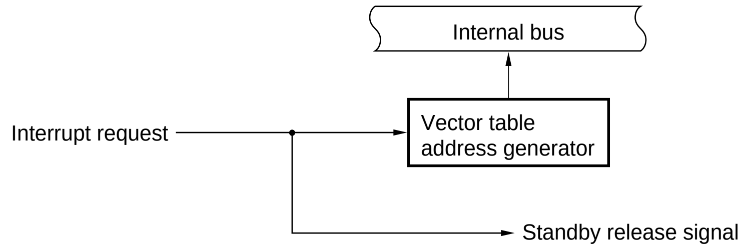
Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTKR1	Key return input falling edge detected[Note 3]	External	0002H	(A)
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTTM30	8-bit timer 30 match signal generation		0006H	
	2	INTTM40	8-bit timer 40 match signal generation		0008H	
	3	INTLVI1	LVI interrupt request signal		000AH	
	4	INTEE0	EEPROM write termination signal		000CH	

Notes 1. The priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 4 is the lowest.
2. Basic configuration type (A) and (B) correspond to (A) and (B) in Figure 7-1.
3. Only in STOP mode. Interrupt request signals are not generated other than in STOP mode.

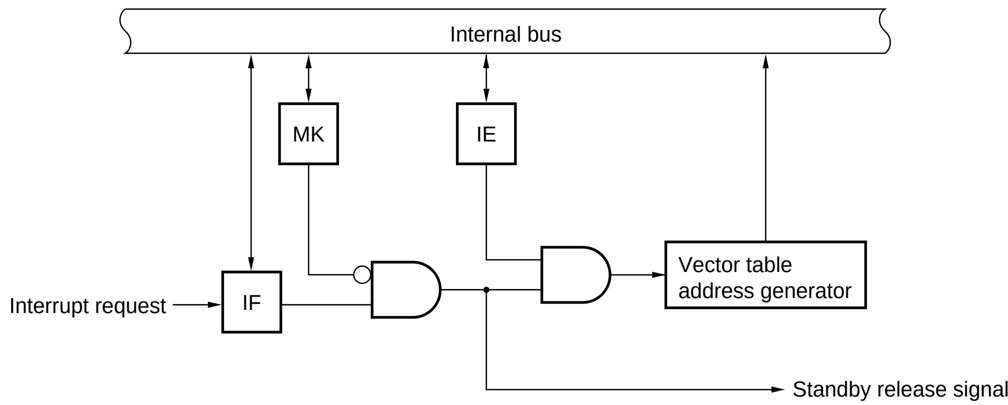
Remark Only one of watchdog timer interrupt sources (INTWDT), non-maskable or maskable, can be chosen.

Figure 7-1. Basic Configuration of Interrupt Functions

(A) External/internal non-maskable interrupt



(B) Internal maskable interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7.3 Registers That Control Interrupt Functions

The following three registers control the interrupt functions.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- Program status word (PSW)

Table 7-2 shows the names of the interrupt request flag and interrupt mask flag for each interrupt request.

Table 7-2. Flags for Interrupt Request Signal Names

Interrupt Request Signal Name	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	TMIF4	TMMK4
INTTM30	TMIF30	TMMK30
INTTM40	TMIF40	TMMK40
INTLVI	LVIIF1	LVIMK1
INTEE0	EEIF0	EEMK0

(1) Interrupt request flag register 0 (IF0)

The interrupt request flag is a flag that is set (1) by the generation of a corresponding interrupt request or the execution of an instruction and that is cleared (0) by executing an instruction when an interrupt request is acknowledged or $\overline{\text{RESET}}$ is input.

IF0 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 7-2. Format of Interrupt Request Flag Register 0

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0	0	0	0	EEIF0	LVIIF1	TMIF40	TMIF30	TMIF4	FFE0H	00H	R/W

××IF×	Interrupt request flag
0	Interrupt request signal has not been generated
1	Interrupt request signal generated; interrupt request state

Cautions 1. Be sure to set bits 5 to 7 to 0.

2. The TMIF4 flag can be read or written only when the watchdog timer is being used as an interval timer. Set the TMIF4 flag to 0 when using it in watchdog timer mode 1 or 2.

(2) Interrupt mask flag register 0 (MK0)

The interrupt mask flag is a flag that sets the servicing of the corresponding maskable interrupt to enabled or disabled.

MK0 can be set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to FFH.

Figure 7-3. Format of Interrupt Mask Flag Register 0

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0	1	1	1	EEMK0	LVIMK1	TMMK40	TMMK30	TMMK4	FFE4H	FFH	R/W

××MK×	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Cautions 1. Be sure to set bits 5 to 7 to 1.

2. The TMMK4 flag can be read or written only when the watchdog timer is being used as an interval timer. Set the TMMK4 flag to 0 when using it in watchdog timer mode 1 or 2.

(3) Program status word (PSW)

The program status word is a register that maintains the current state with respect to the result of instruction execution or an interrupt request. The IE flag, which sets maskable interrupts to enabled or disabled, is mapped to it.

Besides manipulation of reading or writing in 8-bit units, manipulation by bit manipulation instructions and dedicated instructions (EI, DI) is also possible. When a vector interrupt is acknowledged, the PSW is automatically saved in the stack and the IE flag is reset (0).

$\overline{\text{RESET}}$ input sets the PSW to 02H.

Figure 7-4. Configuration of Program Status Word

Symbol	7	6	5	4	3	2	1	0	After reset
PSW	IE	Z	0	AC	0	0	1	CY	02H

(Z, AC, CY) → Used when executing normal instructions

IE	Interrupt acknowledgement enabled/disabled
0	Disabled
1	Enabled

8. STANDBY FUNCTION

8.1 Standby Function

The standby function is a function for decreasing the system's power consumption. Two standby modes available: HALT mode and STOP mode.

Set the HALT mode using the HALT instruction and the STOP mode using the STOP instruction.

(1) HALT mode

In this mode, the CPU operation clock is stopped. Average power consumption can be reduced by intermittent operation combining this mode with the normal operation mode.

(2) STOP mode

In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Caution When switching to STOP mode, be sure to execute the STOP instruction after stopping peripheral hardware operations.

Table 8-1. HALT Mode Operating States

Item		HALT Mode Operating State
System clock		System clock oscillation is enabled Clock supply to CPU is stopped
CPU		Operation stopped
EEPROM		Operation enabled[Note]
Ports (output latch)		Maintain state before HALT mode was set
8-bit timer/event counter	TM30	Operation enabled
	TM40	Operation enabled
Watchdog timer		Operation enabled
Power-on-clear circuit	POC	Operation enabled
	LVI	Operation enabled
Bit sequential buffer		Operation enabled
Key return circuit		Operation stopped

Note HALT mode can be set after executing a write instruction.

Table 8-2. STOP Mode Operating States

Item		STOP Mode Operating State
System clock		System clock oscillation is stopped Clock supply to CPU is stopped
CPU		Operation stopped
EEPROM		Operation stopped
Ports (output latch)		Maintain state at time STOP mode was set
8-bit timer/event counter	TM30	Operation enabled[Note 1]
	TM40	Operation enabled[Note 2]
Watchdog timer		Operation stopped
Power-on-clear circuit	POC	Operation enabled
	LVI	Operation stopped
Bit sequential buffer		Operation enabled[Note 3]
Key return circuit		Operation enabled

Notes 1. Operation is enabled only when cascade connected with TM40 (external clock selected for count clock).

2. Operation is enabled only when external clock is selected for count clock.

3. Operation is enabled only when external clock is selected for TM40 count clock and INTTM40 is generated.

8.2 Register That Controls Standby Function (μPD78E9860 Only)Note

The wait time from releasing STOP mode using an interrupt request until oscillation stabilizes is controlled by the oscillation stabilization time selection register (OSTS).

OSTS can be set using an 8-bit memory manipulation instruction.

$\overline{RESET}$ input sets this register to 04H. Note that after $\overline{RESET}$ input the oscillation stabilization time is not $2^{17}/f_X$ but $2^{15}/f_X$.

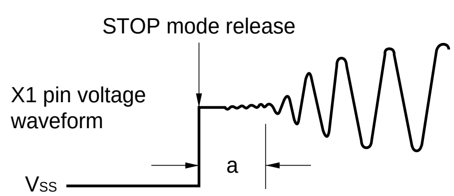
Note There is no OSTS in the μPD78E9861. The oscillation stabilization time of the μPD78E9861 is fixed at $2^7/f_{CC}$.

Figure 8-1. Format of Oscillation Stabilization Time Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	0	$2^{12}/f_X$ (819 μs)
0	1	0	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Other than above			Setting prohibited

Caution For a ceramic/crystal oscillator, the wait time when STOP mode is released does not include the time until clock oscillation begins after $\overline{RESET}$ input or interrupt generation releases STOP mode (a in the figure below).



Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillator)

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

9. RESET FUNCTION

Reset signals are generated by the following three methods.

(1) External reset by $\overline{\text{RESET}}$ signal input
(2) Internal reset by watchdog timer runaway time detection
(3) Internal reset by comparison of POC circuit power supply voltage and detection voltage

An internal reset does not differ functionally from an external reset and both begin program execution at the address written in addresses 0000H and 0001H according to $\overline{\text{RESET}}$ input.

If a low level is input to the $\overline{\text{RESET}}$ pin, a watchdog timer overflow occurs, or the POC circuit detects voltage, a reset occurs and each hardware item enters the state shown in Table 9-1. In addition, during reset input or during the time of oscillation stabilization immediately after reset release, each pin is in a state of high impedance.

If a high level is input to the $\overline{\text{RESET}}$ pin, the reset is released and program execution begins after the oscillation stabilization time elapses. In addition, for a reset by a watchdog timer overflow, the reset is released automatically after reset and program execution begins after the oscillation stabilization time elapses.

Cautions 1. When performing an external reset, input a low level to the $\overline{\text{RESET}}$ pin for at least 10 μs.

2. When releasing STOP mode using a reset, the contents at the time of STOP mode are maintained during reset input. However, port pins become high impedance.

Figure 9-1. Reset Function Block Diagram

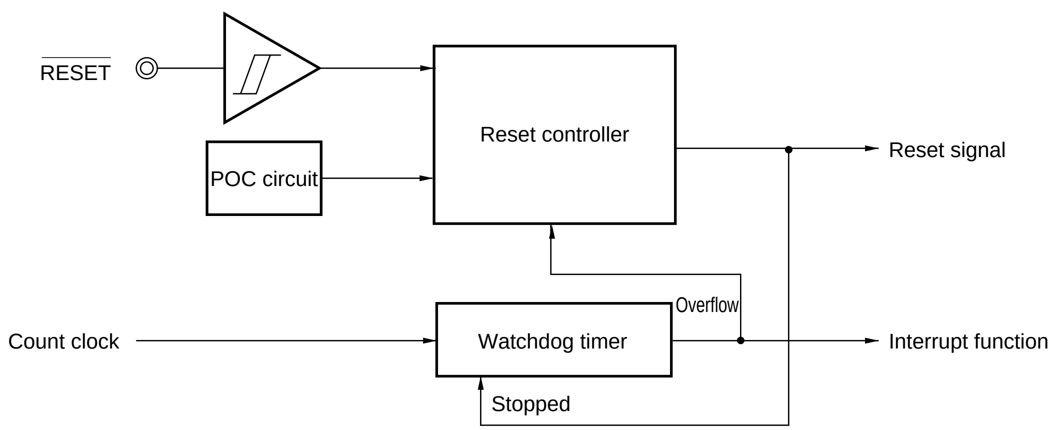


Table 9-1. States of Hardware After Reset

Hardware		State After Reset
Program counter (PC)[Note 1]		Contents of reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
EEPROM (EEWC10)		08H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Ports (P0, P2) (Output latches)		00H
Port mode registers (PM0, PM2)		FFH
Pull-up resistor option registers (PU0, PUB2, PUB3)		00H
Processor clock control register (PCC)		02H
Oscillation stabilization time selection register (OSTS)[Note 3]		04H
8-bit timer/event counter	Timer counters (TM30, TM40)	00H
	Compare registers (CR30, CR40, CRH40)	Undefined
	Mode control registers (TMC30, TMC40)	00H
	Carrier generator output control register (TCA40)	00H
★ Watchdog timer	Timer clock select register 2 (TCL2)	00H
	Mode register (WDTM)	00H
Power-on-clear circuit	Power-on-clear register (POCF1)	00H[Note 4]
	Low-voltage detection register (LVIF1)	00H
	Low-voltage detection level selection register (LVIS1)	00H
Bit sequential buffer	Data registers (BSFRL10, BSFRH10)	Undefined
	Output control register (BSFC10)	00H
Interrupts	Request flag register (IF0)	00H
	Mask flag register (MK0)	FFH

Notes 1. Among the hardware, only the contents of the PC are in an undefined state during reset input and during an oscillation stabilization time wait. For all other hardware, the state is the same as the state after a reset.

2. The state after a reset in standby mode is maintained.

3. μPD78E9860 only.

4. This value is 04H only after a power-on-clear reset.

10. EEPROM (PROGRAM MEMORY)

The on-chip program memory in the μPD78E9860 and 78E9861 is EEPROM.

This section describes the functions of the EEPROM incorporated in the program memory area. For the EEPROM incorporated in data memory, refer to **5. EEPROM (DATA MEMORY)**.

EEPROM can be written with the μPD78E9860 and 78E9861 mounted on the target system (on-board). Connect the dedicated flash writer (Flashpro III (part no. FL-PR3, PG-FP3)) to the host machine and target system to write to EEPROM.

Remark FL-PR3 is made by Naito Densei Machida Mfg. Co., Ltd.

10.1 Selecting Communication Mode

EEPROM is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 10-1. To select a communication mode, use the format shown in Figure 10-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 10-1.

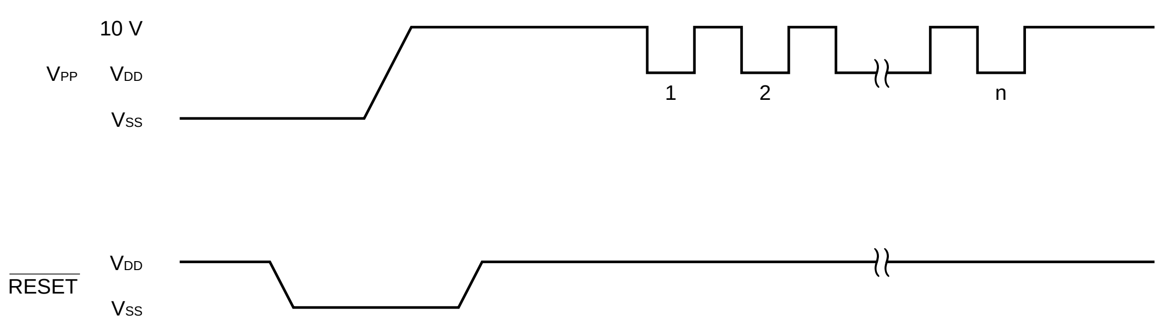
Table 10-1. Communication Mode

Communication Mode	Pins Used	Number of V_{PP} Pulses
Pseudo 3-wire[Note]	P00 (serial clock input) P01 (serial data output) P02 (serial data input)	12

Note Serial transfer is performed by controlling ports by software.

Caution Be sure to select a communication mode depending on the V_{PP} pulse number shown in Table 10-2.

Figure 10-1. Communication Mode Selection Format



10.2 Function of Flash Memory Programming

By transmitting/receiving commands and data in the selected communication mode, operations such as writing to the flash memory are performed. Table 10-2 shows the major functions of flash memory programming.

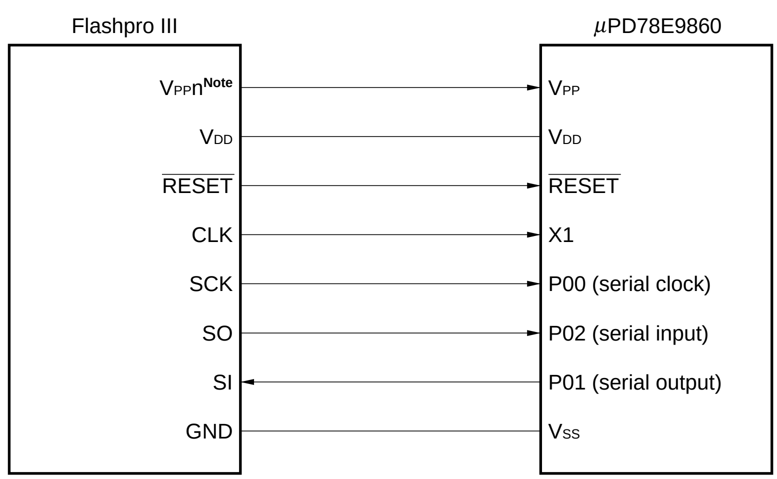
Table 10-2. Functions of Flash Memory Programming

Function	Description
Batch erase	Erases all contents of memory
Batch blank check	Checks erased state of entire memory
Data write	Writes to flash memory based on write start address and number of data written (number of bytes)
Batch verify	Compares all contents of memory with input data

10.3 Flashpro III Connection Example

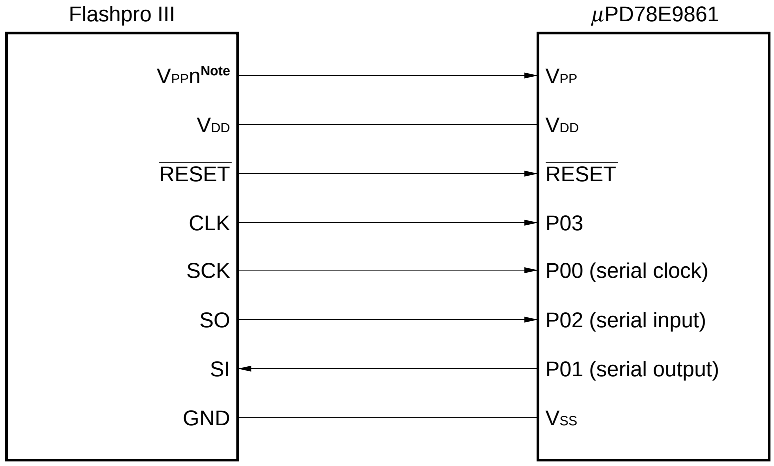
Figures 10-2 and 10-3 show the connection of the Flashpro III and μPD78E9860 or 78E9861.

Figure 10-2. Flashpro III Connection Example in Pseudo 3-Wire Mode (μPD78E9860)



Note n = 1, 2

Figure 10-3. Flashpro III Connection Example in Pseudo 3-Wire Mode (μPD78E9861)



Note n = 1, 2

10.4 Example of Settings for Flashpro III (PG-FP3)

Make the following settings when writing to flash memory using Flashpro III (PG-FP3).

<1> Load the parameter file.
<2> Select the serial mode and serial clock using the type command.
<3> An example of settings for the PG-FP3 is shown below.

Table 10-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		Number of V_{PP} Pulses[Note]
Pseudo 3-wire	COMM PORT	Port A	12
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1 kHz	

Note The number of V_{PP} pulses supplied from Flashpro III when serial communication is initialized. The pins to be used for communication are determined according to the number of these pulses.

Remark COMM PORT: Selection of serial port
SIO CLK: Selection of serial clock frequency
CPU CLK: Selection of source of CPU clock to be input

11. INSTRUCTION SET SUMMARY

This section lists the μPD78E9860 and μPD78E9861 instruction set.

11.1 Conventions

11.1.1 Operand identifiers and description methods

Operands are described in the Operand column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and symbols, #, !, $ and [ ] are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $, [ ] and symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 11-1. Operand Identifiers Forms and Description Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH immediate data or label
saddrp	FE20H to FF1FH immediate data or label (Even numbered addresses only)
addr16	0000H to FFFFH immediate data or label
	(Even numbered addresses only if a 16-bit data transfer instruction)
addr5	0040H to 007FH immediate data or label (Even numbered addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

Remark Refer to **Table 4-1 List of Special Function Registers** for special function register symbols.

11.1.2 Explanation of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt processing flag
( ) : Contents of memory represented by contents of register or address in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
——: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

11.1.3 Explanation of flags column

(blank): No change
0: Cleared to 0
1: Set to 1
×: Set or cleared according to result
R: Previously saved value is stored

11.2 List of Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	AC	CY
MOV	r. #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r[Note 1]	2	4	A ← r			
	r, A[Note 1]	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ←→ X			
	A, r[Note 2]	2	6	A ←→ r			
	A, saddr	2	6	A ←→ (saddr)			
	A, sfr	2	6	A ←→ (sfr)			
	A, [DE]	1	8	A ←→ (DE)			
	A, [HL]	1	8	A ←→ (HL)			
	A, [HL + byte]	2	8	A ←→ (HL+byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp[Note 3]	1	4	AX ← rp			
	rp, AX[Note 3]	1	4	rp ← AX			

Notes 1. Except r = A

2. Except r = A, X

3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP -– 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z AC CY
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC_H ← A, PC_L ← X	
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A.bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW.bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set Stop Mode	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{PP}		–0.3 to +10.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total of all pins	80	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

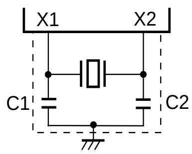
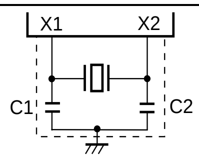
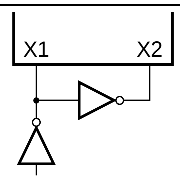
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum rating are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions the ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics

Ceramic or crystal oscillation (μPD78E9860)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2				30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width(t_{XH},t_{XL})		85		500	ns

Notes. 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

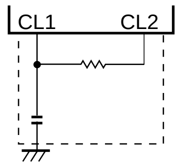
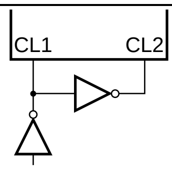
Caution When using a ceramic or crystal oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

RC oscillation (μPD78E9861)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})Notes 1,2	V_{DD} = Oscillation voltage range	0.85		1.15	MHz
External clock		CL1 input frequency (f_{CC})Note 1		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH},t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Variations due to external resistance and external capacitance are not included.

Caution When using an RC oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin				2.5	mA
		All pins				5.0	mA
Output current, high	I_{OH}	Per pin				–0.5	mA
		All pins				–5.0	mA
Input voltage, high	V_{IH1}	P00 to P07	$2.7 \le V_{DD} \le 3.6$ V	$0.7V_{DD}$		V_{DD}	V
			$1.8 \le V_{DD} < 2.7$ V	$0.9V_{DD}$		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P20, P21, P40 to P43	$2.7 \le V_{DD} \le 3.6$ V	$0.8V_{DD}$		V_{DD}	V
			$1.8 \le V_{DD} < 2.7$ V	$0.9V_{DD}$		V_{DD}	V
	V_{IH3}	X1, X2 (CL1, CL2)		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07	$2.7 \le V_{DD} \le 3.6$ V	0		$0.3V_{DD}$	V
			$1.8 \le V_{DD} < 2.7$ V	0		$0.1V_{DD}$	V
	V_{IL2}	$\overline{RESET}$, P20, P21, P40 to P43	$2.7 \le V_{DD} \le 3.6$ V	0		$0.2V_{DD}$	V
			$1.8 \le V_{DD} < 2.7$ V	0		$0.1V_{DD}$	V
	V_{IL3}	X1, X2 (CL1, CL2)		0		V_{DD} – 0.1	V
Output voltage, high	V_{OH1}	P00 to P07, P20, P21	I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH2}		I_{OH} = –500 μA	V_{DD} – 0.7			V
Output voltage, low	V_{OL1}	P00 to P07, P20, P21	I_{OL} = 400 μA			0.5	V
	V_{OL2}		I_{OL} = 2.5 mA			0.7	V
Input leakage current, high	L_{LIH1}	$V_I = V_{DD}$	Pins other than X1, X2 (CL1, CL2)			3	μA
	L_{LIH2}		X1, X2 (CL1, CL2)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than X1, X2 (CL1, CL2)			–3	μA
	I_{LIL2}		X1, X2 (CL1, CL2)			–20	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

2. The parenthesized pin names apply to the μPD78E9861.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note] Ceramic/crystal oscillation: μPD78E9860	I_{DD1}	4.19 MHz crystal oscillation operating mode (EEPROM (data memory) halted) $C_1 = C_2$ = 22 pF	V_{DD} = 3.6 V		4.55	5.0	mA
	I_{DD2}	4.19 MHz crystal oscillation HALT mode (EEPROM (data memory) halted) $C_1 = C_2$ = 22 pF	V_{DD} = 3.6 V		0.4	0.6	mA
	I_{DD3}	STOP mode (POC operating)	V_{DD} = 3.6 V		2.0	3.0	μA
			V_{DD} = 3.0 V T_A = –20 to +75°C		Undefined	Undefined	μA
	I_{DD4}	STOP mode (POC operation halted)	V_{DD} = 3.0 V T_A = –20 to +75°C			Undefined	μA
Power supply current[Note] RC oscillation: μPD78E9861	I_{DD1}	1.0 MHz RC oscillation operating mode (EEPROM (data memory) halted) R = 22 kΩ, C = 27 pF	V_{DD} = 3.6 V		4.95	5.5	mA
	I_{DD2}	1.0 MHz RC oscillation HALT mode (EEPROM (data memory) halted) R = 22 kΩ, C = 27 pF	V_{DD} = 3.6 V		0.8	1.0	mA
	I_{DD3}	STOP mode (POC operating)	V_{DD} = 3.6 V		2.0	3.0	μA
			V_{DD} = 3.0 V T_A = –20 to +75°C		Undefined	Undefined	μA
	I_{DD4}	STOP mode (POC operation halted)	V_{DD} = 3.0 V T_A = –20 to +75°C			Undefined	μA

Note Port current (including current flowing in on-chip pull-up resistors) is not included. This current will be further added to when writing to or reading from EEPROM (data memory). For the specific current values, refer to **EEPROM (Data Memory) Characteristics**.

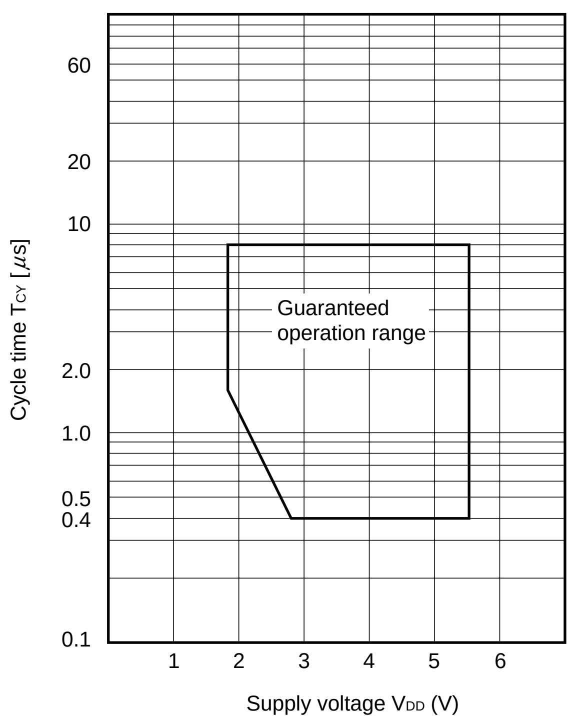
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85 °C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 3.6 V	0.4		8	μs
			1.6		8	μs
TMI input input frequency	f_{TI}	2.7 ≤ V_{DD} ≤ 3.6 V	0		4.0	MHz
		1.8 ≤ V_{DD} < 2.7 V	0		500	kHz
TMI high-/low-level width	t_{TIH}, t_{TIL}	2.7 ≤ V_{DD} ≤ 3.6 V	0.1			μs
		1.8 ≤ V_{DD} < 2.7 V	1.0			μs
Key return input pin low-level width	t_{KRIL}	KR10 to KR13	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD} (System Clock: Ceramic/Crystal Oscillation)

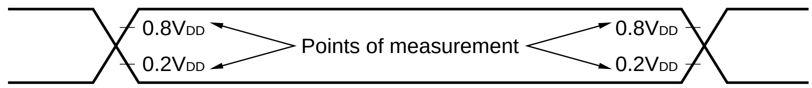


(2) RC frequency oscillation characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

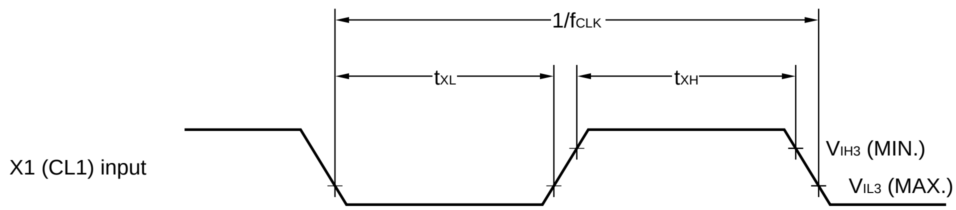
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency[Note]	f_{CC}	R = undefined, C = undefined	0.85		1.15	MHz

Note Variations due to external resistance and external capacitance are not included.

AC Timing Measurement Points (Excluding X1 Input)

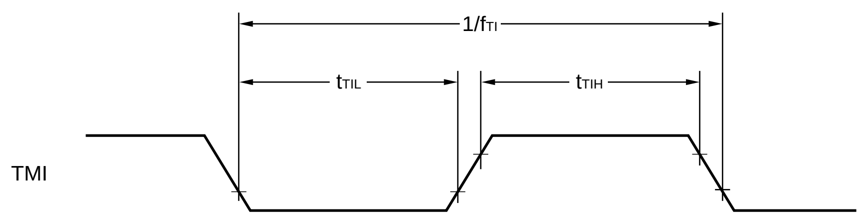


Clock Timing

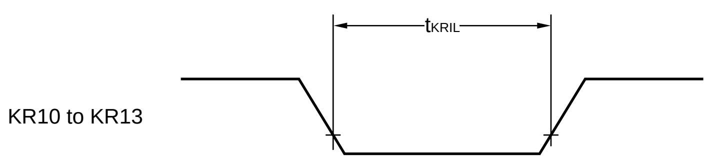


Remark f_{CLK}: f_X or f_{CC}

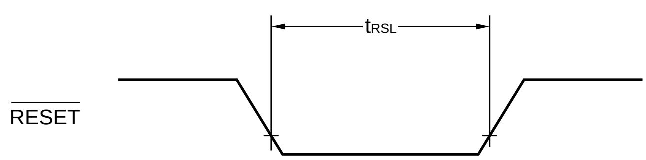
TMI Timing



Key Return Input Timing



$\overline{\text{RESET}}$ Input Timing



Power-on-Clear Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

(1) POC

(a) DC characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}	Response time[Note]: 2 ms	1.8	1.9	2.0	V

Note Time from detecting voltage until output reverses and time until stable operation after transition from halted state to operating state.

(b) AC characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power rise time	T_{Pth1}	V_{DD}: 0 → 1.8 V	0.01		100	ms
	T_{Pth2}	V_{DD}: 0 → 1.8 V T_A = +25°C	10		Undefined	μs

(2) LVI

(a) DC characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LVI7 detection voltage	V_{LVI7}	Response time[Note 1]: 2 ms	2.4	2.6	2.8	V
LVI6 detection voltage	V_{LVI6}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI5 detection voltage	V_{LVI5}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI4 detection voltage	V_{LVI4}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI3 detection voltage	V_{LVI3}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI2 detection voltage	V_{LVI2}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI1 detection voltage	V_{LVI1}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI0 detection voltage	V_{LVI0}	Response time[Note 1]: 2 ms	**Note 3**	2.0	2.2	V

Notes 1. Time from detecting voltage until output reverses and time until stable operation after transition from halted state to operating state

2. Relative relationship: $V_{LVI7} > V_{LVI6} > V_{LVI5} > V_{LVI4} > V_{LVI3} > V_{LVI2} > V_{LVI1} > V_{LVI0}$

3. $V_{POC} < V_{LVI0}$

EEPROM (Data Memory) Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

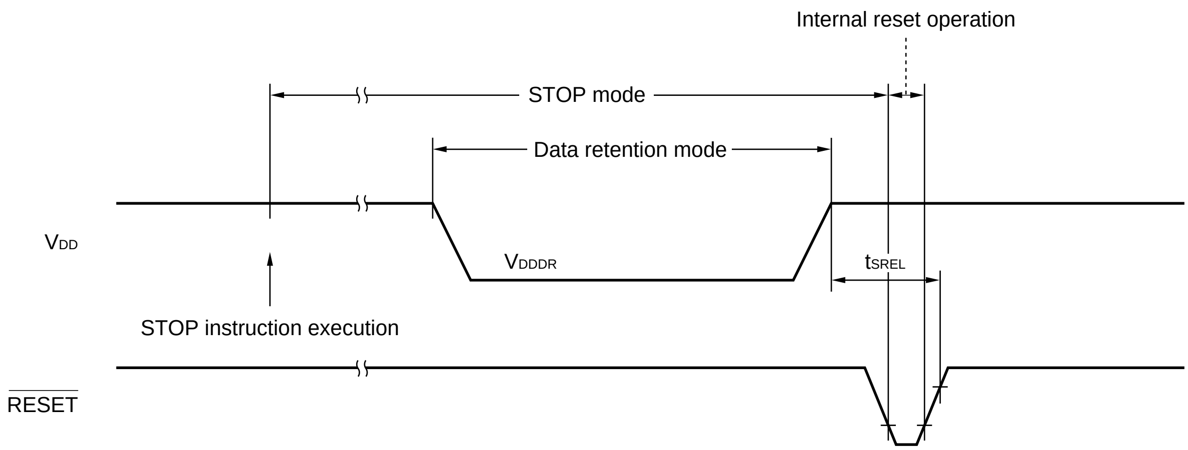
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Write time[Note 1]				3.3		6.6	ms
No. of overwrites		Per byte				10	10,000 times
Write voltage				2.0		3.6	V
		T_A = Undefined		1.8		3.6	V
Read voltage				1.8		3.6	V
Power supply current		ERE10[Note 2] = 1, EWE10[Note 3] = 1	V_{DD} = 3.0 V ±10%		0.3[Notes 4, 6]	Undefined	mA
			V_{DD} = 2.0 V ±10%		0.1[Notes 5, 7]	Undefined	mA
		ERE10[Note 2] = 1, EWE10[Note 3] = 0	V_{DD} = 3.0 V ±10%		0.27[Note 6]	Undefined	mA
			V_{DD} = 2.0 V ±10%		0.09[Note 7]	Undefined	mA
		ERE10[Note 2] = 0, EWE10[Note 3] = 0 or STOP mode	V_{DD} = 1.8 V to 3.6 V		0	1	μA

Notes
1. Write time = T × 145 (T = time of 1 clock cycle selected by EWCS100 to EWCS102)
2. Bit 2 of EEPROM write control register 10 (EEWC10)
3. Bit 0 of EEWC10
4. A further 0.7 mA (TYP.) current flows during a write operation.
5. A further 0.9 mA (TYP.) current flows during a write operation.
6. A further 0.9 mA (TYP.) current flows during a read operation.
7. A further 0.3 mA (TYP.) current flows during a read operation.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		3.6	V
Release signal set time	t_{SREL}	STOP release by $\overline{\text{RESET}}$ pin	10			μs

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



★ **Oscillation Stabilization Wait Time (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)**

(a) Ceramic/crystal oscillator (μPD78E9860)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation wait time[Note 1]		STOP release by $\overline{\text{RESET}}$ or reset release by POC		$2^{15}/f_X$		s
		Release by interrupt		**Note 2**		s

Notes 1. Time required to stabilize oscillation after a reset or STOP mode release.

2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected using bits 0 to 2 of the oscillation stabilization time selection register (OSTS0 to OSTS2).

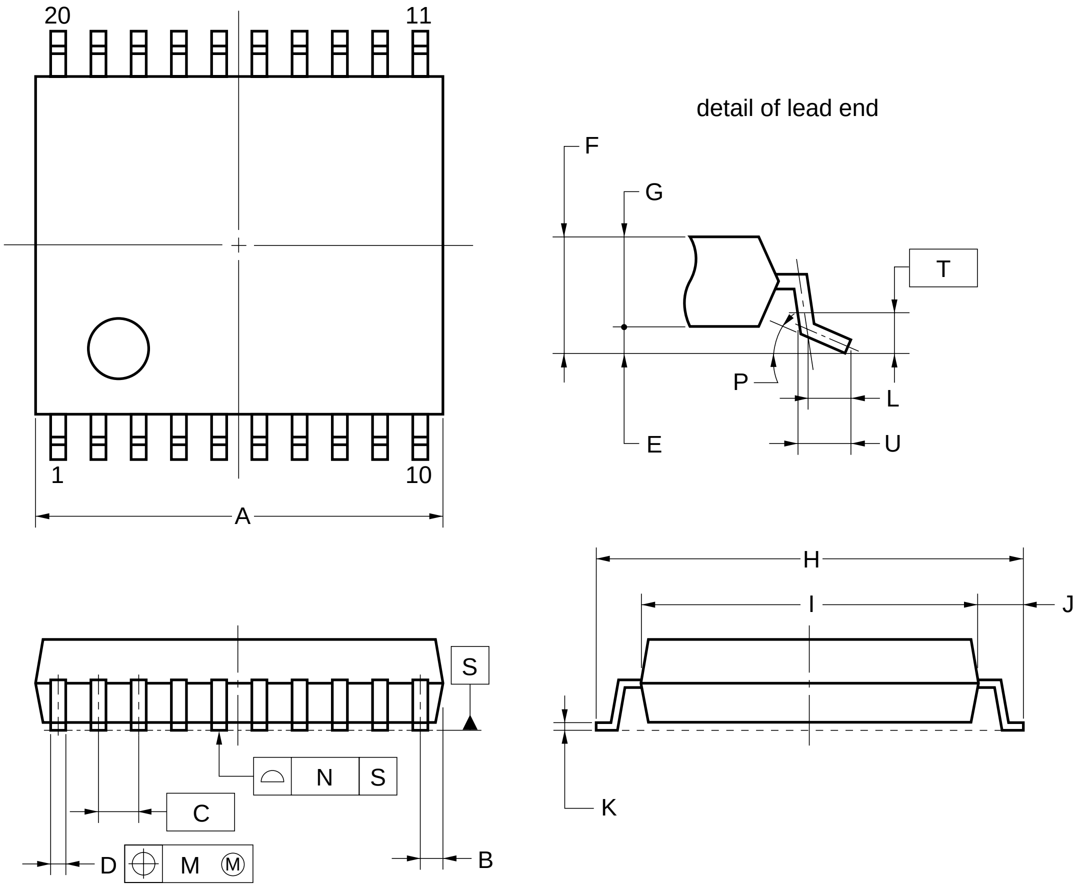
(b) RC oscillation (μPD78E9861)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation wait time[Note]		STOP release by $\overline{\text{RESET}}$ or reset release by POC		$2^{7}/f_{CC}$		s
		Release by interrupt		$2^{7}/f_{CC}$		s

Note Time required to stabilize oscillation after a reset or STOP mode release.

13. PACKAGE DRAWING

20-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

S20MC-65-5A4-2

APPENDIX A. DIFFERENCES BETWEEN EEPROM PRODUCTS AND MASK ROM PRODUCTS

The μPD78E9860 and 78E9861 incorporate EEPROM in place of the internal ROM of the mask ROM products, the μPD789860 and 789861, respectively. Table A-1 shows differences between EEPROM products and mask ROM products.

Table A-1. Differences Between EEPROM Products and Mask ROM Products

Item		EEPROM Products		Mask ROM Products	
		μPD78E9860	μPD78E9861	μPD789860	μPD789861
Program memory	ROM organization	EEPROM		Mask ROM	
	ROM capacity	4 KB			
Data memory	High-speed RAM capacity	128 bytes			
	EEPROM	32 bytes			
System clock		Ceramic/crystal oscillation	RC oscillation	Ceramic/crystal oscillation	RC oscillation
Pull-up resistor		None		4 (specified by the mask option)	
Power-on-clear circuit		POC switching circuit only		POC always on/always off/ switching circuit is selectable (specified by the mask option)	
V_{PP} pin		Yes		None	
IC pin		None		Yes	
Electrical specifications		EEPROM products may differ from mask ROM products.			

Caution There are differences in the amount of noise tolerance and noise radiation between flash memory versions and mask ROM versions. When considering changing from a flash memory version to a mask ROM version during the process from experimental manufacturing to mass production, make sure to sufficiently evaluate commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78E9860 and μPD78E9861.

Language Processing Software

RA78K0S Notes 1, 2, 3	Assembler package common to 78K/0S Series
CC78K0S Notes 1, 2, 3	C compiler package common to 78K/0S Series
CC78K0S-L Notes 1, 2, 3	C compiler source file common to 78K/0S Series
DF789861 Notes 1, 2, 3	Device file for μPD789860, 789861 Subseries

Flash Memory Writing Tools

Flashpro III (Type FL-PR3 Note 4, PG-FP3)	Flash programmer dedicated to microcontrollers with on-chip flash memory (EEPROM)
FA-20MC Note 4	Flash memory (EEPROM) writing adapter for 20-pin plastic SSOP (MC-5A4 type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator used to debug hardware and software when developing an application system using the 78K/0S Series. It corresponds to the integrated debugger (ID78K0S-NS). It is used in combination with an AC adapter, emulation probe, and interface adapter for connecting to a host machine.
IE-70000-MC-PS-B AC adapter	Adapter for providing power from a 100 to 240 V AC
IE-70000-98-IF-C Interface adapter	Adapter required when using a PC-9800 series (except a notebook type) as the IE-78K0S-NS host machine (C bus supported)
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when using a notebook type as the IE-78K0S-NS host machine (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter	Adapter required when using an IBM PC/AT™ or compatibles as the IE-78K0S-NS host machine (ISA bus supported)
IE-70000-PCI-IF Interface adapter	Adapter that is needed when using a personal computer in which a PCI bus is implemented as the IE-78K0S-NS host machine
★ IE-789860-NS-EM1 Note 5 Emulation board	Board for emulating the peripheral hardware of a device. It is used in combination with the in-circuit emulator.
NP-20MC Emulation probe	Probe to connect a target system to the in-circuit emulator. It is for a 20-pin plastic SSOP (MC-5A4 type).
SM78K0S Notes 1, 2	System emulator common to 78K/0S Series
DF789861 Notes 1, 2	Device file for μPD789860, 789861 Subseries

Real-Time OS

MX78K0S Notes 1, 2	OS for 78K/0S Series

Notes 1. PC-9800 Series (Japanese Windows) based

2. IBM PC/AT or compatibles (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based

4. Products of Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.

5. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789860.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.	
	English	Japanese
μPD789860, 789861 Preliminary Product Information	U13917E	U13917J
μPD78E9860, 78E9861 Preliminary Product Information	U14385E	U14385J
μPD789860, 789861 Subseries User's Manual	To be prepared	To be prepared
78K/0S Series User's Manual Instructions	U11047E	U11047J
78K/0 78K/0S Series Application Note Flash Memory Write	U14558E	U14558J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K0S Assembler Package	Operation	U11622E	U11622J
	Assembly Language	U11599E	U11599J
	Structured Assembly Language	U11623E	U11623J
CC78K0S C Compiler	Operation	U11816E	U11816J
	Language	U11817E	U11817J
SM78K0S System Simulator Windows Based	Reference	U11489E	U11489J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901E	U12901J
IE-78K0S-NS In-circuit Emulator		U13549E	U13549J
IE-789860-NS-EM1 Emulation Board		To be prepared	To be prepared

Document Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		English	Japanese
78K/0S Series OS MX78K0S	Fundamental	U12938E	U12938J

Other Documents

Document Name	Document No.	
	English	Japanese
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer — Related Products by Third Party	—	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

These products are manufactured and sold on a license contract with CP8 Transac regarding the EEPROM microcontroller patent.
These products cannot be used for an IC card (SMART CARD).

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
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800-729-9288

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Fax: 01908-670-290

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J99.1

Phase-out/Discontinued