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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD78P4916

16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78P4916 is one of the μPD784915 subseries in the 78K/IV Series microcontrollers which incorporate a high-speed and high-performance 16-bit CPU.

The μPD78P4916 replaces mask ROM with one-time PROM and increases on-chip ROM and RAM capacity compared to the μPD784915.

It is suitable for evaluation at system development and for small quantity production.

Detailed descriptions of functions are provided in the following user's manuals. Be sure to read these documents when designing.

μPD784915 Subseries User's Manual – Hardware : U10444E
78K/IV Series User's Manual – Instruction : U10905E

FEATURES

○ High-speed instruction execution using 16-bit CPU core
- Minimum instruction execution time: 250 ns (at 8-MHz internal clock)

○ On-chip high capacity memory
- PROM : 62 Kbytes **Note**
- RAM : 2048 bytes **Note**

Note It is possible to change the capacity of the internal PROM and the internal RAM by specifying the internal memory capacity select (IMS) register.

ORDERING INFORMATION

Part Number	Package
μPD78P4916GF-3BA	100-pin plastic QFP (14 × 20 mm)

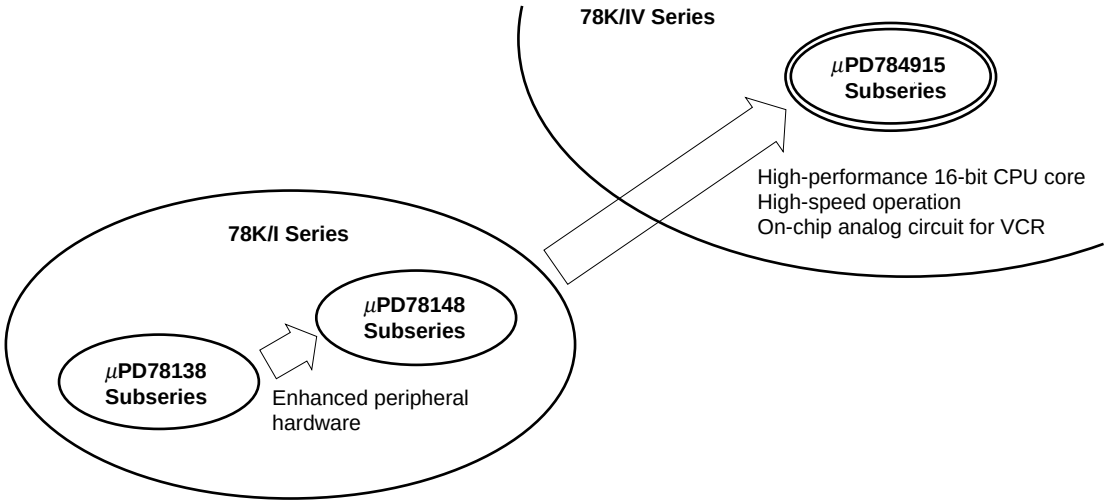
The information in this document is subject to change without notice.

Document No. U11045EJ1V0DS00 (1st edition)
Date Published April 1996 P
Printed in Japan

The mark * shows major revised points.

Phase-out/Discontinued

78K/IV Series Products



Function List (1/2)

<table>
<tr><th colspan="2">Item</th><th>Function</th></tr>
<tr><td colspan="2">Internal PROM capacity</td><td>62 Kbytes Note</td></tr>
<tr><td colspan="2">Internal RAM capacity</td><td>2048 bytes Note</td></tr>
<tr><td colspan="2">Operation clock</td><td>16 MHz (Internal clock: 8 MHz)
Low frequency oscillation mode: 8 MHz (Internal clock: 8 MHz)
Low power consumption mode: 32.768 kHz (Subsystem clock)</td></tr>
<tr><td colspan="2">Minimum instruction execution time</td><td>250 ns (at 8-MHz internal clock)</td></tr>
<tr><td colspan="2">I/O ports</td><td>Total: 54 Input: 8
I/O: 46</td></tr>
<tr><td colspan="2">Real-time output port</td><td>11 (including 3 outputs each for Pseudo-VSYNC, Head amplifier switch, and Chrominance rotate)</td></tr>
<tr><td rowspan="5">Super timer unit</td><td>Timer/counter</td><td>
<table>
<tr><th>Timer/counter</th><th>Compare register</th><th>Capture register</th><th>Remark</th></tr>
<tr><td>TM0 (16-bit)</td><td>3</td><td>–</td><td></td></tr>
<tr><td>TM1 (16-bit)</td><td>3</td><td>1</td><td></td></tr>
<tr><td>FRC (22-bit)</td><td>–</td><td>6</td><td></td></tr>
<tr><td>TM3 (16-bit)</td><td>2</td><td>1</td><td></td></tr>
<tr><td>UDC (5-bit)</td><td>1</td><td>–</td><td></td></tr>
<tr><td>EC (8-bit)</td><td>4</td><td>–</td><td>Generates HSW signal</td></tr>
<tr><td>EDV (8-bit)</td><td>1</td><td>–</td><td>Divides CFG signal</td></tr>
</table>
</td></tr>
<tr><td>Capture register</td><td>
<table>
<tr><th>Input signal</th><th>Number of bits</th><th>Measurement cycle</th><th>Operation edge</th></tr>
<tr><td>CFG</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr>
<tr><td>DFG</td><td>22</td><td>125 ns to 524 ms</td><td>↑</td></tr>
<tr><td>HSW</td><td>16</td><td>1 μs to 65.5 ms</td><td>↑ ↓</td></tr>
<tr><td>VSYNC</td><td>22</td><td>125 ns to 524 ms</td><td>↑</td></tr>
<tr><td>CTL</td><td>16</td><td>1 μs to 65.5 ms</td><td>↑ ↓</td></tr>
<tr><td>TREEL</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr>
<tr><td>SREEL</td><td>22</td><td>125 ns to 524 ms</td><td>↑ ↓</td></tr>
</table>
</td></tr>
<tr><td>Special circuit for VCR</td><td>• VSYNC separator, HSYNC separator
• VISS detector, Wide-aspect detector
• Field identifier
• Head amplifier switch/chrominance rotate output circuit</td></tr>
<tr><td>General purpose timer</td><td>
<table>
<tr><th>Timer</th><th>Compare register</th><th>Capture register</th></tr>
<tr><td>TM2 (16-bit)</td><td>1</td><td>–</td></tr>
<tr><td>TM4 (16-bit)</td><td>1 (Capture/compare)</td><td>1</td></tr>
<tr><td>TM5 (16-bit)</td><td>1</td><td>–</td></tr>
</table>
</td></tr>
<tr><td>PWM output</td><td>• 16-bit precision: 3 channels (Carrier frequency: 62.5 kHz)
• 8-bit precision: 3 channels (Carrier frequency: 62.5 kHz)</td></tr>
<tr><td colspan="2">Serial interface</td><td>3-wire serial I/O: 2 channels
• BUSY/STRB control available (only 1 channel)</td></tr>
<tr><td colspan="2">A/D converter</td><td>8-bit resolution × 12 channels, conversion time: 10 μs</td></tr>
</table>

Note It is possible to change the capacity of the internal PROM and the internal RAM by specifying the internal memory capacity select (IMS) register.

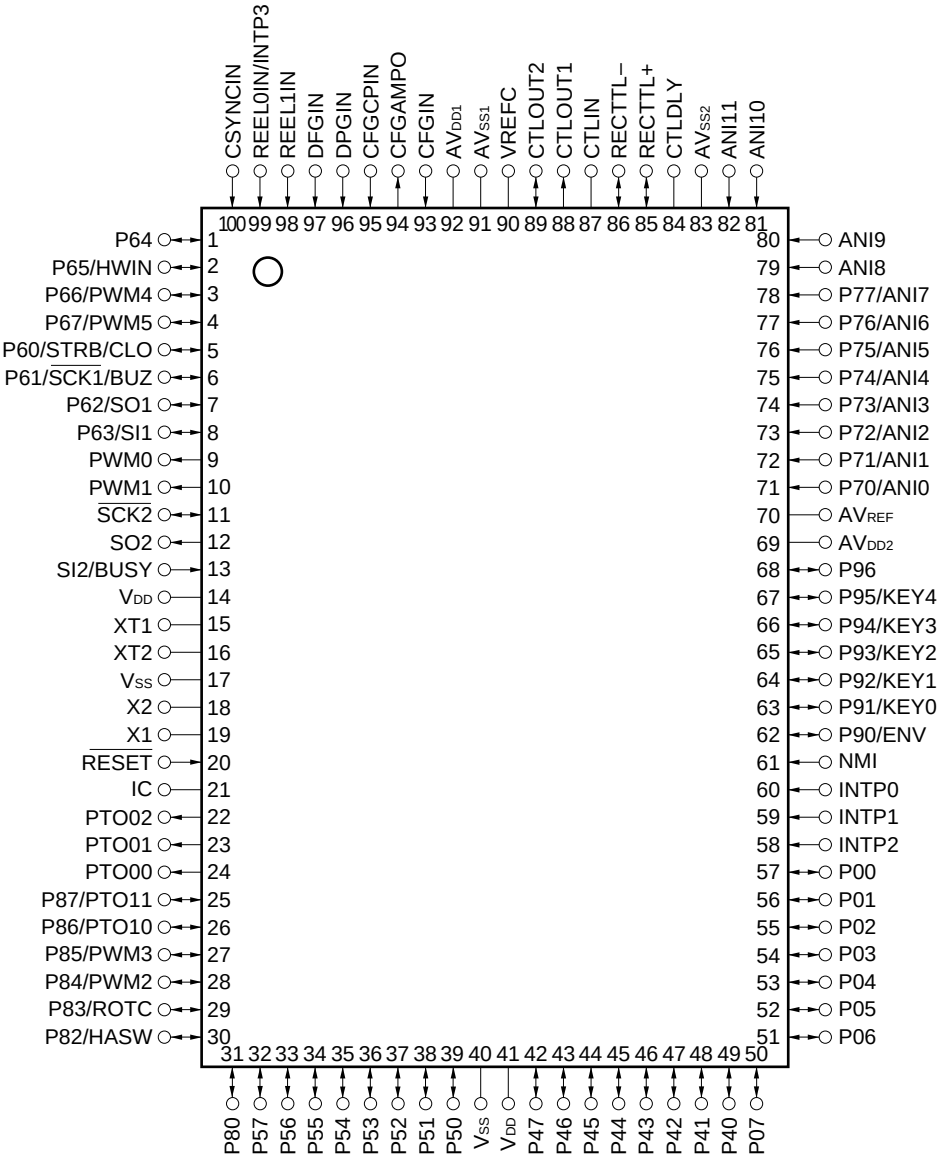
Function List (2/2)

Item		Function
Analog unit		• CTL amplifier • RECCTL driver (supports re-write operation) • DFG amplifier, DPG comparator, CFG amplifier • DPFG separator (Three-value) • Reel FG comparator (2 channels) • CSYNC comparator
Interrupt		Programmable 4 levels, vectored interrupt, macro service, context switching
	External	9 (including NMI)
*	Internal	19 (including software interrupt)
Standby function		HALT mode/STOP mode Low-power consumption mode: HALT mode
		Release from STOP mode by NMI pin's active edge, Watch interrupt (INTW), or INTP1/INTP2/KEY0-KEY4 pins' input.
* Watch function		0.5-sec interval, capable of low-voltage operation (V_{DD} = 2.7 V)
Power supply voltage		V_{DD} = 2.7 to 5.5 V
Package		100-pin plastic QFP (14 × 20 mm)

Pin Configuration (Top View)

(1) Normal Operation Mode

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P4916GF-3BA

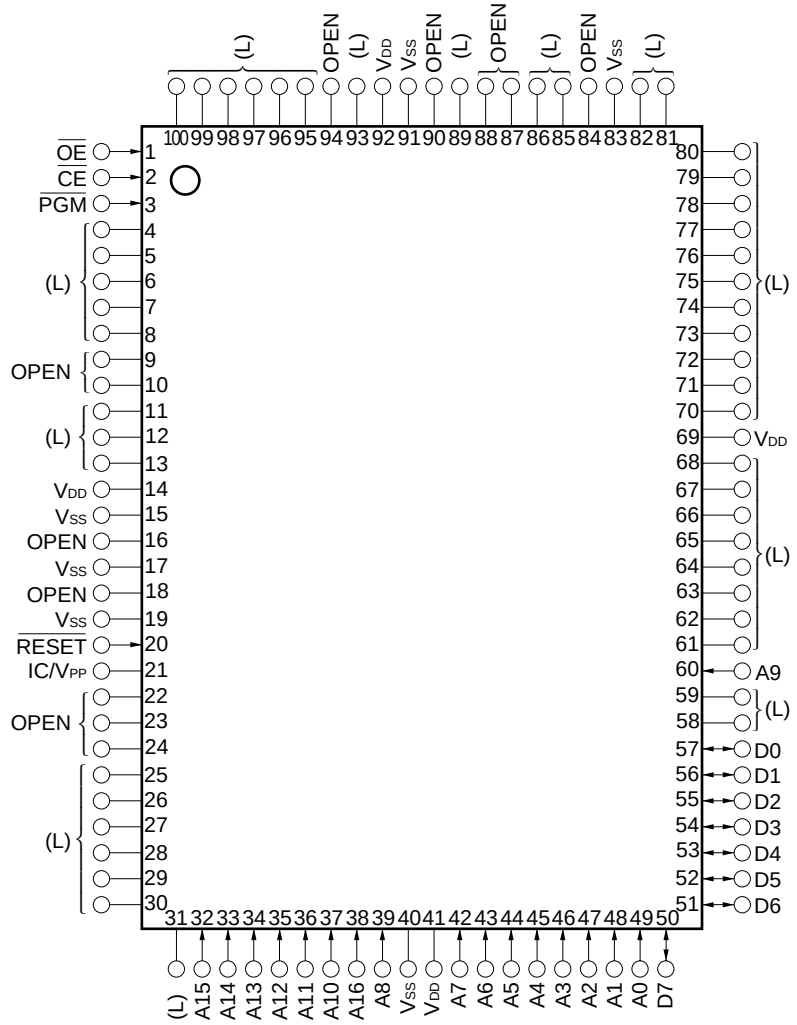


Caution Connect the IC (Internally Connected) pin to V_{SS} directly.

ANI0-ANI11	:	Analog Input
AV_{DD1}, AV_{DD2}	:	Analog Power Supply
AV_{SS1}, AV_{SS2}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
BUSY	:	Serial Busy
BUZ	:	Buzzer Output
CFGAMPO	:	Capstan FG Amplifier Output
CFGCPIN	:	Capstan FG Capacitor Input
CFGIN	:	Analog Unit Input
CLO	:	Clock Output
CSYNCIN	:	Analog Unit Input
CTLDLY	:	Control Delay Input
CTLIN	:	CTL Amplifier Input Capacitor
CTLOUT1, CTLOUT2	:	CTL Amplifier Output
DFGIN	:	Analog Unit Input
DPGIN	:	Analog Unit Input
ENV	:	Envelope Input
HASW	:	Head Amplifier Switch Output
HWIN	:	Hardware Timer External Input
IC	:	Internally Connected
INTP0-INTP3	:	Interrupt From Peripherals
KEY0-KEY4	:	Key Return
NMI	:	Nonmaskable Interrupt
P00-P07	:	Port0
P40-P47	:	Port4
P50-P57	:	Port5
P60-P67	:	Port6
P70-P77	:	Port7
P80, P82-P87	:	Port8
P90-P96	:	Port9
PTO00-PTO02, PTO10, PTO11	:	Programmable Timer Output
PWM0 - PWM5	:	Pulse Width Modulation Output
RECCTL+, RECCTL–	:	RECCTL Output/PBCLT Input
REEL0IN, REEL1IN	:	Analog Unit Input
$\overline{RESET}$	:	Reset
ROTC	:	Chrominance Rotate Output
$\overline{SCK1}$, $\overline{SCK2}$	:	Serial Clock
SI1, SI2	:	Serial Input
SO1, SO2	:	Serial Output
STRB	:	Serial Strobe
V_{DD}	:	Power Supply
VREFC	:	Reference Amplifier Capacitor
Vss	:	Ground
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

(2) PROM Programming Mode

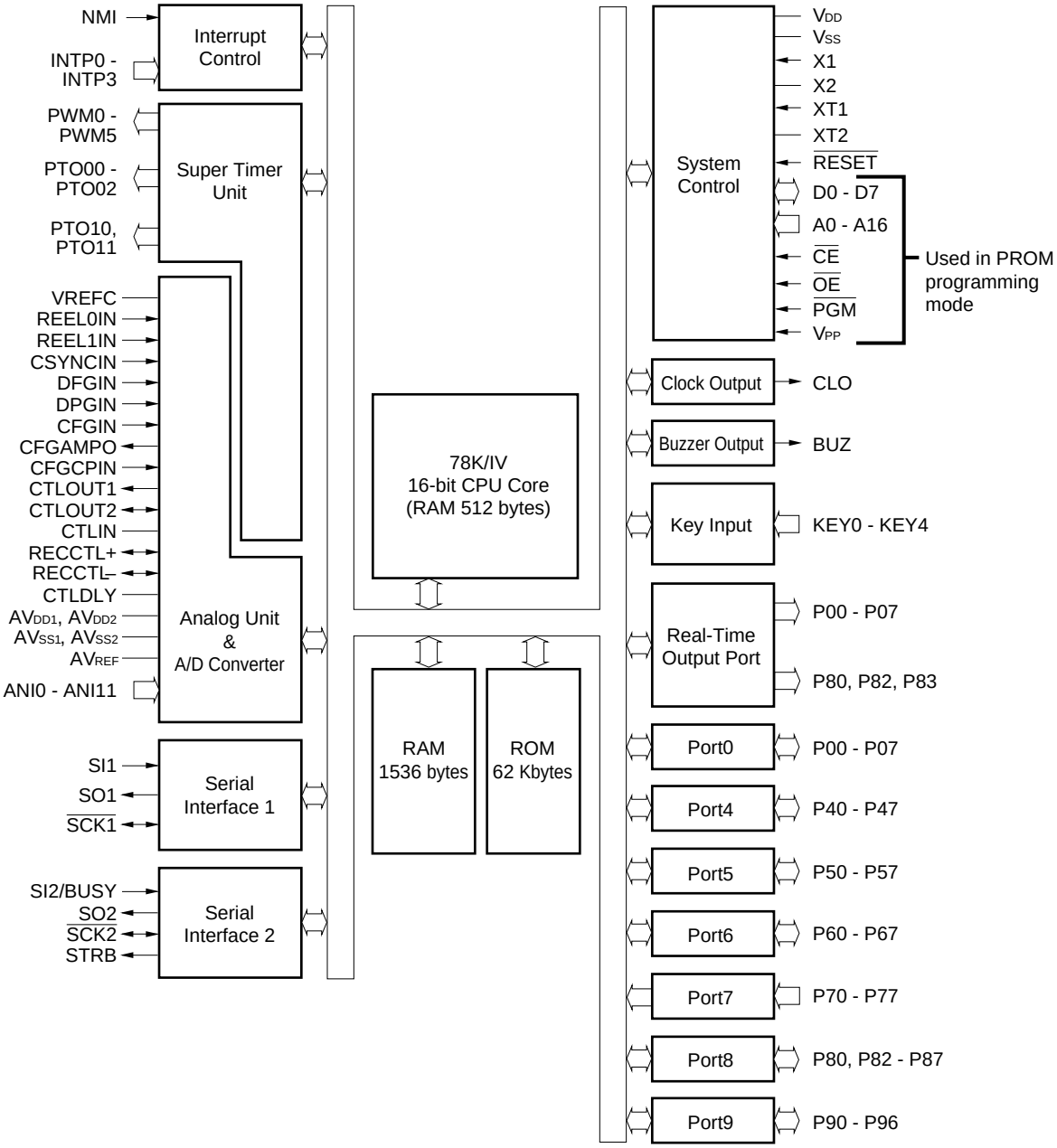
- **100-pin plastic QFP (14 × 20 mm)**
  μPD78P4916GF-3BA



Cautions (L) : Connect to V_{SS} via pull-down resistors individually.
V_{SS} : Connect to ground.
OPEN : Leave this pin unconnected.
$\overline{RESET}$: Apply low level.

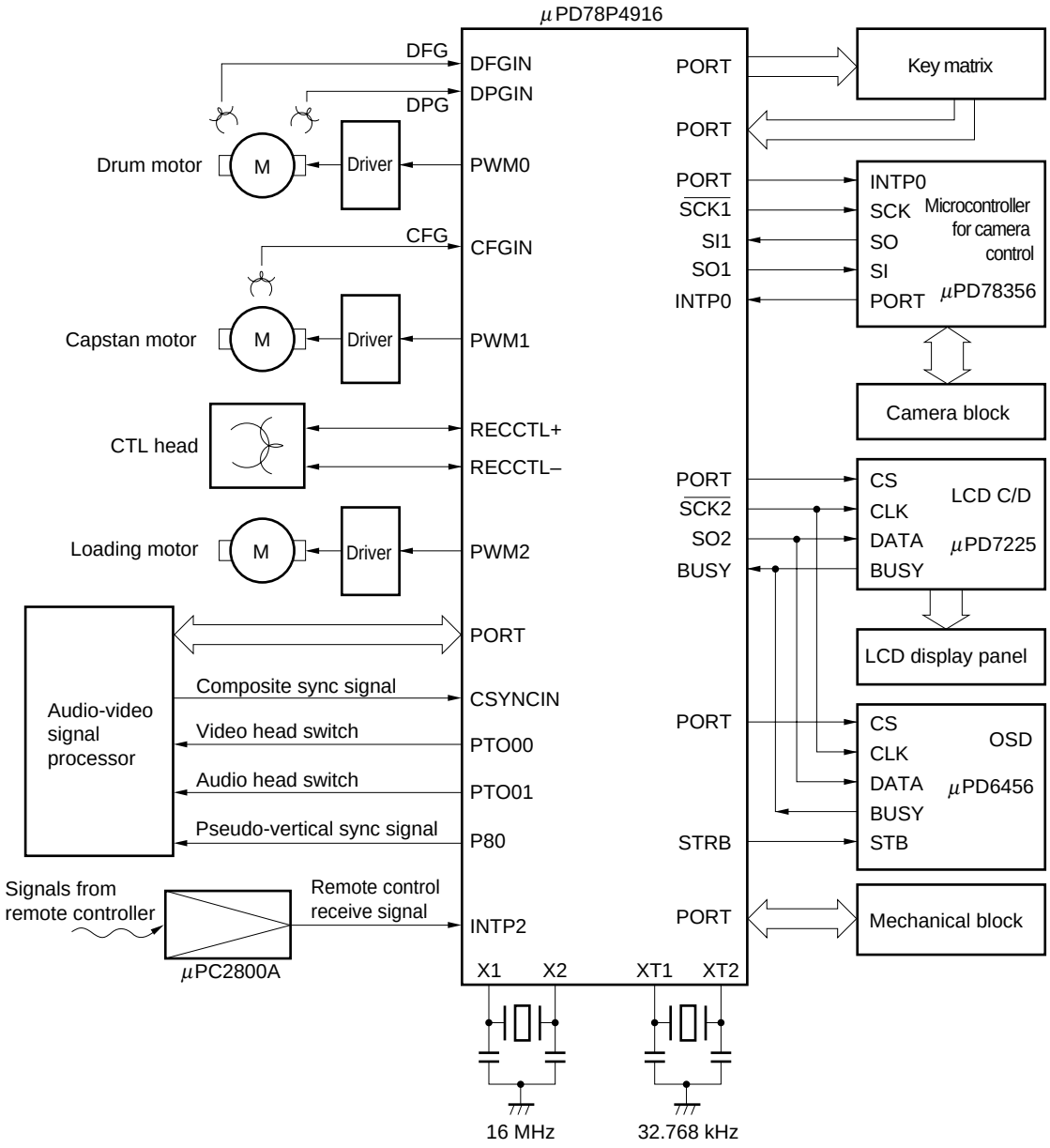
A0 - A16	:	Address Bus	$\overline{RESET}$	:	Reset
D0 - D7	:	Data Bus	V_{DD}	:	Power Supply
$\overline{CE}$	:	Chip Enable	V_{PP}	:	Programming Power Supply
$\overline{OE}$	:	Output Enable	V_{SS}	:	Ground
$\overline{PGM}$	:	Program			

Internal Block Diagram

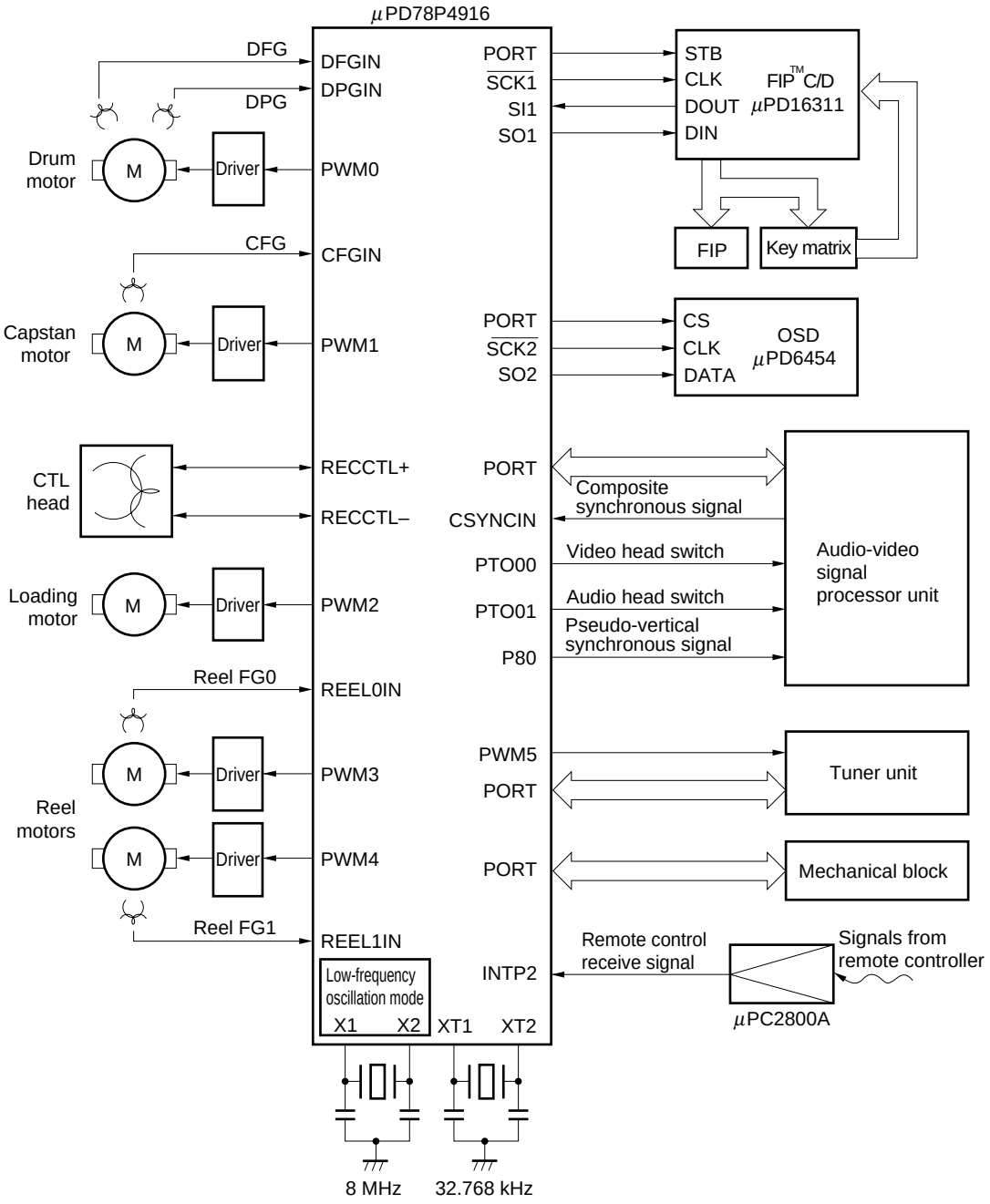


System Configuration Example

- **Camcorder**



- **Deck-type VCR**



Phase-out/Discontinued

CONTENTS

✱ 1. DIFFERENCES BETWEEN μPD78P4916 AND μPD784915, μPD784916A

Other than the memory types, their capacities, and memory-related points, the functions of the three devices are identical: the μPD78P4916 incorporates a one-time PROM that is rewritable by users, while the μPD784915 and 784916A contain mask ROMs.

Table 1-1 shows the differences among these devices. Be sure to keep in mind these differences especially when debugging and pre-producing the application system with the PROM version and then mass-producing it with the mask-ROM version.

For the details about the CPU functions and on-chip hardware, refer to the μPD784915 Subseries User's Manual—Hardware (U10444E).

Table 1-1. Differences among μPD784915 Subseries Devices

Parameters	μPD78P4916	μPD784915	μPD784916A
Internal ROM	One-time PROM	Mask ROM	Mask ROM
	62 Kbytes[Note]	48 Kbytes	62 Kbytes
Internal RAM	2048 bytes[Note]	1280 bytes	1280 bytes
Internal memory size select register (IMS)	Provided	Not provided	Not provided
Pinouts	Pins related to PROM writing and reading are provided on the μPD78P4916.		
Other	There are differences in noise immunity, noise radiation, and some electrical specifications, because of the differences in circuit complexity and mask layout.		

Note The internal PROM and RAM capacities of the μPD78P4916 can be changed through its internal memory size select register (IMS).

Caution There are differences in noise immunity and noise radiation between the PROM and mask-ROM versions. When pre-producing the application set with the PROM version and then mass-producing it with the mask-ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask-ROM version.

2. PIN FUNCTION

2.1 Normal Operation Mode

(1) Port Pins

Pin Name	Input/Output	Alternate function	Description
P00 - P07	I/O	Real-time output port	8-bit input/output port (Port0) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P00 - P07).
P40 - P47	I/O	–	8-bit input/output port (Port4) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P40 - P47).
P50 - P57	I/O	–	8-bit input/output port (Port5) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P50 - P57).
P60	I/O	STRB/CLO	8-bit input/output port (Port6) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P60 - P67).
P61		$\overline{\text{SCK1}}$/BUZ	
P62		SO1	
P63		SI1	
P64		–	
P65		HWIN	
P66		PWM4	
P67		PWM5	
P70 - P77	Input	ANI0 - ANI7	8-bit input port (Port7)
P80	I/O	Real-time output port	for Pseudo-V_{SYNC} output 7-bit input/output port (Port8) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P80, P82 - P87)
P82			for HASW output
P83			for ROTC output
P84		PWM2	
P85		PWM3	
P86		PTO10	
P87		PTO11	
P90	I/O	ENV	7-bit input/output port (Port9) • Specifiable to input or output mode bitwise. • With software-specifiable on-chip pull-up resistors (P90 - P96).
P91 - P95		KEY0 - KEY4	
P96		–	

(2) Non-Port Pins (1/2)

Pin Name	Input/Output	Alternate function	Description
REEL0IN	Input	INTP3	Reel FG inputs
REEL1IN		–	
DFGIN		–	Drum FG, PFG input (Three-value)
DPGIN		–	Drum PG input
CFGIN		–	Capstan FG input
CSYNCIN		–	Composite SYNC input
CFGCPIN		–	CFG comparator input
CFGAMPO	Output	–	CFG amplifier output
PTO00	Output	–	Programmable timer outputs of super timer unit
PTO01		–	
PTO02		–	
PTO10		P86	
PTO11		P87	
PWM0	Output	–	PWM outputs of super timer unit
PWM1		–	
PWM2		P84	
PWM3		P85	
PWM4		P66	
PWM5		P67	
HASW	Output	P82	Head amplifier switch output
ROTC	Output	P83	Chrominance rotate output
ENV	Input	P90	Envelope input
SI1	Input	P63	Serial data input (Serial interface channel 1)
SO1	Output	P62	Serial data output (Serial interface channel 1)
$\overline{\text{SCK1}}$	I/O	P61/BUZ	Serial clock input/output (Serial interface channel 1)
SI2	Input	BUSY	Serial data input (Serial interface channel 2)
SO2	Output	–	Serial data output (Serial interface channel 2)
$\overline{\text{SCK2}}$	I/O	–	Serial clock input/output (Serial interface channel 2)
BUSY	Input	SI2	Serial busy input (Serial interface channel 2)
STRB	Output	P60/CLO	Serial strobe output (Serial interface channel 2)
ANI0 - ANI7	Analog inputs	P70 - P77	Analog inputs for A/D converter
ANI8 - ANI11		–	
CTLIN	–	–	CTL amplifier input capacitor
CTLOUT1	Output	–	CTL amplifier output
CTLOUT2	I/O	–	Logic input/CTL amplifier output
RECCTL+, RECCTL–	I/O	–	RECCTL output/PBCTL input
CTLDLY	–	–	External time-constant connection (to rewrite RECCTL)
VREFC	–	–	AC ground for VREF amplifier
NMI	Input	–	Non-maskable interrupt request input

(2) Non-Port Pins (2/2)

Pin Name	Input/Output	Alternate function	Description
INTP0 - INTP2	Input	–	External interrupt request input
INTP3	Input	REEL0IN	
KEY0 - KEY4	Input	P91 - P95	Key input signal
CLO	Output	P60/STRB	Clock output
BUZ	Output	P61/$\overline{SCK1}$	Buzzer output
HWIN	Input	P65	Hardware timer external input
$\overline{RESET}$	Input	–	Reset input
X1	Input	–	Crystal resonator connection for main system clock oscillation
X2	–		
XT1	Input	–	Crystal resonator connection for subsystem clock oscillation
XT2	–		Crystal resonator connection for clock oscillation of watch
AV_{DD1}, AV_{DD2}	–	–	Positive power supply for analog unit
AV_{SS1}, AV_{SS2}	–	–	GND for analog unit
AV_{REF}	–	–	Reference voltage input to A/D converter
V_{DD}	–	–	Positive power supply to digital unit
V_{SS}	–	–	GND of digital unit
IC	–	–	Internally connected. Connect directly to V_{SS}.

2.2 PROM Programming Mode ($V_{PP} \geq 5$ V, $\overline{RESET}$ = L)

Pin name	Input/output	Function
V_{PP}	–	Set PROM programming mode High voltage applied at program write/verify operation
$\overline{RESET}$	Input	Low level input for setting PROM programming mode
A0 - A16		Address input
D0 - D7	I/O	Data input/output
$\overline{PGM}$	Input	Program inhibit input in PROM programming mode
$\overline{CE}$		PROM enable input / programming pulse input
$\overline{OE}$		Read strobe input to PROM
V_{DD}	–	Positive power supply
V_{SS}		GND potential

✱ 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the input/output circuit types of the device's pins and the recommended connection of the pins which are unnecessary to the user's application. The circuit diagrams for the I/O circuits are shown in Figure 2-1.

Table 2-1. Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)

Pins	I/O circuit types	Direction	Recommended connection of unused pins
P00-P07	5-A	I/O	Input mode: Connect to V_{DD}.
P40-P47			Output mode: Leave unconnected.
P50-P57			
P60/STRB/CLO			
P61/$\overline{SCK1}$/BUZ	8-A		
P62/SO1	5-A		
P63/SI1	8-A		
P64	5-A		
P65/HWIN	8-A		
P66/PWM4	5-A		
P67/PWM5			
P70/ANI0-P77/ANI7	9	Input	Connect to V_{SS}.
P80	5-A	I/O	Input mode: Connect to V_{DD}.
P82/HASW			Output mode: Leave unconnected.
P83/ROTC			
P84/PWM2			
P85/PWM3			
P86/PTO10			
P87/PTO11			
P90/ENV			
P91/KEY0-P95/KEY4	8-A		
P96	5-A		
SI2/BUSY	2-A	Input	Connect to V_{DD}.
SO2	4	Output	High-impedance mode: Connect to V_{SS} via a pull-down resistor. Otherwise: Leave unconnected.
$\overline{SCK2}$	8-A	I/O	Input mode: Connect to V_{DD}. Output mode: Leave unconnected.
ANI8-ANI11	7	Input	Connect to V_{SS}.
RECCTL+, RECCTL–	—	I/O	When ENCTL = 0 and ENREC = 0: Connect to V_{SS}.

Remark ENCTL: Bit 1 of the amplifier control register (AMPC)
ENREC: Bit 7 of the amplifier mode register 0 (AMPM0)

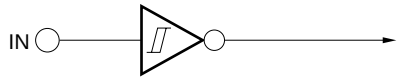
Table 2-1. Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

Pins	I/O circuit types	Direction	Recommended connection of unused pins
DFGIN	—	Input	ENDRUM = 0: Connect to V_{SS}.
DPGIN			ENDRUM = 0, or ENDRUM = 1 and SELPGSEPA = 0: Connect to V_{SS}.
CFGIN, CFGCPIN			ENCAP = 0: Connect to V_{SS}.
CSYNCIN			ENCSYN = 0: Connect to V_{SS}.
REEL0IN/INTP3, REEL1IN			ENREEL = 0: Connect to V_{SS}.
CTLOUT1	—	Output	Leave unconnected.
CTLOUT2	—	I/O	When ENCTL and ENCOMP = 0 and 0: Connect to V_{SS}. ENCTL = 1: Leave unconnected.
CFGAMPO	—	Output	Leave unconnected.
CTLIN	—	—	When ENCTL = 0: Leave unconnected.
VREFC			When ENCTL, ENCAP, and ENCOMP = 0, 0, and 0: Leave unconnected.
CTLDLY			Leave unconnected.
PWM0, PWM1	3	Output	Leave unconnected.
PTO00-PTO02			
NMI	2	Input	Connect to V_{DD}.
INTP0			Connect to V_{DD} or V_{SS}.
INTP1, INTP2	2-A	Input	Connect to V_{DD}.
AV_{DD1}, AV_{DD2}	—	—	Connect to V_{DD}.
AV_{REF}, AV_{SS1}, AV_{SS2}			Connect to V_{SS}.
$\overline{RESET}$	2	—	—
XT1	—	—	Connect to V_{SS}.
XT2			Leave unconnected.
IC			Connect directly to V_{SS}.

Remark ENDRUM: Bit 2 of the amplifier control register (AMPC)
SELPGSEPA: Bit 2 of the amplifier mode register 0 (AMPM0)
ENCAP: Bit 3 of the amplifier control register (AMPC)
ENCSYN: Bit 5 of the amplifier control register (AMPC)
ENREEL: Bit 6 of the amplifier control register (AMPC)
ENCTL: Bit 1 of the amplifier control register (AMPC)
ENCOMP: Bit 4 of the amplifier control register (AMPC)

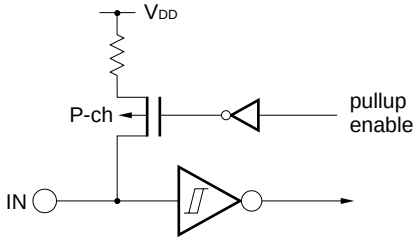
Figure 2-1. Pin I/O Circuit Diagrams (1/2)

Type 2



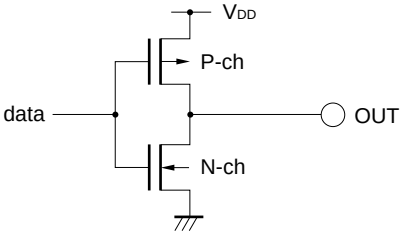
Schmitt triggered input with hysteresis characteristics.

Type 2-A

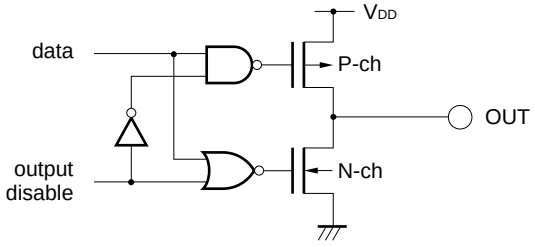


Schmitt triggered input with hysteresis characteristics.

Type 3

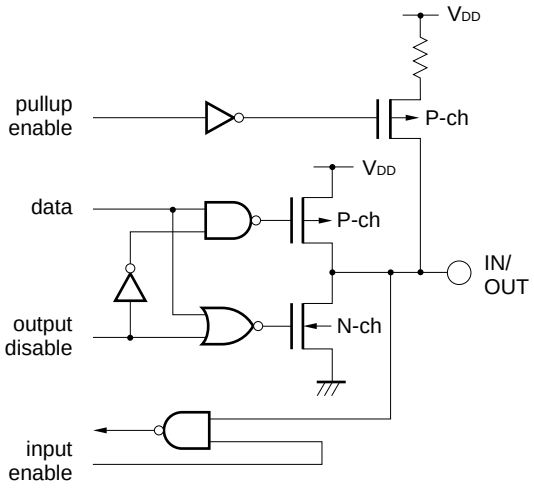


Type 4

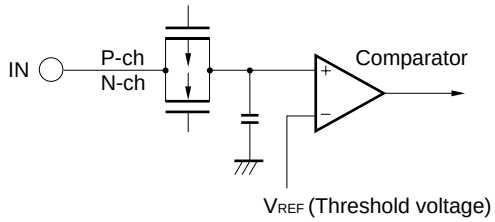


Push-pull output that can also set the output to the high-impedance state
(both P-ch and N-ch transistors are turned off.)

Type 5-A



Type 7



Type 8-A

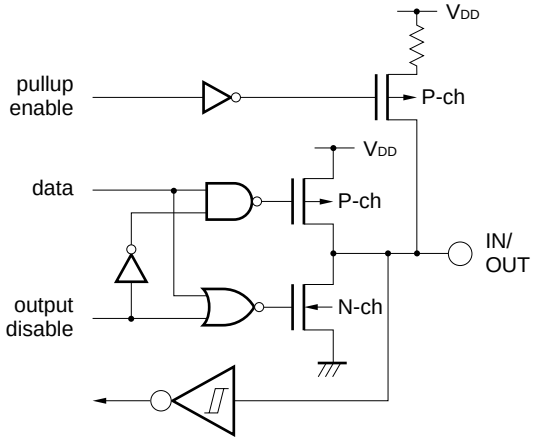
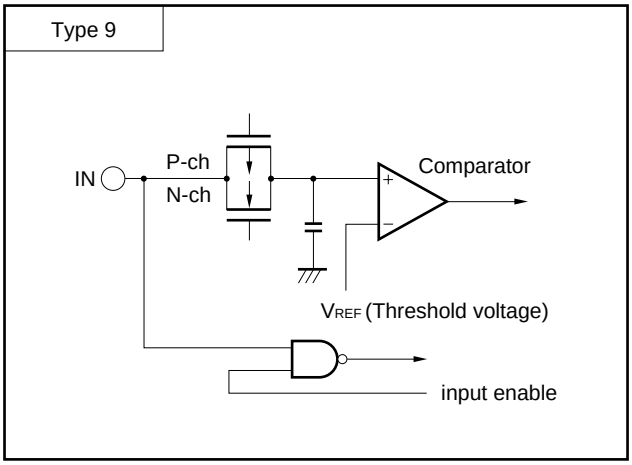


Figure 2-1. Pin I/O Circuit Diagrams (2/2)



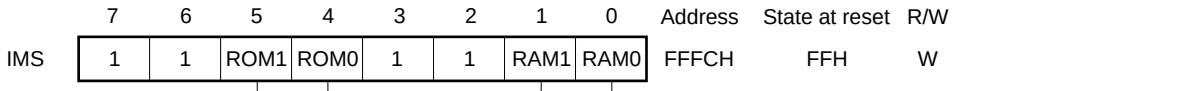
3. INTERNAL MEMORY CAPACITY SELECT REGISTER (IMS)

Internal memory capacity select register (IMS) specifies the effective area of on-chip memory (PROM, RAM) of the μPD78P4916. Setting this register is required when the capacity of the ROM or RAM in the mask version is smaller than that of the μPD78P4916. If the memory capacity of the μPD78P4916 is appropriately defined using this register, bugs in application programs due to accessing an address beyond the memory capacity of the actual chip can be avoided.

The IMS register is write-only register. To write this register, use the 8-bit manipulation instruction.

The register is initialized to FFH by $\overline{\text{RESET}}$ input (ROM: 62 Kbytes, RAM: 2048 bytes).

* **Figure 3-1. Internal Memory Capacity Select Register (IMS) Format**



	7	6	5	4	3	2	1	0	Address	State at reset	R/W
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0	FFFCH	FFH	W

RAM1	RAM0	Specification of internal RAM capacity
0	1	1280 bytes
1	1	2048 bytes
Other		Setting prohibited

ROM1	ROM0	Specification of internal ROM capacity
1	0	48 Kbytes
1	1	62 Kbytes
Other		Setting prohibited

Caution The μPD78P4916 has the IMS and the μPD784915 and 784916A do not have it. However, if a write instruction to IMS is executed in the μPD784915 or 784916A, it does not cause conflicts or malfunctions.

4. PROM PROGRAMMING

The μPD78P4916 has on-chip 62-Kbyte PROM as the program memory. The PROM programming mode is entered by setting V_{DD}, IC/V_{PP}, and $\overline{RESET}$ pins as specified. For the settings of the unused pins in this mode, refer to the drawing of "(2) PROM Programming Mode" in the section "Pin Configuration (Top View)".

4.1 Operation Mode

The PROM programming mode is entered by applying +5 V or +12 V to the IC/V_{PP} pin, +5 V or +6.5 V to the V_{DD} pins, and low-level voltage to the $\overline{RESET}$ pin. Table 4-1 shows the operation mode specified by the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins.

It is possible to read the contents of PROM by setting up read operation mode.

Table 4-1. Operation Mode of PROM Programming

Operation mode \ Pins	$\overline{RESET}$	IC/V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 - D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

Remark ×: Low or high level

(1) Read mode

By setting $\overline{CE}$ = L and $\overline{OE}$ = L, the device enters the read mode.

(2) Output disable mode

By setting $\overline{OE}$ = H, the device enters the output disable mode, where data output pins go to high impedance state.

Therefore it is possible to read data from a specified device by enabling only the $\overline{OE}$ pin of the device to be read, if two or more μPD78P4916s are connected to a data bus.

(3) Standby mode

By setting $\overline{CE}$ = H, the device enters the Standby mode.

In this mode, data output pins go to high impedance state regardless of the $\overline{OE}$ pin condition.

(4) Page data latch mode

By setting $\overline{CE}$ = H, $\overline{PGM}$ = H, and $\overline{OE}$ = L at the beginning of page programming mode, the device enters the page data latch mode.

In this mode, 4-byte data are latched in page units (consisting of 4 bytes) to internal address/data latch circuit.

(5) Page programming mode

After one-page data (consisting of 4 bytes) and their address are latched in the page data latch mode, the page programming operation is executed by applying 0.1-ms programming pulse (active low) to the $\overline{PGM}$ pin under $\overline{CE}$ = H, $\overline{OE}$ = H conditions. Following that operation, the programming data is verified by setting $\overline{CE}$ = L and $\overline{OE}$ = L.

When data is not programmed by one programming pulse, the write and verify operations are repeated X times ($X \leq 10$).

(6) Byte programming mode

Applying 0.1-ms programming pulse (active low) to the $\overline{PGM}$ pin under $\overline{CE}$ = L and $\overline{OE}$ = H condition, byte programming operation is executed. Next, the programming data is verified by setting $\overline{OE}$ = L.

When data is not programmed by one programming pulse, the write and verify operations are repeated X times ($X \leq 10$).

(7) Program verify mode

By setting $\overline{CE}$ = L, $\overline{PGM}$ = H, and $\overline{OE}$ = L, the device enters the program verify mode. Check whether data is programmed correctly or not in this mode after write operation.

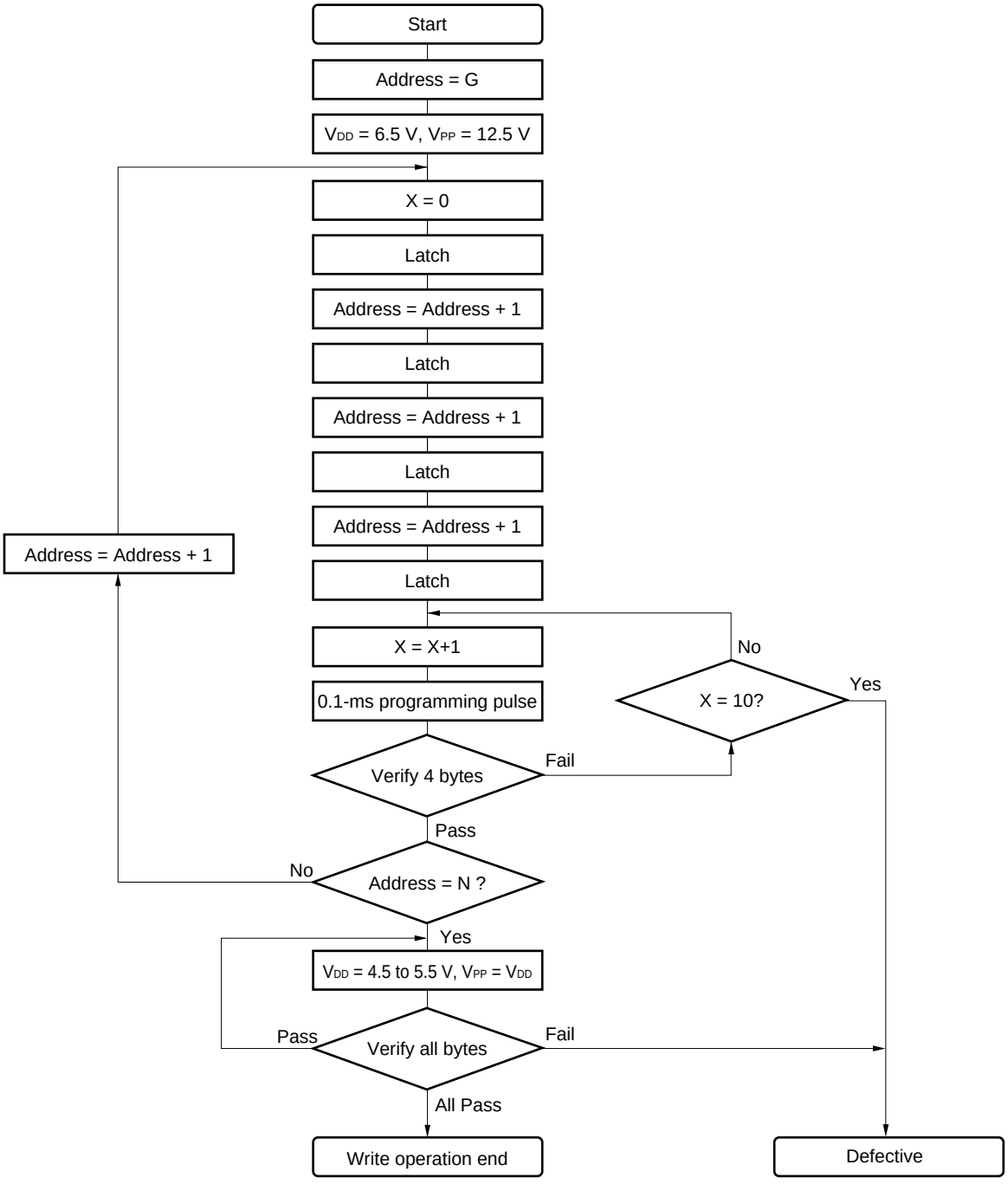
(8) Program inhibit mode

When the $\overline{OE}$ pins, V_{PP} pins, and D0-D7 pins of two or more μPD78P4916s are connected in parallel, use program inhibit mode to write data to one of those devices.

Programming is executed in the page programming mode or byte programming mode as mentioned above. At that time, data is not programmed to a device for which high level voltage is applied to the $\overline{PGM}$ pin.

4.2 PROM Write Procedure

Figure 4-1. Flowchart in Page Programming Mode



Remarks 1. G = Start address

2. N = End address of the program

Figure 4-2. Operation Timing in Page Programming Mode

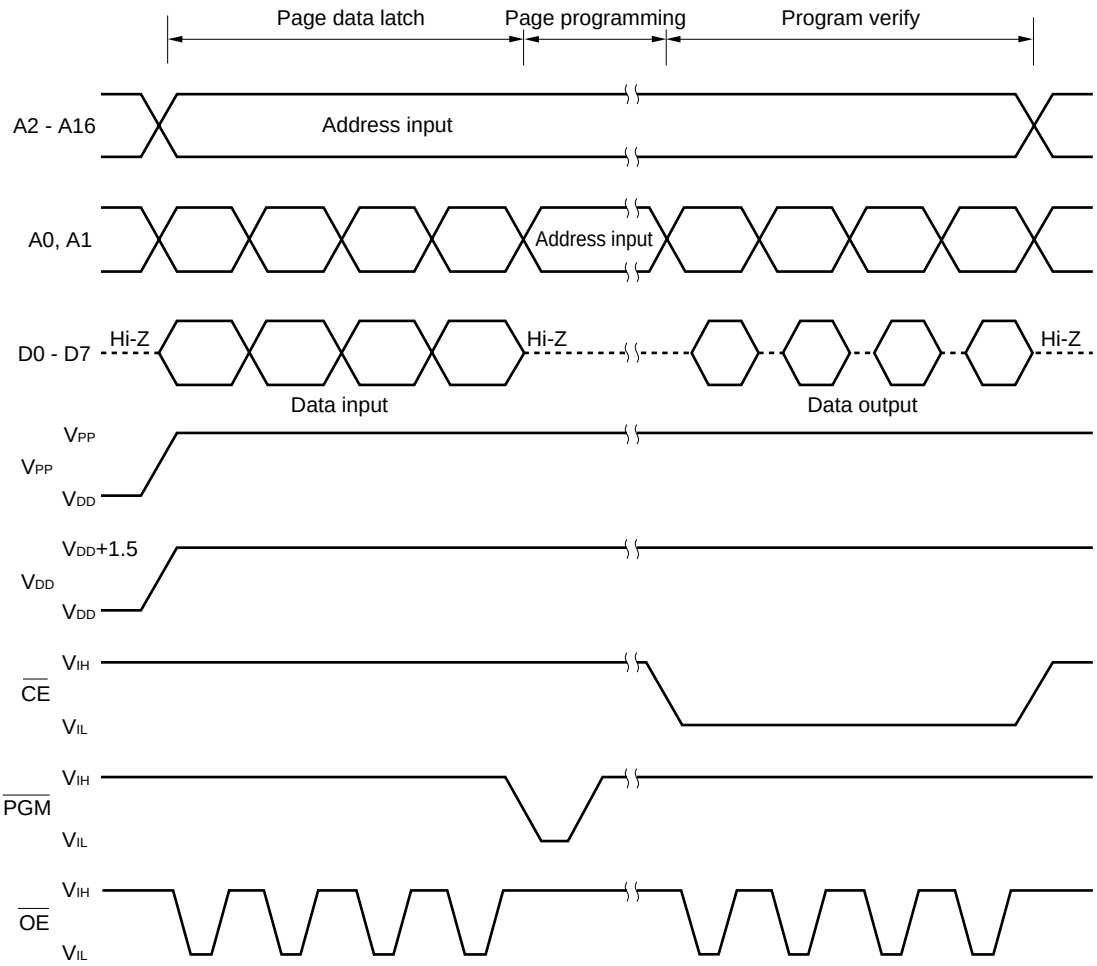
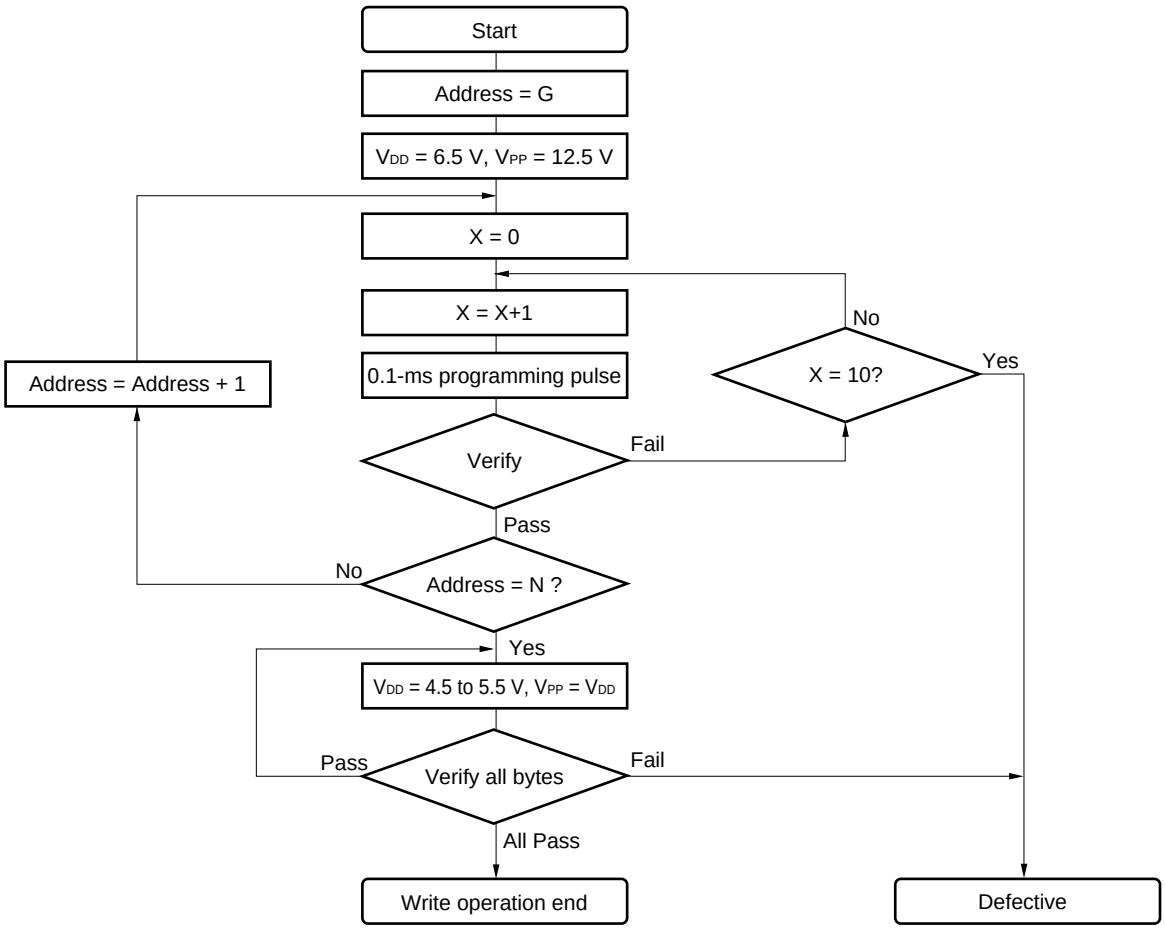


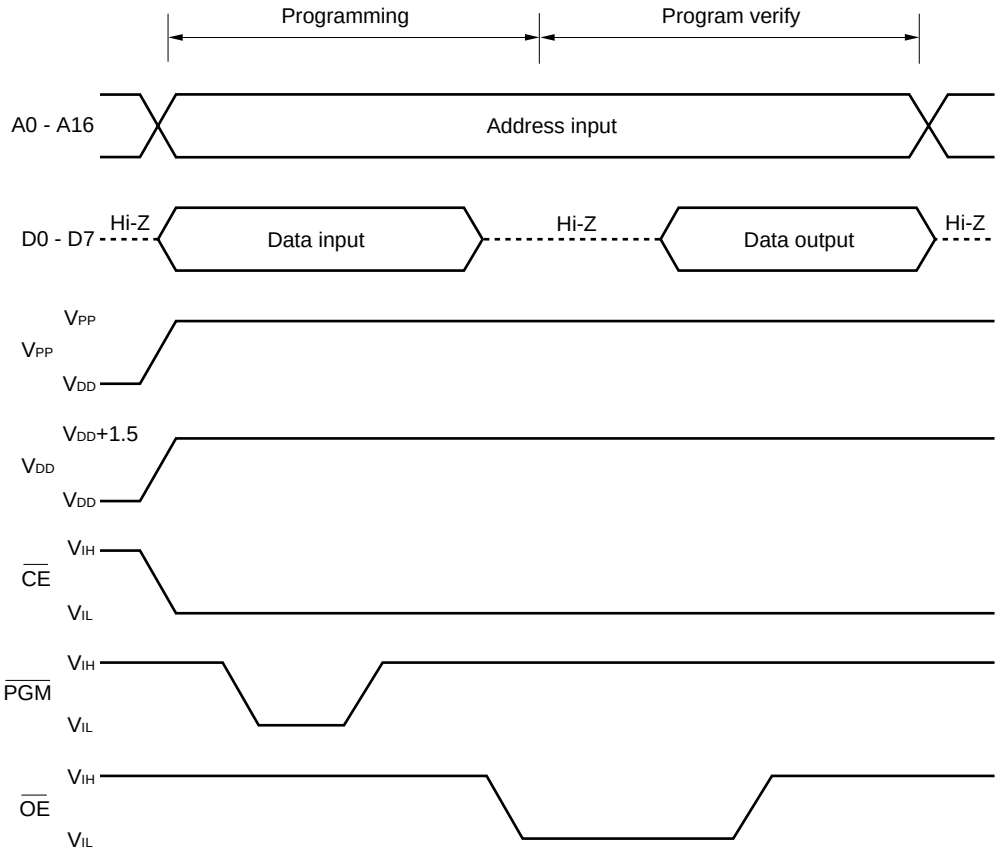
Figure 4-3. Flowchart in Byte Programming Mode



Remarks 1. G = Start address

2. N = End address of the program

Figure 4-4. Operation Timing in Byte Programming Mode



Cautions 1. Apply voltage to V_{DD} before applying voltage to V_{PP}, and cut off V_{DD} voltage after V_{PP} voltage is cut off.

2. The voltage including overshoot applied to V_{PP} pin must be kept less than +13.5 V.

3. If a device is inserted or removed while +12.5 V is applied to V_{PP} pin, it may be adversely affected in reliability.

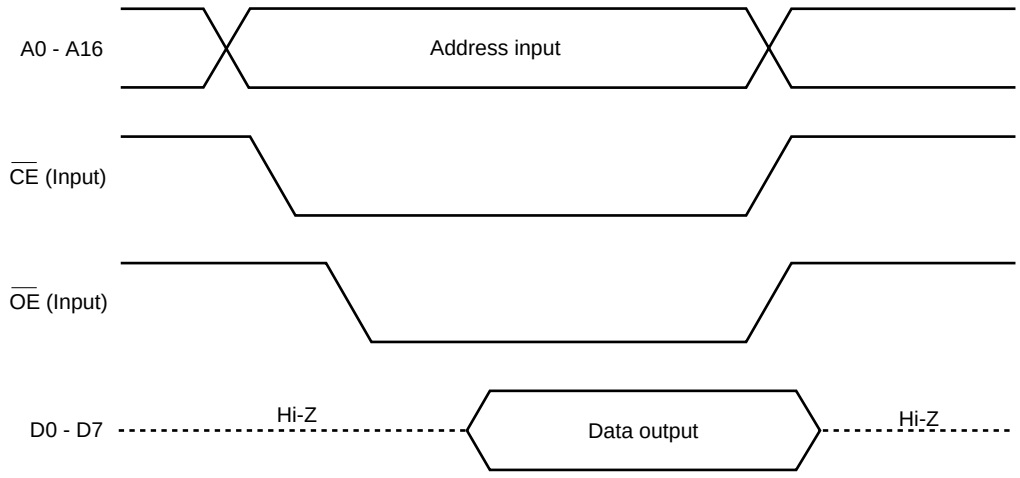
4.3 PROM Read Procedure

The contents of PROM can be read onto external data bus (D0-D7) as described below:

(1) Fix $\overline{\text{RESET}}$ pin to low and supply +5 V to V_{PP} pin. Connect other unused pins as specified in “(2) PROM Programming Mode” in section “Pin Configuration (Top View)."
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0-A16 pins.
(4) Enter the read mode ($\overline{CE}$ = L, $\overline{OE}$ = L).
(5) Output data to D0-D7 pins.

The above operation timing from (2) to (5) is shown in Figure 4-5.

Figure 4-5. PROM Read Timing



4.4 Screening One-time PROM Versions

The one-time PROM version (μPD78P4916GF-3BA) cannot be completely tested by NEC for shipment because of its structure. For screening, it is recommended to verify PROM after storing the necessary data under the following conditions:

Storage Temperature	Storage Time
125 ˚C	24 hours

✱ 5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

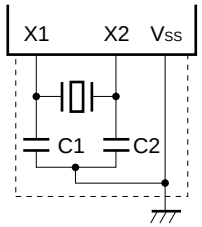
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} - AV_{DD1} \leq 0.5$ V	–0.5 to +7.0	V
	AV_{DD1}	$V_{DD} - AV_{DD2} \leq 0.5$ V	–0.5 to +7.0	V
	AV_{DD2}	$AV_{DD1} - AV_{DD2} \leq 0.5$ V	–0.5 to +7.0	V
	AV_{SS1}		–0.5 to +0.5	V
	AV_{SS2}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD}+0.5	V
Analog input voltage (ANI0-ANI11)	V_{IAN}	$V_{DD} \geq AV_{DD2}$	–0.5 to AV_{DD2}+0.5	V
		$V_{DD} < AV_{DD2}$	–0.5 to V_{DD}+0.5	V
Output voltage	V_O		–0.5 to V_{DD}+0.5	V
Output current, low	I_{OL}	Per pin	15	mA
		Total of all output pins	100	mA
Output current, high	I_{OH}	Per pin	–10	mA
		Total of all output pins	–50	mA
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the above parameters exceeds the absolute maximum ratings, even momentarily, device reliability may be impaired. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.

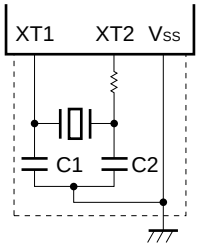
Operating Conditions

Clock frequency	Operating ambient temperature (T_A)	Operating condition	Supply voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 16 MHz	–10 to +70 °C	All functions	+4.5 to +5.5 V
		CPU function only	+4.0 to +5.5 V
32 kHz ≤ f_{XT} ≤ 35 kHz		Subclock operation (CPU, watch, and Port functions only)	+2.7 to +5.5 V

Oscillator Characteristics (Main Clock) (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Item	MIN.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XX})	4	16	MHz

Oscillator Characteristics (Subclock) (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Item	MIN.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})	32	35	kHz

Caution When using the main system clock and subsystem clock oscillators, wiring in the area enclosed with the dotted lines should be carried out as follows to avoid an adverse effect from wiring capacitance:

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
  Wiring should not be placed close to a varying high current.
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
  Do not ground wiring to a ground pattern in which high current flows.
- **Do not fetch a signal from the oscillator.**

As the amplification degree of the subsystem clock oscillator is low to reduce current consumption, pay particular attention to the wiring method.

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	Other than pins indicated in **Note 1** below		0		$0.3V_{DD}$	V
	V_{IL2}	Pins indicated in **Note 1** below		0		$0.2V_{DD}$	V
	V_{IL3}	X1, X2		0		0.4	V
Input voltage, high	V_{IH1}	Other than pins indicated in **Note 1** below		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Pins indicated in **Note 1** below		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD}–0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 5.0 mA (Pins listed in **Note 2** below)				0.6	V
	V_{OL2}	I_{OL} = 2.0 mA				0.45	V
	V_{OL3}	I_{OL} = 100 μA				0.25	V
Output voltage, high	V_{OH1}	I_{OH} = –1.0 mA		V_{DD}–1.0			V
	V_{OH2}	I_{OH} = –100 μA		V_{DD}–0.4			V
Input leakage current	I_{LI}	$0 \le V_I \le V_{DD}$				±10	μA
Output leakage current	I_{LO}	$0 \le V_O \le V_{DD}$				±10	μA
V_{DD} power supply current	I_{DD1}	Operation mode	f_{XX} = 16 MHz f_{XX} = 8 MHz (Low frequency oscillation mode) Internal main clock operation at 8 MHz		35	55	mA
			f_{XT} = 32.768 kHz Subclock operation (CPU, Watch, Port) V_{DD} = 2.7 V		0.9	1.2	mA
	I_{DD2}	HALT mode	f_{XX} = 16 MHz f_{XX} = 8 MHz (Low frequency oscillation mode) Internal main clock operation at 8 MHz		15	27.5	mA
			f_{XT} = 32.768 kHz Subclock operation (CPU, Watch, Port) V_{DD} = 2.7 V		30	60	μA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current Note 3	I_{DDDR}	STOP mode V_{DDDR} = 5.0 V	Subclock oscillation		36	75	μA
		STOP mode V_{DDDR} = 2.7 V	Subclock oscillation		3.5	15	μA
		STOP mode V_{DDDR} = 2.5 V	Subclock suspended		1.5	10	μA
Pull-up resistor	R_L	V_I = 0 V		25	55	110	kΩ

Notes 1. $\overline{\text{RESET}}$, IC, NMI, INTP0-INTP2, P61/$\overline{\text{SCK1}}$/BUZ, P63/SI1, $\overline{\text{SCK2}}$, SI2/BUSY, P65/HWIN, P91/KEY0-P95/KEY4.

2. P46, P47

3. When subclock is suspended at STOP mode, disconnect feedback resistor and connect XT1 pin to the V_{DD} potential.

AC Characteristics

CPU and peripheral unit operation clocks (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	TYP.	Unit
CPU operation clock cycle time	t_{CLK}	f_{XX} = 16 MHz V_{DD} = AV_{DD} = 4.0 to 5.5 V CPU function only	125	ns
		f_{XX} = 16 MHz		
		f_{XX} = 8 MHz, Low frequency oscillation mode (CC bit7 = 1)		
Peripheral unit operation clock cycle time	t_{CLK1}	f_{XX} = 16 MHz	125	ns
		f_{XX} = 8 MHz, Low frequency oscillation mode (CC bit7 = 1)		

Serial interface

(1) SIOn: n = 1, 2 (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	f_{CLK1}/8	1.0		μs
			f_{CLK1}/16	2.0		μs
			f_{CLK1}/32	4.0		μs
			f_{CLK1}/64	8.0		μs
			f_{CLK1}/128	16		μs
			f_{CLK1}/256	32		μs
Serial clock high/low level width	t_{WSKH}	Input	External clock	420		ns
	t_{WSKL}	Output	Internal clock	t_{CYSK}/2–50		ns
SIn set-up time (to $\overline{SCKn}$ ↑)	t_{SSSK}			100		ns
SIn hold time (from $\overline{SCKn}$ ↑)	t_{HSSK}			400		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	t_{DSSK}			0	300	ns

Remarks 1. f_{CLK1}: Operation clock for peripheral unit (8 MHz)

2. n = 1, 2

(2) Only SIO2 (T_A= –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK2}$(8) ↑ → STRB ↑	t_{DSTRB}		t_{WSKH}	t_{CYSK}	
Strobe high level width	t_{WSTRB}		t_{CYSK}–30	t_{CYSK}+30	ns
BUSY setup time (to BUSY detection timing)	t_{SBUSY}		100		ns
BUSY hold time (from BUSY detection timing)	t_{HBUSY}		100		ns
Busy inactive → $\overline{SCK2}$(1) ↓	t_{LBUSY}			t_{CYSK}+t_{WSKH}	

Remarks 1. The value in the parentheses following $\overline{SCK2}$ indicates the sequential number of the $\overline{SCK2}$.

2. BUSY detection timing is (n + 2) × t_{CYSK} (n = 0, 1,...) after $\overline{SCK2}$(8) ↑.

3. BUSY inactive → $\overline{SCK2}$(1) ↓ is a value at the time data is already written in SIO2.

Other Operations (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter		Symbol	Conditions		MIN.	MAX.	Unit
Timer unit input low level width		t_{WCTL}	at DFGIN, CFGIN, DPGIN, REEL0IN, REEL1IN logic level input		t_{CLK1}		ns
Timer unit input high level width		t_{WCTH}	at DFGIN, CFGIN, DPGIN, REEL0IN, REEL1IN logic level input		t_{CLK1}		ns
Timer unit input signal valid edge input cycle		t_{PERIN}	DFGIN, CFGIN and DPGIN input		2		μs
CSYNCIN low level width		t_{WCR1L}	Digital noise eliminator not used		$8t_{CLK1}$		ns
			Digital noise eliminator used (INTM2 bit 4 = 0)		$108t_{CLK1}$		ns
			Digital noise eliminator used (INTM2 bit 4 = 1)		$180t_{CLK1}$		ns
CSYNCIN high level width		t_{WCR1H}	Digital noise eliminator not used		$8t_{CLK1}$		ns
			Digital noise eliminator used (INTM2 bit 4 = 0)		$108t_{CLK1}$		ns
			Digital noise eliminator used (INTM2 bit 4 = 1)		$180t_{CLK1}$		ns
Digital noise eliminator	Eliminated pulse width	t_{WSEP}	INTM2 bit 4 = 0			$104t_{CLK1}$	ns
			INTM2 bit 4 = 1			$176t_{CLK1}$	ns
	Passed pulse width		INTM2 bit 4 = 0		$108t_{CLK1}$		ns
			INTM2 bit 4 = 1		$180t_{CLK1}$		ns
NMI low level width		t_{WNIL}	V_{DD} = AV_{DD} = 2.7 to 5.5 V		10		μs
NMI high level width		t_{WNIH}	V_{DD} = AV_{DD} = 2.7 to 5.5 V		10		μs
INTP0 and INTP3 low level width		t_{WIPL0}			$2t_{CLK1}$		ns
INTP0 and INTP3 high level width		t_{WIPH0}			$2t_{CLK1}$		ns
INTP1, KEY0 - KEY4 low level width		t_{WIPL1}	Other than in STOP mode		$2t_{CLK1}$		ns
			When cancelling STOP mode		10		μs
INTP1, KEY0 - KEY4 high level width		t_{WIPH1}	Other than in STOP mode		$2t_{CLK1}$		ns
			When cancelling STOP mode		10		μs
INTP2 low level width		t_{WIPL2}	Main clock operation in normal mode	Sampled at f_{CLK}	$2t_{CLK1}$		ns
				Sampled at f_{CLK}/128	32 Note		μs
			Subclock operation in normal mode	Sampled at f_{CLK}	61		μs
				Sampled at f_{CLK}/128	7.9 Note		ms
			When cancelling STOP mode		10		μs
INTP2 high level width		t_{WIPH2}	Main clock operation in normal mode	Sampled at f_{CLK}	$2t_{CLK1}$		ns
				Sampled at f_{CLK}/128	32 Note		μs
			Subclock operation in normal mode	Sampled at f_{CLK}	61		μs
				Sampled at f_{CLK}/128	7.9 Note		ms
			When cancelling STOP mode		10		μs
$\overline{\text{RESET}}$ low level width		t_{WRSL}			10		μs

Note If a high level or low level is input two times in succession during the sampling period, high level or low level is detected.

Remark t_{CLK1}: Operation clock cycle time for peripheral unit (125 ns).

Clock Output Operation (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Expression	MIN.	MAX.	Unit
CLO cycle time	t_{CYCL}		250	2000	ns
CLO low level width	t_{CLL}	$t_{CYCL}/2 \pm 50$	75	1050	ns
CLO high level width	t_{CLH}	$t_{CYCL}/2 \pm 50$	75	1050	ns
CLO rising time	t_{CLR}			50	ns
CLO falling time	t_{CLF}			50	ns

Data Retention Characteristics (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 2.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}	Pins listed in **Note** below	0		$0.1V_{DDDR}$	V
Input voltage, high	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

Note $\overline{RESET}$, IC, NMI, INTP0-INTP2, P61/$\overline{SCK1}$/BUZ, P63/SI1, $\overline{SCK2}$, SI2/BUSY, P65/HWIN, P91/KEY0-P95/KEY4

Watch Function (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Subclock oscillation retention voltage	V_{DDXT}		2.7		V
Hardware watch function operation voltage	V_{DDW}		2.7		V

Subclock Oscillation Suspension Detection Flag (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Oscillation suspension detection width	t_{OSCF}		45		μs

A/D Converter Characteristics (T_A = –10 to +70 °C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error		$AV_{REF} = V_{DD}$			2.0	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	ADM bit 4 = 0	$160t_{CLK1}$			μs
		ADM bit 4 = 1	$80t_{CLK1}$			μs
Sampling time	t_{SAMP}	ADM bit 4 = 0	$32t_{CLK1}$			μs
		ADM bit 4 = 1	$16t_{CLK1}$			μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Analog input impedance	Z_{AN}			1000		MΩ
AV_{REF} current	AI_{REF}			0.4	1.2	mA

VREF Amplifier (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}		2.35	2.50	2.65	V
Charge current	I_{CHG}	AMPM0.0 is set to 1 for pins listed in **Note** below.	300			μA

Note RECCTL+, RECCTL–, CFGIN, CFGCPIN, DFGIN, DPGIN, CSYNCIN, REEL0IN, REEL1IN

CTL Amplifier (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

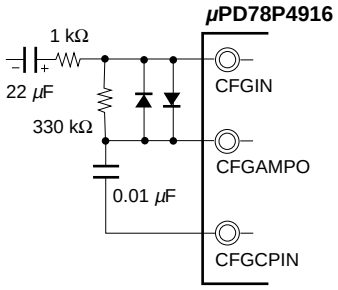
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CTL+, – input resistance	R_{ICTL}		2	5	10	kΩ
Feedback resistance	R_{FCTL}		20	50	100	kΩ
Bias resistance	R_{BCTL}		20	50	100	kΩ
Minimum voltage gain	G_{CTLMIN}		17	20	22	dB
Maximum voltage gain	G_{CTLMAX}		71	75		dB
Gain switching step	S_{GAIN}			1.77		dB
Common mode signal rejection	CMR	DC, Voltage gain: 20 dB		50		dB
Comparator set voltage for waveform regulation, high	$V_{PBCTLHS}$		V_{REF}+0.47	V_{REF}+0.50	V_{REF}+0.53	V
Comparator reset voltage for waveform regulation, high	$V_{PBCTLHR}$		V_{REF}+0.27	V_{REF}+0.30	V_{REF}+0.33	V
Comparator set voltage for waveform regulation, low	$V_{PBCTLLS}$		V_{REF}–0.53	V_{REF}–0.50	V_{REF}–0.47	V
Comparator reset voltage for waveform regulation, low	$V_{PBCTLLR}$		V_{REF}–0.33	V_{REF}–0.30	V_{REF}–0.27	V
Comparator high voltage for CLT flag S	V_{FSH}		V_{REF}+1.00	V_{REF}+1.05	V_{REF}+1.10	V
Comparator low voltage for CLT flag S	V_{FSL}		V_{REF}–1.10	V_{REF}–1.05	V_{REF}–1.00	V
Comparator high voltage for CLT flag L	V_{FLH}		V_{REF}+1.40	V_{REF}+1.45	V_{REF}+1.50	V
Comparator low voltage for CLT flag L	V_{FLL}		V_{REF}–1.50	V_{REF}–1.45	V_{REF}–1.40	V

CFG Amplifier (AC Coupling) (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage gain 1	G_{CFG1}	f_i = 2 kHz, open loop	50			dB
Voltage gain 2	G_{CFG2}	f_i = 2 kHz, open loop	34			dB
CFGAMPO output current, high	I_{OHCFG}	DC	–1			mA
CFGAMPO output current, low	I_{OLCFG}	DC	0.4			mA
Comparator high voltage	V_{CFGH}		V_{REF}+0.09	V_{REF}+0.12	V_{REF}+0.15	V
Comparator low voltage	V_{CFGL}		V_{REF}–0.15	V_{REF}–0.12	V_{REF}–0.09	V
Duty precision	P_{DUTY}	See **Note** below.	49.7	50.0	50.3	%

Note The following circuit and input signal conditions are assumed.

- Input signal: sine wave input (5 mV_{p-p}), f_i = 1 kHz
- Voltage gain: 50 dB



DFG Amplifier (AC Coupling) (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage gain	G_{DFG}	f_i = 900 Hz, open loop	50			dB
Feedback resistance	R_{FDFG}		160	400	640	kΩ
Input protect resistance	R_{IDFG}			150		Ω
Comparator high voltage	V_{DFGH}		V_{REF}+0.07	V_{REF}+0.10	V_{REF}+0.14	V
Comparator low voltage	V_{DFGL}		V_{REF}–0.14	V_{REF}–0.10	V_{REF}–0.07	V

Caution The resistance of the pin to be connected to the DFGIN pin must be below 16 kΩ. If the resistance is higher than the limit, the DFG amplifier may oscillate.

DPG Comparator (AC Coupling) (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IDPG}		20	50	100	kΩ
Comparator high voltage	V_{DPGH}		V_{REF}+0.02	V_{REF}+0.05	V_{REF}+0.08	V
Comparator low voltage	V_{DPGL}		V_{REF}–0.08	V_{REF}–0.05	V_{REF}–0.02	V

Three-value divider (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IPFG}		20	50	100	kΩ
Comparator high voltage	V_{PFGH}		V_{REF}+0.5	V_{REF}+0.7	V_{REF}+0.9	V
Comparator low voltage	V_{PFGL}		V_{REF}–1.4	V_{REF}–1.2	V_{REF}–1.0	V

CSYNC Comparator (AC Coupling) (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{ICSYN}		20	50	100	kΩ
Comparator high voltage	V_{CSYNH}		V_{REF}+0.07	V_{REF}+0.10	V_{REF}+0.13	V
Comparator low voltage	V_{CSYNL}		V_{REF}–0.13	V_{REF}–0.10	V_{REF}–0.07	V

Reel FG Comparator (AC Coupling) (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

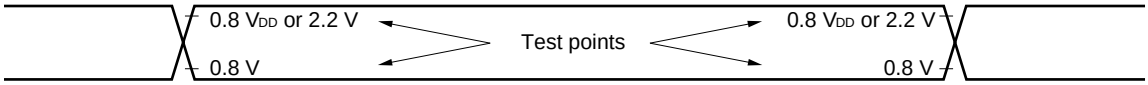
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input impedance	Z_{IRLFG}		20	50	100	kΩ
Comparator high voltage	V_{RLFGH}		V_{REF}+0.02	V_{REF}+0.05	V_{REF}+0.08	V
Comparator low voltage	V_{RLFGL}		V_{REF}–0.08	V_{REF}–0.05	V_{REF}–0.02	V

RECCTL Driver (T_A = 25 °C, V_{DD} = AV_{DD} = 5 V, V_{SS} = AV_{SS} = 0 V)

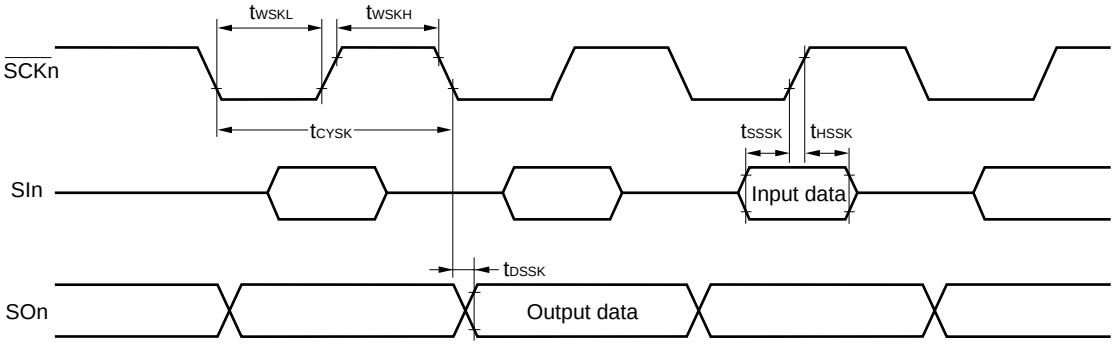
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RECCTL+, – high level output voltage	V_{OHREC}	I_{OH} = –4 mA	V_{DD}–0.8			V
RECCTL+, – low level output voltage	V_{OLREC}	I_{OL} = 4 mA			0.8	V
CTLDLY on-chip resistor	R_{CTL}		40	70	140	kΩ
CTLDLY charge current	I_{OHCTL}	On-chip resistor disabled	–3			mA
CTLDLY discharge current	I_{OLCTL}		–3			mA

Timing Waveform

AC timing test point

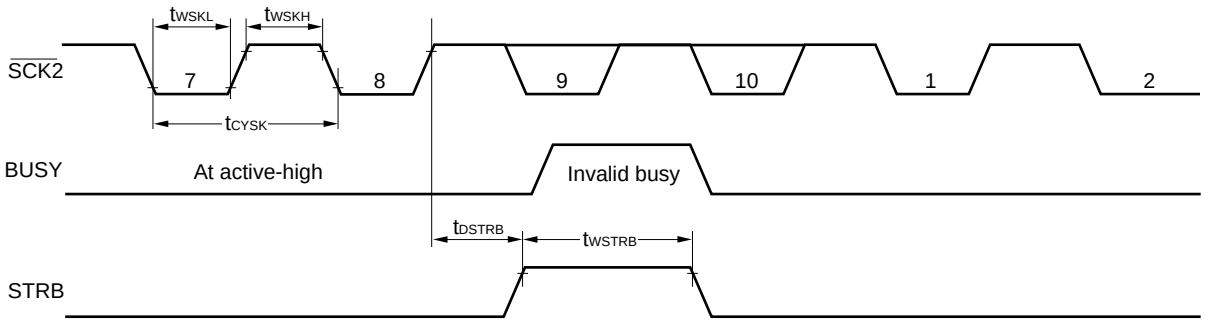


Serial Transfer Timing (SIOn: n = 1, 2)

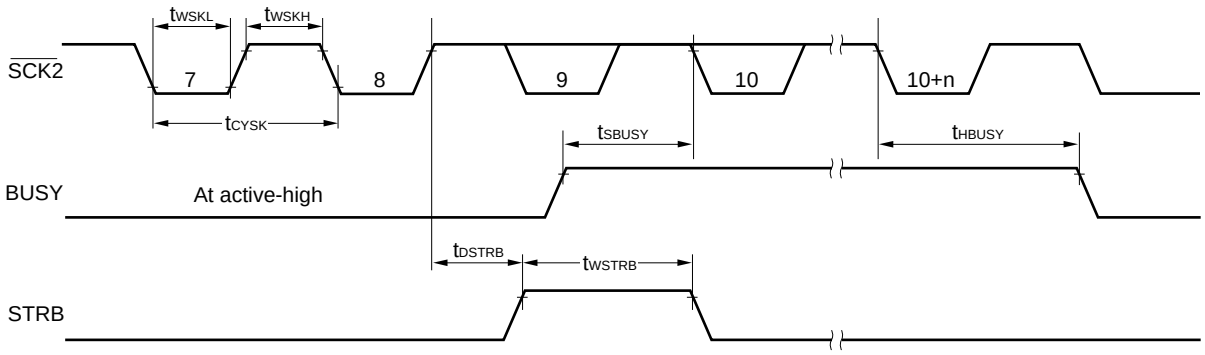


Serial Transfer Timing (Only SIO2)

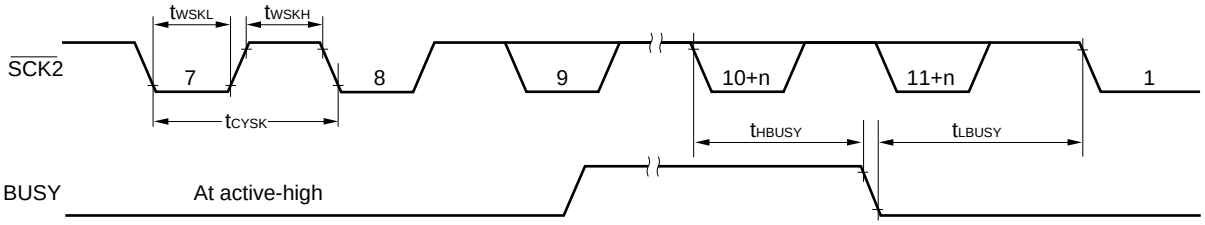
No busy processing



Continue busy processing



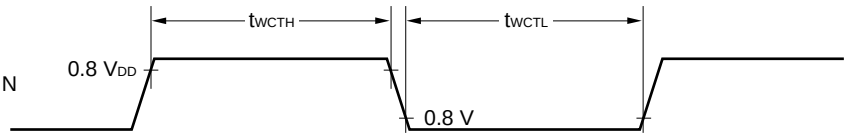
Terminate busy processing



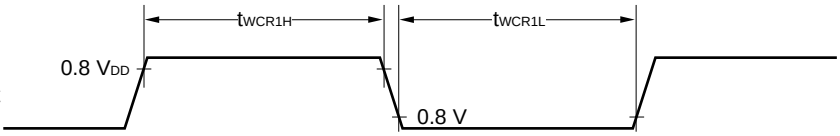
Caution Do not use busy control and strobe control whenever the external clock is selected as a serial clock.

Super timer unit input timing

At DFGIN, CFGIN, DPGIN, REEL0IN and REEL1IN logic level input

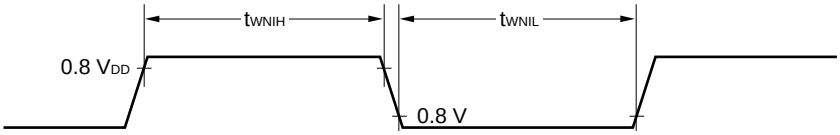


At CSYNCIN logic level input

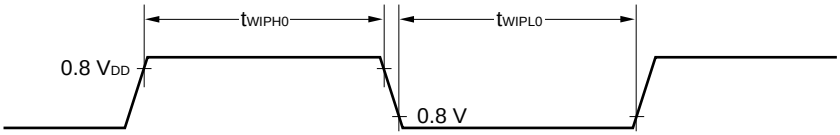


Interrupt input timing

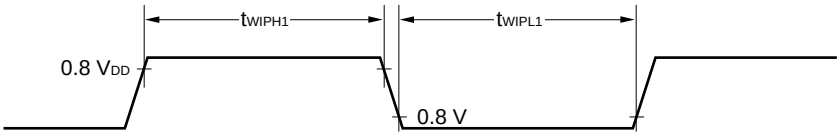
NMI



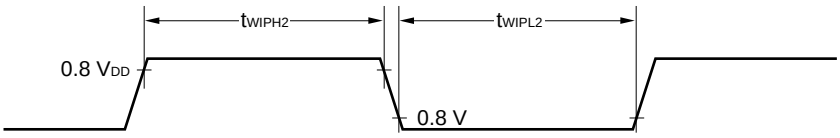
INTP0, INTP3



INTP1, KEY0 - KEY4

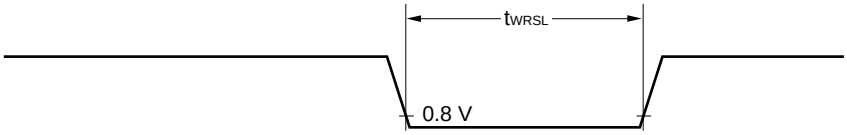


INTP2

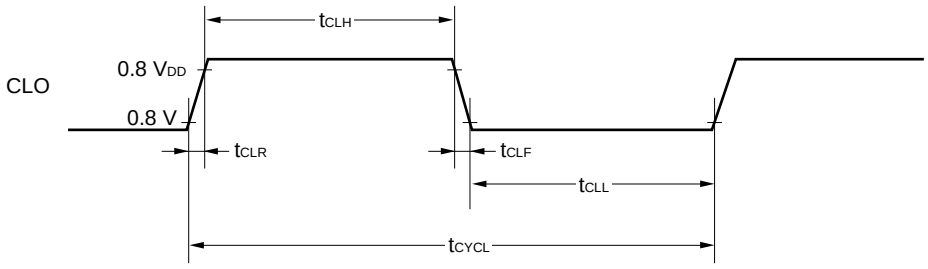


Reset input timing

$\overline{\text{RESET}}$



Clock output timing



DC Programming Characteristics (T_A = +25 ± 5 °C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Symbol Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Input voltage, low	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 ≤ V_I ≤ V_{DDP} Note 2			±10	μA
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DDP}–0.7			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}		0 ≤ V_O ≤ V_{DDP}, $\overline{OE}$ = V_{IH}			±10	μA
V_{DD} supply voltage	V_{DDP}	V_{DD}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.50	5.0	5.50	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DD} supply current	I_{DD}	I_{DD}	Program memory write mode			50	mA
			Program memory read mode			30	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode			50	mA
			Program memory read mode		1	100	μA

Notes 1. Corresponding symbols of the μPD27C1001A.

2. V_{DDP} is a V_{DD} pin during programming.

AC Programming Characteristics (T_A = +25 ± 5 °C, V_{SS} = AV_{SS} = 0 V)

PROM Write Operation Mode (Page Programming Mode)

Parameter	Symbol Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		230	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS} Note 2		2			μs
Initial programming pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
$\overline{OE}$ → valid data delay time	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latch	t_{LW}		1			μs
$\overline{PGM}$ set-up time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

Notes 1. Correspond to symbols of the μPD27C1001A (except t_{VDS}).

2. t_{VDS} corresponds to t_{VCS} of the μPD27C1001A.

PROM Write Mode (Byte Programming Mode)

Parameter	Symbol Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS} Note 2		2			μs
Initial programming pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
$\overline{OE}$ → valid data delay time	t_{OE}				150	ns

Notes 1. Correspond to symbols of the μPD27C1001A (except t_{VDS}).

2. t_{VDS} corresponds to t_{VCS} of the μPD27C1001A.

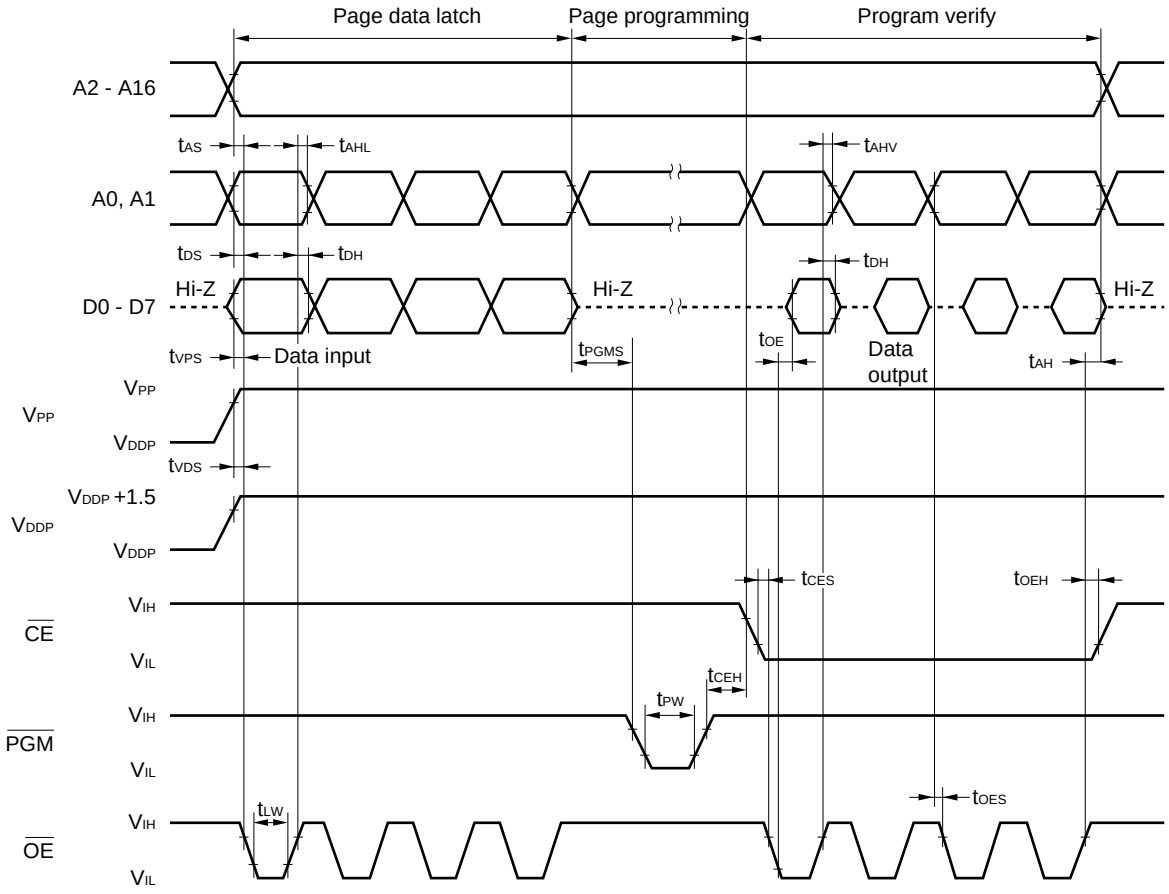
PROM Read Mode

Parameter	Symbol Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address → data output time	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
$\overline{CE}$ ↓ → data output time	t_{CE}	$\overline{OE} = V_{IL}$			200	ns
$\overline{OE}$ ↓ → data output time	t_{OE}	$\overline{CE} = V_{IL}$			75	ns
Data hold time (from $\overline{OE}$ ↑, $\overline{CE}$ ↑) Note 2	t_{DF}	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$	0		60	ns
Data hold time (from address)	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

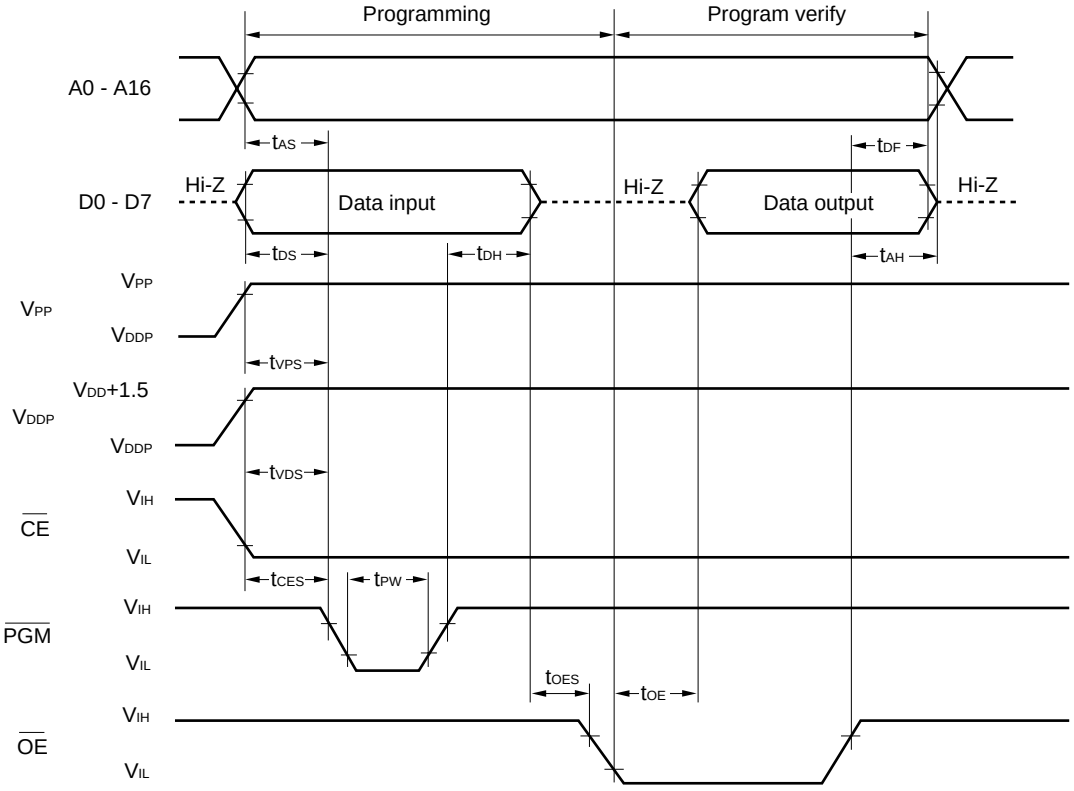
Notes 1. Correspond to symbols of the μPD27C1001A.

2. t_{DF} is a time after either $\overline{OE}$ or $\overline{CE}$ rose to V_{IH} first.

PROM Write Mode Timing (Page Programming Mode)



PROM Write Mode Timing (Byte Programming Mode)

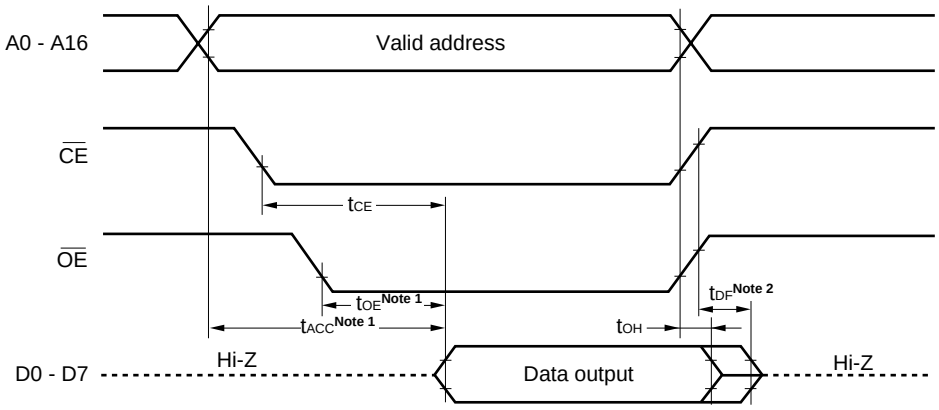


Cautions 1. Apply voltage to V_{DDP} before applying voltage to V_{PP}, and cut off V_{DDP} voltage after V_{PP} voltage is cut off.

2. The voltage, including overshoot, applied to V_{PP} pin must be kept less than +13.5 V.

3. If a device is inserted or removed while +12.5 V is applied to V_{PP} pin, it may be adversely affected in reliability.

PROM Read Mode Timing

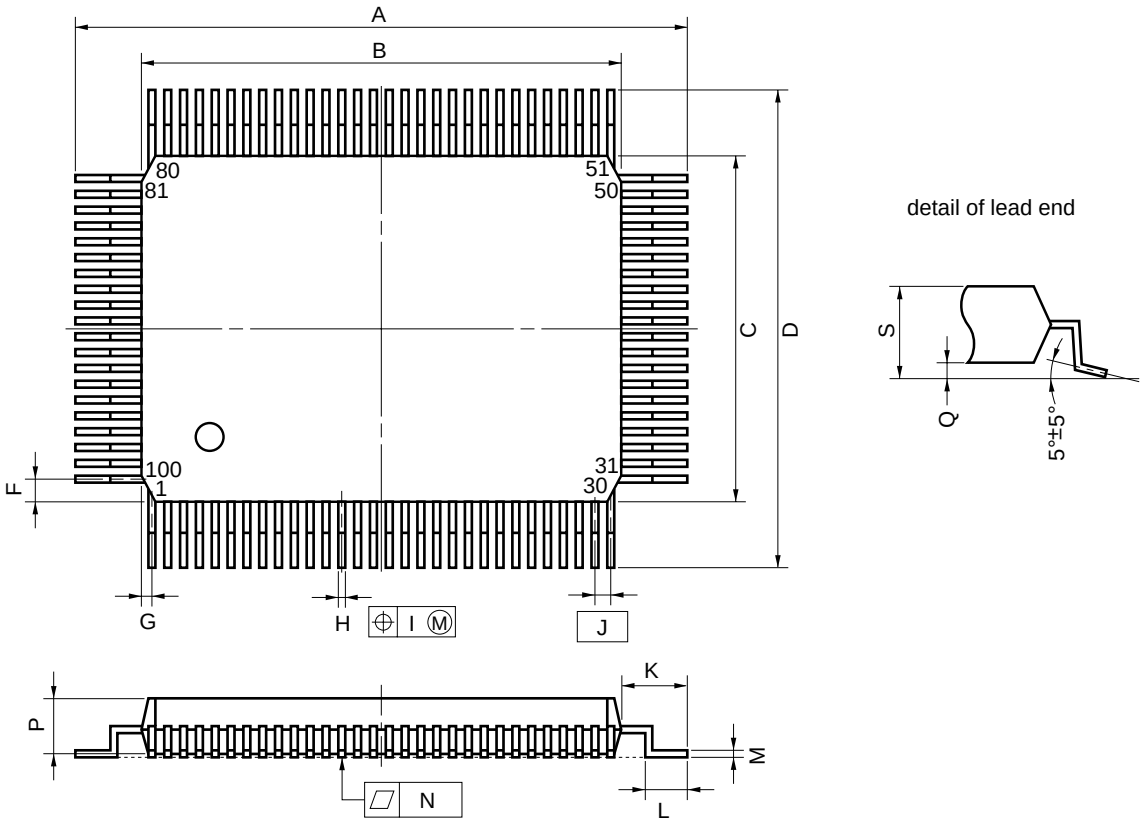


Notes 1. If data need to be read within t_{ACC}, the maximum delay time of $\overline{OE}$ active level input from $\overline{CE}$ falling should be $t_{ACC} - t_{OE}$.

2. t_{DF} is the time after either $\overline{OE}$ or $\overline{CE}$ first rose to V_{IH}.

6. PACKAGE DRAWING

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

7. RECOMMENDED SOLDERING CONDITIONS *

This device should be soldered and mounted under the following conditions.

For details about the recommended conditions, refer to the document “Semiconductor Device Mounting Technology Manual” (C10535E). For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 7-1. Surface Mounting Type Soldering Conditions

μPD78P4916GF-3BA: 100-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared rays reflow	Peak package's surface temperature: 235 ˚C, Reflow time: 30 seconds or less (at 210 ˚C or higher), Number of reflow processes: 2 or less **<Attention>** **(1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow.** **(2) Do not perform flux cleaning of the soldered portion after the first reflow.**	IR35-00-2
VPS	Peak package's surface temperature: 215 ˚C, Reflow time: 40 seconds or less (at 200 ˚C or higher), Number of reflow processes: 2 or less **<Attention>** **(1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow.** **(2) Do not perform flux cleaning of the soldered portion after the first reflow.**	VP15-00-2
Wave soldering	Solder temperature: 260 ˚C or below, Flow time: 10 seconds or less, Number of flow process: 1, Preheating temperature; 120 ˚C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 ˚C or below, Time: 3 seconds or less (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

✱ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are prepared for system development using the μPD78P4916.

Language Software

RA78K4 Note 1	Assembler package common to the 78K/IV Series
CC78K4 Note 1	C compiler package common to the 78K/IV Series
CC78K4-L Note 1	C compiler library source file common to the 78K/IV Series

PROM Writing Tool

PG-1500	PROM programmer
PA-78P4916GF	Programmer adapter connected to the PG-1500
PG-1500 Controller Note 2	Control program for PG-1500

Debugging Tool

IE-784000-R	In-circuit emulator common to the 78K/IV Series
IE-784000-R-BK	Break board common to the 78K/IV Series
IE-784000-R-EM	Emulation board common to the 78K/IV Series
IE-784915-R-EM1	Emulation board for evaluation of the μPD784915 Subseries
IE-78000-R-SV3	Interface adapter when using EWS as a host machine
IE-70000-98-IF-B	Interface adapter when using PC-9800 series (except notebook type) as a host machine
IE-70000-98N-IF	Interface adapter and cable when using notebook type PC-9800 series as a host machine
IE-70000-PC-IF-B	Interface adapter when using IBM PC/AT™ as a host machine
EP-784915GF-R	Emulation probe common to the μPD784915 subseries
EV-9200GF-100	Conversion socket for 100-pin plastic QFP to mount a device on a target system
SM78K4 Note 3	System emulator for all 78K/IV series devices
ID78K4 Note 3	Integrated debugger for IE-784000-R
DF784915 Note 4	Device file common to the μPD784915 subseries

✱ Real-time OS

RX78K/IV Note 4	Real-time OS common to the 78K/IV series
MX78K4 Note 2	OS common to the 78K/IV series

Notes 1. • PC-9800 series (for MS-DOS™) based *

- IBM PC/AT and compatibles (for PC DOS™, Windows™, MS-DOS, and IBM DOS™) based
- HP9000 series 700™ (for HP-UX™) based
- SPARCstation™ (for SunOS™) based
- NEWS™ (NEWS-OS™) based

2. • PC-9800 series (for MS-DOS) based

- IBM PC/AT and its compatibles (for PC DOS, Windows, MS-DOS, and IBM DOS) based

3. • PC-9800 series (for Windows on MS-DOS) based

- IBM PC/AT and its compatibles (for PC DOS, Windows, MS-DOS, and IBM DOS) based
- HP9000 series 700 (for HP-UX) based
- SPARCstation (for SunOS) based

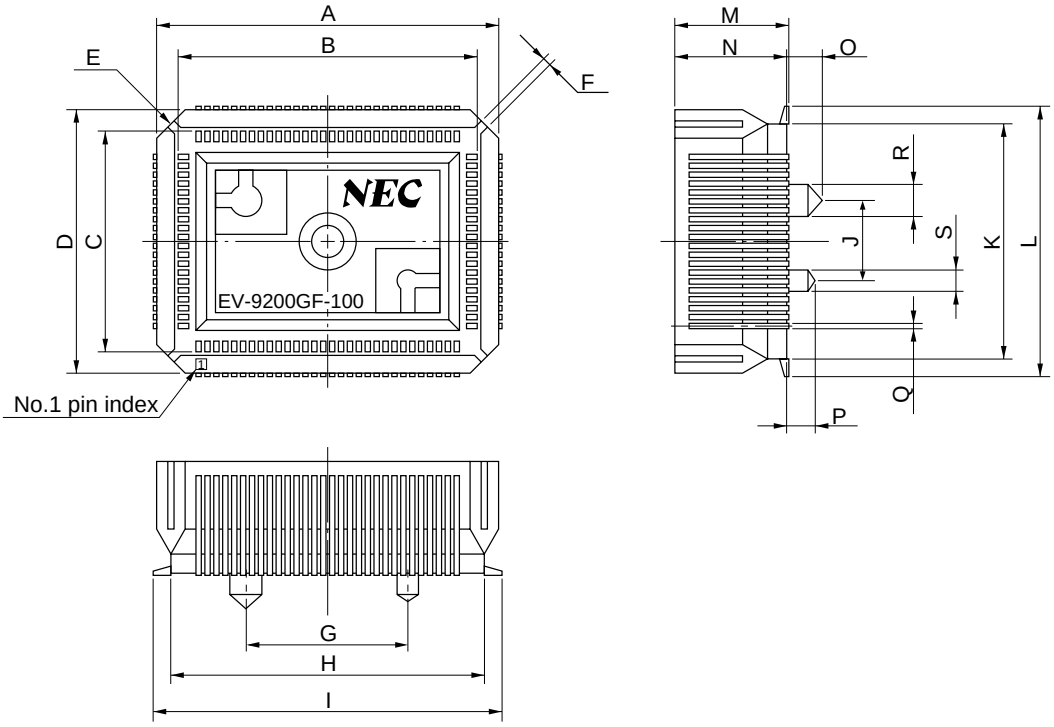
4. • PC-9800 series (for MS-DOS) based

- IBM PC/AT and compatibles (for PC DOS, Windows, MS-DOS, and IBM DOS) based
- HP9000 series 700 (for HP-UX) based
- SPARCstation (for SunOS) based

Remark The RA78K4, CC78K4, SM78K4, and ID78K4 should be used in combination with the DF784915.

✱ APPENDIX B. SOCKET DRAWING AND RECOMMENDED FOOTPRINT

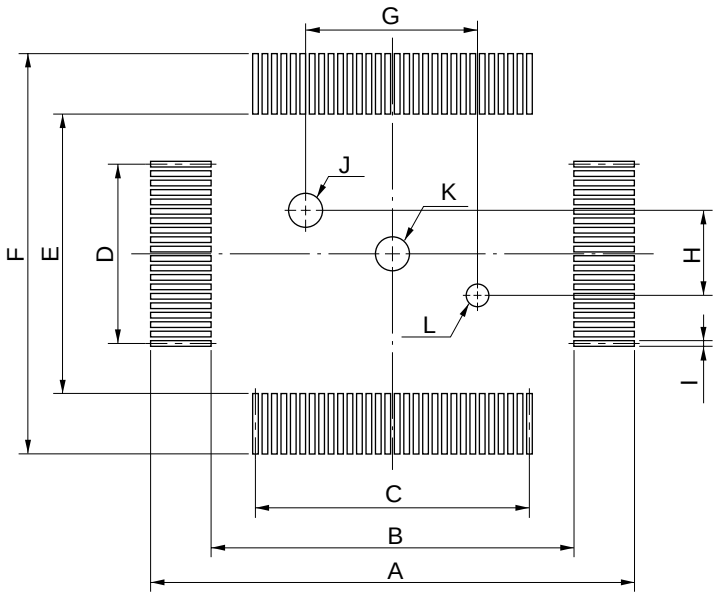
Figure B-1. EV-9200GF-100 Drawing
(For reference purpose only)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure B-2. Recommended EV-9200GF-100 Footprint (For reference purpose only)



EV-9200GF-100-P1

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

✱ APPENDIX C. RELATED DOCUMENTS

Document related to device

Title	Document No.	
	Japanese	English
μPD784915 Subseries User's Manual – Hardware	U10444J	U10444E
μPD784915 Subseries Special Function Register Table	U10976J	—
78K/IV Series User's Manual – Instructions	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	—
78K/IV Series Instruction Set	U10595J	—
78K/IV Series Application Note – Software Basics	U10095J	—

Development tool documents (User's Manual)

Title		Document No.	
		Japanese	English
RA78K Series Assembler Package	Language	EEU-809	EEU-1399
	Operation	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Language	EEU-656	EEU-1280
	Operation	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 series – MS-DOS base		EEU-704	EEU-1291
PG-1500 Controller IBM PC series – PC DOS base		EEU-5008	U10540E
IE-784000-R		EEU-5004	EEU-1534
IE-784915-R-EM1 EP-784915GF-R		U10931J	—
ID78K4 Integrated Debugger – Reference		U10440J	IEU-1412

Embedded-software documents (User's Manual)

Title		Document No.	
		Japanese	English
RX78K/IV Series Real-time OS	Basics	U10604J	—
	Installation	U10603J	—
	Debugger	U10364J	—

Caution The contents of the documents listed above are subject to change without prior notice to users. Be sure to use the latest edition when starting design.

Other documents *

Title	Document No.	
	Japanese	English
Semiconductor Device Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcontroller-Related Product Guide - Third Party Products	MEI-604	—

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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The application circuits and their parameters are for reference only and are not intended for use in actual design-in's.

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