Overview

This document describes changes in the functionality and register map between firmware version 4.8 and version 4.8.7. There are several related documents listed in Table 1 that describe specific functions or details that would overly burden this document.

Table 1. Related Documents

Document Title	Document Description
8A3xxxx Device Datasheet	Contains a functional overview of a specific 8A3xxxx Family device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxxx Family Programming Guide v4.8 dated November 4, 2019	Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.
8A3xxxx Family Programming Guide v4.8.7 dated January 20, 2020	

Table 2. Affected Devices

List of Affected Devices			
8A34001E	8A34013E	8A34046E	8A35024E
8A34002E	8A34041E	8A35000E	8A35025E
8A34003E	8A34042E	8A35001E	8A35027E
8A34004E	8A34043E	8A35003E	8A35029E
8A34011E	8A34044E	8A35004E	8A35032E
8A34012E	8A34045E	8A35012E	8A35036E

Compatibility with Software and EEPROMs Created for Earlier Firmware Versions

8A3xxxx devices running firmware version 4.8.7 are backward compatible with external software and configurations written for firmware version 4.8 that do not alter reserved or undocumented fields in the version 4.8 register map.

8A3xxxx devices will load and execute firmware found on an EEPROM regardless if the version in the EEPROM is older than the version embedded in the chip ROM.

Revision E devices utilize registers from 0x0F40 to 0x0F4F for internal purposes. Care should be taken to ensure that software and EEPROM configurations written for Revision B or C devices and used for Revision E devices does not alter registers from 0x0F40 to 0x0F4F.

Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version	
			v4.8	v4.8.7
Offset Address (Hex)	Individual Register Name	Register Description	Default Value	Default Value
010h	GENERAL_STATUS.MAJ_REL	Major release number.	09h	09h
011h	GENERAL_STATUS.MIN_REL	Minor release number.	08h	08h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number.	00h	07h

Functional Differences

The following tables describe the functional differences between firmware version 4.8 and version 4.8.7.

Issue Number: BRMBXR-1830	
Firmware	**Functional Difference**
v4.8	STATUS.DPLLx_REF_STAT reports 0x1F instead of 0x11 when selected reference is write-frequency input.
v4.8.7	Corrected.

Issue Number: BRMBXR-2124	
Firmware	**Functional Difference**
v4.8	The Maximum Time Interval Error (MTIE) for hitless reference switching depends on the phase difference between the two references. A DCO can be used as a “satellite DCO” for a DPLL channel; in this way it provides additional frequency synthesis and outputs for its master DPLL. Output TDCs are used to align the output phase of a satellite DCO with the output phase of its master DPLL.
v4.8.7	Added the HITLESS_TYPE control bit. HITLESS_TYPE = 0: ▪ Hitless reference switching algorithm is similar to v4.8 but with improved phase measurement precision that reduces the resulting MTIE HITLESS_TYPE = 1: ▪ Enables a hitless reference switching algorithm with MTIE that is reduced and that does not depend on the phase difference between the two references A DCO can be used as a “satellite DCO” for a DPLL channel; in this way it provides additional frequency synthesis and outputs for its master DPLL. Output TDCs are used to align the output phase of a satellite DCO with the output phase of its master DPLL. If a DPLL is using HITLESS_TYPE = 1, then when that DPLL executes a hitless reference switch any satellite DCOs following that DPLL will exhibit a small (several ps) random phase change relative to the DPLL. These phase changes will accumulate with each hitless reference switching event.

Issue Number: BRMBXR-2378	
Firmware	**Functional Difference**
v4.8	Fast lock cannot be triggered when transitioning from the Locked state to the Lock Recovery state. This can lead to long recovery times if the phase of the reference input clock changes significantly when the PLL is locked.
v4.8.7	Fast lock can be triggered when transitioning from the Locked state to the Lock Recovery state.

Issue Number: BRMBXR-2485	
Firmware	**Functional Difference**
v4.8	GPIO Soft Control Status Register (SCSR) Status Registers are not updated when the GPIO function is set as LOS indicator.
v4.8.7	Corrected.

Issue Number: BRMBXR-2612	
Firmware	**Functional Difference**
v4.8	IN[15:0]_TRANS_DETECT_STICKY/LIVE/MASK bits were not implemented.
v4.8.7	IN[15:0]_TRANS_DETECT_STICKY/LIVE/MASK bits have been implemented.

Issue Number: BRMBXR-2739	
Firmware	**Functional Difference**
v4.8	Changes to input configuration through SCSRs cause the DPLL state machine to reset if it was tracking that input.
v4.8.7	Corrected.

Issue Number: BRMBXR-2886	
Firmware	**Functional Difference**
v4.8	DPLL Fast Lock is not supported when the reference clock is an internal feedback clock from another channel.
v4.8.7	DPLL Fast Lock is supported when the reference clock is an internal feedback clock from another channel.

Issue Number: BRMBXR-2941	
Firmware	**Functional Difference**
v4.8	When a DPLL channel is put into Phase Measurement mode the associated FOD is disabled. When a DPLL channel is put into Phase Measurement mode the filter_status word is automatically enabled for phase measurements. However, the TDC frequency is not automatically adjusted to ensure the TDC frequency is not an integer multiple of the input clock frequencies being measured. In this state, the TDC and digital filter are not properly configured for fine phase measurements. See AN-1010 for more information about configuring TDCs for finer measurement resolution.
v4.8.7	When a DPLL channel is put into Phase Measurement mode the associated FOD is available to generate a clock. When a DPLL channel is put into Phase Measurement mode the filter_status word is not automatically enabled for phase measurements.

Issue Number: BRMBXR-2950	
Firmware	**Functional Difference**
v4.8	When GPIO function 0x4 or 0x5 are enabled (inc DCO FFO (in), dec DCO FFO (in)), it causes the SYS_DPLL to behave like it is in freerun.
v4.8.7	Corrected.

Issue Number: BRMBXR-2952	
Firmware	**Functional Difference**
v4.8	The reference frequency monitor does not work for 0.5Hz reference clocks.
v4.8.7	Corrected.

Issue Number: BRMBXR-2955	
Firmware	**Functional Difference**
v4.8	DPLLs can generate unexpected phase transients when locking to a clock and frame pulse pair or a clock and sync pulse pair using high DPLL bandwidth (Bandwidth > 1kHz).
v4.8.7	Corrected.

Issue Number: BRMBXR-2970	
Firmware	**Functional Difference**
v4.8	Output dividers for Q8 and Q11 are not re-synchronized when the output muxes are reconfigured using FOD5_TO_OUT_DIV8 or FOD6_TO_OUT_DIV11.
v4.8.7	Corrected.

Issue Number: BRMBXR-2974	
Firmware	**Functional Difference**
v4.8	When a channel is configured as an open loop DCO, its internal feedback signal can be used as a reference for a DPLL channel. When the device configures the feedback divider to set the frequency of the internal feedback signal it always assumes the FOD frequency is 500MHz.
v4.8.7	Corrected.

Issue Number: BRMBXR-2986	
Firmware	**Functional Difference**
v4.8	When the output TDCs are used to align the phase of a DCO channel with the phase of another DPLL or DCO channel that is using a different FOD frequency then there will be a static phase offset between the two channels of up to 9ns.
v4.8.7	Corrected.

Issue Number: BRMBXR-3005	
Firmware	**Functional Difference**
v4.8	When DPLLs try to exit the forced holdover state to enter the automatic state, the state machine returns to the forced holdover state.
v4.8.7	Corrected.

Issue Number: BRMBXR-3027	
Firmware	**Functional Difference**
v4.8	DPLL channels in frame pulse / sync pulse mode during reference switching with high DPLL bandwidth (bandwidth > 1kHz) will generate an unexpected output phase transient.
v4.8.7	Corrected.

Issue Number: BRMBXR-3059	
Firmware	**Functional Difference**
v4.8	A GPIO in Lock or Holdover Indicator mode does not retain its active output if the relevant GPIO config module trigger is re-triggered. The GPIO state is updated only upon an event transition when indicating Lock and Holdover.
v4.8.7	Corrected.

Issue Number: BRMBXR-3079	
Firmware	**Functional Difference**
v4.8	If a DPLL is configured while its FOD frequency is 0Hz then when the FOD is subsequently programmed to generate an output clock the FOD will generate an incorrect frequency for 10s.
v4.8.7	Corrected.

Issue Number: BRMBXR-3209	
Firmware	**Functional Difference**
v4.8	DPLLs that enter automatic holdover due to the detection of a Loss Of Signal (LOS) event on the input clock can, in rare cases, generate an output phase transient that exceeds datasheet limits. Note: Automatic reference switching events that are triggered by the detection of a LOS event cause entry into automatic holdover and are affected by this issue.
v4.8.7	Corrected.

Issue Number: BRMBXR-3212	
Firmware	**Functional Difference**
v4.8	When a DPLL is disabled the associated FOD cannot be disabled and still draws power.
v4.8.7	When a DPLL is disabled the associated FOD can be disabled so that it does not draw power.

Register Addresses with Differences Between Versions 4.8 and 4.8.7

The register addresses and descriptions in the following tables are according to firmware version 4.8.7. The registers listed in these tables are defined and/or described differently than the same register addresses for firmware version 4.8. Please refer to the 8A3xxxx Family Programming Guide v4.8 and v4.8.7 for the full descriptions of these registers.

Register Module Base Address: C03Ch		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
008h	STATUS.IN0_MON_STATUS	Input 0 reference monitor status.
009h	STATUS.IN1_MON_STATUS	Input 1 reference monitor status.
00Ah	STATUS.IN2_MON_STATUS	Input 2 reference monitor status.
00Bh	STATUS.IN3_MON_STATUS	Input 3 reference monitor status.
00Ch	STATUS.IN4_MON_STATUS	Input 4 reference monitor status.
00Dh	STATUS.IN5_MON_STATUS	Input 5 reference monitor status.
00Eh	STATUS.IN6_MON_STATUS	Input 6 reference monitor status.
00Fh	STATUS.IN7_MON_STATUS	Input 7 reference monitor status.
010h	STATUS.IN8_MON_STATUS	Input 8 reference monitor status.
011h	STATUS.IN9_MON_STATUS	Input 9 reference monitor status.
012h	STATUS.IN10_MON_STATUS	Input 10 reference monitor status.
013h	STATUS.IN11_MON_STATUS	Input 11 reference monitor status.
014h	STATUS.IN12_MON_STATUS	Input 12 reference monitor status.
015h	STATUS.IN13_MON_STATUS	Input 13 reference monitor status.
016h	STATUS.IN14_MON_STATUS	Input 14 reference monitor status.
017h	STATUS.IN15_MON_STATUS	Input 15 reference monitor status.
018h	STATUS.DPLL0_STATUS	DPLL 0 status.
019h	STATUS.DPLL1_STATUS	DPLL 1 status.
01Ah	STATUS.DPLL2_STATUS	DPLL 2 status.
01Bh	STATUS.DPLL3_STATUS	DPLL 3 status.
01Ch	STATUS.DPLL4_STATUS	DPLL 4 status.
01Dh	STATUS.DPLL5_STATUS	DPLL 5 status.
01Eh	STATUS.DPLL6_STATUS	DPLL 6 status.
01Fh	STATUS.DPLL7_STATUS	DPLL 7 status.

Register Module Base Address: C188h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
000h	ALERT_CFG.IN1_0_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 0 and 1.
001h	ALERT_CFG.IN3_2_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 2 and 3.
002h	ALERT_CFG.IN5_4_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 4 and 5.
003h	ALERT_CFG.IN7_6_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 6 and 7.
004h	ALERT_CFG.IN9_8_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 8 and 9.
005h	ALERT_CFG.IN11_10_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 10 and 11.
006h	ALERT_CFG.IN13_12_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 12 and 13.
007h	ALERT_CFG.IN15_14_MON_ALERT_MASK	GPIO alert enable masks for reference monitors 14 and 15.

Register Module Base Address: C194h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
006h	SYS_DPLL_XO.XO_FREQ	XO_DPLL frequency in Hz.
007h	SYS_DPLL_XO.XO_FREQ	XO_DPLL frequency in Hz.

Register Module Base Address: C19Ch		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
00Eh	SYS_APLL.SYS_APLL_XTAL_FREQ	System APLL crystal frequency in Hz.
00Fh	SYS_APLL.SYS_APLL_XTAL_FREQ	System APLL crystal frequency in Hz.

Register Module Base Address: C1B0h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
006h	INPUT_0.IN_FREQ	Input frequency in Hz.
007h	INPUT_0.IN_FREQ	Input frequency in Hz.

Register Module Base Address: C3B0h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
003h	DPLL_0.DPLL_CTRL_1	Configure other hitless switch features and DPLL feedback as a reference.
00Fh	DPLL_0.DPLL_REF_PRIORITY_0	Select input for highest (0) priority.
010h	DPLL_0.DPLL_REF_PRIORITY_1	Select input for priority 1.
011h	DPLL_0.DPLL_REF_PRIORITY_2	Select input for priority 2.
012h	DPLL_0.DPLL_REF_PRIORITY_3	Select input for priority 3.
013h	DPLL_0.DPLL_REF_PRIORITY_4	Select input for priority 4.
014h	DPLL_0.DPLL_REF_PRIORITY_5	Select input for priority 5.
015h	DPLL_0.DPLL_REF_PRIORITY_6	Select input for priority 6.
016h	DPLL_0.DPLL_REF_PRIORITY_7	Select input for priority 7.
017h	DPLL_0.DPLL_REF_PRIORITY_8	Select input for priority 8.
018h	DPLL_0.DPLL_REF_PRIORITY_9	Select input for priority 9.
019h	DPLL_0.DPLL_REF_PRIORITY_10	Select input for priority 10.
01Ah	DPLL_0.DPLL_REF_PRIORITY_11	Select input for priority 11.
01Bh	DPLL_0.DPLL_REF_PRIORITY_12	Select input for priority 12.
01Ch	DPLL_0.DPLL_REF_PRIORITY_13	Select input for priority 13.
01Dh	DPLL_0.DPLL_REF_PRIORITY_14	Select input for priority 14.
01Eh	DPLL_0.DPLL_REF_PRIORITY_15	Select input for priority 15.
01Fh	DPLL_0.DPLL_REF_PRIORITY_16	Select input for priority 16.
020h	DPLL_0.DPLL_REF_PRIORITY_17	Select input for priority 17.
021h	DPLL_0.DPLL_REF_PRIORITY_18	Select input for priority 18.
036h	DPLL_0.DPLL_PHASE_MEASUREMENT_CFG	Phase measurement mode configuration.
037h	DPLL_0.DPLL_MODE	DPLL operating modes.

Register Module Base Address: C600h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
022h	DPLL_CTRL_0.DPLL_FOD_FREQ	Fractional Output Divider (FOD) frequency in Hz.
023h	DPLL_CTRL_0.DPLL_FOD_FREQ	Fractional Output Divider (FOD) frequency in Hz.

Register Module Base Address: C8C2h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
001h	GPIO_0.GPIO_OUT_CTRL_0	GPIO controlled output squelch for outputs 0–7.
002h	GPIO_0.GPIO_OUT_CTRL_1	GPIO controlled output squelch for outputs 8–11.

Register Module Base Address: CC00h		
Offset Address (Hex)	**Individual register Name**	**Register Description**
00Fh	TOD_WRITE_0.TOD_WRITE_CMD	TOD write trigger selection.

Register Module Base Address: CC40h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
00Dh	TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_SEL_CFG_1	TOD read trigger configuration.
00Eh	TOD_READ_PRIMARY_0.TOD_READ_PRIMARY_CMD	TOD read trigger selection.

Register Module Base Address: CC90h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
00Dh	TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_SEL_CFG_1	TOD read trigger configuration.
00Eh	TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD	TOD read trigger selection.

Register Module Base Address: CD00h		
Offset Address (Hex)	**Individual Register Name**	**Register Description**
004h	OUTPUT_TDC_0.OUTPUT_TDC_CTRL_2	Output TDC control register.
005h	OUTPUT_TDC_0.OUTPUT_TDC_CTRL_3	Output TDC control register.

Register Module Base Address: CD20h		
Offset Address (Hex)	**Individual register Name**	**Register Description**
004h	INPUT_TDC.INPUT_TDC_FBD_CTRL	Input TDC feedback divider control.

Revision History

Revision Date	Description of Change
December 1, 2020	Updated functional difference descriptions for Issue Number: BRMBXR-2941.
January 24, 2020	This is the first release of 8A3xxxx Firmware Version 4.8.7 Release Notes.

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