System Requirements for Software:
The HSP50216 / ISL5216 evaluation board requires an IBM PC compatible computer with an available parallel interface (printer) port or Universal Serial Bus (USB) port. A 120 MHz Pentium or faster CPU and 800x600 or higher screen resolution is recommended. The supported operating systems and interface types are shown below. The USB interface (USBINTERFACE-DBEVAL1) is a daughterboard which connects to the HSP50216 / ISL5216 evaluation board. Up to 8 evaluation boards may be connected to a computer's USB interface using these daughterboards. Only one evaluation board may be connected to a parallel port.

Operating System	Parallel Port supported	USB supported
Microsoft Windows 95	X	
Microsoft Windows 98	X	X
Microsoft Windows NT 4	X	
Microsoft Windows 2000	X	X

Software Installation:
Windows 95 / Windows 98 using parallel port:

1. Run the self-extracting zip exe file 216SETUP.EXE
2. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
3. Click "Unzip".
4. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows NT 4 / Windows 2000 using parallel port:

1. Log into the computer using an account with administrator access.
2. Run the self-extracting zip exe file 216SETUP.EXE
3. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
4. Click "Unzip".
5. Run port95nt.exe (Scientific Software Tools, Inc.'s DriverLINX installer program) and follow the on-screen instructions. This installs drivers used by the evaluation board software to access I/O ports. Information on this driver is available on SST's website at http://www.sstnet.com.
6. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows 98 using USB port:

1. Run the self-extracting zip exe file 216SETUP.EXE
2. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
3. Click "Unzip".
4. Set the 3 binary address switches on the USB daughterboard to a unique address (0 – 7).
5. Connect the USB daughterboard to the computer's USB port.
6. When the "Add New Hardware Wizard" box appears, click "Next".
7. Verify that "Search for the best driver for your device. (Recommended)" is checked and click "Next".
8. Click "Specify a location" and enter the path to the HSP50216 directory created above (default of "C:\HSP50216"), click "Next".
9. Verify driver file search finds "Intersil HSP50216 / ISL5216 Eval Board (no firmware)", click Next.

10. Click “Finish”.
11. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows 2000 using USB port:

1. Log into the computer using an account with administrator access.
2. Run the self-extracting zip exe file 216SETUP.EXE
3. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
4. Click “Unzip”.
5. Set the 3 binary address switches on the USB daughterboard to a unique address (0 – 7).
6. Connect the USB daughterboard to the computer’s USB port.
7. When “Found New Hardware Wizard” appears, click “Next”
8. Verify that “Search for a suitable driver for my device (recommended)” is checked and click “Next”.
9. Click “Specify a location” and click “Next”.
10. Enter the path to the HSP50216 directory created above (default of “C:\HSP50216”) and click “Next”.
11. Click “Finish” and reboot the computer if asked.
12. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows NT 4 and Windows 2000 installations (parallel or USB) require an administrator account to install the necessary drivers. Once installed, user accounts will be able to access the hardware.

Evaluation Board Hardware Configuration:

For parallel port connections, the port should be configured for ECP-mode. This option is often available in the computer’s BIOS settings.

Jumper Settings: JP7

Evaluation board JP7 pins 7 and 9 should be shorted to connect the HSP50216/ISL5216’s SYNCO to SYNCI (on Sigtek ST-116 boards, this is J10 pins 7 and 9). JP1 should be set for the desired clock source: pins 1 and 2 if the clock is provided on J4 (parallel input bus C) or J2 (LVDS bus A), or 2 and 3 if the clock source is the on-board 32 MHz oscillator.

Power:

The board uses 5V DC power. On the cable provided for connecting to a power supply, the wire with the white stripe is the +5 volt lead (center conductor is positive). The eval board currently uses approximately 500 - 600 mA at 5V and 32 MHz. There are 3.3V and 2.5V regulators on the board to supply the HSP50216 (3.3V) / ISL5216 (3.3V and 2.5V) and other 3.3V devices. Note that the Sigtek ST-116 boards use an HSP50216 and have only the 3.3V regulator.

Inputs:

The I/O busses have receivers/drivers with 5V tolerant I/Os, however, pins connected directly to the HSP50216/ISL5216 ARE NOT 5V tolerant.

Inputs J4 (parallel input bus C) and J5 (parallel input bus D) are compatible with the pinout of the HSP50215EVAL. The JP4 (LVDS bus A) and JP5 (LVDS bus B) inputs are high speed serial inputs using National Semiconductor’s “ChannelLink” serial LVDS parts. On the Sigtek ST-116, these are referred to as J2 and J3 respectively.

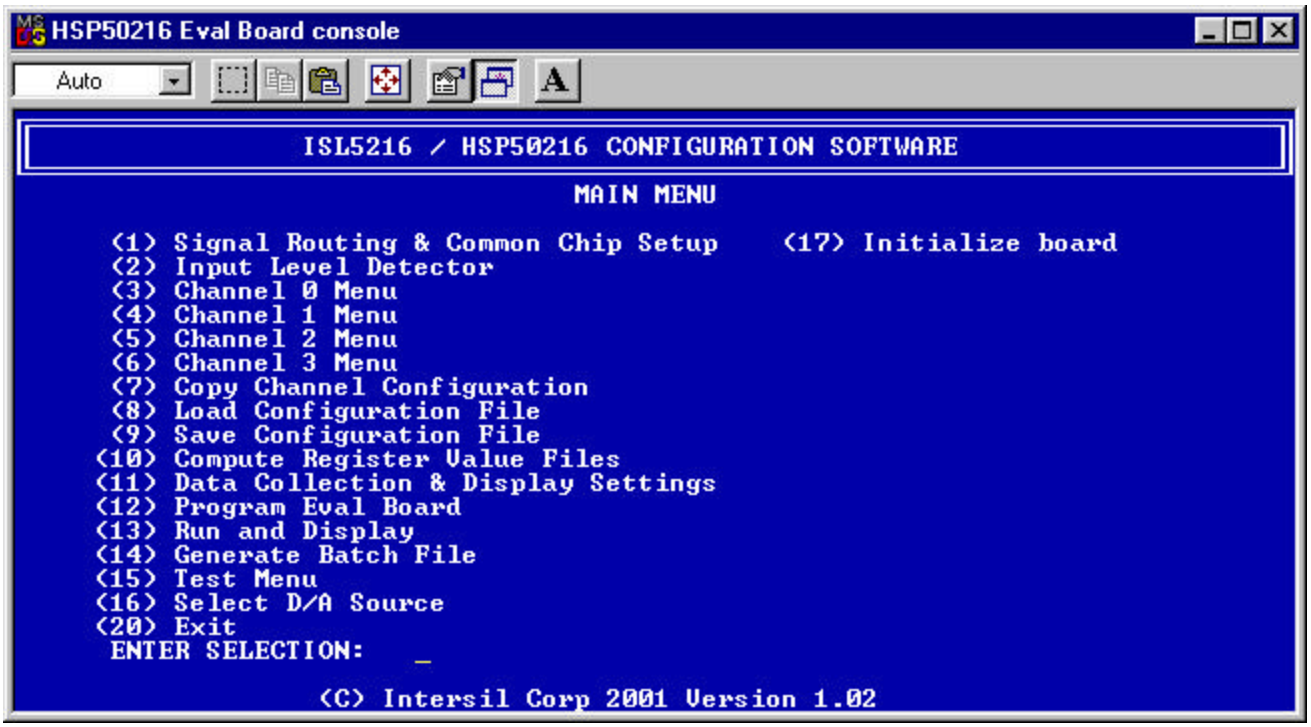
Due to the difficulty in aligning the clocks for the two types of inputs, it is expected that one or the other input type will be used at a time but not both.
The clock for parallel port inputs J4 and J5 comes in on the J4 connector. The clock for LVDS inputs JP4 and JP5 comes in on the JP4 connector (J2 for the Sigtek board). The input clock is distributed using a PLL-based zero delay buffer. This part (and therefore the board) has a minimum input clock rate of 20 MHz.

DAC outputs
A dual 12-bit D/A (Intersil HI5828) is provided for observing the output signals on an oscilloscope or spectrum analyzer. It outputs to phono-plug J7 and 3-pin header J8. The initial build of the Sigtek boards has a series capacitor in the D/A output path that limits the low frequency response to J7 and J8. This has been replaced in later Sigtek boards with a zero ohm resistor. The ISL5216EVAL1 board has J7 capacitively coupled and J8 DC coupled.

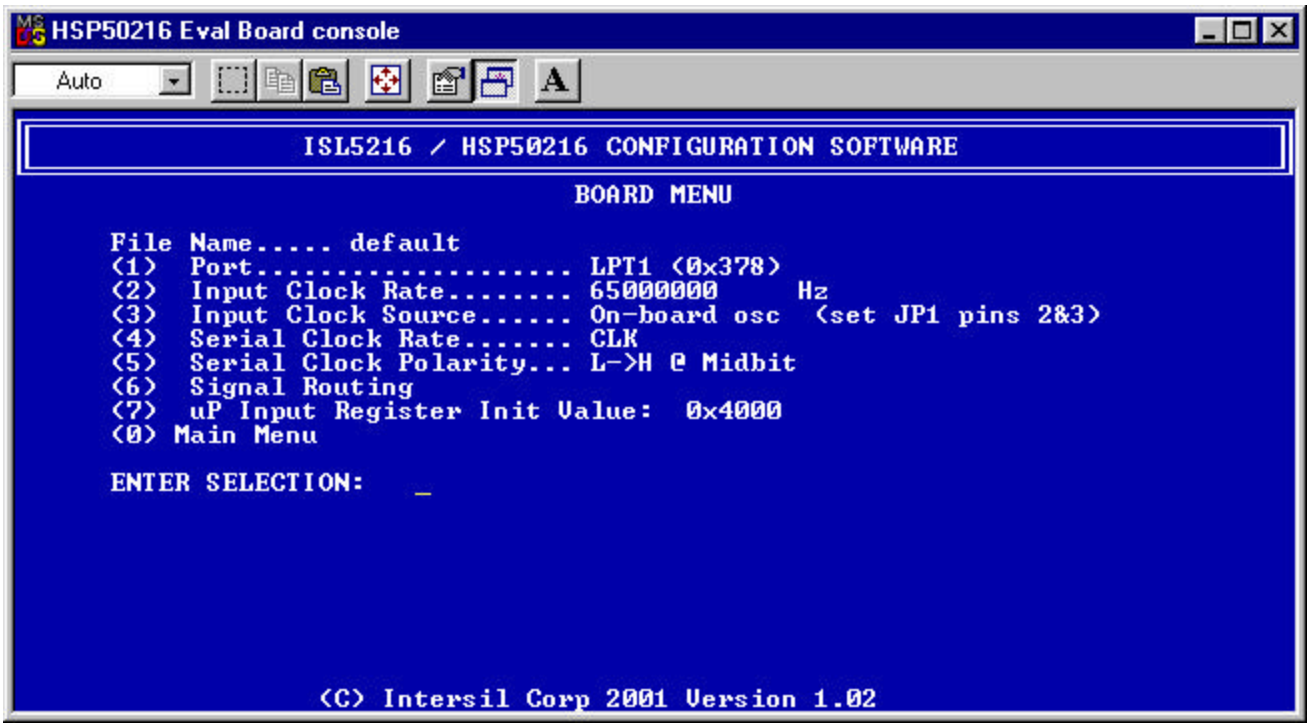
Note that when using the resampler or interpolation halfband filters, the spacing between samples can be uneven and will time-distort the DAC signals. The FIFO delay in the 216 may need to be adjusted for optimum analog performance, but normally a setting of "AUTO" in the software will provide the correct FIFO delay. The FIFO was intended mainly to spread output samples from the interpolation halfband filters. It can partially de-jitter the resampler or resampler plus one interpolation halfband filter combination, but the FIFO is not deep enough to de-jitter a resampler/2-IHBF combination.

A note on rates
For testing with non-real-time signals, the clock rate and sample rate in the menus do not have to match the input clock for the board. For example, the clocks in the menus can be set to 65 MHz while the clock for the board is actually 32 MHz (the on-board oscillator frequency). The frequencies in the displays and calculated register values will reflect the menu clock rates.

Running the Software:
Start the program by running HSP50216.EXE.



Select main menu item 1 for the board menu to set the port and clock settings.



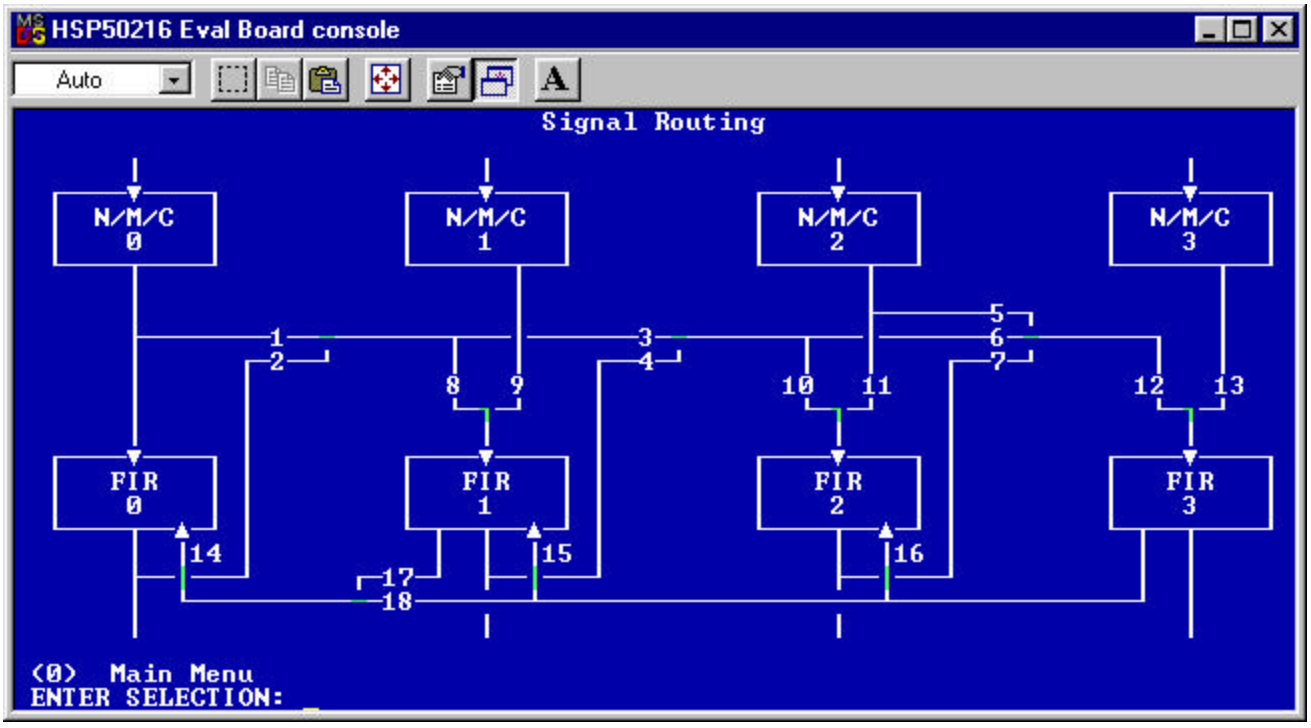
Port: this setting is used to specify how the evaluation board is connected to the computer. Enter 1, 2, or 3 for LPT1, LPT2, LPT3, respectively, or the base address in hex for a non-standard parallel port (for example, enter "0x290" for a parallel port at 290H). For a USB interface, enter –0 to –7 for USB board addresses of 0 through 7.

Input Clock Rate: clock rate of the HSP50216 in Hz. As stated above in “A note on rates”, this frequency does not need to be the actual clock rate on the eval board. It is used in register calculations and to report configuration warnings. Enter the rate of the clock that will be used in the final application.

Input clock source: selects between on-board oscillator (32 MHz), JP4 / J2 (LVDS) clock input or J4 (parallel bus) clock input. Note that a change to JP1 may also be required when changing this.

Serial Clock Rate and Serial Clock Polarity affect the SCLK timing. These should be left alone when targeting the evaluation board for testing, but may be set as needed when generating register files for a final design.

Signal routing:
This screen controls the HSP50216 / ISL5216 global write address register F801H (bus routing control). This allows channels to be cascaded or polyphased to increase bandwidth or allow for more filter taps. In the screen below, for example, all 4 channels are combined into a single polyphase filter. Selections 1 – 13 change the signal routing while selections 14 – 18 control the AGC routing. In this case, channel 0’s NCO / mixer / CIC output to all 4 filter compute engines (FIR0 – FIR3). Channel 3’s AGC sets the gain for channels 0, 1 and 2 by way of paths 14, 18, 15, and 16. Paths 14, 15, and 16 may be toggled on or off as desired, allowing channels to control their own gains. Entering 0 from this screen returns to the board menu.

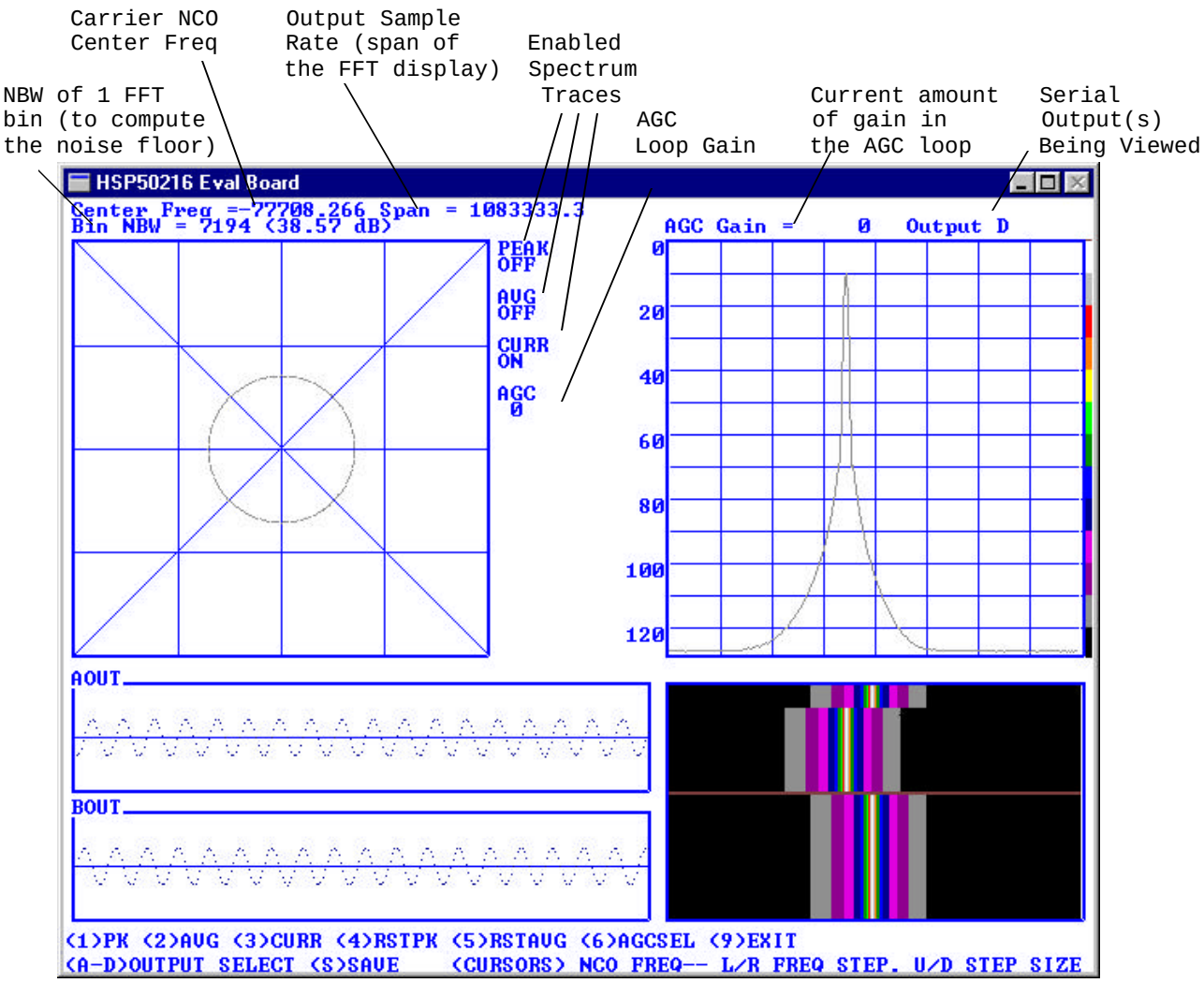


Select 0 from the board menu to return to the main menu. From the main menu, select option 17 to initialize the board. Board initialization consists of programming the FPGA and configuring the clock buffers according to the settings made in the board menu. After successful board initialization, the HSP50216 is ready for register loading.

To calculate the register values from the current configuration data, select option 10 from the main menu. A set of files is produced with file extensions of ".r0", ".r1", ".r2", ".r3" and ".rtp" for channels 0, 1, 2, 3 and the global registers, respectively. These files contain the actual values to be loaded into the device for the given configuration. They are human-readable text files with each line having a 16 bit integer register number and a 32 bit integer value, both in hex. Additionally, an ".sta" report file is created to summarize FIR engine clock and memory usage – information which is useful in determining whether longer filters can be implemented. During register value computation, error messages will appear if certain device limitations are exceeded. After returning to the main menu, the ".sta" file can be opened to determine how to correct the problem. The initial file prefix for the six files described above is "default". This is changed when the configuration data are saved (main menu option 9) or loaded (main menu option 8).

Once the register values are calculated, select main menu item 12 to configure the part. The ".r0", ".r1", ".r2", ".r3" and ".rtp" files created above are downloaded to the HSP50216 / ISL5216 and a SYNCO is generated. Normally JP7 (Sigtek's J10) pins 7 and 9 are shorted so that SYNCO is connected directly to SYNCI, enabling inputs and synchronizing blocks programmed to respond to SYNCI.

Main menu item 13 ("Run and Display") provides the graphics window shown below to collect and display the output samples. While running, the evaluation board hardware captures 256 sample snapshots which are then transferred to the computer for FFT computation and display. The text at the bottom of the window lists the key functions available —
"1": toggles peak on / off
"2": toggles average on / off
"3": toggles current (real-time) FFT on / off
"4": resets peak trace
"5": resets average trace
"6": toggles between the two AGC loop gains
"A"-"D": selects the serial output to monitor (if other than D, it must be sync'd to D) . N/A in polyphase mode.
The left and right arrow keys step the carrier center frequency. The up and down arrow keys increase or decrease the step size (amount carrier frequency changes when left/right arrow keys are pressed). The step size range is 2^N FFT bins with N = 0 to 8.


Carrier NCO Center Freq
Output Sample Rate (span of the FFT display)
Enabled Spectrum Traces
NBW of 1 FFT bin (to compute the noise floor)
AGC Loop Gain
Current amount of gain in the AGC loop
Serial Output(s) Being Viewed
HSP50216 Eval Board
Center Freq =-77708.266 Span = 1083333.3
Bin NBW = 7194 (38.57 dB)
AGC Gain = 0 Output D
PEAK OFF
AVG OFF
CURR ON
AGC 0
0
20
40
60
80
100
120
AOUT
BOUT
(1)PK (2)AVG (3)CURR (4)RSTPK (5)RSTAVG (6)AGCSEL (9)EXIT
(A-D)OUTPUT SELECT (S)SAVE (CURSORS) NCO FREQ-- L/R FREQ STEP. U/D STEP SIZE