

# Renesas Flexible Software Package (FSP) v.3.2.0

User's Manual

## Renesas RA Family

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# Chapter 1 Introduction

## 1.1 Overview

This manual describes how to use the Renesas Flexible Software Package (FSP) for writing applications for the RA microcontroller series.

## 1.2 Using this Manual

This manual provides a wide variety of information, so it can be helpful to know where to start. Here is a short description of each main section and how they can be used.

**Starting Development** - Provides a step by step guide on how to use e2 studio and FSP to develop a project for RA MCUs. This is a good place to start to get up to speed quickly and efficiently.

**FSP Architecture** - Provides useful background material on key FSP concepts such as Modules, Stacks, and API standards. Reference this section to extend or refresh your knowledge of FSP concepts.

**API Reference** - Provides detailed information on each module and interface including features, API functions, configuration settings, usage notes, function prototypes and code examples. Board Support Package (BSP) related API functions are also included.

### Note

*Much of the information in the API Reference section is available from within the e2 studio tool via the [Developer Assistance](#) feature. The information here can be referenced for additional details on API features.*

## 1.3 Documentation Standard

Each **Modules** section user guide outlines the following:

- **Features:** A bullet list of high level features provided by the module.
- **Configuration:** A description of module specific configurations available in the RA Configuration editor.
- **Usage Notes:** Module specific documentation and limitations.
- **Examples:** Example code provided to help the user get started.
- **API Reference:** Usage notes for each API in the module, including the function prototype and hyperlinks to the interface documentation for parameter definitions.

Each **Interfaces** section user guide outlines the following:

- **Detailed Description:** A short description and summary of the interface functionality.
- **Data Structures:** A list and definition of each data structure used by the interface including the structure of the pointers that define the API and are shared by all modules that implement the interface.
- **Typedefs:** A list and description of the typedefs used by the interface.
- **Enumerations:** A list and description of the enumerations used by the interface.

## 1.4 Introduction to FSP

### 1.4.1 Purpose

The Renesas Flexible Software Package (FSP) is an optimized software package designed to provide easy to use, scalable, high quality software for embedded system design. The primary goal is to provide lightweight, efficient drivers that meet common use cases in embedded systems.

### 1.4.2 Quality

FSP code quality is enforced by peer reviews, automated requirements-based testing, and automated static analysis.

### 1.4.3 Ease of Use

FSP provides uniform and intuitive APIs that are well documented. Each module is supported with detailed user documentation including example code.

### 1.4.4 Scalability

FSP modules can be used on any MCU in the RA family, provided the MCU has any peripherals required by the module.

### 1.4.5 Build Time Configurations

FSP modules also have build time configurations that can be used to optimize the size of the module for the feature set required by the application.

### 1.4.6 e2 studio IDE

FSP provides a host of efficiency enhancing tools for developing projects targeting the Renesas RA series of MCU devices. The e2 studio IDE provides a familiar development cockpit from which the key steps of project creation, module selection and configuration, code development, code generation, and debugging are all managed.

# Chapter 2 Starting Development

## 2.1 Starting Development Introduction

The wealth of resources available to learn about and use e2 studio and FSP can be overwhelming on first inspection, so this section provides a Starting Development Guide with a list of the most important initial steps. Following these highly recommended first 11 steps will bring you up to speed on the development environment in record time. Even experienced developers can benefit from the use of this guide, to learn the terminology that might be unfamiliar or different from previous environments.

1. Read the section [What is e2 studio?](#), up to but not including [e2 studio Prerequisites](#). This will provide a description of the various windows and views to use e2 studio to create a project, add modules and threads, configure module properties, add code, and debug a project. It also describes how to use key coding 'accelerators' like Developer Assist (to drag and drop parameter populated API function calls right into your code), a context aware Autocomplete (to easily find and select from suggested enumerations, functions, types, and many other coding elements), and many other similar productivity enhancers.
2. Read the [FSP Architecture](#), [FSP Modules](#) and [FSP Stacks](#) sections. These provide the basic background on how FSP modules and stacks are used to construct your application. Understanding their definitions and the theory behind how they combine will make it easier to develop with FSP.
3. Read a few [Modules](#) sections to see how to use API function calls, structures, enumerations, types and callbacks. These module guides provide the information you will use to implement your project code.
4. After you have a Kit and you have downloaded and installed e2 studio and FSP, you can build and debug a simple project to test your installation, tool flow, and the kit. (If you do not have a Kit or have not yet installed the development software, use the links included in the [e2 studio Prerequisites](#) for more information.) The simple [Tutorial: Your First RA MCU Project - Blinky](#) will Blink an LED on and off. Follow the instructions for importing and running this project in section [Create a New Project for Blinky](#). It will use some of the key steps for managing projects within e2 studio and is a good way to learn the basics.
5. Once you have successfully run Blinky you have a good starting point for using FSP for more complex projects. The Using HAL Drivers Tutorial, available at [Tutorial: Using HAL Drivers - Programming the WDT](#), shows how to create a project from scratch, using FSP API functions. Do this next.
6. Several Hands-on Quick FSP Labs are available that cover key development topics with short 15-minute Do it Yourself (DIY) activities targeting the EK-RA6M3. Topics covered include code development accelerators like Developer Assistance, Autocomplete, Help, Visual Expressions and using Example Projects. The complete list of available Quick FSP Labs can be found here: <https://en-support.renesas.com/knowledgeBase/category/31087/subcategory/31090>. Doing a couple of these labs provides further details on using FSP, and is also good practice. Running these labs is highly recommended.
7. The balance of the [FSP Architecture](#) sections (that is, those not called out in step 2 above) contain additional reference material that may be helpful in the future. Scan them so you know what they contain, in case you need them.
8. The balance of the e2 studio User Guide, starting with the [What is a Project?](#) section up to, but not including, [Writing the Application](#) section, provides a detailed description of each of

the key steps, windows, and entries used to create, manage, configure, build and debug a project. Much of this may be familiar after running through the tutorials and Quick Labs. However, it is important to have a good grasp of what each of the configuration tabs are used for as that is where the bulk of the project preparation work takes place prior to writing code. Skim over this section as it may help with any questions in the future.

9. Read the [Writing the Application](#) section to get a short introduction to the steps used when creating application code with FSP. It covers both RTOS-independent and RTOS-dependent applications. It also includes a short description for several of the code accelerators you should be familiar with by now. Using additional Quick FSP Labs is a good way to become familiar with the application development process and links to them are included in the appropriate places in this section. You can find the complete list of available Quick FSP Labs here: <https://en-support.renesas.com/knowledgeBase/19308277>.
10. Scan the [Debugging the Project](#) section to see the steps required to download and start a debug session.
11. Explore the additional material available on the following web pages and bookmark the resources that look most valuable to you:
  - a. RA Landing Page: <https://www.renesas.com/ra>
  - b. FSP Landing Page: <https://www.renesas.com/fsp>
  - c. Example Projects on GitHub: <https://github.com/renesas/ra-fsp-examples>
  - d. Quick FSP Labs Listing: <https://en-support.renesas.com/knowledgeBase/19308277>
  - e. RA and FSP Knowledge Base (with articles of interest on RA and FSP): <https://en-support.renesas.com/knowledgeBase/category/31087>
  - f. RA and FSP Renesas Rulz site (Community posted and answered questions): <https://renesasrulz.com/ra/>
  - g. FSP Releases: <https://github.com/renesas/fsp/releases>
  - h. FSP Documentation: <https://renesas.github.io/fsp>
  - i. Online Technical Support: <https://www.renesas.com/us/en/support/contact.html>

## 2.2 e2 studio User Guide

### 2.2.1 What is e2 studio?

Renesas e2 studio is a development tool encompassing code development, build, and debug. e2 studio is based on the open-source Eclipse IDE and the associated C/C++ Development Tooling (CDT).

When developing for RA MCUs, e2 studio hosts the Renesas Flexible Software Package (FSP). FSP provides a wide range of time saving tools to simplify the selection, configuration, and management of modules and threads, to easily implement complex applications. The time saving tools available in e2 studio and FSP include the following:

- A Graphical User Interface (GUI) (see [Adding Threads and Drivers](#)) with numerous wizards for configuring and auto-generating code
- A context sensitive Autocomplete (see [Tutorial: Using HAL Drivers - Programming the WDT](#)) feature that provides intelligent options for completing a programming element
- A [Developer Assistance](#) tool for selection of and drag and drop placement of API functions directly in application code
- A [Welcome Window](#) with links to example projects, application notes and a variety of other self-help support resources
- An [Information Icon](#) from each module is provided in the graphic configuration viewer that links to specific design resources, including code 'cheat sheets' that provide useful starting points for common application implementations.



Figure 1: e2 studio Splash Screen

e2 studio organizes project work based on Perspectives, Views, Windows, Panes, and Pages (sometimes called Tabs). A window is a section of the e2 studio GUI that presents information on a key topic. Windows often use tabs to select sub-topics. For example, an editor window might have a tab available for each open file, so it is easy to switch back and forth between them. A window Pane is a section of a window. Within a window, multiple Panes can be opened and viewed simultaneously, as opposed to a tabbed window, where only individual content is displayed. A memory-display Window, for example, might have multiple Panes that allow the data to be displayed in different formats, simultaneously. A Perspective is a collection of Views and Windows typical for a specific stage of development. The default perspectives are a C/C++ Perspective, an FSP Configuration Perspective and a Debug Perspective. These provide specific Views, Windows, Tabs, and Panes tailored for the common tasks needed during the specific development stage.

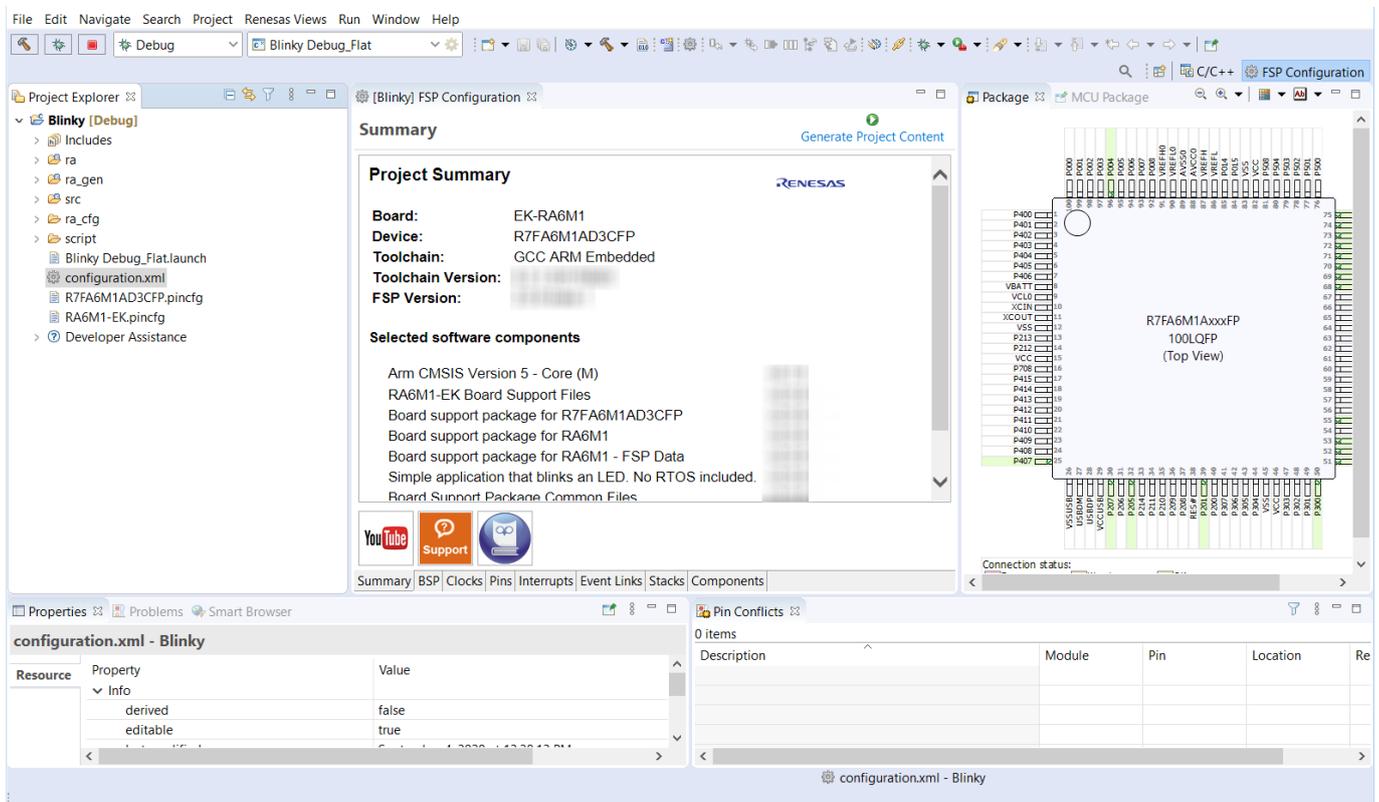


Figure 2: Default Perspective

In addition to managing project development, selecting modules, configuring them and simplifying code development, e2 studio also hosts the engine for automatically generating code based on module selections and configurations. The engine continually checks for dependencies and automatically adds any needed lower level modules to the module stack. It also identifies any lower level modules that require configuration (for example, an interrupt that needs to have a priority assigned). It also provides a guide for selecting between multiple choices or options to make it easy to complete a fully functional module stack.

The Generate Project Content function takes the selected and configured modules and automatically generates the complete and correct configuration code. The code is added to the folders visible in the **Project Explorer** window in e2 studio. The configuration.xml file in the project folder holds all the generated configuration settings. This file can be opened in the GUI-based RA Configuration editor to make further edits and changes. Once a project has been generated, you can go back and reconfigure any of the modules and settings if required using this editor.

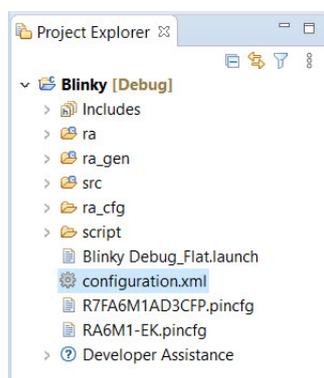


Figure 3: Project Explorer Window showing generated folders and configuration.xml file

## 2.2.2 e2 studio Prerequisites

### 2.2.2.1 Obtaining an RA MCU Kit

To develop applications with FSP, start with one of the Renesas RA MCU Evaluation Kits. The Renesas RA MCU Evaluation Kits are designed to seamlessly integrate with the e2 studio.

Ordering information, Quick Start Guides, User Manuals, and other related documents for all RA MCU Evaluation Kits are available at <https://www.renesas.com/ra>.

### 2.2.2.2 PC Requirements

The following are the minimum PC requirements to use e2 studio:

- Windows 10 with Intel i5 or i7, or AMD A10-7850K or FX
- Memory: 8-GB DDR3 or DDR4 DRAM (16-GB DDR4/2400-MHz RAM is preferred)
- Minimum 250-GB hard disk

### 2.2.2.3 Installing e2 studio, platform installer and the FSP package

Detailed installation instructions for the e2 studio and the FSP are available on the Renesas website <https://www.renesas.com/fsp>. Review the release notes for e2 studio to ensure that the e2 studio version supports the selected FSP version. The starting version of the installer includes all features of the RA MCUs.

### 2.2.2.4 Choosing a Toolchain

e2 studio can work with several toolchains and toolchain versions such as the GNU Arm compiler and Arm AC6. A version of the GNU Arm compiler is included in the e2 studio installer and has been verified to run with the FSP version.

### 2.2.2.5 Licensing

FSP licensing includes full source code, limited to Renesas hardware only.

## 2.2.3 What is a Project?

In e2 studio, all FSP applications are organized in RA MCU projects. Setting up an RA MCU project involves:

1. Creating a Project
2. Configuring a Project

These steps are described in detail in the next two sections. When you have existing projects already, after you launch e2 studio and select a workspace, all projects previously saved in the selected workspace are loaded and displayed in the **Project Explorer** window. Each project has an associated configuration file named `configuration.xml`, which is located in the project's root directory.

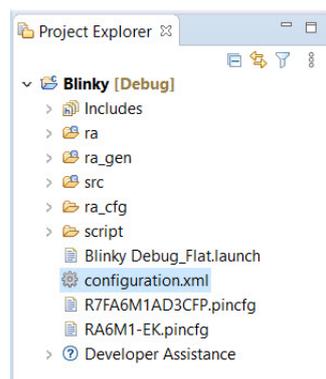


Figure 4: e2 studio Project Configuration file

Double-click on the `configuration.xml` file to open the RA MCU Project Editor. To edit the project configuration, make sure that the **FSP Configuration** perspective is selected in the upper right hand corner of the e2 studio window. Once selected, you can use the editor to view or modify the configuration settings associated with this project.



Figure 5: e2 studio FSP Configuration Perspective

#### Note

*Whenever the RA project configuration (that is, the `configuration.xml` file) is saved, a verbose RA Project Report file (`ra_cfg.txt`) with all the project settings is generated. The format allows differences to be easily viewed using a text comparison tool. The generated file is located in the project root directory.*

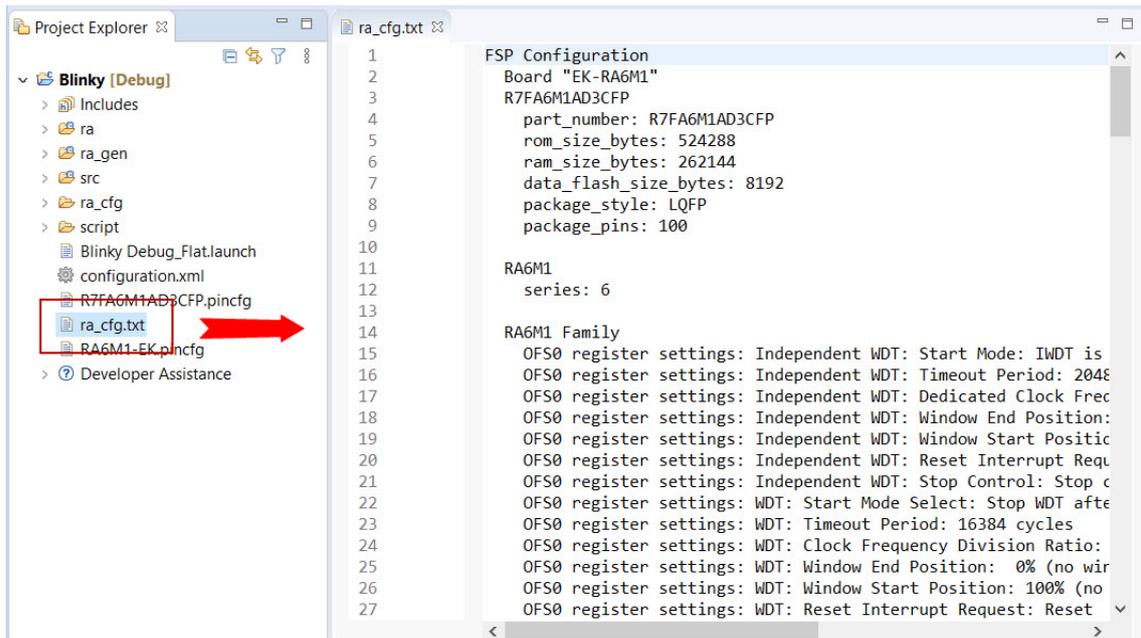


Figure 6: RA Project Report

The RA Project Editor has a number of tabs. The configuration steps and options for individual tabs are discussed in the following sections.

*Note*

*The tabs available in the RA Project Editor depend on the e2 studio version and the layout may vary slightly, however the functionality should be easy to follow..*

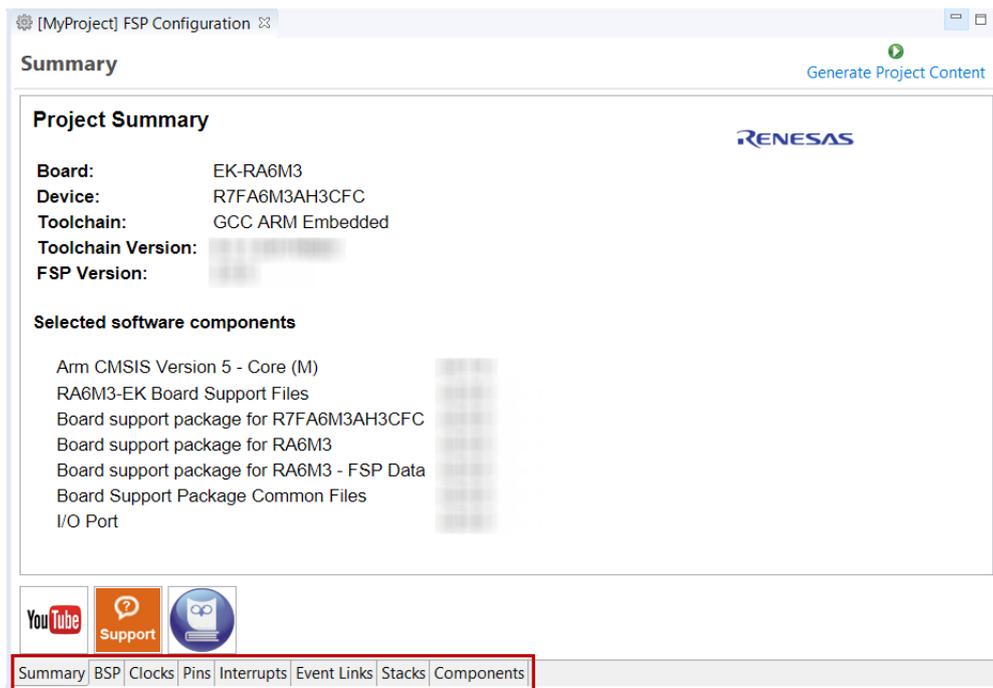


Figure 7: RA Project Editor tabs

- Click on the YouTube icon to visit the Renesas FSP playlist on YouTube
- Click on the Support icon to visit RA support pages at Renesas.com
- Click on the user manual (owl) icon to open the RA software package User's Manual

## 2.2.4 Creating a Project

During project creation, you specify the type of project, give it a project name and location, and configure the project settings for version, target board, whether an RTOS is included, the toolchain version, and the beginning template. This section includes easy-to-follow step-by-step instructions for all of the project creation tasks. Once you have created the project, you can move to configuring the project hardware (clocks, pins, interrupts) and the parameters of all the modules that are part of your application.

### 2.2.4.1 Creating a New Project

For RA MCU applications, generate a new project using the following steps:

1. Click on **File > New > RA C/C++ Project**.

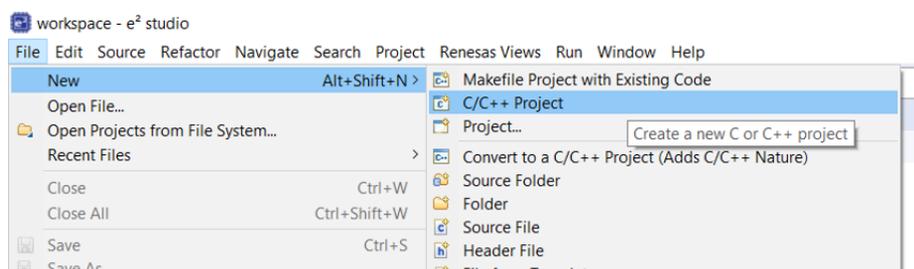


Figure 8: New RA MCU Project

Then click on the type of template for the type of project you are creating.

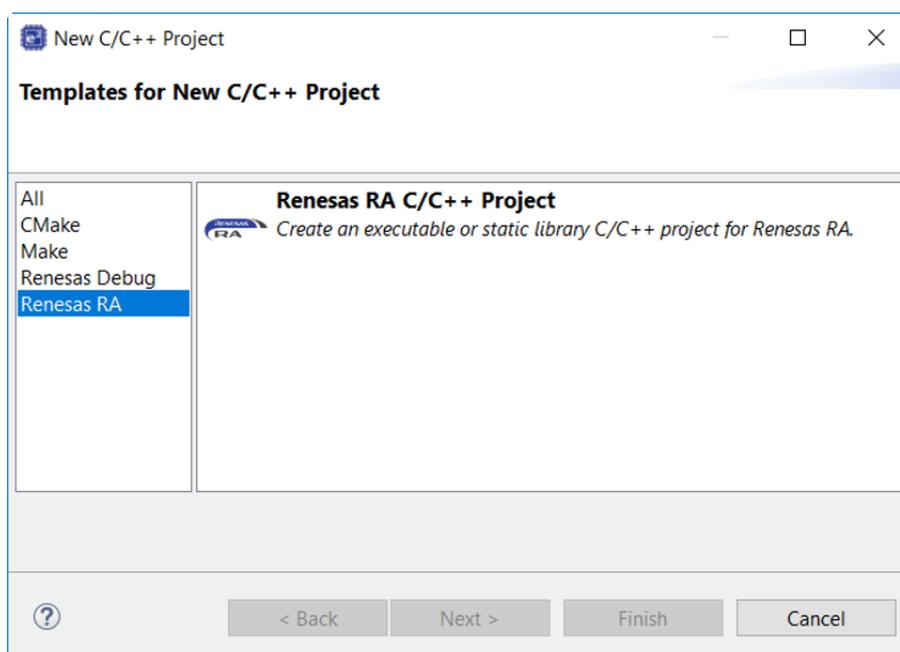


Figure 9: New Project Templates

## 2. Select a project name and location.

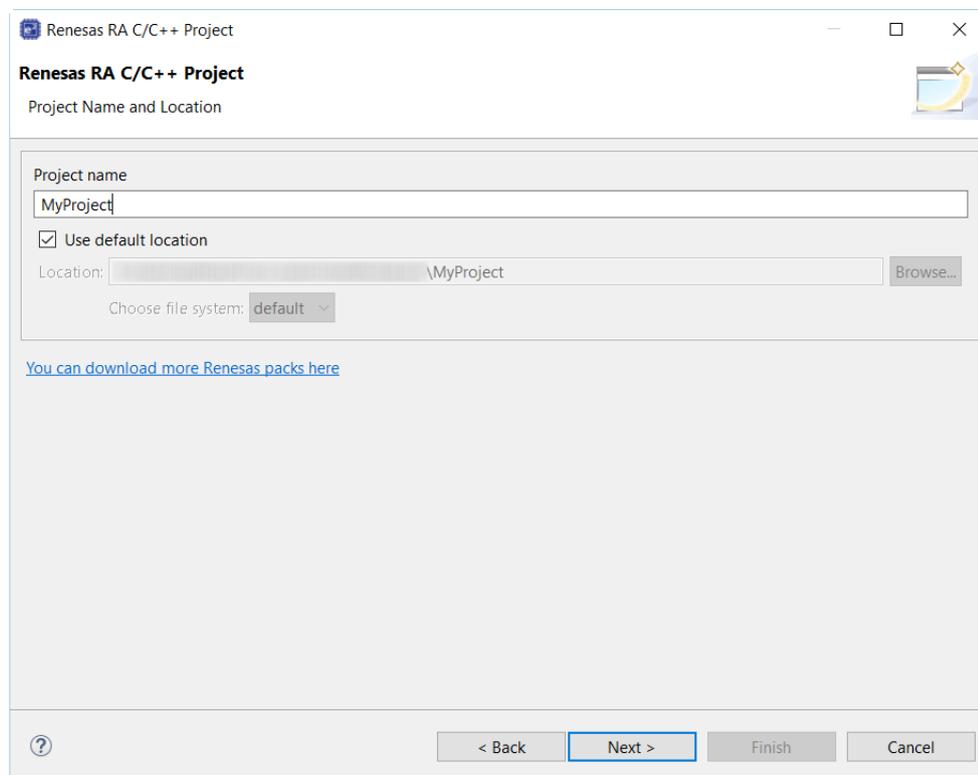


Figure 10: RA MCU Project Generator (Screen 1)

## 3. Click **Next**.

### 2.2.4.2 Selecting a Board and Toolchain

In the **Project Configuration** window select the hardware and software environment:

1. Select the **FSP version**.
2. Select the **Board** for your application. You can select an existing RA MCU Evaluation Kit or select **Custom User Board** for any of the RA MCU devices with your own BSP definition.
3. Select the **Device**. The **Device** is automatically populated based on the **Board** selection. Only change the **Device** when using the **Custom User Board (Any Device)** board selection.
4. To add threads, select **RTOS**, or **No RTOS** if an RTOS is not being used.
5. The **Toolchain** selection defaults to **GCC Arm Embedded**.
6. Select the **Toolchain version**. This should default to the installed toolchain version.
7. Select the **Debugger**. The J-Link Arm Debugger is preselected.

## 8. Click **Next**.

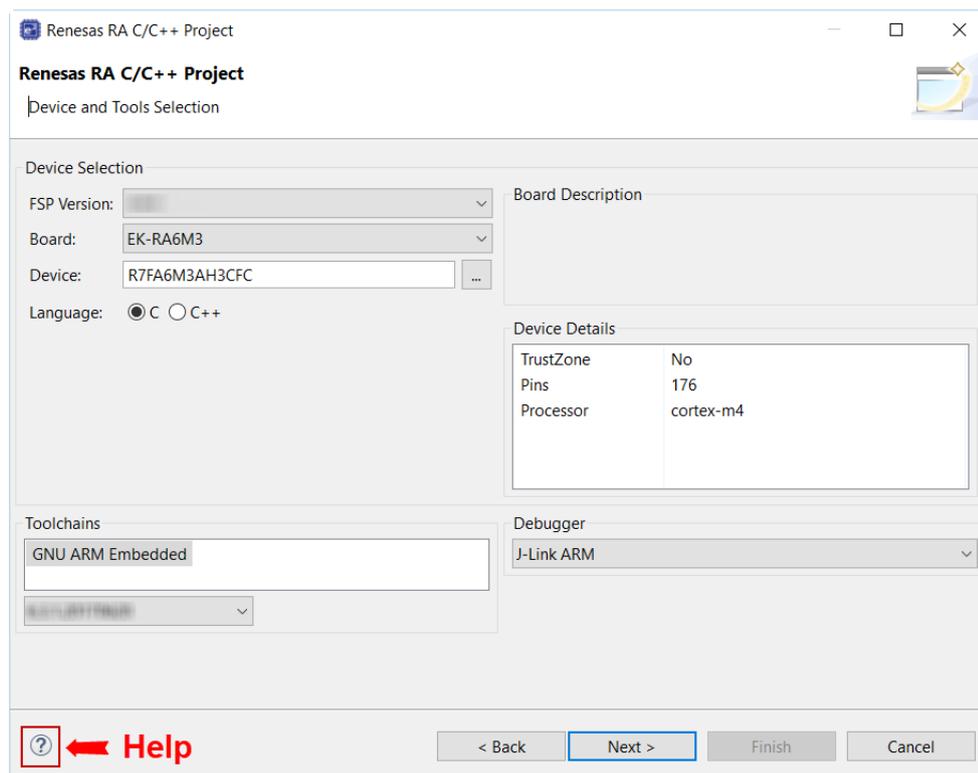


Figure 11: RA MCU Project Generator (Screen 2)

*Note*

Click on the **Help** icon (?) for user guides, RA contents, and other documents.

### 2.2.4.3 Selecting Flat or Arm® TrustZone® Project

If you selected a device or tool based on an Arm® Cortex®-M33, you next select whether to use Arm® TrustZone® in your project. For normal, non-TrustZone projects, select "Flat".

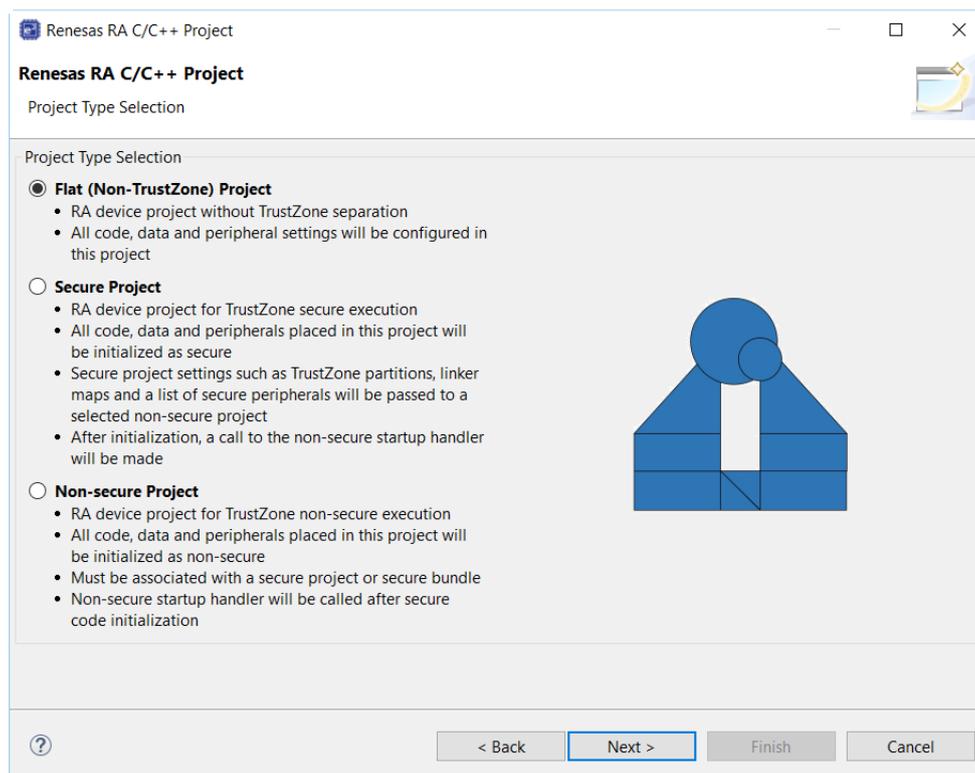


Figure 12: Flat, Secure, or Non-Secure Project

For more information on Arm® TrustZone®, see [Primer: ARM® TrustZone® Project Development](#).

#### 2.2.4.4 Selecting a Project Template

In the next window, select the build artifact and RTOS.

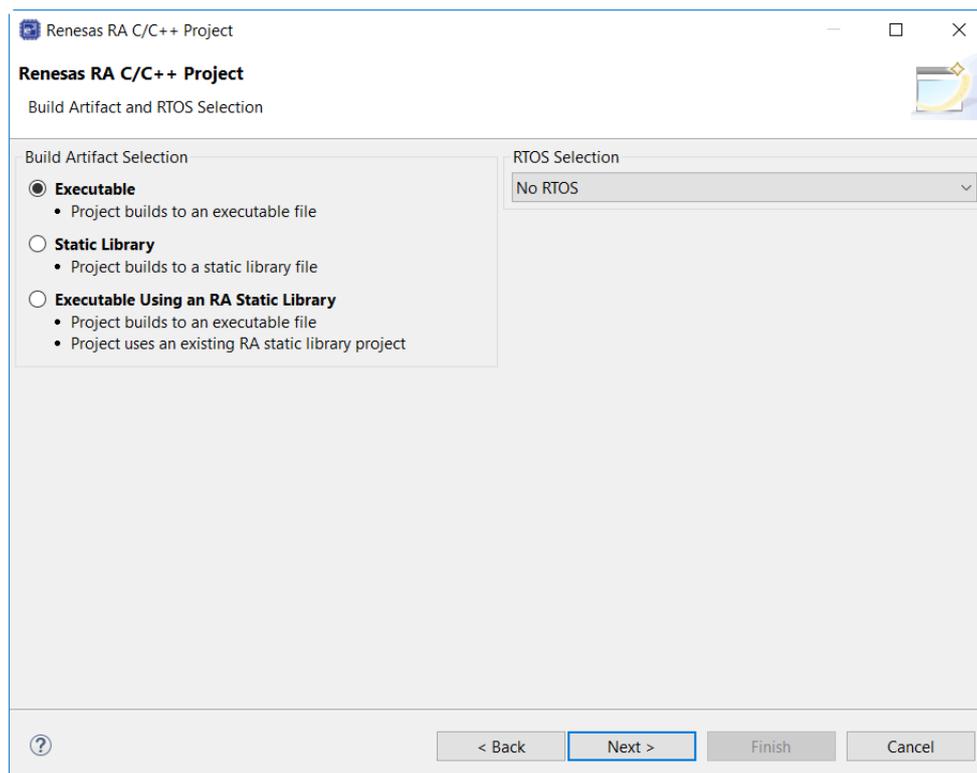


Figure 13: RA MCU Project Generator (Screen 3)

In the next window, select a project template from the list of available templates. By default, this screen shows the templates that are included in your current RA MCU pack. Once you have selected the appropriate template, click **Finish**.

*Note*

*If you want to develop your own application, select the basic template for your board, **Bare Metal - Minimal**.*

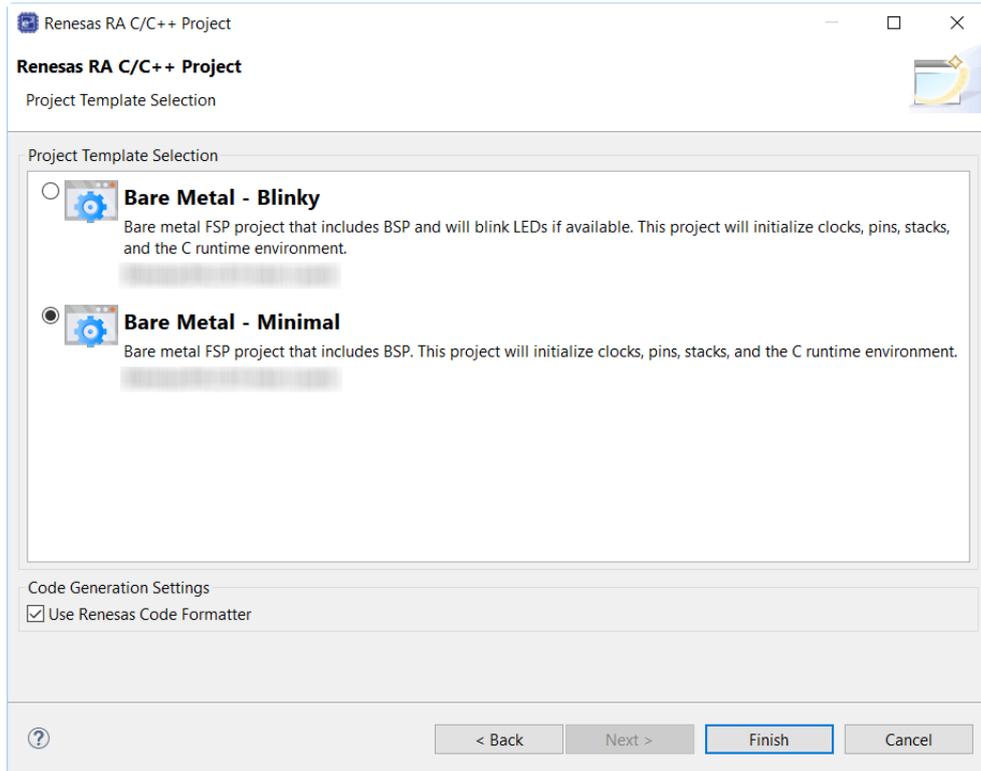


Figure 14: RA MCU Project Generator (Screen 4)

When the project is created, e2 studio displays a summary of the current project configuration in the RA MCU Project Editor.

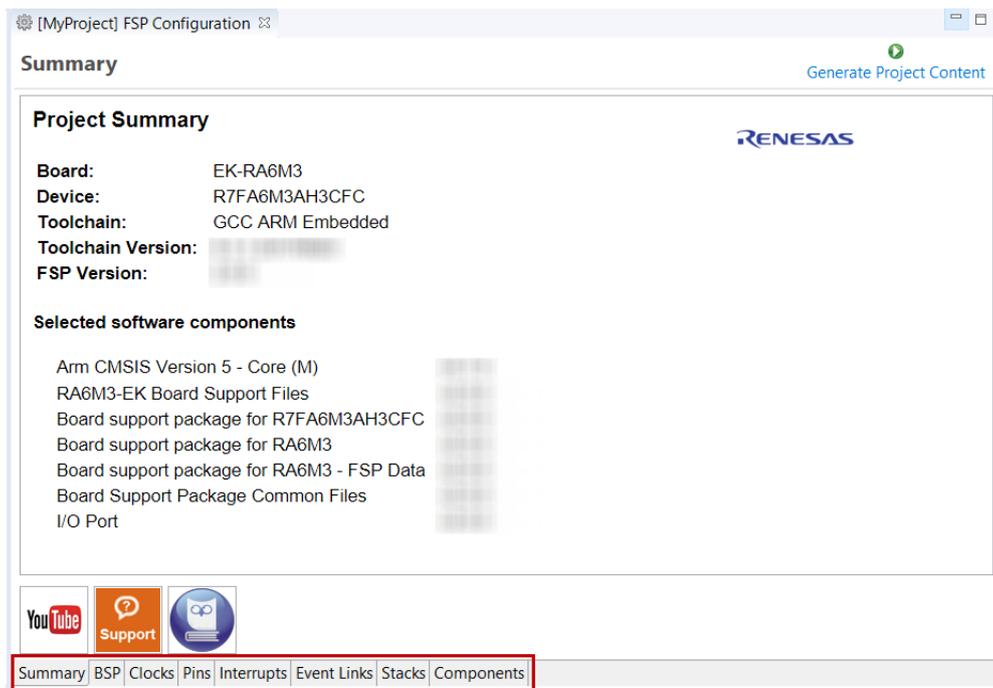


Figure 15: RA MCU Project Editor and available editor tabs

On the bottom of the RA MCU Project Editor view, you can find the tabs for configuring multiple aspects of your project:

- With the **Summary** tab, you can see all the key characteristics of the project: board, device, toolchain, and more.
- With the **BSP** tab, you can change board specific parameters from the initial project selection.
- With the **Clocks** tab, you can configure the MCU clock settings for your project.
- With the **Pins** tab, you can configure the electrical characteristics and functions of each port pin.
- With the **Interrupts** tab, you can add new user events/interrupts.
- With the **Event Links** tab, you can configure events used by the Event Link Controller.
- With the **Stacks** tab, you can add and configure FSP modules. For each module selected in this tab, the **Properties** window provides access to the configuration parameters, interrupt priorities, and pin selections.
- The **Components** tab provides an overview of the selected modules. Although you can also add drivers for specific FSP releases and application sample code here, this tab is normally only used for reference.

The functions and use of each of these tabs is explained in detail in the next section.

## 2.2.5 Configuring a Project

Each of the configurable elements in an FSP project can be edited using the appropriate tab in the RA Configuration editor window. Importantly, the initial configuration of the MCU after reset and before any user code is executed is set by the configuration settings in the **BSP**, **Clocks** and **Pins** tabs. When you select a project template during project creation, e2 studio configures default values that are appropriate for the associated board. You can change those default values as needed. The following sections detail the process of configuring each of the project elements for each of the associated tabs.

### 2.2.5.1 Summary Tab

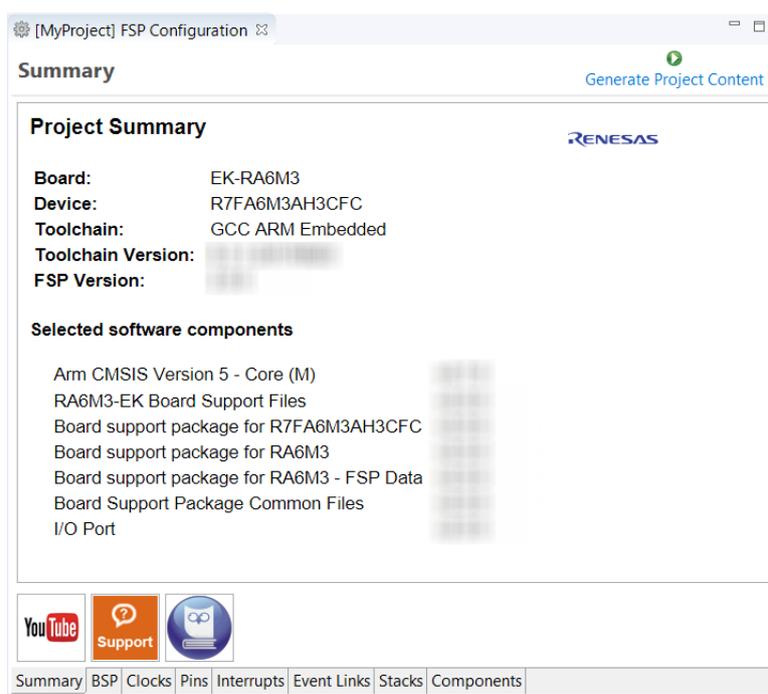


Figure 16: Configuration Summary tab

The **Summary** tab, seen in the above figure, identifies all the key elements and components of a project. It shows the target board, the device, toolchain and FSP version. Additionally, it provides a list of all the selected software components and modules used by the project. This is a more convenient summary view when compared to the **Components** tab.

The summary tab also includes handy icons with links to the Renesas YouTube channel, the Renesas support page and to the RA FSP User Manual that was downloaded during the installation process.

### 2.2.5.2 Configuring the BSP

The **BSP** tab shows the currently selected board (if any) and device. The Properties view is located in the lower left of the Project Configurations view as shown below.

*Note*

*If the Properties view is not visible, click **Window > Show View > Properties** in the top menu bar.*

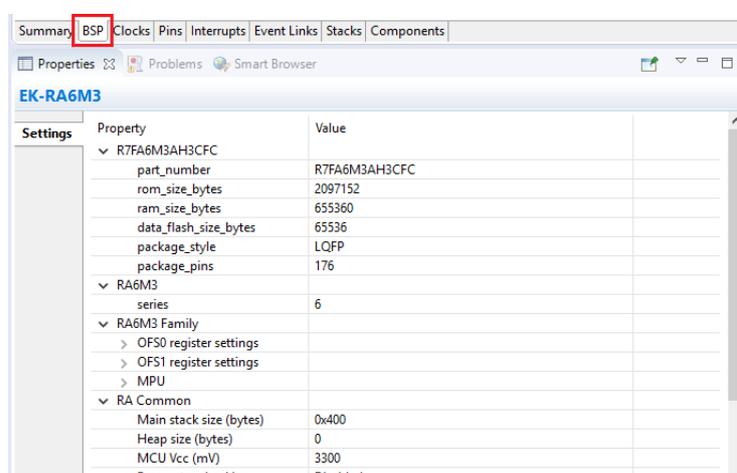


Figure 17: Configuration BSP tab

The **Properties** view shows the configurable options available for the BSP. These can be changed as required. The BSP is the FSP layer above the MCU hardware. e2 studio checks the entry fields to flag invalid entries. For example, only valid numeric values can be entered for the stack size.

When you click the **Generate Project Content** button, the BSP configuration contents are written to `ra_cfg/fsp_cfg/bsp/bsp_cfg.h`

This file is created if it does not already exist.

**Warning**

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

### 2.2.5.3 Configuring Clocks

The **Clocks** tab presents a graphical view of the MCU's clock tree, allowing the various clock dividers and sources to be modified. If a clock setting is invalid, the offending clock value is highlighted in red. It is still possible to generate code with this setting, but correct operation cannot be guaranteed. In the figure below, the USB clock UCLK has been changed so the resulting clock frequency is 60 MHz

instead of the required 48 MHz. This parameter is colored red.

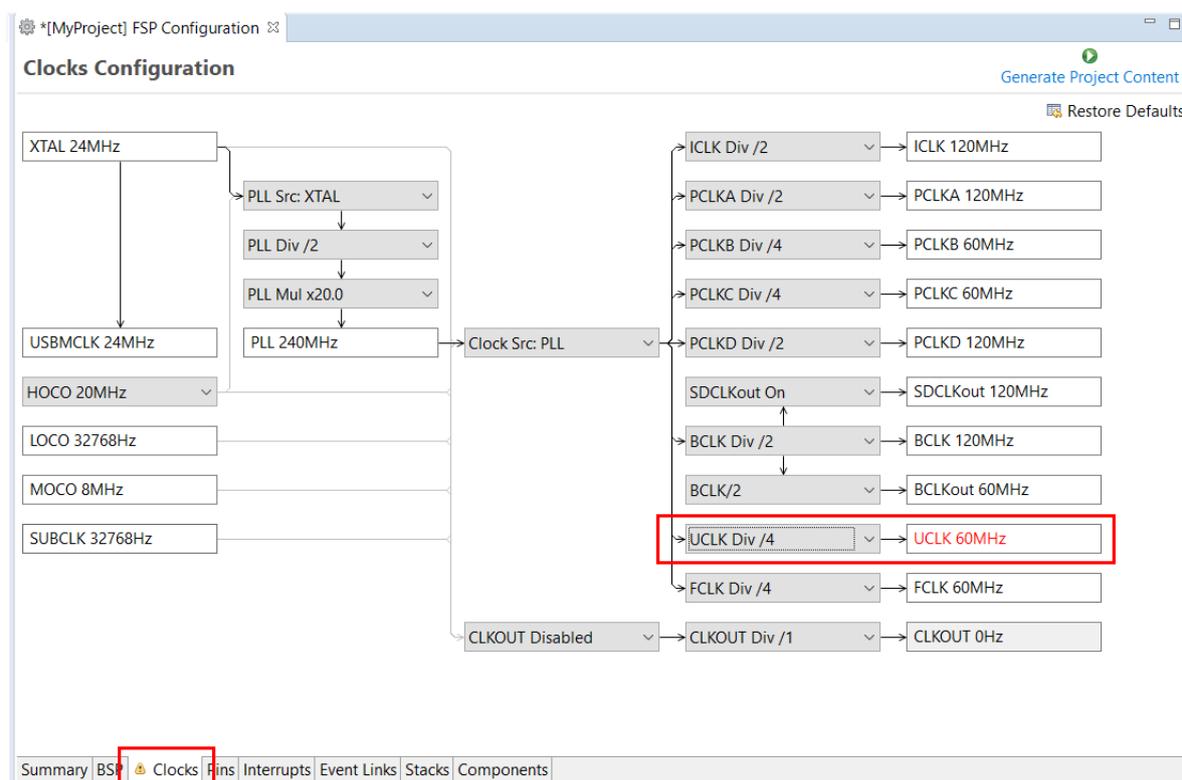


Figure 18: Configuration Clocks tab

When you click the **Generate Project Content** button, the clock configuration contents are written to: `ra_gen/bsp_clock_cfg.h`

This file will be created if it does not already exist.

#### Warning

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

### 2.2.5.4 Configuring Pins

The **Pins** tab provides flexible configuration of the MCU's pins. As many pins are able to provide multiple functions, they can be configured on a peripheral basis. For example, selecting a serial channel via the SCI peripheral offers multiple options for the location of the receive and transmit pins for that module and channel. Once a pin is configured, it is shown as green in the **Package** view.

#### Note

If the **Package** view window is not open in e2 studio, select **Window > Show View > Pin Configurator > Package** from the top menu bar to open it.

The **Pins** tab simplifies the configuration of large packages with highly multiplexed pins by highlighting errors and presenting the options for each pin or for each peripheral. If you selected a project template for a specific board such as the EK-RA6M3, some peripherals connected on the board are preselected.

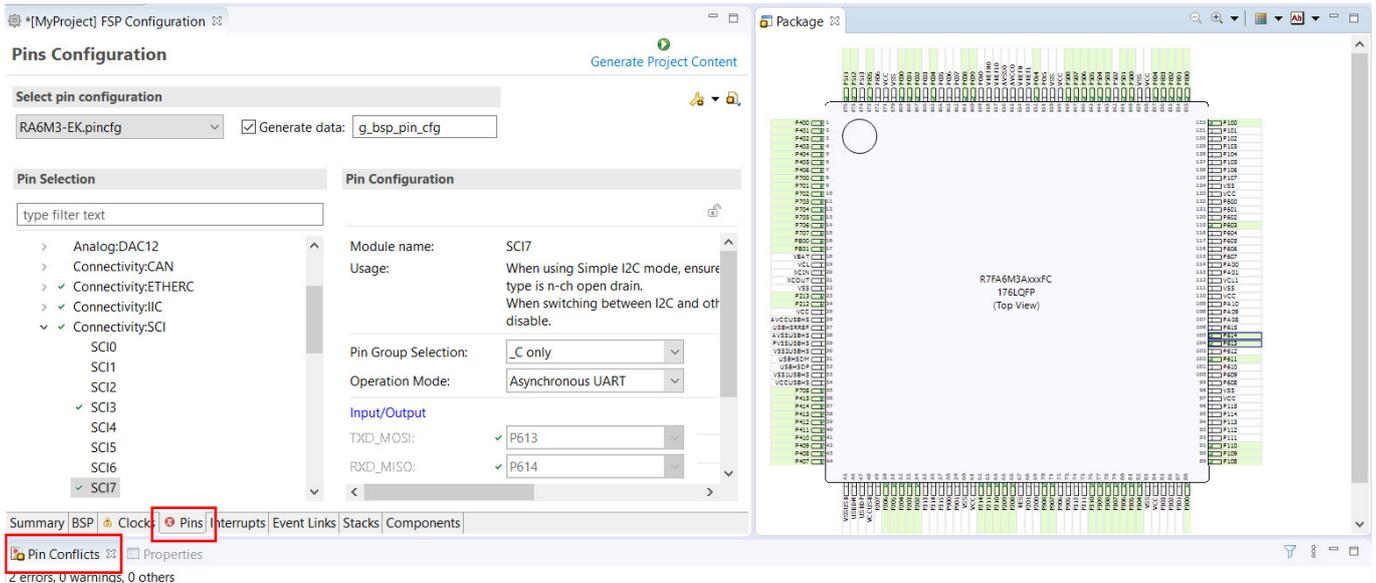


Figure 19: Pins Configuration

The pin configurator includes a built-in conflict checker, so if the same pin is allocated to another peripheral or I/O function the pin will be shown as red in the package view and also with white cross in a red square in the **Pin Selection** pane and **Pin Configuration** pane in the main **Pins** tab. The **Pin Conflicts** view provides a list of conflicts, so conflicts can be quickly identified and fixed.

In the example shown below, port P611 is already used by the CAC, and the attempt to connect this port to the Serial Communications Interface (SCI) results in a dangling connection error. To fix this error, select another port from the pin drop-down list or disable the CAC in the **Pin Selection** pane on the left side of the tab.

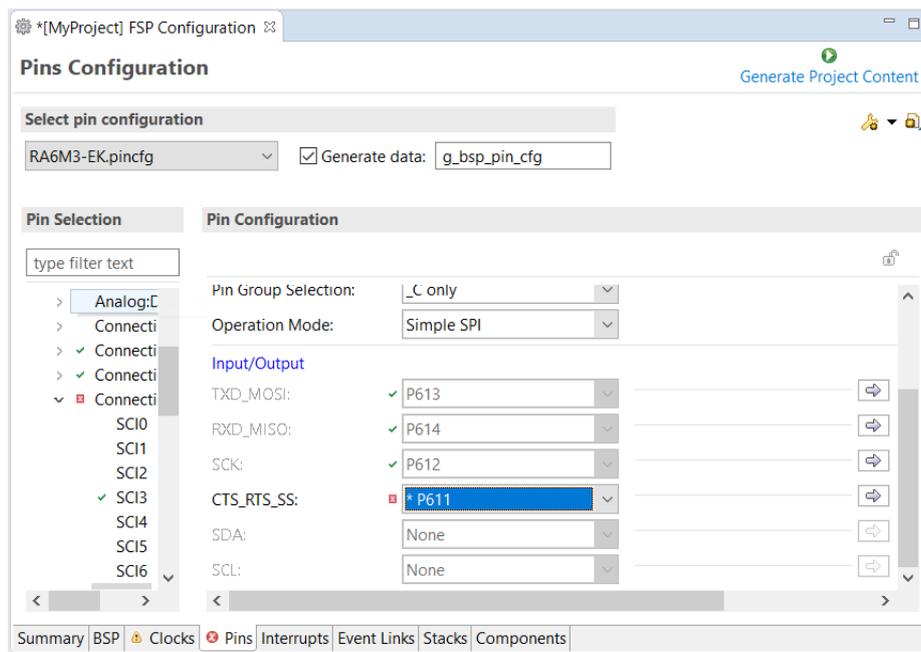


Figure 20: e2 studio Pin configurator

The pin configurator also shows a package view and the selected electrical or functional characteristics of each pin.

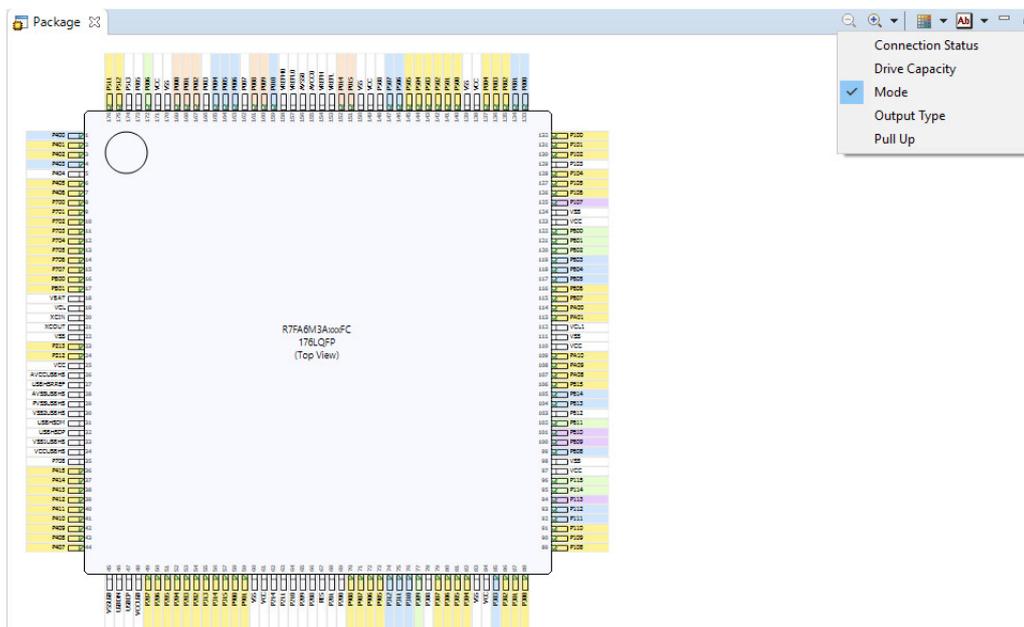


Figure 21: e2 studio Pin configurator package view

When you click the **Generate Project Content** button, the pin configuration contents are written to: `ra_gen\bsp_pin_cfg.h`

This file will be created if it does not already exist.

#### Warning

Do not edit this file as it is overwritten whenever the **Generate Project Content** button is clicked.

To make it easy to share pinning information for your project, e2 studio exports your pin configuration settings to a csv format and copies the csv file to `ra_gen/<MCU package>.csv`.

### 2.2.5.5 Configuring Interrupts from the Stacks Tab

You can use the **Properties** view in the **Stacks** tab to enable interrupts by setting the interrupt priority. Select the driver in the **Stacks** pane to view and edit its properties.

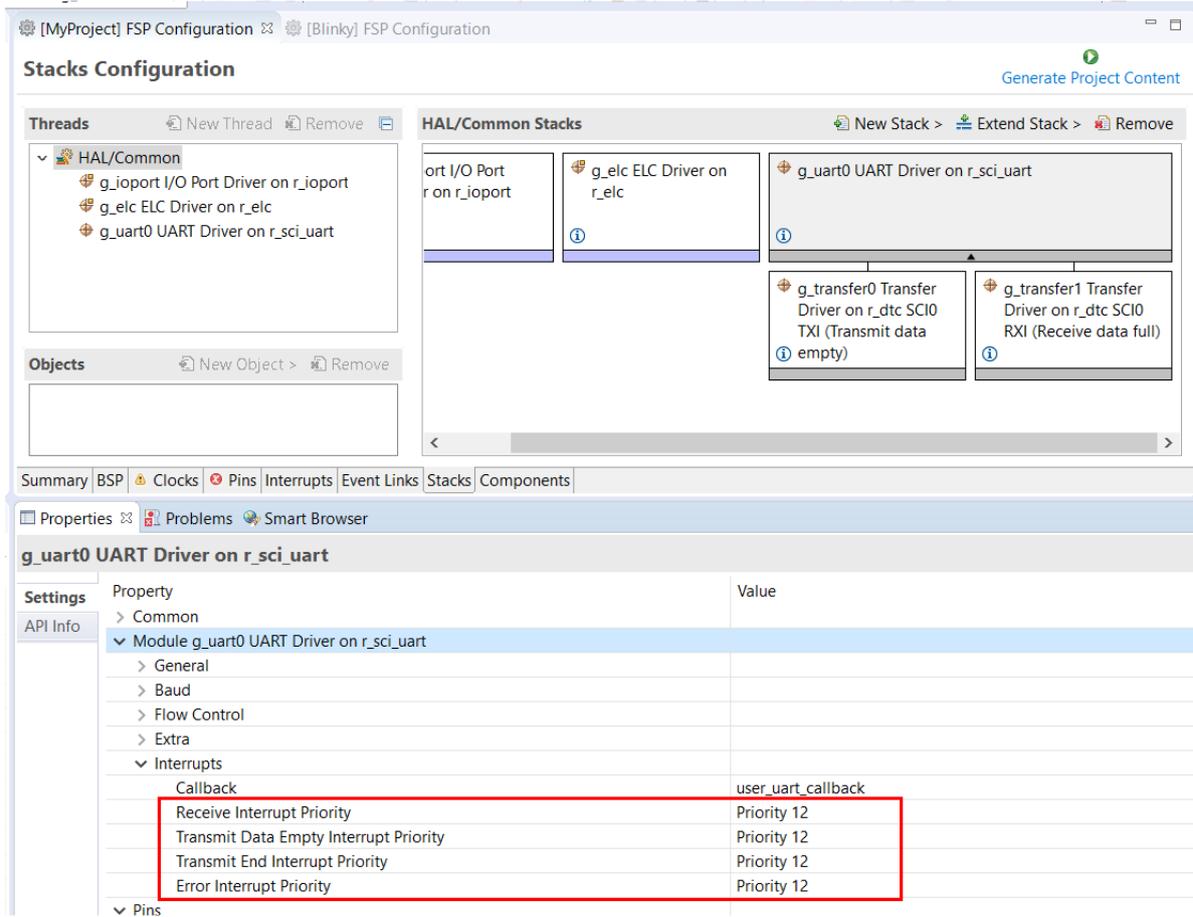


Figure 22: Configuring Interrupts in the Stacks tab

### Creating Interrupts from the Interrupts Tab

On the **Interrupts** tab, the user can bypass a peripheral interrupt set by the FSP by setting a user-defined ISR. This can be done by adding a new event via the **New User Event** button.

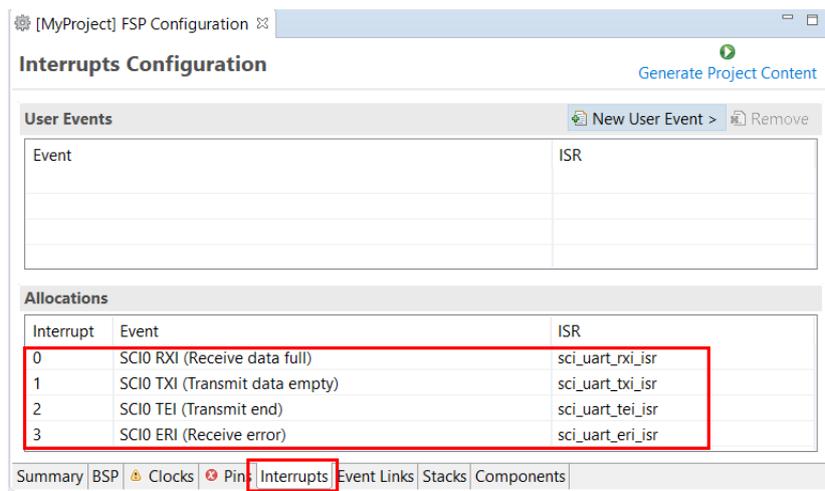


Figure 23: Configuring interrupt in Interrupt Tab

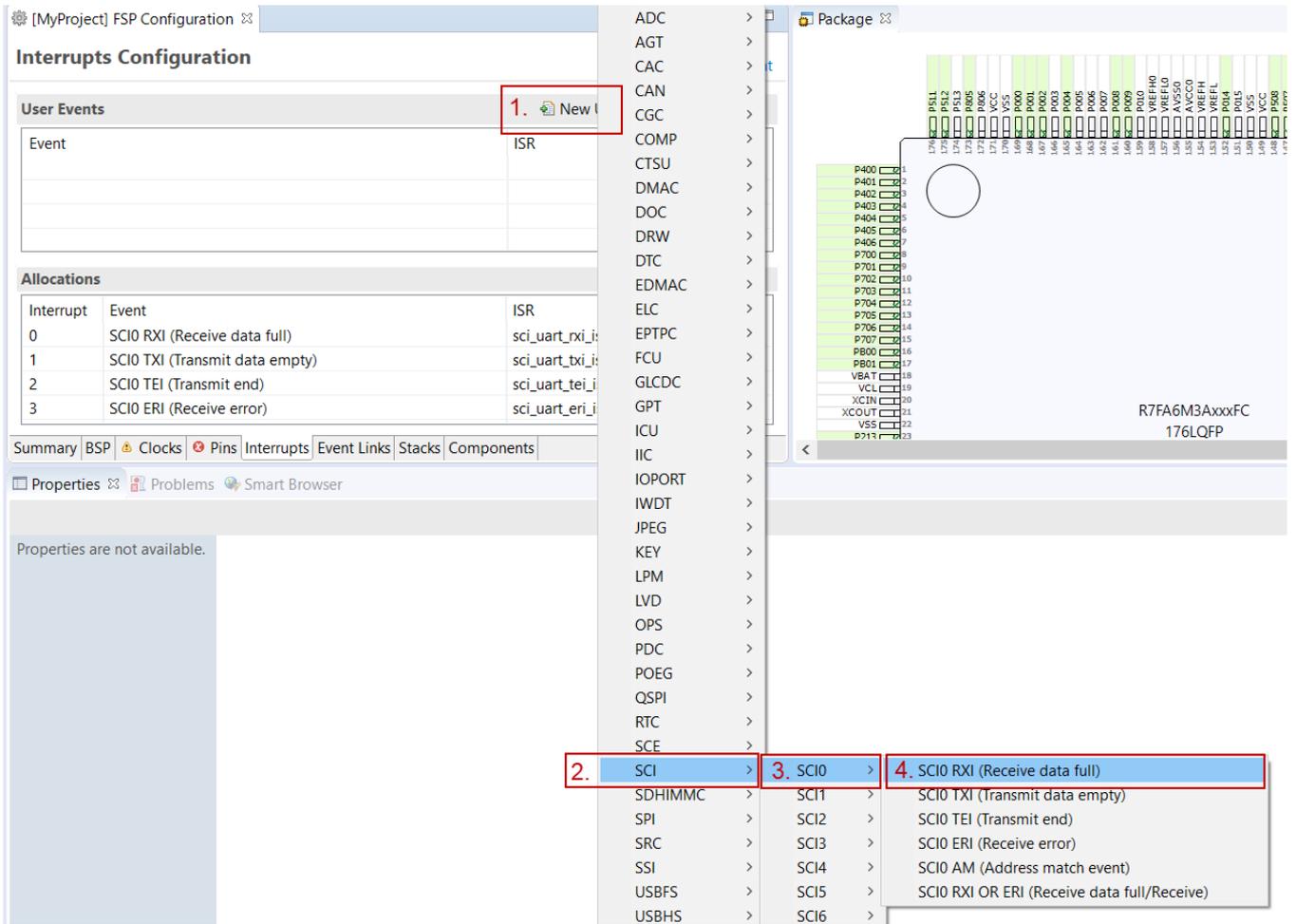


Figure 24: Adding user-defined event

Enter the name of ISR for the new user event.

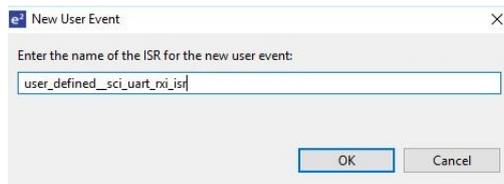


Figure 25: User-defined event ISR

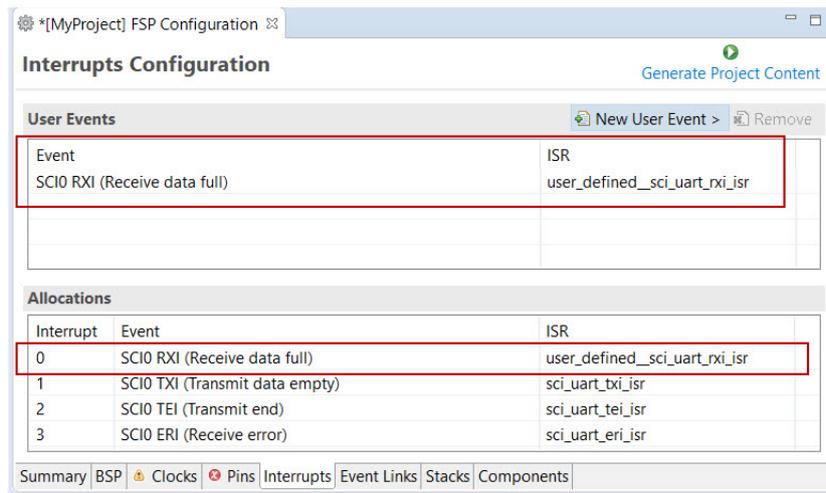


Figure 26: Using a user-defined event

### 2.2.5.6 Viewing Event Links

The Event Links tab can be used to view the Event Link Controller events. The events are sorted by peripheral to make it easy to find and verify them.

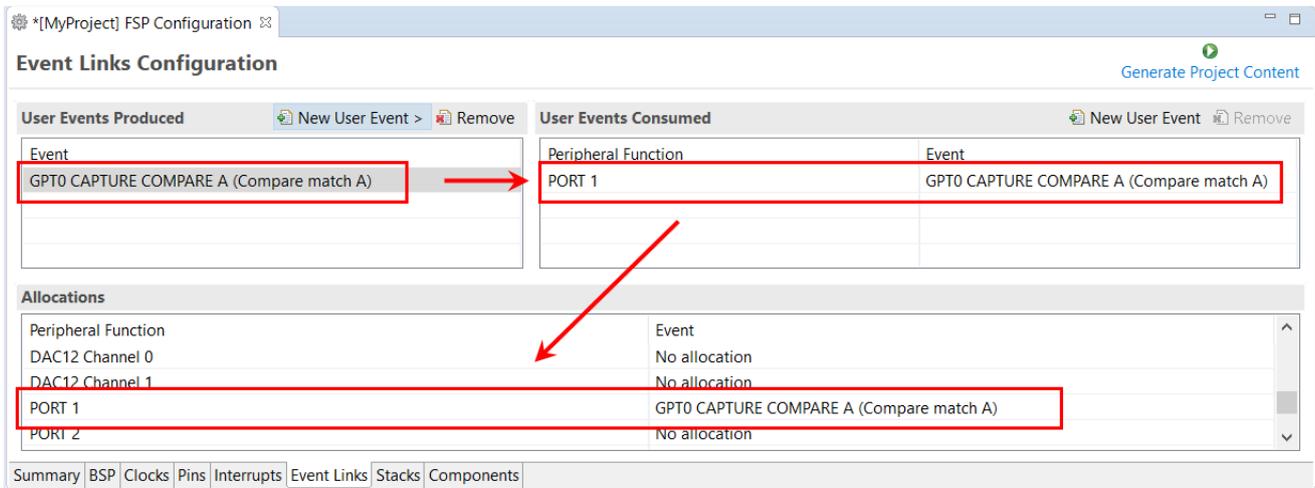


Figure 27: Viewing Event Links

Like the Interrupts tab, user-defined event sources and destinations (producers and consumers) can be defined by clicking the relevant **New User Event** button. Once a consumer is linked to a producer the link will appear in the **Allocations** section at the bottom.

*Note*

*When selecting an ELC event to receive for a module (or when manually defining an event link), only the events that are made available by the modules configured in the project will be shown.*

### 2.2.6 Adding Threads and Drivers

Every RTOS-based RA Project includes at least one RTOS Thread and a stack of FSP modules running

in that thread. The **Stacks** tab is a graphical user interface which helps you to add the right modules to a thread and configure the properties of both the threads and the modules associated with each thread. Once you have configured the thread, e2 studio automatically generates the code reflecting your configuration choices.

For any driver, or, more generally, any module that you add to a thread, e2 studio automatically resolves all dependencies with other modules and creates the appropriate stack. This stack is displayed in the Stacks pane, which e2 studio populates with the selected modules and module options for the selected thread.

The default view of the **Stacks** tab includes a Common Thread called **HAL/Common**. This thread includes the driver for I/O control (IOPORT). The default stack is shown in the **HAL/Common Stacks** pane. The default modules added to the HAL/Common driver are special in that the FSP only requires a single instance of each, which e2 studio then includes in every user-defined thread by default.

In applications that do not use an RTOS or run outside of the RTOS, the HAL/Common thread becomes the default location where you can add additional drivers to your application.

For a detailed description on how to add and configure modules and stacks, see the following sections:

- [Adding and Configuring HAL Drivers](#)
- [Adding Drivers to a Thread and Configuring the Drivers](#)

Once you have added a module either to HAL/Common or to a new thread, you can access the driver's configuration options in the **Properties** view. If you added thread objects, you can access the objects configuration options in the **Properties** view in the same way.

You can find details about how to configure threads here: [Configuring Threads](#)

*Note*

*Driver and module selections and configuration options are defined in the FSP pack and can therefore change when the FSP version changes.*

### 2.2.6.1 Adding and Configuring HAL Drivers

For applications that run outside or without the RTOS, you can add additional HAL drivers to your application using the HAL/Common thread. To add drivers, follow these steps:

1. Click on the HAL/Common icon in the **Stacks** pane. The Modules pane changes to **HAL/Common Stacks**.

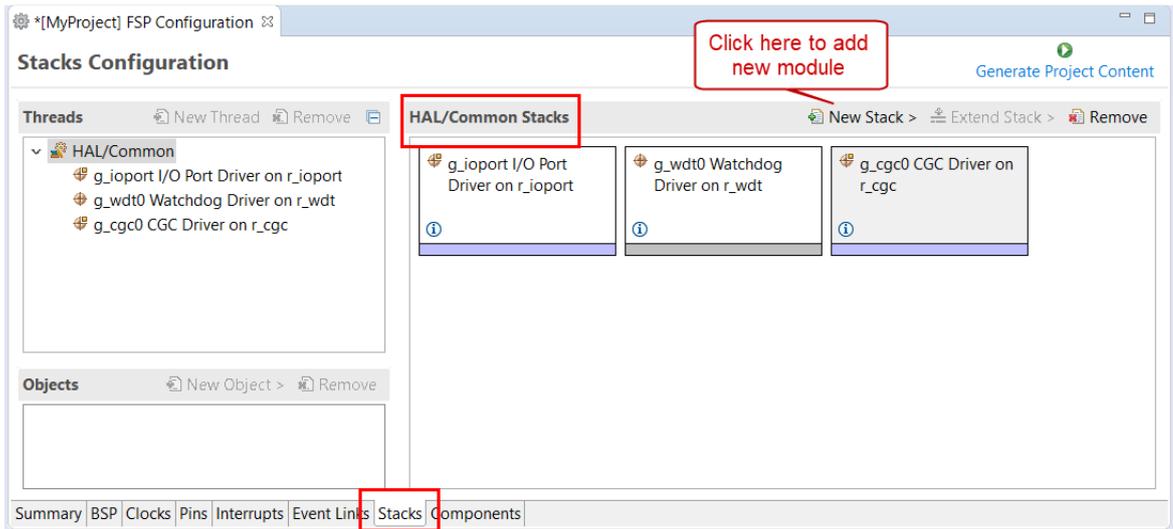


Figure 28: e2 studio Project configurator - Adding drivers

2. Click **New Stack** to see a drop-down list of HAL level drivers available in the FSP.
3. Select a driver from the menu **New Stack > Driver**.

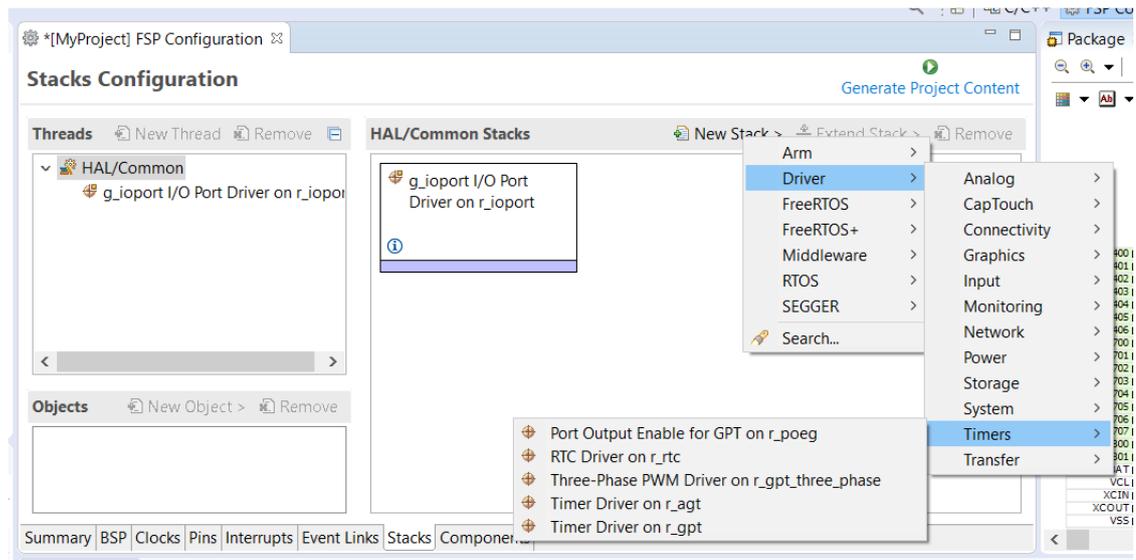


Figure 29: Select a driver

4. Select the driver module in the **HAL/Common Modules** pane and configure the driver properties in the **Properties** view.

e2 studio adds the following files when you click the **Generate Project Content** button:

- The selected driver module and its files to the ra/fsp directory
- The main() function and configuration structures and header files for your application as shown in the table below.

File	Contents	Overwritten by Generate Project Content?
------	----------	--

ra_gen/main.c	Contains main() calling generated and user code. When called, the BSP already has Initialized the MCU.	Yes
ra_gen/hal_data.c	Configuration structures for HAL Driver only modules.	Yes
ra_gen/hal_data.h	Header file for HAL driver only modules.	Yes
src/hal_entry.c	User entry point for HAL Driver only code. Add your code here.	No

The configuration header files for all included modules are created or overwritten in this folder:  
ra\_cfg/fsp\_cfg

### 2.2.6.2 Adding Drivers to a Thread and Configuring the Drivers

For an application that uses the RTOS, you can add one or more threads, and for each thread at least one module that runs in the thread. You can select modules from the Driver dropdown menu. To add modules to a thread, follow these steps:

1. In the **Threads** pane, click **New Thread** to add a Thread.

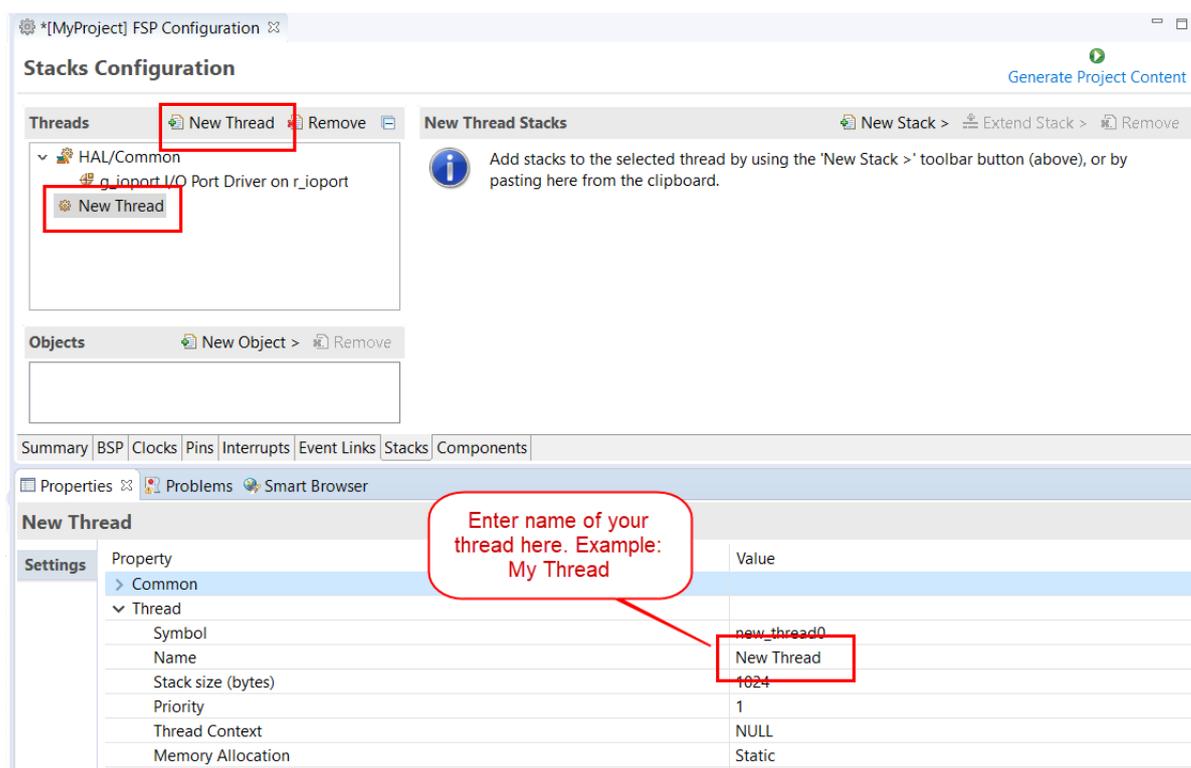


Figure 30: Adding a new RTOS Thread on the Stacks tab

2. In the **Properties** view, click on the **Name** and **Symbol** entries and enter a distinctive name and symbol for the new thread.

Note

e2 studio updates the name of the thread stacks pane to **My Thread Stacks**.

3. In the **My Thread Stacks** pane, click on **New Stack** to see a list of modules and drivers. HAL-level drivers can be added here.

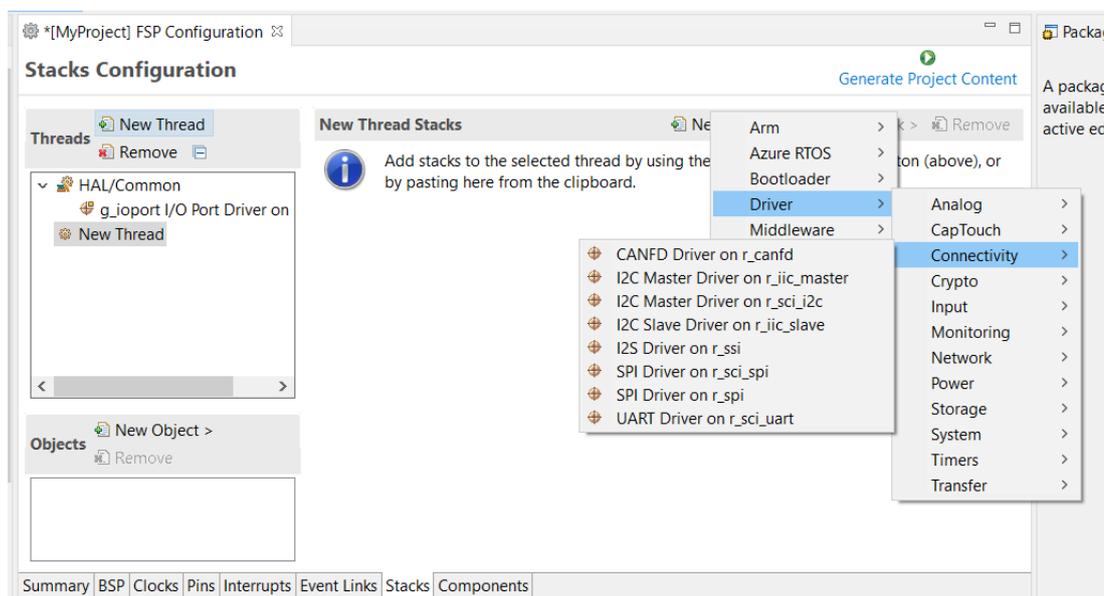


Figure 31: Adding Modules and Drivers to a thread

4. Select a module or driver from the list.
5. Click on the added driver and configure the driver as required by the application by updating the configuration parameters in the **Properties** view. To see the selected module or driver and be able to edit its properties, make sure the Thread containing the driver is highlighted in the **Threads** pane.

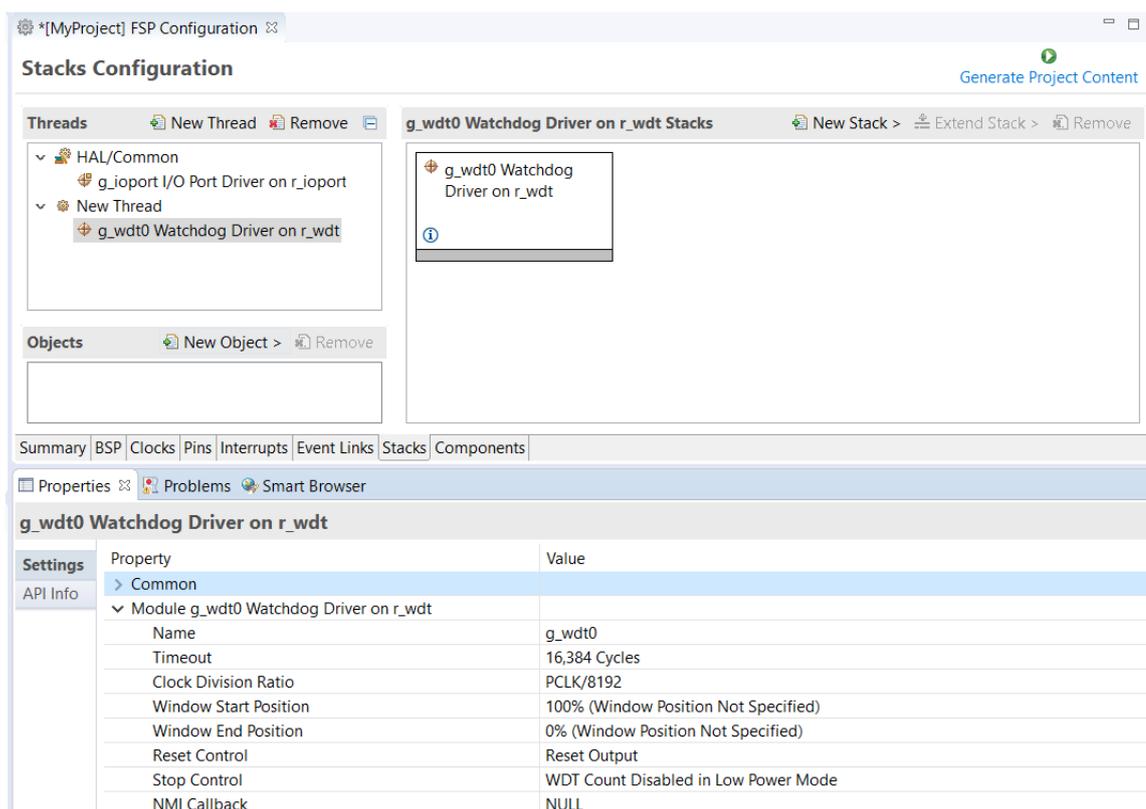


Figure 32: Configuring Module or Driver properties

6. If needed, add another thread by clicking **New Thread** in the **Threads** pane.

When you press the **Generate Project Content** button for the example above, e2 studio creates the files as shown in the following table:

File	Contents	Overwritten by Generate Project Content?
ra_gen/main.c	Contains main() calling generated and user code. When called the BSP will have initialized the MCU.	Yes
ra_gen/my_thread.c	Generated thread "my_thread" and configuration structures for modules added to this thread.	Yes
ra_gen/my_thread.h	Header file for thread "my_thread"	Yes
ra_gen/hal_data.c	Configuration structures for HAL Driver only modules.	Yes
ra_gen/hal_data.h	Header file for HAL Driver only modules.	Yes
src/hal_entry.c	User entry point for HAL Driver only code. Add your code here.	No

src/my_thread_entry.c	User entry point for thread "my_thread". Add your code here.	No
-----------------------	--	----

The configuration header files for all included modules and drivers are created or overwritten in the following folders: ra\_cfg/fsp\_cfg/<header files>

### 2.2.6.3 Configuring Threads

If the application uses an RTOS, the **Stacks** tab can be used to simplify the creation of RTOS threads, semaphores, mutexes, and event flags.

The components of each thread can be configured from the **Properties** view as shown below.

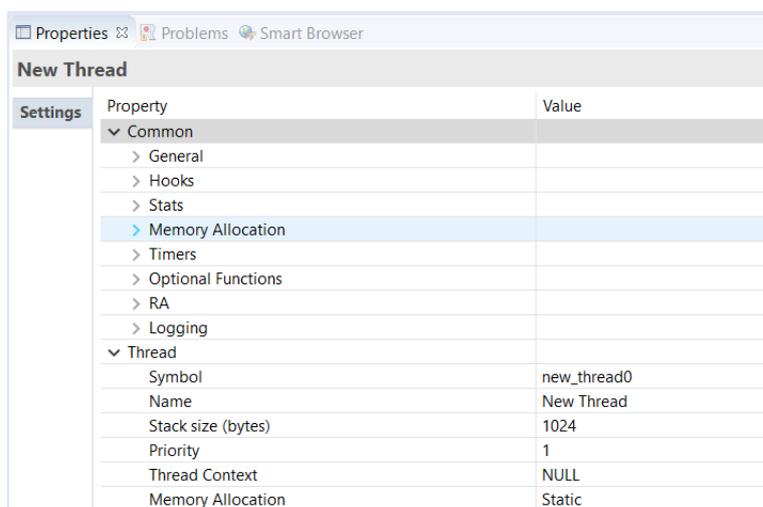


Figure 33: New Thread Properties

The **Properties** view contains settings common for all Threads (**Common**) and settings for this particular thread (**Thread**).

For this thread instance, the thread's name and properties (such as priority level or stack size) can be easily configured. e2 studio checks that the entries in the property field are valid. For example, it will verify that the field **Priority**, which requires an integer value, only contains numeric values between 0 and 9.

To add RTOS resources to a Thread, select a thread and click on **New Object** in the Thread Objects pane. The pane takes on the name of the selected thread, in this case **My Thread Objects**.

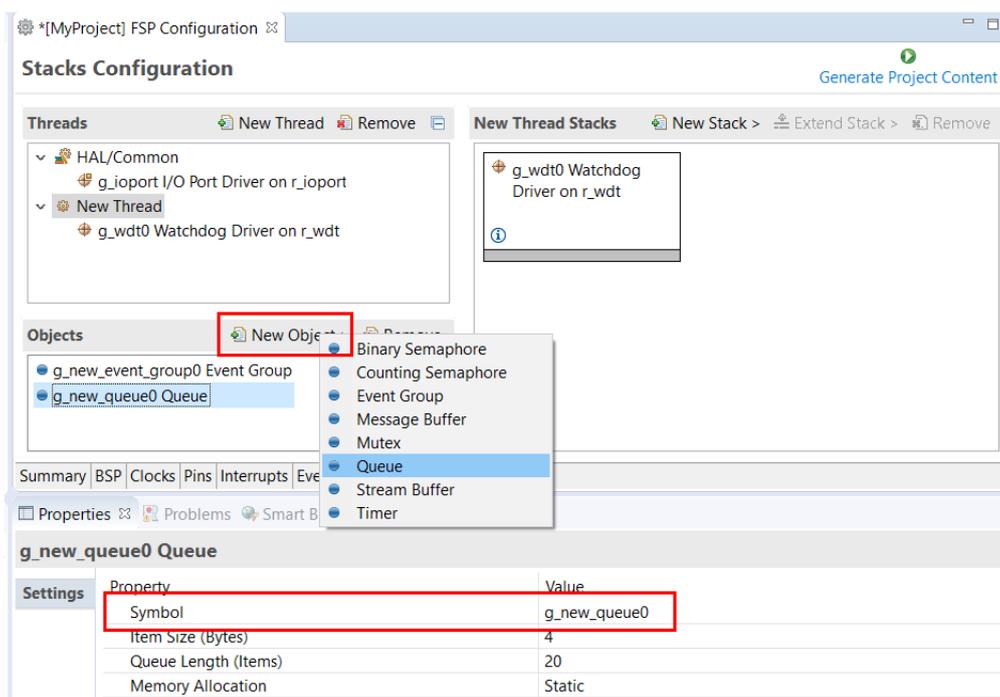


Figure 34: Configuring Thread Object Properties

Make sure to give each thread object a unique name and symbol by updating the **Name** and **Symbol** entries in the **Properties** view.

## 2.2.7 Reviewing and Adding Components

The **Components** tab enables the individual modules required by the application to be included or excluded. Modules common to all RA MCU projects are preselected (for example: **BSP > BSP > Board-specific BSP** and **HAL Drivers > all > r\_cgc**). All modules that are necessary for the modules selected in the **Stacks** tab are included automatically. You can include or exclude additional modules by ticking the box next to the required component.

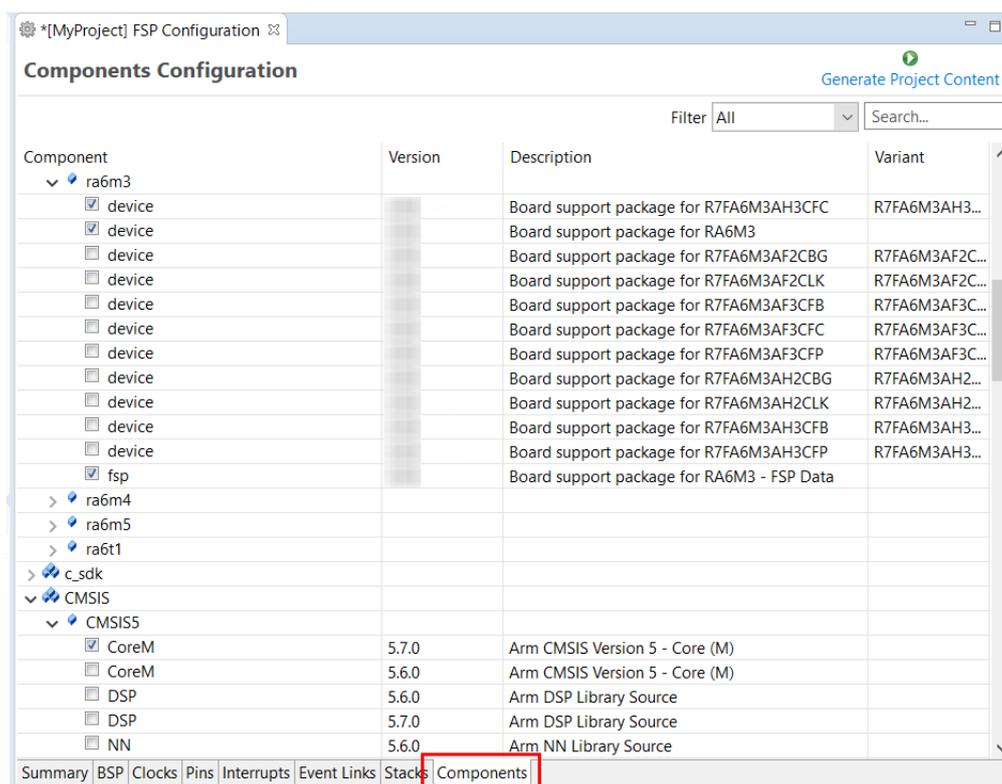


Figure 35: Components Tab

Clicking the **Generate Project Content** button copies the .c and .h files for each selected component into the following folders:

- ra/fsp/inc/api
- ra/fsp/inc/instances
- ra/fsp/src/bsp
- ra/fsp/src/<Driver\_Name>

e2 studio also creates configuration files in the ra\_cfg/fsp\_cfg folder with configuration options set in the **Stacks** tab.

## 2.2.8 Writing the Application

Once you have added Modules and drivers and set their configuration parameters in the **Stacks** tab, you can add the application code that calls the Modules and drivers.

*Note*

*To check your configuration, build the project once without errors before adding any of your own application code.*

### 2.2.8.1 Coding Features

e2 studio provides several efficiency improving features that help write code. Review these features prior to digging into the code development step-by-step sections that follow.

#### Autocomplete

Autocomplete is a context aware coding accelerator that suggests possible completions for partially

typed-in code elements. If you can 'guess' the first part of a macro, for example, the Autocomplete function can suggest options for completing the rest of the macro.

In the following example, a macro related to a BSP\_IO setting needs to be found. After typing BSP\_IO\_ in a source code file, pressing Ctrl + Space opens the Autocomplete list. This list shows a selection of context aware options for completing the macro. Scroll through the window to find the desired macro (in this case BSP\_IO\_LEVEL\_HIGH) and click on it to add it to your code.

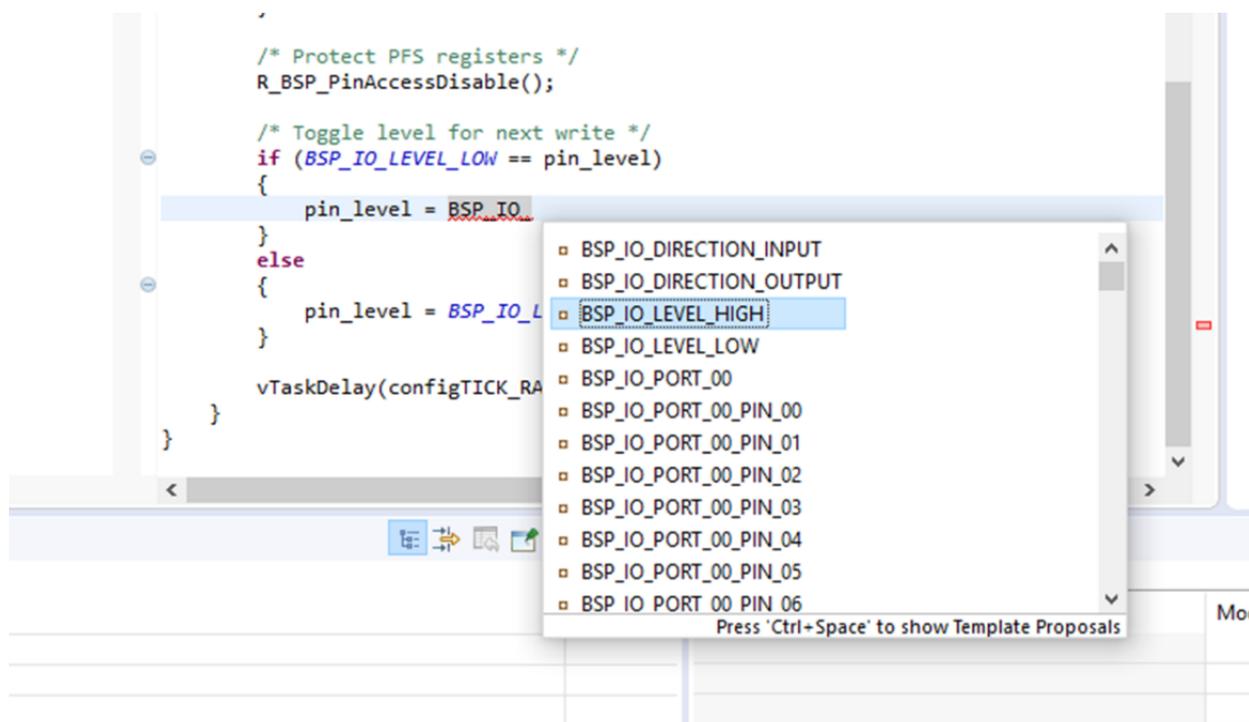


Figure 36: Autocomplete example

Other code elements can use autocomplete too. Some of the more common uses for Autocomplete include Enumerations, Types, and API functions - but try it in any situation you think the tool may have enough context to determine what you might be looking for.

For a hands-on experience using Autocomplete use the Quick FSP Labs for [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, and the Help system.

## Welcome Window

The e2 studio Welcome window displays useful information and common links to assist in development. Check out these resources to see what is available. They are updated with each release, so check back to see what has been added after a new release.

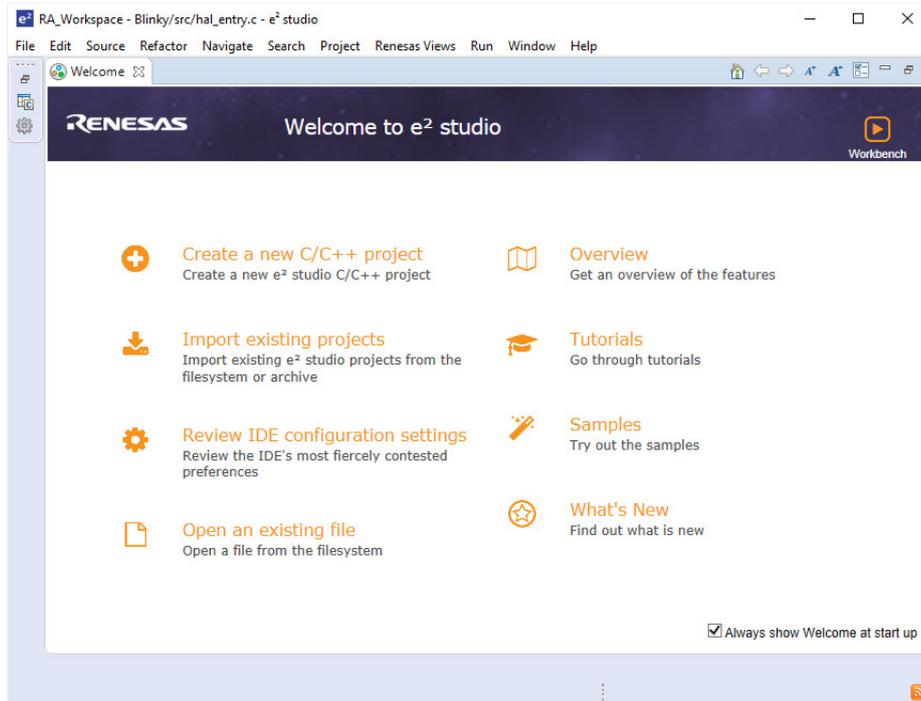


Figure 37: Welcome window

## Cheat Sheets

Cheat sheets are macro driven illustrations of some common tasks. They show, step-by-step, what commands and menus are used. These will be populated with more examples on each release. Cheat Sheets are available from the **Help** menu.

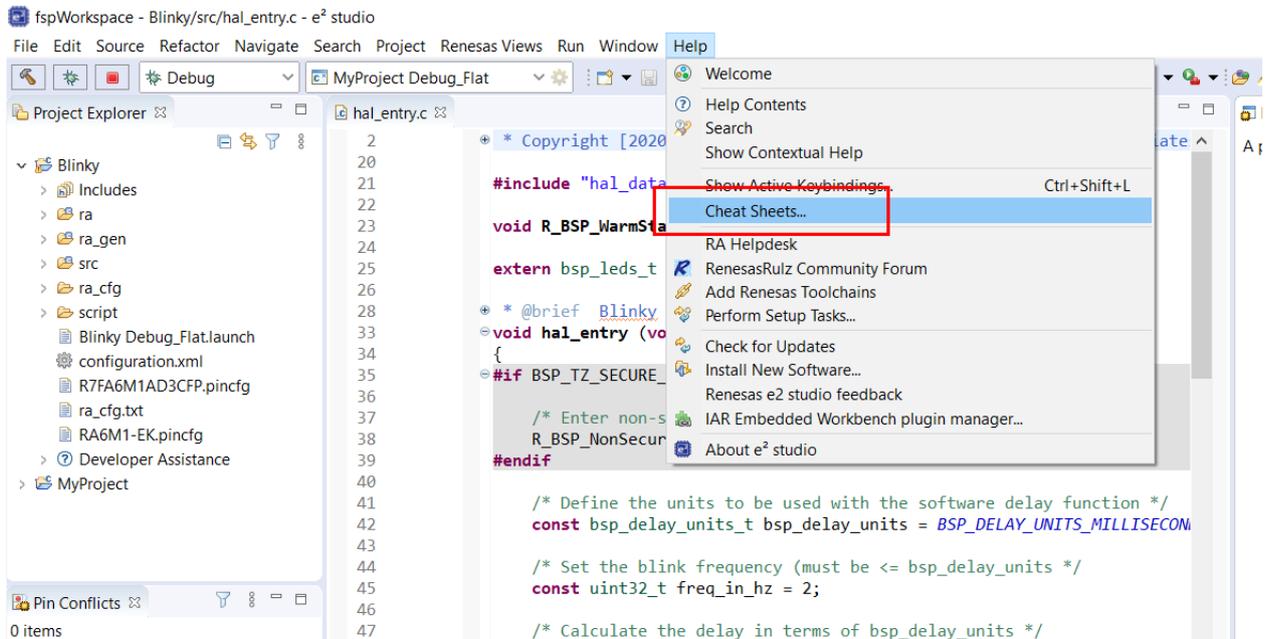


Figure 38: Cheat Sheets

## Developer Assistance

FSP Developer Assistance provides developers with module and Application Programming Interface (API) reference documentation in e2 studio. After configuring the threads and software stacks for an FSP project with the RA Configuration editor, Developer Assistance quickly helps you get started writing C/C++ application code for the project using the configured stack modules.

### 1. Expand the project explorer to view Developer Assistance

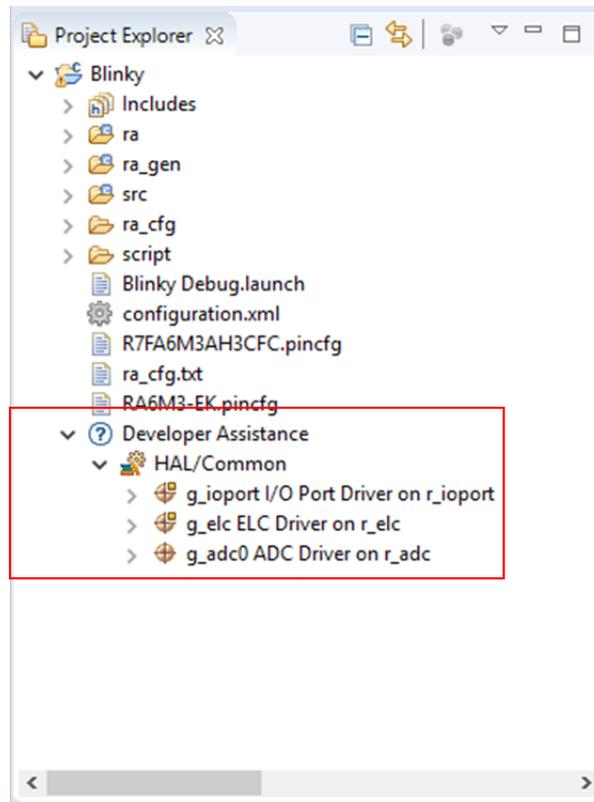


Figure 39: Developer Assistance

### 2. Expand a stack module to show its APIs

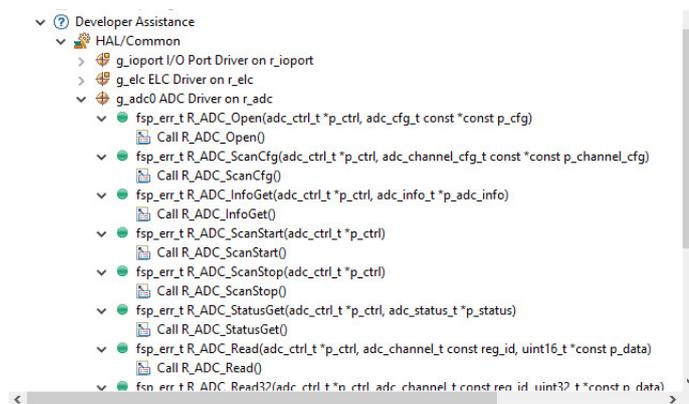


Figure 40: Developer Assistance APIs

### 3. Dragging and dropping an API from Develop Assistance to a source file helps to write source

code quickly.

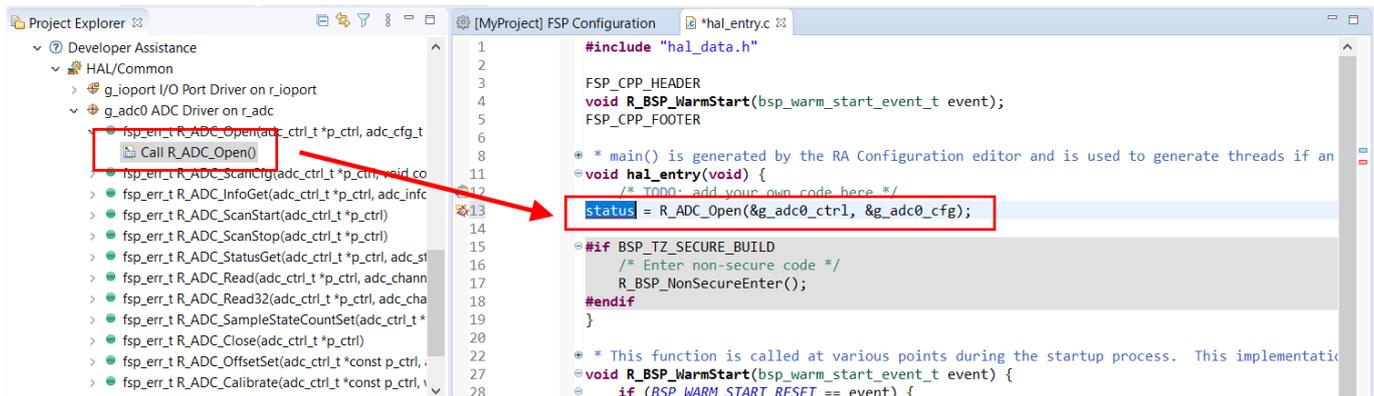


Figure 41: Dragging and Dropping an API in Developer Assistance

For a hands-on experience using Developer Assistance use the Quick FSP Labs for [An Introduction to Developer Assistance](#), [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, and the Help system.

### Information Icon

Information icons are available on each module in the thread stack. Clicking on these icons opens a module folder on GitHub that contains additional information on the module. An example information icon is shown below:

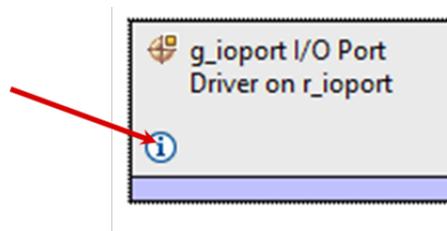


Figure 42: Information icon

### IDE Help

A good source of additional information for many FSP topics is the Help system. To get to the Help system, click on **Help** and then select **Help Contents** as seen below.

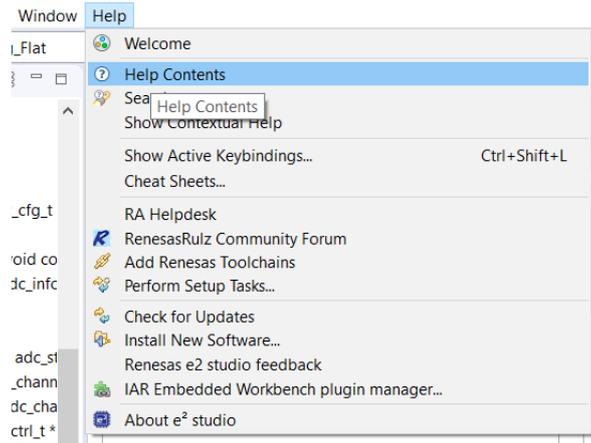


Figure 43: Opening the Help System

Once the Help system is open, select the **RA Contents** entry in the left side Guide-bar. Expand it to see the main RA Topics.

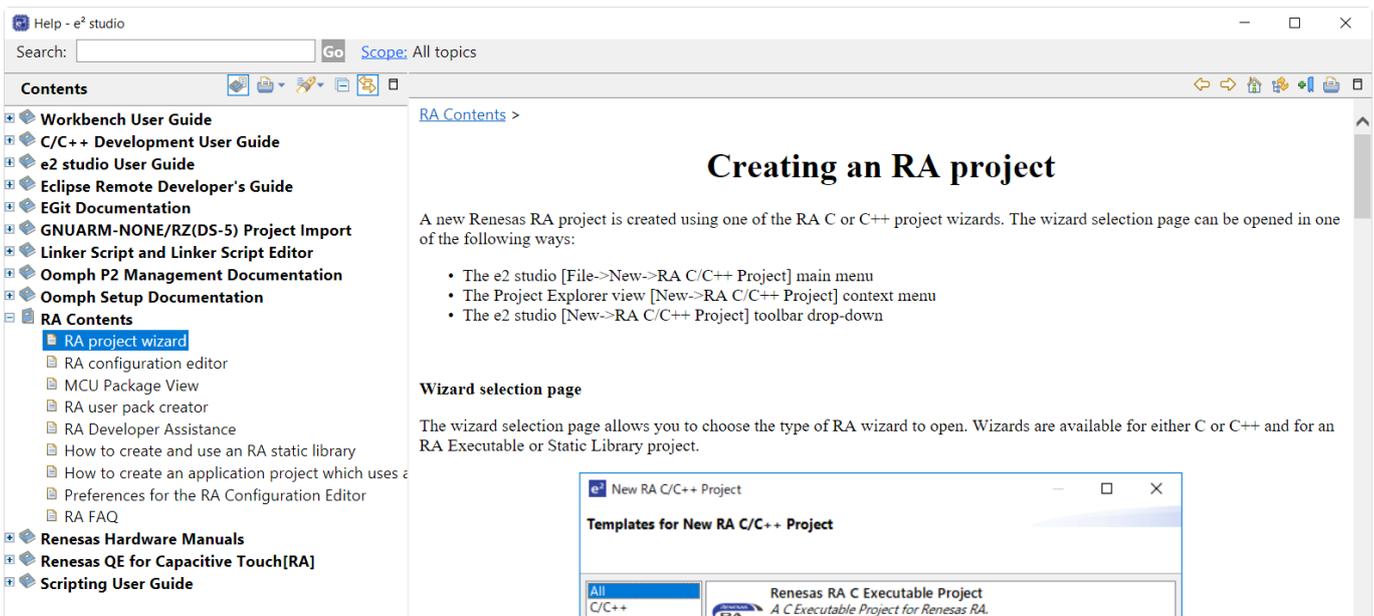


Figure 44: RA Content Help

You can also search for help topics by using the Search bar. Below is an example searching for Visual Expressions, a helpful feature in the e2 studio debugger.

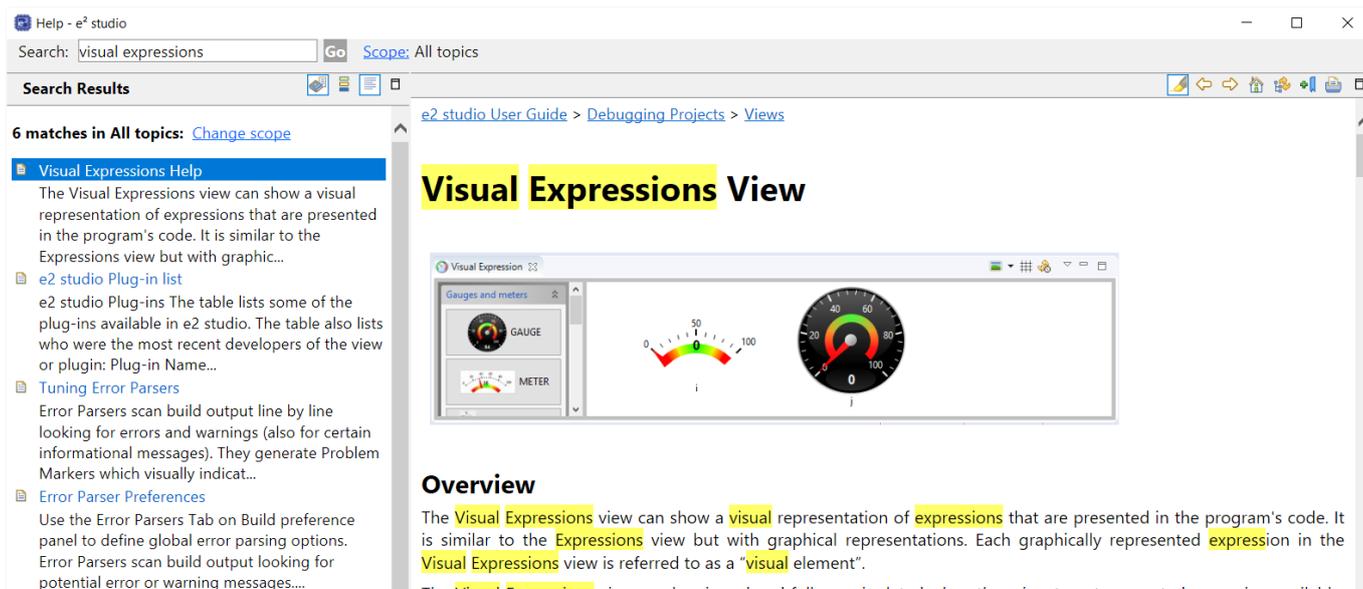


Figure 45: e2 studio Help from the Search Bar

For a hands-on experience using the Help system use the Quick FSP Labs for [An Introduction to Developer Assistance](#), [Creating Blinky from Scratch](#) and [Creating an RTC Blinky from Scratch](#). These 15-minute Do it Yourself labs take you through the step-by-step process of using Autocomplete, Developer Assistance, and the Help system.

### 2.2.8.2 HAL Modules in FSP: A Practical Description

The [FSP Architecture](#) section describes FSP stacks, modules and interfaces in significant detail, providing an understanding of the theory behind them. The following sections provides a quick and practical introduction on how to use API functions when writing code and where in the API reference sections you can find useful API related information.

#### Introduction to HAL Modules

In FSP, HAL module drivers provide convenient API functions that access RA processor peripheral features. Module properties are defined in the RA GUI configurator, eliminating the tedious and error prone process of setting peripheral control registers. When configuration is complete, the generator automatically creates the code needed to implement the associated API functions. API functions are the main way a developer interacts with the target processor and peripherals.

#### HAL Driver API Function Call Formats

HAL driver API functions all have a similar format. They all start with "R\_" to indicate they are HAL related functions. Next comes the module name followed by the function and any parameters. This format is illustrated below:

```
R_<module>_<function>( <parameters> );
```

Here are some examples:

```

status = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
status = R_GPT_Start(&g_timer0_ctrl);
status = R_GPT_PeriodSet(&g_timer0_ctrl, period);
status = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
status = R_ADC_InfoGet(&g_adc0_ctrl, &adc_info);

```

## HAL Driver API Call Reference Information

Each HAL module has a useful API Reference section that includes key details on each function. The function prototype is presented first, showing the return type (usually `fsp_status_t` for HAL functions) and the function parameters. A short description and any warnings or notes follow the function definition. In some cases, a code snippet is included to illustrate use of the function. Finally, all possible return values are provided to assist in debugging and error management.

### ◆ R\_GPT\_PeriodSet()

```

fsp_err_t R_GPT_PeriodSet ( timer_ctrl_t *const p_ctrl,
                           uint32_t const   period_counts
                           )

```

Sets period value provided. If the timer is running, the period will be updated after the next counter overflow. If the timer is stopped, this function resets the counter and updates the period. Implements `timer_api_t::periodSet`.

**Warning**  
If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and a GPT overflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter overflow after processing completes.

Example:

```

/* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
 * - If the PCLKD frequency has not changed since reset, the source clock
 *   frequency is
 *   BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
 * - Use the R_GPT_InfoGet function (it accounts for the divider).
 * - Calculate the current PCLKD frequency using R_FSP_SystemClockHzGet
 *   (FSP_PRIV_CLOCK_PCLKD) and right shift
 *   by timer_cfg_t::source_div.
 * This example uses the 3rd option (R_FSP_SystemClockHzGet).
 */
uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
    g_timer0_cfg.source_div;

/* Calculate the desired period based on the current clock. Note that this
 * calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
 * used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
    GPT_EXAMPLE_MSEC_PER_SEC);

/* Set the calculated period. */
err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
handle_error(err);

```

**Return values**

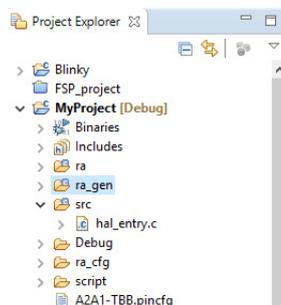
<code>FSP_SUCCESS</code>	Period value written successfully.
<code>FSP_ERR_ASSERTION</code>	<code>p_ctrl</code> was NULL.
<code>FSP_ERR_NOT_OPEN</code>	The instance is not opened.

Figure 46: Module Api Reference Section Example

### 2.2.8.3 RTOS-Independent Applications

To write application code:

1. Add all drivers and modules in the **Stacks** tab and resolve all dependencies flagged by e2 studio such as missing interrupts or drivers.
2. Configure the drivers in the **Properties** view.
3. In the Project Configuration view, click the **Generate Project Content** button.
4. In the **Project Explorer** view, double-click on the src/hal\_entry.c file to edit the source file.

**Note**

All configuration structures necessary for the driver to be called in the application are initialized in `ra_gen/hal_data.c`.

**Warning**

Do not modify the files in the directory `ra_gen`. These files are overwritten every time you push the **Generate Project Content** button.

5. Add your application code here:



Figure 47: Adding user code to hal\_entry.c

6. Build the project without errors by clicking on **Project > Build Project**.

The following tutorial shows how execute the steps above and add application code: [Tutorial: Using HAL Drivers - Programming the WDT](#).

The WDT example is a HAL level application which does not use an RTOS. The user guides for each module also include basic application code that you can add to `hal_entry.c`.

### 2.2.8.4 RTOS Applications

To write RTOS-aware application code using RTOS, follow these steps:

1. Add a thread using the **Stacks** tab.
2. Provide a unique name for the thread in the **Properties** view for this thread.

3. Configure all drivers and resources for this thread and resolve all dependencies flagged by e2 studio such as missing interrupts or drivers.
  4. Configure the thread objects.
  5. Provide unique names for each thread object in the **Properties** view for each object.
  6. Add more threads if needed and repeat steps 1 to 5.
  7. In the **RA Project Editor**, click the **Generate Project Content** button.
8. In the **Project Explorer** view, double-click on the src/my\_thread\_1\_entry.c file to edit the source file.

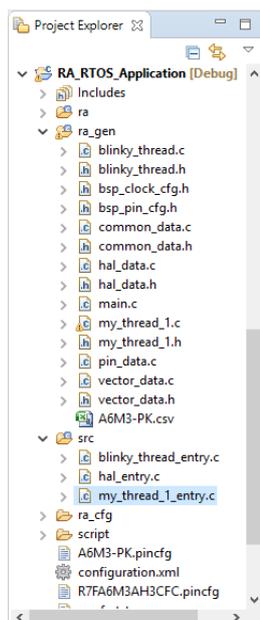


Figure 48: Generated files for an RTOS application

*Note*

All configuration structures necessary for the driver to be called in the application are initialized in ra\_gen/my\_thread\_1.c and my\_thread\_2.c

**Warning**

Do not modify the files in the directory ra\_gen. These files are overwritten every time you push the **Generate Project Content** button.

9. Add your application code here:

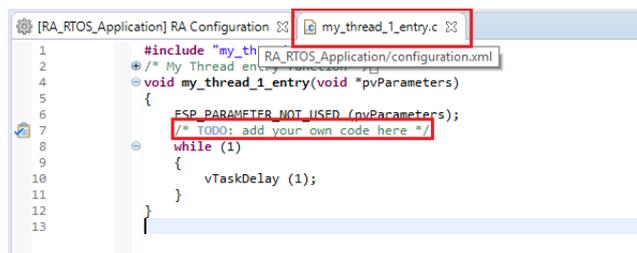


Figure 49: Adding user code to my\_thread\_1.entry

10. Repeat steps 1 to 9 for the next thread.

11. Build your project without errors by clicking on **Project > Build Project**.

## 2.2.8.5 Additional Resources for Application Development

### Example Projects

A wide variety of Example Projects for FSP and RA MCUs is available on the GitHub site here: <https://github.com/renesas/ra-fsp-examples>. Example projects are organized by target kit so it is easy to find all the examples for your kit of choice.

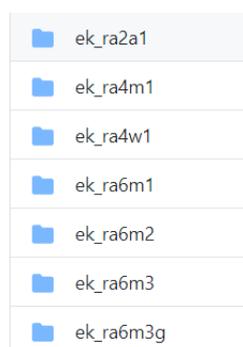


Figure 50: FSP Example Projects Organized by Kit

Projects are available as both downloadable zip files and as project source files. Typically, there is a project for each module. New example projects are being added periodically, so check back if a particular module isn't yet available.



Figure 51: A Selection of Example Projects Available on GitHub

### Quick Labs

A variety of Hands-on Do It Yourself labs are available on the Renesas RA and FSP Knowledge Base. Quick FSP Labs target the EK-RA6M3 kit and typically require only 15 minutes to complete. Each lab covers a couple related development tools and techniques like Autocomplete, Developer Assistance,

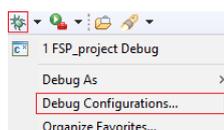
console I/O over RTT, and Visual Expressions, that can speed up the development process. A list of all available Quick Labs can be found here: <https://en-support.renesas.com/knowledgeBase/19450948>

## 2.2.9 Debugging the Project

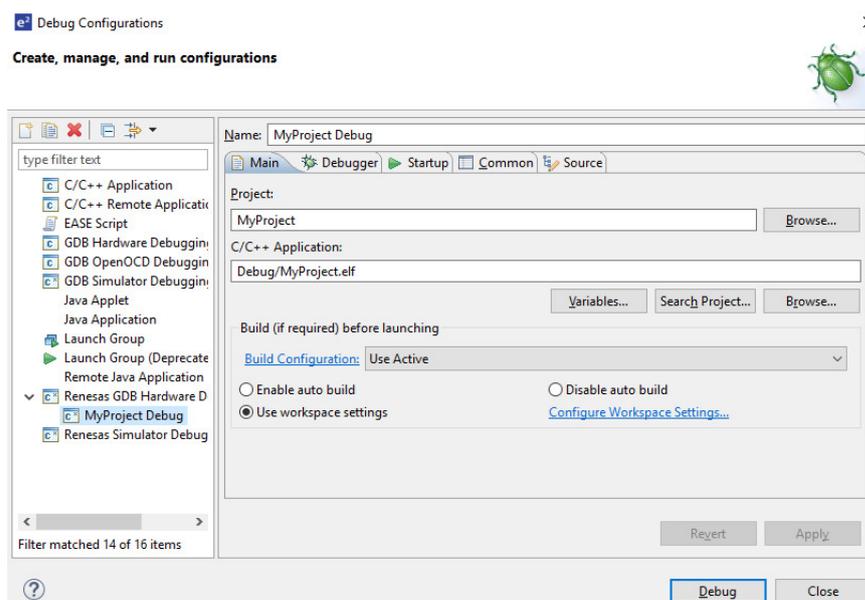
Once your project builds without errors, you can use the Debugger to download your application to the board and execute it.

To debug an application follow these steps:

1. On the drop-down list next to the debug icon, select **Debug Configurations**.



2. In the **Debug Configurations** view, click on your project listed as **MyProject Debug**.



3. Connect the board to your PC via either a standalone Segger J-Link debugger, a Segger J-Link On-Board (included on all RA EKs), or an E2 or E2 Lite and click **Debug**.

*Note*

*For details on using J-Link and connecting the board to the PC, see the Quick Start Guide included in the RA MCU Kit.*

## 2.2.10 Modifying Toolchain Settings

There are instances where it may be necessary to make changes to the toolchain being used (for example, to change optimization level of the compiler or add a library to the linker). Such modifications can be made from within e2 studio through the menu **Project > Properties > Settings** when the project is selected. The following screenshot shows the settings dialog for the GNU Arm toolchain. This dialog will look slightly different depending upon the toolchain being used.

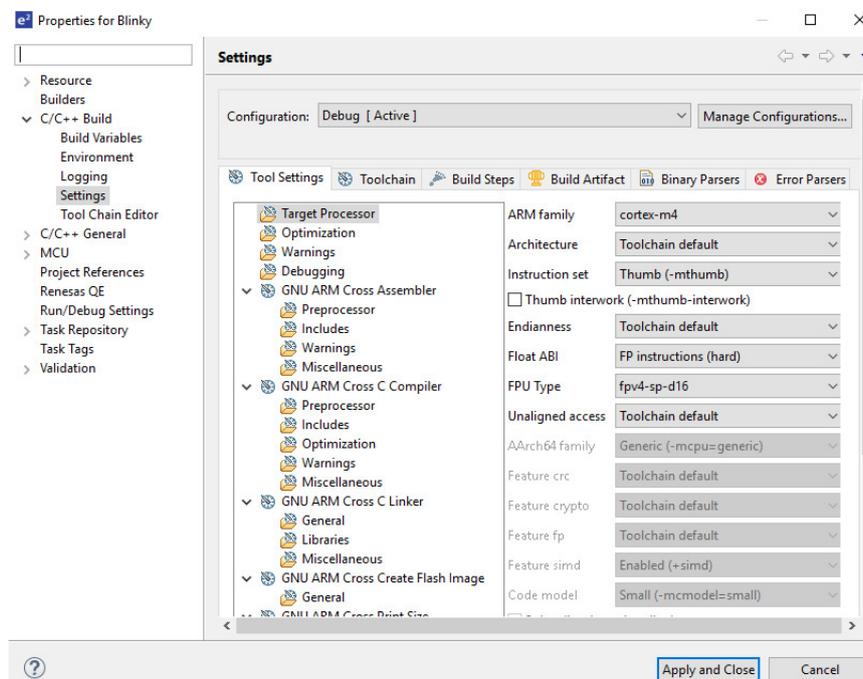


Figure 52: e2 studio Project toolchain settings

The scope for the settings is project scope which means that the settings are valid only for the project being modified.

The settings for the linker which control the location of the various memory sections are contained in a script file specific for the device being used. This script file is included in the project when it is created and is found in the script folder (for example, /script/a6m3.ld).

### 2.2.11 Creating RA project with ARM Compiler 6 in e2 studio

e2 studio does not include the ARM Compiler 6 (AC6) toolchain by default. Follow the steps below to integrate AC6 into e2 studio and create an AC6 RA project.

#### Note

*It is assumed that the user is already familiar with RA project creation in e2 studio. e2 studio does not include ARM Compiler 6 (AC6) toolchain by default.*

Steps 1 through 8 describe the process for integrating ARM Compiler 6 into e2 studio.

1. Download, install, and configure license for the AC6 toolchain (<https://developer.arm.com/tools-and-software/embedded/arm-compiler/downloads/version-6>).
2. Launch e2 studio.
3. Go to **Window > Preferences > Toolchains**.

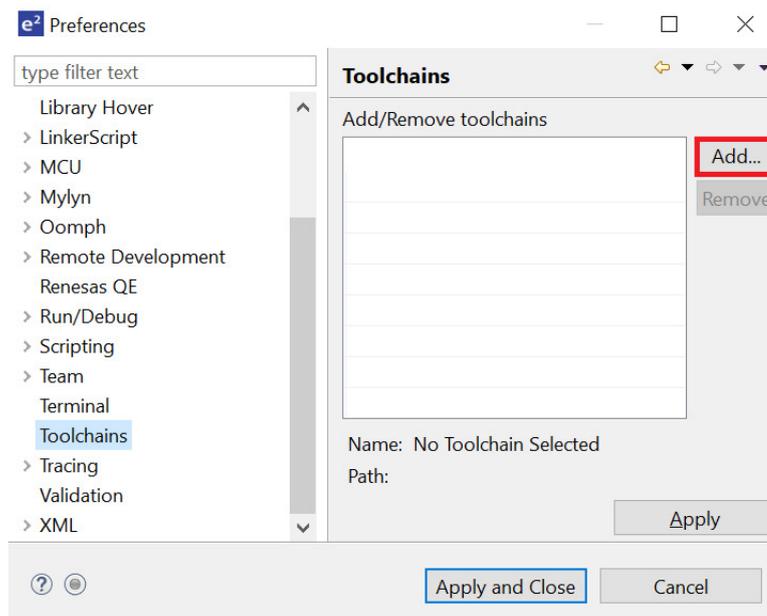
4. Click **Add**.

Figure 53: Add Toolchain

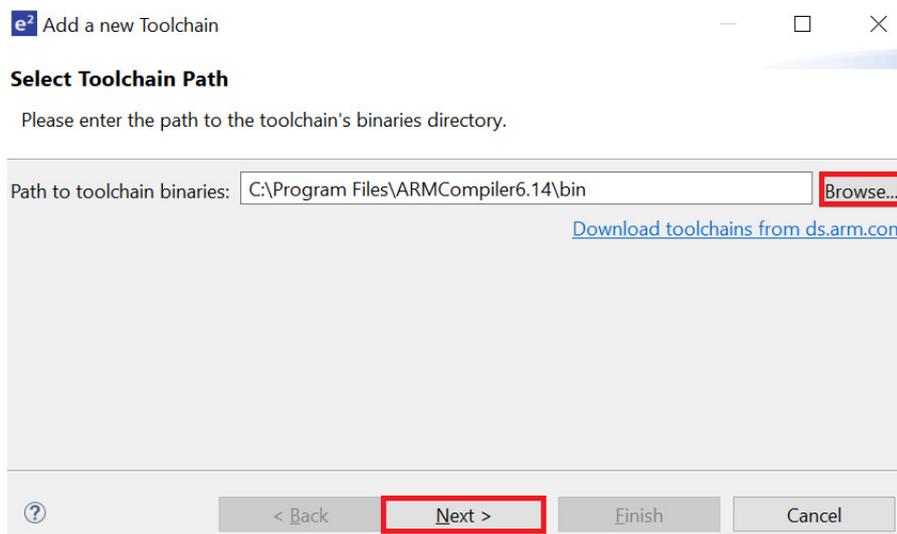
5. Browse to the path where AC6 toolchain is installed and select the \bin folder. Click **Next**.

Figure 54: Browse to AC6 Compiler

6. Toolchain information is displayed. Click **Finish**.

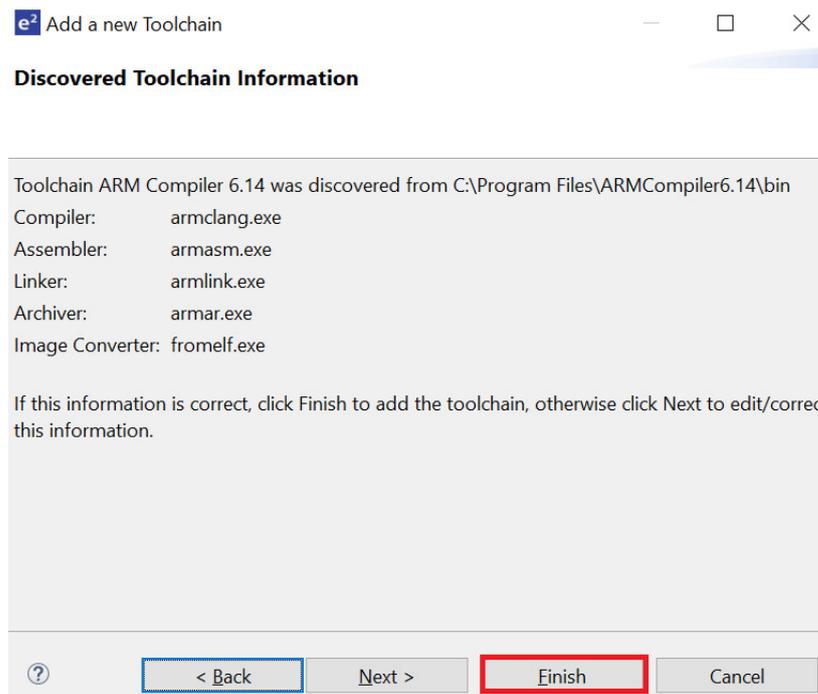


Figure 55: Toolchain Information

## 7. Click **Apply and Close**.

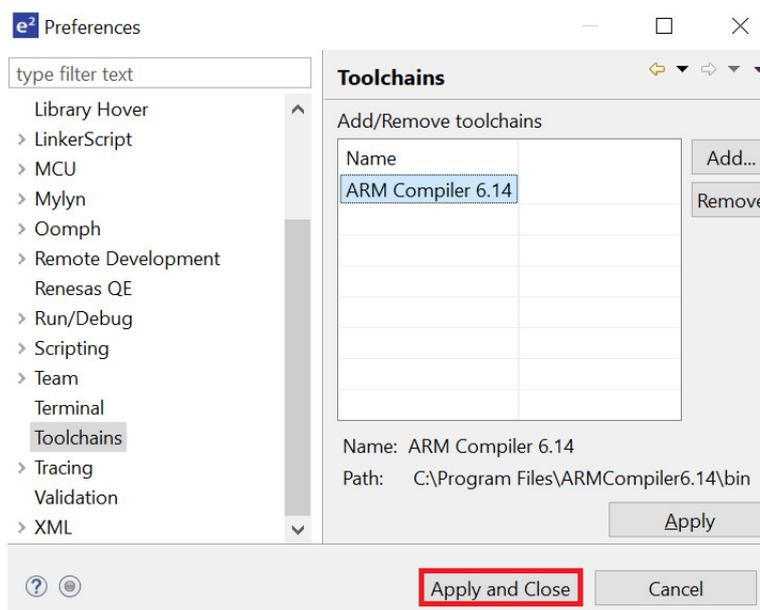


Figure 56: Apply and Close

## 8. Click **Restart Eclipse** when prompted.

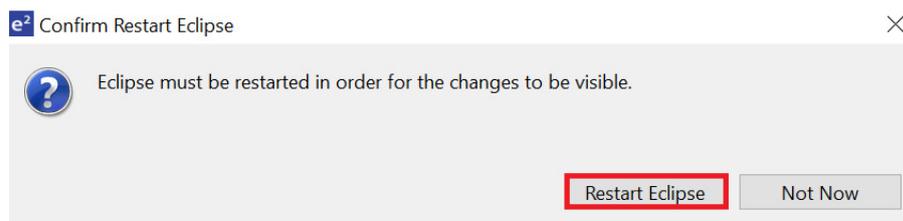


Figure 57: Restart Eclipse

9. When creating a new RA C/C++ project, select **ARM Compiler 6** included in the Toolchains section.

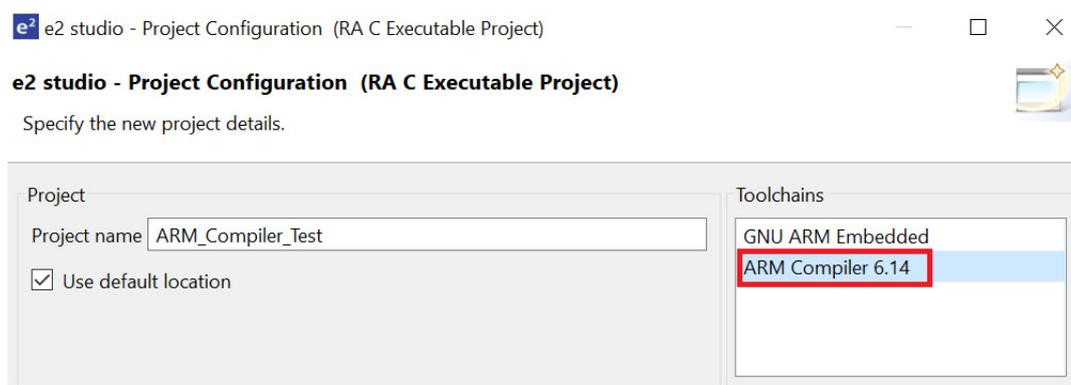


Figure 58: Select Arm Compiler

## 2.2.12 Importing an Existing Project into e2 studio

1. Start by opening e2 studio.
2. Open an existing Workspace to import the project and skip to step d. If the workspace doesn't exist, proceed with the following steps:
  - a. At the end of e2 studio startup, you will see the Workspace Launcher Dialog box as shown in the following figure.

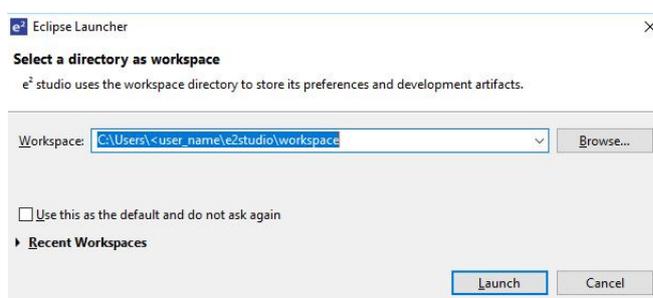


Figure 59: Workspace Launcher dialog

- b. Enter a new workspace name in the Workspace Launcher Dialog as shown in the following figure. e2 studio creates a new workspace with this name.

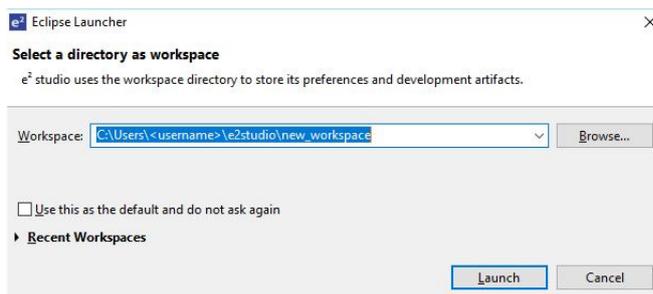


Figure 60: Workspace Launcher dialog - Select Workspace

- c. Click **Launch**.
- d. When the workspace is opened, you may see the Welcome Window. Click on the **Workbench** arrow button to proceed past the Welcome Screen as seen in the following figure.

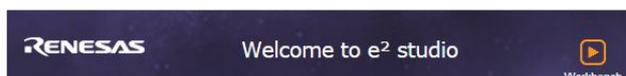


Figure 61: Workbench arrow button

3. You are now in the workspace that you want to import the project into. Click the **File** menu in the menu bar, as shown in the following figure.

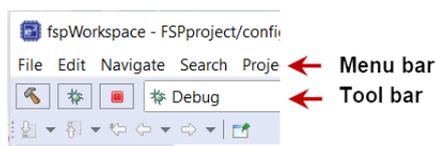


Figure 62: Menu and tool bar

4. Click **Import** on the **File** menu or in the menu bar, as shown in the following figure.

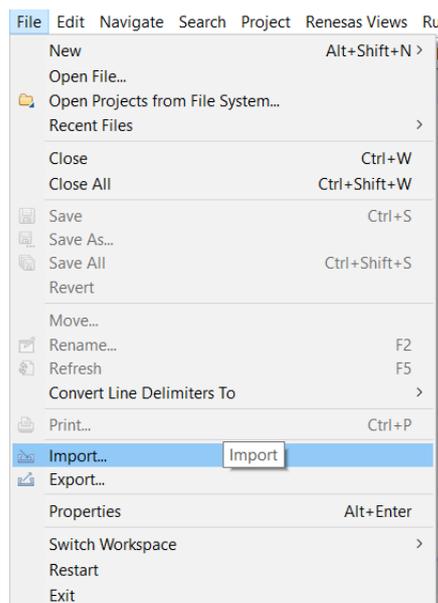


Figure 63: File drop-down menu

5. In the **Import** dialog box, as shown in the following figure, choose the **General** option, then **Existing Projects into Workspace**, to import the project into the current workspace.

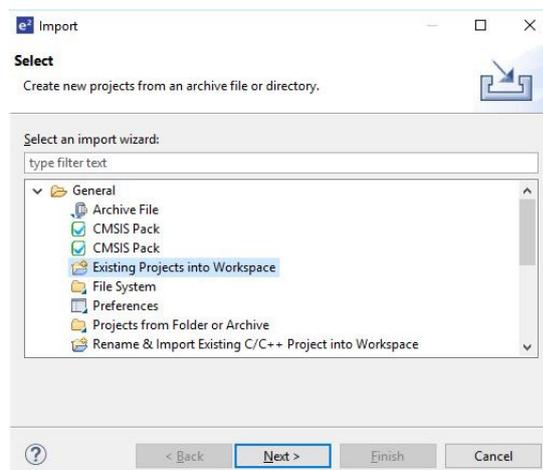


Figure 64: Project Import dialog with "Existing Projects into Workspace" option selected

6. Click **Next**.
7. To import the project, use either **Select archive file** or **Select root directory**.
  - a. Click **Select archive file** as shown in the following figure.

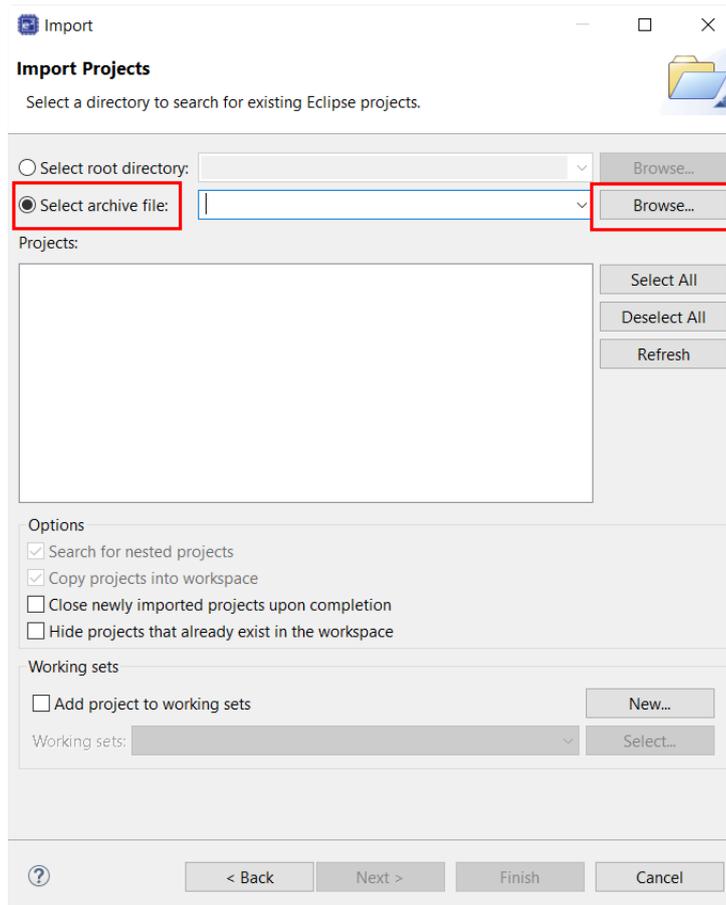


Figure 65: Import Existing Project dialog 1 - Select archive file

- b. Click **Select root directory** as shown in the following figure.

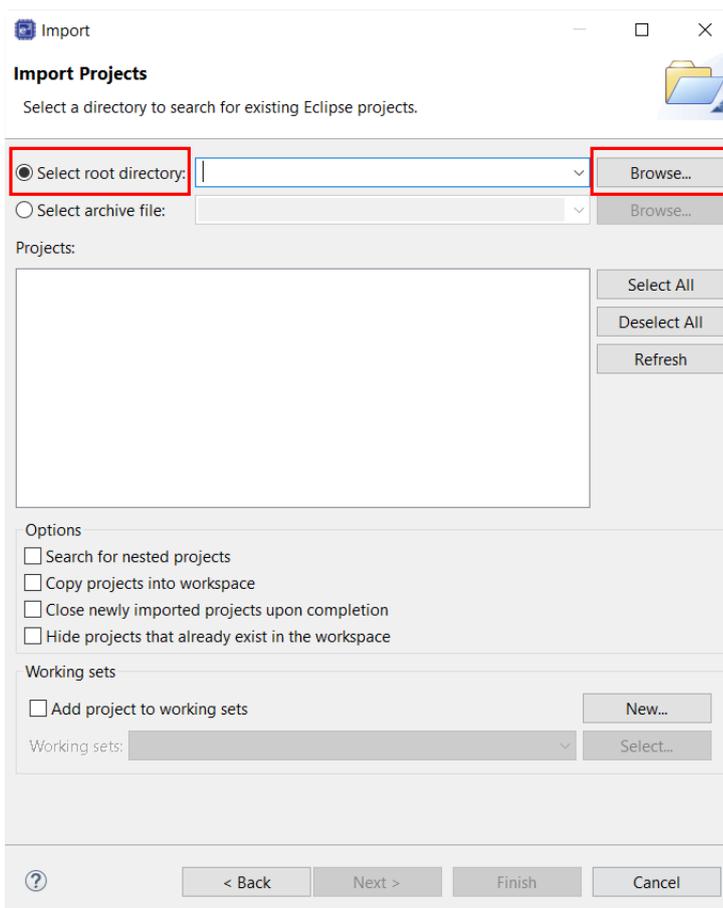


Figure 66: Import Existing Project dialog 1 - Select root directory

8. Click **Browse**.
9. For **Select archive file**, browse to the folder where the zip file for the project you want to import is located. For **Select root directory**, browse to the project folder that you want to import.
10. Select the file for import. In our example, it is CAN\_HAL\_MG\_AP.zip or CAN\_HAL\_MG\_AP.
11. Click **Open**.
12. Select the project to import from the list of **Projects**, as shown in the following figure.

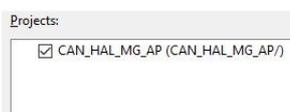


Figure 67: Import Existing Project dialog 2

13. Click **Finish** to import the project.

## 2.3 Tutorial: Your First RA MCU Project - Blinky

### 2.3.1 Tutorial Blinky

The goal of this tutorial is to quickly get acquainted with the Flexible Platform by moving through the

steps of creating a simple application using e2 studio and running that application on an RA MCU board.

## 2.3.2 What Does Blinky Do?

The application used in this tutorial is Blinky, traditionally the first program run in a new embedded development environment.

Blinky is the "Hello World" of microcontrollers. If the LED blinks you know that:

- The toolchain is setup correctly and builds a working executable image for your chip.
- The debugger has installed with working drivers and is properly connected to the board.
- The board is powered up and its jumper and switch settings are probably correct.
- The microcontroller is alive, the clocks are running, and the memory is initialized.

The Blinky example application used in this tutorial is designed to run the same way on all boards offered by Renesas that hold the RA microcontroller. The code in Blinky is completely board independent. It does the work by calling into the BSP (board support package) for the particular board it is running on. This works because:

- Every board has at least one LED connected to a GPIO pin.
- That one LED is always labelled LED1 on the silk screen.
- Every BSP supports an API that returns a list of LEDs on a board, and their port and pin assignments.

## 2.3.3 Prerequisites

To follow this tutorial, you need:

- Windows based PC
- e2 studio
- Flexible Software Package
- An RA MCU board kit

## 2.3.4 Create a New Project for Blinky

The creation and configuration of an RA MCU project is the first step in the creation of an application. The base RA MCU pack includes a pre-written Blinky example application that is simple and works on all Renesas RA MCU boards.

Follow these steps to create an RA MCU project:

1. In e2 studio, click **File > New > C/C++ Project** and select **Renesas RA** and **Renesas RA C/C++ Project**.
2. Assign a name to this new project. Blinky is a good name to use for this tutorial.
3. Click **Next**. The **Project Configuration** window shows your selection.

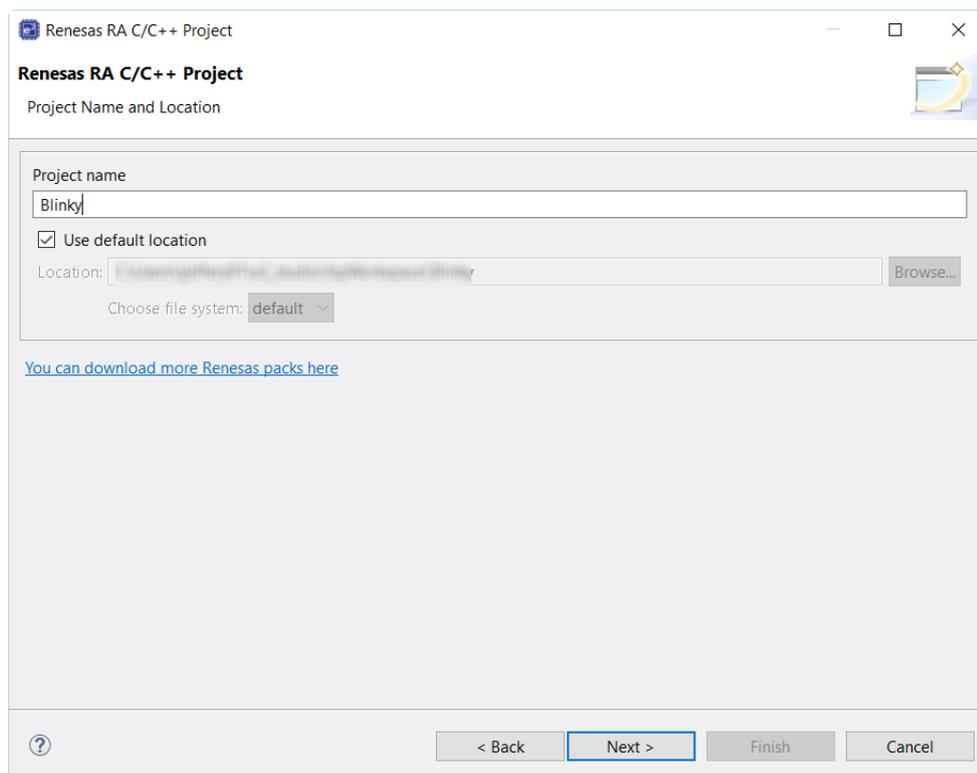


Figure 68: e2 studio Project Configuration window (part 1)

4. Select the board support package by selecting the name of your board from the **Device Selection** drop-down list and click **Next**.

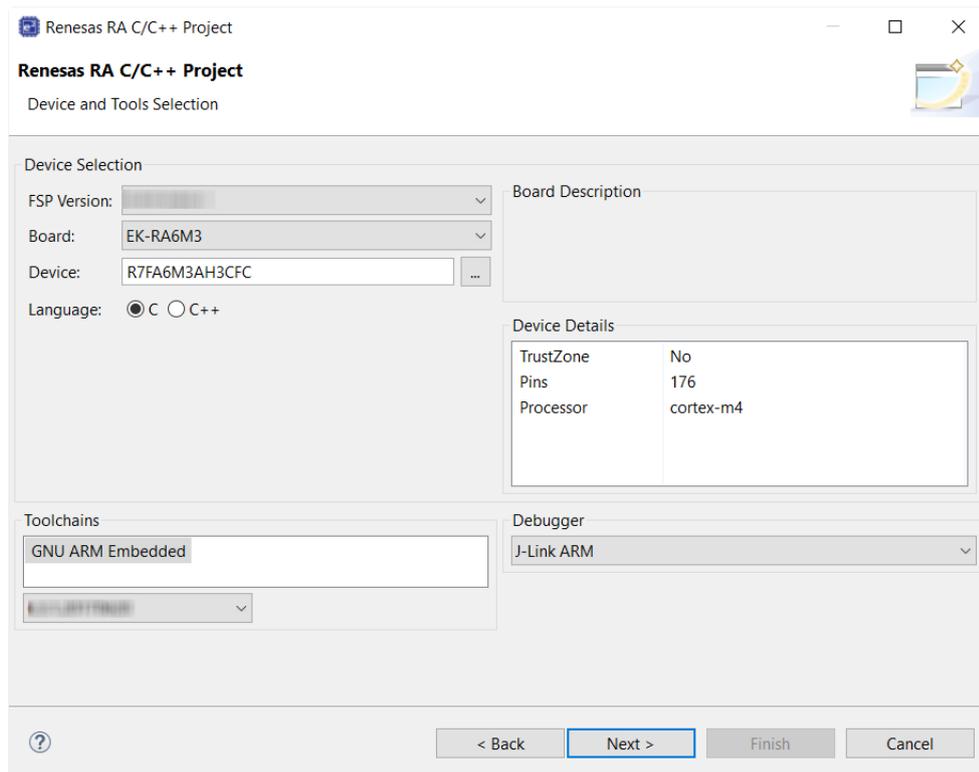


Figure 69: e2 studio Project Configuration window (part 2)

5. Select the build artifact and RTOS.

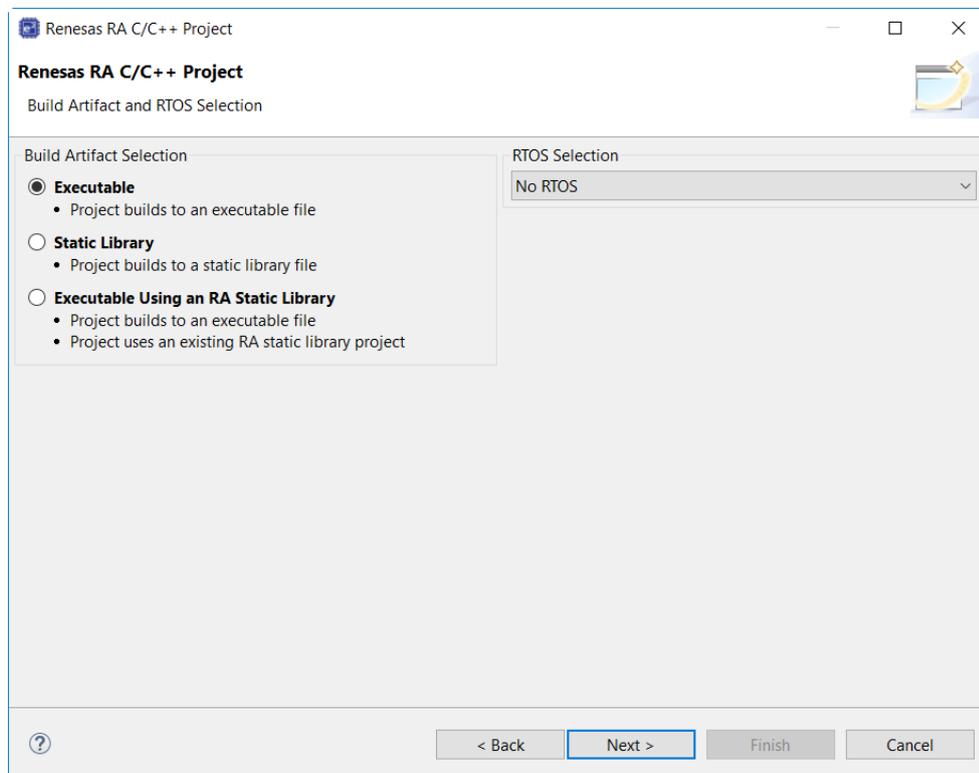


Figure 70: e2 studio Project Configuration window (part 3)

6. Select the Blinky template for your board and click **Finish**.

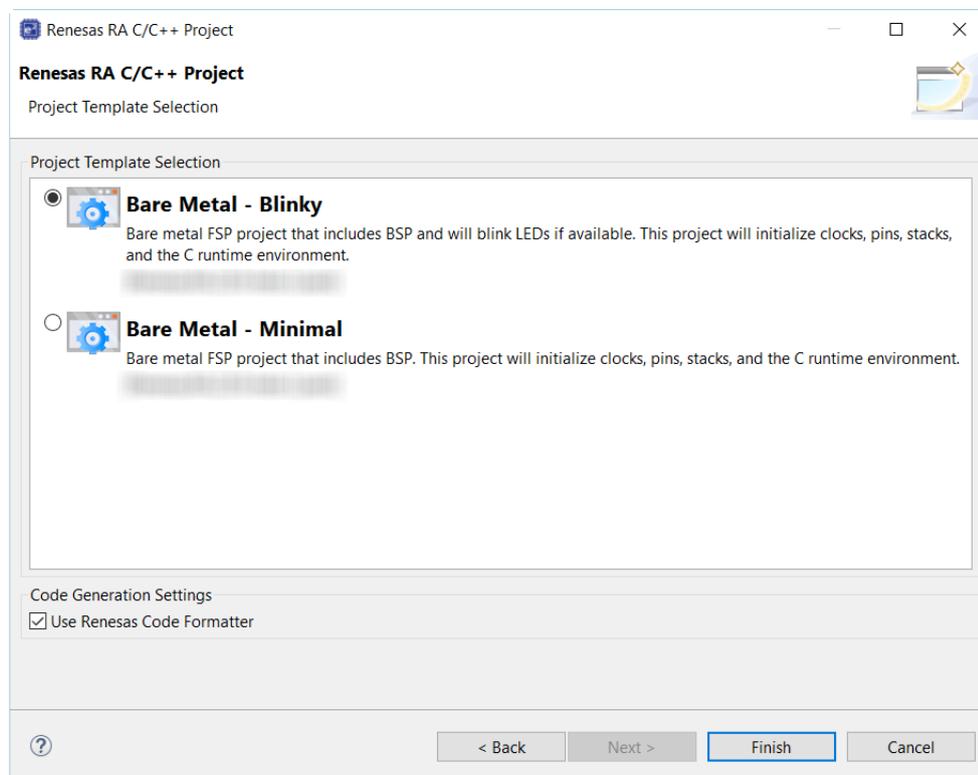


Figure 71: e2 studio Project Configuration window (part 4)

Once the project has been created, the name of the project will show up in the **Project Explorer** window of e2 studio. Now click the **Generate Project Content** button in the top right corner of the **Project Configuration** window to generate your board specific files.

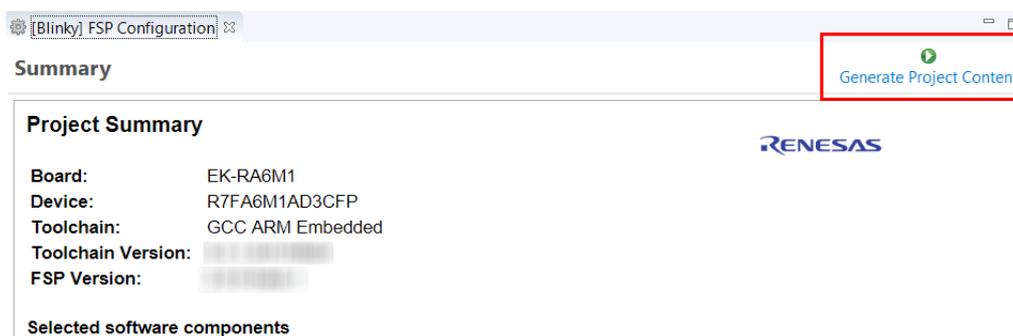


Figure 72: e2 studio Project Configuration tab

Your new project is now created, configured, and ready to build.

### 2.3.4.1 Details about the Blinky Configuration

The **Generate Project Content** button creates configuration header files, copies source files from templates, and generally configures the project based on the state of the **Project Configuration** screen.

For example, if you check a box next to a module in the **Components** tab and click the **Generate Project Content** button, all the files necessary for the inclusion of that module into the project will be copied or created. If that same check box is then unchecked those files will be deleted.

#### 2.3.4.2 Configuring the Blinky Clocks

By selecting the Blinky template, the clocks are configured by e2 studio for the Blinky application. The clock configuration tab (see [Configuring Clocks](#)) shows the Blinky clock configuration. The Blinky clock configuration is stored in the BSP clock configuration file (see [BSP Clock Configuration](#)).

#### 2.3.4.3 Configuring the Blinky Pins

By selecting the Blinky template, the GPIO pins used to toggle the LED1 are configured by e2 studio for the Blinky application. The pin configuration tab shows the pin configuration for the Blinky application (see [Configuring Pins](#)). The Blinky pin configuration is stored in the BSP configuration file (see [BSP Pin Configuration](#)).

#### 2.3.4.4 Configuring the Parameters for Blinky Components

The Blinky project automatically selects the following HAL components in the Components tab:

- r\_ioport

To see the configuration parameters for any of the components, check the **Properties** tab in the HAL window for the respective driver (see [Adding and Configuring HAL Drivers](#)).

#### 2.3.4.5 Where is main()?

The main function is located in < project >/ra\_gen/main.c. It is one of the files that are generated during the project creation stage and only contains a call to hal\_entry(). For more information on generated files, see [Adding and Configuring HAL Drivers](#).

#### 2.3.4.6 Blinky Example Code

The blinky application is stored in the hal\_entry.c file. This file is generated by e2 studio when you select the Blinky Project template and is located in the project's src/ folder.

The application performs the following steps:

1. Get the LED information for the selected board by bsp\_leds\_t structure.
2. Define the output level HIGH for the GPIO pins controlling the LEDs for the selected board.
3. Get the selected system clock speed and scale down the clock, so the LED toggling can be observed.
4. Toggle the LED by writing to the GPIO pin with R\_BSP\_PinWrite((bsp\_io\_port\_pin\_t) pin, pin\_level);

### 2.3.5 Build the Blinky Project

Highlight the new project in the **Project Explorer** window by clicking on it and build it.

There are three ways to build a project:



Refer to your board's user manual to learn how to connect the JTAG debugger to e2 studio.

### 2.3.6.2 Debug steps

To debug the Blinky application, follow these steps:

1. Configure the debugger for your project by clicking **Run > Debugger Configurations ...**

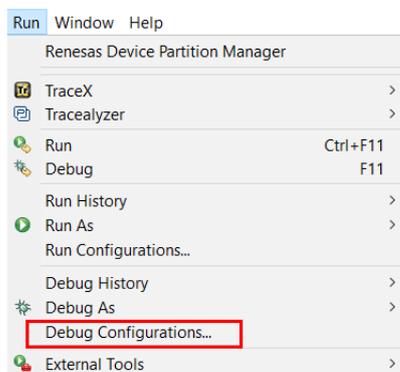


Figure 75: e2 studio Debug icon

or by selecting the drop-down menu next to the bug icon and selecting **Debugger Configurations ...**

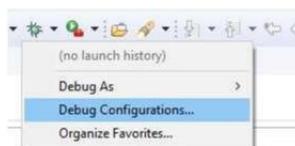


Figure 76: e2 studio Debugger Configurations selection option

2. Select your debugger configuration in the window. If it is not visible then it must be created by clicking the **New** icon in the top left corner of the window. Once selected, the **Debug Configuration** window displays the Debug configuration for your Blinky project.

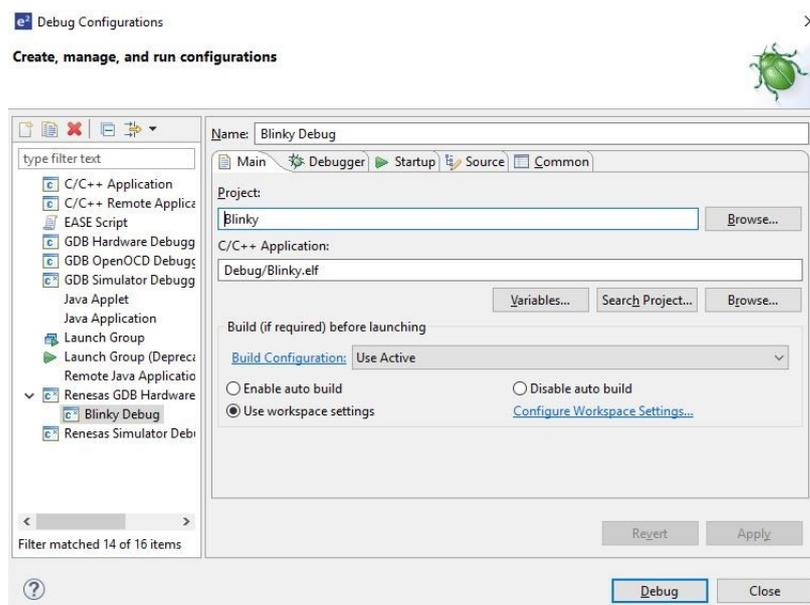
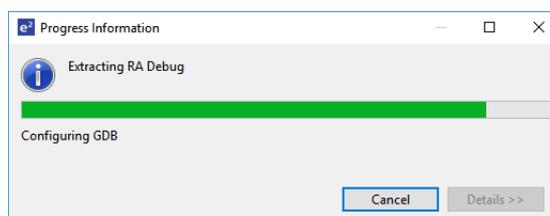


Figure 77: e2 studio Debugger Configurations window with Blinky project

3. Click **Debug** to begin debugging the application.

4. Extracting RA Debug.



### 2.3.6.3 Details about the Debug Process

In debug mode, e2 studio executes the following tasks:

1. Downloading the application image to the microcontroller and programming the image to the internal flash memory.
2. Setting a breakpoint at main().
3. Setting the stack pointer register to the stack.
4. Loading the program counter register with the address of the reset vector.
5. Displaying the startup code where the program counter points to.

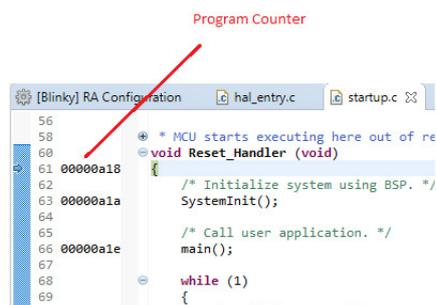


Figure 78: e2 studio Debugger memory window

## 2.3.7 Run the Blinky Project

While in Debug mode, click **Run > Resume** or click on the **Play** icon twice.



Figure 79: e2 studio Debugger Play icon

The LEDs on the board marked LED1, LED2, and LED3 should now be blinking.

## 2.4 Tutorial: Using HAL Drivers - Programming the WDT

### 2.4.1 Application WDT

This tutorial illustrates the creation of a simple application that uses the Watchdog Timer module to monitor program operation. The tutorial shows each step in the development process and in particular identifies the auto-generated files and project structure created when using FSP and its GUI based configurator. The level of detail provided here is more than is normally needed during development but can be helpful in explaining how FSP works behind the scenes to simplify your work.

This application makes use of the following FSP modules:

- [MCU Board Support Package](#)
- [Watchdog Timer \(r\\_wdt\)](#)
- [I/O Ports \(r\\_ioport\)](#)

### 2.4.2 Creating a WDT Application Using the RA MCU FSP and e2 studio

#### 2.4.2.1 Using the FSP and e2 studio

The Flexible Software Package (FSP) from Renesas provides a complete driver library for developing RA MCU applications. The FSP provides Hardware Abstraction Layer (HAL) drivers, Board Support Package (BSP) drivers for the developer to use to create applications. The FSP is integrated into Renesas e2 studio based on eclipse providing build (editor, compiler and linker) and debug phases with an extended GNU Debug (GDB) interface.

#### 2.4.2.2 The WDT Application

The flowchart for the WDT application is shown below.

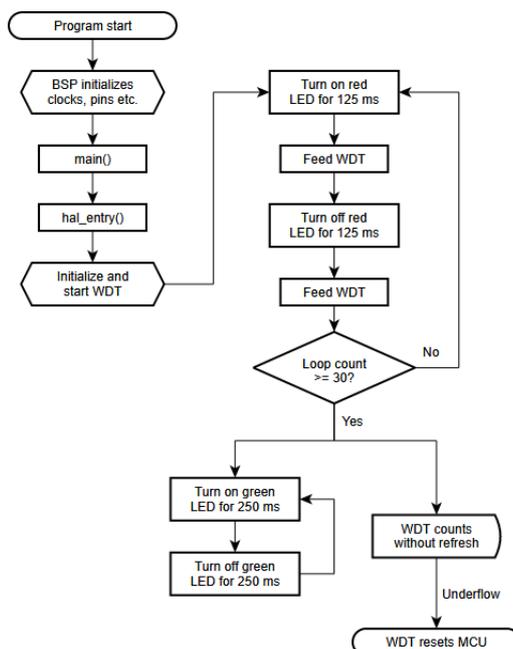


Figure 80: WDT Application flow diagram

### 2.4.2.3 WDT Application flow

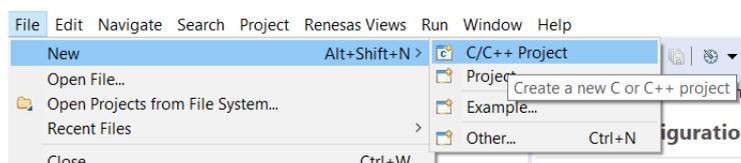
The main sections of the WDT application are:

1. The BSP initializes the clocks, pins and other elements of the MCU readying the application to run.
2. main() calls hal\_entry(). The function hal\_entry() is created by the FSP with a placeholder for user code. The code for the WDT is added to this function.
3. Initialize the WDT, but do not start it.
4. Start the WDT by refreshing it.
5. In the first loop the red LED flashes 30 times and refreshes the watchdog each time the LED state is changed.
6. In the second loop, the green LED flashes, but the program DOES NOT refresh the watchdog. After the watchdog timeout period the device will reset which can be observed by the red LED flashing again as the sequence repeats.

### 2.4.3 Creating the Project with e2 studio

Start e2 studio and choose a workspace folder in the Workspace Launcher. Configure a new RA MCU project as follows.

1. Select **File > New > RA C/C++ Project**. Then select the template for the project.



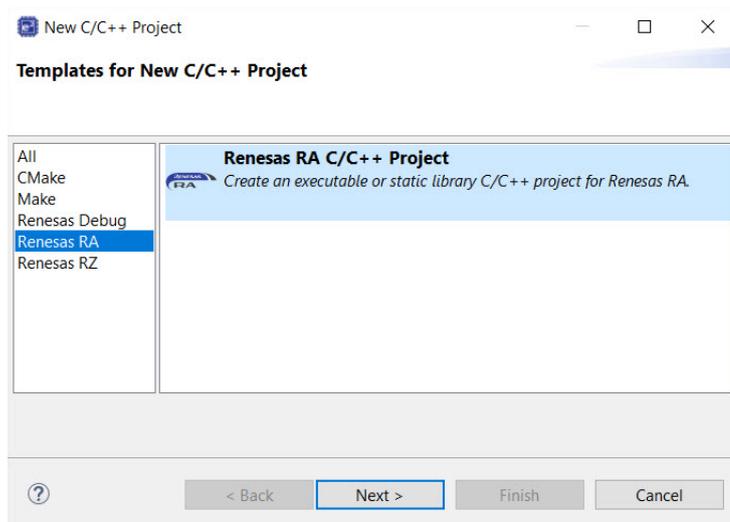


Figure 81: Creating a new project

2. In the e2 studio Project **Configuration (RA Project)** window enter a project name, for example, WDT\_Application. In addition, select the toolchain. If you want to choose new locations for the project unselect **Use default location**. Click **Next**.

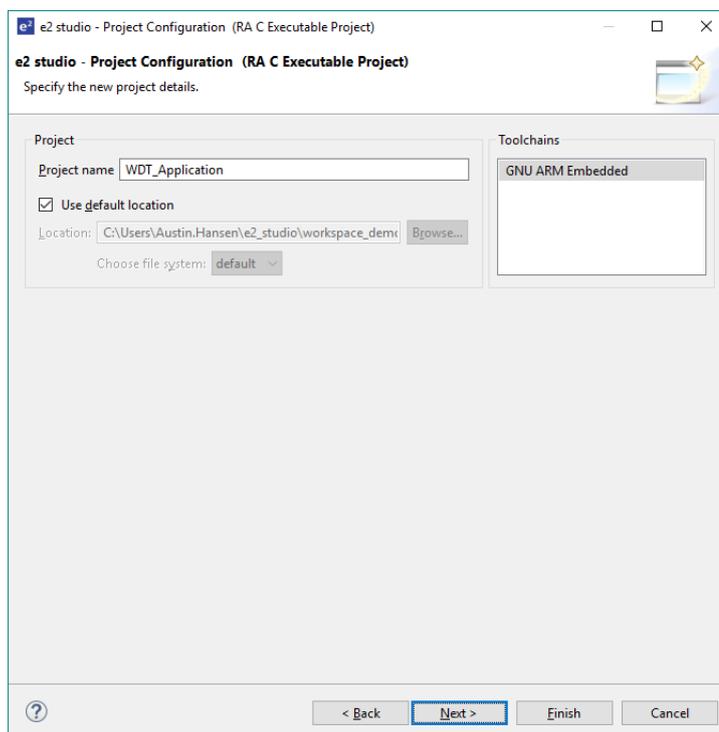


Figure 82: Project configuration (part 1)

3. This application runs on the EK-RA6M3 board. So, for the **Board** select **EK-RA6M3**.

This will automatically populate the **Device** drop-down with the correct device used on this board. Select the **Toolchain** version. Select **J-Link ARM** as the **Debugger**. Click **Next** to configure the project.

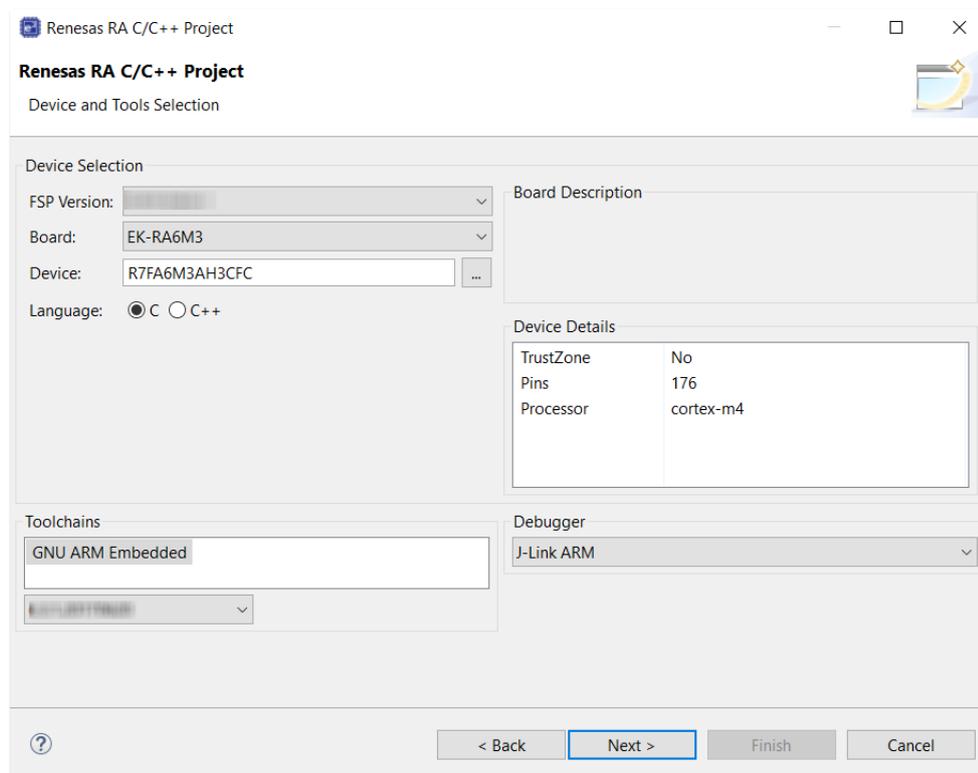


Figure 83: Project configuration (part 2)

The project template is now selected. As no RTOS is required select **Bare Metal - Blinky**.

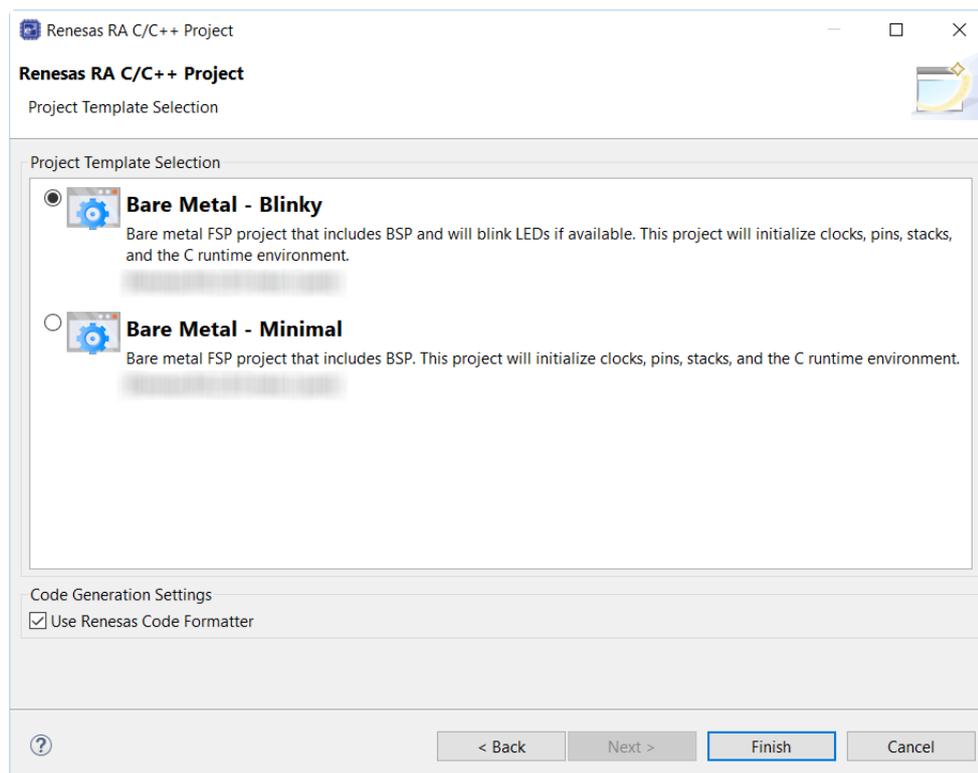


Figure 84: Project configuration (part 3)

#### 4. Click **Finish**.

e2 studio creates the project and opens the **Project Explorer** and **Project Configuration Settings** views with the **Summary** page showing a summary of the project configuration.

### 2.4.4 Configuring the Project with e2 studio

e2 studio simplifies and accelerates the project configuration process by providing a GUI interface for selecting the options to configure the project.

e2 studio offers a selection of perspectives presenting different windows to the user depending on the operation in progress. The default perspectives are **C/C++**, **FSP Configuration** and **Debug**. The perspective can be changed by selecting a new one from the buttons at the top right.

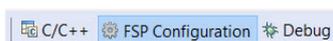


Figure 85: Selecting a perspective

The **C/C++** perspective provides a layout selected for code editing. The **FSP Configuration** perspective provides elements for configuring a RA MCU project, and the **Debug** perspective provides a view suited for debugging.

1. In order to configure the project settings ensure the **FSP Configuration** perspective is selected.

2. Ensure the **Project Configuration [WDT Application]** is open. It is already open if the Summary information is visible. To open the Project Configuration now or at any time make sure the **RA Configuration** perspective is selected and double-click on the configuration.xml file in the Project Explorer pane on the right side of e2 studio.

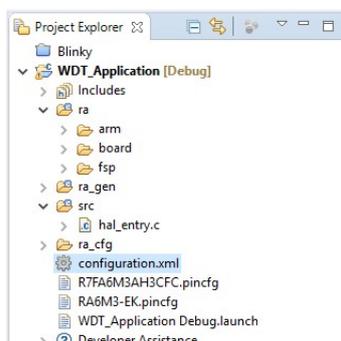


Figure 86: RA MCU Project Configuration Settings

At the base of the Project Configuration view there are several tabs for configuring the project. A project may require changes to some or all of these tabs. The tabs are shown below.

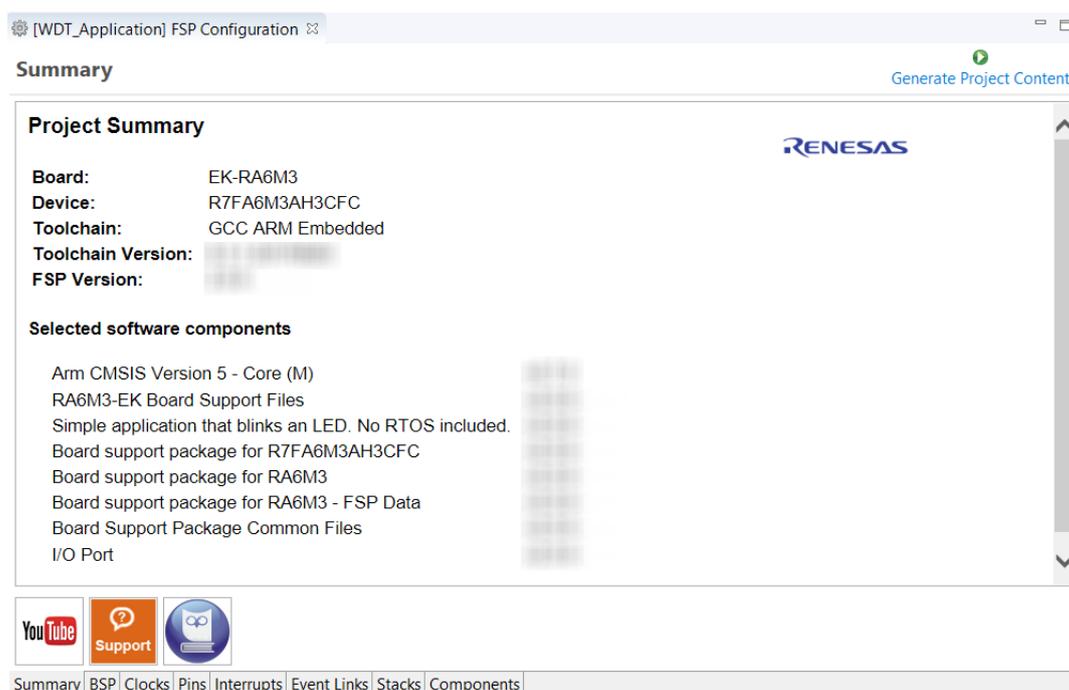


Figure 87: Project Configuration Tabs

#### 2.4.4.1 BSP Tab

The **BSP** tab allows the Board Support Package (BSP) options to be modified from their defaults. For this particular WDT project no changes are required. However, if you want to use the WDT in auto-start mode, you can configure the settings of the OFS0 (Option Function Select Register 0) register in the **BSP** tab. See the RA Hardware User's Manual for details on the WDT autostart mode.

#### 2.4.4.2 Clocks Tab

The **Clocks** tab presents a graphical view of the clock tree of the device. The drop-down boxes in the GUI enables configuration of the various clocks. The WDT uses PCLKB. The default output frequency for this clock is 60 MHz. Ensure this clock is outputting this value.

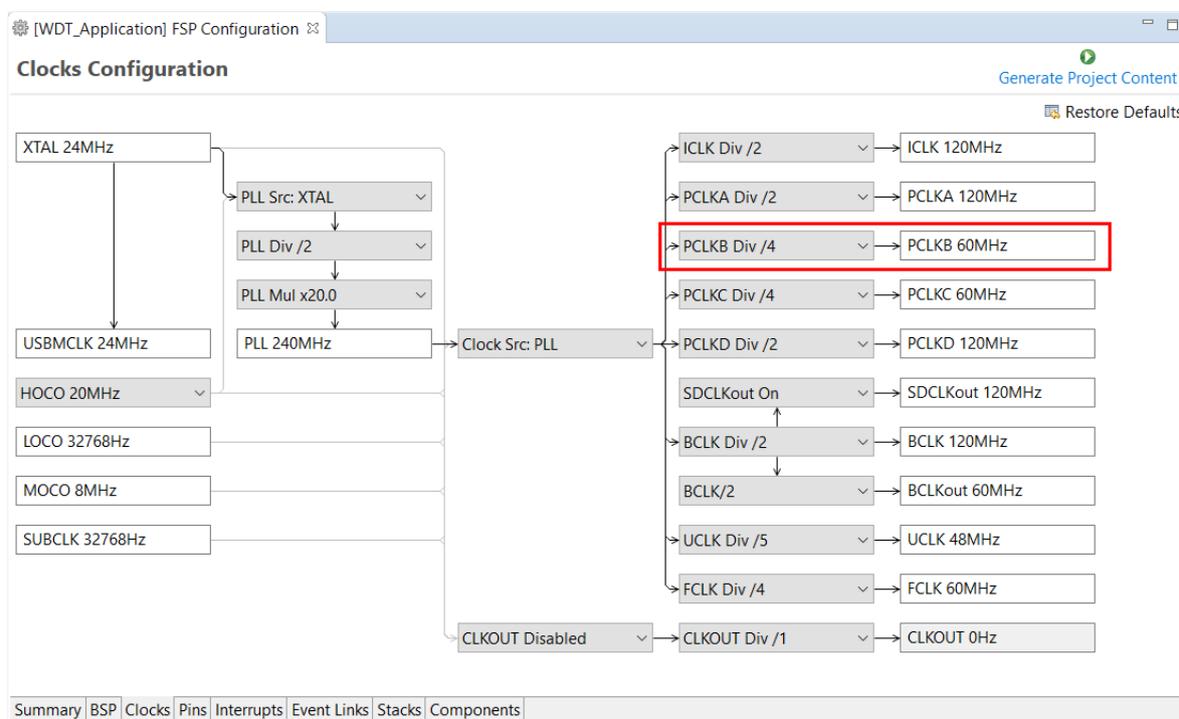


Figure 88: Clock configuration

### 2.4.4.3 Interrupts Tab

The **Interrupts** tab is used to add new user events or interrupts. No new interrupts or events are needed by the application, so no edits in this tab are required.

### 2.4.4.4 Event Links Tab

The **Event Links** tab is used to configure events used by the Event Link Controller (ELC). This project doesn't use the ELC, so no edits in this tab are required.

### 2.4.4.5 Pins Tab

The **Pins** tab provides a graphical tool for configuring the functionality of the pins of the device. For the WDT project no pin configuration is required. Although the project uses two LEDs connected to pins on the device, these pins are pre-configured as output GPIO pins by the BSP.

### 2.4.4.6 Stacks Tab

You can add any driver to the project using the **Stacks** tab. The HAL driver IO port pins are added automatically by e2 studio when the project is configured. The WDT application uses no RTOS Resources, so you only need to add the HAL WDT driver.

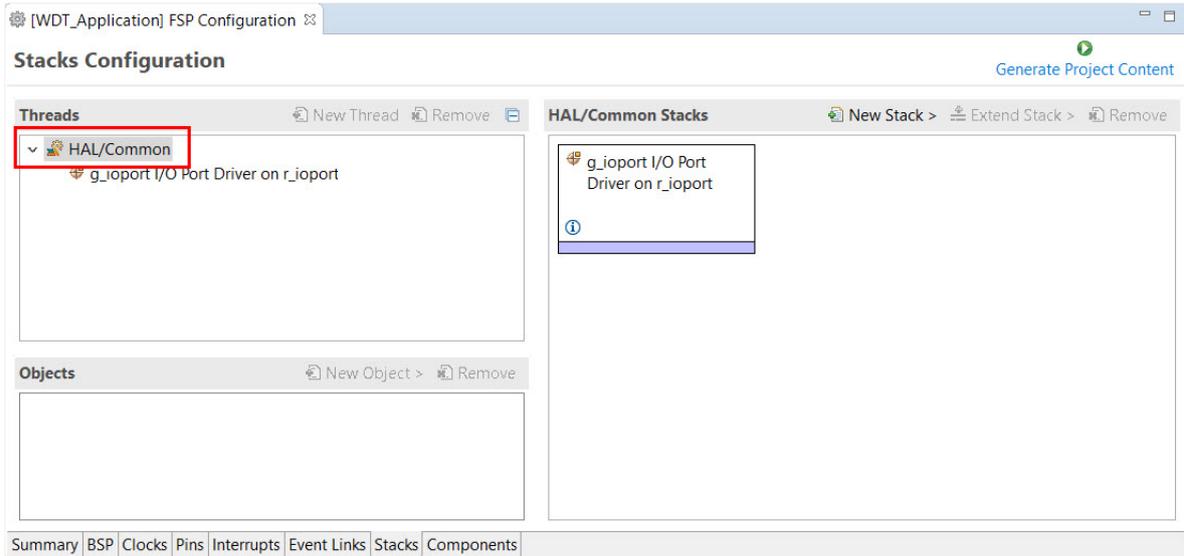


Figure 89: Stacks tab

1. Click on the **HAL/Common Panel** in the Threads Window as indicated in the figure above.

The Stacks Panel becomes a **HAL/Common Stacks** panel and is populated with the modules preselected by e2 studio.

2. Click on **New Stack** to find a pop-up window with the available HAL level drivers.
3. Select **WATCHDOG Driver on r\_wdt**.

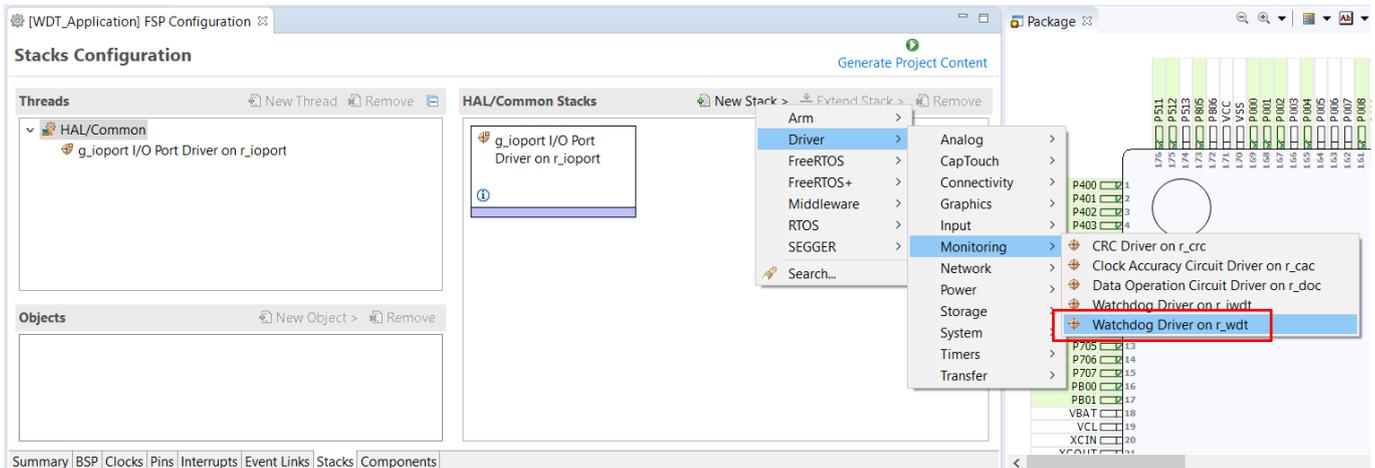
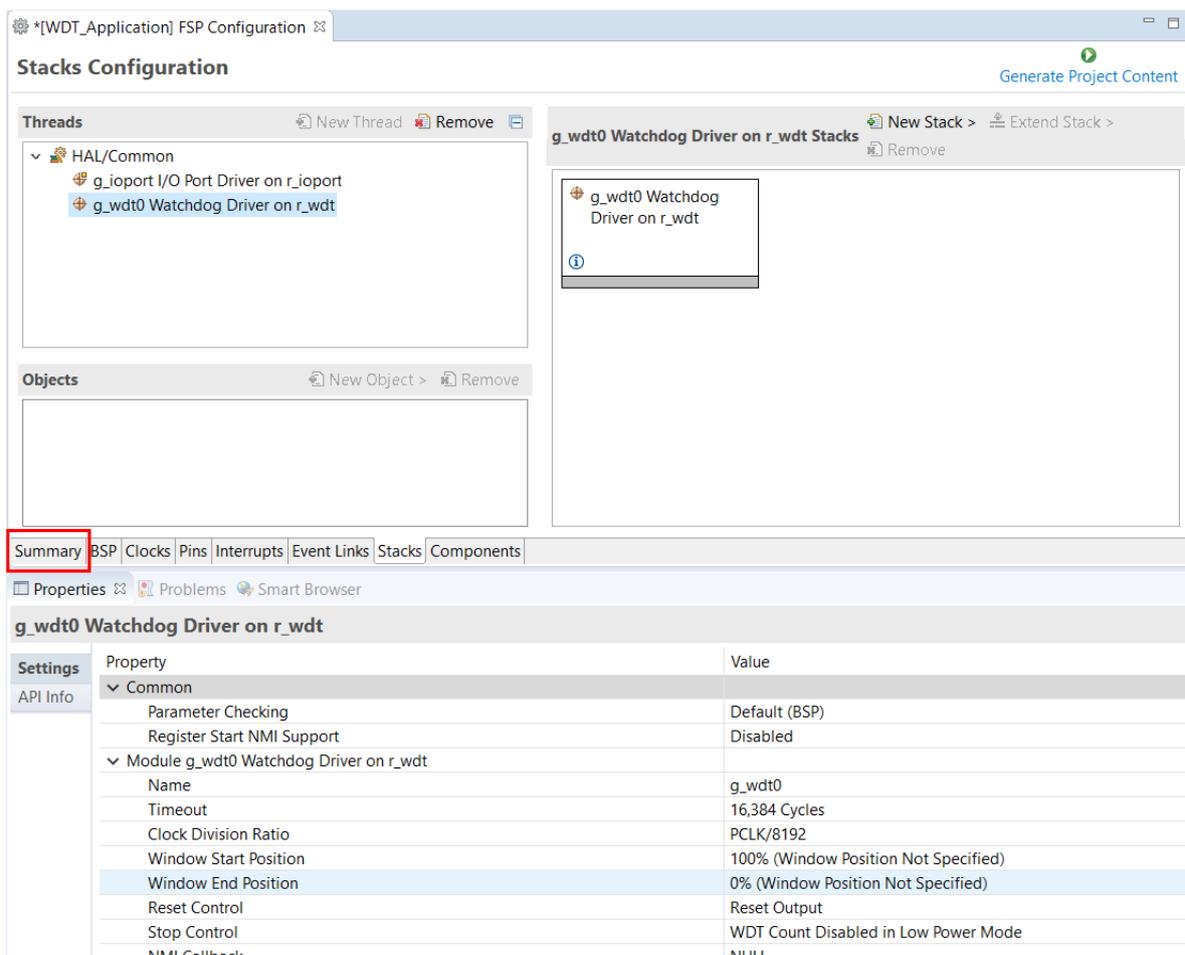


Figure 90: Module Selection

The selected HAL WDT driver is added to the **HAL/Common Stacks** Panel and the **Property** Window shows all configuration options for the selected module. The **Property** tab for the WDT should be visible at the bottom left of the screen. If it is not visible, check that the **FSP Configuration** perspective is selected.

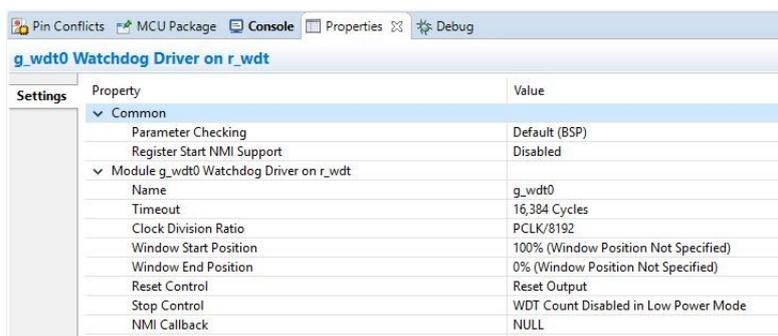


The screenshot shows the 'Stacks Configuration' window in the IDE. The 'Summary' tab is selected, displaying the properties for the 'g\_wdt0 Watchdog Driver on r\_wdt' module. The properties are listed in a table with columns for 'Property' and 'Value'.

Property	Value
Common	
Parameter Checking	Default (BSP)
Register Start NMI Support	Disabled
Module g_wdt0 Watchdog Driver on r_wdt	
Name	g_wdt0
Timeout	16,384 Cycles
Clock Division Ratio	PCLK/8192
Window Start Position	100% (Window Position Not Specified)
Window End Position	0% (Window Position Not Specified)
Reset Control	Reset Output
Stop Control	WDT Count Disabled in Low Power Mode
NMI Callback	NULL

Figure 91: Module Properties

All parameters can be left with their default values.



The screenshot shows the 'Properties' window in the IDE, specifically the 'Settings' tab for the 'g\_wdt0 Watchdog Driver on r\_wdt' module. The properties are listed in a table with columns for 'Property' and 'Value'.

Property	Value
Common	
Parameter Checking	Default (BSP)
Register Start NMI Support	Disabled
Module g_wdt0 Watchdog Driver on r_wdt	
Name	g_wdt0
Timeout	16,384 Cycles
Clock Division Ratio	PCLK/8192
Window Start Position	100% (Window Position Not Specified)
Window End Position	0% (Window Position Not Specified)
Reset Control	Reset Output
Stop Control	WDT Count Disabled in Low Power Mode
NMI Callback	NULL

Figure 92: g\_wdt WATCHDOG Driver on WDT properties

With PCLKB running at 60 MHz the WDT will reset the device 2.23 seconds after the last refresh.

$$\text{WDT clock} = 60 \text{ MHz} / 8192 = 7.32 \text{ kHz}$$

$$\text{Cycle time} = 1 / 7.324 \text{ kHz} = 136.53 \text{ us}$$

Timeout =  $136.53 \text{ us} \times 16384 = 2.23 \text{ seconds}$

Save the **Project Configuration** file and click the **Generate Project Content** button in the top right corner of the **Project Configuration** pane.

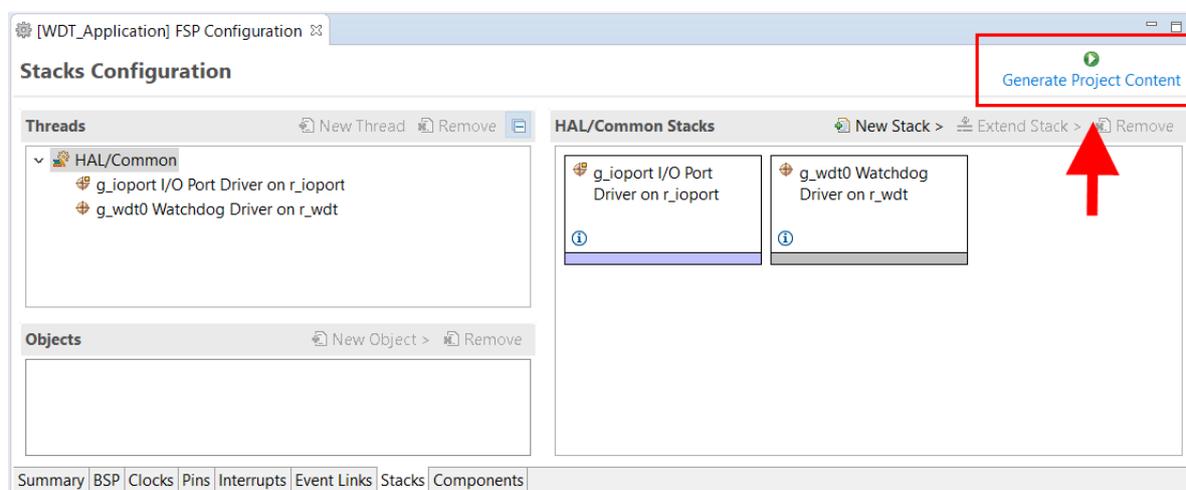


Figure 93: Generate Project Content button

e2 studio generates the project files.

#### 2.4.4.7 Components Tab

The components tab is included for reference to see which modules are included in the project. Modules are selected automatically in the Components view after they are added in the Stacks Tab.

For the WDT project ensure that the following modules are selected:

1. HAL\_Drivers -> r\_ioport
2. HAL\_Drivers -> r\_wdt

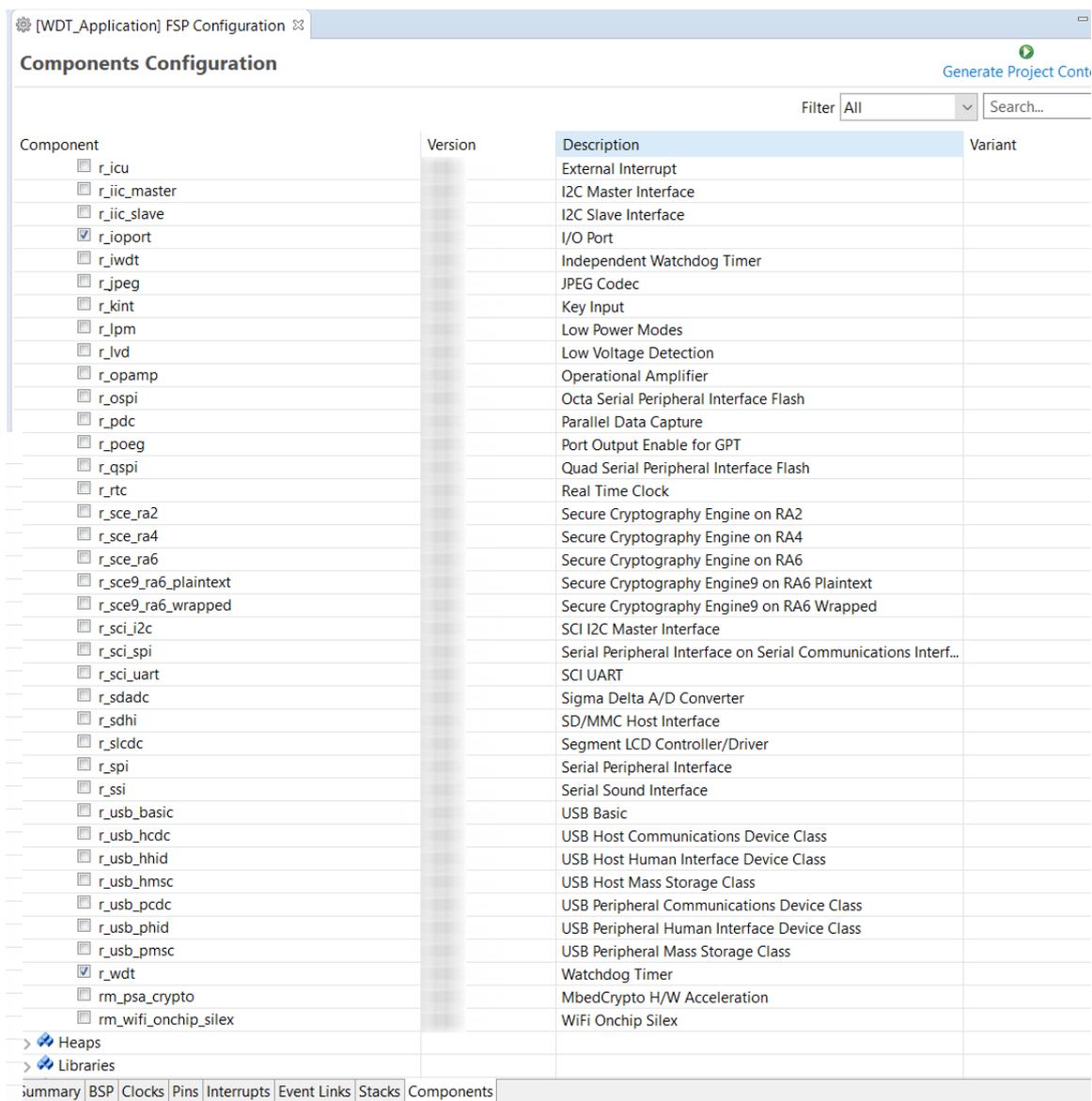


Figure 94: Component Selection

*Note*

The list of modules displayed in the Components tab depends on the installed FSP version.

## 2.4.5 WDT Generated Project Files

Clicking the Generate Project Content button performs the following tasks.

- r\_wdt folder and WDT driver contents created at:

ra/fsp/src

- r\_wdt\_api.h created in:

ra/fsp/inc/api

- r\_wdt.h created in:

ra/fsp/inc/instances

The above files are the standard files for the WDT HAL module. They contain no specific project contents. They are the driver files for the WDT. Further information on the contents of these files can be found in the documentation for the WDT HAL module.

Configuration information for the WDT HAL module in the WDT project is found in:

ra\_cfg/fsp\_cfg/r\_wdt\_cfg.h

The above file's contents are based upon the **Common** settings in the **g\_wdt WATCHDOG Driver on WDT Properties** pane.

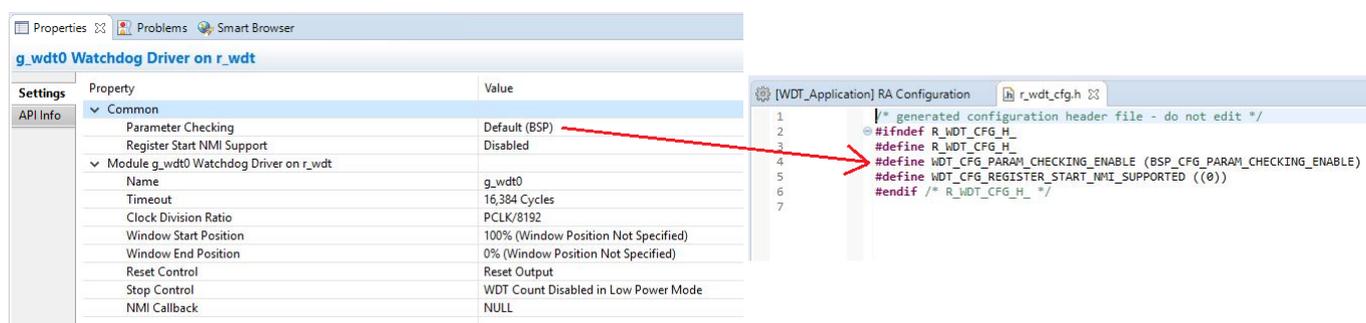


Figure 95: r\_wdt\_cfg.h contents

## Warning

Do not edit any of these files as they are recreated every time the Generate Project Content button is clicked and so any changes will be overwritten.

The r\_ioport folder is not created at ra/fsp/src as this module is required by the BSP and so already exists. It is included in the WDT project in order to include the correct header file in ra\_gen/hal\_data.c—see later in this document for further details. For the same reason the other IOPORT header files— ra/fsp/inc/api/r\_ioport\_api.handra/fsp/inc/instances/r\_ioport.h—are not created as they already exist.

In addition to generating the HAL driver files for the WDT and IOPORT files e2 studio also generates files containing configuration data for the WDT and a file where user code can safely be added. These files are shown below.

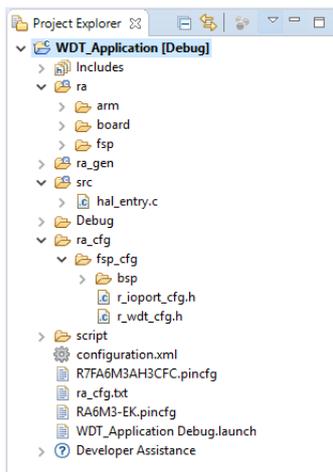


Figure 96: WDT project files

### 2.4.5.1 WDT hal\_data.h

The contents of hal\_data.h are shown below.

```
/* generated HAL header file - do not edit */
#ifndef HAL_DATA_H_
#define HAL_DATA_H_
#include <stdint.h>
#include "bsp_api.h"
#include "common_data.h"
#include "r_wdt.h"
#include "r_wdt_api.h"
#ifdef __cplusplus
extern "C"
{
#endif
extern const wdt_instance_t g_wdt0;
#ifdef NULL
void NULL(wdt_callback_args_t * p_args);
#endif
extern wdt_instance_ctrl_t g_wdt0_ctrl;
extern const wdt_cfg_t g_wdt0_cfg;
void hal_entry(void);
void g_hal_init(void);
```

```
#ifndef __cplusplus
} /* extern "C" */
#endif
#endif /* HAL_DATA_H_ */
```

hal\_data.h contains the header files required by the generated project. In addition this file includes external references to the **g\_wdt0** instance structure which contains pointers to the configuration, control, api structures used for WDT HAL driver.

#### Warning

This file is regenerated each time Generate Project Content is clicked and must not be edited.

#### 2.4.5.2 WDT hal\_data.c

The contents of hal\_data.c are shown below.

```
/* generated HAL source file - do not edit */
#include "hal_data.h"
wdt_instance_ctrl_t g_wdt0_ctrl;
const wdt_cfg_t g_wdt0_cfg =
{
    .timeout          = WDT_TIMEOUT_16384,
    .clock_division  = WDT_CLOCK_DIVISION_8192,
    .window_start    = WDT_WINDOW_START_100,
    .window_end      = WDT_WINDOW_END_0,
    .reset_control   = WDT_RESET_CONTROL_RESET,
    .stop_control    = WDT_STOP_CONTROL_ENABLE,
    .p_callback      = NULL,
};
/* Instance structure to use this module. */
const wdt_instance_t g_wdt0 =
{.p_ctrl = &g_wdt0_ctrl, .p_cfg = &g_wdt0_cfg, .p_api = &g_wdt_on_wdt};
void g_hal_init (void)
{
    g_common_init();
}
```

hal\_data.c contains g\_wdt0\_ctrl which is the control structure for this instance of the WDT HAL driver. This structure should not be initialized as this is done by the driver when it is opened.

The contents of g\_wdt0\_cfg are populated in this file using the **Watchdog Driver on g\_wdt0** pane in the Project Configuration **Stacks** tab. If the contents of this structure do not reflect the settings made in the IDE, ensure the **Project Configuration** settings are saved before clicking the **Generate Project Content** button.

#### Warning

This file is regenerated each time Generate Project Content is clicked and so should not be edited.

### 2.4.5.3 WDT main.c

Contains main() called by the BSP start-up code. main() calls hal\_entry() which contains user developed code (see next file). Here are the contents of main.c.

```
/* generated main source file - do not edit*/
#include "hal_data.h"

int main (void)
{
    hal_entry();
    return 0;
}
```

#### Warning

This file is regenerated each time Generate Project Content is clicked and so should not be edited.

### 2.4.5.4 WDT hal\_entry.c

This file contains the function hal\_entry() called from main(). User developed code should be placed in this file and function.

For the WDT project edit the contents of this file to contain the code below. This code implements the flowchart in overview section of this document.

```
#include "hal_data.h"
#include "bsp_pin_cfg.h"
#include "r_ioport.h"
#define RED_LED_NO_OF_FLASHES 30
#define RED_LED_PIN BSP_IO_PORT_01_PIN_00
#define GREEN_LED_PIN BSP_IO_PORT_04_PIN_00
#define RED_LED_DELAY_MS 125
```

```
#define GREEN_LED_DELAY_MS 250
volatile uint32_t delay_counter;
volatile uint16_t loop_counter;
void R_BSP_WarmStart(bsp_warm_start_event_t event);
/*****
*****/
void hal_entry (void)
{
    /* Allow the WDT to run when the debugger is connected */
    R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;

    /* Open the WDT */
    R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Start the WDT by refreshing it */
    R_WDT_Refresh(&g_wdt0_ctrl);

    /* Flash the red LED and feed the WDT for a few seconds */
    for (loop_counter = 0; loop_counter < RED_LED_NO_OF_FLASHES; loop_counter++)
    {
        /* Turn red LED on */
        R_IOPORT_PinWrite(&g_ioport_ctrl, RED_LED_PIN, BSP_IO_LEVEL_LOW);

        /* Delay */
        R_BSP_SoftwareDelay(RED_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);

        /* Refresh WDT */
        R_WDT_Refresh(&g_wdt0_ctrl);

        R_IOPORT_PinWrite(&g_ioport_ctrl, RED_LED_PIN, BSP_IO_LEVEL_HIGH);

        /* Delay */
        R_BSP_SoftwareDelay(RED_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);

        /* Refresh WDT */
        R_WDT_Refresh(&g_wdt0_ctrl);
    }

    /* Flash green LED but STOP feeding the WDT. WDT should reset the
    * device */
    while (1)
    {
        /* Turn green LED on */
```

```
R_IOPORT_PinWrite(&g_ioport_ctrl, GREEN_LED_PIN, BSP_IO_LEVEL_LOW);
/* Delay */
R_BSP_SoftwareDelay(GREEN_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);
/* Turn green off */
R_IOPORT_PinWrite(&g_ioport_ctrl, GREEN_LED_PIN, BSP_IO_LEVEL_HIGH);
/* Delay */
R_BSP_SoftwareDelay(GREEN_LED_DELAY_MS, BSP_DELAY_UNITS_MILLISECONDS);
}
}
/*****
*****/
void R_BSP_WarmStart (bsp_warm_start_event_t event)
{
    if (BSP_WARM_START_RESET == event)
    {
#if BSP_FEATURE_FLASH_LP_VERSION != 0
        /* Enable reading from data flash. */
        R_FACI_LP->DFLCTL = 1U;

        /* Would normally have to wait for tDSTOP(6us) for data flash recovery. Placing the
        enable here, before clock and
        * C runtime initialization, should negate the need for a delay since the
        initialization will typically take more than 6us. */
#endif
    }

    if (BSP_WARM_START_POST_C == event)
    {
        /* C runtime environment and system clocks are setup. */
        /* Configure pins. */
        R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
    }
}
```

The WDT HAL driver API functions are defined in `r_wdt.h`. The WDT HAL driver is opened through the open API call using the instance structure defined in `r_wdt_api.h`:

```
/* Open the WDT */  
R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);
```

The first passed parameter is the pointer to the control structure `g_wdt0_ctrl` instantiated in `hal_data.c`. The second parameter is the pointer to the configuration data `g_wdto_cfg` instantiated in the same `hal_data.c` file.

The WDT is started and refreshed through the API call:

```
/* Start the WDT by refreshing it */  
R_WDT_Refresh(&g_wdt0_ctrl);
```

Again the first (and only in this case) parameter passed to this API is the pointer to the control structure of this instance of the driver.

## 2.4.6 Building and Testing the Project

Build the project in e2 studio by clicking **Build > Build Project** or by clicking the build icon. The project should build without errors.

To debug the project

1. Connect the USB cable between the target board debug port and host PC.
2. In the **Project Explorer** pane on the left side of e2 studio, right-click on the WDT project **WDT\_Application** and select **Debug As > Debug Configurations**.
3. Under **Renesas GDB Hardware Debugging** select **WDT\_Application Debug** as shown below.

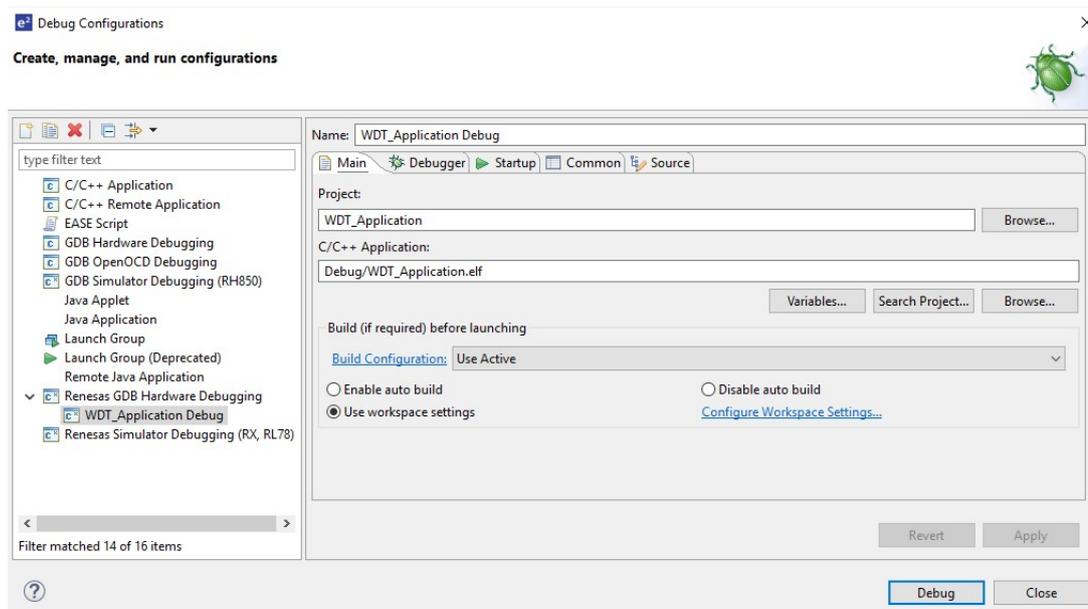
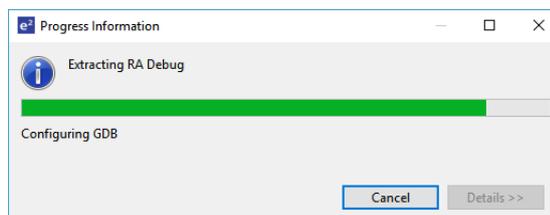


Figure 97: Debug configuration

- Click the **Debug** button. Click Yes to the debug perspective if asked.



- The code should run the `Reset_Handler()` function.
- Resume execution via **Run > Resume**. Execution will stop in `main()` at the call to `hal_entry()`.
- Resume execution again.

The red LED should start flashing. After 30 flashes the green LED will start flashing and the red LED will stop flashing.

While the green LED is flashing the WDT will underflow and reset the device resulting in the red LED to flash again as the sequence repeats.

- Stop the debugger in e2 studio via **Run > Terminate**.
- Click the reset button on the target board. The LEDs begin flashing.

## 2.5 Primer: ARM® TrustZone® Project Development

This section will introduce the user to the tools supporting ARM® TrustZone® configuration for the RA Family of microcontrollers. It is intended to be read by development engineers implementing RA ARM® TrustZone® projects for the first time. It will introduce basic concepts followed by workflow

and tooling functions designed to simplify and accelerate their first ARM® TrustZone® development. A background knowledge of e<sup>2</sup> studio and RA device hardware is expected.

## Target Device

RA Cortex®-M33 or Cortex®-M23 devices with ARM® TrustZone® security extension.

### 2.5.1 Renesas Implementation of ARM® TrustZone® Technology

For brevity, ARM® TrustZone® will be abbreviated to TZ in this document.

The following section is supplied for reference only. For full details of TZ implementation, refer to Arm documentation (<https://developer.arm.com/ip-products/security-ip/trustzone>) and the RA6M4 device manual.

Arm TZ technology divides the MCU and therefore the application into Secure and Non-Secure partitions. Secure applications can access both Secure and Non-Secure memory and resources. Non-Secure code can access Non-Secure memory and resources as well as Secure resources through a set of so-called veneers located in the Non-Secure Callable (NSC) region. This ensures a single access point for Secure code when called from the Non-Secure partition. The MCU starts up in the Secure partition by default. The security state of the CPU can be either Secure or Non-Secure.

The MCU code flash, data flash, and SRAM are divided into Secure (S) and Non-Secure (NS) regions. Code flash and SRAM include a further region known as Non-Secure Callable (NSC). These memory security attributes are set into the non-volatile memory via SCI or USB boot mode commands when the device lifecycle is Secure Software Debug (SSD) state. The memory security attributes are loaded into the Implementation Defined Attribution Unit (IDAU) peripheral and the memory controller before application execution and cannot be updated by application code.

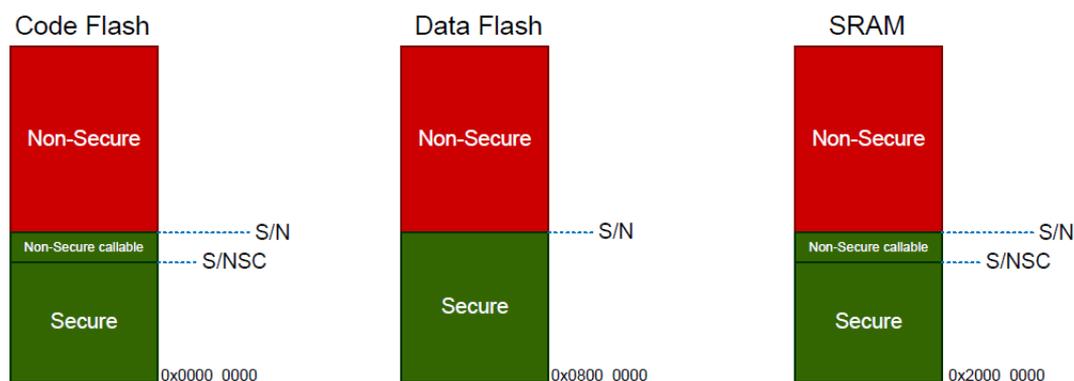


Figure 98: Secure and Non-Secure Regions

Note: All external memory accesses are considered to be Non-Secure.

Code Flash and SRAM can be divided into Secure, Non-Secure, and Non-Secure Callable. All secure memory accesses from the Non-Secure region MUST go through the Non-Secure Callable gateway and target a specific Secure Gateway (SG) assembler instruction. This forces access to Secure APIs at a fixed location and prevents calls to sub-functions and so on. Failing to target an SG instruction will generate a TZ exception.

TZ enabled compilers will manage generation of the NSC veneer automatically using CMSE extensions.

### 2.5.1.1 Calling from Non-Secure to Secure

A new instruction SG (Secure Gateway) has been added to the Armv8-M architecture. This MUST be the destination instruction for any branch within the Non-Secure Callable region. If an attempt is made to branch to any other instruction from the Non-Secure partition, a TZ exception will be thrown.

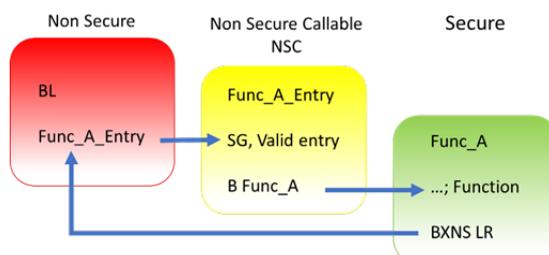


Figure 99: Calling from Non-Secure to Secure Functions

### 2.5.1.2 Calling from Secure to Non-Secure

Secure code uses B(L)XNS instructions to make direct calls to Non-Secure functions. While this is certainly possible, it can create a security vulnerability in the application. It is also challenging for the Secure application to determine the address of the non-secure function during build phase. From the RA Tools and FSP point view, calling directly from Secure to Non-Secure via FSP API is not supported.

Preference is for the Secure code to initialise as necessary from reset, then pass control to the Non-Secure partition. It will manage any data transfers and so forth via FSP call-backs as security checks. For example, secure data can be copied to Non-Secure RAM.

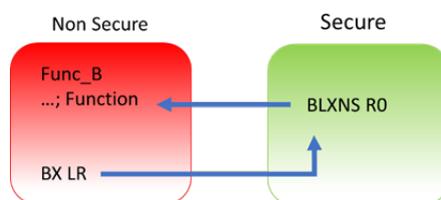


Figure 100: Calling from Secure to Non-Secure Functions

## 2.5.2 Workflow

ARM® TrustZone® MCU development normally consists of two projects within a workspace, Secure and Non-Secure. General project workflows are described in the following sections. The Renesas project generator also supports development with "Flat project" model with no ARM® TrustZone® awareness.

### 2.5.2.1 Secure Project

1. Start a new Secure project in e<sup>2</sup> studio.
2. Select and configure pins and drivers/stacks that need to be initialized and used in Secure

- mode. This should be kept to a minimum to reduce the security attack surface.
3. Expose top of stacks as Non-Secure Callable (NSC) **if** they need to be accessed from Non-Secure partition. Again, this should be kept to a minimum.
  4. Generate project content and write Secure code such as key handling and opening drives as needed.
  5. Modify/remove any unnecessary "Guard" functions as needed to control access via NSC.
  6. Build project.
  7. A Non-Secure project will be needed before debugging. If necessary, prepare a "dummy" Non-Secure project or replace `R_BSP_NonSecureEnter();` with `while(1);` in `hal_entry.c`.

### 2.5.2.2 Non-Secure Project

1. Start a new Non-Secure project.
2. If you have access to the Secure project, choose this option. However, if you only have access to a device with pre-programmed Secure code (commonly referred to as provisioned device) choose "Secure Bundle".
3. Select and configure pins and drivers/stacks that need to be initialized and used in Non-Secure mode.
4. Note that you can add NSC drivers and stacks as needed.
5. Generate project content and write Non-Secure code as needed
6. Access NSC drivers and Stacks via Guard functions.
7. Build and debug project.

### 2.5.2.3 Flat Project

A flat project does not technically use ARM® TrustZone® as the developer has made a decision to place the entire application in Secure partition from restart.

Notes:

- Any code placed in external memory (such as OSPI or QSPI) will be Non-Secure.
- The Ethernet EDMAC is designed to be a Non-Secure bus master so associated Ethernet RAM buffers will be placed in Non-Secure RAM. The tooling will automatically manage this.

The workflow is as follows:

1. Start a new Flat project.
2. Select and configure pins and drivers/stacks as needed.
3. Generate project content and write code as needed.
4. Build and debug project.

## 2.5.3 RA Project Generator (PG)

The RA project generators have been created to help users through setting up new TZ enabled projects. User will be prompted for project settings such as Project Type (Secure, Non-Secure, or Flat), compiler, RTOS and debugger. Care is needed when setting up a TZ project to ensure that the connection between Secure and Non-Secure partitions are managed correctly.

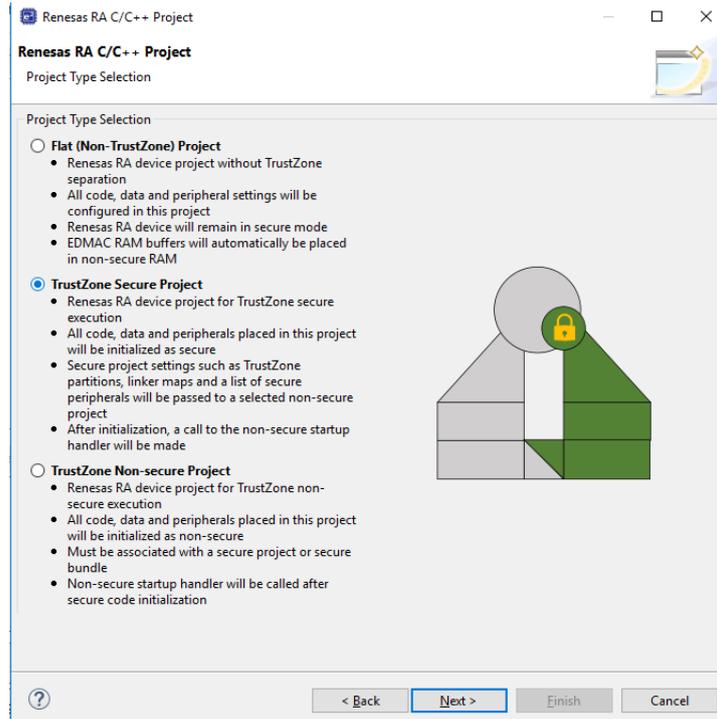


Figure 101: Secure Project (following Arm notation as green)

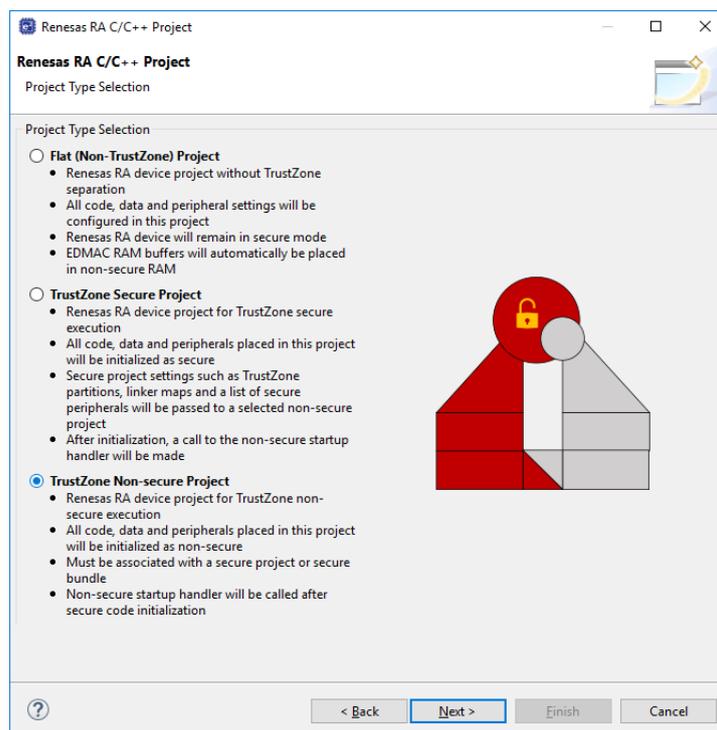


Figure 102: Non-Secure Project (following Arm notation as red)

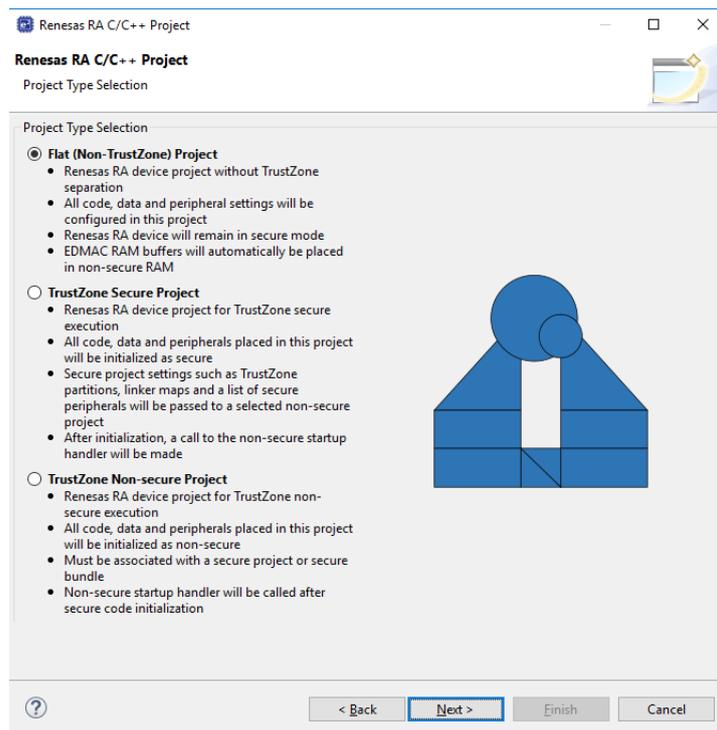


Figure 103: Flat Project

### 2.5.3.1 Secure Project Set Up

All code, data, and peripherals in this project will be configured as Secure using the device Peripheral Security Attribution (PSA) registers. Although it is very application specific, we recommend keeping the Secure project code as small as possible to reduce the attack surface. For example, secure key handling may be the only application code in the secure project.

Necessary values to set up the TZ memory partition (IDAU registers) will be automatically calculated after the project is built to ensure they match the code and data size, keeping the attack surface as small as possible.

Typically, ANSI C start up code (clearing of RAM, variable initialisation, etc) , clock, and secure peripheral initialisation will occur in this project.

At the end of the Secure code, a call will be made to `R_BSP_NonSecureEnter()`; to pass control to the Non-Secure partition.

Non-Secure Callable (NSC) "Guard" functions are added to the project and expose selected modules to Non-Secure projects. User can add application-specific access checks as needed in these functions.

Output of this project type will be an elf file that must be either pre-programmed (provisioned) into a device or referenced by a Non-Secure project (via Secure bundle \*.SBD) to build a final image.

This project type will NOT typically be debugged in isolation and will normally require a Non-Secure project such as a call to a `R_BSP_NonSecureEnter()` to be made. This can be replaced with `while(1);` if needed.

### 2.5.3.2 RTOS Support in TZ Project

Although the RTOS kernel and user tasks will reside in the Non-Secure partition, the Secure partition needs to allocate stack space and so on. It is essential when starting a new RTOS project that the TrustZone Secure RTOS-Minimal template is selected. This will add the Arm TrustZone Context RA Port as below.

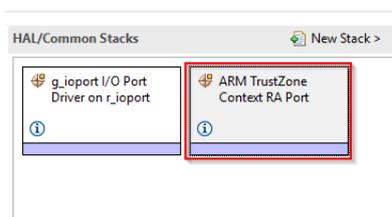
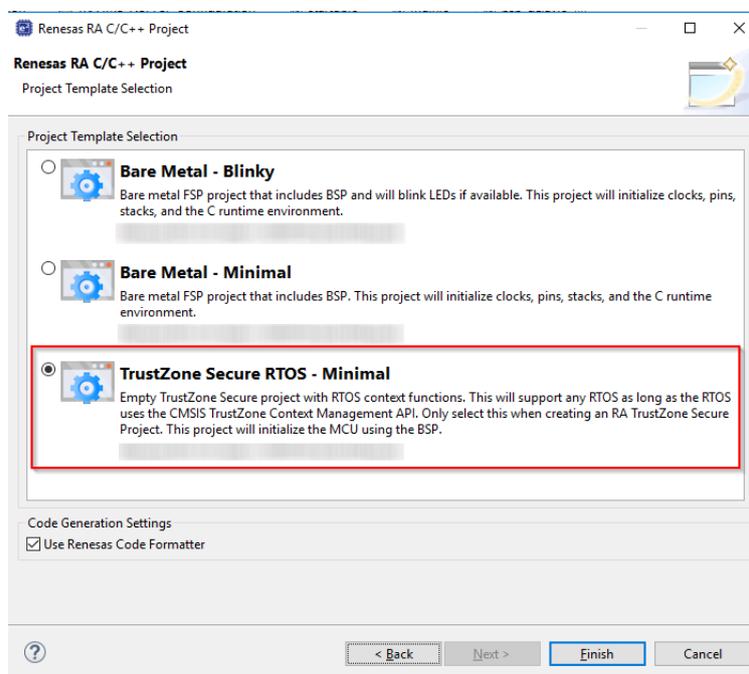


Figure 104: Secure RTOS-Minimal Template

### 2.5.3.3 Peripheral Security Attribution

Each peripheral can be configured to be Secure or Non-Secure. Peripherals are divided into two types.

Type-1 peripherals have one security attribute. Access to all registers is controlled by one security attribute. The Type-1 peripheral security attribute is set in the PSARx (x = B to E) register by the secure application.

Type-2 peripherals have the security attribute for each register or for each bit. Access to each register or bit field is controlled according to these security attributes. The Type-2 peripheral security attribute is set in the Security Attribution register in each module by the Secure application. For more information about the Security Attribution register, see sections in the Appropriate MCU's User's Manual for each peripheral.

Table 1. Secure and Non-Secure Peripherals

Type	Peripheral
Type 1	SCI, SPI, USBFS, CAN, IIC, SCE9, DOC, SDHI, SSIE, CTSU, CRC, CAC, TSN, ADC12, DAC12, POEG, AGT, GPT, RTC, IWDT, WDT
Type 2	System control (Resets, LVD, Clock Generation Circuit, Low Power Modes, Battery Backup Function), FLASH CACHE, SRAM controller, CPU CACHE, DMAC, DTC, ICU, MPU, BUS, Security setting, ELC, I/O ports
Always Non-Secure	CS Area Controller, QSPI, OSPI, ETHERC, EDMAC

FSP will initialise the arbitration registers during Secure project BSP start up. User code may also be written to set or clear further arbitration. However care must be taken not to undermine FSP.

#### 2.5.3.4 Non-Secure

All code, data, and peripherals in this project will be configured as Non-Secure. This project type must be associated with a Secure project to enable access to secure code, peripherals, linker scripts and others.

#### 2.5.3.5 Flat Project Type

All code, data, and peripherals are configured in a Secure single partition except for the EDMAC RAM buffers that will remain in the Non-Secure partition. Effectively, TZ is disabled.

#### 2.5.3.6 Secure Connection to Non-Secure Project

When starting a new Non-Secure Project, the user will be prompted for either a Secure Project or Secure Bundle. In each case, details of the linker settings, Non-Secure Callable functions, and Secure peripherals will be read to enable the Non-Secure project setup.

Should the Secure project or bundle be rebuilt, the Non-Secure editor will detect this and prompt user to regenerate the Non-Secure project configuration.

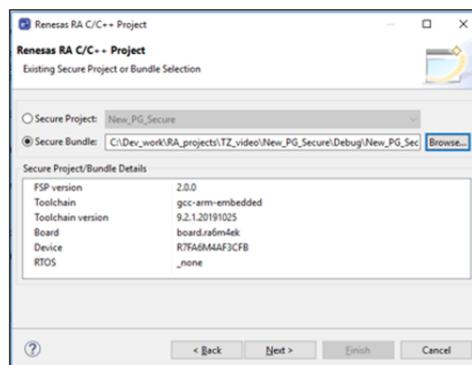


Figure 105: Secure Project or Bundle Selection

### Secure Project (Combined)

A Secure project must reside in the same Workspace as the Non-Secure project and will typically be used when a design engineer has access to both the Secure and Non-Secure project sources. This is sometimes known as "Combined model".

A Secure .elf file will be referenced and included in the debug configuration for download to the target device. The development engineer will have visibility of Secure and Non-Secure project source code and configuration.

### **Secure Bundle (Split)**

A Secure Bundle will ONLY include linker memory ranges, symbol references, and details of locked Secure peripheral configuration settings but no access to Secure source code (API header files will be included as necessary).

The Secure bundle file (\*.SBD) must be supplied to the Non-Secure developer by the Secure project developer.

The development engineer will typically not have access to the Secure project or .elf file which MUST be pre-programmed or provisioned into the target MCU.

The DLM state of target device should then be switched to NSECSD (see section 6.2) before the device is provided to the non-secure developer.

This is often referred to as "Split model" where a basic security set up is developed by a Secure team and then passed to the Non-Secure team in the same facility or at a third party. The Non-Secure team has no access to the Secure source code and cannot directly access Secure peripherals, data, or APIs.

### **2.5.3.7 Debug Configurations**

After each project type has been selected, a suitable debug configuration will be generated.

#### **Non-Secure with Secure Project (Combined)**

Both Secure and Non-Secure .elf files will be downloaded.

A debug configuration called <project name>\_SSD will be generated.

#### **Non-Secure with Secure Bundle (Split)**

Only a Non-Secure elf will be downloaded. This configuration must be used with a pre-provisioned device (Secure project pre-programmed into MCU Flash).

A debug configuration called <project name>\_NSECSD will be generated.

#### **Flat Debug**

A single .elf file will be downloaded.

A debug configuration called <project name>\_FLAT will be generated.

### **2.5.4 Secure Projects**

As mentioned, Secure code will be called immediately after device reset and run ANSI C start up, clock, interrupt vector table, and secure peripheral initialization before starting user code. All

selected peripheral configuration settings will be automatically initialised as Secure.

### 2.5.4.1 Secure Clock

Device clock settings are the possible exception in that they will be initialised in the Secure project (to enable faster start up from reset) but can be set as Secure or Non-Secure as user application may need to change settings during execution (for low-power mode and so on). The Secure and Non-Secure FSP BSPs can both change the clock settings.

However, clock settings can be locked as Secure should the developer choose to do so.

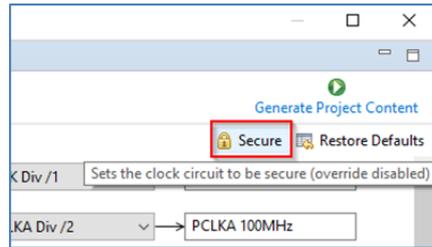


Figure 106: Secure Clock Setting

### 2.5.4.2 Setting Drivers as NSC

Some driver and middleware stacks in the Secure project may need to be accessed by the Non-Secure partition. To enable generation of NSC veneers, set "Non-Secure Callable" from the right-click context menu for the selected modules in the Configurator.

Note: It is only possible to "expose" top of stacks as NSC.

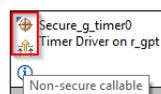
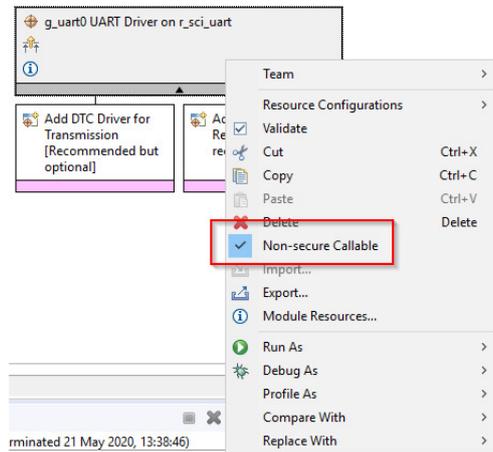


Figure 107: Generate NSC Veneers

The top of the stack will be marked with a new icon and tool tip to signify NSC access.

### 2.5.4.3 Guard Functions

Access to NSC drivers from a Non-Secure project is possible through the Guard APIs. FSP will automatically generate Guard functions for all the top of stack/driver APIs added to the project as Non-Secure Callable.

User can choose to add further levels of access control or delete guard function if they wish to only expose a limited range of APIs to a Non-Secure developer.

```
BSP_CMSE_NONSECURE_ENTRY fsp_err_t g_uart0_open_guard(  
    uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg) {  
    /* TODO: add your own security checks here */  
    FSP_PARAMETER_NOT_USED(p_api_ctrl);  
    FSP_PARAMETER_NOT_USED(p_cfg);  
    return R_SCI_UART_Open(&g_uart0_ctrl, &g_uart0_cfg);  
}
```

For example, an SCI channel may be opened and configured for a desired baud rate by the Secure developer, but only enable the Write API to the Non-Secure developer. In which case, all but `g_uart0_write_guard()` could be deleted. CTRL structures are not required as they will be added on the Secure side.

For example, the call from the Non-Secure partition would be as follows:

```
err = g_uart0_open_guard(0,0);
```

## 2.5.5 Non-Secure projects

Configuration of the project can continue as for other RA devices, but certain resources will be locked if they have been previously set up as Secure.

The Non-Secure project will be called from the Secure project via `R_BSP_NonSecureEnter()`;

### 2.5.5.1 Clock Set Up

You may recall that clocks can be set as Secure or Non-Secure. If they are set as Secure, settings will only be available to view, and user will not be able to change them. The Override button will be greyed. This is useful to preserve CGC sync with secure project by not overriding unless necessary. If it is NOT set as Secure, user can choose to override the initial Secure settings

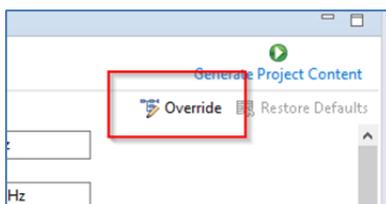


Figure 108: Clock Setting as Non-Secure

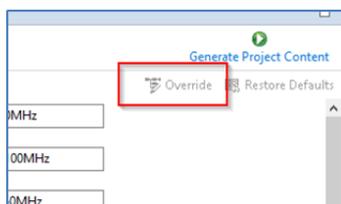


Figure 109: Clock Setting as Secure

### 2.5.5.2 Selecting NSC Drivers

Drivers declared as NSC in a Secure project can be selected and added to Non-Secure project and will be decorated as before.

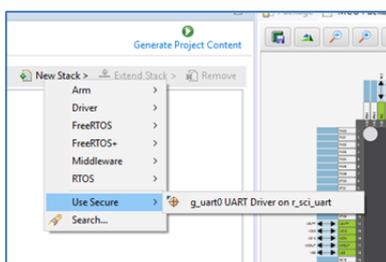
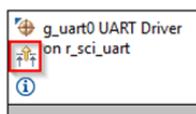


Figure 110: Selecting NSC Drivers

### 2.5.5.3 Locked Resources

When a NSC Secure driver is added to a Non-Secure project, the configuration settings are locked and are available for information only. A padlock is added for indication.

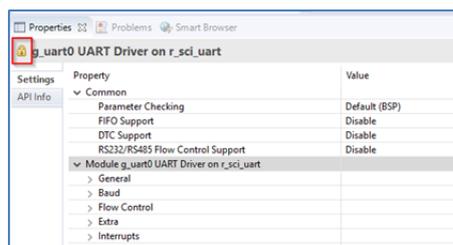


Figure 111: Locked Resources

#### 2.5.5.4 Locked Channels

In a peripheral with multiple channels, for example, DMA, if a Non-Secure developer tries to select a channel that has already been defined as Secure, the following error message type will be displayed.

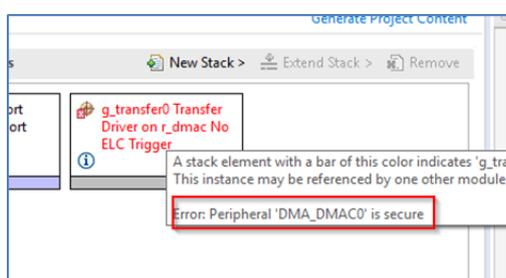


Figure 112: Error Message when Selecting a Secure Channel

### 2.5.6 IDAU registers

Renesas RA TZ-enabled devices include a set of registers known as Implementation Defined Attribution Unit (IDAU) that are used to set up partitions between Secure, Non-Secure Callable, and Non-Secure regions. The IDAU registers can only be programmed during MCU **boot mode** and NOT through the debug interfaces. Because of this, special debugger firmware has been developed to manage bringing the device up in SCI boot mode to set up the IDAU registers (automatically drives MD pin) and then switch back to debug mode as needed.

**Note:** Please be aware of the extra signal connection (MD pin) needed on the debug interface connector. The Renesas Evaluation Kit (EK) for your selected device is a good reference.

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK Wired OR with MD	P300/TCK Wired OR with MD	P201/MD
6	P109/SWO/TXD9	P109/TDO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TRACECLK	P214/TRACECLK	NC
14	P211/TRACEDATA[0]	P211/TRACEDATA[0]	NC
16	P210/TRACEDATA[1]	P210/TRACEDATA[1]	NC
18	P209/TRACEDATA[2]	P209/TRACEDATA[2]	NC
20	P208/TRACEDATA[3]	P208/TRACEDATA[3]	NC
3, 5, 15,17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

The e<sup>2</sup> studio build phase automatically extracts the IDAU partition register settings from the Secure.elf file and programs them into the device during debug connection, which can be observed in the console.

This is an important phase of TZ development as the Secure partitions should be set as small as possible to ensure that the security attack surface is as small as possible.

However, should the developer wish to make these partitions larger to accommodate, for example during field firmware updates, const or data arrays should be placed in the Secure project as needed.

```

Console Problems Debugger Console Smart Browser
New_PC_Non_Secure_Debug_SSD [Renesas GDB Hardware Debugging]

Starting server with the following options:
  Raw options          : C:\Users\b3800280\...

Connecting to E2, ARM target
  GDBServer endian    : little
  Target power        : on
Starting target connection

Current status of the RA TrustZone device
  DLM state           : SSD
  Debug level         : 2
  IDAU memory regions :
  - Code Flash Secure size (kB) : 8
  - Code Flash NSC size (kB)   : 24
  - Data Flash Secure size (kB) : 0
  - SRAM Secure size (kB)      : 2
  - SRAM NSC size (kB)         : 6
  
```

Figure 113: RA TrustZone Device Current Status

It is also possible to manually set up the partition registers through the Renesas Device Partition Manager.

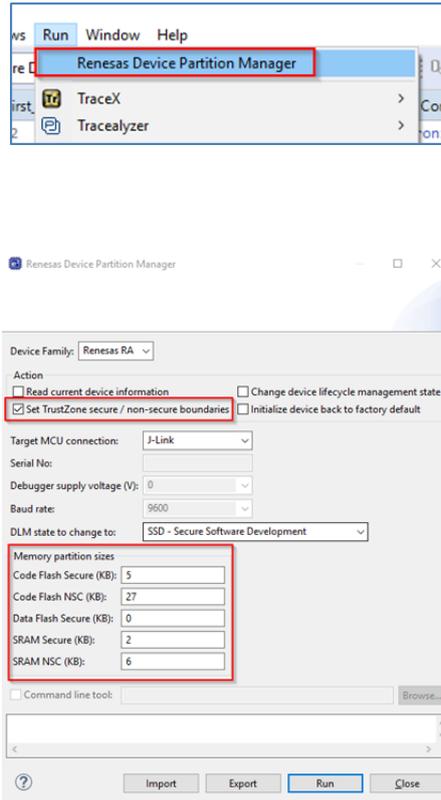


Figure 114: Renesas Device Partition Manager

### 2.5.6.1 SCI Boot Mode

Example of MD mode pin connection to debugger connector (from EK schematic).

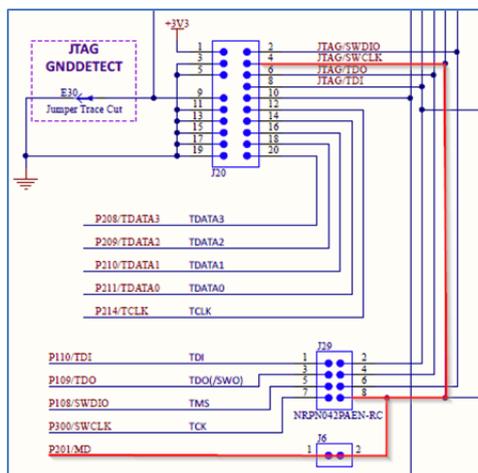


Figure 115: Example of MD Mode Pin Connection to Debugger Connector (from EK schematic)

### 2.5.6.2 DLM States

Device lifecycle defines the current phase of the device and controls the capabilities of the debug interface, the serial programming interface and Renesas test mode. The following illustration shows the lifecycle definitions and capability in each lifecycle.

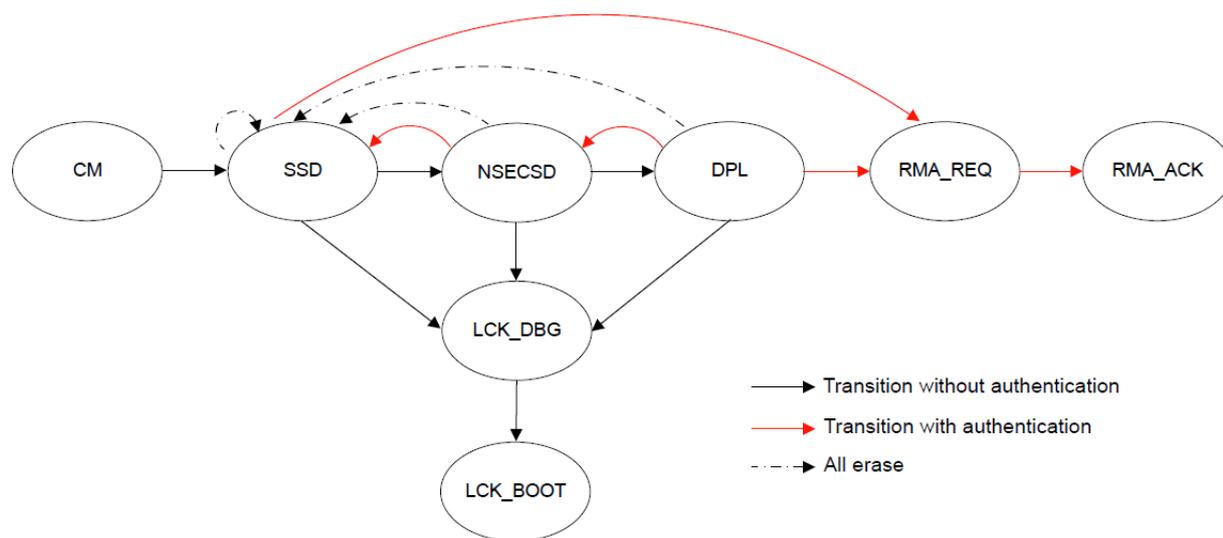


Figure 116: Lifecycle Stages

Note: All authentication key exchange and transitioning to LCK\_DBG, LCK\_BOOT, RMA\_REQ is only managed by Renesas Flash Programmer (RFP) and NOT within e<sup>2</sup> studio.

Lifecycle	Definition	Debug level	Serial programming	Test mode
CM	“Chip Manufacturing” The state when the customer received the device.	DBG2	Available, cannot access code/data flash	Not available
SSD	“Secure Software Development” The secure part of application is being developed.	DBG2	Available can program/erase/read all code/data flash area	Not available
NSECSD	“Non-SECure Software Development” The non-secure part of application is being developed.	DBG1	Available can program/erase/read all code/data flash area	Not available
DPL	“DePloyed” The device is in-field.	DBG0	Available cannot access code/data flash area	Not available
LCK_DBG	“LoCKed DeBuG” The debug interface is permanently disabled.	DBG0	Available cannot access code/data flash area	Not available
LCK_BOOT	“LoCKed BOOT interface” The debug interface and the serial programming interface are permanently disabled.	DBG0	Not available	Not available
RMA_REQ	“Return Material Authorization REQuest” Request for RMA. The customer must send the device to Renesas in this state.	DBG0	Available cannot access code/data flash area	Not available
RMA_ACK	“Return Material Authorization ACKnowledged” Failure analysis in Renesas	DBG2	Available cannot access code/data flash area	Available

Figure 117: Lifecycle Stages and Debug Levels

There are three debug access levels. The debug access level changes according to the lifecycle state.

- DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals

- DBG1: The debugger connection is allowed, and restricted to access only Non-Secure memory regions and peripherals
- DBG0: The debugger connection is not allowed

Transitions for one state to another can be performed using the Renesas Flash Programmer (RFP, see section below) or using the Renesas Device Partition Manager (limited number of states possible). It is possible to secure transitions between states using authentication keys. For more information on DLM states and transitions (device specific), please refer to device user manual.

### 2.5.7 Debug

By default, the device will be in SSD mode and so allow access to Secure and Non-Secure partitions. In this mode both Secure and Non-Secure .elf files will be downloaded.

The current debugger status is displayed in the lower left corner and includes the DLM state (SSD or NSECSD) and current partition (Secure, Non-Secure, or Non-Secure Callable) when the debugger is stopped, for example.



Figure 118: Current Debugger Status

#### 2.5.7.1 Non-Secure Debug

Once the device is transitioned to NSECSD mode, only Non-Secure Flash, RAM and Peripherals can be accessed. In this mode, a Secure .elf must be pre-programmed (provisioned) into the device, and only a Non-Secure .elf file will be downloaded.

When in NSECSD mode access to Secure elements will be blocked and data displayed as ????????.

In NSECSD mode, it is not possible to set breakpoints on Secure code or data.

It is not possible to step into Secure code; the debugger will perform a step-over of any Secure function calls. Should the user press the Suspend button during execution, the debugger will stop at the next Non-Secure code access.

Assuming Secure memory region finishes at 32K (0x8000) in NSECSD debug mode (colour coding added for indication only), memory will be displayed as shown in the following figure.

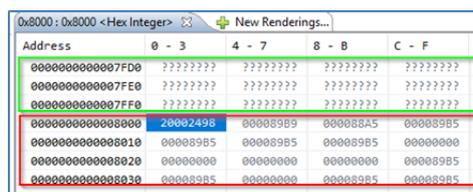


Figure 119: Memory Display in NSECSD Debug Mode

Disassembly will be displayed as shown in the following figure.

```

Disassembly 0x8000
Cannot access memory at address 0x7ffc
00007ffd: Failed to execute MI command:
-data-disassemble -s 32765 -e 32797 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffc
00007ffe: Failed to execute MI command:
-data-disassemble -s 32766 -e 32798 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffe
00007fff: Failed to execute MI command:
-data-disassemble -s 32767 -e 32799 -- 3
Error message from debugger back end:
Cannot access memory at address 0x7ffe
vector:
00008000: movs r4, #152 ; 0x98
00008002: movs r0, #0
00008004: ldrh r1, [r7, #12]
00008006: movs r0, r0
00008008: ldrh r5, [r4, #4]

```

Figure 120: Disassembly Display in NSECSD Debug Mode

## 2.5.8 Debugger support

Renesas E2, E2 Lite, and SEGGER J-Link are supported in e<sup>2</sup> studio for TZ projects.

### Debugger Support for TZ Projects

Feature	E2 Lite	E2	J-Link	J-Link OB	ULINK	IAR i-Jet
JTAG	Yes	Yes	Yes	No	Yes	Yes
SWD	Yes	Yes	Yes	Yes	Yes	Yes
ETB trace	Yes	Yes	Yes	Yes	Yes	Yes
ETM trace	No	Yes	Yes	No	Yes	Yes
TZ partition programming	Yes	Yes	Yes	Yes	No	No
Non secure debug	Yes	Yes	Yes	Yes	Yes	Yes
e <sup>2</sup> studio	Yes	Yes	Yes	Yes	No	TBC
IAR EW Arm	Under consideration	Under consideration	Yes	Yes	No	Yes
Keil MDK	Under consideration	Under consideration	Yes	Yes	Yes	No

## 2.5.9 Third-Party IDEs

Third-party IDEs such as IAR Systems EWARM and Keil MDK (uVision) are supported by the RA Smart Configurator (RA SC).

In general, RA SC offers the same configurator functionality as e<sup>2</sup> studio documented above. Project

generators are available to initialise workspaces in the target IDEs as well as setting up debug configurations and so forth. However, there are some limitations that need to be noted especially with regards to IDAU TZ partition register programming. See the specific RA SC documentation for usage details.

### 2.5.10 Renesas Flash Programmer (RFP)

Updated versions of Renesas Flash Programmer (RFP) are available to support setting of partitions, DLM state and Authentication keys.

RFP can be downloaded free of charge on the Renesas web site.

A new mode has been added to Program Flash Options as shown in the following graphics.

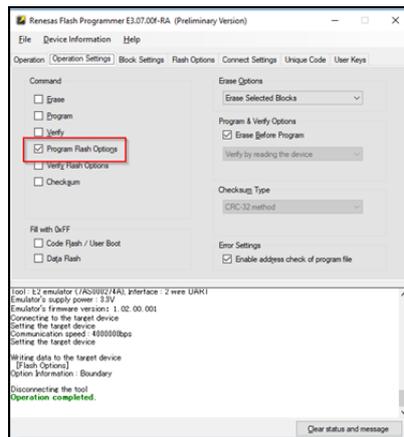


Figure 121: RFP Program Flash Options

Options to set partition boundaries are shown in the following figure.

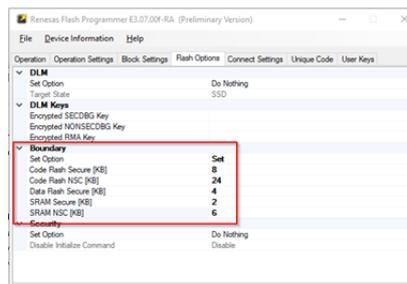


Figure 122: RFP Partition Boundaries

Options to set DLM state, Authentication keys, and Security settings are shown in the following figure.

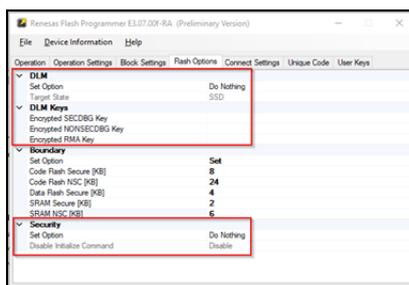


Figure 123: RFP DLM State, Authentication Keys, and Security Settings

Great care is needed here as some DLM states can **\*\*permanently\*\*** turn off debug and boot mode on the devices. Equally programming a security access authentication key can lead to permanently locked devices if the key is lost.

## 2.5.11 Glossary

### IDAU

Implementation Defined Attribute Unit. Used to program TZ partitions in SCI book mode.

### NSECSD

Non-Secure Software Development mode

### SSD

Secure Software Development mode

### NSC

Non-Secure Callable. Special Secure memory region used for Veneer to allow access to Secure APIs from Non-Secure code.

### Provisioned

Device with Secure code pre-programmed and DLM state set to **NSECSD**

### Flat project

All code, data and peripherals are configured as secure with the exception of the EDMAC RAM buffer which are placed in Non-Secure RAM due to the configuration of the internal bus masters.

### Veneer

Code that resides in Non-Secure Callable region

### Combined model

Development engineer has access to both Secure and Non-Secure project and source code

### Split model

Development Engineer has access to only the Non-Secure partition. No visibility of Secure source code. Secure code will be provisioned into device.

### 2.5.11.1 Configurator Icon Glossary

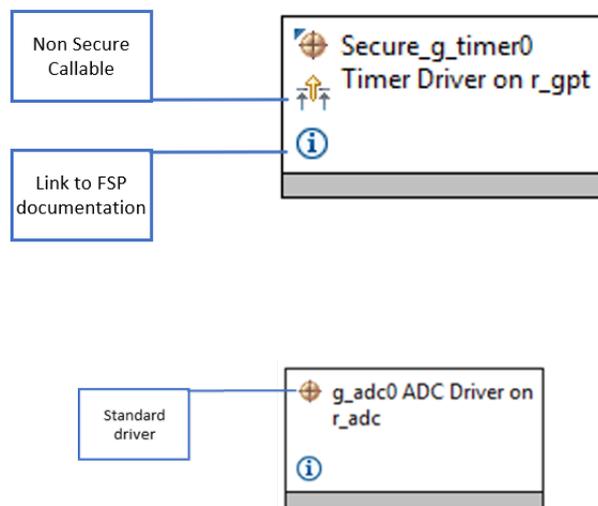


Figure 124: Configurator Icons

## 2.6 RA SC User Guide for MDK and IAR

### 2.6.1 What is RA SC?

The Renesas RA Smart Configurator (RA SC) is a desktop application designed to configure device hardware such as clock set up and pin assignment as well as initialization of FSP software components for a Renesas RA microcontroller project when using a 3rd-party IDE and toolchain.

The RA Smart Configurator can currently be used with

1. Keil MDK and the Arm compiler toolchain.
2. IAR EWARM with IAR toolchain for Arm

Projects can be configured and the project content generated in the same way as in e2 studio. Please refer to [Configuring a Project](#) section for more details.

### 2.6.2 Using RA Smart Configurator with Keil MDK

#### 2.6.2.1 Prerequisites

- Keil MDK and Arm compiler are installed and licensed. Please refer to the RASC Release notes for the version to be installed.
- Import the RA device pack. Download the RA device pack archive file (ex: MDK\_Device\_Packs\_2.x.x.zip) from the [FSP GitHub release page](#). Extract the archive file to locate the RA device pack. To import the RA device pack, launch the PackInstaller.exe from <keil\_mdk\_install\_dir>\UV4. Select the menu item **File > Import...** and browse to the extracted .pack file.
- Verify that the latest updates for RA devices are included in Keil MDK. To verify, select the menu "Packs" in Pack Installer and verify that the menu item **Check for Updates on Launch** is selected. If not, select **Check for Updates on Launch** and relaunch Pack

Installer.

- For flashing and debugging, the latest Segger J-Link DLL is installed into Keil MDK.
- Install RA SC and FSP using the Platform Installer from the GitHub release page.

### 2.6.2.2 Create new RA project

The following steps are required to create an RA project using Keil MDK, RA SC and FSP:

1. Start the RA Smart Configurator.
2. Enter a project folder and project name.

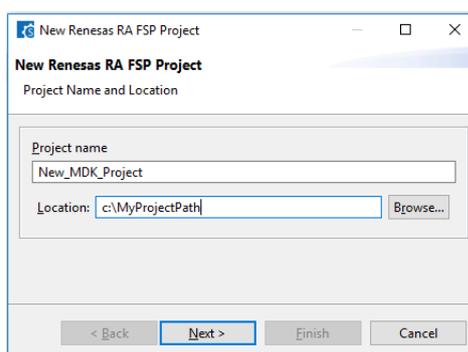


Figure 125: RA SC project settings

3. Select the target device and IDE.

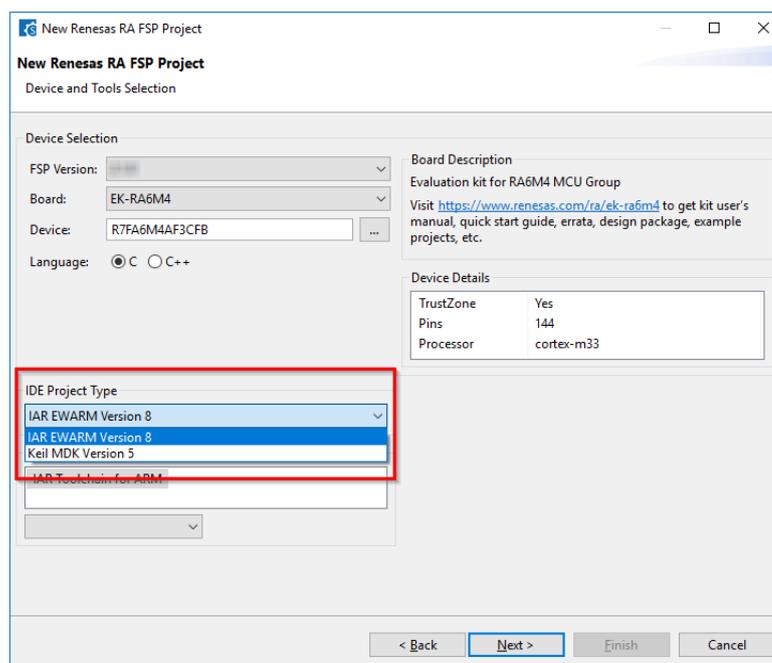


Figure 126: Target device and IDE selection

4. The rest of the project generator and FSP configuration is the same as e2 studio. Please

refer to the previous sections for details.

5. On completion of the FSP configuration, press "Generate Project Content"
6. A new Keil MDK project file will be generated in the project path. Double click this file to open MDK and continue development as usual.

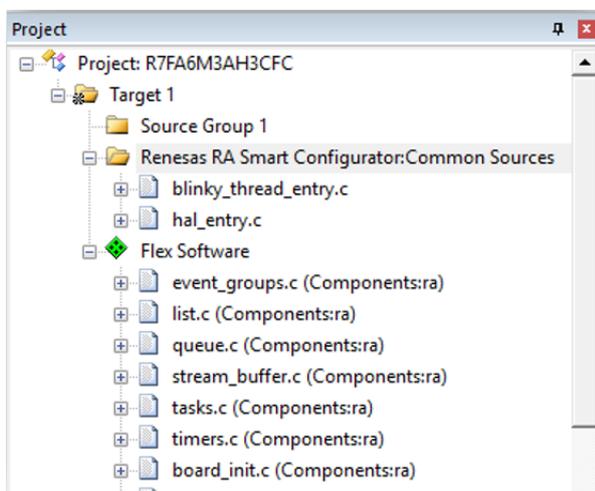


Figure 127: uVision project workspace with imported project data

### 2.6.2.3 Modify existing RA project

Once an initial project has been generated and configured, it is also possible to make changes using RA SC as follows.

*Note*

*This setup only needs to be done once per project.*

Set up the following links to RA SC:

1. In Keil MDK uVision, select **Tools > Customize Tools Menu...**
2. Select the **new** icon and fill in the fields as follows for each tool:
  - a. RA Smart Configurator:
    - Menu item name: Enter: RA Smart Configurator
    - Command: Select "." and navigate to rasc.exe
    - Initial Folder: Enter: \$P
    - Arguments: Enter: --device \$D --compiler ARMv6 configuration.xml
  - b. Device Partition Manager:
    - Menu item name: Enter: Device Partition Manager
    - Command: Select "." and navigate to rasc.exe
    - Initial Folder: Enter: \$P
    - Arguments: Enter: -application com.renesas.cdt.ddsc.dpm.ui.dpmapplication configuration.xml "SL%L"

To reconfigure an existing project select **Tools > RA Smart Configurator**

To reconfigure the TrustZone partitions select **Tools > Device Partition Manager**

### 2.6.2.4 Build and Debug RA project

The project can be built by selecting the menu item **Project > Build Target** or tool bar item **Rebuild** or the keyboard shortcut F7.

Assembler, Compiler, Linker and Debugger settings can be changed in **Options for Target** dialog, which can be launched using the menu item **Project > Options for Target**, the tool bar item **Options for Target** or the keyboard shortcut Alt+F7.

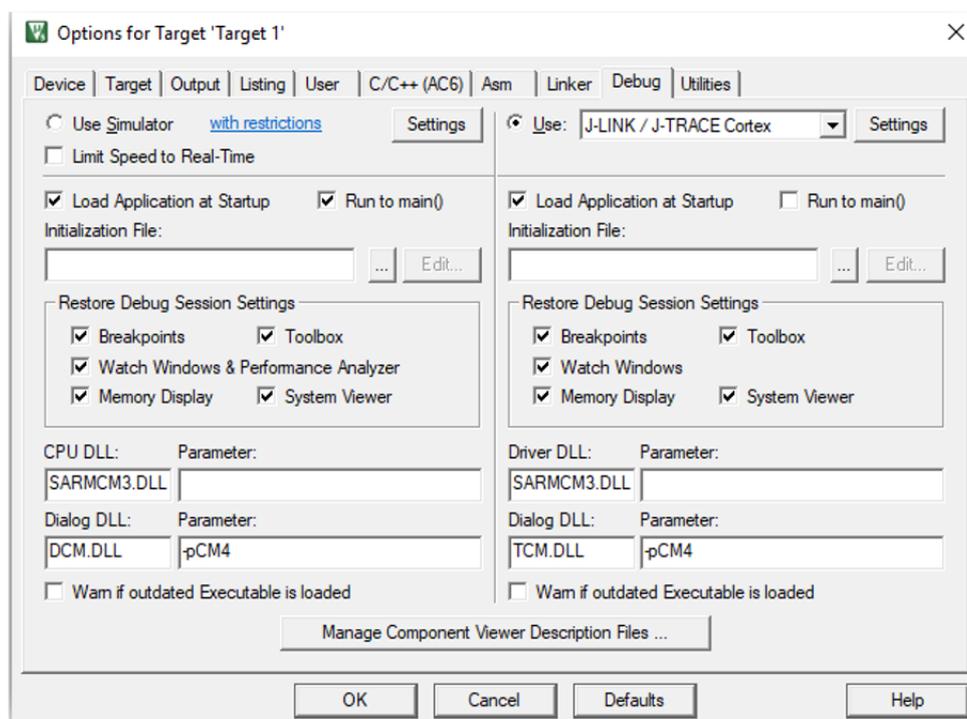


Figure 128: Options for Target

RA SC will set up the uVision project to debug the selected device using J-Link or J-Link OB debugger by default.

A Debug session can be started or stopped by selecting the menu item **Debug > Start/Stop Debug Session** or keyboard shortcut CTRL+F5. When debugging for the first time, J-Link firmware update may be needed if requested by the tool.

Refer to the documentation from Keil to get more information on the debug features in uVision. Note that not all features supported by uVision debugger are implemented in the J-Link interface. Consult SEGGER J-Link documentation for more information.

### 2.6.2.5 Notes and Restrictions

1. **When debugging a TrustZone based project, the Secure project image MUST be downloaded before the Non Secure project.**
2. For TrustZone enabled devices, the user will need to manually set up the memory partitions using the "Renesas Device Partition Manager" from inside RA SC before downloading.

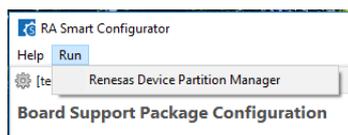


Figure 129: Renesas Device partition Manager

3. RA FSP contains a full set of drivers and middleware and may not be compatible with other CMSIS packs from Keil, Arm or third parties.
4. Flash programming is currently only supported through the debugger connection.

### 2.6.3 Using RA Smart Configurator with IAR EWARM

IAR Systems Embedded Workbench for Arm (EWARM) includes support for Renesas RA devices. These can be set up as bare metal designs within EWARM. However, most RA developers will want to integrate RA FSP drivers and middleware into their designs. RA SC will facilitate this.

RA SC generates a "Project Connection" file that can be loaded directly into EWARM to update project files.

#### 2.6.3.1 Prerequisites

- IAR EWARM installed and licensed. Please refer to the Release notes for the version to be installed.
- RA SC and FSP Installed

#### 2.6.3.2 Create new RA project

The following steps are required to create an RA project using IAR EWARM, RA SC and FSP:

1. Start the RA Smart Configurator.
2. Enter a project folder and project name.

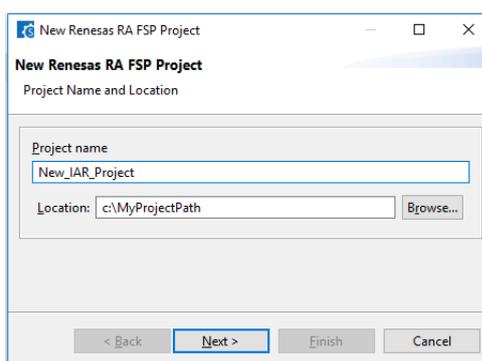


Figure 130: RA SC project settings

3. Select the target device and IDE.

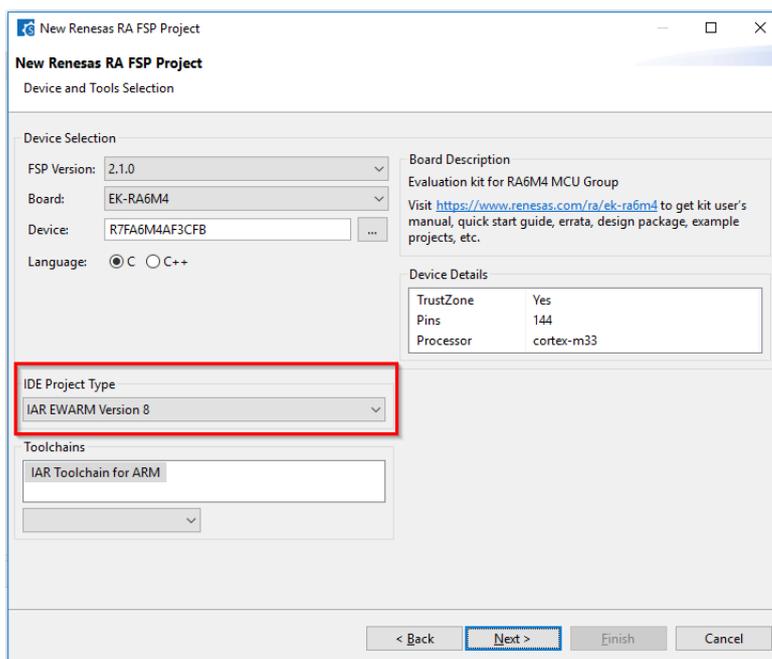


Figure 131: Target device and IDE selection

4. The rest of the project generator and FSP configuration operates the same as e2 studio. Refer to the previous sections for details.
5. On completion of the FSP configuration, press **Generate Project Content**.
6. A new IAR EWARM project file will be generated in the project path. Double click this file to open IAR EWARM and continue development as usual.
7. To Use RA SC with EWARM, RA SC needs to be configured as a tool in EWARM by selecting the menu item **Tools > Configure Tools...**. Select **New** to create a new tool in the dialog shown and add the following information:
  - Menu Text: **RA Smart Configurator**
    - a. Command: Select **Browse...** and navigate to rasc.exe in the installed RA SC
    - b. Argument: -compiler IAR configuration.xml
    - c. Initial Directory: \$PROJ\_DIR\$
    - d. Tool Available: Always
  - Menu Text: **Device Partition Manager**
    - a. Command: Select **Browse...** and navigate to rasc.exe in the installed RA SC
    - b. Argument: -application com.renesas.cdt.ddsc.dpm.ui.dpmapplication configuration.xml "\$TARGET\_PATH\$"
    - c. Initial Directory: \$PROJ\_DIR\$
    - d. Tool Available: Always
8. RA SC can now be re-launched from EWARM using the menu item **Tools > RA Smart Configurator**.
9. A Project connection needs to be set up in EWARM to build the project. Select **Project > Add Project Connection** in EWARM and select **IAR Project Connection**. Navigate to the project folder and select buildinfo.ipcf and click **Open**. The project can now build in EWARM.

### 2.6.3.3 Notes and Restrictions

When starting a TrustZone enabled debug session Partition sizes are checked automatically.

- If partition sizes are set correctly, the debug session will launch as normal.

- If partition sizes need to be changed, IAR EWARM will prompt to run the Renesas Device Partition Manager. Select **Yes**. The Device Partition Manager will start with the required partition sizes prefilled.
- Select **Set TrustZone secure / non-secure boundaries** as the only action.
- Enter debugger details, if required.
- Select **Run** to program the partitions.
- Return to the IDE and relaunch the debug session

# Chapter 3 FSP Architecture

## 3.1 FSP Architecture Overview

This guide describes the Renesas Flexible Software Package (FSP) architecture and how to use the FSP Application Programming Interface (API).

### 3.1.1 C99 Use

The FSP uses the ISO/IEC 9899:1999 (C99) C programming language standard. Specific features introduced in C99 that are used include standard integer types (`stdint.h`), booleans (`stdbool.h`), designated initializers, and the ability to intermingle declarations and code.

### 3.1.2 Doxygen

Doxygen is the default documentation tool used by FSP. You can find Doxygen comments throughout the FSP source.

### 3.1.3 Weak Symbols

Weak symbols are used occasionally in the FSP. They are used to ensure that a project builds even when the user has not defined an optional function.

### 3.1.4 Memory Allocation

Dynamic memory allocation through use of the `malloc()` and `free()` functions are not used in FSP modules; all memory required by FSP modules is allocated in the application and passed to the module in a pointer. Exceptions are considered only for ports of 3rd party code that require dynamic memory.

### 3.1.5 FSP Terms

Term	Description	Reference
BSP	Short for Board Support Package. In the FSP the BSP provides just enough foundation to allow other FSP modules to work together without issue.	<a href="#">MCU Board Support Package</a>

Module	Modules can be peripheral drivers, purely software, or anything in between. Each module consists of a folder with source code, documentation, and anything else that the customer needs to use the code effectively. Modules are independent units, but they may depend on other modules. Applications can be built by combining multiple modules to provide the user with the features they need.	<a href="#">FSP Modules</a>
Driver	A driver is a specific kind of module that directly modifies registers on the MCU.	-
Interface	An interface contains API definitions that can be shared by modules with similar features. Interfaces are definitions only and do not add to code size.	<a href="#">FSP Interfaces</a>
Stacks	The FSP architecture is designed such that modules work together to form a stack. A stack consists of a top level module and all its dependencies.	<a href="#">FSP Stacks</a>
Module Instance	Single and independent instantiation of a module. An application may require two GPT timers. Each of these timers is a module instance of the r_gpt module.	-
Application	Code that is owned and maintained by the user. Application code may be based on sample application code provided by Renesas, but it is the responsibility of the user to maintain as necessary.	-

Callback Function	This term refers to a function that is called when an event occurs. As an example, suppose the user would like to be notified every second based on the RTC. As part of the RTC configuration, a callback function can be supplied that will be jumped to during each RTC interrupt. When a single callback services multiple events, the arguments contain the triggering event. Callback functions for interrupts should be kept short and handled carefully because when they are called the MCU is still inside of an interrupt, delaying any pending interrupts.	-
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## 3.2 FSP Modules

Modules are the core building block of FSP. Modules can do many different things, but all modules share the basic concept of providing functionality upwards and requiring functionality from below.

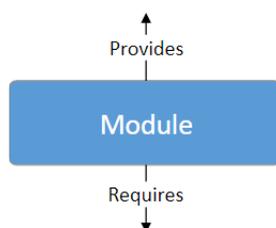


Figure 132: Modules

The amount of functionality provided by a module is determined based on functional use cases. Common functionality required by multiple modules is often placed into a self-contained submodule so it can be reused. Code size, speed and complexity are also considered when defining a module.

The simplest FSP application consists of one module with the Board Support Package (BSP) and the user application on top.

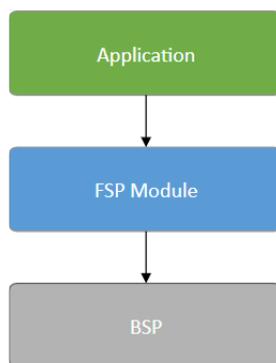


Figure 133: Module with application

The Board Support Package (BSP) is the foundation for FSP modules, providing functionality to determine the MCU used as well as configuring clocks, interrupts and pins. For the sake of clarity, the BSP will be omitted from further diagrams.

### 3.3 FSP Stacks

When modules are layered atop one another, an FSP stack is formed. The stacking process is performed by matching what one module provides with what another module requires. For example, the SPI module ([Serial Peripheral Interface \(r\\_spi\)](#)) requires a module that provides the transfer interface ([Transfer Interface](#)) to send or receive data without a CPU interrupt. The transfer interface requirement can be fulfilled by the DTC driver module ([Data Transfer Controller \(r\\_dtc\)](#)).

Through this methodology the same code can be shared by several modules simultaneously. The example below illustrates how the same DTC module can be used with SPI ([Serial Peripheral Interface \(r\\_spi\)](#)), UART ([Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)) and SDHI ([SD/MMC Host Interface \(r\\_sdhi\)](#)).

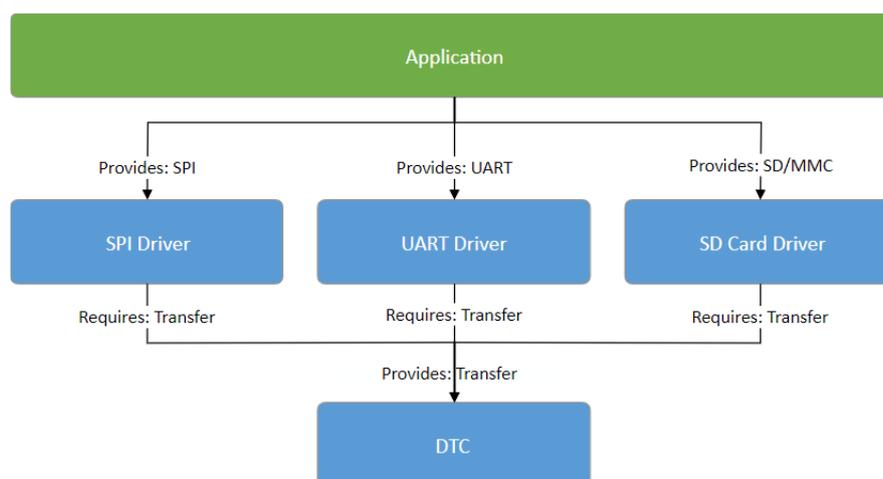


Figure 134: Stacks -- Shared DTC Module

The ability to stack modules ensures the flexibility of the architecture as a whole. If multiple modules include the same functionality issues arise when application features must work across different user designs. To ensure that modules are reusable, any dependent modules must be capable of being swapped out for other modules that provide the same features. The FSP

architecture provides this flexibility to swap modules in and out through the use of FSP interfaces.

## 3.4 FSP Interfaces

At the architecture level, interfaces are the way that modules provide common features. This commonality allows modules that adhere to the same interface to be used interchangeably. Interfaces can be thought of as a contract between two modules - the modules agree to work together using the information that was established in the contract.

On RA hardware there is occasionally an overlap of features between different peripherals. For example, I2C communications can be achieved through use of the IIC peripheral or the SCI peripheral. However, there is a difference in the level of features provided by both peripherals; in I2C mode the SCI peripheral will only support a subset of the capabilities of the fully-featured IIC.

Interfaces aim to provide support for the common features that most users would expect. This means that some of the advanced features of a peripheral (such as IIC) might not be available in the interface. In most cases these features are still available through interface extensions.

In FSP design, interfaces are defined in header files. All interface header files are located in the folder `ra/fsp/inc/api` and end with `*_api.h`. Interface extensions are defined in header files in the folder `ra/fsp/inc/instances`. The following sections detail what makes up an interface.

### 3.4.1 FSP Interface Enumerations

Whenever possible, interfaces use typed enumerations for function parameters and structure members.

```
typedef enum e_i2c_master_addr_mode
{
    I2C_MASTER_ADDR_MODE_7BIT = 1,    ///< Use 7-bit addressing mode
    I2C_MASTER_ADDR_MODE_10BIT = 2,   ///< Use 10-bit addressing mode
} i2c_master_addr_mode_t;
```

Enumerations remove uncertainty when deciding what values are available for a parameter. FSP enumeration options follow a strict naming convention where the name of the type is prefixed on the available options. Combining the naming convention with the autocomplete feature available in e2 studio (Ctrl + Space) provides the benefits of rapid coding while maintaining high readability.

### 3.4.2 FSP Interface Callback Functions

Callback functions allow modules to asynchronously alert the user application when an event has occurred, such as when a byte has been received over a UART channel or an IRQ pin is toggled. FSP driver modules define and handle the interrupt service routines for RA MCU peripherals to ensure any required hardware procedures are implemented. The interrupt service routines in FSP modules then call the user-defined callbacks to allow the application to respond.

Callback functions must be defined in the user application. They always return void and take a structure for their one parameter. The structure is defined in the interface for the module and is named `<interface>_callback_args_t`. The contents of the structure may vary depending on the

interface, but two members are common: event and p\_context.

The event member is an enumeration defined in the interface used by the application to determine why the callback was called. Using the UART example, the callback could be triggered for many different reasons, including when a byte is received, all bytes have been transmitted, or a framing error has occurred. The event member allows the application to determine which of these three events has occurred and handle it appropriately.

The p\_context member is used for providing user-specified data to the callback function. In many cases a callback function is shared between multiple channels or module instances; when the callback occurs, the code handling the callback needs context information so that it can determine which module instance the callback is for. For example, if the callback wanted to make an FSP API call in the callback, then at a minimum the callback will need a reference to the relevant control structure. To make this easy, the user can provide a pointer to the control structure as the p\_context. When the callback occurs, the control structure is passed in the p\_context element of the callback structure.

Callback functions are called from within an interrupt service routine. For this reason callback functions should be kept as short as possible so they do not affect the real time performance of the user's system. An example skeleton function for the flash interface callback is shown below.

```
void flash_callback (flash_callback_args_t * p_args)
{
    /* See what event caused this callback. */
    switch (p_args->event)
    {
        case FLASH_EVENT_ERASE_COMPLETE:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_WRITE_COMPLETE:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_BLANK:
            {
                /* Handle event. */
                break;
            }
        case FLASH_EVENT_NOT_BLANK:
```

```
    {
/* Handle event. */
break;
    }
case FLASH_EVENT_ERR_DF_ACCESS:
    {
/* Handle error. */
break;
    }
case FLASH_EVENT_ERR_CF_ACCESS:
    {
/* Handle error. */
break;
    }
case FLASH_EVENT_ERR_CMD_LOCKED:
    {
/* Handle error. */
break;
    }
case FLASH_EVENT_ERR_FAILURE:
    {
/* Handle error. */
break;
    }
case FLASH_EVENT_ERR_ONE_BIT:
    {
/* Handle error. */
break;
    }
}
}
```

When a module is not directly used in the user application (that is, it is not the top layer of the stack), its callback function will be handled by the module above. For example, if a module requires

a UART interface module the upper layer module will control and use the UART's callback function. In this case the user would not need to create a callback function for the UART module in their application code.

### 3.4.3 FSP Interface Data Structures

At a minimum, all FSP interfaces include three data structures: a configuration structure, an API structure, and an instance structure.

#### 3.4.3.1 FSP Interface Configuration Structure

The configuration structure is used for the initial configuration of a module during the `<MODULE>_Open()` call. The structure consists of members such as channel number, bitrate, and operating mode.

The configuration structure is used purely as an input into the module. It may be stored and referenced by the module, so the configuration structure and anything it references must persist as long as the module is open.

The configuration structure is allocated for each module instance in files generated by the RA Configuration editor.

When FSP stacks are used, it is also important to understand that configuration structures only have members that apply to the current interface. If multiple layers in the same stack define the same configuration parameters then it becomes difficult to know where to modify the option. For example, the baud rate for a UART is only defined in the UART module instance. Any modules that use the UART interface rely on the baud rate being provided in the UART module instance and do not offer it in their own configuration structures.

#### 3.4.3.2 FSP Interface API Structure

All interfaces include an API structure which contains function pointers for all the supported interface functions. An example structure for the [Digital to Analog Converter \(r\\_dac\)](#) is shown below.

```
typedef struct st_dac_api
{
    /** Initial configuration.
     * @par Implemented as
     * - @ref R_DAC_Open()
     * - @ref R_DAC8_Open()
     *
     * @param[in] p_ctrl Pointer to control block. Must be declared by user. Elements
    set here.
     * @param[in] p_cfg Pointer to configuration structure. All elements of this
    structure must be set by user.
     */
    fsp_err_t (* open)(dac_ctrl_t * const p_ctrl, dac_cfg_t const * const p_cfg);
}
```

```
/** Close the D/A Converter.
 * @par Implemented as
 * - @ref R_DAC_Close()
 * - @ref R_DAC8_Close()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 */
fsp_err_t (* close)(dac_ctrl_t * const p_ctrl);
/** Write sample value to the D/A Converter.
 * @par Implemented as
 * - @ref R_DAC_Write()
 * - @ref R_DAC8_Write()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 * @param[in] value Sample value to be written to the D/A Converter.
 */
fsp_err_t (* write)(dac_ctrl_t * const p_ctrl, uint16_t value);
/** Start the D/A Converter if it has not been started yet.
 * @par Implemented as
 * - @ref R_DAC_Start()
 * - @ref R_DAC8_Start()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
timer.
 */
fsp_err_t (* start)(dac_ctrl_t * const p_ctrl);
/** Stop the D/A Converter if the converter is running.
 * @par Implemented as
 * - @ref R_DAC_Stop()
 * - @ref R_DAC8_Stop()
 *
 * @param[in] p_ctrl Control block set in @ref dac_api_t::open call for this
```

```
timer.  
    */  
    fsp_err_t (* stop)(dac_ctrl_t * const p_ctrl);  
} dac_api_t;
```

The API structure is what allows for modules to easily be swapped in and out for other modules that are instances of the same interface. Let's look at an example application using the DAC interface above.

RA MCUs have an internal DAC peripheral. If the DAC API structure in the DAC interface is not used the application can make calls directly into the module. In the example below the application is making calls to the [R\\_DAC\\_Write\(\)](#) function which is provided in the `r_dac` module.

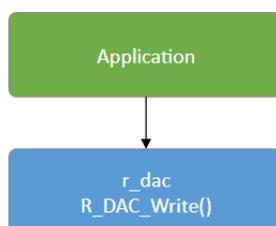


Figure 135: DAC Write example

Now let's assume that the user needs more DAC channels than are available on the MCU and decides to add an external DAC module named `dac_external` using I2C for communications. The application must now distinguish between the two modules, adding complexity and further dependencies to the application.

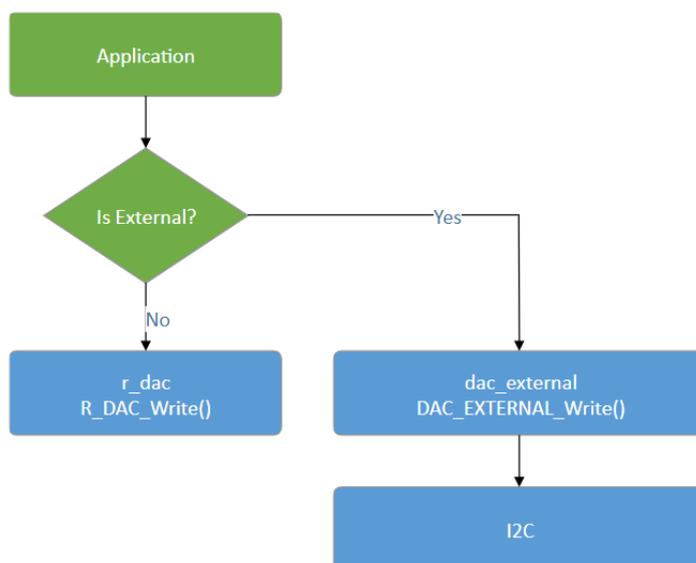


Figure 136: DAC Write with two write modules

The use of interfaces and the API structure allows for the use of an abstracted DAC. This means that no extra logic is needed if the user's `dac_external` module implements the FSP DAC interface, so the application no longer depends upon hard-coded module function names. Instead the application now depends on the DAC interface API which can be implemented by any number of modules.

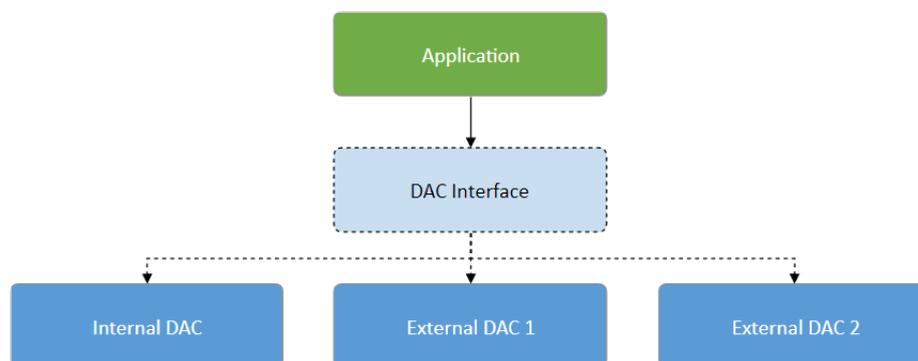


Figure 137: DAC Interface

### 3.4.3.3 FSP Interface Instance Structure

Every FSP interface also has an instance structure. The instance structure encapsulates everything required to use the module:

- A pointer to the instance API structure ([FSP Instance API](#))
- A pointer to the configuration structure
- A pointer to the control structure

The instance structure is not required at the application layer. It is used to connect modules to their dependencies (other than the BSP).

Instance structures have a standardized name of `<interface>_instance_t`. An example from the [Transfer Interface](#) is shown below.

```

typedef struct st_transfer_instance
{
    transfer_ctrl_t      * p_ctrl; ///< Pointer to the control structure for this
instance
    transfer_cfg_t const * p_cfg;   ///< Pointer to the configuration structure
for this instance
    transfer_api_t const * p_api;  ///< Pointer to the API structure for this
instance
} transfer_instance_t;
  
```

Note that when an instance structure variable is declared, the API is the only thing that is instance specific, not *module instance* specific. This is because all module instances of the same module share the same underlying module source code. If SPI is being used on SCI channels 0 and 2 then

both module instances use the same API while the configuration and control structures are typically different.

## 3.5 FSP Instances

While interfaces dictate the features that are provided, instances actually implement those features. Each instance is tied to a specific interface. Instances use the enumerations, data structures, and API prototypes from the interface. This allows an application that uses an interface to swap out the instance when needed.

On RA MCUs some peripherals are used to implement multiple interfaces. In the example below the IIC and SPI peripherals map to only one interface each while the SCI peripheral implements three interfaces.

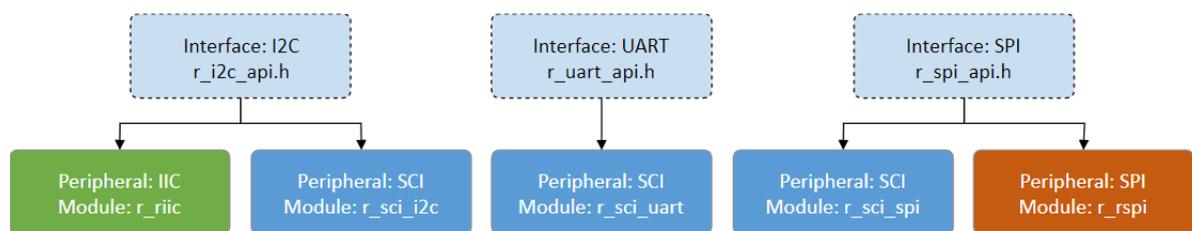


Figure 138: Instances

In FSP design, instances consist of the interface extension and API defined in the instance header file located in the folder `ra/fsp/inc/instances` and the module source `ra/fsp/src/<module>`.

### 3.5.1 FSP Instance Control Structure

The control structure is used as a unique identifier for the module instance and contains memory required by the module. Elements in the control structure are owned by the module and *must not be modified* by the application. The user allocates storage for a control structure, often as a global variable, then sends a pointer to it into the `<MODULE>_Open()` call for a module. At this point, the module initializes the structure as needed. The user must then send in a pointer to the control structure for all subsequent module calls.

### 3.5.2 FSP Interface Extensions

In some cases, instances require more information than is provided in the interface. This situation can occur in the following cases:

- An instance offers extra features that are not common to most instances of the interface. An example of this is the start source selection of the GPT ([General PWM Timer \(r\\_gpt\)](#)). The GPT can be configured to start based on hardware events such as a falling edge on a trigger pin. This feature is not common to all timers, so it is included in the GPT instance.
- An interface must be very generic out of necessity. As an interface becomes more generic, the number of possible instances increases. An example of an interface that must be generic is a block media interface that abstracts functions required by a file system. Possible instances include SD card, SPI Flash, SDRAM, USB, and many more.

The `p_extend` member provides this extension function.

Use of interface extensions is not always necessary. Some instances do not offer an extension since

all functionality is provided in the interface. In these cases the `p_extend` member can be set to `NULL`. The documentation for each instance indicates whether an interface extension is available and whether it is mandatory or optional.

### 3.5.2.1 FSP Extended Configuration Structure

When extended configuration is required it can be supplied through the `p_extend` parameter of the interface configuration structure.

The extended configuration structure is part of the instance, but it is also still considered to be part of the configuration structure. All usage notes about the configuration structure described in [FSP Interface Configuration Structure](#) apply to the extended configuration structure as well.

The extended configuration structure and all typed structures and enumerations required to define it make up the interface extension.

### 3.5.3 FSP Instance API

Each instance includes a constant global variable tying the interface API functions to the functions provided by the module. The name of this structure is standardized as `g_<interface>_on_<instance>`. Examples include `g_spi_on_spi`, `g_transfer_on_dtc`, and `g_adc_on_adc`. This structure is available to be used through an `extern` in the instance header file (`r_spi.h`, `r_dtc.h`, and `r_adc.h` respectively).

## 3.6 FSP API Standards

### 3.6.1 FSP Function Names

FSP functions start with the uppercase module name (`<MODULE>`). All modules have `<MODULE>_Open()` and `<MODULE>_Close()` functions. The `<MODULE>_Open()` function must be called before any of the other functions.

Other functions that will commonly be found are `<MODULE>_Read()`, `<MODULE>_Write()`, `<MODULE>_InfoGet()`, and `<MODULE>_StatusGet()`. The `<MODULE>_StatusGet()` function provides a status that could change asynchronously, while `<MODULE>_InfoGet()` provides information that cannot change after open or can only be updated by API calls. Example function names include:

- `R_SPI_Read()`, `R_SPI_Write()`, `R_SPI_WriteRead()`
- `R_SDHI_StatusGet()`
- `R_RTC_CalendarAlarmSet()`, `R_RTC_CalendarAlarmGet()`
- `R_FLASH_HP_AccessWindowSet()`, `R_FLASH_HP_AccessWindowClear()`

### 3.6.2 Use of const in API parameters

The `const` qualifier is used with API parameters whenever possible. An example case is shown below.

```
fsp_err_t R_FLASH_HP_Open(flash_ctrl_t * const p_api_ctrl, flash_cfg_t const * const p_cfg);
```

□

In this example, `flash_cfg_t` is a structure of configuration parameters for the `r_flash_hp` module. The parameter `p_cfg` is a pointer to this structure. The first `const` qualifier on `p_cfg` ensures the

`flash_cfg_t` structure cannot be modified by `R_FLASH_HP_Open()`. This allows the structure to be allocated as a const variable and stored in ROM instead of RAM.

The const qualifier after the pointer star for both `p_ctrl` and `p_cfg` ensures the FSP function does not modify the input pointer addresses. While not fool-proof by any means this does provide some extra checking inside the FSP code to ensure that arguments that should not be altered are treated as such.

### 3.6.3 FSP Version Information

The BSP provides a function `R_FSP_VersionGet()` which fills in a structure of type `fsp_pack_version_t`. This can be used to determine the FSP version at runtime.

There are also `FSP_VERSION_*` macros in `fsp_version.h` that can be used to determine the FSP version at build time.

## 3.7 FSP Build Time Configurations

All modules have a build-time configuration header file. Most configuration options are supplied at run time, though options that are rarely used or apply to all instances of a module may be moved to build time. The advantage of using a build-time configuration option is to potentially reduce code size reduction by removing an unused feature.

All modules have a build time option to enable or disable parameter checking for the module. FSP modules check function arguments for validity when possible, though this feature is disabled by default to reduce code size. Enabling it can help catch parameter errors during development and debugging. By default, each module's parameter checking configuration inherits the BSP parameter checking setting (set on the BSP tab of the RA Configuration editor). Leaving each module's parameter checking configuration set to Default (BSP) allows parameter checking to be enabled or disabled globally in all FSP code through the parameter checking setting on the BSP tab.

If an error condition can reasonably be avoided it is only checked in a section of code that can be disabled by disabling parameter checking. Most FSP APIs can only return `FSP_SUCCESS` if parameter checking is disabled. An example of an error that cannot be reasonably avoided is the "bus busy" error that occurs when another master is using an I2C bus. This type of error can be returned even if parameter checking is disabled.

## 3.8 FSP File Structure

The high-level file structure of an FSP project is shown below.

```
ra_gen
ra
+---fsp
    +---inc
    |   +---api
    |   \---instances
    \---src
        +---bsp
```

```
    \---r_module
ra_cfg
+---fsp_cfg
    +---bsp
    +---driver
```

Directly underneath the base ra folder the folders are split into the source and include folders. Include folders are kept separate from the source for easy browsing and easy setup of include paths.

The ra\_gen folder contains code generated by the RA Configuration editor. This includes global variables for the control structure and configuration structure for each module.

The ra\_cfg folder is where configuration header files are stored for each module. See [FSP Build Time Configurations](#) for information on what is provided in these header files.

## 3.9 FSP TrustZone Support

TrustZone support for FSP is primarily handled in the RA Configuration Tool.

### 3.9.1 FSP TrustZone Projects

During development of a TrustZone project, users create an RA TrustZone Secure Project first, followed by an RA TrustZone Non-secure Project that is linked to the RA TrustZone Secure Project. Allocation of secure memory is handled automatically within the tooling. The non-secure project starts at the required alignment boundary beyond the memory taken by the secure project.

### 3.9.2 Non-Secure Callable Guard Functions

The tooling generates guard functions for any module marked as Non-secure Callable. These guard functions are owned by the application once generated, so they can be modified as necessary by the secure application developer.

The default non-secure callable guard functions limit the configuration and control structure to the structures generated in the secure project. They also check any input pointers to ensure the caller does not overwrite secure memory.

### 3.9.3 Callbacks in Non-Secure from Non-Secure Callable Modules

If the non-secure project needs a callback function from a non-secure callable module, the callback can be registered after the module is opened using the `callback_set()` guard function.

### 3.9.4 Additional TrustZone Information

The following resources provide technical background, application notes and example projects that demonstrate key TrustZone concepts and implementation procedures.

- [The Benefits of Using Arm® TrustZone® in Your Design](#) (Brochure)
- [RA Arm® TrustZone® Tooling Primer](#) (Application Note)
- [Renesas RA Family Security Design with Arm® TrustZone® - IP Protection](#) (Application

Note)

- [Renesas RA Family Securing Data at Rest Using the Arm® TrustZone® \(Application Note\)](#)

## 3.10 FSP Architecture in Practice

### 3.10.1 FSP Connecting Layers

FSP modules are meant to be both reusable and stackable. It is important to remember that modules are not dependent upon other modules, but upon other interfaces. The user is then free to fulfill the interface using the instance that best fits their needs.

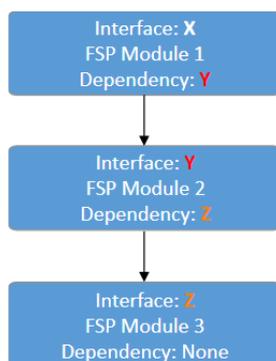


Figure 139: Connecting layers

In the image above interface Y is a dependency of interface X and has its own dependency on interface Z. Interface X only has a dependency on interface Y. Interface X has no knowledge of interface Z. This is a requirement for ensuring that layers can easily be swapped out.

### 3.10.2 Using FSP Modules in an Application

The typical use of an FSP module involves generating required module data then using the API in the application.

#### 3.10.2.1 Create a Module Instance in the RA Configuration Editor

The RA Configuration editor (available both in the Renesas e2 studio IDE as well as through the standalone RA Smart Configurator) provides a graphical user interface for setting the parameters of the interface and instance configuration structures. It also automatically includes those structures (once they are configured in the GUI) in application-specific header files that can be included in application code.

The RA Configuration editor allocates storage for the control structures, all required configuration structures, and the instance structure in generated files in the ra\_gen folder. Use the **Properties** window to set the values for the members of the configuration structures as needed. Refer to the Configuration section of the module usage notes for documentation about the configuration options.

If the interface has a callback function option then the application must declare and define the function. The return value is always of type void and the parameter to the function is a typed structure of name <interface>\_callback\_args\_t. Once the function has been defined, assign its name to the p\_callback member of the configuration structure. Callback function names can be assigned through the **Properties** window for the selected module.

### 3.10.2.2 Use the Instance API in the Application

Call the module's <MODULE>\_Open() function. Pass pointers to the generated control structure and configuration structure. The names of these structures are based on the 'Name' field provided in the configuration editor. The control structure is <Name>\_ctrl and the configuration structure is <Name>\_cfg. An example <MODULE>\_Open() call for an r\_rtc module instance named g\_clock is:

```
R_RTC_Open(&g_clock_ctrl, &g_clock_cfg);
```

#### Note

*Each layer in the FSP Stack is responsible for calling the API functions of its dependencies. This means that users are only responsible for calling the API functions at the layer at which they are interfacing. Using the example above of a SPI module with a DTC dependency, the application uses only SPI APIs. The application starts by calling [R\\_SPI\\_Open\(\)](#). Internally, the SPI module opens the DTC. It locates [R\\_DTC\\_Open\(\)](#) by accessing the dependent transfer interface function pointers from the pointers DTC instances ([spi\\_cfg\\_t::p\\_transfer\\_tx](#) and [spi\\_cfg\\_t::p\\_transfer\\_rx](#)) to open the DTC.*

Refer to the module usage notes for example code to help get started with any particular module.

# Chapter 4 API Reference

This section includes the FSP API Reference for the Module and Interface level functions.

- ▶ [BSP](#)                      Common code shared by FSP drivers
- ▶ [Modules](#)                      Modules are the smallest unit of software available in the FSP. Each module implements one interface
- ▶ [Interfaces](#)                      The FSP interfaces provide APIs for common functionality. They can be implemented by one or more modules. Modules can use other modules as dependencies using this interface layer

## 4.1 BSP

### Detailed Description

Common code shared by FSP drivers.

#### Modules

##### [Common Error Codes](#)

##### [MCU Board Support Package](#)

The BSP is responsible for getting the MCU from reset to the user's application. Before reaching the user's application, the BSP sets up the stacks, heap, clocks, interrupts, C runtime environment, and stack monitor.

##### [BSP I/O access](#)

This module provides basic read/write access to port pins.

#### Data Structures

union [fsp\\_pack\\_version\\_t](#)

struct [fsp\\_pack\\_version\\_t.\\_\\_unnamed\\_\\_](#)

#### Macros

```
#define FSP_VERSION_MAJOR
```

```
#define FSP_VERSION_MINOR
```

```
#define FSP_VERSION_PATCH
```

```
#define FSP_VERSION_BUILD
```

```
#define FSP_VERSION_STRING
```

```
#define FSP_VERSION_BUILD_STRING
```

## Data Structure Documentation

### ◆ fsp\_pack\_version\_t

union fsp_pack_version_t		
FSP Pack version structure		
Data Fields		
uint32_t	version_id	Version id
struct fsp_pack_version_t	__unnamed__	Code version parameters, little endian order.

### ◆ fsp\_pack\_version\_t.\_\_unnamed\_\_

struct fsp_pack_version_t.__unnamed__		
Code version parameters, little endian order.		
Data Fields		
uint8_t	build	Build version of FSP Pack.
uint8_t	patch	Patch version of FSP Pack.
uint8_t	minor	Minor version of FSP Pack.
uint8_t	major	Major version of FSP Pack.

## Macro Definition Documentation

### ◆ FSP\_VERSION\_MAJOR

#define FSP_VERSION_MAJOR
FSP pack major version.

### ◆ FSP\_VERSION\_MINOR

```
#define FSP_VERSION_MINOR
```

FSP pack minor version.

### ◆ FSP\_VERSION\_PATCH

```
#define FSP_VERSION_PATCH
```

FSP pack patch version.

### ◆ FSP\_VERSION\_BUILD

```
#define FSP_VERSION_BUILD
```

FSP pack version build number (currently unused).

### ◆ FSP\_VERSION\_STRING

```
#define FSP_VERSION_STRING
```

Public FSP version name.

### ◆ FSP\_VERSION\_BUILD\_STRING

```
#define FSP_VERSION_BUILD_STRING
```

Unique FSP version ID.

## 4.1.1 Common Error Codes

### BSP

#### Detailed Description

All FSP modules share these common error codes.

#### Macros

```
#define FSP_PARAMETER_NOT_USED(p)
```

```
#define FSP_CPP_HEADER
```

```
#define FSP_HEADER
```

```
#define FSP_SECURE_ARGUMENT
```

## Enumerations

```
enum fsp_err_t
```

## Macro Definition Documentation

### ◆ FSP\_PARAMETER\_NOT\_USED

```
#define FSP_PARAMETER_NOT_USED ( p)
```

This macro is used to suppress compiler messages about a parameter not being used in a function. The nice thing about using this implementation is that it does not take any extra RAM or ROM.

### ◆ FSP\_CPP\_HEADER

```
#define FSP_CPP_HEADER
```

Determine if a C++ compiler is being used. If so, ensure that standard C is used to process the API information.

### ◆ FSP\_HEADER

```
#define FSP_HEADER
```

FSP Header and Footer definitions

### ◆ FSP\_SECURE\_ARGUMENT

```
#define FSP_SECURE_ARGUMENT
```

Macro to be used when argument to function is ignored since function call is NSC and the parameter is statically defined on the Secure side.

## Enumeration Type Documentation

## ◆ fsp\_err\_t

enum fsp_err_t	
Common error codes	
Enumerator	
FSP_ERR_ASSERTION	A critical assertion has failed.
FSP_ERR_INVALID_POINTER	Pointer points to invalid memory location.
FSP_ERR_INVALID_ARGUMENT	Invalid input parameter.
FSP_ERR_INVALID_CHANNEL	Selected channel does not exist.
FSP_ERR_INVALID_MODE	Unsupported or incorrect mode.
FSP_ERR_UNSUPPORTED	Selected mode not supported by this API.
FSP_ERR_NOT_OPEN	Requested channel is not configured or API not open.
FSP_ERR_IN_USE	Channel/peripheral is running/busy.
FSP_ERR_OUT_OF_MEMORY	Allocate more memory in the driver's cfg.h.
FSP_ERR_HW_LOCKED	Hardware is locked.
FSP_ERR_IRQ_BSP_DISABLED	IRQ not enabled in BSP.
FSP_ERR_OVERFLOW	Hardware overflow.
FSP_ERR_UNDERFLOW	Hardware underflow.
FSP_ERR_ALREADY_OPEN	Requested channel is already open in a different configuration.
FSP_ERR_APPROXIMATION	Could not set value to exact result.
FSP_ERR_CLAMPED	Value had to be limited for some reason.
FSP_ERR_INVALID_RATE	Selected rate could not be met.
FSP_ERR_ABORTED	An operation was aborted.
FSP_ERR_NOT_ENABLED	Requested operation is not enabled.
FSP_ERR_TIMEOUT	Timeout error.

FSP_ERR_INVALID_BLOCKS	Invalid number of blocks supplied.
FSP_ERR_INVALID_ADDRESS	Invalid address supplied.
FSP_ERR_INVALID_SIZE	Invalid size/length supplied for operation.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_ERASE_FAILED	Erase operation failed.
FSP_ERR_INVALID_CALL	Invalid function call is made.
FSP_ERR_INVALID_HW_CONDITION	Detected hardware is in invalid condition.
FSP_ERR_INVALID_FACTORY_FLASH	Factory flash is not available on this MCU.
FSP_ERR_INVALID_STATE	API or command not valid in the current state.
FSP_ERR_NOT_ERASED	Erase verification failed.
FSP_ERR_SECTOR_RELEASE_FAILED	Sector release failed.
FSP_ERR_NOT_INITIALIZED	Required initialization not complete.
FSP_ERR_NOT_FOUND	The requested item could not be found.
FSP_ERR_NO_CALLBACK_MEMORY	Non-secure callback memory not provided for non-secure callback.
FSP_ERR_BUFFER_EMPTY	No data available in buffer.
FSP_ERR_INTERNAL	Internal error.
FSP_ERR_WAIT_ABORTED	Wait aborted.
FSP_ERR_FRAMING	Framing error occurs.
FSP_ERR_BREAK_DETECT	Break signal detects.
FSP_ERR_PARITY	Parity error occurs.
FSP_ERR_RXBUF_OVERFLOW	Receive queue overflow.
FSP_ERR_QUEUE_UNAVAILABLE	Can't open s/w queue.
FSP_ERR_INSUFFICIENT_SPACE	Not enough space in transmission circular buffer.

FSP_ERR_INSUFFICIENT_DATA	Not enough data in receive circular buffer.
FSP_ERR_TRANSFER_ABORTED	The data transfer was aborted.
FSP_ERR_MODE_FAULT	Mode fault error.
FSP_ERR_READ_OVERFLOW	Read overflow.
FSP_ERR_SPI_PARITY	Parity error.
FSP_ERR_OVERRUN	Overrun error.
FSP_ERR_CLOCK_INACTIVE	Inactive clock specified as system clock.
FSP_ERR_CLOCK_ACTIVE	Active clock source cannot be modified without stopping first.
FSP_ERR_NOT_STABILIZED	Clock has not stabilized after its been turned on/off.
FSP_ERR_PLL_SRC_INACTIVE	PLL initialization attempted when PLL source is turned off.
FSP_ERR_OSC_STOP_DET_ENABLED	Illegal attempt to stop LOCO when Oscillation stop is enabled.
FSP_ERR_OSC_STOP_DETECTED	The Oscillation stop detection status flag is set.
FSP_ERR_OSC_STOP_CLOCK_ACTIVE	Attempt to clear Oscillation Stop Detect Status with PLL/MAIN_OSC active.
FSP_ERR_CLKOUT_EXCEEDED	Output on target output clock pin exceeds maximum supported limit.
FSP_ERR_USB_MODULE_ENABLED	USB clock configure request with USB Module enabled.
FSP_ERR_HARDWARE_TIMEOUT	A register read or write timed out.
FSP_ERR_LOW_VOLTAGE_MODE	Invalid clock setting attempted in low voltage mode.
FSP_ERR_PE_FAILURE	Unable to enter Programming mode.
FSP_ERR_CMD_LOCKED	Peripheral in command locked state.
FSP_ERR_FCLK	FCLK must be $\geq 4$ MHz.

FSP_ERR_INVALID_LINKED_ADDRESS	Function or data are linked at an invalid region of memory.
FSP_ERR_BLANK_CHECK_FAILED	Blank check operation failed.
FSP_ERR_INVALID_CAC_REF_CLOCK	Measured clock rate < reference clock rate.
FSP_ERR_CLOCK_GENERATION	Clock cannot be specified as system clock.
FSP_ERR_INVALID_TIMING_SETTING	Invalid timing parameter.
FSP_ERR_INVALID_LAYER_SETTING	Invalid layer parameter.
FSP_ERR_INVALID_ALIGNMENT	Invalid memory alignment found.
FSP_ERR_INVALID_GAMMA_SETTING	Invalid gamma correction parameter.
FSP_ERR_INVALID_LAYER_FORMAT	Invalid color format in layer.
FSP_ERR_INVALID_UPDATE_TIMING	Invalid timing for register update.
FSP_ERR_INVALID_CLUT_ACCESS	Invalid access to CLUT entry.
FSP_ERR_INVALID_FADE_SETTING	Invalid fade-in/fade-out setting.
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid gamma correction parameter.
FSP_ERR_JPEG_ERR	JPEG error.
FSP_ERR_JPEG_SOI_NOT_DETECTED	SOI not detected until EOI detected.
FSP_ERR_JPEG_SOF1_TO_SOFF_DETECTED	SOF1 to SOFF detected.
FSP_ERR_JPEG_UNSUPPORTED_PIXEL_FORMAT	Unprovided pixel format detected.
FSP_ERR_JPEG_SOF_ACCURACY_ERROR	SOF accuracy error: other than 8 detected.
FSP_ERR_JPEG_DQT_ACCURACY_ERROR	DQT accuracy error: other than 0 detected.
FSP_ERR_JPEG_COMPONENT_ERROR1	Component error 1: the number of SOF0 header components detected is other than 1, 3, or 4.
FSP_ERR_JPEG_COMPONENT_ERROR2	Component error 2: the number of components differs between SOF0 header and SOS.
FSP_ERR_JPEG_SOF0_DQT_DHT_NOT_DETECTED	SOF0, DQT, and DHT not detected when SOS detected.

FSP_ERR_JPEG_SOS_NOT_DETECTED	SOS not detected: SOS not detected until EOI detected.
FSP_ERR_JPEG_EOI_NOT_DETECTED	EOI not detected (default)
FSP_ERR_JPEG_RESTART_INTERVAL_DATA_NUMBER_ERROR	Restart interval data number error detected.
FSP_ERR_JPEG_IMAGE_SIZE_ERROR	Image size error detected.
FSP_ERR_JPEG_LAST_MCU_DATA_NUMBER_ERROR	Last MCU data number error detected.
FSP_ERR_JPEG_BLOCK_DATA_NUMBER_ERROR	Block data number error detected.
FSP_ERR_JPEG_BUFFERSIZE_NOT_ENOUGH	User provided buffer size not enough.
FSP_ERR_JPEG_UNSUPPORTED_IMAGE_SIZE	JPEG Image size is not aligned with MCU.
FSP_ERR_CALIBRATE_FAILED	Calibration failed.
FSP_ERR_IP_HARDWARE_NOT_PRESENT	Requested IP does not exist on this device.
FSP_ERR_IP_UNIT_NOT_PRESENT	Requested unit does not exist on this device.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel does not exist on this device.
FSP_ERR_NO_MORE_BUFFER	No more buffer found in the memory block pool.
FSP_ERR_ILLEGAL_BUFFER_ADDRESS	Buffer address is out of block memory pool.
FSP_ERR_INVALID_WORKBUFFER_SIZE	Work buffer size is invalid.
FSP_ERR_INVALID_MSG_BUFFER_SIZE	Message buffer size is invalid.
FSP_ERR_TOO_MANY_BUFFERS	Number of buffer is too many.
FSP_ERR_NO_SUBSCRIBER_FOUND	No message subscriber found.
FSP_ERR_MESSAGE_QUEUE_EMPTY	No message found in the message queue.
FSP_ERR_MESSAGE_QUEUE_FULL	No room for new message in the message queue.
FSP_ERR_ILLEGAL_SUBSCRIBER_LISTS	Message subscriber lists is illegal.
FSP_ERR_BUFFER_RELEASED	Buffer has been released.

FSP_ERR_D2D_ERROR_INIT	D/AVE 2D has an error in the initialization.
FSP_ERR_D2D_ERROR_DEINIT	D/AVE 2D has an error in the initialization.
FSP_ERR_D2D_ERROR_RENDERING	D/AVE 2D has an error in the rendering.
FSP_ERR_D2D_ERROR_SIZE	D/AVE 2D has an error in the rendering.
FSP_ERR_ETHER_ERROR_NO_DATA	No Data in Receive buffer.
FSP_ERR_ETHER_ERROR_LINK	ETHERC/EDMAC has an error in the Auto-negotiation.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, and transmission/reception is not enabled.
FSP_ERR_ETHER_ERROR_TRANSMIT_BUFFER_FULL	Transmit buffer is not empty.
FSP_ERR_ETHER_ERROR_FILTERING	Detect multicast frame when multicast frame filtering enable.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	ETHERC/EDMAC has an error in the phy communication.
FSP_ERR_ETHER_RECEIVE_BUFFER_ACTIVE	Receive buffer is active.
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY is not link up.
FSP_ERR_ETHER_PHY_NOT_READY	PHY has an error in the Auto-negotiation.
FSP_ERR_QUEUE_FULL	Queue is full, cannot queue another data.
FSP_ERR_QUEUE_EMPTY	Queue is empty, no data to dequeue.
FSP_ERR_CTSU_SCANNING	Scanning.
FSP_ERR_CTSU_NOT_GET_DATA	Not processed previous scan data.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.
FSP_ERR_CTSU_DIAG_NOT_YET	Diagnosis of data collected no yet.
FSP_ERR_CTSU_DIAG_LDO_OVER_VOLTAGE	Diagnosis of LDO over voltage failed.
FSP_ERR_CTSU_DIAG_CCO_HIGH	Diagnosis of CCO into 19.2uA failed.
FSP_ERR_CTSU_DIAG_CCO_LOW	Diagnosis of CCO into 2.4uA failed.

FSP_ERR_CTSU_DIAG_SSCG	Diagnosis of SSCG frequency failed.
FSP_ERR_CTSU_DIAG_DAC	Diagnosis of non-touch count value failed.
FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE	Diagnosis of LDO output voltage failed.
FSP_ERR_CTSU_DIAG_OVER_VOLTAGE	Diagnosis of over voltage detection circuit failed.
FSP_ERR_CTSU_DIAG_OVER_CURRENT	Diagnosis of over current detection circuit failed.
FSP_ERR_CTSU_DIAG_LOAD_RESISTANCE	Diagnosis of LDO internal resistance value failed.
FSP_ERR_CTSU_DIAG_CURRENT_SOURCE	Diagnosis of Current source value failed.
FSP_ERR_CTSU_DIAG_SENSCLK_GAIN	Diagnosis of SENSCLK frequency gain failed.
FSP_ERR_CTSU_DIAG_SUCLK_GAIN	Diagnosis of SUCLK frequency gain failed.
FSP_ERR_CTSU_DIAG_CLOCK_RECOVERY	Diagnosis of SUCLK clock recovery function failed.
FSP_ERR_CTSU_DIAG_CFC_GAIN	Diagnosis of CFC oscillator gain failed.
FSP_ERR_CARD_INIT_FAILED	SD card or eMMC device failed to initialize.
FSP_ERR_CARD_NOT_INSERTED	SD card not installed.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low or another operation is ongoing.
FSP_ERR_CARD_NOT_INITIALIZED	SD card was removed.
FSP_ERR_CARD_WRITE_PROTECTED	Media is write protected.
FSP_ERR_TRANSFER_BUSY	Transfer in progress.
FSP_ERR_RESPONSE	Card did not respond or responded with an error.
FSP_ERR_MEDIA_FORMAT_FAILED	Media format failed.
FSP_ERR_MEDIA_OPEN_FAILED	Media open failed.
FSP_ERR_CAN_DATA_UNAVAILABLE	No data available.
FSP_ERR_CAN_MODE_SWITCH_FAILED	Switching operation modes failed.

FSP_ERR_CAN_INIT_FAILED	Hardware initialization failed.
FSP_ERR_CAN_TRANSMIT_NOT_READY	Transmit in progress.
FSP_ERR_CAN_RECEIVE_MAILBOX	Mailbox is setup as a receive mailbox.
FSP_ERR_CAN_TRANSMIT_MAILBOX	Mailbox is setup as a transmit mailbox.
FSP_ERR_CAN_MESSAGE_LOST	Receive message has been overwritten or overrun.
FSP_ERR_CAN_TRANSMIT_FIFO_FULL	Transmit FIFO is full.
FSP_ERR_WIFI_CONFIG_FAILED	WiFi module Configuration failed.
FSP_ERR_WIFI_INIT_FAILED	WiFi module initialization failed.
FSP_ERR_WIFI_TRANSMIT_FAILED	Transmission failed.
FSP_ERR_WIFI_INVALID_MODE	API called when provisioned in client mode.
FSP_ERR_WIFI_FAILED	WiFi Failed.
FSP_ERR_WIFI_SCAN_COMPLETE	Wifi scan has completed.
FSP_ERR_CELLULAR_CONFIG_FAILED	Cellular module Configuration failed.
FSP_ERR_CELLULAR_INIT_FAILED	Cellular module initialization failed.
FSP_ERR_CELLULAR_TRANSMIT_FAILED	Transmission failed.
FSP_ERR_CELLULAR_FW_UPTODATE	Firmware is uptodate.
FSP_ERR_CELLULAR_FW_UPGRADE_FAILED	Firmware upgrade failed.
FSP_ERR_CELLULAR_FAILED	Cellular Failed.
FSP_ERR_CELLULAR_INVALID_STATE	API Called in invalid state.
FSP_ERR_CELLULAR_REGISTRATION_FAILED	Cellular Network registration failed.
FSP_ERR_BLE_FAILED	BLE operation failed.
FSP_ERR_BLE_INIT_FAILED	BLE device initialization failed.
FSP_ERR_BLE_CONFIG_FAILED	BLE device configuration failed.
FSP_ERR_BLE_PRF_ALREADY_ENABLED	BLE device Profile already enabled.

FSP_ERR_BLE_PRF_NOT_ENABLED	BLE device not enabled.
FSP_ERR_BLE_ABS_INVALID_OPERATION	Invalid operation is executed.
FSP_ERR_BLE_ABS_NOT_FOUND	Valid data or free space is not found.
FSP_ERR_CRYPTO_CONTINUE	Continue executing function.
FSP_ERR_CRYPTO_SCE_RESOURCE_CONFLICT	Hardware resource busy.
FSP_ERR_CRYPTO_SCE_FAIL	Internal I/O buffer is not empty.
FSP_ERR_CRYPTO_SCE_HRK_INVALID_INDEX	Invalid index.
FSP_ERR_CRYPTO_SCE_RETRY	Retry.
FSP_ERR_CRYPTO_SCE_VERIFY_FAIL	Verify is failed.
FSP_ERR_CRYPTO_SCE_ALREADY_OPEN	HW SCE module is already opened.
FSP_ERR_CRYPTO_NOT_OPEN	Hardware module is not initialized.
FSP_ERR_CRYPTO_UNKNOWN	Some unknown error occurred.
FSP_ERR_CRYPTO_NULL_POINTER	Null pointer input as a parameter.
FSP_ERR_CRYPTO_NOT_IMPLEMENTED	Algorithm/size not implemented.
FSP_ERR_CRYPTO_RNG_INVALID_PARAM	An invalid parameter is specified.
FSP_ERR_CRYPTO_RNG_FATAL_ERROR	A fatal error occurred.
FSP_ERR_CRYPTO_INVALID_SIZE	Size specified is invalid.
FSP_ERR_CRYPTO_INVALID_STATE	Function used in an valid state.
FSP_ERR_CRYPTO_ALREADY_OPEN	control block is already opened
FSP_ERR_CRYPTO_INSTALL_KEY_FAILED	Specified input key is invalid.
FSP_ERR_CRYPTO_AUTHENTICATION_FAILED	Authentication failed.
FSP_ERR_CRYPTO_SCE_KEY_SET_FAIL	Failure to Init Cipher.
FSP_ERR_CRYPTO_SCE_AUTHENTICATION	Authentication failed.
FSP_ERR_CRYPTO_SCE_PARAMETER	Input date is illegal.

FSP_ERR_CRYPTO_SCE_PROHIBIT_FUNCTION	An invalid function call occurred.
FSP_ERR_CRYPTO_COMMON_NOT_OPENED	Crypto Framework Common is not opened.
FSP_ERR_CRYPTO_HAL_ERROR	Crypto HAL module returned an error.
FSP_ERR_CRYPTO_KEY_BUF_NOT_ENOUGH	Key buffer size is not enough to generate a key.
FSP_ERR_CRYPTO_BUF_OVERFLOW	Attempt to write data larger than what the buffer can hold.
FSP_ERR_CRYPTO_INVALID_OPERATION_MODE	Invalid operation mode.
FSP_ERR_MESSAGE_TOO_LONG	Message for RSA encryption is too long.
FSP_ERR_RSA_DECRYPTION_ERROR	RSA Decryption error.
FSP_ERR_SENSOR_INVALID_DATA	Data is invalid.  <i>Note</i> <i>SF_CRYPTO APIs may return an error code starting from 0x10000 which is of Crypto module. Refer to sf_crypto_err.h for Crypto error codes.</i>
FSP_ERR_SENSOR_IN_STABILIZATION	Sensor is stabilizing.
FSP_ERR_SENSOR_MEASUREMENT_NOT_FINISHED	Measurement is not finished.
FSP_ERR_COMMS_BUS_NOT_OPEN	Bus is not open.

## 4.1.2 MCU Board Support Package

### BSP

#### Functions

`fsp_err_t` `R_FSP_VersionGet` (`fsp_pack_version_t` \*const p\_version)

`void` `Reset_Handler` (`void`)

`void` `Default_Handler` (`void`)

`void` `NMI_Handler` (`void`)

`void` `SystemInit` (`void`)

---

	void	<a href="#">R_BSP_WarmStart</a> ( <a href="#">bsp_warm_start_event_t</a> event)
<code>__STATIC_INLINE</code>	<a href="#">IRQn_Type</a>	<a href="#">R_FSP_CurrentIrqGet</a> (void)
<code>__STATIC_INLINE</code>	<a href="#">uint32_t</a>	<a href="#">R_FSP_SystemClockHzGet</a> ( <a href="#">fsp_priv_clock_t</a> clock)
<code>__STATIC_INLINE</code> <code>bsp_unique_id_t const *</code>		<a href="#">R_BSP_UniqueIdGet</a> ()
<code>__STATIC_INLINE</code>	void	<a href="#">R_BSP_FlashCacheDisable</a> ()
<code>__STATIC_INLINE</code>	void	<a href="#">R_BSP_FlashCacheEnable</a> ()
	void	<a href="#">R_BSP_SoftwareDelay</a> ( <a href="#">uint32_t</a> delay, <a href="#">bsp_delay_units_t</a> units)
	<a href="#">fsp_err_t</a>	<a href="#">R_BSP_GroupIrqWrite</a> ( <a href="#">bsp_grp_irq_t</a> irq, void(*p_callback)( <a href="#">bsp_grp_irq_t</a> irq))
	void	<a href="#">R_BSP_RegisterProtectEnable</a> ( <a href="#">bsp_reg_protect_t</a> regs_to_protect)
	void	<a href="#">R_BSP_RegisterProtectDisable</a> ( <a href="#">bsp_reg_protect_t</a> regs_to_unprotect)

## Detailed Description

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The BSP is responsible for getting the MCU from reset to the user's application. Before reaching the user's application, the BSP sets up the stacks, heap, clocks, interrupts, C runtime environment, and stack monitor.

- [BSP Features](#)
- [BSP Clock Configuration](#)
- [System Interrupts](#)
- [Group Interrupts](#)
- [External and Peripheral Interrupts](#)
- [Error Logging](#)
- [BSP Weak Symbols](#)
- [Warm Start Callbacks](#)
- [C Runtime Initialization](#)
- [Register Protection](#)
- [ID Codes](#)
- [Software Delay](#)
- [Octal-SPI Clock Update](#)
- [Board Specific Features](#)
- [Configuration](#)

## Overview

### BSP Features

### BSP Clock Configuration

All system clocks are set up during BSP initialization based on the settings in `bsp_clock_cfg.h`. These settings are derived from clock configuration information provided from the RA Configuration editor **Clocks** tab.

- Clock configuration is performed prior to initializing the C runtime environment to speed up the startup process, as it is possible to start up on a relatively slow (that is, 32 kHz) clock.
- The BSP implements the required delays to allow the selected clock to stabilize.
- The BSP will configure the CMSIS `SystemCoreClock` variable after clock initialization with the current system clock frequency.

## System Interrupts

As RA MCUs are based on the Cortex-M ARM architecture, the NVIC Nested Vectored Interrupt Controller (NVIC) handles exceptions and interrupt configuration, prioritization and interrupt masking. In the ARM architecture, the NVIC handles exceptions. Some exceptions are known as System Exceptions. System exceptions are statically located at the "top" of the vector table and occupy vector numbers 1 to 15. Vector zero is reserved for the MSP Main Stack Pointer (MSP). The remaining 15 system exceptions are shown below:

- Reset
- NMI
- Cortex-M4 Hard Fault Handler
- Cortex-M4 MPU Fault Handler
- Cortex-M4 Bus Fault Handler
- Cortex-M4 Usage Fault Handler
- Reserved
- Reserved
- Reserved
- Reserved
- Cortex-M4 SVCALL Handler
- Cortex-M4 Debug Monitor Handler
- Reserved
- Cortex-M4 PendSV Handler
- Cortex-M4 SysTick Handler

NMI and Hard Fault exceptions are enabled out of reset and have fixed priorities. Other exceptions have configurable priorities and some can be disabled.

## Group Interrupts

Group interrupt is the term used to describe the 12 sources that can trigger the Non-Maskable Interrupt (NMI). When an NMI occurs the NMI Handler examines the NMISR (status register) to determine the source of the interrupt. NMI interrupts take precedence over all interrupts, are usable only as CPU interrupts, and cannot activate the RA peripherals Data Transfer Controller (DTC) or Direct Memory Access Controller (DMAC).

Possible group interrupt sources include:

- IWDT Underflow/Refresh Error
- WDT Underflow/Refresh Error
- Voltage-Monitoring 1 Interrupt
- Voltage-Monitoring 2 Interrupt
- VBATT monitor Interrupt
- Oscillation Stop is detected
- NMI pin

- RAM Parity Error
- RAM ECC Error
- MPU Bus Slave Error
- MPU Bus Master Error
- MPU Stack Error
- TrustZone Filter Error A user may enable notification for one or more group interrupts by registering a callback using the BSP API function [R\\_BSP\\_GroupIrqWrite\(\)](#). When an NMI interrupt occurs, the NMI handler checks to see if there is a callback registered for the cause of the interrupt and if so calls the registered callback function.

## External and Peripheral Interrupts

User configurable interrupts begin with slot 16. These may be external, or peripheral generated interrupts.

Although the number of available slots for the NVIC interrupt vector table may seem small, the BSP defines up to 512 events that are capable of generating an interrupt. By using Event Mapping, the BSP maps user-enabled events to NVIC interrupts. For an RA6M3 MCU, only 96 of these events may be active at any one time, but the user has flexibility by choosing which events generate the active event.

By allowing the user to select only the events they are interested in as interrupt sources, we are able to provide an interrupt service routine that is fast and event specific.

For example, on other microcontrollers a standard NVIC interrupt vector table might contain a single vector entry for the SCIO (Serial Communications Interface) peripheral. The interrupt service routine for this would have to check a status register for the 'real' source of the interrupt. In the RA implementation there is a vector entry for each of the SCIO events that we are interested in.

## BSP Weak Symbols

You might wonder how the BSP is able to place ISR addresses in the NVIC table without the user having explicitly defined one. All that is required by the BSP is that the interrupt event be given a priority.

This is accomplished through the use of the 'weak' attribute. The weak attribute causes the declaration to be emitted as a weak symbol rather than a global. A weak symbol is one that can be overridden by an accompanying strong reference with the same name. When the BSP declares a function as weak, user code can define the same function and it will be used in place of the BSP function. By defining all possible interrupt sources as weak, the vector table can be built at compile time and any user declarations (strong references) will be used at runtime.

Weak symbols are supported for ELF targets and also for a.out targets when using the GNU assembler and linker.

Note that in CMSIS system.c, there is also a weak definition (and a function body) for the Warm Start callback function [R\\_BSP\\_WarmStart\(\)](#). Because this function is defined in the same file as the weak declaration, it will be called as the 'default' implementation. The function may be overridden by the user by copying the body into their user application and modifying it as necessary. The linker identifies this as the 'strong' reference and uses it.

## Warm Start Callbacks

As the BSP is in the process of bringing up the board out of reset, there are three points where the user can request a callback. These are defined as the 'Pre Clock Init', 'Post Clock Init' and 'Post C'

warm start callbacks.

As described above, this function is already weakly defined as `R_BSP_WarmStart()`, so it is a simple matter of redefining the function or copying the existing body from CMSIS `system.c` into the application code to get a callback. `R_BSP_WarmStart()` takes an event parameter of type `bsp_warm_start_event_t` which describes the type of warm start callback being made.

This function is not enabled/disabled and is always called for both events as part of the BSP startup. Therefore it needs a function body, which will not be called if the user is overriding it. The function body is located in `system.c`. To use this function just copy this function into your own code and modify it to meet your needs.

## C Runtime Initialization

This BSP configuration allows the user to skip the FSP C runtime initialization code by setting the "C Runtime Initialization" to "Disabled" on the BSP tab of the RA Configuration editor. Disabling this option is useful in cases where a non-standard linker script is being used or other modifications to the runtime initialization are desired. If this macro is disabled, the user must use the 'Post Clock Init' event from the warm start (described above) to run their own runtime initialization code.

## Heap Allocation

The relatively low amount of on-chip SRAM available and lack of memory protection in an MCU means that heap use must be very carefully controlled to avoid memory leaks, overruns and attempted overallocation. Further, many RTOSes provide their own dynamic memory allocation system. For these reasons the default heap size is set at 0 bytes, effectively disabling dynamic memory. If it is required for an application setting a positive value to the "Heap size (bytes)" option in the RA Common configurations on the **BSP** tab will allocate a heap.

### Note

*When using `printf/sprintf` (and other variants) to output floating point numbers a heap is required. A minimum size of 0x1000 (4096) bytes is recommended when starting development in this case.*

## Error Logging

When error logging is enabled, the error logging function can be redefined on the command line by defining `FSP_ERROR_LOG(err)` to the desired function call. The default function implementation is `FSP_ERROR_LOG(err)=fsp_error_log(err, FILE, LINE)`. This implementation uses the predefined macros **FILE** and **LINE** to help identify the location where the error occurred. Removing the line from the function call can reduce code size when error logging is enabled. Some compilers may support other predefined macros like **FUNCTION**, which could be helpful for customizing the error logger.

## Register Protection

The BSP register protection functions utilize reference counters to ensure that an application which has specified a certain register and subsequently calls another function doesn't have its register protection settings inadvertently modified.

Each time `R_BSP_RegisterProtectDisable()` is called, the respective reference counter is incremented.

Each time `R_BSP_RegisterProtectEnable()` is called, the respective reference counter is decremented.

Both functions will only modify the protection state if their reference counter is zero.

```
/* Enable writing to protected CGC registers */
R_BSP_RegisterProtectDisable(BSP_REG_PROTECT_CGC);
/* Insert code to modify protected CGC registers. */
/* Disable writing to protected CGC registers */
R_BSP_RegisterProtectEnable(BSP_REG_PROTECT_CGC);
```

## ID Codes

The ID code is a 16-byte value that can be used to protect the MCU from being connected to a debugger or from connecting in Serial Boot Mode. There are different settings that can be set for the ID code; please refer to the hardware manual for your device for available options.

## Software Delay

Implements a blocking software delay. A delay can be specified in microseconds, milliseconds or seconds. The delay is implemented based on the system clock rate.

```
/* Delay at least 1 second. Depending on the number of wait states required for the
region of memory
 * that the software_delay_loop has been linked in this could take longer. The
default is 4 cycles per loop.
 * This can be modified by redefining DELAY_LOOP_CYCLES. BSP_DELAY_UNITS_SECONDS,
BSP_DELAY_UNITS_MILLISECONDS,
 * and BSP_DELAY_UNITS_MICROSECONDS can all be used with R_BSP_SoftwareDelay. */
R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_SECONDS);
```

## Critical Section Macros

Implements a critical section. Some MCUs (MCUs with the BASEPRI register) support allowing high priority interrupts to execute during critical sections. On these MCUs, interrupts with priority less than or equal to `BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION` are not serviced in critical sections. Interrupts with higher priority than `BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION` still execute in critical sections.

```
FSP_CRITICAL_SECTION_DEFINE;
/* Store the current interrupt posture. */
FSP_CRITICAL_SECTION_ENTER;
/* Interrupts cannot run in this section unless their priority is less than
BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION. */
/* Restore saved interrupt posture. */
```

```
FSP_CRITICAL_SECTION_EXIT;
```

## OctaClock Update

Supports changing the Octal-SPI Clock (OCTACLK) during runtime if supported by the MCU. The OCTACLK source and clock divisor can be updated. It is user's responsibility to ensure the selected clock source is running before attempting to update OCTACLK.

## Sealing the Main Stack (TrustZone Secure Projects)

In TrustZone secure projects, the BSP seals the main stack by placing the value 0xFE5EDA5 above the stack top. For more information, refer to section 3.5 "Sealing a Stack" in "Secure software guidelines for ARMv8-M": <https://developer.arm.com/documentation/100720/0300>.

## Board Specific Features

The BSP will call the board's initialization function (bsp\_init) which can initialize board specific features. Possible board features are listed below.

Board Feature	Description
SDRAM Support	The BSP will initialize SDRAM if the board supports it
QSPI Support	The BSP will initialize QSPI if the board supports it and put it into ROM mode. Use the R_QSPI module to write and erase the QSPI chip.

## Configuration

The BSP is heavily data driven with most features and functionality being configured based on the content from configuration files. Configuration files represent the settings specified by the user and are generated when the project is built and/or when the Generate Project Content button is clicked in the RA Configuration editor.

### Build Time Configurations for fsp\_common

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_cfg.h:

Configuration	Options	Default	Description
Main stack size (bytes)	Value must be an integer multiple of 8 and between 8 and 0xFFFFFFFF	0x400	Set the size of the main program stack.  NOTE: This entry is for the main stack. When using an RTOS, thread stacks can be configured in the properties for each

Heap size (bytes)	Value must be 0 or an integer multiple of 8 between 8 and 0xFFFFFFFF.	0	thread.  The main heap is disabled by default. Set the heap size to a positive integer divisible by 8 to enable it.  A minimum of 4K (0x1000) is recommended if standard library functions are to be used.
MCU Vcc (mV)	Value must between 0 and 5500 (5.5V)	3300	Some peripherals require different settings based on the supplied voltage. Entering Vcc here (in mV) allows the relevant driver modules to configure the associated peripherals accordingly.
Parameter checking	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	When enabled, parameter checking for the BSP is turned on. In addition, any modules whose parameter checking configuration is set to 'Default (BSP)' will perform parameter checking as well.
Assert Failures	<ul style="list-style-type: none"> <li>Return FSP_ERR_ASSERTION</li> <li>Call fsp_error_log then Return FSP_ERR_ASSERTION</li> <li>Use assert() to Halt Execution</li> <li>Disable checks that would return FSP_ERR_ASSERTION</li> </ul>	Return FSP_ERR_ASSERTION	Define the behavior of the <a href="#">FSP_ASSERT()</a> macro.
Error Log	<ul style="list-style-type: none"> <li>No Error Log</li> <li>Errors Logged via fsp_error_log</li> </ul>	No Error Log	Specify error logging behavior.
Soft Reset	<ul style="list-style-type: none"> <li>Disabled</li> </ul>	Disabled	Support for soft reset.

	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>		If disabled, registers are assumed to be set to their default value during startup.
Main Oscillator Populated	<ul style="list-style-type: none"> <li>• Populated</li> <li>• Not Populated</li> </ul>	Populated	Select whether or not there is a main oscillator (XTAL) on the board. This setting can be overridden in board_cfg.h.
PFS Protect	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Keep the PFS registers locked when they are not being modified. If disabled they will be unlocked during startup.
C Runtime Initialization	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Select if the C runtime initialization in the BSP is to be used. If disabled, use the BSP_WARM_START_POST_CLOCK event to run user defined equivalent.
Main Oscillator Clock Source	<ul style="list-style-type: none"> <li>• External Oscillator</li> <li>• Crystal or Resonator</li> </ul>	Crystal or Resonator	Select the main oscillator clock source. This setting can be overridden in board_cfg.h
Subclock Populated	<ul style="list-style-type: none"> <li>• Populated</li> <li>• Not Populated</li> </ul>	Populated	Select whether or not there is a subclock crystal on the board. This setting can be overridden in board_cfg.h.
Subclock Drive (Drive capacitance availability varies by MCU)	<ul style="list-style-type: none"> <li>• Standard/Normal mode</li> <li>• Low/Low power mode 1</li> <li>• Low power mode 2</li> <li>• Low power mode 3</li> </ul>	Standard/Normal mode	Select the subclock oscillator drive capacitance. This setting can be overridden in board_cfg.h
Subclock Stabilization Time (ms)	Value must between 0 and 10000	1000	Select the subclock oscillator stabilization time. This is only used in the startup code if the subclock is selected as the system clock on the Clocks tab or if the HOCO FLL function is enabled.

This setting can be overridden in board\_cfg.h

## Modules

RA2A1

RA2E1

RA2L1

RA4M1

RA4M2

RA4M3

RA4W1

RA6M1

RA6M2

RA6M3

RA6M4

RA6M5

RA6T1

## Macros

#define BSP\_IRQ\_DISABLED

#define FSP\_LOG\_PRINT(X)

#define FSP\_RETURN(err)

#define FSP\_ERROR\_LOG(err)

#define FSP\_ASSERT(a)

#define FSP\_ERROR\_RETURN(a, err)

#define FSP\_CRITICAL\_SECTION\_ENTER

#define FSP\_CRITICAL\_SECTION\_EXIT

```
#define FSP_INVALID_VECTOR
```

```
#define BSP_CFG_HANDLE_UNRECOVERABLE_ERROR(x)
```

```
#define BSP_STACK_ALIGNMENT
```

```
#define R_BSP_MODULE_START(ip, channel)
```

```
#define R_BSP_MODULE_STOP(ip, channel)
```

## Enumerations

```
enum fsp_ip_t
```

```
enum fsp_signal_t
```

```
enum bsp_warm_start_event_t
```

```
enum bsp_delay_units_t
```

```
enum bsp_grp_irq_t
```

```
enum bsp_reg_protect_t
```

## Variables

```
uint32_t SystemCoreClock
```

## Macro Definition Documentation

### ◆ BSP\_IRQ\_DISABLED

```
#define BSP_IRQ_DISABLED
```

Used to signify that an ELC event is not able to be used as an interrupt.

### ◆ FSP\_LOG\_PRINT

```
#define FSP_LOG_PRINT ( X)
```

Macro that can be defined in order to enable logging in FSP modules.

### ◆ FSP\_RETURN

```
#define FSP_RETURN ( err)
```

Macro to log and return error without an assertion.

**◆ FSP\_ERROR\_LOG**

```
#define FSP_ERROR_LOG ( err)
```

This function is called before returning an error code. To stop on a runtime error, define `fsp_error_log` in user code and do required debugging (breakpoints, stack dump, etc) in this function.

**◆ FSP\_ASSERT**

```
#define FSP_ASSERT ( a)
```

Default assertion calls `FSP_ERROR_RETURN` if condition "a" is false. Used to identify incorrect use of API's in FSP functions.

**◆ FSP\_ERROR\_RETURN**

```
#define FSP_ERROR_RETURN ( a, err )
```

All FSP error codes are returned using this macro. Calls `FSP_ERROR_LOG` function if condition "a" is false. Used to identify runtime errors in FSP functions.

**◆ FSP\_CRITICAL\_SECTION\_ENTER**

```
#define FSP_CRITICAL_SECTION_ENTER
```

This macro temporarily saves the current interrupt state and disables interrupts.

**◆ FSP\_CRITICAL\_SECTION\_EXIT**

```
#define FSP_CRITICAL_SECTION_EXIT
```

This macro restores the previously saved interrupt state, reenabling interrupts.

**◆ FSP\_INVALID\_VECTOR**

```
#define FSP_INVALID_VECTOR
```

Used to signify that the requested IRQ vector is not defined in this system.

### ◆ BSP\_CFG\_HANDLE\_UNRECOVERABLE\_ERROR

```
#define BSP_CFG_HANDLE_UNRECOVERABLE_ERROR ( x)
```

In the event of an unrecoverable error the BSP will by default call the `__BKPT()` intrinsic function which will alert the user of the error. The user can override this default behavior by defining their own `BSP_CFG_HANDLE_UNRECOVERABLE_ERROR` macro.

### ◆ BSP\_STACK\_ALIGNMENT

```
#define BSP_STACK_ALIGNMENT
```

Stacks (and heap) must be sized and aligned to an integer multiple of this number.

### ◆ R\_BSP\_MODULE\_START

```
#define R_BSP_MODULE_START ( ip, channel )
```

Cancels the module stop state.

#### Parameters

ip	fsp_ip_t enum value for the module to be stopped
channel	The channel. Use channel 0 for modules without channels.

### ◆ R\_BSP\_MODULE\_STOP

```
#define R_BSP_MODULE_STOP ( ip, channel )
```

Enables the module stop state.

#### Parameters

ip	fsp_ip_t enum value for the module to be stopped
channel	The channel. Use channel 0 for modules without channels.

## Enumeration Type Documentation

## ◆ fsp\_ip\_t

enum fsp_ip_t	
Available modules.	
Enumerator	
FSP_IP_CFLASH	Code Flash.
FSP_IP_DFLASH	Data Flash.
FSP_IP_RAM	RAM.
FSP_IP_LVD	Low Voltage Detection.
FSP_IP_CGC	Clock Generation Circuit.
FSP_IP_LPM	Low Power Modes.
FSP_IP_FCU	Flash Control Unit.
FSP_IP_ICU	Interrupt Control Unit.
FSP_IP_DMAC	DMA Controller.
FSP_IP_DTC	Data Transfer Controller.
FSP_IP_IOPORT	I/O Ports.
FSP_IP_PFS	Pin Function Select.
FSP_IP_ELC	Event Link Controller.
FSP_IP_MPU	Memory Protection Unit.
FSP_IP_MSTP	Module Stop.
FSP_IP_MMF	Memory Mirror Function.
FSP_IP_KEY	Key Interrupt Function.
FSP_IP_CAC	Clock Frequency Accuracy Measurement Circuit.
FSP_IP_DOC	Data Operation Circuit.
FSP_IP_CRC	Cyclic Redundancy Check Calculator.
FSP_IP_SCI	Serial Communications Interface.

FSP_IP_IIC	I2C Bus Interface.
FSP_IP_SPI	Serial Peripheral Interface.
FSP_IP_CTSU	Capacitive Touch Sensing Unit.
FSP_IP_SCE	Secure Cryptographic Engine.
FSP_IP_SLCDC	Segment LCD Controller.
FSP_IP_AES	Advanced Encryption Standard.
FSP_IP_TRNG	True Random Number Generator.
FSP_IP_FCACHE	Flash Cache.
FSP_IP_SRAM	SRAM.
FSP_IP_ADC	A/D Converter.
FSP_IP_DAC	12-Bit D/A Converter
FSP_IP_TSN	Temperature Sensor.
FSP_IP_DAAD	D/A A/D Synchronous Unit.
FSP_IP_ACMPHS	High Speed Analog Comparator.
FSP_IP_ACMPLP	Low Power Analog Comparator.
FSP_IP_OPAMP	Operational Amplifier.
FSP_IP_SDADC	Sigma Delta A/D Converter.
FSP_IP_RTC	Real Time Clock.
FSP_IP_WDT	Watch Dog Timer.
FSP_IP_IWDT	Independent Watch Dog Timer.
FSP_IP_GPT	General PWM Timer.
FSP_IP_POEG	Port Output Enable for GPT.
FSP_IP_OPS	Output Phase Switch.
FSP_IP_AGT	Asynchronous General-Purpose Timer.

FSP_IP_CAN	Controller Area Network.
FSP_IP_IRDA	Infrared Data Association.
FSP_IP_QSPI	Quad Serial Peripheral Interface.
FSP_IP_USBFS	USB Full Speed.
FSP_IP_SDHI	SD/MMC Host Interface.
FSP_IP_SRC	Sampling Rate Converter.
FSP_IP_SSI	Serial Sound Interface.
FSP_IP_DALI	Digital Addressable Lighting Interface.
FSP_IP_ETHER	Ethernet MAC Controller.
FSP_IP_EDMAC	Ethernet DMA Controller.
FSP_IP_EPTPC	Ethernet PTP Controller.
FSP_IP_PDC	Parallel Data Capture Unit.
FSP_IP_GLCDC	Graphics LCD Controller.
FSP_IP_DRW	2D Drawing Engine
FSP_IP_JPEG	JPEG.
FSP_IP_DAC8	8-Bit D/A Converter
FSP_IP_USBHS	USB High Speed.
FSP_IP_OSPI	Octa Serial Peripheral Interface.
FSP_IP_CEC	HDMI CEC.

◆ **fsp\_signal\_t**

enum fsp_signal_t	
Signals that can be mapped to an interrupt.	
Enumerator	
FSP_SIGNAL_ADC_COMPARE_MATCH	ADC COMPARE MATCH.
FSP_SIGNAL_ADC_COMPARE_MISMATCH	ADC COMPARE MISMATCH.
FSP_SIGNAL_ADC_SCAN_END	ADC SCAN END.
FSP_SIGNAL_ADC_SCAN_END_B	ADC SCAN END B.
FSP_SIGNAL_ADC_WINDOW_A	ADC WINDOW A.
FSP_SIGNAL_ADC_WINDOW_B	ADC WINDOW B.
FSP_SIGNAL_AES_RDREQ	AES RDREQ.
FSP_SIGNAL_AES_WRREQ	AES WRREQ.
FSP_SIGNAL_AGT_COMPARE_A	AGT COMPARE A.
FSP_SIGNAL_AGT_COMPARE_B	AGT COMPARE B.
FSP_SIGNAL_AGT_INT	AGT INT.
FSP_SIGNAL_CAC_FREQUENCY_ERROR	CAC FREQUENCY ERROR.
FSP_SIGNAL_CAC_MEASUREMENT_END	CAC MEASUREMENT END.
FSP_SIGNAL_CAC_OVERFLOW	CAC OVERFLOW.
FSP_SIGNAL_CAN_ERROR	CAN ERROR.
FSP_SIGNAL_CAN_FIFO_RX	CAN FIFO RX.
FSP_SIGNAL_CAN_FIFO_TX	CAN FIFO TX.
FSP_SIGNAL_CAN_MAILBOX_RX	CAN MAILBOX RX.
FSP_SIGNAL_CAN_MAILBOX_TX	CAN MAILBOX TX.
FSP_SIGNAL_CGC_MOSC_STOP	CGC MOSC STOP.
FSP_SIGNAL_LPM_SNOOZE_REQUEST	LPM SNOOZE REQUEST.

FSP_SIGNAL_LVD_LVD1	LVD LVD1.
FSP_SIGNAL_LVD_LVD2	LVD LVD2.
FSP_SIGNAL_VBATT_LVD	VBATT LVD.
FSP_SIGNAL_LVD_VBATT	LVD VBATT.
FSP_SIGNAL_ACMPHS_INT	ACMPHS INT.
FSP_SIGNAL_ACMPLP_INT	ACMPLP INT.
FSP_SIGNAL_CTSU_END	CTSU END.
FSP_SIGNAL_CTSU_READ	CTSU READ.
FSP_SIGNAL_CTSU_WRITE	CTSU WRITE.
FSP_SIGNAL_DALI_DEI	DALI DEI.
FSP_SIGNAL_DALI_CLI	DALI CLI.
FSP_SIGNAL_DALI_SDI	DALI SDI.
FSP_SIGNAL_DALI_BPI	DALI BPI.
FSP_SIGNAL_DALI_FEI	DALI FEI.
FSP_SIGNAL_DALI_SDI_OR_BPI	DALI SDI OR BPI.
FSP_SIGNAL_DMAC_INT	DMAC INT.
FSP_SIGNAL_DOC_INT	DOC INT.
FSP_SIGNAL_DRW_INT	DRW INT.
FSP_SIGNAL_DTC_COMPLETE	DTC COMPLETE.
FSP_SIGNAL_DTC_END	DTC END.
FSP_SIGNAL_EDMAC_EINT	EDMAC EINT.
FSP_SIGNAL_ELC_SOFTWARE_EVENT_0	ELC SOFTWARE EVENT 0.
FSP_SIGNAL_ELC_SOFTWARE_EVENT_1	ELC SOFTWARE EVENT 1.
FSP_SIGNAL_EPTPC_IPLS	EPTPC IPLS.

FSP_SIGNAL_EPTPC_MINT	EPTPC MINT.
FSP_SIGNAL_EPTPC_PINT	EPTPC PINT.
FSP_SIGNAL_EPTPC_TIMER0_FALL	EPTPC TIMER0 FALL.
FSP_SIGNAL_EPTPC_TIMER0_RISE	EPTPC TIMER0 RISE.
FSP_SIGNAL_EPTPC_TIMER1_FALL	EPTPC TIMER1 FALL.
FSP_SIGNAL_EPTPC_TIMER1_RISE	EPTPC TIMER1 RISE.
FSP_SIGNAL_EPTPC_TIMER2_FALL	EPTPC TIMER2 FALL.
FSP_SIGNAL_EPTPC_TIMER2_RISE	EPTPC TIMER2 RISE.
FSP_SIGNAL_EPTPC_TIMER3_FALL	EPTPC TIMER3 FALL.
FSP_SIGNAL_EPTPC_TIMER3_RISE	EPTPC TIMER3 RISE.
FSP_SIGNAL_EPTPC_TIMER4_FALL	EPTPC TIMER4 FALL.
FSP_SIGNAL_EPTPC_TIMER4_RISE	EPTPC TIMER4 RISE.
FSP_SIGNAL_EPTPC_TIMER5_FALL	EPTPC TIMER5 FALL.
FSP_SIGNAL_EPTPC_TIMER5_RISE	EPTPC TIMER5 RISE.
FSP_SIGNAL_FCU_FIFERR	FCU FIFERR.
FSP_SIGNAL_FCU_FRDYI	FCU FRDYI.
FSP_SIGNAL_GLCDC_LINE_DETECT	GLCDC LINE DETECT.
FSP_SIGNAL_GLCDC_UNDERFLOW_1	GLCDC UNDERFLOW 1.
FSP_SIGNAL_GLCDC_UNDERFLOW_2	GLCDC UNDERFLOW 2.
FSP_SIGNAL_GPT_CAPTURE_COMPARE_A	GPT CAPTURE COMPARE A.
FSP_SIGNAL_GPT_CAPTURE_COMPARE_B	GPT CAPTURE COMPARE B.
FSP_SIGNAL_GPT_COMPARE_C	GPT COMPARE C.
FSP_SIGNAL_GPT_COMPARE_D	GPT COMPARE D.
FSP_SIGNAL_GPT_COMPARE_E	GPT COMPARE E.

FSP_SIGNAL_GPT_COMPARE_F	GPT COMPARE F.
FSP_SIGNAL_GPT_COUNTER_OVERFLOW	GPT COUNTER OVERFLOW.
FSP_SIGNAL_GPT_COUNTER_UNDERFLOW	GPT COUNTER UNDERFLOW.
FSP_SIGNAL_GPT_AD_TRIG_A	GPT AD TRIG A.
FSP_SIGNAL_GPT_AD_TRIG_B	GPT AD TRIG B.
FSP_SIGNAL_OPS_UVW_EDGE	OPS UVW EDGE.
FSP_SIGNAL_ICU_IRQ0	ICU IRQ0.
FSP_SIGNAL_ICU_IRQ1	ICU IRQ1.
FSP_SIGNAL_ICU_IRQ2	ICU IRQ2.
FSP_SIGNAL_ICU_IRQ3	ICU IRQ3.
FSP_SIGNAL_ICU_IRQ4	ICU IRQ4.
FSP_SIGNAL_ICU_IRQ5	ICU IRQ5.
FSP_SIGNAL_ICU_IRQ6	ICU IRQ6.
FSP_SIGNAL_ICU_IRQ7	ICU IRQ7.
FSP_SIGNAL_ICU_IRQ8	ICU IRQ8.
FSP_SIGNAL_ICU_IRQ9	ICU IRQ9.
FSP_SIGNAL_ICU_IRQ10	ICU IRQ10.
FSP_SIGNAL_ICU_IRQ11	ICU IRQ11.
FSP_SIGNAL_ICU_IRQ12	ICU IRQ12.
FSP_SIGNAL_ICU_IRQ13	ICU IRQ13.
FSP_SIGNAL_ICU_IRQ14	ICU IRQ14.
FSP_SIGNAL_ICU_IRQ15	ICU IRQ15.
FSP_SIGNAL_ICU_SNOOZE_CANCEL	ICU SNOOZE CANCEL.
FSP_SIGNAL_IIC_ERI	IIC ERI.

FSP_SIGNAL_IIC_RXI	IIC RXI.
FSP_SIGNAL_IIC_TEI	IIC TEI.
FSP_SIGNAL_IIC_TXI	IIC TXI.
FSP_SIGNAL_IIC_WUI	IIC WUI.
FSP_SIGNAL_IOPORT_EVENT_1	IOPORT EVENT 1.
FSP_SIGNAL_IOPORT_EVENT_2	IOPORT EVENT 2.
FSP_SIGNAL_IOPORT_EVENT_3	IOPORT EVENT 3.
FSP_SIGNAL_IOPORT_EVENT_4	IOPORT EVENT 4.
FSP_SIGNAL_IWDT_UNDERFLOW	IWDT UNDERFLOW.
FSP_SIGNAL_JPEG_JDTI	JPEG JDTI.
FSP_SIGNAL_JPEG_JEDI	JPEG JEDI.
FSP_SIGNAL_KEY_INT	KEY INT.
FSP_SIGNAL_PDC_FRAME_END	PDC FRAME END.
FSP_SIGNAL_PDC_INT	PDC INT.
FSP_SIGNAL_PDC_RECEIVE_DATA_READY	PDC RECEIVE DATA READY.
FSP_SIGNAL_POEG_EVENT	POEG EVENT.
FSP_SIGNAL_QSPI_INT	QSPI INT.
FSP_SIGNAL_RTC_ALARM	RTC ALARM.
FSP_SIGNAL_RTC_PERIOD	RTC PERIOD.
FSP_SIGNAL_RTC_CARRY	RTC CARRY.
FSP_SIGNAL_SCE_INTEGRATE_RDRDY	SCE INTEGRATE RDRDY.
FSP_SIGNAL_SCE_INTEGRATE_WRRDY	SCE INTEGRATE WRRDY.
FSP_SIGNAL_SCE_LONG_PLG	SCE LONG PLG.
FSP_SIGNAL_SCE_PROC_BUSY	SCE PROC BUSY.

FSP_SIGNAL_SCE_RDRDY_0	SCE RDRDY 0.
FSP_SIGNAL_SCE_RDRDY_1	SCE RDRDY 1.
FSP_SIGNAL_SCE_ROMOK	SCE ROMOK.
FSP_SIGNAL_SCE_TEST_BUSY	SCE TEST BUSY.
FSP_SIGNAL_SCE_WRRDY_0	SCE WRRDY 0.
FSP_SIGNAL_SCE_WRRDY_1	SCE WRRDY 1.
FSP_SIGNAL_SCE_WRRDY_4	SCE WRRDY 4.
FSP_SIGNAL_SCI_AM	SCI AM.
FSP_SIGNAL_SCI_ERI	SCI ERI.
FSP_SIGNAL_SCI_RXI	SCI RXI.
FSP_SIGNAL_SCI_RXI_OR_ERI	SCI RXI OR ERI.
FSP_SIGNAL_SCI_TEI	SCI TEI.
FSP_SIGNAL_SCI_TXI	SCI TXI.
FSP_SIGNAL_SDADC_ADI	SDADC ADI.
FSP_SIGNAL_SDADC_SCANEND	SDADC SCANEND.
FSP_SIGNAL_SDADC_CALIEND	SDADC CALIEND.
FSP_SIGNAL_SDHIMMC_ACCS	SDHIMMC ACCS.
FSP_SIGNAL_SDHIMMC_CARD	SDHIMMC CARD.
FSP_SIGNAL_SDHIMMC_DMA_REQ	SDHIMMC DMA REQ.
FSP_SIGNAL_SDHIMMC_SDIO	SDHIMMC SDIO.
FSP_SIGNAL_SPI_ERI	SPI ERI.
FSP_SIGNAL_SPI_IDLE	SPI IDLE.
FSP_SIGNAL_SPI_RXI	SPI RXI.
FSP_SIGNAL_SPI_TEI	SPI TEI.

FSP_SIGNAL_SPI_TXI	SPI TXI.
FSP_SIGNAL_SRC_CONVERSION_END	SRC CONVERSION END.
FSP_SIGNAL_SRC_INPUT_FIFO_EMPTY	SRC INPUT FIFO EMPTY.
FSP_SIGNAL_SRC_OUTPUT_FIFO_FULL	SRC OUTPUT FIFO FULL.
FSP_SIGNAL_SRC_OUTPUT_FIFO_OVERFLOW	SRC OUTPUT FIFO OVERFLOW.
FSP_SIGNAL_SRC_OUTPUT_FIFO_UNDERFLOW	SRC OUTPUT FIFO UNDERFLOW.
FSP_SIGNAL_SSI_INT	SSI INT.
FSP_SIGNAL_SSI_RXI	SSI RXI.
FSP_SIGNAL_SSI_TXI	SSI TXI.
FSP_SIGNAL_SSI_TXI_RXI	SSI TXI RXI.
FSP_SIGNAL_TRNG_RDREQ	TRNG RDREQ.
FSP_SIGNAL_USB_FIFO_0	USB FIFO 0.
FSP_SIGNAL_USB_FIFO_1	USB FIFO 1.
FSP_SIGNAL_USB_INT	USB INT.
FSP_SIGNAL_USB_RESUME	USB RESUME.
FSP_SIGNAL_USB_USB_INT_RESUME	USB USB INT RESUME.
FSP_SIGNAL_WDT_UNDERFLOW	WDT UNDERFLOW.

◆ **bsp\_warm\_start\_event\_t**

enum <code>bsp_warm_start_event_t</code>	
Different warm start entry locations in the BSP.	
Enumerator	
<code>BSP_WARM_START_RESET</code>	Called almost immediately after reset. No C runtime environment, clocks, or IRQs.
<code>BSP_WARM_START_POST_CLOCK</code>	Called after clock initialization. No C runtime environment or IRQs.
<code>BSP_WARM_START_POST_C</code>	Called after clocks and C runtime environment have been set up.

◆ **bsp\_delay\_units\_t**

enum <code>bsp_delay_units_t</code>	
Available delay units for <code>R_BSP_SoftwareDelay()</code> . These are ultimately used to calculate a total # of microseconds	
Enumerator	
<code>BSP_DELAY_UNITS_SECONDS</code>	Requested delay amount is in seconds.
<code>BSP_DELAY_UNITS_MILLISECONDS</code>	Requested delay amount is in milliseconds.
<code>BSP_DELAY_UNITS_MICROSECONDS</code>	Requested delay amount is in microseconds.

◆ **bsp\_grp\_irq\_t**

enum <code>bsp_grp_irq_t</code>	
Which interrupts can have callbacks registered.	
Enumerator	
<code>BSP_GRP_IRQ_IWDT_ERROR</code>	IWDT underflow/refresh error has occurred.
<code>BSP_GRP_IRQ_WDT_ERROR</code>	WDT underflow/refresh error has occurred.
<code>BSP_GRP_IRQ_LVD1</code>	Voltage monitoring 1 interrupt.
<code>BSP_GRP_IRQ_LVD2</code>	Voltage monitoring 2 interrupt.
<code>BSP_GRP_IRQ_VBATT</code>	VBATT monitor interrupt.
<code>BSP_GRP_IRQ_OSC_STOP_DETECT</code>	Oscillation stop is detected.
<code>BSP_GRP_IRQ_NMI_PIN</code>	NMI Pin interrupt.
<code>BSP_GRP_IRQ_RAM_PARITY</code>	RAM Parity Error.
<code>BSP_GRP_IRQ_RAM_ECC</code>	RAM ECC Error.
<code>BSP_GRP_IRQ_MPU_BUS_SLAVE</code>	MPU Bus Slave Error.
<code>BSP_GRP_IRQ_MPU_BUS_MASTER</code>	MPU Bus Master Error.
<code>BSP_GRP_IRQ_MPU_STACK</code>	MPU Stack Error.
<code>BSP_GRP_IRQ_TRUSTZONE</code>	MPU Stack Error.
<code>BSP_GRP_IRQ_CACHE_PARITY</code>	MPU Stack Error.

◆ **bsp\_reg\_protect\_t**

enum <code>bsp_reg_protect_t</code>	
The different types of registers that can be protected.	
Enumerator	
<code>BSP_REG_PROTECT_CGC</code>	Enables writing to the registers related to the clock generation circuit.
<code>BSP_REG_PROTECT_OM_LPC_BATT</code>	Enables writing to the registers related to operating modes, low power consumption, and battery backup function.
<code>BSP_REG_PROTECT_LVD</code>	Enables writing to the registers related to the LVD: LVCMPCR, LVDLVLRL, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR.
<code>BSP_REG_PROTECT_SAR</code>	Enables writing to the registers related to the security function.

**Function Documentation**◆ **R\_FSP\_VersionGet()**

<code>fsp_err_t R_FSP_VersionGet ( fsp_pack_version_t *const p_version)</code>		
Get the FSP version based on compile time macros.		
<b>Parameters</b>		
[out]	<code>p_version</code>	Memory address to return version information to.
<b>Return values</b>		
<code>FSP_SUCCESS</code>		Version information stored.
<code>FSP_ERR_ASSERTION</code>		The parameter <code>p_version</code> is NULL.

◆ **Reset\_Handler()**

<code>void Reset_Handler ( void )</code>
MCU starts executing here out of reset. Main stack pointer is set up already.

◆ **Default\_Handler()**

```
void Default_Handler ( void )
```

Default exception handler.

◆ **NMI\_Handler()**

```
void NMI_Handler ( void )
```

Non-maskable interrupt handler. This exception is defined by the BSP, unlike other system exceptions, because there are many sources that map to the NMI exception.

◆ **SystemInit()**

```
void SystemInit ( void )
```

Initialize the MCU and the runtime environment.

◆ **R\_BSP\_WarmStart()**

```
void R_BSP_WarmStart ( bsp_warm_start_event_t event)
```

This function is called at various points during the startup process. This function is declared as a weak symbol higher up in this file because it is meant to be overridden by a user implemented version. One of the main uses for this function is to call functional safety code during the startup process. To use this function just copy this function into your own code and modify it to meet your needs.

**Parameters**

[in]	event	Where the code currently is in the start up process
------	-------	---

◆ **R\_FSP\_CurrentIrqGet()**

```
__STATIC_INLINE IRQn_Type R_FSP_CurrentIrqGet ( void )
```

Return active interrupt vector number value

**Returns**

Active interrupt vector number value

**◆ R\_FSP\_SystemClockHzGet()**

```
__STATIC_INLINE uint32_t R_FSP_SystemClockHzGet ( fsp_priv_clock_t clock)
```

Gets the frequency of a system clock.

**Returns**

Frequency of requested clock in Hertz.

**◆ R\_BSP\_UniqueIdGet()**

```
__STATIC_INLINE bsp_unique_id_t const* R_BSP_UniqueIdGet ( )
```

Get unique ID for this device.

**Returns**

A pointer to the unique identifier structure

**◆ R\_BSP\_FlashCacheDisable()**

```
__STATIC_INLINE void R_BSP_FlashCacheDisable ( )
```

Disables the flash cache.

**◆ R\_BSP\_FlashCacheEnable()**

```
__STATIC_INLINE void R_BSP_FlashCacheEnable ( )
```

Enables the flash cache.

◆ **R\_BSP\_SoftwareDelay()**

```
void R_BSP_SoftwareDelay ( uint32_t delay, bsp_delay_units_t units )
```

Delay for at least the specified duration in units and return.

**Parameters**

[in]	delay	The number of 'units' to delay.
[in]	units	The 'base' (bsp_delay_units_t) for the units specified. Valid values are: BSP_DELAY_UNITS_SECONDS , BSP_DELAY_UNITS_MILLISECONDS, BSP_DELAY_UNITS_MICROSECONDS. For example: At 1 MHz one cycle takes 1 microsecond (.000001 seconds). At 12 MHz one cycle takes 1/12 microsecond or 83 nanoseconds. Therefore one run through bsp_prv_software_delay_loop( ) takes: ~ (83 * BSP_DELAY_LOOP_CYCLES) or 332 ns. A delay of 2 us therefore requires 2000ns/332ns or 6 loops.

The 'theoretical' maximum delay that may be obtained is determined by a full 32 bit loop count and the system clock rate. @120MHz:  $((0xFFFFFFFF \text{ loops} * 4 \text{ cycles /loop}) / 120000000) = 143$  seconds. @32MHz:  $((0xFFFFFFFF \text{ loops} * 4 \text{ cycles /loop}) / 32000000) = 536$  seconds

Note that requests for very large delays will be affected by rounding in the calculations and the actual delay achieved may be slightly longer. @32 MHz, for example, a request for 532 seconds will be closer to 536 seconds.

Note also that if the calculations result in a loop\_cnt of zero, the bsp\_prv\_software\_delay\_loop() function is not called at all. In this case the requested delay is too small (nanoseconds) to be carried out by the loop itself, and the overhead associated with executing the code to just get to this point has certainly satisfied the requested delay.

**Note**

*This function calls bsp\_cpu\_clock\_get() which ultimately calls R\_CGC\_SystemClockFreqGet() and therefore requires that the BSP has already initialized the CGC (which it does as part of the Sysinit). Care should be taken to ensure this remains the case if in the future this function were to be called as part of the BSP initialization.*

◆ **R\_BSP\_GroupIrqWrite()**

```
fsp_err_t R_BSP_GroupIrqWrite ( bsp_grp_irq_t irq, void(*)(bsp_grp_irq_t irq) p_callback )
```

Register a callback function for supported interrupts. If NULL is passed for the callback argument then any previously registered callbacks are unregistered.

**Parameters**

[in]	irq	Interrupt for which to register a callback.
[in]	p_callback	Pointer to function to call when interrupt occurs.

**Return values**

FSP_SUCCESS	Callback registered
FSP_ERR_ASSERTION	Callback pointer is NULL

◆ **R\_BSP\_RegisterProtectEnable()**

```
void R_BSP_RegisterProtectEnable ( bsp_reg_protect_t regs_to_protect)
```

Enable register protection. Registers that are protected cannot be written to. Register protection is enabled by using the Protect Register (PRCR) and the MPC's Write-Protect Register (PWPR).

**Parameters**

[in]	regs_to_protect	Registers which have write protection enabled.
------	-----------------	--

◆ **R\_BSP\_RegisterProtectDisable()**

```
void R_BSP_RegisterProtectDisable ( bsp_reg_protect_t regs_to_unprotect)
```

Disable register protection. Registers that are protected cannot be written to. Register protection is disabled by using the Protect Register (PRCR) and the MPC's Write-Protect Register (PWPR).

**Parameters**

[in]	regs_to_unprotect	Registers which have write protection disabled.
------	-------------------	---

**Variable Documentation**

## ◆ SystemCoreClock

uint32\_t SystemCoreClock

System Clock Frequency (Core Clock)

### 4.1.2.1 RA2A1

[BSP](#) » [MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for ra2a1\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings	<ul style="list-style-type: none"> <li>NMI request or</li> </ul>	Reset is enabled	

> Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode

OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 3.84 V</li> <li>• 2.82 V</li> <li>• 2.51 V</li> <li>• 1.90 V</li> <li>• 1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	HOCO oscillation is enabled after reset	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in low voltage mode and the HOCO must be operating in low voltage mode.
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > PC0 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000 and 0x200FFFFC (RAM)	0x000FFFFC	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x000FFFFF (ROM) or between 0x1FF00003 and 0x200FFFFF (RAM)	0x000FFFFF	
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > PC1 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000 and 0x200FFFFC (RAM)	0x000FFFFC	
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x000FFFFF (ROM) or between 0x1FF00003 and 0x200FFFFF (RAM)	0x000FFFFF	
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	

MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x000FFFFC	0x000FFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x000FFFFF	0x000FFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFC	0x200FFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF

Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4 when oscillation stop detection is used.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 2 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> <li>• 32768 cycles</li> <li>• 65536 cycles</li> <li>• 131072 cycles</li> <li>• 262144 cycles</li> </ul>	262144 cycles	Number of cycles to wait for the main oscillator clock to stabilize.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

```
enum elc\_event\_t
```

### Enumeration Type Documentation

#### ◆ [elc\\_event\\_t](#)

```
enum elc\_event\_t
```

Sources of event signals to be linked to other peripherals or the CPU

**Note**

*This list may change based on based on the device.*

#### 4.1.2.2 RA2E1

BSP » MCU Board Support Package

### Detailed Description

#### Build Time Configurations for ra2e1\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled	
OFS0 register settings	<ul style="list-style-type: none"> <li>Counting</li> </ul>	Stop counting when in	

> Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>continues</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Internal Clock Supply Architecture Type	<ul style="list-style-type: none"> <li>Type B</li> <li>Type A</li> </ul>	Type A
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after</li> </ul>	Voltage monitor 0 reset is disabled after reset

	<ul style="list-style-type: none"> <li>reset</li> <li>Voltage monitor 0 reset is disabled after reset</li> </ul>		
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>3.84 V</li> <li>2.82 V</li> <li>2.51 V</li> <li>1.90 V</li> <li>1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>HOCO oscillation is enabled after reset</li> <li>HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in low voltage mode and the HOCO must be operating in low voltage mode.
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	
MPU > PC0 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000 and 0x200FFFFC (RAM)	0x000FFFFC	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x000FFFFF (ROM) or between 0x1FF00003 and 0x200FFFFF (RAM)	0x000FFFFF	
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	
MPU > PC1 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000 and 0x200FFFFC (RAM)	0x000FFFFC	
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x000FFFFF (ROM) or between 0x1FF00003 and 0x200FFFFF (RAM)	0x000FFFFF	
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	
MPU > Memory Region 0 Start	Value must be an integer between 0 and	0x000FFFFC	

	0x000FFFFC		
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x000FFFFF	0x000FFFFF	
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFC	0x200FFFFC	
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF	
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	Not Supported	config.bsp.low_voltage_mode.disabled	Use the low voltage mode. This limits the

ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4 when oscillation stop detection is used.

Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 2 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> <li>• 32768 cycles</li> <li>• 65536 cycles</li> <li>• 131072 cycles</li> <li>• 262144 cycles</li> </ul>	262144 cycles	Number of cycles to wait for the main oscillator clock to stabilize.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

enum [icu\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

#### Note

*This list may change based on based on the device.*

◆ **ic\_u\_event\_t**enum `ic_u_event_t`

Events to be used with the IELSR register to link interrupt events to the NVIC

*Note**This list is device specific.***4.1.2.3 RA2L1**

BSP » MCU Board Support Package

**Functions**`bsp_power_mode_t` `R_BSP_PowerModeSet (bsp_power_mode_t mode)`**Detailed Description****Build Time Configurations for ra211\_fsp**The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	

OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset

## Interrupt Request

OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Internal Clock Supply Architecture Type	<ul style="list-style-type: none"> <li>Type B</li> <li>Type A</li> </ul>	Type A	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after reset</li> <li>Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>3.84 V</li> <li>2.82 V</li> <li>2.51 V</li> <li>1.90 V</li> <li>1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>HOCO oscillation is enabled after reset</li> <li>HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in low voltage mode and the HOCO must be operating in low voltage mode.
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	
MPU > PC0 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000 and 0x200FFFFC (RAM)	0x000FFFFC	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x000FFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFF (RAM)	0x000FFFFFF	
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	
MPU > PC1 Start	Value must be an integer between 0 and 0x000FFFFC (ROM) or between 0x1FF00000	0x000FFFFC	

	and 0x200FFFC (RAM)	
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x000FFFF (ROM) or between 0x1FF00003 and 0x200FFFF (RAM)	0x000FFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x000FFFC	0x000FFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x000FFFF	0x000FFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFC	0x200FFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFF	0x200FFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFC	0x407FFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFF	0x407FFFF
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region	Value must be an	0x400DFFFC

3 Start	integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC		
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Power > DC-DC Regulator	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> <li>• Enabled at startup</li> </ul>	Disabled	<p>To use the DCDC regulator an external inductor and capacitor must be connected as specified in chapter 40 of the RA2L1 manual. In addition the supply voltage must be above 2.4V and ICLK must be 2 MHz or higher.</p> <p>When set to 'Enabled at startup' the BSP will switch to the DCDC regulator during startup using the voltage range specified below.</p>
Power > DC-DC Supply Range	<ul style="list-style-type: none"> <li>• 2.4V to 2.7V</li> <li>• 2.7V to 3.6V</li> <li>• 3.6V to 4.5V</li> <li>• 4.5V to 5.5V</li> </ul>	2.7V to 3.6V	Set this to the expected MCU supply voltage (Vcc) at startup when using the DCDC regulator.
Use Low Voltage Mode	Not Supported	config.bsp.low_voltage_mode.disabled	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4 when oscillation stop detection is used.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 2 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> <li>• 32768 cycles</li> <li>• 65536 cycles</li> <li>• 131072 cycles</li> <li>• 262144 cycles</li> </ul>	262144 cycles	Number of cycles to wait for the main oscillator clock to stabilize.

ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

Common macro for FSP header files. There is also a corresponding FSP\_FOOTER macro at the end of this file.

## Enumerations

enum [elc\\_event\\_t](#)

enum [icu\\_event\\_t](#)

enum [bsp\\_power\\_mode\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

**Note**

*This list may change based on based on the device.*

### ◆ [icu\\_event\\_t](#)

enum [icu\\_event\\_t](#)

Events to be used with the IELSR register to link interrupt events to the NVIC

**Note**

*This list is device specific.*

◆ **bsp\_power\_mode\_t**

enum <code>bsp_power_mode_t</code>	
Voltage regulator mode	
Enumerator	
<code>BSP_POWER_MODE_DCDC_2V4_TO_2V7</code>	DCDC mode; 2.4V to 2.7V supply.
<code>BSP_POWER_MODE_DCDC_2V7_TO_3V6</code>	DCDC mode; 2.7V to 3.6V supply.
<code>BSP_POWER_MODE_DCDC_3V6_TO_4V5</code>	DCDC mode; 3.6V to 4.5V supply.
<code>BSP_POWER_MODE_DCDC_4V5_TO_5V5</code>	DCDC mode; 4.5V to 5.5V supply.
<code>BSP_POWER_MODE_LDO</code>	LDO mode.

**Function Documentation**◆ **R\_BSP\_PowerModeSet()**

<code>bsp_power_mode_t</code> R_BSP_PowerModeSet ( <code>bsp_power_mode_t</code> mode)
<p>Select either the LDO or DCDC regulator and/or update the MCU supply voltage range. Returns the previously selected mode.</p> <p><i>Note</i></p> <p><i>DCDC mode has the following limitations:</i></p> <ul style="list-style-type: none"> <li>◦ Supply voltage must be 2.4V or greater</li> <li>◦ Low- and Subosc-speed modes are not available</li> <li>◦ Software Standby is not available. Ensure these limitations are respected before entering DCDC mode. If supply voltage may drop below 2.4V during operation, configure a LVD channel to interrupt or reset the MCU near this threshold to switch back to the LDO.</li> </ul> <p><i>Switching to DCDC mode temporarily disables all interrupts and blocks for 22 microseconds; switching to LDO from DCDC temporarily disables all peripherals and interrupts and blocks for 60 microseconds.</i></p> <p><i>If the supply voltage falls outside the range originally specified when starting the DCDC regulator, call this function again with the updated supply voltage.</i></p> <p><b>Returns</b></p> <p>The previously selected power mode.</p>

**4.1.2.4 RA4M1**

BSP » MCU Board Support Package

**Detailed Description****Build Time Configurations for ra4m1\_fsp**

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled	
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby	
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start)</li> </ul>	Stop WDT after a reset (register-start mode)	

	mode)		
	<ul style="list-style-type: none"> <li>Stop WDT after a reset (register-start mode)</li> </ul>		
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles	
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128	
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after reset</li> <li>Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>3.84 V</li> <li>2.82 V</li> <li>2.51 V</li> <li>1.90 V</li> <li>1.70 V</li> </ul>	1.90 V	
OFS1 register settings > HOCO Oscillation Enable	HOCO oscillation is enabled after reset	HOCO oscillation is enabled after reset	HOCO must be enabled out of reset because the MCU starts up in

low voltage mode and the HOCO must be operating in low voltage mode.

MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF	0x00FFFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC

MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFF	0x200FFFFFF	
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 2 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> <li>• 32768 cycles</li> <li>• 65536 cycles</li> <li>• 131072 cycles</li> </ul>	262144 cycles	Number of cycles to wait for the main oscillator clock to stabilize.

ID Code Mode	<ul style="list-style-type: none"> <li>• 262144 cycles</li> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

```
enum elc_event_t
```

## Enumeration Type Documentation

### ◆ elc\_event\_t

```
enum elc_event_t
```

Sources of event signals to be linked to other peripherals or the CPU

**Note**

*This list may change based on based on the device.*

### 4.1.2.5 RA4M2

BSP » [MCU Board Support Package](#)

## Build Time Configurations for ra4m2\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
Security > Exceptions > Exception Response	<ul style="list-style-type: none"> <li>• Non-Maskable Interrupt</li> <li>• Reset</li> </ul>	Non-Maskable Interrupt	Configure the result of a TrustZone Filter exception. This

exception is generated when the TrustZone Filter detects access to a protected region.

This setting is only valid when building projects with TrustZone.

Value for SCB->AIRCR register bit BFHFNMIN. Defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.

This setting is only valid when building projects with TrustZone.

Value for SCB->AIRCR register bit PRIS. When enabled, all Non-secure interrupt priorities are automatically demoted by right shifting their priority by one then setting the most significant bit. As there is effectively one less bit care must be taken to ensure the prioritization of non-secure interrupts is correct.

This setting is only valid when building projects with TrustZone.

Defines whether SRAMPRCR is write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > Exceptions > BusFault, HardFault, and NMI Target

- Non-Secure State
  - Secure State
- Secure State

Security > Exceptions > Prioritize Secure Exceptions

- Enabled
  - Disabled
- Disabled

Security > SRAM Accessibility > SRAM Protection

- Both Secure and Non-Secure State
  - Secure State
- Both Secure and Non-Secure State

Security > SRAM  
Accessibility > SRAM  
ECC

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Defines whether SRAM ECC registers are write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > SRAM  
Accessibility > Standby  
RAM

- Regions 7-0 are all Secure.
- Region 7 is Non-secure. Regions 6-0 are Secure.
- Regions 7-6 are Non-secure. Regions 5-0 are Secure.
- Regions 7-5 are Non-secure. Regions 4-0 are Secure.
- Regions 7-4 are Non-secure. Regions 3-0 are Secure.
- Regions 7-3 are Non-secure. Regions 2-0 are Secure.
- Regions 7-2 are Non-secure. Regions 1-0 are Secure.
- Regions 7-1 are Non-secure. Region 0 is Secure.
- Regions 7-0 are all Non-secure.

config.bsp.fsp.tz.stbramsar.both

Defines whether Standby RAM registers are accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > BUS  
Accessibility > Bus  
Security Attribution  
Register A

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Defines whether the Slave Bus Control Registers (BUSSCNT<slave>) are write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > BUS  
Accessibility > Bus

- Both Secure and Non-Secure State

Both Secure and Non-Secure State

Defines whether the Bus and DMAC/DTC

Security Attribution Register B	State <ul style="list-style-type: none"> <li>Secure State</li> </ul>	Error Clear Registers are write accessible for the Non-secure application.
Security > System Reset Request Accessibility	Secure State <ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	This setting is only valid when building projects with TrustZone.  Value for SCB->AIRCR register bit SYSRESETREQS. Defines whether the SYSRESETREQ bit is functional for Non-secure use.
Security > Cache Accessibility	Both Secure and Non-Secure State <ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	This setting is only valid when building projects with TrustZone.  Defines whether the Cache registers are write accessible for the Non-secure application.
Security > System Reset Status Accessibility	Both Secure and Non-Secure State <ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	This setting is only valid when building projects with TrustZone.  Defines whether the reset status registers (RSTSRn) can be cleared from the Non-secure application.
Security > Battery Backup Accessibility	Both Secure and Non-Secure State <ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	This setting is only valid when building projects with TrustZone.  Defines whether the battery backup registers are accessible for the Non-secure application. If Secure State is selected, all battery backup registers are read only except for VBTBKRn registers which are both read and write protected.

This setting is only valid when building projects with TrustZone.

OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>• IWDT is Disabled</li> <li>• IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 128 cycles</li> <li>• 512 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> </ul>	2048 cycles
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 1</li> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby

	when in Sleep, Snooze mode, or Software Standby	
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after reset</li> <li>Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset

OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>		HOCO oscillation is disabled after reset
Block Protection Settings (BPS) > BPS0	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 0
Permanent Block Protection Settings (PBPS) > PBPS0	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 0
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Startup C-Cache Line Size	<ul style="list-style-type: none"> <li>• 32 Bytes</li> <li>• 64 Bytes</li> </ul>	32 Bytes	Set the C-Cache line size configured during startup.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 3 cycles</li> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> </ul>	8163 cycles	Number of cycles to wait for the main oscillator clock to stabilize.

- 259 cycles
- 547 cycles
- 1059 cycles
- 2147 cycles
- 4291 cycles
- 8163 cycles

#### 4.1.2.6 RA4M3

[BSP](#) » [MCU Board Support Package](#)

### Build Time Configurations for ra4m3\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
Security > Exceptions > Exception Response	<ul style="list-style-type: none"> <li>• Non-Maskable Interrupt</li> <li>• Reset</li> </ul>	Non-Maskable Interrupt	<p>Configure the result of a TrustZone Filter exception. This exception is generated when the TrustZone Filter detects access to a protected region.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > BusFault, HardFault, and NMI Target	<ul style="list-style-type: none"> <li>• Non-Secure State</li> <li>• Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit BFHFNMIN. Defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > Prioritize Secure Exceptions	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Value for SCB-&gt;AIRCR register bit PRIS. When enabled, all Non-secure interrupt priorities are automatically demoted by right shifting their priority by one then</p>

setting the most significant bit. As there is effectively one less bit care must be taken to ensure the prioritization of non-secure interrupts is correct.

This setting is only valid when building projects with TrustZone.

Defines whether SRAMPRCR is write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Defines whether SRAM ECC registers are write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Defines whether Standby RAM registers are accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > SRAM  
Accessibility > SRAM  
Protection

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Security > SRAM  
Accessibility > SRAM  
ECC

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Security > SRAM  
Accessibility > Standby  
RAM

- Regions 7-0 are all Secure.
- Region 7 is Non-secure. Regions 6-0 are Secure.
- Regions 7-6 are Non-secure. Regions 5-0 are Secure.
- Regions 7-5 are Non-secure. Regions 4-0 are Secure.
- Regions 7-4 are Non-secure. Regions 3-0 are Secure.
- Regions 7-3 are Non-secure. Regions 2-0 are Secure.
- Regions 7-2 are

config.bsp.fsp.tz.stbra  
msar.both

	<ul style="list-style-type: none"> <li>• Non-secure. Regions 1-0 are Secure.</li> <li>• Regions 7-1 are Non-secure. Region 0 is Secure.</li> <li>• Regions 7-0 are all Non-secure.</li> </ul>		
Security > BUS Accessibility > Bus Security Attribution Register A	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Slave Bus Control Registers (BUSSCNT&lt;slave&gt;) are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > BUS Accessibility > Bus Security Attribution Register B	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Bus and DMAC/DTC Error Clear Registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > System Reset Request Accessibility	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit SYSRESETREQS. Defines whether the SYSRESETREQ bit is functional for Non-secure use.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Cache Accessibility	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Cache registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>

Security > System Reset Status Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the reset status registers (RSTSRn) can be cleared from the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Battery Backup Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the battery backup registers are accessible for the Non-secure application. If Secure State is selected, all battery backup registers are read only except for VBTBKRn registers which are both read and write protected.</p> <p>This setting is only valid when building projects with TrustZone.</p>
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings	<ul style="list-style-type: none"> <li>25%</li> </ul>	100% (no window start)	

> Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> </ul>	100% (no window start position)

Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>		
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset	
Block Protection Settings (BPS) > BPS0	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 0
Block Protection Settings (BPS) > BPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> <li>• Flash Block 37</li> </ul>	0U	Configure Block Protection Register 1
Permanent Block Protection Settings (PBPS) > PBPS0	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 0
Permanent Block Protection Settings (PBPS) > PBPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> <li>• Flash Block 37</li> </ul>	0U	Configure Permanent Block Protection Register 1

Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Startup C-Cache Line Size	<ul style="list-style-type: none"> <li>• 32 Bytes</li> <li>• 64 Bytes</li> </ul>	32 Bytes	Set the C-Cache line size configured during startup.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 3 cycles</li> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> <li>• 259 cycles</li> <li>• 547 cycles</li> <li>• 1059 cycles</li> <li>• 2147 cycles</li> <li>• 4291 cycles</li> <li>• 8163 cycles</li> </ul>	8163 cycles	Number of cycles to wait for the main oscillator clock to stabilize.

#### 4.1.2.7 RA4W1

[BSP » MCU Board Support Package](#)

### Detailed Description

#### Build Time Configurations for ra4w1\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

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Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled	
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby	
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-</li> </ul>	Stop WDT after a reset (register-start mode)	

	start mode)	
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.82 V</li> <li>• 2.51 V</li> <li>• 1.90 V</li> </ul>	1.90 V
OFS1 register settings > HOCO Oscillation Enable	HOCO oscillation is enabled after reset	config.bsp.fsp.OFS1.hoco_osc.disabled
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and	0x00FFFFFFC

	0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	
MPU > PC0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0x00FFFFFFC (ROM) or between 0x1FF00000 and 0x200FFFFFFC (RAM)	0x00FFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF (ROM) or between 0x1FF00003 and 0x200FFFFFFF (RAM)	0x00FFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFFF	0x00FFFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFFF	0x200FFFFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2	Value must be an integer between 0x407FFFFFFC and 0x407FFFFFFC	0x407FFFFFFC

2 Start	integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC		
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Use Low Voltage Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Use the low voltage mode. This limits the ICLK operating frequency to 4 MHz and requires all clock dividers to be at least 4.
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 2 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> <li>• 32768 cycles</li> <li>• 65536 cycles</li> <li>• 131072 cycles</li> <li>• 262144 cycles</li> </ul>	262144 cycles	Number of cycles to wait for the main oscillator clock to stabilize.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless.

When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.

ID Code (32 Hex Characters)

Value must be a 32 character long hex string

FFFFFFFFFFFFFFFFFFFF  
FFFFFFFFFFFF

Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU1

#### Note

*This list may change based on device. This list is for RA4W1.*

### 4.1.2.8 RA6M1

BSP » [MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for [ra6m1\\_fsp](#)

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> </ul>	2048 cycles	

	<ul style="list-style-type: none"> <li>• 2048 cycles</li> </ul>	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 1</li> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles

OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC

MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFF	0x200FFFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFFFC	0x407FFFFFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or	0x407FFFFFF

	between 0x40100003 and 0x407FFFFFFF		
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFFFF	0x400DFFFF	
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> <li>• 259 cycles</li> <li>• 547 cycles</li> <li>• 1059 cycles</li> <li>• 2147 cycles</li> <li>• 4291 cycles</li> </ul>	8163 cycles	Number of cycles to wait for the main oscillator clock to stabilize. Drive capability automatic switching function is by default disabled.

ID Code Mode	<ul style="list-style-type: none"> <li>• 8163 cycles</li> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

**Note**

*This list may change based on based on the device.*

### 4.1.2.9 RA6M2

[BSP](#) » [MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for [ra6m2\\_fsp](#)

The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT >	<ul style="list-style-type: none"> <li>• IWDT is Disabled</li> </ul>	IWDT is Disabled	

Start Mode	<ul style="list-style-type: none"> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset</li> </ul>	Stop WDT after a reset (register-start mode)

	(auto-start mode)	
	<ul style="list-style-type: none"> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> </ul>	HOCO oscillation is disabled after reset

	<ul style="list-style-type: none"> <li>• HOCO oscillation is disabled after reset</li> </ul>	
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFF	0x00FFFFFF
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFC	0x200FFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled

MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFFFF	0x407FFFFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFFFF	0x400DFFFF	
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby</p>

Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> <li>• 259 cycles</li> <li>• 547 cycles</li> <li>• 1059 cycles</li> <li>• 2147 cycles</li> <li>• 4291 cycles</li> <li>• 8163 cycles</li> </ul>	8163 cycles	modes are not available. Number of cycles to wait for the main oscillator clock to stabilize. Drive capability automatic switching function is by default disabled.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked (Ignore ID)</li> <li>• Locked with All Erase support</li> <li>• Locked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.
ID Code (32 Hex Characters)	Value must be a 32 character long hex string	FFFFFFFFFFFFFFFFFFFF FFFFFFFFFFFF	Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

**Note**

*This list may change based on based on the device.*

### 4.1.2.10 RA6M3

BSP » [MCU Board Support Package](#)

## Detailed Description

### Build Time Configurations for ra6m3\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled	
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby	

	Standby Mode)	
	<ul style="list-style-type: none"> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>NMI</li> <li>Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues</li> <li>Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>Voltage monitor 0 reset is enabled after reset</li> <li>Voltage monitor 0 reset is disabled after</li> </ul>	Voltage monitor 0 reset is disabled after reset

	reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC0 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFF	0xFFFFFFFF
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFF	0x00FFFFFF
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFF	0x200FFFFFF

MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFF	0x200FFFFF	
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x407FFFFC	
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x407FFFFF	
MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the</p>

Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.

When FLL is enabled Software Standby and Deep Software Standby modes are not available.

Number of cycles to wait for the main oscillator clock to stabilize. Drive capability automatic switching function is by default disabled.

Main Oscillator Wait Time

- 35 cycles
  - 67 cycles
  - 131 cycles
  - 259 cycles
  - 547 cycles
  - 1059 cycles
  - 2147 cycles
  - 4291 cycles
  - 8163 cycles
- 8163 cycles

ID Code Mode

- Unlocked (Ignore ID)
  - Locked with All Erase support
  - Locked
- Unlocked (Ignore ID)

When set to 'Locked with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.

ID Code (32 Hex Characters)

Value must be a 32 character long hex string

FFFFFFFFFFFFFFFFFFFF  
FFFFFFFFFFFFFF

Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

◆ **elc\_event\_t**enum `elc_event_t`

Sources of event signals to be linked to other peripherals or the CPU

*Note**This list may change based on based on the device.***4.1.2.11 RA6M4**[BSP](#) » [MCU Board Support Package](#)**Build Time Configurations for ra6m4\_fsp**The following build time configurations are defined in `fsp_cfg/bsp/bsp_mcu_family_cfg.h`:

Configuration	Options	Default	Description
Security > Exceptions > Exception Response	<ul style="list-style-type: none"> <li>Non-Maskable Interrupt</li> <li>Reset</li> </ul>	Non-Maskable Interrupt	<p>Configure the result of a TrustZone Filter exception. This exception is generated when the TrustZone Filter detects access to a protected region.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > BusFault, HardFault, and NMI Target	<ul style="list-style-type: none"> <li>Non-Secure State</li> <li>Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit BFHFNMIN. Defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > Prioritize Secure Exceptions	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	<p>Value for SCB-&gt;AIRCR register bit PRIS. When enabled, all Non-secure interrupt priorities are</p>

automatically demoted by right shifting their priority by one then setting the most significant bit. As there is effectively one less bit care must be taken to ensure the prioritization of non-secure interrupts is correct.

This setting is only valid when building projects with TrustZone.

Defines whether SRAMPRCR is write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Defines whether SRAM ECC registers are write accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Defines whether Standby RAM registers are accessible for the Non-secure application.

This setting is only valid when building projects with TrustZone.

Security > SRAM  
Accessibility > SRAM  
Protection

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Security > SRAM  
Accessibility > SRAM  
ECC

- Both Secure and Non-Secure State
- Secure State

Both Secure and Non-Secure State

Security > SRAM  
Accessibility > Standby  
RAM

- Regions 7-0 are all Secure.
- Region 7 is Non-secure. Regions 6-0 are Secure.
- Regions 7-6 are Non-secure. Regions 5-0 are Secure.
- Regions 7-5 are Non-secure. Regions 4-0 are Secure.
- Regions 7-4 are Non-secure. Regions 3-0 are Secure.
- Regions 7-3 are Non-secure.

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	<ul style="list-style-type: none"> <li>Regions 2-0 are Secure.</li> <li>Regions 7-2 are Non-secure.</li> <li>Regions 1-0 are Secure.</li> <li>Regions 7-1 are Non-secure.</li> <li>Region 0 is Secure.</li> <li>Regions 7-0 are all Non-secure.</li> </ul>		
Security > BUS Accessibility > Bus Security Attribution Register A	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Slave Bus Control Registers (BUSSCNT&lt;slave&gt;) are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > BUS Accessibility > Bus Security Attribution Register B	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Bus and DMAC/DTC Error Clear Registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > System Reset Request Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit SYSRESETREQS. Defines whether the SYSRESETREQ bit is functional for Non-secure use.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Cache Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Cache registers are write accessible for the Non-secure application.</p> <p>This setting is only</p>

Security > System Reset Status Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	valid when building projects with TrustZone.
Security > Battery Backup Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>This setting is only valid when building projects with TrustZone.</p> <p>Defines whether the battery backup registers are accessible for the Non-secure application. If Secure State is selected, all battery backup registers are read only except for VBTBKRn registers which are both read and write protected.</p> <p>This setting is only valid when building projects with TrustZone.</p>
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>1</li> <li>16</li> <li>32</li> <li>64</li> <li>128</li> <li>256</li> </ul>	128	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> </ul>	0% (no window end position)	

OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>0% (no window end position)</li> <li>25%</li> <li>50%</li> <li>75%</li> <li>100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>NMI request or interrupt request is enabled</li> <li>Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>Automatically activate WDT after a reset (auto-start mode)</li> <li>Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>1024 cycles</li> <li>4096 cycles</li> <li>8192 cycles</li> <li>16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division Ratio	<ul style="list-style-type: none"> <li>4</li> <li>64</li> <li>128</li> <li>512</li> <li>2048</li> <li>8192</li> </ul>	128
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>75%</li> <li>50%</li> <li>25%</li> <li>0% (no window</li> </ul>	0% (no window end position)

	end position)		
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset	
Block Protection Settings (BPS) > BPS0	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 0
Block Protection Settings (BPS) > BPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> <li>• Flash Block 37</li> </ul>	0U	Configure Block Protection Register 1
Block Protection Settings (BPS) > BPS2	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 2
Permanent Block Protection Settings (PBPS) > PBPS0	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 0

Permanent Block Protection Settings (PBPS) > PBPS1	<ul style="list-style-type: none"> <li>Flash Block 32</li> <li>Flash Block 33</li> <li>Flash Block 34</li> <li>Flash Block 35</li> <li>Flash Block 36</li> <li>Flash Block 37</li> </ul>	0U	Configure Permanent Block Protection Register 1
Permanent Block Protection Settings (PBPS) > PBPS2	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 2
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Startup C-Cache Line Size	<ul style="list-style-type: none"> <li>32 Bytes</li> <li>64 Bytes</li> </ul>	32 Bytes	Set the C-Cache line size configured during startup.
Dual Bank Mode	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Enabling dual bank mode splits the flash into two banks that can be swapped by programming the BANKSEL non-volatile register. When enabled, one bank will start at address 0x0 and the other will start at 0x200000. Each bank contains exactly half the capacity of the

entire code flash. When Dual Bank mode is enabled, Startup Program Protection and Block Swap functions cannot be used.

Number of cycles to wait for the main oscillator clock to stabilize.

Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 3 cycles</li> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> <li>• 259 cycles</li> <li>• 547 cycles</li> <li>• 1059 cycles</li> <li>• 2147 cycles</li> <li>• 4291 cycles</li> <li>• 8163 cycles</li> </ul>	8163 cycles
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#### 4.1.2.12 RA6M5

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#### Build Time Configurations for ra6m5\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
Security > Exceptions > Exception Response	<ul style="list-style-type: none"> <li>• Non-Maskable Interrupt</li> <li>• Reset</li> </ul>	Non-Maskable Interrupt	<p>Configure the result of a TrustZone Filter exception. This exception is generated when the TrustZone Filter detects access to a protected region.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > Exceptions > BusFault, HardFault, and NMI Target	<ul style="list-style-type: none"> <li>• Non-Secure State</li> <li>• Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit BFHFNMIN. Defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.</p> <p>This setting is only</p>

Security > Exceptions > Prioritize Secure Exceptions	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	valid when building projects with TrustZone.
Security > SRAM Accessibility > SRAM Protection	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Value for SCB-&gt;AIRCR register bit PRIS. When enabled, all Non-secure interrupt priorities are automatically demoted by right shifting their priority by one then setting the most significant bit. As there is effectively one less bit care must be taken to ensure the prioritization of non-secure interrupts is correct.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > SRAM Accessibility > SRAM ECC	<ul style="list-style-type: none"> <li>• Both Secure and Non-Secure State</li> <li>• Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether SRAMPRCR is write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p> <p>Defines whether SRAM ECC registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > SRAM Accessibility > Standby RAM	<ul style="list-style-type: none"> <li>• Regions 7-0 are all Secure.</li> <li>• Region 7 is Non-secure. Regions 6-0 are Secure.</li> <li>• Regions 7-6 are Non-secure. Regions 5-0 are Secure.</li> <li>• Regions 7-5 are Non-secure.</li> </ul>	config.bsp.fsp.tz.stbra msar.both	<p>Defines whether Standby RAM registers are accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>

	<ul style="list-style-type: none"> <li>Regions 4-0 are Secure.</li> <li>Regions 7-4 are Non-secure. Regions 3-0 are Secure.</li> <li>Regions 7-3 are Non-secure. Regions 2-0 are Secure.</li> <li>Regions 7-2 are Non-secure. Regions 1-0 are Secure.</li> <li>Regions 7-1 are Non-secure. Region 0 is Secure.</li> <li>Regions 7-0 are all Non-secure.</li> </ul>		
Security > BUS Accessibility > Bus Security Attribution Register A	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Slave Bus Control Registers (BUSSCNT&lt;slave&gt;) are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > BUS Accessibility > Bus Security Attribution Register B	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	<p>Defines whether the Bus and DMAC/DTC Error Clear Registers are write accessible for the Non-secure application.</p> <p>This setting is only valid when building projects with TrustZone.</p>
Security > System Reset Request Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Secure State	<p>Value for SCB-&gt;AIRCR register bit SYSRESETREQS. Defines whether the SYSRESETREQ bit is functional for Non-secure use.</p> <p>This setting is only valid when building projects with</p>

Security > Cache Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	TrustZone. Defines whether the Cache registers are write accessible for the Non-secure application.  This setting is only valid when building projects with TrustZone.
Security > System Reset Status Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	Defines whether the reset status registers (RSTSRn) can be cleared from the Non-secure application.  This setting is only valid when building projects with TrustZone.
Security > Battery Backup Accessibility	<ul style="list-style-type: none"> <li>Both Secure and Non-Secure State</li> <li>Secure State</li> </ul>	Both Secure and Non-Secure State	Defines whether the battery backup registers are accessible for the Non-secure application. If Secure State is selected, all battery backup registers are read only except for VBTBKRn registers which are both read and write protected.  This setting is only valid when building projects with TrustZone.
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>IWDT is Disabled</li> <li>IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>128 cycles</li> <li>512 cycles</li> <li>1024 cycles</li> <li>2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings > Independent WDT >	<ul style="list-style-type: none"> <li>1</li> <li>16</li> </ul>	128	

Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock Frequency Division	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> <li>• 128</li> </ul>	128

Ratio	<ul style="list-style-type: none"> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>		
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)	
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)	
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset	
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode	
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset	
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V	
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset	
Block Protection Settings (BPS) > BPS0	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 0
Block Protection Settings (BPS) > BPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> </ul>	0U	Configure Block Protection Register 1

	• Flash Block 37		
Block Protection Settings (BPS) > BPS2	Refer to the RA Configuration tool for available options.	0U	Configure Block Protection Register 2
Permanent Block Protection Settings (PBPS) > PBPS0	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 0
Permanent Block Protection Settings (PBPS) > PBPS1	<ul style="list-style-type: none"> <li>• Flash Block 32</li> <li>• Flash Block 33</li> <li>• Flash Block 34</li> <li>• Flash Block 35</li> <li>• Flash Block 36</li> <li>• Flash Block 37</li> </ul>	0U	Configure Permanent Block Protection Register 1
Permanent Block Protection Settings (PBPS) > PBPS2	Refer to the RA Configuration tool for available options.	0U	Configure Permanent Block Protection Register 2
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Startup C-Cache Line Size	<ul style="list-style-type: none"> <li>• 32 Bytes</li> <li>• 64 Bytes</li> </ul>	32 Bytes	Set the C-Cache line size configured during startup.
Dual Bank Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enabling dual bank mode splits the flash into two banks that can be swapped by programming the

BANKSEL non-volatile register. When enabled, one bank will start at address 0x0 and the other will start at 0x200000. Each bank contains exactly half the capacity of the entire code flash. When Dual Bank mode is enabled, Startup Program Protection and Block Swap functions cannot be used.

Number of cycles to wait for the main oscillator clock to stabilize.

Main Oscillator Wait Time

- 3 cycles
  - 35 cycles
  - 67 cycles
  - 131 cycles
  - 259 cycles
  - 547 cycles
  - 1059 cycles
  - 2147 cycles
  - 4291 cycles
  - 8163 cycles
- 8163 cycles

#### 4.1.2.13 RA6T1

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### Detailed Description

#### Build Time Configurations for ra6t1\_fsp

The following build time configurations are defined in fsp\_cfg/bsp/bsp\_mcu\_family\_cfg.h:

Configuration	Options	Default	Description
OFS0 register settings > Independent WDT > Start Mode	<ul style="list-style-type: none"> <li>• IWDT is Disabled</li> <li>• IWDT is automatically activated after a reset (Autostart mode)</li> </ul>	IWDT is Disabled	
OFS0 register settings > Independent WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 128 cycles</li> <li>• 512 cycles</li> <li>• 1024 cycles</li> <li>• 2048 cycles</li> </ul>	2048 cycles	
OFS0 register settings	<ul style="list-style-type: none"> <li>• 1</li> </ul>	128	

> Independent WDT > Dedicated Clock Frequency Divisor	<ul style="list-style-type: none"> <li>• 16</li> <li>• 32</li> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	
OFS0 register settings > Independent WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > Independent WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > Independent WDT > Reset Interrupt Request Select	<ul style="list-style-type: none"> <li>• NMI request or interrupt request is enabled</li> <li>• Reset is enabled</li> </ul>	Reset is enabled
OFS0 register settings > Independent WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues (Note: Device will not enter Deep Standby Mode when selected. Device will enter Software Standby Mode)</li> <li>• Stop counting when in Sleep, Snooze mode, or Software Standby</li> </ul>	Stop counting when in Sleep, Snooze mode, or Software Standby
OFS0 register settings > WDT > Start Mode Select	<ul style="list-style-type: none"> <li>• Automatically activate WDT after a reset (auto-start mode)</li> <li>• Stop WDT after a reset (register-start mode)</li> </ul>	Stop WDT after a reset (register-start mode)
OFS0 register settings > WDT > Timeout Period	<ul style="list-style-type: none"> <li>• 1024 cycles</li> <li>• 4096 cycles</li> <li>• 8192 cycles</li> <li>• 16384 cycles</li> </ul>	16384 cycles
OFS0 register settings > WDT > Clock	<ul style="list-style-type: none"> <li>• 4</li> <li>• 64</li> </ul>	128

Frequency Division Ratio	<ul style="list-style-type: none"> <li>• 128</li> <li>• 512</li> <li>• 2048</li> <li>• 8192</li> </ul>	
OFS0 register settings > WDT > Window End Position	<ul style="list-style-type: none"> <li>• 75%</li> <li>• 50%</li> <li>• 25%</li> <li>• 0% (no window end position)</li> </ul>	0% (no window end position)
OFS0 register settings > WDT > Window Start Position	<ul style="list-style-type: none"> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> <li>• 100% (no window start position)</li> </ul>	100% (no window start position)
OFS0 register settings > WDT > Reset Interrupt Request	<ul style="list-style-type: none"> <li>• NMI</li> <li>• Reset</li> </ul>	Reset
OFS0 register settings > WDT > Stop Control	<ul style="list-style-type: none"> <li>• Counting continues</li> <li>• Stop counting when entering Sleep mode</li> </ul>	Stop counting when entering Sleep mode
OFS1 register settings > Voltage Detection 0 Circuit Start	<ul style="list-style-type: none"> <li>• Voltage monitor 0 reset is enabled after reset</li> <li>• Voltage monitor 0 reset is disabled after reset</li> </ul>	Voltage monitor 0 reset is disabled after reset
OFS1 register settings > Voltage Detection 0 Level	<ul style="list-style-type: none"> <li>• 2.94 V</li> <li>• 2.87 V</li> <li>• 2.80 V</li> </ul>	2.80 V
OFS1 register settings > HOCO Oscillation Enable	<ul style="list-style-type: none"> <li>• HOCO oscillation is enabled after reset</li> <li>• HOCO oscillation is disabled after reset</li> </ul>	HOCO oscillation is disabled after reset
MPU > Enable or disable PC Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC0 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC
MPU > PC0 End	Value must be an integer between	0xFFFFFFFF

	0x00000003 and 0xFFFFFFFF	
MPU > Enable or disable PC Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > PC1 Start	Value must be an integer between 0 and 0xFFFFFFFFC	0xFFFFFFFFC
MPU > PC1 End	Value must be an integer between 0x00000003 and 0xFFFFFFFF	0xFFFFFFFF
MPU > Enable or disable Memory Region 0	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 0 Start	Value must be an integer between 0 and 0x00FFFFFFC	0x00FFFFFFC
MPU > Memory Region 0 End	Value must be an integer between 0x00000003 and 0x00FFFFFF	0x00FFFFFF
MPU > Enable or disable Memory Region 1	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 1 Start	Value must be an integer between 0x1FF00000 and 0x200FFFFFFC	0x200FFFFFFC
MPU > Memory Region 1 End	Value must be an integer between 0x1FF00003 and 0x200FFFFFF	0x200FFFFFF
MPU > Enable or disable Memory Region 2	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
MPU > Memory Region 2 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFFFC	0x407FFFFFFC
MPU > Memory Region 2 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFFF	0x407FFFFFF

MPU > Enable or disable Memory Region 3	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	
MPU > Memory Region 3 Start	Value must be an integer between 0x400C0000 and 0x400DFFFC or between 0x40100000 and 0x407FFFFC	0x400DFFFC	
MPU > Memory Region 3 End	Value must be an integer between 0x400C0003 and 0x400DFFFF or between 0x40100003 and 0x407FFFFF	0x400DFFFF	
Clocks > HOCO FLL Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Setting this option to Enabled improves HOCO accuracy significantly by using the subclock, but incurs certain restrictions.</p> <p>The FLL function requires the subclock oscillator to be running and stabilized. When enabled and running the PLL or system clock from HOCO, the BSP will wait for both the Subclock Stabilization Time as well as the FLL Stabilization Time when setting up clocks at startup.</p> <p>When FLL is enabled Software Standby and Deep Software Standby modes are not available.</p>
Main Oscillator Wait Time	<ul style="list-style-type: none"> <li>• 35 cycles</li> <li>• 67 cycles</li> <li>• 131 cycles</li> <li>• 259 cycles</li> <li>• 547 cycles</li> <li>• 1059 cycles</li> <li>• 2147 cycles</li> <li>• 4291 cycles</li> <li>• 8163 cycles</li> </ul>	8163 cycles	Number of cycles to wait for the main oscillator clock to stabilize. Drive capability automatic switching function is by default disabled.
ID Code Mode	<ul style="list-style-type: none"> <li>• Unlocked</li> </ul>	Unlocked (Ignore ID)	When set to 'Locked

- (Ignore ID)
- Locked with All Erase support
  - Locked

with All Erase support', the ID Code must be set in the debugger to read or write data to the MCU, but the All Erase command is still accepted regardless. When set to 'Locked', all erase/download/debug access is disabled unless the ID Code is provided.

ID Code (32 Hex Characters)

Value must be a 32 character long hex string

FFFFFFFFFFFFFFFFFFFF  
FFFFFFFFFFFFFF

Set the ID Code for locking debug access. This setting is only used when the ID Code Mode is not set to Unlocked.

## Enumerations

enum [elc\\_event\\_t](#)

## Enumeration Type Documentation

### ◆ [elc\\_event\\_t](#)

enum [elc\\_event\\_t](#)

Sources of event signals to be linked to other peripherals or the CPU

*Note*

*This list may change based on based on the device.*

## 4.1.3 BSP I/O access

### BSP

#### Functions

`__STATIC_INLINE uint32_t` [R\\_BSP\\_PinRead](#) ([bsp\\_io\\_port\\_pin\\_t](#) pin)

`__STATIC_INLINE void` [R\\_BSP\\_PinWrite](#) ([bsp\\_io\\_port\\_pin\\_t](#) pin, [bsp\\_io\\_level\\_t](#) level)

`__STATIC_INLINE void` [R\\_BSP\\_PinCfg](#) ([bsp\\_io\\_port\\_pin\\_t](#) pin, [uint32\\_t](#) cfg)

`__STATIC_INLINE void` [R\\_BSP\\_PinAccessEnable](#) (void)

`__STATIC_INLINE void` [R\\_BSP\\_PinAccessDisable](#) (void)

## Detailed Description

This module provides basic read/write access to port pins.

### Enumerations

enum [bsp\\_io\\_level\\_t](#)

enum [bsp\\_io\\_direction\\_t](#)

enum [bsp\\_io\\_port\\_t](#)

enum [bsp\\_io\\_port\\_pin\\_t](#)

### Enumeration Type Documentation

#### ◆ [bsp\\_io\\_level\\_t](#)

enum <a href="#">bsp_io_level_t</a>	
Levels that can be set and read for individual pins	
Enumerator	
BSP_IO_LEVEL_LOW	Low.
BSP_IO_LEVEL_HIGH	High.

#### ◆ [bsp\\_io\\_direction\\_t](#)

enum <a href="#">bsp_io_direction_t</a>	
Direction of individual pins	
Enumerator	
BSP_IO_DIRECTION_INPUT	Input.
BSP_IO_DIRECTION_OUTPUT	Output.

◆ **bsp\_io\_port\_t**

enum <code>bsp_io_port_t</code>	
Superset list of all possible IO ports.	
Enumerator	
<code>BSP_IO_PORT_00</code>	IO port 0.
<code>BSP_IO_PORT_01</code>	IO port 1.
<code>BSP_IO_PORT_02</code>	IO port 2.
<code>BSP_IO_PORT_03</code>	IO port 3.
<code>BSP_IO_PORT_04</code>	IO port 4.
<code>BSP_IO_PORT_05</code>	IO port 5.
<code>BSP_IO_PORT_06</code>	IO port 6.
<code>BSP_IO_PORT_07</code>	IO port 7.
<code>BSP_IO_PORT_08</code>	IO port 8.
<code>BSP_IO_PORT_09</code>	IO port 9.
<code>BSP_IO_PORT_10</code>	IO port 10.
<code>BSP_IO_PORT_11</code>	IO port 11.

◆ **bsp\_io\_port\_pin\_t**

enum <code>bsp_io_port_pin_t</code>	
Superset list of all possible IO port pins.	
Enumerator	
<code>BSP_IO_PORT_00_PIN_00</code>	IO port 0 pin 0.
<code>BSP_IO_PORT_00_PIN_01</code>	IO port 0 pin 1.
<code>BSP_IO_PORT_00_PIN_02</code>	IO port 0 pin 2.
<code>BSP_IO_PORT_00_PIN_03</code>	IO port 0 pin 3.
<code>BSP_IO_PORT_00_PIN_04</code>	IO port 0 pin 4.

BSP_IO_PORT_00_PIN_05	IO port 0 pin 5.
BSP_IO_PORT_00_PIN_06	IO port 0 pin 6.
BSP_IO_PORT_00_PIN_07	IO port 0 pin 7.
BSP_IO_PORT_00_PIN_08	IO port 0 pin 8.
BSP_IO_PORT_00_PIN_09	IO port 0 pin 9.
BSP_IO_PORT_00_PIN_10	IO port 0 pin 10.
BSP_IO_PORT_00_PIN_11	IO port 0 pin 11.
BSP_IO_PORT_00_PIN_12	IO port 0 pin 12.
BSP_IO_PORT_00_PIN_13	IO port 0 pin 13.
BSP_IO_PORT_00_PIN_14	IO port 0 pin 14.
BSP_IO_PORT_00_PIN_15	IO port 0 pin 15.
BSP_IO_PORT_01_PIN_00	IO port 1 pin 0.
BSP_IO_PORT_01_PIN_01	IO port 1 pin 1.
BSP_IO_PORT_01_PIN_02	IO port 1 pin 2.
BSP_IO_PORT_01_PIN_03	IO port 1 pin 3.
BSP_IO_PORT_01_PIN_04	IO port 1 pin 4.
BSP_IO_PORT_01_PIN_05	IO port 1 pin 5.
BSP_IO_PORT_01_PIN_06	IO port 1 pin 6.
BSP_IO_PORT_01_PIN_07	IO port 1 pin 7.
BSP_IO_PORT_01_PIN_08	IO port 1 pin 8.
BSP_IO_PORT_01_PIN_09	IO port 1 pin 9.
BSP_IO_PORT_01_PIN_10	IO port 1 pin 10.
BSP_IO_PORT_01_PIN_11	IO port 1 pin 11.
BSP_IO_PORT_01_PIN_12	IO port 1 pin 12.

BSP_IO_PORT_01_PIN_13	IO port 1 pin 13.
BSP_IO_PORT_01_PIN_14	IO port 1 pin 14.
BSP_IO_PORT_01_PIN_15	IO port 1 pin 15.
BSP_IO_PORT_02_PIN_00	IO port 2 pin 0.
BSP_IO_PORT_02_PIN_01	IO port 2 pin 1.
BSP_IO_PORT_02_PIN_02	IO port 2 pin 2.
BSP_IO_PORT_02_PIN_03	IO port 2 pin 3.
BSP_IO_PORT_02_PIN_04	IO port 2 pin 4.
BSP_IO_PORT_02_PIN_05	IO port 2 pin 5.
BSP_IO_PORT_02_PIN_06	IO port 2 pin 6.
BSP_IO_PORT_02_PIN_07	IO port 2 pin 7.
BSP_IO_PORT_02_PIN_08	IO port 2 pin 8.
BSP_IO_PORT_02_PIN_09	IO port 2 pin 9.
BSP_IO_PORT_02_PIN_10	IO port 2 pin 10.
BSP_IO_PORT_02_PIN_11	IO port 2 pin 11.
BSP_IO_PORT_02_PIN_12	IO port 2 pin 12.
BSP_IO_PORT_02_PIN_13	IO port 2 pin 13.
BSP_IO_PORT_02_PIN_14	IO port 2 pin 14.
BSP_IO_PORT_02_PIN_15	IO port 2 pin 15.
BSP_IO_PORT_03_PIN_00	IO port 3 pin 0.
BSP_IO_PORT_03_PIN_01	IO port 3 pin 1.
BSP_IO_PORT_03_PIN_02	IO port 3 pin 2.
BSP_IO_PORT_03_PIN_03	IO port 3 pin 3.
BSP_IO_PORT_03_PIN_04	IO port 3 pin 4.

BSP_IO_PORT_03_PIN_05	IO port 3 pin 5.
BSP_IO_PORT_03_PIN_06	IO port 3 pin 6.
BSP_IO_PORT_03_PIN_07	IO port 3 pin 7.
BSP_IO_PORT_03_PIN_08	IO port 3 pin 8.
BSP_IO_PORT_03_PIN_09	IO port 3 pin 9.
BSP_IO_PORT_03_PIN_10	IO port 3 pin 10.
BSP_IO_PORT_03_PIN_11	IO port 3 pin 11.
BSP_IO_PORT_03_PIN_12	IO port 3 pin 12.
BSP_IO_PORT_03_PIN_13	IO port 3 pin 13.
BSP_IO_PORT_03_PIN_14	IO port 3 pin 14.
BSP_IO_PORT_03_PIN_15	IO port 3 pin 15.
BSP_IO_PORT_04_PIN_00	IO port 4 pin 0.
BSP_IO_PORT_04_PIN_01	IO port 4 pin 1.
BSP_IO_PORT_04_PIN_02	IO port 4 pin 2.
BSP_IO_PORT_04_PIN_03	IO port 4 pin 3.
BSP_IO_PORT_04_PIN_04	IO port 4 pin 4.
BSP_IO_PORT_04_PIN_05	IO port 4 pin 5.
BSP_IO_PORT_04_PIN_06	IO port 4 pin 6.
BSP_IO_PORT_04_PIN_07	IO port 4 pin 7.
BSP_IO_PORT_04_PIN_08	IO port 4 pin 8.
BSP_IO_PORT_04_PIN_09	IO port 4 pin 9.
BSP_IO_PORT_04_PIN_10	IO port 4 pin 10.
BSP_IO_PORT_04_PIN_11	IO port 4 pin 11.
BSP_IO_PORT_04_PIN_12	IO port 4 pin 12.

BSP_IO_PORT_04_PIN_13	IO port 4 pin 13.
BSP_IO_PORT_04_PIN_14	IO port 4 pin 14.
BSP_IO_PORT_04_PIN_15	IO port 4 pin 15.
BSP_IO_PORT_05_PIN_00	IO port 5 pin 0.
BSP_IO_PORT_05_PIN_01	IO port 5 pin 1.
BSP_IO_PORT_05_PIN_02	IO port 5 pin 2.
BSP_IO_PORT_05_PIN_03	IO port 5 pin 3.
BSP_IO_PORT_05_PIN_04	IO port 5 pin 4.
BSP_IO_PORT_05_PIN_05	IO port 5 pin 5.
BSP_IO_PORT_05_PIN_06	IO port 5 pin 6.
BSP_IO_PORT_05_PIN_07	IO port 5 pin 7.
BSP_IO_PORT_05_PIN_08	IO port 5 pin 8.
BSP_IO_PORT_05_PIN_09	IO port 5 pin 9.
BSP_IO_PORT_05_PIN_10	IO port 5 pin 10.
BSP_IO_PORT_05_PIN_11	IO port 5 pin 11.
BSP_IO_PORT_05_PIN_12	IO port 5 pin 12.
BSP_IO_PORT_05_PIN_13	IO port 5 pin 13.
BSP_IO_PORT_05_PIN_14	IO port 5 pin 14.
BSP_IO_PORT_05_PIN_15	IO port 5 pin 15.
BSP_IO_PORT_06_PIN_00	IO port 6 pin 0.
BSP_IO_PORT_06_PIN_01	IO port 6 pin 1.
BSP_IO_PORT_06_PIN_02	IO port 6 pin 2.
BSP_IO_PORT_06_PIN_03	IO port 6 pin 3.
BSP_IO_PORT_06_PIN_04	IO port 6 pin 4.

BSP_IO_PORT_06_PIN_05	IO port 6 pin 5.
BSP_IO_PORT_06_PIN_06	IO port 6 pin 6.
BSP_IO_PORT_06_PIN_07	IO port 6 pin 7.
BSP_IO_PORT_06_PIN_08	IO port 6 pin 8.
BSP_IO_PORT_06_PIN_09	IO port 6 pin 9.
BSP_IO_PORT_06_PIN_10	IO port 6 pin 10.
BSP_IO_PORT_06_PIN_11	IO port 6 pin 11.
BSP_IO_PORT_06_PIN_12	IO port 6 pin 12.
BSP_IO_PORT_06_PIN_13	IO port 6 pin 13.
BSP_IO_PORT_06_PIN_14	IO port 6 pin 14.
BSP_IO_PORT_06_PIN_15	IO port 6 pin 15.
BSP_IO_PORT_07_PIN_00	IO port 7 pin 0.
BSP_IO_PORT_07_PIN_01	IO port 7 pin 1.
BSP_IO_PORT_07_PIN_02	IO port 7 pin 2.
BSP_IO_PORT_07_PIN_03	IO port 7 pin 3.
BSP_IO_PORT_07_PIN_04	IO port 7 pin 4.
BSP_IO_PORT_07_PIN_05	IO port 7 pin 5.
BSP_IO_PORT_07_PIN_06	IO port 7 pin 6.
BSP_IO_PORT_07_PIN_07	IO port 7 pin 7.
BSP_IO_PORT_07_PIN_08	IO port 7 pin 8.
BSP_IO_PORT_07_PIN_09	IO port 7 pin 9.
BSP_IO_PORT_07_PIN_10	IO port 7 pin 10.
BSP_IO_PORT_07_PIN_11	IO port 7 pin 11.
BSP_IO_PORT_07_PIN_12	IO port 7 pin 12.

BSP_IO_PORT_07_PIN_13	IO port 7 pin 13.
BSP_IO_PORT_07_PIN_14	IO port 7 pin 14.
BSP_IO_PORT_07_PIN_15	IO port 7 pin 15.
BSP_IO_PORT_08_PIN_00	IO port 8 pin 0.
BSP_IO_PORT_08_PIN_01	IO port 8 pin 1.
BSP_IO_PORT_08_PIN_02	IO port 8 pin 2.
BSP_IO_PORT_08_PIN_03	IO port 8 pin 3.
BSP_IO_PORT_08_PIN_04	IO port 8 pin 4.
BSP_IO_PORT_08_PIN_05	IO port 8 pin 5.
BSP_IO_PORT_08_PIN_06	IO port 8 pin 6.
BSP_IO_PORT_08_PIN_07	IO port 8 pin 7.
BSP_IO_PORT_08_PIN_08	IO port 8 pin 8.
BSP_IO_PORT_08_PIN_09	IO port 8 pin 9.
BSP_IO_PORT_08_PIN_10	IO port 8 pin 10.
BSP_IO_PORT_08_PIN_11	IO port 8 pin 11.
BSP_IO_PORT_08_PIN_12	IO port 8 pin 12.
BSP_IO_PORT_08_PIN_13	IO port 8 pin 13.
BSP_IO_PORT_08_PIN_14	IO port 8 pin 14.
BSP_IO_PORT_08_PIN_15	IO port 8 pin 15.
BSP_IO_PORT_09_PIN_00	IO port 9 pin 0.
BSP_IO_PORT_09_PIN_01	IO port 9 pin 1.
BSP_IO_PORT_09_PIN_02	IO port 9 pin 2.
BSP_IO_PORT_09_PIN_03	IO port 9 pin 3.
BSP_IO_PORT_09_PIN_04	IO port 9 pin 4.

BSP_IO_PORT_09_PIN_05	IO port 9 pin 5.
BSP_IO_PORT_09_PIN_06	IO port 9 pin 6.
BSP_IO_PORT_09_PIN_07	IO port 9 pin 7.
BSP_IO_PORT_09_PIN_08	IO port 9 pin 8.
BSP_IO_PORT_09_PIN_09	IO port 9 pin 9.
BSP_IO_PORT_09_PIN_10	IO port 9 pin 10.
BSP_IO_PORT_09_PIN_11	IO port 9 pin 11.
BSP_IO_PORT_09_PIN_12	IO port 9 pin 12.
BSP_IO_PORT_09_PIN_13	IO port 9 pin 13.
BSP_IO_PORT_09_PIN_14	IO port 9 pin 14.
BSP_IO_PORT_09_PIN_15	IO port 9 pin 15.
BSP_IO_PORT_10_PIN_00	IO port 10 pin 0.
BSP_IO_PORT_10_PIN_01	IO port 10 pin 1.
BSP_IO_PORT_10_PIN_02	IO port 10 pin 2.
BSP_IO_PORT_10_PIN_03	IO port 10 pin 3.
BSP_IO_PORT_10_PIN_04	IO port 10 pin 4.
BSP_IO_PORT_10_PIN_05	IO port 10 pin 5.
BSP_IO_PORT_10_PIN_06	IO port 10 pin 6.
BSP_IO_PORT_10_PIN_07	IO port 10 pin 7.
BSP_IO_PORT_10_PIN_08	IO port 10 pin 8.
BSP_IO_PORT_10_PIN_09	IO port 10 pin 9.
BSP_IO_PORT_10_PIN_10	IO port 10 pin 10.
BSP_IO_PORT_10_PIN_11	IO port 10 pin 11.
BSP_IO_PORT_10_PIN_12	IO port 10 pin 12.

BSP_IO_PORT_10_PIN_13	IO port 10 pin 13.
BSP_IO_PORT_10_PIN_14	IO port 10 pin 14.
BSP_IO_PORT_10_PIN_15	IO port 10 pin 15.
BSP_IO_PORT_11_PIN_00	IO port 11 pin 0.
BSP_IO_PORT_11_PIN_01	IO port 11 pin 1.
BSP_IO_PORT_11_PIN_02	IO port 11 pin 2.
BSP_IO_PORT_11_PIN_03	IO port 11 pin 3.
BSP_IO_PORT_11_PIN_04	IO port 11 pin 4.
BSP_IO_PORT_11_PIN_05	IO port 11 pin 5.
BSP_IO_PORT_11_PIN_06	IO port 11 pin 6.
BSP_IO_PORT_11_PIN_07	IO port 11 pin 7.
BSP_IO_PORT_11_PIN_08	IO port 11 pin 8.
BSP_IO_PORT_11_PIN_09	IO port 11 pin 9.
BSP_IO_PORT_11_PIN_10	IO port 11 pin 10.
BSP_IO_PORT_11_PIN_11	IO port 11 pin 11.
BSP_IO_PORT_11_PIN_12	IO port 11 pin 12.
BSP_IO_PORT_11_PIN_13	IO port 11 pin 13.
BSP_IO_PORT_11_PIN_14	IO port 11 pin 14.
BSP_IO_PORT_11_PIN_15	IO port 11 pin 15.

## Function Documentation

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◆ **R\_BSP\_PinRead()**

<code>__STATIC_INLINE uint32_t R_BSP_PinRead ( bsp_io_port_pin_t pin)</code>		
Read the current input level of the pin.		
<b>Parameters</b>		
[in]	pin	The pin
<b>Return values</b>		
Current	input level	

◆ **R\_BSP\_PinWrite()**

<code>__STATIC_INLINE void R_BSP_PinWrite ( bsp_io_port_pin_t pin, bsp_io_level_t level )</code>		
Set a pin to output and set the output level to the level provided. If PFS protection is enabled, disable PFS protection using <a href="#">R_BSP_PinAccessEnable()</a> before calling this function.		
<b>Parameters</b>		
[in]	pin	The pin
[in]	level	The level

◆ **R\_BSP\_PinCfg()**

<code>__STATIC_INLINE void R_BSP_PinCfg ( bsp_io_port_pin_t pin, uint32_t cfg )</code>		
Configure a pin. If PFS protection is enabled, disable PFS protection using <a href="#">R_BSP_PinAccessEnable()</a> before calling this function.		
<b>Parameters</b>		
[in]	pin	The pin
[in]	cfg	Configuration for the pin (PmnPFS register setting)

◆ **R\_BSP\_PinAccessEnable()**

<code>__STATIC_INLINE void R_BSP_PinAccessEnable ( void )</code>		
Enable access to the PFS registers. Uses a reference counter to protect against interrupts that could occur via multiple threads or an ISR re-entering this code.		

**◆ R\_BSP\_PinAccessDisable()**

```
__STATIC_INLINE void R_BSP_PinAccessDisable ( void )
```

Disable access to the PFS registers. Uses a reference counter to protect against interrupts that could occur via multiple threads or an ISR re-entering this code.

## 4.2 Modules

### Detailed Description

Modules are the smallest unit of software available in the FSP. Each module implements one interface.

For more information on FSP Modules and Interfaces review [FSP Modules](#), [FSP Stacks](#) and [FSP Interfaces](#) in the FSP Architecture section of this manual.

*Note*

*Not all modules are available for all MCUs. For more information, see the User's Manual for the specific MCU.*

### Organization of Module Sections

Each module within FSP has a detailed Users' Guide listed below. Each guide typically includes the following content:

- **Functions:** A list of all the API functions associated with the module
- **Detailed Description:** A short description of the module and the peripherals used
- **Overview:** An operational summary and a list of high level features provided by the module
- **Configuration:** A description of module specific settings available in the configuration tool including clock and pin configurations
- **Usage Notes:** Module specific documentation and limitations
- **Examples:** Illustrative code snippets that help the user better understand API use and operation
- **Data Structure and Enumeration:** Definitions for data structures, enumerations and similar elements used by the module API
- **Function Documentation:** Details on each API function, including the function prototype, a function summary, a simple use example, list of return values and links to documentation for any needed parameter definitions

### Modules

**High-Speed Analog Comparator (r\_acmphs)**

Driver for the ACPHPS peripheral on RA MCUs. This module implements the [Comparator Interface](#).

**Low-Power Analog Comparator (r\_acmplp)**

Driver for the ACMLP peripheral on RA MCUs. This module

implements the [Comparator Interface](#).

#### [Analog to Digital Converter \(r\\_adc\)](#)

Driver for the ADC12, ADC14, and ADC16 peripherals on RA MCUs. This module implements the [ADC Interface](#).

#### [Asynchronous General Purpose Timer \(r\\_agt\)](#)

Driver for the AGT peripheral on RA MCUs. This module implements the [Timer Interface](#).

#### [Bluetooth Low Energy Library \(r\\_ble\)](#)

Driver for the Radio peripheral on RA MCUs. This module implements the [BLE Interface](#).

#### [Clock Frequency Accuracy Measurement Circuit \(r\\_cac\)](#)

Driver for the CAC peripheral on RA MCUs. This module implements the [CAC Interface](#).

#### [Controller Area Network \(r\\_can\)](#)

Driver for the CAN peripheral on RA MCUs. This module implements the [CAN Interface](#).

#### [Controller Area Network - Flexible Data \(r\\_canfd\)](#)

Driver for the CANFD peripheral on RA MCUs. This module implements the [CAN Interface](#).

#### [Consumer Electronics Control \(r\\_cec\)](#)

Driver for the CEC peripheral on RA MCUs. This module implements the [CEC Interface](#).

#### [Clock Generation Circuit \(r\\_cgc\)](#)

Driver for the CGC peripheral on RA MCUs. This module implements the [CGC Interface](#).

#### [Cyclic Redundancy Check \(CRC\) Calculator \(r\\_crc\)](#)

Driver for the CRC peripheral on RA MCUs. This module implements the [CRC Interface](#).

### Capacitive Touch Sensing Unit (r\_ctsu)

This HAL driver supports the Capacitive Touch Sensing Unit (CTSU). It implements the [CTSU Interface](#).

### Digital to Analog Converter (r\_dac)

Driver for the DAC12 peripheral on RA MCUs. This module implements the [DAC Interface](#).

### Digital to Analog Converter (r\_dac8)

Driver for the DAC8 peripheral on RA MCUs. This module implements the [DAC Interface](#).

### Direct Memory Access Controller (r\_dmac)

Driver for the DMAC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

### Data Operation Circuit (r\_doc)

Driver for the DOC peripheral on RA MCUs. This module implements the [DOC Interface](#).

### D/AVE 2D Port Interface (r\_drw)

Driver for the DRW peripheral on RA MCUs. This module is a port of D/AVE 2D.

### Data Transfer Controller (r\_dtc)

Driver for the DTC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

### Event Link Controller (r\_elc)

Driver for the ELC peripheral on RA MCUs. This module implements the [ELC Interface](#).

### Ethernet (r\_ether)

Driver for the Ethernet peripheral on RA MCUs. This module implements the [Ethernet Interface](#).

### Ethernet PHY (r\_ether\_phy)

The Ethernet PHY module (`r_ether_phy`) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral. It implements the [Ethernet PHY Interface](#).

#### High-Performance Flash Driver (`r_flash_hp`)

Driver for the flash memory on RA high-performance MCUs. This module implements the [Flash Interface](#).

#### Low-Power Flash Driver (`r_flash_lp`)

Driver for the flash memory on RA low-power MCUs. This module implements the [Flash Interface](#).

#### Graphics LCD Controller (`r_glcdc`)

Driver for the GLCDC peripheral on RA MCUs. This module implements the [Display Interface](#).

#### General PWM Timer (`r_gpt`)

Driver for the GPT32 and GPT16 peripherals on RA MCUs. This module implements the [Timer Interface](#).

#### General PWM Timer Three-Phase Motor Control Driver (`r_gpt_three_phase`)

Driver for 3-phase motor control using the GPT peripheral on RA MCUs. This module implements the [Three-Phase Interface](#).

#### Interrupt Controller Unit (`r_icu`)

Driver for the ICU peripheral on RA MCUs. This module implements the [External IRQ Interface](#).

#### I2C Master on IIC (`r_iic_master`)

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

#### I2C Slave on IIC (`r_iic_slave`)

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Slave Interface](#).

#### I/O Ports (`r_ioport`)

Driver for the I/O Ports peripheral on RA MCUs. This module implements the [I/O Port Interface](#).

#### [Independent Watchdog Timer \(r\\_iwdt\)](#)

Driver for the IWDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

#### [JPEG Codec \(r\\_jpeg\)](#)

Driver for the JPEG peripheral on RA MCUs. This module implements the [JPEG Codec Interface](#).

#### [Key Interrupt \(r\\_kint\)](#)

Driver for the KINT peripheral on RA MCUs. This module implements the [Key Matrix Interface](#).

#### [Low Power Modes \(r\\_lpm\)](#)

Driver for the LPM peripheral on RA MCUs. This module implements the [Low Power Modes Interface](#).

#### [Low Voltage Detection \(r\\_lvd\)](#)

Driver for the LVD peripheral on RA MCUs. This module implements the [Low Voltage Detection Interface](#).

#### [Operational Amplifier \(r\\_opamp\)](#)

Driver for the OPAMP peripheral on RA MCUs. This module implements the [OPAMP Interface](#).

#### [Octa Serial Peripheral Interface Flash \(r\\_ospi\)](#)

Driver for the OSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

#### [Parallel Data Capture \(r\\_pdc\)](#)

Driver for the PDC peripheral on RA MCUs. This module implements the [PDC Interface](#).

#### [Port Output Enable for GPT \(r\\_poeg\)](#)

Driver for the POEG peripheral on RA MCUs. This module implements

the [POEG Interface](#).

#### [Precision Time Protocol \(r\\_ptp\)](#)

Driver for the PTP peripheral on RA MCUs. This module implements the [PTP Interface](#).

#### [Quad Serial Peripheral Interface Flash \(r\\_qspi\)](#)

Driver for the QSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

#### [Realtime Clock \(r\\_rtc\)](#)

Driver for the RTC peripheral on RA MCUs. This module implements the [RTC Interface](#).

#### [Secure Crypto Engine \(r\\_sce\\_protected\)](#)

Driver for the Secure Crypto Engine (SCE) on RA MCUs.

#### [Serial Communications Interface \(SCI\) I2C \(r\\_sci\\_i2c\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

#### [Serial Communications Interface \(SCI\) SPI \(r\\_sci\\_spi\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [SPI Interface](#).

#### [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)

Driver for the SCI peripheral on RA MCUs. This module implements the [UART Interface](#).

#### [Sigma Delta Analog to Digital Converter \(r\\_sdadc\)](#)

Driver for the SDADC24 peripheral on RA MCUs. This module implements the [ADC Interface](#).

#### [SD/MMC Host Interface \(r\\_sdhi\)](#)

Driver for the SD/MMC Host Interface (SDHI) peripheral on RA MCUs. This module implements the [SD/MMC Interface](#).

### Segment LCD Controller (r\_slcdc)

Driver for the SLCDC peripheral on RA MCUs. This module implements the [SLCDC Interface](#).

### Serial Peripheral Interface (r\_spi)

Driver for the SPI peripheral on RA MCUs. This module implements the [SPI Interface](#).

### Serial Sound Interface (r\_ssi)

Driver for the SSIE peripheral on RA MCUs. This module implements the [I2S Interface](#).

### USB (r\_usb\_basic)

Driver for the USB peripheral on RA MCUs. This module implements the [USB Interface](#).

### USB Composite Class (r\_usb\_composite)

### USB Host Communications Device Class Driver (r\_usb\_hcdc)

This module provides a USB Host Communications Device Class (HDCD) driver. It implements the [USB HDCD Interface](#).

### USB Host Human Interface Device Class Driver (r\_usb\_hhid)

This module provides a USB Host Human Interface Device Class Driver (HHID). It implements the [USB HHID Interface](#).

### USB Host Mass Storage Class Driver (r\_usb\_hmsc)

This module provides a USB Host Mass Storage Class (HMSC) driver. It implements the [USB HMSC Interface](#).

### USB Host Vendor Class (r\_usb\_hvnd)

### USB Peripheral Communications Device Class (r\_usb\_pcdc)

This module provides a USB Peripheral Communications Device Class Driver (PCDC). It implements the [USB PCDC Interface](#).

### USB Peripheral Human Interface Device Class (r\_usb\_phid)

This module is USB Peripheral Human Interface Device Class Driver

(PHID). It implements the [USB PHID Interface](#).

#### [USB Peripheral Mass Storage Class \(r\\_usb\\_pmsc\)](#)

This module provides a USB Peripheral Mass Storage Class (PMSC) driver. It implements the [USB PMSC Interface](#).

#### [USB Peripheral Vendor Class \(r\\_usb\\_pvnd\)](#)

#### [Watchdog Timer \(r\\_wdt\)](#)

Driver for the WDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

#### [ADPCM Decoder \(rm\\_adpcm\\_decoder\)](#)

Middleware to implement the ADPCM Audio Decoder. This module implements the [ADPCM Decoder Interface](#).

#### [Audio Playback with PWM \(rm\\_audio\\_playback\\_pwm\)](#)

Driver for the Audio Playback middleware on RA MCUs. This module implements the [AUDIO PLAYBACK Interface](#).

#### [AWS PKCS11 PAL \(rm\\_aws\\_pkcs11\\_pal\)](#)

PKCS#11 PAL layer implementation for use by FreeRTOS TLS.

#### [AWS PKCS11 PAL LITTLEFS \(rm\\_aws\\_pkcs11\\_pal\\_littlefs\)](#)

PKCS#11 PAL LittleFS layer implementation for use by FreeRTOS TLS.

#### [Bluetooth Low Energy Abstraction \(rm\\_ble\\_abs\)](#)

Middleware for the Bluetooth peripheral on RA MCUs. This module implements the [BLE ABS Interface](#).

#### [SD/MMC Block Media Implementation \(rm\\_block\\_media\\_sdmmc\)](#)

Middleware to implement the block media interface on SD cards. This module implements the [Block Media Interface](#).

#### [SPI Block Media Implementation \(rm\\_block\\_media\\_spi\)](#)

Middleware to implement the block media interface on SPI flash

memory. This module implements the [Block Media Interface](#).

#### [USB HMSC Block Media Implementation \(rm\\_block\\_media\\_usb\)](#)

Middleware to implement the block media interface on USB mass storage devices. This module implements the [Block Media Interface](#).

#### [User Block Media Implementation \(rm\\_block\\_media\\_user\)](#)

Middleware that implements a block media interface on the media of your choice. This module implements the [Block Media Interface](#).

#### [I2C Communicatons Middleware \(rm\\_comms\\_i2c\)](#)

Middleware to implement the I2C communications interface. This module implements the [Communicatons Middleware Interface](#).

#### [SEGGER emWin Port \(rm\\_emwin\\_port\)](#)

SEGGER emWin port for RA MCUs.

#### [Azure RTOS FileX Block Media I/O Driver \(rm\\_filex\\_block\\_media\)](#)

Middleware for the Azure RTOS FileX File System control using Block Media on RA MCUs.

#### [Azure RTOS FileX LevelX I/O Driver \(rm\\_filex\\_levelx\\_nor\)](#)

Middleware for the Azure RTOS FileX File System control using LevelX NOR on RA MCUs.

#### [FreeRTOS+FAT Port \(rm\\_freertos\\_plus\\_fat\)](#)

Middleware for the FAT File System control on RA MCUs.

#### [FreeRTOS Plus TCP \(rm\\_freertos\\_plus\\_tcp\)](#)

Middleware for using TCP on RA MCUs.

#### [FreeRTOS Port \(rm\\_freertos\\_port\)](#)

FreeRTOS port for RA MCUs.

#### [RTOS Context Management \(rm\\_tz\\_context\)](#)

RTOS Context Management for RA MCUs.

[Azure RTOS GUIX Port \(rm\\_guix\\_port\)](#)[HS300X Sensor Middleware \(rm\\_hs300x\)](#)

Middleware to implement the HS300X sensor interface. This module implements the [HS300X Middleware Interface](#).

[Azure RTOS LevelX NOR SPI Driver \(rm\\_levelx\\_nor\\_spi\)](#)

Middleware for using Azure RTOS LevelX on NOR SPI memory.

[LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#)

Middleware for the LittleFS File System control on RA MCUs.

[MCUboot Port \(rm\\_mcuboot\\_port\)](#)

MCUboot Port for RA MCUs.

[Motor Current \(rm\\_motor\\_current\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor current Interface](#).

[Motor Driver \(rm\\_motor\\_driver\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor driver Interface](#).

[Motor encoder vector control \(rm\\_motor\\_encoder\)](#)

Control a SPM motor on RA MCUs. This module implements the [Motor encoder vector control \(rm\\_motor\\_encoder\)](#).

[Motor Angle and Speed Estimation \(rm\\_motor\\_estimate\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor angle Interface](#).

[Motor Position \(rm\\_motor\\_position\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor position Interface](#).

[Motor Angle and Speed Calculation with an Encoder \(rm\\_motor\\_sense\\_encoder\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor angle Interface](#).

#### [Motor Sensorless Vector Control \(rm\\_motor\\_sensorless\)](#)

Usual control of a SPM motor on RA MCUs. This module implements the [Motor Sensorless Vector Control \(rm\\_motor\\_sensorless\)](#).

#### [Motor Speed \(rm\\_motor\\_speed\)](#)

Calculation process for the motor control on RA MCUs. This module implements the [Motor speed Interface](#).

#### [Azure RTOS NetX Secure Crypto Hardware Acceleration \(rm\\_netx\\_secure\\_crypto\)](#)

Hardware acceleration for the Netx Crypto implementation of the Microsoft Azure RTOS NetX Crypto API.

#### [Azure RTOS NetX Duo Ether Driver \(rm\\_netxduo\\_ether\)](#)

#### [Azure RTOS NetX Duo WiFi Driver \(rm\\_netxduo\\_wifi\)](#)

#### [Crypto Middleware \(rm\\_psa\\_crypto\)](#)

Hardware acceleration for the mbedCrypto implementation of the ARM PSA Crypto API.

#### [Azure RTOS ThreadX Port \(rm\\_threadx\\_port\)](#)

ThreadX port for RA MCUs.

#### [Intel TinyCrypt \(rm\\_tinycrypt\\_port\)](#)

AES128 Hardware acceleration for TinyCrypt on the RA2 family.

#### [Capacitive Touch Middleware \(rm\\_touch\)](#)

This module supports the Capacitive Touch Sensing Unit (CTSUS). It implements the [Touch Middleware Interface](#).

#### [USBX Porting Layer \(rm\\_usbx\\_port\)](#)

#### [Virtual EEPROM \(rm\\_vee\\_flash\)](#)

Virtual EEPROM on RA MCUs. This module implements the [Virtual EEPROM Interface](#).

### [AWS Device Provisioning](#)

AWS Device Provisioning example software.

### [AWS HTTPS](#)

This module provides the AWS HTTPS integration documentation.

### [AWS MQTT](#)

This module provides the AWS MQTT integration documentation.

### [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#)

Wifi and Socket implementation using the Silex SX-ULPGN WiFi module on RA MCUs.

### [AWS Secure Sockets](#)

This module provides the AWS Secure Sockets implementation.

### [ZMOD4XXX Sensor Middleware \(rm\\_zmod4xxx\)](#)

Middleware to implement the ZMOD4XXX sensor interface. This module implements the [ZMOD4XXX Middleware Interface](#).

## 4.2.1 High-Speed Analog Comparator (r\_acmphs)

### Modules

#### Functions

`fsp_err_t` [R\\_ACMPHS\\_Open](#) (`comparator_ctrl_t *p_ctrl`, `comparator_cfg_t const *const p_cfg`)

`fsp_err_t` [R\\_ACMPHS\\_OutputEnable](#) (`comparator_ctrl_t *const p_ctrl`)

`fsp_err_t` [R\\_ACMPHS\\_InfoGet](#) (`comparator_ctrl_t *const p_ctrl`, `comparator_info_t *const p_info`)

`fsp_err_t` [R\\_ACMPHS\\_StatusGet](#) (`comparator_ctrl_t *const p_ctrl`, `comparator_status_t *const p_status`)

`fsp_err_t` [R\\_ACMPHS\\_Close](#) (`comparator_ctrl_t *const p_ctrl`)

## Detailed Description

Driver for the ACMPHS peripheral on RA MCUs. This module implements the [Comparator Interface](#).

## Overview

### Features

The ACMPHS HAL module supports the following features:

- Callback on rising edge, falling edge or both
- Configurable debounce filter
- Option for comparator output on VCOOUT pin
- ELC event output

## Configuration

### Build Time Configurations for r\_acmphs

The following build time configurations are defined in fsp\_cfg/r\_acmphs\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > Comparator Driver on r\_acmphs

This module can be added to the Stacks tab via New Stack > Driver > Analog > Comparator Driver on r\_acmphs.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_comparator0	Module name.
Channel	Value must be a non-negative integer	0	Select the hardware channel.
Trigger Edge Selector	<ul style="list-style-type: none"> <li>• Rising</li> <li>• Falling</li> <li>• Both Edge</li> </ul>	Both Edge	The trigger specifies when a comparator callback event should occur. Unused if the interrupt priority is disabled or the callback is NULL.
Noise Filter	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• 8</li> <li>• 16</li> <li>• 32</li> </ul>	No Filter	Select the PCLK divisor for the hardware digital debounce filter. Larger divisors provide a longer debounce and

take longer for the output to update.

Maximum status retries (CMPMON)	Must be a valid non-negative integer between 2 and 32-bit maximum value	1024	Maximum number of status retries.
Output Polarity	<ul style="list-style-type: none"> <li>• Not Inverted</li> <li>• Inverted</li> </ul>	Not Inverted	When enabled comparator output is inverted. This affects the output read from <a href="#">R_ACMPHS_StatusGet()</a> , the pin output level, and the edge trigger.
Pin Output(VCOUT)	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Turn this on to include the output from this comparator on VCOUT. The comparator output on VCOUT is OR'd with output from all other ACMPHS and ACMPLP comparators.
Callback	Name must be a valid C symbol	NULL	Define this function in the application. It is called when the Trigger event occurs.
Comparator Interrupt Priority	MCU Specific Options		Select the interrupt priority for the comparator interrupt.
Analog Input Voltage Source (IVCMP)	MCU Specific Options		Select the Analog input voltage source. Channel mentioned in the options represents channel in ACMPHS
Reference Voltage Input Source (IVREF)	MCU Specific Options		Select the Analog reference voltage source. Channel mentioned in the options represents channel in ACMPHS

## Clock Configuration

The ACMPHS peripheral is clocked from PCLKB. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

Comparator output can be enabled or disabled on each channel individually. The VCOUT pin is a logical OR of all comparator outputs.

The IVCMpN pins are used as comparator inputs. The IVREFn pins are used as comparator reference

values.

## Usage Notes

### Noise Filter

When the noise filter is enabled, the ACMPHP0/ACMPHP1 signal is sampled three times based on the sampling clock selected. The filter clock frequency is determined by PCLKB and the `comparator_filter_t` setting.

### Output Polarity

If output polarity is configured as "Inverted" then the VCOOUT signal will be inverted and the `R_ACMPHS_StatusGet()` will return an inverted status.

### Limitations

- Once the analog comparator is configured, the program must wait for the stabilization time to elapse before using the comparator.
- When the noise filter is not enabled the hardware requires software debouncing of the output (two consecutive equal values). This is automatically managed in `R_ACMPHS_StatusGet` but may result in delay or an API error in rare edge cases.
- Constraints apply on the simultaneous use of ACMPHS analog input and ADC analog input. Refer to the "Usage Notes" section in your MCU's User's Manual for the ADC unit(s) for more details.
- To allow ACMPHS0 to cancel Software Standby mode or enter Snooze, set the CSTEN bit to 1 and the CDFS bits to 00 in the CMPCTL0 register.

## Examples

### Basic Example

The following is a basic example of minimal use of the ACMPHS. The comparator is configured to trigger a callback when the input rises above the internal reference voltage (VREF). A GPIO output acts as the comparator input and is externally connected to the IVCMP input of the ACMPHS.

```
/* Connect this control pin to the VCMP input of the comparator. This can be any GPIO
pin
 * that is not input only. */
#define ACMPHS_EXAMPLE_CONTROL_PIN (BSP_IO_PORT_05_PIN_03)
#define ADC_PGA_BYPASS_VALUE (0x9999)
volatile uint32_t g_comparator_events = 0U;
/* This callback is called when a comparator event occurs. */
void acmphs_example_callback (comparator_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_comparator_events++;
}
```

```
}  
void acmphs_example ()  
{  
    fsp_err_t err = FSP_SUCCESS;  
    /* Disable pin register write protection, if enabled */  
    R_BSP_PinAccessEnable();  
    /* Start with the VCMP pin low. This example assumes the comparator is configured to  
trigger  
    * when VCMP rises above VREF. */  
    (void) R_BSP_PinWrite(ACMPHS_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_LOW);  
    /* Initialize the ACMPHS module */  
    err = R_ACMPHS_Open(&g_comparator_ctrl, &g_comparator_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    assert(FSP_SUCCESS == err);  
    /* Bypass PGA on ADC unit 0.  
    * (See Table 50.2 "Input source configuration of the ACMPHS" in the RA6M3 User's  
Manual (R01UH0886EJ0100)) */  
    R_BSP_MODULE_START(FSP_IP_ADC, 0);  
    R_ADC0->ADPGACR = ADC_PGA_BYPASS_VALUE;  
    R_ADC0->ADPGADCR0 = 0;  
    /* Wait for the minimum stabilization wait time before enabling output. */  
    comparator_info_t info;  
    R_ACMPHS_InfoGet(&g_comparator_ctrl, &info);  
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);  
    /* Enable the comparator output */  
    (void) R_ACMPHS_OutputEnable(&g_comparator_ctrl);  
    /* Set the VCMP pin high. */  
    (void) R_BSP_PinWrite(ACMPHS_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_HIGH);  
    while (0 == g_comparator_events)  
    {  
        /* Wait for interrupt. */  
    }  
    comparator_status_t status;  
    /* Check status of comparator, Status will be COMPARATOR_STATE_OUTPUT_HIGH */
```

```
(void) R_ACMPHS_StatusGet (&g_comparator_ctrl, &status);
}
```

## Function Documentation

### ◆ R\_ACMPHS\_Open()

```
fsp_err_t R_ACMPHS_Open ( comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg )
```

Configures the comparator and starts operation. Callbacks and pin output are not active until `outputEnable()` is called. `comparator_api_t::outputEnable()` should be called after the output has stabilized. Implements `comparator_api_t::open()`.

Comparator inputs must be configured in the application code prior to calling this function.

#### Return values

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	An input pointer is NULL
FSP_ERR_INVALID_ARGUMENT	An argument is invalid. Window mode (COMPARATOR_MODE_WINDOW) and filter of 1 (COMPARATOR_FILTER_1) are not supported in this implementation.
FSP_ERR_ALREADY_OPEN	The control block is already open or the hardware lock is taken.

### ◆ R\_ACMPHS\_OutputEnable()

```
fsp_err_t R_ACMPHS_OutputEnable ( comparator_ctrl_t *const p_ctrl)
```

Enables the comparator output, which can be polled using `comparator_api_t::statusGet()`. Also enables pin output and interrupts as configured during `comparator_api_t::open()`. Implements `comparator_api_t::outputEnable()`.

#### Return values

FSP_SUCCESS	Comparator output is enabled.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMPHS\_InfoGet()**

```
fsp_err_t R_ACMPHS_InfoGet ( comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements `comparator_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMPHS\_StatusGet()**

```
fsp_err_t R_ACMPHS_StatusGet ( comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status )
```

Provides the operating status of the comparator. Implements `comparator_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Operating status of the comparator is provided in p_status.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_TIMEOUT	The debounce filter is off and 2 consecutive matching values were not read within 1024 attempts.

◆ **R\_ACMPHS\_Close()**

```
fsp_err_t R_ACMPHS_Close ( comparator_ctrl_t * p_ctrl)
```

Stops the comparator. Implements `comparator_api_t::close()`.

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

## 4.2.2 Low-Power Analog Comparator (r\_acmplp)

### Modules

#### Functions

fsp\_err\_t R\_ACMLP\_Open (comparator\_ctrl\_t \*const p\_ctrl, comparator\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_ACMLP\_OutputEnable (comparator\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t R\_ACMLP\_InfoGet (comparator\_ctrl\_t \*const p\_ctrl, comparator\_info\_t \*const p\_info)

fsp\_err\_t R\_ACMLP\_StatusGet (comparator\_ctrl\_t \*const p\_ctrl, comparator\_status\_t \*const p\_status)

fsp\_err\_t R\_ACMLP\_Close (comparator\_ctrl\_t \*const p\_ctrl)

#### Detailed Description

Driver for the ACMLP peripheral on RA MCUs. This module implements the [Comparator Interface](#).

## Overview

### Features

The ACMLP HAL module supports the following features:

- Normal mode or window mode
- Callback on rising edge, falling edge or both
- Configurable debounce filter
- Option for comparator output on VCOUT pin
- ELC event output

## Configuration

### Build Time Configurations for r\_acmplp

The following build time configurations are defined in fsp\_cfg/r\_acmplp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Reference Voltage Selection for ACMLP1	<ul style="list-style-type: none"> <li>• IVREF0</li> <li>• IVREF1</li> </ul>	IVREF1	ACMLP1 may optionally be

(Standard mode only)

configured to use IVREF0 as a reference input instead of IVREF1. Note that if IVREF0 is selected, ACMPLP0 and ACMPLP1 must use the same setting for IVREF.

### Configurations for Driver > Analog > Comparator Driver on r\_acmplp

This module can be added to the Stacks tab via New Stack > Driver > Analog > Comparator Driver on r\_acmplp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_comparator0	Module name.
Channel	Value must be a non-negative integer	0	Select the hardware channel.
Mode	<ul style="list-style-type: none"> <li>Standard</li> <li>Window</li> </ul>	Standard	In standard mode, comparator output is high if VCMP > VREF. In window mode, comparator output is high if VCMP is outside the range of VREF0 to VREF1.
Trigger	<ul style="list-style-type: none"> <li>Rising</li> <li>Falling</li> <li>Both Edge</li> </ul>	Both Edge	The trigger specifies when a comparator callback event should occur. Unused if the interrupt priority is disabled or the callback is NULL.
Filter	<ul style="list-style-type: none"> <li>No sampling (bypass)</li> <li>Sampling at PCLKB</li> <li>Sampling at PCLKB/8</li> <li>Sampling at PCLKB/32</li> </ul>	No sampling (bypass)	Select the PCLK divisor for the hardware digital debounce filter. Larger divisors provide a longer debounce and take longer for the output to update.
Output Polarity	<ul style="list-style-type: none"> <li>Not Inverted</li> <li>Inverted</li> </ul>	Not Inverted	When enabled comparator output is inverted. This affects the output read from <a href="#">R_ACMLP_StatusGet()</a> , the pin output level, and the edge trigger.
Pin Output (VCOUT)	<ul style="list-style-type: none"> <li>Disabled</li> </ul>	Disabled	Turn this on to include

	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>		the output from this comparator on VCOUT. The comparator output on VCOUT is OR'd with output from all other ACMPHS and ACMPLP comparators.
Vref (Standard mode only)	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If reference voltage selection is enabled then internal reference voltage is used as comparator input
Callback	Name must be a valid C symbol	NULL	Define this function in the application. It is called when the Trigger event occurs.
Comparator Interrupt Priority	MCU Specific Options		Select the interrupt priority for the comparator interrupt.
Analog Input Voltage Source (IVCMP)	MCU Specific Options		Select the comparator input source. Only options for the configured channel are valid.
Reference Voltage Input Source (IVREF)	MCU Specific Options		Select the comparator reference voltage source.  If channel 1 is selected and the 'Reference Voltage Selection (ACMPLP1)' config option is set to IVREF0, select one of the Channel 0 options. In all other cases, only options for the configured channel are valid.

## Clock Configuration

The ACMPLP peripheral is clocked from PCLKB. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

Comparator output can be enabled or disabled on each channel individually. The VCOUT pin is a logical OR of all comparator outputs.

The CMPINn pins are used as comparator inputs. The CMPREFn pins are used as comparator reference values.

## Usage Notes

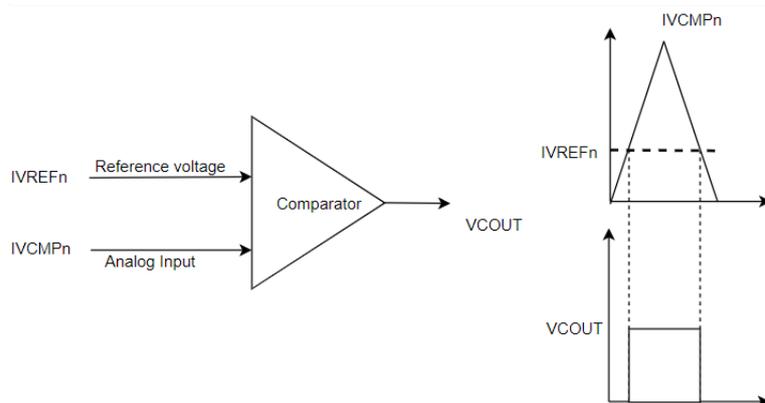


Figure 140: ACMLP Standard Mode Operation

### Noise Filter

When the noise filter is enabled, the ACMLP0/ACMLP1 signal is sampled three times based on the sampling clock selected. The filter clock frequency is determined by PCLKB and the comparator\_filter\_t setting.

### Output Polarity

If output polarity is configured as "Inverted" then the VCOUT signal will be inverted and the [R\\_ACMLP\\_StatusGet\(\)](#) will return an inverted status.

### Window Mode

In window mode, the comparator indicates if the analog input voltage falls within the window (low and high reference voltage) or is outside the window.

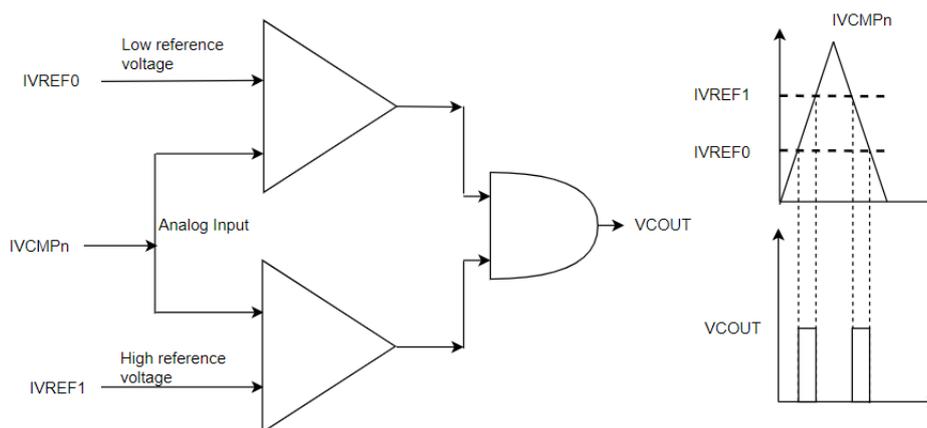


Figure 141: ACMLP Window Mode Operation

### Limitations

- Once the analog comparator is configured, the program must wait for the stabilization time to elapse before using the comparator.

- Low speed is not supported by the ACMPLP driver.

## Examples

### Basic Example

The following is a basic example of minimal use of the ACMPLP. The comparator is configured to trigger a callback when the input rises above the internal reference voltage (VREF). A GPIO output acts as the comparator input and is externally connected to the CMPIN input of the ACMPLP.

```
/* Connect this control pin to the VCMP input of the comparator. This can be any GPIO
pin
 * that is not input only. */
#define ACMPLP_EXAMPLE_CONTROL_PIN (BSP_IO_PORT_04_PIN_08)
volatile uint32_t g_comparator_events = 0U;
/* This callback is called when a comparator event occurs. */
void acmplp_example_callback (comparator_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_comparator_events++;
}
void acmplp_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /* Disable pin register write protection, if enabled */
    R_BSP_PinAccessEnable();
    /* Start with the VCMP pin low. This example assumes the comparator is configured to
trigger
 * when VCMP rises above VREF. */
    (void) R_BSP_PinWrite(ACMPLP_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_LOW);
    /* Initialize the ACMPLP module */
    err = R_ACMPLP_Open(&g_comparator_ctrl, &g_comparator_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Wait for the minimum stabilization wait time before enabling output. */
    comparator_info_t info;
    R_ACMPLP_InfoGet(&g_comparator_ctrl, &info);
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
```

```

/* Enable the comparator output */
(void) R_AC MPLP_OutputEnable(&g_comparator_ctrl);
/* Set VCMP low. */
(void) R_BSP_PinWrite(ACMPLP_EXAMPLE_CONTROL_PIN, BSP_IO_LEVEL_HIGH);
while (0 == g_comparator_events)
{
/* Wait for interrupt. */
}
comparator_status_t status;
/* Check status of comparator, Status will be COMPARATOR_STATE_OUTPUT_HIGH */
(void) R_AC MPLP_StatusGet(&g_comparator_ctrl, &status);
}

```

## Enumerations

enum [acmplp\\_input\\_t](#)

enum [acmplp\\_reference\\_t](#)

## Enumeration Type Documentation

### ◆ [acmplp\\_input\\_t](#)

enum <a href="#">acmplp_input_t</a>	
Enumerator	
ACMPLP_INPUT_AMPO	Not available on all MCUs.
ACMPLP_INPUT_CMPIN_1	Not available on all MCUs.

### ◆ [acmplp\\_reference\\_t](#)

enum <a href="#">acmplp_reference_t</a>	
Enumerator	
ACMPLP_REFERENCE_CMPREF_1	Not available on all MCUs.

## Function Documentation

◆ **R\_ACMLP\_Open()**

```
fsp_err_t R_ACMLP_Open ( comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg )
```

Configures the comparator and starts operation. Callbacks and pin output are not active until `outputEnable()` is called. `comparator_api_t::outputEnable()` should be called after the output has stabilized. Implements `comparator_api_t::open()`.

Comparator inputs must be configured in the application code prior to calling this function.

**Return values**

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	An input pointer is NULL
FSP_ERR_INVALID_ARGUMENT	An argument is invalid. Window mode (COMPARATOR_MODE_WINDOW) and filter of 1 (COMPARATOR_FILTER_1) are not supported in this implementation. <code>p_cfg-&gt;p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use callback function.
FSP_ERR_ALREADY_OPEN	The control block is already open or the hardware lock is taken.
FSP_ERR_IN_USE	The channel is already in use.

◆ **R\_ACMLP\_OutputEnable()**

```
fsp_err_t R_ACMLP_OutputEnable ( comparator_ctrl_t *const p_ctrl)
```

Enables the comparator output, which can be polled using `comparator_api_t::statusGet()`. Also enables pin output and interrupts as configured during `comparator_api_t::open()`. Implements `comparator_api_t::outputEnable()`.

**Return values**

FSP_SUCCESS	Comparator output is enabled.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_InfoGet()**

```
fsp_err_t R_ACMLP_InfoGet ( comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements [comparator\\_api\\_t::infoGet\(\)](#).

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_StatusGet()**

```
fsp_err_t R_ACMLP_StatusGet ( comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status )
```

Provides the operating status of the comparator. Implements [comparator\\_api\\_t::statusGet\(\)](#).

**Return values**

FSP_SUCCESS	Operating status of the comparator is provided in p_status.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_ACMLP\_Close()**

```
fsp_err_t R_ACMLP_Close ( comparator_ctrl_t * p_ctrl)
```

Stops the comparator. Implements [comparator\\_api\\_t::close\(\)](#).

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**4.2.3 Analog to Digital Converter (r\_adc)**

## Modules

## Functions

fsp\_err\_t R\_ADC\_Open (adc\_ctrl\_t \*p\_ctrl, adc\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_ADC\_ScanCfg (adc\_ctrl\_t \*p\_ctrl, void const \*const p\_channel\_cfg)

fsp\_err\_t R\_ADC\_InfoGet (adc\_ctrl\_t \*p\_ctrl, adc\_info\_t \*p\_adc\_info)

fsp\_err\_t R\_ADC\_ScanStart (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_ADC\_ScanStop (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_ADC\_StatusGet (adc\_ctrl\_t \*p\_ctrl, adc\_status\_t \*p\_status)

fsp\_err\_t R\_ADC\_Read (adc\_ctrl\_t \*p\_ctrl, adc\_channel\_t const reg\_id, uint16\_t \*const p\_data)

fsp\_err\_t R\_ADC\_Read32 (adc\_ctrl\_t \*p\_ctrl, adc\_channel\_t const reg\_id, uint32\_t \*const p\_data)

fsp\_err\_t R\_ADC\_SampleStateCountSet (adc\_ctrl\_t \*p\_ctrl, adc\_sample\_state\_t \*p\_sample)

fsp\_err\_t R\_ADC\_Close (adc\_ctrl\_t \*p\_ctrl)

fsp\_err\_t R\_ADC\_OffsetSet (adc\_ctrl\_t \*const p\_ctrl, adc\_channel\_t const reg\_id, int32\_t offset)

fsp\_err\_t R\_ADC\_Calibrate (adc\_ctrl\_t \*const p\_ctrl, void \*const p\_extend)

fsp\_err\_t R\_ADC\_CallbackSet (adc\_ctrl\_t \*const p\_api\_ctrl, void(\*p\_callback)(adc\_callback\_args\_t \*), void const \*const p\_context, adc\_callback\_args\_t \*const p\_callback\_memory)

## Detailed Description

Driver for the ADC12, ADC14, and ADC16 peripherals on RA MCUs. This module implements the [ADC Interface](#).

## Overview

### Features

The ADC module supports the following features:

- 12, 14, or 16 bit maximum resolution depending on the MCU
- Configure scans to include:
  - Multiple analog channels
  - Temperature sensor channel

- Voltage sensor channel
- Configurable scan start trigger:
  - Software scan triggers
  - Hardware scan triggers (timer expiration, for example)
  - External scan triggers from the ADTRGn port pins
- Configurable scan mode:
  - Single scan mode, where each trigger starts a single scan
  - Continuous scan mode, where all channels are scanned continuously
  - Group scan mode, where channels are grouped into group A and group B. The groups can be assigned different start triggers, and group A can be given priority over group B. When group A has priority over group B, a group A trigger suspends an ongoing group B scan.
- Supports adding and averaging converted samples
- Optional callback when scan completes
- Supports reading converted data
- Sample and hold support
- Double-trigger support

## Configuration

### Build Time Configurations for r\_adc

The following build time configurations are defined in fsp\_cfg/r\_adc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > ADC Driver on r\_adc

This module can be added to the Stacks tab via New Stack > Driver > Analog > ADC Driver on r\_adc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_adc0	Module name
General > Unit	Unit must be a non-negative integer	0	Specifies the ADC Unit to be used.
General > Resolution	MCU Specific Options		Specifies the conversion resolution for this unit.
General > Alignment	MCU Specific Options		Specifies the conversion result alignment.
General > Clear after read	<ul style="list-style-type: none"> <li>• Off</li> <li>• On</li> </ul>	On	Specifies if the result register will be

			automatically cleared after the conversion result is read.
General > Mode	<ul style="list-style-type: none"> <li>• Single Scan</li> <li>• Continuous Scan</li> <li>• Group Scan</li> </ul>	Single Scan	Specifies the mode that this ADC unit is used in.
General > Double-trigger	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> <li>• Enabled (extended mode)</li> </ul>	Disabled	<p>When enabled, the scan-end interrupt for Group A is only thrown on every second scan. Extended double-trigger mode (single-scan only) triggers on both ELC events, allowing (for example) a scan on two different timer compare match values.</p> <p>In group mode Group B is unaffected.</p>
Input > Sample and Hold > Sample and Hold Channels (Available only on selected MCUs)	<ul style="list-style-type: none"> <li>• Channel 0</li> <li>• Channel 1</li> <li>• Channel 2</li> </ul>		Specifies if this channel is included in the Sample and Hold Mask.
Input > Sample and Hold > Sample Hold States (Applies only to channels 0, 1, 2)	Must be a valid non-negative integer with configurable value 4 to 255	24	Specifies the updated sample-and-hold count for the channel dedicated sample-and-hold circuit
Input > Channel Scan Mask (channel availability varies by MCU)	Refer to the RA Configuration tool for available options.		In Normal mode of operation, this bitmask field specifies the channels that are enabled in that ADC unit. In group mode, this field specifies which channels belong to group A.
Input > Group B Scan Mask (channel availability varies by MCU)	Refer to the RA Configuration tool for available options.		In group mode, this field specifies which channels belong to group B.
Input > Add/Average Count	MCU Specific Options		Specifies if addition or averaging needs to be done for any of the channels in this unit.

Input > Reference Voltage control	MCU Specific Options		Specify VREFH/VREFADC output voltage control.
Input > Addition/Averaging Mask (channel availability varies by MCU and unit)	Refer to the RA Configuration tool for available options.		Select channels to include in the Addition/Averaging Mask
Interrupts > Normal/Group A Trigger	MCU Specific Options		Specifies the trigger type to be used for this unit.
Interrupts > Group B Trigger	MCU Specific Options		Specifies the trigger for Group B scanning in group scanning mode. This event is also used to trigger Group A in extended double-trigger mode.
Interrupts > Group Priority (Valid only in Group Scan Mode)	<ul style="list-style-type: none"> <li>Group A cannot interrupt Group B</li> <li>Group A can interrupt Group B; Group B scan restarts at next trigger</li> <li>Group A can interrupt Group B; Group B scan restarts immediately</li> <li>Group A can interrupt Group B; Group B scan restarts immediately and scans continuously</li> </ul>	Group A cannot interrupt Group B	Determines whether an ongoing group B scan can be interrupted by a group A trigger, whether it should abort on a group A trigger, or if it should pause to allow group A scan and restart immediately after group A scan is complete.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the ADC scan completes.
Interrupts > Scan End Interrupt Priority	MCU Specific Options		Select scan end interrupt priority.
Interrupts > Scan End Group B Interrupt	MCU Specific Options		Select group B scan end interrupt priority.

**Priority**

Extra &gt; ADC Ring Buffer

MCU Specific Options

ADC Ring Buffer to be used only with DMAC transfers, keep this property disabled for normal ADC operations. When enabled, ADC converted data is stored in ADBUF registers in place of ADDR registers. The read API will not read from this location for normal ADC operations.

**Clock Configuration**

The ADC clock is PCLKC if the MCU has PCLKC, or PCLKD otherwise.

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKD
RA2E1	PCLKD
RA2L1	PCLKD
RA4M1	PCLKC
RA4M2	PCLKC
RA4M3	PCLKC
RA4W1	PCLKC
RA6M1	PCLKC
RA6M2	PCLKC
RA6M3	PCLKC
RA6M4	PCLKC
RA6M5	PCLKC
RA6T1	PCLKC

The ADC clock must be at least 1 MHz when the ADC is used. Many MCUs also have PCLK ratio restrictions when the ADC is used. For details on PCLK ratio restrictions, reference the footnotes in the second table of the Clock Generation Circuit chapter of the MCU User's Manual (for example, Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100).

**Pin Configuration**

The ANxxx pins are analog input channels that can be used with the ADC.

ADTRG0 and ADTRG1 can be used to start scans with an external trigger for unit 0 and 1

respectively. When external triggers are used, ADC scans begin on the falling edge of the ADTRG pin.

## Usage Notes

### Sample Hold

Enabling the sample and hold functionality reduces the maximum scan frequency because the sample and hold time is added to each scan. Refer to the hardware manual for details on the sample and hold time.

### ADC Operational Modes

The driver supports three operation modes: single-scan, continuous-scan, and group-scan modes. In each mode, analog channels are converted in ascending order of channel number, followed by scans of the temperature sensor and voltage sensor if they are included in the mask of channels to scan.

#### Single-scan Mode

In single scan mode, one or more specified channels are scanned once per trigger.

#### Continuous-scan Mode

In continuous scan mode, a single trigger is required to start the scan. Scans continue until [R\\_ADC\\_ScanStop\(\)](#) is called.

#### Group-scan Mode

Group-scan mode allows the application to allocate channels to one of two groups (A and B). Conversion begins when the specified ELC start trigger for that group is received.

With the priority configuration parameter, you can optionally give group A priority over group B. If group A has priority over group B, a group B scan is interrupted when a group A scan trigger occurs. The following options exist for group B when group A has priority:

- To restart the interrupted group B scan after the group A scan completes.
- To wait for another group B trigger and forget the interrupted scan.
- To continuously scan group B and suspend scanning group B only when a group A trigger is received.

*Note*

*If this option is selected, group B scanning begins immediately after [R\\_ADC\\_ScanCfg\(\)](#). Group A scan triggers must be enabled by [R\\_ADC\\_ScanStart\(\)](#) and can be disabled by [R\\_ADC\\_ScanStop\(\)](#). Group B scans can only be disabled by reconfiguring the group A priority to a different mode.*

#### Double-triggering

When double-triggering is enabled a single channel is selected to be scanned twice before an interrupt is thrown. The first scan result when using double-triggering is always saved to the selected channel's data register. The second result is saved to the data duplexing register ([ADC\\_CHANNEL\\_DUPLEX](#)).

Double-triggering uses Group A; only one channel can be selected when enabled. No other scanning is possible on Group A while double-trigger mode is selected. In addition, any special ADC channels

(such as temperature sensors or voltage references) are not valid double-trigger channels.

When extended double-triggering is enabled both ADC input events are routed to Group A. The interrupt is still thrown after every two scans regardless of the triggering event(s). While the first and second scan are saved to the selected ADC data register and the ADC duplexing register as before, scans associated with event A and B are additionally copied into duplexing register A and B, respectively (`ADC_CHANNEL_DUPLEX_A` and `ADC_CHANNEL_DUPLEX_B`).

### When Interrupts Are Not Enabled

If interrupts are not enabled, the `R_ADC_StatusGet` API can be used to poll the ADC to determine when the scan has completed. The read API function is used to access the converted ADC result. This applies to both normal scans and calibration scans for MCUs that support calibration.

### Sample-State Count Setting

The application program can modify the setting of the sample-state count for analog channels by calling the `R_ADC_SampleStateCountSet()` API function. The application program only needs to modify the sample-state count settings from their default values to increase the sampling time. This can be either because the impedance of the input signal is too high to secure sufficient sampling time under the default setting or if the ADCLK is too slow. To modify the sample-state count for a given channel, set the channel number and the number of states when calling the `R_ADC_SampleStateCountSet()` API function. Valid sample state counts are 7-255.

#### Note

*Although the hardware supports a minimum number of sample states of 5, some MCUs require 7 states, so the minimum is set to 7. At the lowest supported ADC conversion clock rate (1 MHz), these extra states will lead to, at worst case, a 2 microsecond increase in conversion time. At 60 MHz the extra states will add 33.4 ns to the conversion time.*

If the sample state count needs to be changed for multiple channels, the application program must call the `R_ADC_SampleStateCountSet()` API function repeatedly, with appropriately modified arguments for each channel.

If the ADCLK frequency changes, the sample states may need to be updated.

### Sample States for Temperature Sensor and Internal Voltage Reference

Sample states for the temperature sensor and the internal reference voltage are calculated during `R_ADC_ScanCfg()` based on the ADCLK frequency at the time. The sample states for the temperature sensor and internal voltage reference cannot be updated with `R_ADC_SampleStateCountSet()`. If the ADCLK frequency changes, call `R_ADC_ScanCfg()` before using the temperature sensor or internal reference voltage again to ensure the sampling time for the temperature sensor and internal voltage reference is optimal.

### Selecting Reference Voltage

The ADC16 can select VREFH0 or VREFADC as the high-potential reference voltage on selected MCU's. When using VREFADC stabilization time of 1500us is required after call for `R_ADC_Open()`.

### Using the Temperature Sensor with the ADC

The ADC HAL module supports reading the data from the on-chip temperature sensor. The value returned from the sensor can be converted into degrees Celsius or Fahrenheit in the application program using the following formula,  $T = (V_s - V_1)/\text{slope} + T_1$ , where:

- T: Measured temperature (degrees C)
- Vs: Voltage output by the temperature sensor at the time of temperature measurement (Volts)
- T1: Temperature experimentally measured at one point (degrees C)
- V1: Voltage output by the temperature sensor at the time of measurement of T1 (Volts)
- T2: Temperature at the experimental measurement of another point (degrees C)
- V2: Voltage output by the temperature sensor at the time of measurement of T2 (Volts)
- Slope: Temperature gradient of the temperature sensor (V/degrees C); slope = (V2 - V1)/(T2 - T1)

#### Note

The slope value can be obtained from the hardware manual for each device in the *Electrical Characteristics Chapter - TSN Characteristics Table, Temperature slope entry*.

## Reading CTSU TSCAP with ADC

Some MCUs support reading CTSU TSCAP with ADC. CTSU TSCAP is connected to ADC0 channel 16. Use existing enums for channel 16 to set sample states for the sensor connected to CTSU TSCAP, enable scanning of CTSU TSCAP, and read results for CTSU TSCAP.

## Usage Notes for ADC16

### Calibration

Calibration is required to use the ADC16 peripheral. When using this driver on an MCU that has ADC16, call [R\\_ADC\\_Calibrate\(\)](#) after open, and prior to any other function.

### Range of ADC16 Results

The range of the ADC16 is from 0 (lowest) to 0x7FFF (highest) when used in single-ended mode. This driver only supports single ended mode.

## Examples

### Basic Example

This is a basic example of minimal use of the ADC in an application.

```
/* A channel configuration is generated by the RA Configuration editor based on the
options selected. If additional
* configurations are desired additional adc_channel_cfg_t elements can be defined
and passed to R_ADC_ScanCfg. */
const adc_channel_cfg_t g_adc0_channel_cfg =
{
    .scan_mask          = ADC_MASK_CHANNEL_0 | ADC_MASK_CHANNEL_1,
    .scan_mask_group_b = 0,
    .priority_group_a   = (adc_group_a_t) 0,
    .add_mask           = 0,
```

```
.sample_hold_mask    = 0,
.sample_hold_states = 0,
};
void adc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable channels. */
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    assert(FSP_SUCCESS == err);
    /* In software trigger mode, start a scan by calling R_ADC_ScanStart(). In other
modes, enable external
    * triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);
    /* Wait for conversion to complete. */
    adc_status_t status;
    status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
    {
        (void) R_ADC_StatusGet(&g_adc0_ctrl, &status);
    }
    /* Read converted data. */
    uint16_t channel1_conversion_result;
    err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_1, &channel1_conversion_result);
    assert(FSP_SUCCESS == err);
}
```

## Temperature Sensor Example

This example shows how to calculate the MCU temperature using the ADC and the temperature sensor.

```
#define ADC_EXAMPLE_CALIBRATION_DATA_RA6M1 (0x7D5)
#define ADC_EXAMPLE_VCC_MICROVOLT (3300000)
#define ADC_EXAMPLE_TEMPERATURE_RESOLUTION (12U)
#define ADC_EXAMPLE_REFERENCE_CALIBRATION_TEMPERATURE (127)
void adc_temperature_example (void)
{
    /* The following example calculates the temperature on an RA6M1 device using the
    data provided in the section
    * 44.3.1 "Preparation for Using the Temperature Sensor" of the RA6M1 manual
    R01UH0884EJ0100. */
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable temperature sensor. */
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
    assert(FSP_SUCCESS == err);
    /* In software trigger mode, start a scan by calling R_ADC_ScanStart(). In other
    modes, enable external
    * triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);
    /* Wait for conversion to complete. */
    adc_status_t status;
    status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
    {
        (void) R_ADC_StatusGet(&g_adc0_ctrl, &status);
    }
    /* Read converted data. */
    uint16_t temperature_conversion_result;
    err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_TEMPERATURE,
    &temperature_conversion_result);
    assert(FSP_SUCCESS == err);
}
```

```
/* If the MCU does not provide calibration data, use the value in the hardware
manual or determine it
* experimentally. */
/* Get Calibration data from the MCU if available. */
int32_t    reference_calibration_data;
adc_info_t adc_info;
(void) R_ADC_InfoGet(&g_adc0_ctrl, &adc_info);
reference_calibration_data = (int32_t) adc_info.calibration_data;
/* NOTE: The slope of the temperature sensor varies from sensor to sensor. Renesas
recommends calculating
* the slope of the temperature sensor experimentally.
*
* This example uses the typical slope provided in Table 52.38 "TSN characteristics"
in the RA6M1 manual
* R01UM0011EU0050. */
int32_t slope_uv_per_c = BSP_FEATURE_ADC_TSN_SLOPE;
/* Formula for calculating temperature copied from section 44.3.1 "Preparation for
Using the Temperature Sensor"
* of the RA6M1 manual R01UH0884EJ0100:
*
* In this MCU, the TSCDR register stores the temperature value (CAL127) of the
temperature sensor measured
* under the condition Ta = Tj = 127 C and AVCC0 = 3.3 V. By using this value as the
sample measurement result
* at the first point, preparation before using the temperature sensor can be
omitted.
*
* If V1 is calculated from CAL127,
* V1 = 3.3 * CAL127 / 4096 [V]
*
* Using this, the measured temperature can be calculated according to the following
formula.
*
* T = (Vs - V1) / Slope + 127 [C]
```

```

* T: Measured temperature (C)
* Vs: Voltage output by the temperature sensor when the temperature is measured (V)
* V1: Voltage output by the temperature sensor when Ta = Tj = 127 C and AVCC0 = 3.3
V (V)
* Slope: Temperature slope given in Table 52.38 / 1000 (V/C)
*/
int32_t v1_uv = (ADC_EXAMPLE_VCC_MICROVOLT >> ADC_EXAMPLE_TEMPERATURE_RESOLUTION)
*
reference_calibration_data;
int32_t vs_uv = (ADC_EXAMPLE_VCC_MICROVOLT >> ADC_EXAMPLE_TEMPERATURE_RESOLUTION)
*
temperature_conversion_result;
int32_t temperature_c = (vs_uv - v1_uv) / slope_uv_per_c +
ADC_EXAMPLE_REFERENCE_CALIBRATION_TEMPERATURE;
/* Expect room temperature, break if temperature is outside the range of 20 C to 25
C. */
if ((temperature_c < 20) || (temperature_c > 25))
{
__BKPT(0);
}
}

```

## Double-Trigger Example

This example demonstrates reading data from a double-trigger scan. A flag is used to wait for a callback event. Two scans must occur before the callback is called. These results are read via [R\\_ADC\\_Read](#) using the selected channel enum value as well as [ADC\\_CHANNEL\\_DUPLEX](#).

```

volatile bool scan_complete_flag = false;
void adc_callback (adc_callback_args_t * p_args)
{
FSP_PARAMETER_NOT_USED(p_args);
scan_complete_flag = true;
}
void adc_double_trigger_example (void)
{

```

```
fsp_err_t err = FSP_SUCCESS;

/* Initialize the module. */
err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Enable double-trigger channel. */
err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
assert(FSP_SUCCESS == err);

/* Enable scan triggering from ELC events. */
(void) R_ADC_ScanStart(&g_adc0_ctrl);

/* Wait for conversion to complete. Two scans must be triggered before a callback
occurs. */
scan_complete_flag = false;
while (!scan_complete_flag)
{
/* Wait for callback to set flag. */
}

/* Read converted data from both scans. */
uint16_t channel1_conversion_result_0;
uint16_t channel1_conversion_result_1;
err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_1, &channel1_conversion_result_0);
assert(FSP_SUCCESS == err);
err = R_ADC_Read(&g_adc0_ctrl, ADC_CHANNEL_DUPLEX,
&channel1_conversion_result_1);
assert(FSP_SUCCESS == err);
}
```

### ADC-DMAC Repeat-Block Transfer Example

This example demonstrates writing multiple data from DAC peripheral to ADC channels and storing the data in memory through DMAC using Repeat-Block Transfer mode. It creates single block to multiple ring buffer type of transfer topology. Ping-Pong mechanism is used to read the data from memory in between the transfers. This example is valid only for MCUs that have ADBUF.

```
#define ADC_DMACH_EXAMPLE_DATA_LOW (0U)
#define ADC_DMACH_EXAMPLE_DATA_HIGH (0x000FU)
```

```
#define ADC_DMAC_EXAMPLE_DELAY_1000_MS (1000U)
#define ADC_DMAC_EXAMPLE_NUM_PING_PONG_BUFFERS (2)
static uint16_t g_adc_dmac_example_buffer[ADC_DMAC_EXAMPLE_NUM_PING_PONG_BUFFERS][
    ADC_DMAC_EXAMPLE_ADC_CHANNELS_PER_BLOCK][ADC_DMAC_EXAMPLE_SAMPLES_PER_CHANNEL];
// Destination buffer for DMAC transfers
static volatile uint16_t g_adc_dmac_example_ping_pong_index = 0U;
static volatile void * gp_read_data;
/* DMAC callback */
void adc_dmac_callback (dmac_callback_args_t * p_args)
{
    (void) p_args;
    /* Store the pointer to the last buffer that was written
     * An array of data for the first enabled channel is at
    &g_adc_dmac_example_buffer[g_adc_dmac_example_ping_pong_index][0][0],
     * an array of data for the next channel is at
    &g_adc_dmac_example_buffer[g_adc_dmac_example_ping_pong_index][1][0], etc.
     */
    gp_read_data =
    &g_adc_dmac_example_buffer[g_adc_dmac_example_ping_pong_index][0][0];
    /* Select the other ping-pong buffer which is free for writing */
    g_adc_dmac_example_ping_pong_index = !g_adc_dmac_example_ping_pong_index;
    /* Reset the destination pointer and DMAC peripheral */
    R_DMAC_Reset(&g_transfer0_ctrl,
        NULL,
        (void *)
    &g_adc_dmac_example_buffer[g_adc_dmac_example_ping_pong_index][0][0],
        ADC_DMAC_EXAMPLE_SAMPLES_PER_CHANNEL);
    FSP_PARAMETER_NOT_USED(gp_read_data);
}
void adc_dmac_repeat_block_transfer_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Open ADC Module and configure the channels */
    /* Enable the ADBUF property from configurations */
```

```
err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
assert(FSP_SUCCESS == err);
err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
assert(FSP_SUCCESS == err);
/* Open DMAC channel for repeat-block transfer with following configurations
 * (1) Destination address as
&g_adc_dmac_example_buffer[g_adc_dmac_example_ping_pong_index][0][0]
 * (2) Enable end of transfer interrupt
 * (3) Configure source address mode as incremented and destination address mode as
offset addition,
 * fixed to address of ADBUF register by configurator with ADC-DMAC module
 * (4) Configure source buffer size as total size of source buffer - Refer RA6M4
Hardware Manual R01UH0890EJ0110,
 * section 16.2.15 for source buffer size limitations
 * (5) Configure transfer mode as Repeat-Block mode
 * (6) Refer RA6M4 Hardware Manual R01UH0890EJ0110,
 * section 16.2.16 for total number of blocks which decides destination buffer size
 * (7) Number of blocks is determined by the samples per channel property for ADC-
DMAC module
 * (8) Size of block is determined using the enabled ADC channels in the
configurator when using ADC-DMAC-module
 * (9) Configure DMAC activation source as A/D scan end interrupt
 */
err = R_DMACE_Open(&g_transfer0_ctrl, &g_transfer0_cfg);
assert(FSP_SUCCESS == err);
err = R_DMACE_Enable(&g_transfer0_ctrl);
assert(FSP_SUCCESS == err);
uint16_t count = ADC_DMACE_EXAMPLE_DATA_LOW;
adc_status_t adc_status;
/* Trigger the ADC scan for "count" times, this can be replaced by triggering the
ADC using a timer */
while (count <= (uint16_t) ADC_DMACE_EXAMPLE_DATA_HIGH)
{
/* Scan the data with ADC channels*/
```

```

    err = R_ADC_ScanStart(&g_adc0_ctrl);
    assert(FSP_SUCCESS == err);
    /* Wait for conversion to complete */
    uint16_t timeout = UINT16_MAX;
    adc_status.state = ADC_STATE_SCAN_IN_PROGRESS;
    while ((ADC_STATE_SCAN_IN_PROGRESS == adc_status.state) && (timeout > 0U))
    {
        timeout--;
        R_ADC_StatusGet(&g_adc0_ctrl, &adc_status);
    }
    R_BSP_SoftwareDelay(ADC_DMACEXAMPLE_DELAY_1000_MS, BSP_DELAY_UNITS_MICROSECONDS);
    count++;
}

```

## Data Structures

struct [adc\\_sample\\_state\\_t](#)

struct [adc\\_extended\\_cfg\\_t](#)

struct [adc\\_channel\\_cfg\\_t](#)

struct [adc\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [adc\\_mask\\_t](#)

enum [adc\\_add\\_t](#)

enum [adc\\_clear\\_t](#)

enum [adc\\_vref\\_control\\_t](#)

enum [adc\\_sample\\_state\\_reg\\_t](#)

enum [adc\\_group\\_a\\_t](#)

enum [adc\\_double\\_trigger\\_t](#)

## Data Structure Documentation

### ◆ [adc\\_sample\\_state\\_t](#)

struct adc_sample_state_t		
ADC sample state configuration		
Data Fields		
adc_sample_state_reg_t	reg_id	Sample state register ID.
uint8_t	num_states	Number of sampling states for conversion. Ch16-20/21 use the same value.

◆ **adc\_extended\_cfg\_t**

struct adc_extended_cfg_t		
Extended configuration structure for ADC.		
Data Fields		
adc_add_t	add_average_count	Add or average samples.
adc_clear_t	clearing	Clear after read.
adc_trigger_t	trigger_group_b	Group B trigger source; valid only for group mode.
adc_double_trigger_t	double_trigger_mode	Double-trigger mode setting.
adc_vref_control_t	adc_vref_control	VREFADC output voltage control.
uint8_t	enable_adbuf	Enable ADC Ring Buffer, Valid only to use along with DMAC transfer.

◆ **adc\_channel\_cfg\_t**

struct adc_channel_cfg_t		
ADC channel(s) configuration		
Data Fields		
uint32_t	scan_mask	Channels/bits: bit 0 is ch0; bit 15 is ch15.
uint32_t	scan_mask_group_b	Valid for group modes.
uint32_t	add_mask	Valid if add enabled in Open().
adc_group_a_t	priority_group_a	Valid for group modes.
uint8_t	sample_hold_mask	Channels/bits 0-2.
uint8_t	sample_hold_states	Number of states to be used for sample and hold. Affects channels 0-2.

◆ **adc\_instance\_ctrl\_t**

struct adc_instance_ctrl_t		

ADC instance control block. DO NOT INITIALIZE. Initialized in `adc_api_t::open()`.

## Enumeration Type Documentation

### ◆ `adc_mask_t`

enum `adc_mask_t`

For ADC Scan configuration `adc_channel_cfg_t::scan_mask`, `adc_channel_cfg_t::scan_mask_group_b`, `adc_channel_cfg_t::add_mask` and `adc_channel_cfg_t::sample_hold_mask`. Use bitwise OR to combine these masks for desired channels and sensors.

#### Enumerator

<code>ADC_MASK_OFF</code>	No channels selected.
<code>ADC_MASK_CHANNEL_0</code>	Channel 0 mask.
<code>ADC_MASK_CHANNEL_1</code>	Channel 1 mask.
<code>ADC_MASK_CHANNEL_2</code>	Channel 2 mask.
<code>ADC_MASK_CHANNEL_3</code>	Channel 3 mask.
<code>ADC_MASK_CHANNEL_4</code>	Channel 4 mask.
<code>ADC_MASK_CHANNEL_5</code>	Channel 5 mask.
<code>ADC_MASK_CHANNEL_6</code>	Channel 6 mask.
<code>ADC_MASK_CHANNEL_7</code>	Channel 7 mask.
<code>ADC_MASK_CHANNEL_8</code>	Channel 8 mask.
<code>ADC_MASK_CHANNEL_9</code>	Channel 9 mask.
<code>ADC_MASK_CHANNEL_10</code>	Channel 10 mask.
<code>ADC_MASK_CHANNEL_11</code>	Channel 11 mask.
<code>ADC_MASK_CHANNEL_12</code>	Channel 12 mask.
<code>ADC_MASK_CHANNEL_13</code>	Channel 13 mask.
<code>ADC_MASK_CHANNEL_14</code>	Channel 14 mask.
<code>ADC_MASK_CHANNEL_15</code>	Channel 15 mask.
<code>ADC_MASK_CHANNEL_16</code>	Channel 16 mask.

ADC_MASK_CHANNEL_17	Channel 17 mask.
ADC_MASK_CHANNEL_18	Channel 18 mask.
ADC_MASK_CHANNEL_19	Channel 19 mask.
ADC_MASK_CHANNEL_20	Channel 20 mask.
ADC_MASK_CHANNEL_21	Channel 21 mask.
ADC_MASK_CHANNEL_22	Channel 22 mask.
ADC_MASK_CHANNEL_23	Channel 23 mask.
ADC_MASK_CHANNEL_24	Channel 24 mask.
ADC_MASK_CHANNEL_25	Channel 25 mask.
ADC_MASK_CHANNEL_26	Channel 26 mask.
ADC_MASK_CHANNEL_27	Channel 27 mask.
ADC_MASK_TEMPERATURE	Temperature sensor channel mask.
ADC_MASK_VOLT	Voltage reference channel mask.
ADC_MASK_SENSORS	All sensor channel mask.

◆ **adc\_add\_t**

enum <a href="#">adc_add_t</a>	
ADC data sample addition and averaging options	
Enumerator	
ADC_ADD_OFF	Addition turned off for channels/sensors.
ADC_ADD_TWO	Add two samples.
ADC_ADD_THREE	Add three samples.
ADC_ADD_FOUR	Add four samples.
ADC_ADD_SIXTEEN	Add sixteen samples.
ADC_ADD_AVERAGE_TWO	Average two samples.
ADC_ADD_AVERAGE_FOUR	Average four samples.
ADC_ADD_AVERAGE_EIGHT	Average eight samples.
ADC_ADD_AVERAGE_SIXTEEN	Add sixteen samples.

◆ **adc\_clear\_t**

enum <a href="#">adc_clear_t</a>	
ADC clear after read definitions	
Enumerator	
ADC_CLEAR_AFTER_READ_OFF	Clear after read off.
ADC_CLEAR_AFTER_READ_ON	Clear after read on.

◆ **adc\_vref\_control\_t**

enum <code>adc_vref_control_t</code>	
Enumerator	
<code>ADC_VREF_CONTROL_VREFH</code>	VREFAMPcnt reset value. VREFADC Output voltage is Hi-Z.
<code>ADC_VREF_CONTROL_1_5V_OUTPUT</code>	BGR turn ON. VREFADC Output voltage is 1.5 V.
<code>ADC_VREF_CONTROL_2_0V_OUTPUT</code>	BGR turn ON. VREFADC Output voltage is 2.0 V.
<code>ADC_VREF_CONTROL_2_5V_OUTPUT</code>	BGR turn ON. VREFADC Output voltage is 2.5 V.
<code>ADC_VREF_CONTROL_AVCC0_AVSS0</code>	High potential is AVCC0, low potential is AVSS0.
<code>ADC_VREF_CONTROL_VREFH0_AVSS0</code>	High potential is VREFH0, low potential is AVSS0.
<code>ADC_VREF_CONTROL_IVREF_AVSS0</code>	High potential is internal reference voltage, low potential is AVSS0. When the high potential is set to the internal reference voltage, wait 5 us after <code>R_ADC_Open()</code> to start an ADC measurement.
<code>ADC_VREF_CONTROL_AVCC0_VREFLO</code>	High potential is AVCC0, low potential is VREFLO.
<code>ADC_VREF_CONTROL_VREFH0_VREFLO</code>	High potential is VREFH0, low potential is VREFLO.
<code>ADC_VREF_CONTROL_IVREF_VREFLO</code>	High potential is internal reference voltage, low potential is VREFLO. When the high potential is set to the internal reference voltage, wait 5 us after <code>R_ADC_Open()</code> to start an ADC measurement.

◆ **adc\_sample\_state\_reg\_t**

enum <code>adc_sample_state_reg_t</code>	
ADC sample state registers	
Enumerator	
<code>ADC_SAMPLE_STATE_CHANNEL_0</code>	Sample state register channel 0.
<code>ADC_SAMPLE_STATE_CHANNEL_1</code>	Sample state register channel 1.
<code>ADC_SAMPLE_STATE_CHANNEL_2</code>	Sample state register channel 2.
<code>ADC_SAMPLE_STATE_CHANNEL_3</code>	Sample state register channel 3.
<code>ADC_SAMPLE_STATE_CHANNEL_4</code>	Sample state register channel 4.
<code>ADC_SAMPLE_STATE_CHANNEL_5</code>	Sample state register channel 5.
<code>ADC_SAMPLE_STATE_CHANNEL_6</code>	Sample state register channel 6.
<code>ADC_SAMPLE_STATE_CHANNEL_7</code>	Sample state register channel 7.
<code>ADC_SAMPLE_STATE_CHANNEL_8</code>	Sample state register channel 8.
<code>ADC_SAMPLE_STATE_CHANNEL_9</code>	Sample state register channel 9.
<code>ADC_SAMPLE_STATE_CHANNEL_10</code>	Sample state register channel 10.
<code>ADC_SAMPLE_STATE_CHANNEL_11</code>	Sample state register channel 11.
<code>ADC_SAMPLE_STATE_CHANNEL_12</code>	Sample state register channel 12.
<code>ADC_SAMPLE_STATE_CHANNEL_13</code>	Sample state register channel 13.
<code>ADC_SAMPLE_STATE_CHANNEL_14</code>	Sample state register channel 14.
<code>ADC_SAMPLE_STATE_CHANNEL_15</code>	Sample state register channel 15.
<code>ADC_SAMPLE_STATE_CHANNEL_16_TO_31</code>	Sample state register channel 16 to 31.

◆ **adc\_group\_a\_t**

enum <a href="#">adc_group_a_t</a>	
ADC action for group A interrupts group B scan. This enumeration is used to specify the priority between Group A and B in group mode.	
Enumerator	
ADC_GROUP_A_PRIORITY_OFF	Group A ignored and does not interrupt ongoing group B scan.
ADC_GROUP_A_GROUP_B_WAIT_FOR_TRIGGER	Group A interrupts Group B(single scan) which restarts at next Group B trigger.
ADC_GROUP_A_GROUP_B_RESTART_SCAN	Group A interrupts Group B(single scan) which restarts immediately after Group A scan is complete.
ADC_GROUP_A_GROUP_B_CONTINUOUS_SCAN	Group A interrupts Group B(continuous scan) which continues scanning without a new Group B trigger.

◆ **adc\_double\_trigger\_t**

enum <a href="#">adc_double_trigger_t</a>	
ADC double-trigger mode definitions	
Enumerator	
ADC_DOUBLE_TRIGGER_DISABLED	Double-triggering disabled.
ADC_DOUBLE_TRIGGER_ENABLED	Double-triggering enabled.
ADC_DOUBLE_TRIGGER_ENABLED_EXTENDED	Double-triggering enabled on both ADC ELC events.

**Function Documentation**

◆ **R\_ADC\_Open()**

```
fsp_err_t R_ADC_Open ( adc_ctrl_t* p_ctrl, adc_cfg_t const *const p_cfg )
```

Sets the operational mode, trigger sources, interrupt priority, and configurations for the peripheral as a whole. If interrupt is enabled, the function registers a callback function pointer for notifying the user whenever a scan has completed.

**Return values**

FSP_SUCCESS	Module is ready for use.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_ALREADY_OPEN	The instance control structure has already been opened.
FSP_ERR_IRQ_BSP_DISABLED	A callback is provided, but the interrupt is not enabled.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The requested unit does not exist on this MCU.
FSP_ERR_INVALID_HW_CONDITION	The ADC clock must be at least 1 MHz

◆ **R\_ADC\_ScanCfg()**

```
fsp_err_t R_ADC_ScanCfg ( adc_ctrl_t* p_ctrl, void const *const p_channel_cfg )
```

Configures the ADC scan parameters. Channel specific settings are set in this function. Pass a pointer to `adc_channel_cfg_t` to `p_channel_cfg`.

**Note**

*This starts group B scans if `adc_channel_cfg_t::priority_group_a` is set to `ADC_GROUP_A_GROUP_B_CONTINUOUS_SCAN`.*

**Return values**

FSP_SUCCESS	Channel specific settings applied.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

## ◆ R\_ADC\_InfoGet()

```
fsp_err_t R_ADC_InfoGet ( adc_ctrl_t* p_ctrl, adc_info_t* p_adc_info )
```

Returns the address of the lowest number configured channel and the total number of bytes to be read in order to read the results of the configured channels and return the ELC Event name. If no channels are configured, then a length of 0 is returned.

Also provides the temperature sensor slope and the calibration data for the sensor if available on this MCU. Otherwise, invalid calibration data of 0xFFFFFFFF will be returned.

**Note**

*In group mode, information is returned for group A only. Calculating information for group B is not currently supported.*

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

## ◆ R\_ADC\_ScanStart()

```
fsp_err_t R_ADC_ScanStart ( adc_ctrl_t* p_ctrl)
```

Starts a software scan or enables the hardware trigger for a scan depending on how the triggers were configured in the R\_ADC\_Open call. If the unit was configured for ELC or external hardware triggering, then this function allows the trigger signal to get to the ADC unit. The function is not able to control the generation of the trigger itself. If the unit was configured for software triggering, then this function starts the software triggered scan.

**Precondition**

Call R\_ADC\_ScanCfg after R\_ADC\_Open before starting a scan.

On MCUs that support calibration, call R\_ADC\_Calibrate and wait for calibration to complete before starting a scan.

**Return values**

FSP_SUCCESS	Scan started (software trigger) or hardware triggers enabled.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.
FSP_ERR_IN_USE	Another scan is still in progress (software trigger).

◆ **R\_ADC\_ScanStop()**

```
fsp_err_t R_ADC_ScanStop ( adc_ctrl_t* p_ctrl)
```

Stops the software scan or disables the unit from being triggered by the hardware trigger (ELC or external) based on what type of trigger the unit was configured for in the R\_ADC\_Open function. Stopping a hardware triggered scan via this function does not abort an ongoing scan, but prevents the next scan from occurring. Stopping a software triggered scan aborts an ongoing scan.

**Return values**

FSP_SUCCESS	Scan stopped (software trigger) or hardware triggers disabled.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_StatusGet()**

```
fsp_err_t R_ADC_StatusGet ( adc_ctrl_t* p_ctrl, adc_status_t* p_status )
```

Provides the status of any scan process that was started, including scans started by ELC or external triggers and calibration scans on MCUs that support calibration.

**Return values**

FSP_SUCCESS	Module status stored in the provided pointer p_status
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Read()**

```
fsp_err_t R_ADC_Read ( adc_ctrl_t* p_ctrl, adc_channel_t const reg_id, uint16_t*const p_data )
```

Reads conversion results from a single channel or sensor.

**Return values**

FSP_SUCCESS	Data read into provided p_data.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Read32()**

```
fsp_err_t R_ADC_Read32 ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data )
```

Reads conversion results from a single channel or sensor register into a 32-bit result.

**Return values**

FSP_SUCCESS	Data read into provided p_data.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_SampleStateCountSet()**

```
fsp_err_t R_ADC_SampleStateCountSet ( adc_ctrl_t * p_ctrl, adc_sample_state_t * p_sample )
```

Sets the sample state count for individual channels. This only needs to be set for special use cases. Normally, use the default values out of reset.

*Note*

*The sample states for the temperature and voltage sensor are set in R\_ADC\_ScanCfg.*

**Return values**

FSP_SUCCESS	Sample state count updated.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_Close()**

```
fsp_err_t R_ADC_Close ( adc_ctrl_t * p_ctrl)
```

This function ends any scan in progress, disables interrupts, and removes power to the A/D peripheral.

**Return values**

FSP_SUCCESS	Module closed.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **R\_ADC\_OffsetSet()**

```
fsp_err_t R_ADC_OffsetSet ( adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t offset )
```

`adc_api_t::offsetSet` is not supported on the ADC.

**Return values**

FSP_ERR_UNSUPPORTED	Function not supported in this implementation.
---------------------	--

◆ **R\_ADC\_Calibrate()**

```
fsp_err_t R_ADC_Calibrate ( adc_ctrl_t *const p_ctrl, void *const p_extend )
```

Initiates calibration of the ADC on MCUs that require calibration. This function must be called before starting a scan on MCUs that require calibration.

Calibration is complete when the callback is called with `ADC_EVENT_CALIBRATION_COMPLETE` or when `R_ADC_StatusGet` returns `ADC_STATUS_IDLE`. Reference Figure 32.35 "Software flow and operation example of calibration operation." in the RA2A1 manual R01UH0888EJ0100.

ADC calibration time: 12 PCLKB + 774,930 ADCLK. (Reference Table 32.16 "Required calibration time (shown as the number of ADCLK and PCLKB cycles)" in the RA2A1 manual R01UH0888EJ0100. The lowest supported ADCLK is 1MHz.

Calibration will take a minimum of 24 milliseconds at 32 MHz PCLKB and ADCLK. This wait could take up to 780 milliseconds for a 1 MHz PCLKD (ADCLK).

**Parameters**

[in]	p_ctrl	Pointer to the instance control structure
[in]	p_extend	Unused argument. Pass NULL.

**Return values**

FSP_SUCCESS	Calibration successfully initiated.
FSP_ERR_INVALID_HW_CONDITION	A scan is in progress or hardware triggers are enabled.
FSP_ERR_UNSUPPORTED	Calibration not supported on this MCU.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

### ◆ R\_ADC\_CallbackSet()

```
fsp_err_t R_ADC_CallbackSet ( adc_ctrl_t *const p_api_ctrl, void(*) (adc_callback_args_t *)
p_callback, void const *const p_context, adc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `adc_api_t::callbackSet`

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.4 Asynchronous General Purpose Timer (r\_agt)

### Modules

#### Functions

```
fsp_err_t R_AGT_Close (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_PeriodSet (timer_ctrl_t *const p_ctrl, uint32_t const
period_counts)
```

```
fsp_err_t R_AGT_DutyCycleSet (timer_ctrl_t *const p_ctrl, uint32_t const
duty_cycle_counts, uint32_t const pin)
```

```
fsp_err_t R_AGT_Reset (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_Start (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_Enable (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_Disable (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_InfoGet (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
```

```
fsp_err_t R_AGT_StatusGet (timer_ctrl_t *const p_ctrl, timer_status_t *const
p_status)
```

```
fsp_err_t R_AGT_Stop (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_AGT_Open (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_AGT_CallbackSet (timer_ctrl_t *const p_api_ctrl,
void(*p_callback)(timer_callback_args_t *), void const *const
p_context, timer_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the AGT peripheral on RA MCUs. This module implements the [Timer Interface](#).

## Overview

### Features

The AGT module has the following features:

- Supports periodic mode, one-shot mode, and PWM mode.
- Signal can be output to a pin.
- Configurable period (counts per timer cycle).
- Configurable duty cycle in PWM mode.
- Configurable clock source, including PCLKB, LOCO, SUBCLK, and external sources input to AGTIO.
- Supports runtime reconfiguration of period.
- Supports runtime reconfiguration of duty cycle in PWM mode.
- Supports counting based on an external clock input to AGTIO.
- Supports debounce filter on AGTIO pins.
- Supports measuring pulse width or pulse period.
- APIs are provided to start, stop, and reset the counter.
- APIs are provided to get the current period, source clock frequency, and count direction.
- APIs are provided to get the current timer status and counter value.

### Selecting a Timer

RA MCUs have two timer peripherals: the General PWM Timer (GPT) and the Asynchronous General Purpose Timer (AGT). When selecting between them, consider these factors:

	GPT	AGT
Low Power Modes	The GPT can operate in sleep mode.	The AGT can operate in all low power modes (when count source is LOCO or subclock).
Available Channels	The number of GPT channels is device specific. All currently supported MCUs have at least 7 GPT channels.	All MCUs have 2 AGT channels.
Timer Resolution	All MCUs have at least one 32-bit GPT timer.	The AGT timers are 16-bit timers.

Clock Source	The GPT runs off PCLKD with a configurable divider up to 1024. It can also be configured to count ELC events or external pulses.	The AGT runs off PCLKB, LOCO, or subclock with a configurable divider up to 8 for PCLKB or up to 128 for LOCO or subclock.
--------------	--	--

## Configuration

### Build Time Configurations for r\_agt

The following build time configurations are defined in fsp\_cfg/r\_agt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Pin Output Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> </ul>	Disabled	If selected code for outputting a waveform to a pin is included in the build.
Pin Input Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> </ul>	Disabled	Enable input support to use pulse width measurement mode, pulse period measurement mode, or input from P402, P402, or AGTIO.

### Configurations for Driver > Timers > Timer Driver on r\_agt

This module can be added to the Stacks tab via New Stack > Driver > Timers > Timer Driver on r\_agt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_timer0	Module name.
General > Channel	Channel number does not exist	0	Physical hardware channel.
General > Mode	<ul style="list-style-type: none"> <li>Periodic</li> <li>One-Shot</li> <li>PWM</li> </ul>	Periodic	Mode selection. Note: One-shot mode is implemented in software. ISR's must be enabled for one shot even if callback is unused.
General > Period	Value must be non-negative	0x10000	Specify the timer period based on the

selected unit.

When the unit is set to 'Raw Counts', setting the period to 0x10000 results in the maximum period at the lowest divisor (fastest timer tick). Set the period to 0x10000 for a free running timer, pulse width measurement or pulse period measurement. Setting the period higher will automatically select a higher divider; the period can be set up to 0x80000 when counting from PCLKB or 0x800000 when counting from LOCO/subclock, which will use a divider of 8 or 128 respectively with the maximum period.

If the requested period cannot be achieved, the settings with the largest possible period that is less than or equal to the requested period are used. The theoretical calculated period is printed in a comment in the [timer\\_cfg\\_t](#) structure.

General > Period Unit

- Raw Counts
- Nanoseconds
- Microseconds
- Milliseconds
- Seconds
- Hertz
- Kilohertz

Raw Counts

Unit of the period specified above

General > Count Source

- PCLKB
- LOCO
- SUBCLOCK
- AGT Underflow
- P402 Input
- P403 Input
- AGTIO Input

PCLKB

AGT counter clock source. NOTE: The divisor is calculated automatically based on the selected period. See [agt\\_count\\_source\\_t](#) documentation for details.

Output > Duty Cycle Percent (only applicable in PWM mode)	Value must be between 0 and 100	50	Specify the timer duty cycle percent. Only used in PWM mode.
Output > AGTOA Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTOA output.
Output > AGTOB Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTOB output.
Output > AGTO Output	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Start Level Low</li> <li>• Start Level High</li> </ul>	Disabled	Configure AGTO output.
Input > Measurement Mode	<ul style="list-style-type: none"> <li>• Measure Disabled</li> <li>• Measure Low Level Pulse Width</li> <li>• Measure High Level Pulse Width</li> <li>• Measure Pulse Period</li> </ul>	Measure Disabled	Select if the AGT should be used to measure pulse width or pulse period. In high level pulse width measurement mode, the AGT counts when AGTIO is high and starts counting immediately in the middle of a pulse if AGTIO is high when <a href="#">R_AGT_Start()</a> is called. In low level pulse width measurement mode, the AGT counts when AGTIO is low and could start counting in the middle of a pulse if AGTIO is low when <a href="#">R_AGT_Start()</a> is called.
Input > Input Filter	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter sampled at PCLKB</li> <li>• Filter sampled at PCLKB / 8</li> <li>• Filter sampled at PCLKB / 32</li> </ul>	No Filter	Input filter, applies AGTIO in pulse period measurement, pulse width measurement, or event counter mode. The filter requires the signal to be at the same level for 3 successive reads at the specified filter frequency.
Input > Enable Pin	<ul style="list-style-type: none"> <li>• Enable Pin Not Used</li> <li>• Enable Pin Active Low</li> <li>• Enable Pin Active High</li> </ul>	Enable Pin Not Used	Select active edge for the AGTEE pin if used. Only applies if the count source is P402, P403 or AGTIO.

Input > Trigger Edge	<ul style="list-style-type: none"> <li>• Trigger Edge Rising</li> <li>• Trigger Edge Falling</li> <li>• Trigger Edge Both</li> </ul>	Trigger Edge Rising	Select the trigger edge. Applies if measurement mode is pulse period, or if the count source is P402, P403, or AGTIO. Do not select Trigger Edge Both with pulse period measurement.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the timer period elapses.
Interrupts > Underflow Interrupt Priority	MCU Specific Options		Timer interrupt priority.

## Clock Configuration

The AGT clock is based on the PCLKB, LOCO, or Subclock frequency. You can set the clock frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

This module can use the AGTOA and AGTOB pins as output pins for periodic, one-shot, or PWM signals.

For input capture, the input signal must be applied to the AGTIO pin.

For event counting, the AGTEEn enable pin is optional.

## Timer Period

The RA Configuration editor will automatically calculate the period count value and source clock divider based on the selected period time, units, and clock speed.

When the selected unit is "Raw counts", the maximum allowed period setting varies depending on the selected clock source:

Clock source	Maximum period (counts)
LOCO/Subclock	0x800000
PCLKB	0x80000
All other sources	0x10000

### Note

*Though the AGT is a 16-bit timer, because the period interrupt occurs when the counter underflows, setting the period register to 0 results in an effective period of 1 count. For this reason all user-provided raw count values reflect the actual number of period counts (not the raw register values).*

## Usage Notes

### Starting and Stopping the AGT

After starting or stopping the timer, AGT registers cannot be accessed until the AGT state is updated after 3 AGTCLK cycles. If another AGT function is called before the 3 AGTCLK period elapses, the function spins waiting for the AGT state to update. The required wait time after starting or stopping the timer can be determined using the frequency of AGTCLK, which is derived from [timer\\_cfg\\_t::source\\_div](#) and [agt\\_extended\\_cfg\\_t::count\\_source](#).

The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

#### Warning

The subclock can take seconds to stabilize. The RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation.

### Low Power Modes

The AGT1 (channel 1 only) can be used to enter snooze mode or to wake the MCU from snooze, software standby, or deep software standby modes when a counter underflow occurs. The compare match A and B events can also be used to wake from software standby or snooze modes.

### One-Shot Mode

The AGT timer does not support one-shot mode natively. One-shot mode is achieved by stopping the timer in the interrupt service routine before the callback is called. If the interrupt is not serviced before the timer period expires again, the timer generates more than one event. The callback is only called once in this case, but multiple events may be generated if the timer is linked to the [Data Transfer Controller \(r\\_dtc\)](#).

### One-Shot Mode Output

The output waveform in one-shot mode is one AGT clock cycle less than the configured period. The configured period must be at least 2 counts to generate an output pulse.

Examples of one-shot signals that can be generated by this module are shown below:

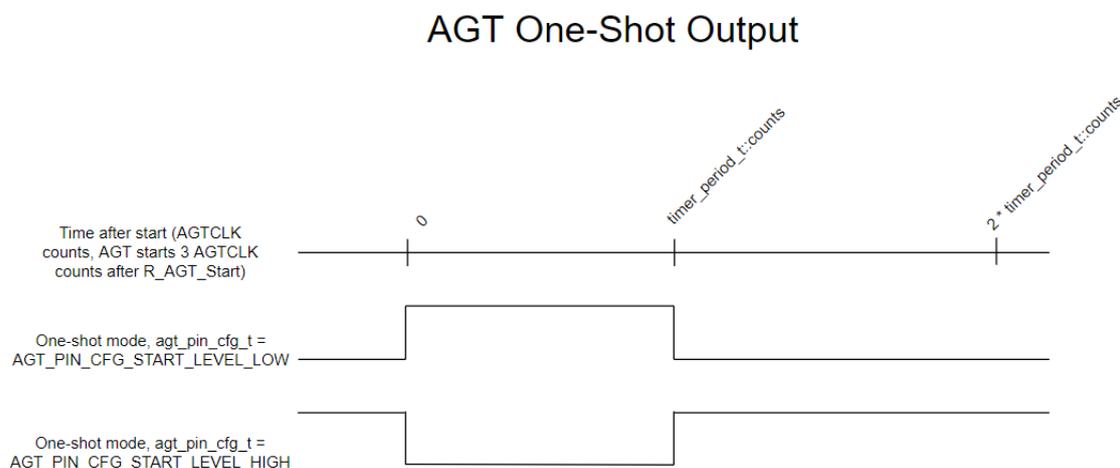


Figure 142: AGT One-Shot Output

### Periodic Output

The AGTOA or AGTOB pin toggles twice each time the timer expires in periodic mode. This is achieved by defining a PWM wave at a 50 percent duty cycle so that the period of the resulting square (from rising edge to rising edge) matches the period of the AGT timer. Since the periodic output is actually a PWM output, the time at the stop level is one cycle shorter than the time opposite the stop level for odd period values.

Examples of periodic signals that can be generated by this module are shown below:

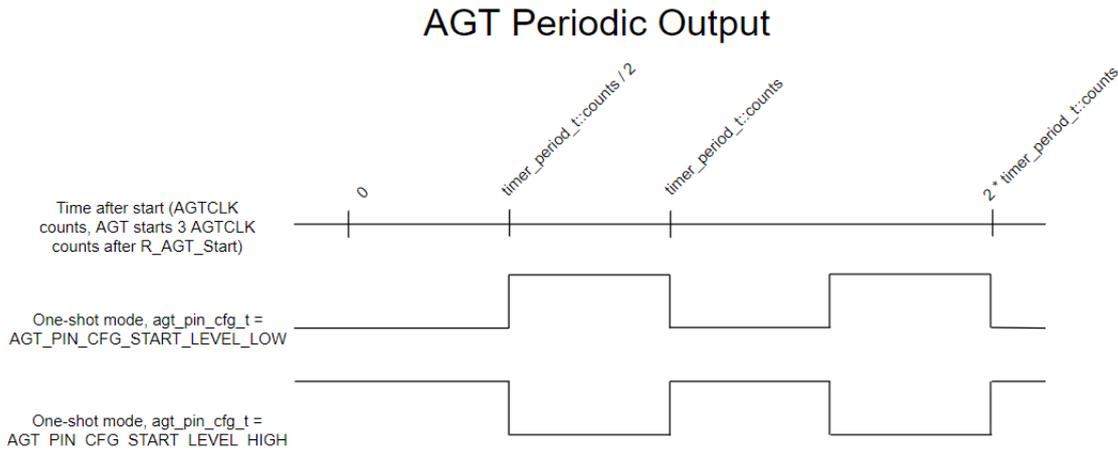


Figure 143: AGT Periodic Output

### PWM Output

This module does not support in phase PWM output. The PWM output signal is low at the beginning of the cycle and high at the end of the cycle.

Examples of PWM signals that can be generated by this module are shown below:

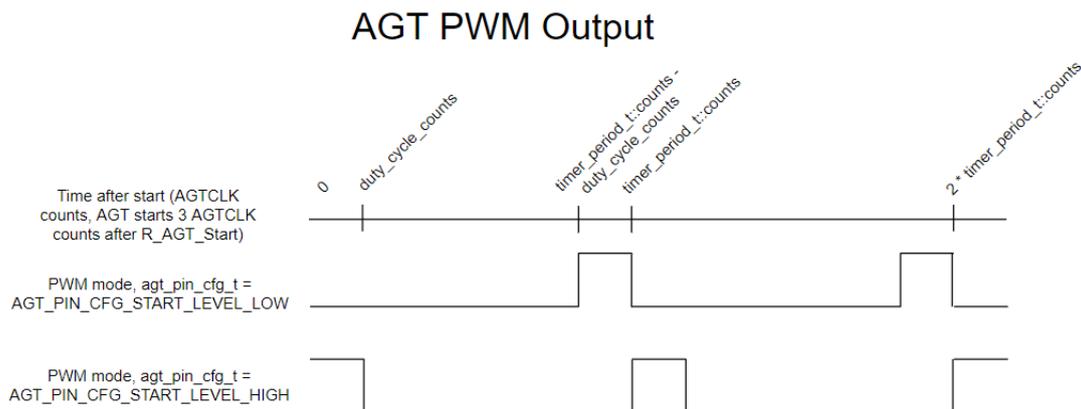


Figure 144: AGT PWM Output

### Triggering ELC Events with AGT

The AGT timer can trigger the start of other peripherals. The [Event Link Controller \(r\\_elc\)](#) guide provides a list of all available peripherals.

## Examples

### AGT Basic Example

This is a basic example of minimal use of the AGT in an application.

```
void agt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);
}
```

### AGT Callback Example

This is an example of a timer callback.

```
/* Example callback called when timer expires. */
void timer_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CYCLE_END == p_args->event)
    {
        /* Add application code to be called periodically here. */
    }
}
```

### AGT Free Running Counter Example

To use the AGT as a free running counter, select periodic mode and set the the Period to 0xFFFF.

```
void agt_counter_example (void)
```

```
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);
    /* (Optional) Stop the timer. */
    (void) R_AGT_Stop(&g_timer0_ctrl);
    /* Read the current counter value. Counter value is in status.counter. */
    timer_status_t status;
    (void) R_AGT_StatusGet(&g_timer0_ctrl, &status);
}
```

### AGT Input Capture Example

This is an example of using the AGT to capture pulse width or pulse period measurements.

```
/* Example callback called when a capture occurs. */
uint64_t g_captured_time = 0U;
uint32_t g_capture_overflows = 0U;
void timer_capture_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CAPTURE_A == p_args->event)
    {
        /* (Optional) Get the current period if not known. */
        timer_info_t info;
        (void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
        uint32_t period = info.period_counts;
        /* Process capture from AGTIO. */
        g_captured_time = ((uint64_t) period * g_capture_overflows) +
p_args->capture;
        g_capture_overflows = 0U;
    }
}
```

```
if (TIMER_EVENT_CYCLE_END == p_args->event)
{
    /* An overflow occurred during capture. This must be accounted for at the
application layer. */
    g_capture_overflows++;
}
}
void agt_capture_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable captures. Captured values arrive in the interrupt. */
    (void) R_AGT_Enable(&g_timer0_ctrl);
    /* (Optional) Disable captures. */
    (void) R_AGT_Disable(&g_timer0_ctrl);
}
```

## AGT Period Update Example

This an example of updating the period.

```
#define AGT_EXAMPLE_MSEC_PER_SEC (1000)
#define AGT_EXAMPLE_DESIRED_PERIOD_MSEC (20)
/* This example shows how to calculate a new period value at runtime. */
void agt_period_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
```

```

(void) R_AGT_Start(&g_timer0_ctrl);

/* Get the source clock frequency (in Hz). There are several ways to do this in FSP:
 * - If LOCO or subclock is chosen in agt_extended_cfg_t::clock_source
 * - The source clock frequency is BSP_LOCO_HZ >> timer_cfg_t::source_div
 * - If PCLKB is chosen in agt_extended_cfg_t::clock_source and the PCLKB frequency
has not changed since reset,
 * - The source clock frequency is BSP_STARTUP_PCLKB_HZ >> timer_cfg_t::source_div
 * - Use the R_AGT_InfoGet function (it accounts for the clock source and divider).
 * - Calculate the current PCLKB frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) and right shift
 * by timer_cfg_t::source_div.
 *
 * This example uses the last option (R_FSP_SystemClockHzGet).
 */
uint32_t timer_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) >>
g_timer0_cfg.source_div;

/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclk_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) timer_freq_hz * AGT_EXAMPLE_DESIRED_PERIOD_MSEC) /
AGT_EXAMPLE_MSEC_PER_SEC);

/* Set the calculated period. This will return an error if parameter checking is
enabled and the calculated
 * period is larger than UINT16_MAX. */
err = R_AGT_PeriodSet(&g_timer0_ctrl, period_counts);
assert(FSP_SUCCESS == err);
}

```

## AGT Duty Cycle Update Example

This an example of updating the duty cycle.

```
#define AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT (25)
```

```
#define AGT_EXAMPLE_MAX_PERCENT (100)

/* This example shows how to calculate a new duty cycle value at runtime. */
void agt_duty_cycle_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Start the timer. */
    (void) R_AGT_Start(&g_timer0_ctrl);

    /* Get the current period setting. */
    timer_info_t info;
    (void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
    uint32_t current_period_counts = info.period_counts;

    /* Calculate the desired duty cycle based on the current period. */
    uint32_t duty_cycle_counts = (current_period_counts *
AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
                                AGT_EXAMPLE_MAX_PERCENT;

    /* Set the calculated duty cycle. */
    err = R_AGT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, AGT_OUTPUT_PIN_AGTOA
);
    assert(FSP_SUCCESS == err);
}
```

### AGT Cascaded Timers Example

This an example of using underflow from an even AGT channel as the count source for the next channel (in this case, AGT0 and AGT1).

```
/* This example shows how use cascaded timers. The count source for AGT channel 1 is
set to AGT0 underflow. */
void agt_cascaded_timers_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
```

```

/* Initialize the timers in any order. */
err = R_AGT_Open(&g_timer_channel0_ctrl, &g_timer_channel0_cfg);
assert(FSP_SUCCESS == err);

err = R_AGT_Open(&g_timer_channel1_ctrl, &g_timer_channel1_cfg);
assert(FSP_SUCCESS == err);

/* Start AGT channel 1 first. */
(void) R_AGT_Start(&g_timer_channel1_ctrl);
(void) R_AGT_Start(&g_timer_channel0_ctrl);

/* (Optional) Stop AGT channel 0 first. */
(void) R_AGT_Stop(&g_timer_channel0_ctrl);
(void) R_AGT_Stop(&g_timer_channel1_ctrl);

/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;
(void) R_AGT_StatusGet(&g_timer_channel1_ctrl, &status);
}

```

## Data Structures

struct [agt\\_instance\\_ctrl\\_t](#)

struct [agt\\_extended\\_cfg\\_t](#)

## Enumerations

enum [agt\\_clock\\_t](#)

enum [agt\\_measure\\_t](#)

enum [agt\\_agtio\\_filter\\_t](#)

enum [agt\\_enable\\_pin\\_t](#)

enum [agt\\_trigger\\_edge\\_t](#)

enum [agt\\_output\\_pin\\_t](#)

enum [agt\\_pin\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ agt\_instance\_ctrl\_t

struct [agt\\_instance\\_ctrl\\_t](#)

Channel control block. DO NOT INITIALIZE. Initialization occurs when `timer_api_t::open` is called.

### ◆ agt\_extended\_cfg\_t

```
struct agt_extended_cfg_t
```

Optional AGT extension data structure.

#### Data Fields

<code>agt_clock_t</code>	<code>count_source</code>	AGT channel clock source. Valid values are: AGT_CLOCK_PCLKB, AGT_CLOCK_LOCO, AGT_CLOCK_FSUB.
<code>union agt_extended_cfg_t</code>	<code>__unnamed__</code>	
<code>agt_pin_cfg_t</code>	<code>agto: 3</code>	Configure AGTO pin.  <i>Note</i> <i>AGTIO polarity is opposite AGTO</i>
<code>agt_measure_t</code>	<code>measurement_mode</code>	Measurement mode.
<code>agt_agtio_filter_t</code>	<code>agtio_filter</code>	Input filter for AGTIO.
<code>agt_enable_pin_t</code>	<code>enable_pin</code>	Enable pin (event counting only)
<code>agt_trigger_edge_t</code>	<code>trigger_edge</code>	Trigger edge to start pulse period measurement or count external event.

## Enumeration Type Documentation

## ◆ agt\_clock\_t

enum agt_clock_t	
Count source	
Enumerator	
AGT_CLOCK_PCLKB	PCLKB count source, division by 1, 2, or 8 allowed.
AGT_CLOCK_LOCO	LOCO count source, division by 1, 2, 4, 8, 16, 32, 64, or 128 allowed.
AGT_CLOCK_AGT_UNDERFLOW	Underflow event signal from next lowest AGT channel, division must be 1.
AGT_CLOCK_SUBCLOCK	Subclock count source, division by 1, 2, 4, 8, 16, 32, 64, or 128 allowed.
AGT_CLOCK_P402	Counts events on P402, events are counted in deep software standby mode.
AGT_CLOCK_P403	Counts events on P403, events are counted in deep software standby mode.
AGT_CLOCK_AGTIO	Counts events on AGTIO, events are not counted in software standby modes.

## ◆ agt\_measure\_t

enum agt_measure_t	
Enable pin for event counting mode.	
Enumerator	
AGT_MEASURE_DISABLED	AGT used as a counter.
AGT_MEASURE_PULSE_WIDTH_LOW_LEVEL	AGT used to measure low level pulse width.
AGT_MEASURE_PULSE_WIDTH_HIGH_LEVEL	AGT used to measure high level pulse width.
AGT_MEASURE_PULSE_PERIOD	AGT used to measure pulse period.

◆ **agt\_agtio\_filter\_t**

enum agt_agtio_filter_t	
Input filter, applies AGTIO in pulse period measurement, pulse width measurement, or event counter mode. The filter requires the signal to be at the same level for 3 successive reads at the specified filter frequency.	
Enumerator	
AGT_AGTIO_FILTER_NONE	No filter.
AGT_AGTIO_FILTER_PCLKB	Filter at PCLKB.
AGT_AGTIO_FILTER_PCLKB_DIV_8	Filter at PCLKB / 8.
AGT_AGTIO_FILTER_PCLKB_DIV_32	Filter at PCLKB / 32.

◆ **agt\_enable\_pin\_t**

enum agt_enable_pin_t	
Enable pin for event counting mode.	
Enumerator	
AGT_ENABLE_PIN_NOT_USED	AGTEE/AGTWEE is not used.
AGT_ENABLE_PIN_ACTIVE_LOW	Events are only counted when AGTEE/AGTWEE is low.
AGT_ENABLE_PIN_ACTIVE_HIGH	Events are only counted when AGTEE/AGTWEE is high.

◆ **agt\_trigger\_edge\_t**

enum agt_trigger_edge_t	
Trigger edge for pulse period measurement mode and event counting mode.	
Enumerator	
AGT_TRIGGER_EDGE_RISING	Measurement starts or events are counted on rising edge.
AGT_TRIGGER_EDGE_FALLING	Measurement starts or events are counted on falling edge.
AGT_TRIGGER_EDGE_BOTH	Events are counted on both edges (n/a for pulse period mode)

◆ **agt\_output\_pin\_t**

enum agt_output_pin_t	
Output pins, used to select which duty cycle to update in <code>R_AGT_DutyCycleSet()</code> .	
Enumerator	
AGT_OUTPUT_PIN_AGTOA	AGTOA.
AGT_OUTPUT_PIN_AGTOB	AGTOB.

◆ **agt\_pin\_cfg\_t**

enum agt_pin_cfg_t	
Level of AGT pin	
Enumerator	
AGT_PIN_CFG_DISABLED	Not used as output pin.
AGT_PIN_CFG_START_LEVEL_LOW	Pin level low.
AGT_PIN_CFG_START_LEVEL_HIGH	Pin level high.

**Function Documentation**

◆ **R\_AGT\_Close()**

```
fsp_err_t R_AGT_Close ( timer_ctrl_t *const p_ctrl)
```

Stops counter, disables interrupts, disables output pins, and clears internal driver data. Implements `timer_api_t::close`.

**Return values**

FSP_SUCCESS	Timer closed.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_PeriodSet()**

```
fsp_err_t R_AGT_PeriodSet ( timer_ctrl_t *const p_ctrl, uint32_t const period_counts )
```

Updates period. The new period is updated immediately and the counter is reset to the maximum value. Implements `timer_api_t::periodSet`.

**Warning**

If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and an AGT underflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter underflow after processing completes.

Stop the timer before calling this function if one-shot output is used.

**Example:**

```
/* Get the source clock frequency (in Hz). There are several ways to do this in FSP:
 * - If LOCO or subclock is chosen in agt_extended_cfg_t::clock_source
 * - The source clock frequency is BSP_LOCO_HZ >> timer_cfg_t::source_div
 * - If PCLKB is chosen in agt_extended_cfg_t::clock_source and the PCLKB frequency
has not changed since reset,
 * - The source clock frequency is BSP_STARTUP_PCLKB_HZ >> timer_cfg_t::source_div
 * - Use the R_AGT_InfoGet function (it accounts for the clock source and divider).
 * - Calculate the current PCLKB frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) and right shift
 * by timer_cfg_t::source_div.
 *
 * This example uses the last option (R_FSP_SystemClockHzGet).
 */
uint32_t timer_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKB) >>
```

```
g_timer0_cfg.source_div;

/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
 * desired period is larger than UINT32_MAX / pclk_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) timer_freq_hz * AGT_EXAMPLE_DESIRED_PERIOD_MSEC) /
AGT_EXAMPLE_MSEC_PER_SEC);

/* Set the calculated period. This will return an error if parameter checking is
enabled and the calculated
 * period is larger than UINT16_MAX. */
err = R_AGT_PeriodSet(&g_timer0_ctrl, period_counts);
assert(FSP_SUCCESS == err);
```

### Return values

FSP_SUCCESS	Period value updated.
FSP_ERR_ASSERTION	A required pointer was NULL, or the period was not in the valid range of 1 to 0xFFFF.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

### ◆ R\_AGT\_DutyCycleSet()

```
fsp_err_t R_AGT_DutyCycleSet ( timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts,
uint32_t const pin )
```

Updates duty cycle. If the timer is counting, the new duty cycle is reflected after the next counter underflow. Implements [timer\\_api\\_t::dutyCycleSet](#).

Example:

```
/* Get the current period setting. */
timer_info_t info;
(void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
uint32_t current_period_counts = info.period_counts;
/* Calculate the desired duty cycle based on the current period. */
uint32_t duty_cycle_counts = (current_period_counts *
AGT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
AGT_EXAMPLE_MAX_PERCENT;
/* Set the calculated duty cycle. */
err = R_AGT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, AGT_OUTPUT_PIN_AGTOA);
assert(FSP_SUCCESS == err);
```

#### Return values

FSP_SUCCESS	Duty cycle updated.
FSP_ERR_ASSERTION	A required pointer was NULL, or the pin was not AGT_AGTO_AGTOA or AGT_AGTO_AGTOB.
FSP_ERR_INVALID_ARGUMENT	Duty cycle was not in the valid range of 0 to period (counts) - 1
FSP_ERR_NOT_OPEN	The instance control structure is not opened.
FSP_ERR_UNSUPPORTED	AGT_CFG_OUTPUT_SUPPORT_ENABLE is 0.

◆ **R\_AGT\_Reset()**

```
fsp_err_t R_AGT_Reset ( timer_ctrl_t *const p_ctrl)
```

Resets the counter value to the period minus one. Implements `timer_api_t::reset`.

**Return values**

FSP_SUCCESS	Counter reset.
FSP_ERR_ASSERTION	p_ctrl is NULL
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_Start()**

```
fsp_err_t R_AGT_Start ( timer_ctrl_t *const p_ctrl)
```

Starts timer. Implements `timer_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_AGT_Start(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer started.
FSP_ERR_ASSERTION	p_ctrl is null.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_Enable()**

```
fsp_err_t R_AGT_Enable ( timer_ctrl_t *const p_ctrl)
```

Enables external event triggers that start, stop, clear, or capture the counter. Implements `timer_api_t::enable`.

Example:

```
/* Enable captures. Captured values arrive in the interrupt. */
(void) R_AGT_Enable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_AGT\_Disable()**

```
fsp_err_t R_AGT_Disable ( timer_ctrl_t *const p_ctrl)
```

Disables external event triggers that start, stop, clear, or capture the counter. Implements `timer_api_t::disable`.

Example:

```
/* (Optional) Disable captures. */
(void) R_AGT_Disable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_AGT\_InfoGet()**

```
fsp_err_t R_AGT_InfoGet ( timer_ctrl_t *const p_ctrl, timer_info_t *const p_info )
```

Gets timer information and store it in provided pointer p\_info. Implements `timer_api_t::infoGet`.

Example:

```
/* (Optional) Get the current period if not known. */
timer_info_t info;
(void) R_AGT_InfoGet(&g_timer0_ctrl, &info);
uint32_t period = info.period_counts;
```

**Return values**

FSP_SUCCESS	Period, count direction, and frequency stored in p_info.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_StatusGet()**

```
fsp_err_t R_AGT_StatusGet ( timer_ctrl_t *const p_ctrl, timer_status_t *const p_status )
```

Retrieves the current state and counter value stores them in p\_status. Implements `timer_api_t::statusGet`.

Example:

```
/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;
(void) R_AGT_StatusGet(&g_timer0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current status and counter value provided in p_status.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

**◆ R\_AGT\_Stop()**

```
fsp_err_t R_AGT_Stop ( timer_ctrl_t *const p_ctrl)
```

Stops the timer. Implements `timer_api_t::stop`.

Example:

```
/* (Optional) Stop the timer. */  
(void) R_AGT_Stop(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance control structure is not opened.

◆ **R\_AGT\_Open()**

```
fsp_err_t R_AGT_Open ( timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg )
```

Initializes the AGT module instance. Implements `timer_api_t::open`.

The AGT hardware does not support one-shot functionality natively. The one-shot feature is therefore implemented in the AGT HAL layer. For a timer configured as a one-shot timer, the timer is stopped upon the first timer expiration.

The AGT implementation of the general timer can accept an optional `agt_extended_cfg_t` extension parameter. For AGT, the extension specifies the clock to be used as timer source and the output pin configurations. If the extension parameter is not specified (NULL), the default clock PCLKB is used and the output pins are disabled.

Example:

```
/* Initializes the module. */
err = R_AGT_Open(&g_timer0_ctrl, &g_timer0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	A required input pointer is NULL or the period is not in the valid range of 1 to 0xFFFF.
FSP_ERR_ALREADY_OPEN	R_AGT_Open has already been called for this p_ctrl.
FSP_ERR_IRQ_BSP_DISABLED	A required interrupt has not been enabled in the vector table.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel number is not available on AGT.

### ◆ R\_AGT\_CallbackSet()

```
fsp_err_t R_AGT_CallbackSet ( timer_ctrl_t *const p_api_ctrl, void(*) (timer_callback_args_t *)
p_callback, void const *const p_context, timer_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `timer_api_t::callbackSet`.

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.5 Bluetooth Low Energy Library (r\_ble)

### Modules

#### Functions

`ble_status_t` [R\\_BLE\\_Open](#) (void)  
Open the BLE protocol stack. [More...](#)

`ble_status_t` [R\\_BLE\\_Close](#) (void)  
Close the BLE protocol stack. [More...](#)

`ble_status_t` [R\\_BLE\\_Execute](#) (void)  
Execute the BLE task. [More...](#)

`uint32_t` [R\\_BLE\\_IsTaskFree](#) (void)  
Check the BLE task queue is free or not. [More...](#)

`ble_status_t` [R\\_BLE\\_SetEvent](#) (`ble_event_cb_t` cb)  
Set event. [More...](#)

uint32\_t [R\\_BLE\\_GetVersion](#) (void)

Get the BLE FIT module version. [More...](#)

uint32\_t [R\\_BLE\\_GetLibType](#) (void)

Get the type of BLE protocol stack library. [More...](#)

## Detailed Description

Driver for the Radio peripheral on RA MCUs. This module implements the [BLE Interface](#).

## Overview

The bluetooth low energy library (r\_ble) provides an API to control the Radio peripheral. This module is configured via the [QE for BLE](#). QE for BLE provides standard services defined by standardization organization and custom services defined by user. [Bluetooth LE Profile API Document User's Manual](#) describes the APIs for standard services.

## Features

- Common
  - Open/Close the BLE protocol stack.
  - Execute the BLE job.
  - Add an event in the BLE protocol stack internal queue.
- [GAP](#)
  - Initialization of the Host stack.
  - Start/Stop Advertising.
  - Start/Stop Scan.
  - Connect/Disconnect a link.
  - Initiate/Respond a pairing request.
- [GATT Common](#)
  - Get MTU size.
- [GATT Server](#)
  - Initialization of GATT Server.
  - Notification/Indication.
- [GATT Client](#)
  - Discovery services, characteristics.
  - Read/Write characteristic.
- [L2CAP](#)
  - Credit-based flow control transaction.
- [Vendor Specific](#)
  - DTM.
  - Set/Get transmit power.
  - Set/Get BD\_ADDR.

## Target Devices

The Renesas Bluetooth Low Energy Library supports the following devices.

- RA4W1

## Configuration

### Clock Configuration

#### Note

System clock (ICLK): 8 MHz or more

Peripheral module clock A (PCLKA): 8MHz or more

The BLE Protocol Stack is optimized for ICLK and PCLKA frequencies of 32 MHz.

It is recommended that the clock be set so that the ICLK and PCLKA frequencies are 32MHz in order to get the best performance from the BLE.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

Figure shows the software structure of the BLE FSP module.

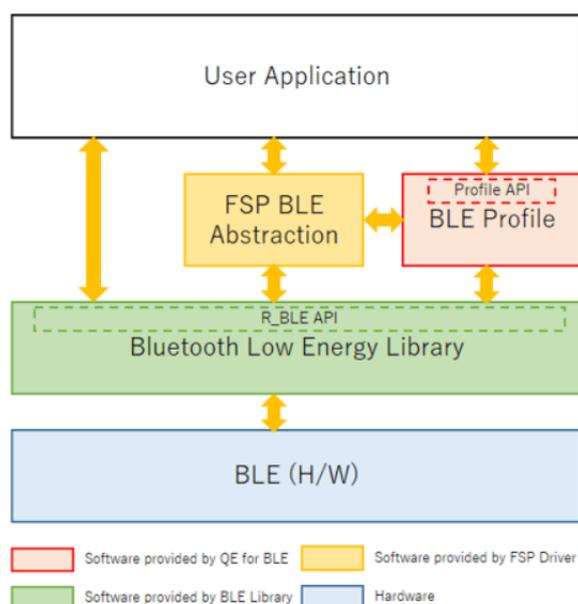


Figure 145: BLE software structure

The BLE FSP module consists of the BLE library.

The BLE Application uses the BLE functions via the [R\\_BLE API](#) provided by the BLE Library.

The QE for BLE generates the source codes (BLE base skeleton program) as a base for the BLE Application and the BLE Profile codes including the Profile API.

### Limitations

Developers should be aware of the following limitations when using the ble:

### Modules

GAP

GATT\_COMMON

GATT\_SERVER

GATT\_CLIENT

L2CAP

VS

## Typedefs

```
typedef void(* ble_event_cb_t) (void)
```

ble\_event\_cb\_t is the callback function type for [R\\_BLE\\_SetEvent\(\)](#).  
[More...](#)

## Typedef Documentation

### ◆ ble\_event\_cb\_t

ble\_event\_cb\_t

ble\_event\_cb\_t is the callback function type for [R\\_BLE\\_SetEvent\(\)](#).

#### Parameters

[in]

void

#### Returns

none

## Function Documentation

### ◆ R\_BLE\_Open()

ble\_status\_t R\_BLE\_Open ( void )

Open the BLE protocol stack.

This function should be called once before using the BLE protocol stack.

#### Return values

BLE\_SUCCESS(0x0000)

Success

◆ **R\_BLE\_Close()**

ble\_status\_t R\_BLE\_Close ( void )

Close the BLE protocol stack.

This function should be called once to close the BLE protocol stack.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

◆ **R\_BLE\_Execute()**

ble\_status\_t R\_BLE\_Execute ( void )

Execute the BLE task.

This handles all the task queued in the BLE protocol stack internal task queue and return. This function should be called repeatedly in the main loop.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

◆ **R\_BLE\_IsTaskFree()**

uint32\_t R\_BLE\_IsTaskFree ( void )

Check the BLE task queue is free or not.

This function returns the BLE task queue free status. When this function returns 0x0, call [R\\_BLE\\_Execute\(\)](#) to execute the BLE task.**Return values**

0x0	BLE task queue is not free
0x1	BLE task queue is free

◆ **R\_BLE\_SetEvent()**

```
ble_status_t R_BLE_SetEvent ( ble_event_cb_t cb)
```

Set event.

This function add an event in the BLE protocol stack internal queue. The event is handled in R\_BLE\_Execute just like Bluetooth event. This function is intended to be called in hardware interrupt context. Even if calling this function with the same cb before the cb is invoked, only one event is registered. The maximum number of the events can be registered at a time is eight.

**Parameters**

cb	The callback for the event.
----	-----------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_ALREADY_IN_PROGRESS(0x000A)	The event already registered with the callback.
BLE_ERR_CONTEXT_FULL(0x000B)	No free slot for the event.

◆ **R\_BLE\_GetVersion()**

```
uint32_t R_BLE_GetVersion ( void )
```

Get the BLE FIT module version.

This function returns the BLE FIT module version.

The major version(BLE\_VERSION\_MAJOR) is contained in the two most significant bytes, and the minor version(BLE\_VERSION\_MINOR) occupies the remaining two bytes.

**Return values**

BLE_VERSION_MAJOR   BLE_VERSION_MINOR	
---------------------------------------	--

### ◆ R\_BLE\_GetLibType()

uint32\_t R\_BLE\_GetLibType ( void )

Get the type of BLE protocol stack library.

This function returns the type of BLE protocol stack library.

#### Return values

BLE_LIB_EXTENDED(0x00)	Extended
BLE_LIB_BALANCE(0x01)	Balance
BLE_LIB_COMPACT(0x02)	Compact

#### 4.2.5.1 GAP

Modules » Bluetooth Low Energy Library (r\_ble)

#### Functions

ble\_status\_t R\_BLE\_GAP\_Init (ble\_gap\_app\_cb\_t gap\_cb)

Initialize the Host Stack. [More...](#)

ble\_status\_t R\_BLE\_GAP\_Terminate (void)

Terminate the Host Stack. [More...](#)

ble\_status\_t R\_BLE\_GAP\_UpdConn (uint16\_t conn\_hdl, uint8\_t mode, uint16\_t accept, st\_ble\_gap\_conn\_param\_t \*p\_conn\_updt\_param)

Update the connection parameters. [More...](#)

ble\_status\_t R\_BLE\_GAP\_SetDataLen (uint16\_t conn\_hdl, uint16\_t tx\_octets, uint16\_t tx\_time)

Update the packet size and the packet transmit time. [More...](#)

ble\_status\_t R\_BLE\_GAP\_Disconnect (uint16\_t conn\_hdl, uint8\_t reason)

Disconnect the link. [More...](#)

ble\_status\_t R\_BLE\_GAP\_SetPhy (uint16\_t conn\_hdl, st\_ble\_gap\_set\_phy\_param\_t \*p\_phy\_param)

Set the phy for connection. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetDefPhy](#) (st\_ble\_gap\_set\_def\_phy\_param\_t \*p\_def\_phy\_param)  
Set the default phy which allows remote device to change. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetPrivMode](#) (st\_ble\_dev\_addr\_t \*p\_addr, uint8\_t \*p\_privacy\_mode, uint8\_t device\_num)  
Set the privacy mode. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ConfWhiteList](#) (uint8\_t op\_code, st\_ble\_dev\_addr\_t \*p\_addr, uint8\_t device\_num)  
Set White List. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_GetVerInfo](#) (void)  
Get the version number of the Controller and the host stack. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReadPhy](#) (uint16\_t conn\_hdl)  
Get the phy settings. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ConfRslvList](#) (uint8\_t op\_code, st\_ble\_dev\_addr\_t \*p\_addr, st\_ble\_gap\_rslv\_list\_key\_set\_t \*p\_peer\_irk, uint8\_t device\_num)  
Set Resolving List. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_EnableRpa](#) (uint8\_t enable)  
Enable/Disable address resolution and generation of a resolvable private address. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetRpaTo](#) (uint16\_t rpa\_timeout)  
Set the update time of resolvable private address. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReadRpa](#) (st\_ble\_dev\_addr\_t \*p\_addr)  
Get the resolvable private address of local device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReadRssi](#) (uint16\_t conn\_hdl)  
Get RSSI. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReadChMap](#) (uint16\_t conn\_hdl)  
Get the Channel Map. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetRandAddr](#) (uint8\_t \*p\_random\_addr)  
Set a random address. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetAdvParam](#) (st\_ble\_gap\_adv\_param\_t \*p\_adv\_param)  
Set advertising parameters. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetAdvSresData](#) (st\_ble\_gap\_adv\_data\_t \*p\_adv\_srsp\_data)  
Set advertising data/scan response data/periodic advertising data. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StartAdv](#) (uint8\_t adv\_hdl, uint16\_t duration, uint8\_t max\_extd\_adv\_evts)  
Start advertising. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StopAdv](#) (uint8\_t adv\_hdl)  
Stop advertising. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetPerdAdvParam](#) (st\_ble\_gap\_perd\_adv\_param\_t \*p\_perd\_adv\_param)  
Set periodic advertising parameters. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StartPerdAdv](#) (uint8\_t adv\_hdl)  
Start periodic advertising. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StopPerdAdv](#) (uint8\_t adv\_hdl)  
Stop periodic advertising. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_GetRemainAdvBufSize](#) (uint16\_t \*p\_remain\_adv\_data\_size, uint16\_t \*p\_remain\_perd\_adv\_data\_size)  
Get buffer size for advertising data/scan response data/periodic advertising data in the Controller. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_RemoveAdvSet](#) (uint8\_t op\_code, uint8\_t adv\_hdl)  
Delete advertising set. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_CreateConn](#) (st\_ble\_gap\_create\_conn\_param\_t \*p\_param)  
Request for a link establishment. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_CancelCreateConn](#) (void)  
Cancel the request for a link establishment. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetChMap](#) (uint8\_t \*p\_channel\_map)  
Set the Channel Map. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StartScan](#) (st\_ble\_gap\_scan\_param\_t \*p\_scan\_param, st\_ble\_gap\_scan\_on\_t \*p\_scan\_enable)  
Set scan parameter and start scan. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StopScan](#) (void)  
Stop scan. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_CreateSync](#) (st\_ble\_dev\_addr\_t \*p\_addr, uint8\_t adv\_sid, uint16\_t skip, uint16\_t sync\_to)  
Request for a periodic sync establishment. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_CancelCreateSync](#) (void)  
Cancel the request for a periodic sync establishment. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_TerminateSync](#) (uint16\_t sync\_hdl)  
Terminate the periodic sync. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ConfPerdAdvList](#) (uint8\_t op\_code, st\_ble\_dev\_addr\_t \*p\_addr, uint8\_t \*p\_adv\_sid\_set, uint8\_t device\_num)  
Set Periodic Advertiser List. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_AuthorizeDev](#) (uint16\_t conn\_hdl, uint8\_t author\_flag)

Authorize a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_GetRemDevInfo](#) (uint16\_t conn\_hdl)  
Get the information about remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetPairingParams](#) (st\_ble\_gap\_pairing\_param\_t \*p\_pair\_param)  
Set the parameters using pairing. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetLocIdInfo](#) (st\_ble\_dev\_addr\_t \*p\_lc\_id\_addr, uint8\_t \*p\_lc\_irk)  
Set the IRK and the identity address distributed to a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetLocCsrk](#) (uint8\_t \*p\_local\_csrk)  
Set the CSRK distributed to a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StartPairing](#) (uint16\_t conn\_hdl)  
Start pairing. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReplyPairing](#) (uint16\_t conn\_hdl, uint8\_t response)  
Reply the pairing request from a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_StartEnc](#) (uint16\_t conn\_hdl)  
Encryption the link. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReplyPasskeyEntry](#) (uint16\_t conn\_hdl, uint32\_t passkey, uint8\_t response)  
Reply the passkey entry request. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReplyNumComp](#) (uint16\_t conn\_hdl, uint8\_t response)  
Reply the numeric comparison request. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_NotifyKeyPress](#) (uint16\_t conn\_hdl, uint8\_t key\_press)  
Notify the input key type which a remote device inputs in the passkey entry. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_GetDevSecInfo](#) (uint16\_t conn\_hdl, st\_ble\_gap\_auth\_info\_t \*p\_sec\_info)  
Get the security information about the remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReplyExKeyInfoReq](#) (uint16\_t conn\_hdl)  
Distribute the keys of local device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetRemOobData](#) (st\_ble\_dev\_addr\_t \*p\_addr, uint8\_t oob\_data\_flag, st\_ble\_gap\_oob\_data\_t \*p\_oob)  
Set the oob data from a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_CreateScOobData](#) (void)  
Create data for oob in secure connection. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_SetBondInfo](#) (st\_ble\_gap\_bond\_info\_t \*p\_bond\_info, uint8\_t device\_num, uint8\_t \*p\_set\_num)  
Set the bonding information stored in non-volatile memory to the host stack. [More...](#)

void [R\\_BLE\\_GAP\\_DeleteBondInfo](#) (int32\_t local, int32\_t remote, st\_ble\_dev\_addr\_t \*p\_addr, ble\_gap\_del\_bond\_cb\_t gap\_del\_bond\_cb)  
This function deletes the bonding information in Host Stack. When a function for deleting the bonding information stored in non-volatile area is registered by the gap\_del\_bond\_cb parameter, it is deleted as well as the bonding information in Host Stack. [More...](#)

ble\_status\_t [R\\_BLE\\_GAP\\_ReplyLtkReq](#) (uint16\_t conn\_hdl, uint16\_t ediv, uint8\_t \*p\_peer\_rand, uint8\_t response)  
Reply the LTK request from a remote device. [More...](#)

## Detailed Description

(end addtogroup BLE\_API)

## Data Structures

struct [st\\_ble\\_evt\\_data\\_t](#)  
[st\\_ble\\_evt\\_data\\_t](#) is the type of the data notified in a GAP Event. [More...](#)

struct [st\\_ble\\_dev\\_addr\\_t](#)  
[st\\_ble\\_dev\\_addr\\_t](#) is the type of bluetooth device address(BD\_ADDR).  
[More...](#)

struct [st\\_ble\\_gap\\_ext\\_adv\\_param\\_t](#)  
Advertising parameters. [More...](#)

struct [st\\_ble\\_gap\\_adv\\_data\\_t](#)  
Advertising data/scan response data/periodic advertising data.  
[More...](#)

struct [st\\_ble\\_gap\\_perd\\_adv\\_param\\_t](#)  
Periodic advertising parameter. [More...](#)

struct [st\\_ble\\_gap\\_scan\\_phy\\_param\\_t](#)  
Scan parameters per scan PHY. [More...](#)

struct [st\\_ble\\_gap\\_ext\\_scan\\_param\\_t](#)  
Scan parameters. [More...](#)

struct [st\\_ble\\_gap\\_scan\\_on\\_t](#)  
Parameters configured when scanning starts. [More...](#)

struct [st\\_ble\\_gap\\_conn\\_param\\_t](#)  
Connection parameters included in connection interval, slave latency, supervision timeout, ce length. [More...](#)

struct [st\\_ble\\_gap\\_conn\\_phy\\_param\\_t](#)  
Connection parameters per PHY. [More...](#)

struct [st\\_ble\\_gap\\_create\\_conn\\_param\\_t](#)  
Connection parameters used in [R\\_BLE\\_GAP\\_CreateConn\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_rslv\\_list\\_key\\_set\\_t](#)

IRK of a remote device and IRK type of local device used in [R\\_BLE\\_GAP\\_ConfRslvList\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_set\\_phy\\_param\\_t](#)

PHY configuration parameters used in [R\\_BLE\\_GAP\\_SetPhy\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_set\\_def\\_phy\\_param\\_t](#)

PHY preferences which allows a remote device to set used in [R\\_BLE\\_GAP\\_SetDefPhy\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_auth\\_info\\_t](#)

Pairing parameters required from a remote device or information about keys distributed from a remote device. [More...](#)

struct [st\\_ble\\_gap\\_key\\_dist\\_t](#)

Keys distributed from a remote device. [More...](#)

struct [st\\_ble\\_gap\\_key\\_ex\\_param\\_t](#)

This structure includes the distributed keys and negotiated LTK size. [More...](#)

struct [st\\_ble\\_gap\\_pairing\\_param\\_t](#)

Pairing parameters used in [R\\_BLE\\_GAP\\_SetPairingParams\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_oob\\_data\\_t](#)

Oob data received from the remote device. This is used in [R\\_BLE\\_GAP\\_SetRemOobData\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_ver\\_num\\_t](#)

Version number of host stack. [More...](#)

struct [st\\_ble\\_gap\\_loc\\_ver\\_info\\_t](#)

Version number of Controller. [More...](#)

struct [st\\_ble\\_gap\\_loc\\_dev\\_info\\_evt\\_t](#)

Version information of local device. [More...](#)

struct [st\\_ble\\_gap\\_hw\\_err\\_evt\\_t](#)  
Hardware error that is notified from Controller. [More...](#)

struct [st\\_ble\\_gap\\_cmd\\_err\\_evt\\_t](#)  
HCI Command error. [More...](#)

struct [st\\_ble\\_gap\\_adv\\_rept\\_t](#)  
Advertising Report. [More...](#)

struct [st\\_ble\\_gap\\_ext\\_adv\\_rept\\_t](#)  
Extended Advertising Report. [More...](#)

struct [st\\_ble\\_gap\\_perd\\_adv\\_rept\\_t](#)  
Periodic Advertising Report. [More...](#)

struct [st\\_ble\\_gap\\_adv\\_rept\\_evt\\_t](#)  
Advertising report. [More...](#)

union [st\\_ble\\_gap\\_adv\\_rept\\_evt\\_t.param](#)  
Advertising Report. [More...](#)

struct [st\\_ble\\_gap\\_adv\\_set\\_evt\\_t](#)  
Advertising handle. [More...](#)

struct [st\\_ble\\_gap\\_adv\\_off\\_evt\\_t](#)  
Information about the advertising set which stops advertising.  
[More...](#)

struct [st\\_ble\\_gap\\_adv\\_data\\_evt\\_t](#)  
This structure notifies that advertising data has been set to Controller by [R\\_BLE\\_GAP\\_SetAdvSresData\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_rem\\_adv\\_set\\_evt\\_t](#)  
This structure notifies that an advertising set has been removed.

[More...](#)

struct [st\\_ble\\_gap\\_conn\\_evt\\_t](#)

This structure notifies that a link has been established. [More...](#)

struct [st\\_ble\\_gap\\_disconn\\_evt\\_t](#)

This structure notifies that a link has been disconnected. [More...](#)

struct [st\\_ble\\_gap\\_rd\\_ch\\_map\\_evt\\_t](#)

This structure notifies that Channel Map has been retrieved by [R\\_BLE\\_GAP\\_ReadChMap\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_rd\\_rssi\\_evt\\_t](#)

This structure notifies that RSSI has been retrieved by [R\\_BLE\\_GAP\\_ReadRssi\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_dev\\_info\\_evt\\_t](#)

This structure notifies that information about remote device has been retrieved by [R\\_BLE\\_GAP\\_GetRemDevInfo\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_conn\\_upd\\_evt\\_t](#)

This structure notifies that connection parameters has been updated. [More...](#)

struct [st\\_ble\\_gap\\_conn\\_upd\\_req\\_evt\\_t](#)

This structure notifies that a request for connection parameters update has been received. [More...](#)

struct [st\\_ble\\_gap\\_conn\\_hdl\\_evt\\_t](#)

This structure notifies that a GAP Event that includes only connection handle has occurred. [More...](#)

struct [st\\_ble\\_gap\\_data\\_len\\_chg\\_evt\\_t](#)

This structure notifies that the packet data length has been updated. [More...](#)

struct [st\\_ble\\_gap\\_rd\\_rpa\\_evt\\_t](#)

This structure notifies that the local resolvable private address has been retrieved by [R\\_BLE\\_GAP\\_ReadRpa\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_phy\\_upd\\_evt\\_t](#)

This structure notifies that PHY for a connection has been updated. [More...](#)

struct [st\\_ble\\_gap\\_phy\\_rd\\_evt\\_t](#)

This structure notifies that the PHY settings has been retrieved by [R\\_BLE\\_GAP\\_ReadPhy\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_scan\\_req\\_rcv\\_evt\\_t](#)

This structure notifies that a Scan Request packet has been received from a Scanner. [More...](#)

struct [st\\_ble\\_gap\\_sync\\_est\\_evt\\_t](#)

This structure notifies that a Periodic sync has been established. [More...](#)

struct [st\\_ble\\_gap\\_sync\\_hdl\\_evt\\_t](#)

This structure notifies that a GAP Event that includes only sync handle has occurred. [More...](#)

struct [st\\_ble\\_gap\\_white\\_list\\_conf\\_evt\\_t](#)

This structure notifies that White List has been configured. [More...](#)

struct [st\\_ble\\_gap\\_rslv\\_list\\_conf\\_evt\\_t](#)

This structure notifies that Resolving List has been configured. [More...](#)

struct [st\\_ble\\_gap\\_perd\\_list\\_conf\\_evt\\_t](#)

This structure notifies that Periodic Advertiser List has been configured. [More...](#)

struct [st\\_ble\\_gap\\_set\\_priv\\_mode\\_evt\\_t](#)

This structure notifies that Privacy Mode has been configured.

[More...](#)

struct [st\\_ble\\_gap\\_pairing\\_req\\_evt\\_t](#)

This structure notifies that a pairing request from a remote device has been received. [More...](#)

struct [st\\_ble\\_gap\\_passkey\\_display\\_evt\\_t](#)

This structure notifies that a request for Passkey display in pairing has been received. [More...](#)

struct [st\\_ble\\_gap\\_num\\_comp\\_evt\\_t](#)

This structure notifies that a request for Numeric Comparison in pairing has been received. [More...](#)

struct [st\\_ble\\_gap\\_key\\_press\\_ntf\\_evt\\_t](#)

This structure notifies that the remote device has input a key in Passkey Entry. [More...](#)

struct [st\\_ble\\_gap\\_pairing\\_info\\_evt\\_t](#)

This structure notifies that the pairing has completed. [More...](#)

struct [st\\_ble\\_gap\\_enc\\_chg\\_evt\\_t](#)

This structure notifies that the encryption status of a link has been changed. [More...](#)

struct [st\\_ble\\_gap\\_peer\\_key\\_info\\_evt\\_t](#)

This structure notifies that the remote device has distributed the keys. [More...](#)

struct [st\\_ble\\_gap\\_ltk\\_req\\_evt\\_t](#)

This structure notifies that a LTK request from a remote device has been received. [More...](#)

struct [st\\_ble\\_gap\\_ltk\\_rsp\\_evt\\_t](#)

This structure notifies that local device has replied to the LTK request from the remote device. [More...](#)

struct [st\\_ble\\_gap\\_sc\\_oob\\_data\\_evt\\_t](#)

This structure notifies that OOB data for Secure Connections has been generated by [R\\_BLE\\_GAP\\_CreateScOobData\(\)](#). [More...](#)

struct [st\\_ble\\_gap\\_bond\\_info\\_t](#)

Bonding information used in [R\\_BLE\\_GAP\\_SetBondInfo\(\)](#). [More...](#)

## Macros

#define [BLE\\_BD\\_ADDR\\_LEN](#)

#define [BLE\\_MASTER](#)

#define [BLE\\_SLAVE](#)

#define [BLE\\_GAP\\_ADDR\\_PUBLIC](#)

#define [BLE\\_GAP\\_ADDR\\_RAND](#)

#define [BLE\\_GAP\\_ADDR\\_RPA\\_ID\\_PUBLIC](#)

Resolvable Private Address. [More...](#)

#define [BLE\\_GAP\\_ADDR\\_RPA\\_ID\\_RANDOM](#)

Resolvable Private Address. [More...](#)

#define [BLE\\_GAP\\_AD\\_FLAGS\\_LE\\_LIM\\_DISC\\_MODE](#)

LE Limited Discoverable Mode flag used in AD type.

#define [BLE\\_GAP\\_AD\\_FLAGS\\_LE\\_GEN\\_DISC\\_MODE](#)

LE General Discoverable Mode flag used in AD type.

#define [BLE\\_GAP\\_AD\\_FLAGS\\_BR\\_EDR\\_NOT\\_SUPPORTED](#)

BR/EDR Not Supported flag used in AD type.

#define [BLE\\_GAP\\_ADV\\_DATA\\_MODE](#)

Advertising data.

#define [BLE\\_GAP\\_SCAN\\_RSP\\_DATA\\_MODE](#)

Scan response data.

```
#define BLE_GAP_PERD_ADV_DATA_MODE  
Periodic advertising data.
```

```
#define BLE_GAP_ADV_CH_37  
Use 37 CH.
```

```
#define BLE_GAP_ADV_CH_38  
Use 38 CH.
```

```
#define BLE_GAP_ADV_CH_39  
Use 39 CH.
```

```
#define BLE_GAP_ADV_CH_ALL  
Use 37 - 39 CH.
```

```
#define BLE_GAP_SCAN_PASSIVE  
Passive Scan.
```

```
#define BLE_GAP_SCAN_ACTIVE  
Active Scan.
```

```
#define BLE_GAP_SCAN_INTV_MIN  
Active Scan.
```

```
#define BLE_GAP_SCAN_FILT_DUPLIC_DISABLE  
Duplicate filter disabled.
```

```
#define BLE_GAP_SCAN_FILT_DUPLIC_ENABLE  
Duplicate filter enabled.
```

```
#define BLE_GAP_SCAN_FILT_DUPLIC_ENABLE_FOR_PERIOD  
Duplicate filtering enabled, reset for each scan period.
```

```
#define BLE_GAP_SCAN_ALLOW_ADV_ALL
```

Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.

```
#define BLE_GAP_SCAN_ALLOW_ADV_WLST
```

Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to local device is ignored.

```
#define BLE_GAP_SCAN_ALLOW_ADV_EXCEPT_DIRECTED
```

Accept all advertising and scan response PDUs except directed advertising PDUs whose the target address is identity address but doesn't address local device. However directed advertising PDUs whose the target address is the local resolvable private address are accepted.

```
#define BLE_GAP_SCAN_ALLOW_ADV_EXCEPT_DIRECTED_WLST
```

Accept all advertising and scan response PDUs.  
The following are excluded. [More...](#)

```
#define BLE_GAP_INIT_FILT_USE_ADDR
```

White List is not used.

```
#define BLE_GAP_INIT_FILT_USE_WLST
```

White List is used.

```
#define BLE_GAP_DATA_0_CLEAR
```

Clear the advertising data/scan response data/periodic advertising data in the advertising set.

```
#define BLE_GAP_DATA_0_DID_UPD
```

Update Advertising DID without changing advertising data.

```
#define BLE_GAP_NET_PRIV_MODE
```

Network Privacy Mode.

```
#define BLE_GAP_DEV_PRIV_MODE
```

Device Privacy Mode.

```
#define BLE_GAP_REM_FEATURE_SIZE
```

The length of the features supported by a remote device.

```
#define BLE_GAP_NOT_AUTHORIZED
```

Not authorize the remote device.

```
#define BLE_GAP_AUTHORIZED
```

Authorize the remote device.

```
#define BLE_GAP_RMV_ADV_SET_REM_OP
```

Delete an advertising set.

```
#define BLE_GAP_RMV_ADV_SET_CLR_OP
```

Delete all the advertising sets.

```
#define BLE_GAP_SC_PROC_GEN
```

General Discovery Procedure.

```
#define BLE_GAP_SC_PROC_LIM
```

Limited Discovery Procedure.

```
#define BLE_GAP_SC_PROC_OBS
```

Observation Procedure.

```
#define BLE_GAP_LIST_ADD_DEV
```

Add the device to the list.

```
#define BLE_GAP_LIST_REM_DEV
```

Delete the device from the list.

```
#define BLE_GAP_LIST_CLR
```

Clear the list.

```
#define BLE_GAP_WHITE_LIST_MAX_ENTRY
```

The maximum entry number of White List.

```
#define BLE_GAP_RSLV_LIST_MAX_ENTRY
```

The maximum entry number of Resolving List.

```
#define BLE_GAP_PERD_LIST_MAX_ENTRY
```

The maximum entry number of Periodic Advertiser List.

```
#define BLE_GAP_RPA_DISABLED
```

Disable RPA generation/resolution.

```
#define BLE_GAP_RPA_ENABLED
```

Enable RPA generation/resolution.

```
#define BLE_GAP_RL_LOC_KEY_ALL_ZERO
```

All-zero IRK.

```
#define BLE_GAP_RL_LOC_KEY_REGISTERED
```

The IRK registered by `R_BLE_GAP_SetLocIdInfo()`.

```
#define BLE_MAX_NO_OF_ADV_SETS_SUPPORTED
```

The maximum number of advertising set for the Abstraction API.

```
#define BLE_GAP_LEGACY_PROP_ADV_IND
```

Connectable and scannable undirected Legacy Advertising Packet.

```
#define BLE_GAP_LEGACY_PROP_ADV_DIRECT_IND
```

Connectable directed (low duty cycle) Legacy Advertising Packet.

```
#define BLE_GAP_LEGACY_PROP_ADV_HDC_DIRECT_IND
```

Connectable directed (high duty cycle) Legacy Advertising Packet.

```
#define BLE_GAP_LEGACY_PROP_ADV_SCAN_IND  
Scannable undirected Legacy Advertising Packet.
```

```
#define BLE_GAP_LEGACY_PROP_ADV_NONCONN_IND  
Non-connectable and non-scannable undirected Legacy Advertising  
Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_CONN_NOSCAN_UNDIRECT  
Connectable and non-scannable undirected Extended Advertising  
Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_CONN_NOSCAN_DIRECT  
Connectable and non-scannable directed (low duty cycle) Extended  
Advertising Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_CONN_NOSCAN_HDC_DIRECT  
Connectable and non-scannable directed (high duty cycle) Extended  
Advertising Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_SCAN_UNDIRECT  
Non-connectable and scannable undirected Extended Advertising  
Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_SCAN_DIRECT  
Non-connectable and scannable directed (low duty cycle) Extended  
Advertising Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_SCAN_HDC_DIRECT  
Non-connectable and scannable directed (high duty cycle) Extended  
Advertising Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_NOSCAN_UNDIRECT  
Non-connectable and non-scannable undirected Extended  
Advertising Packet.
```

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_NOSCAN_DIRECT  
Non-connectable and non-scannable directed (low duty cycle)
```

Extended Advertising Packet.

```
#define BLE_GAP_EXT_PROP_ADV_NOCONN_NOSCAN_HDC_DIRECT
```

Non-connectable and non-scannable directed (high duty cycle) Extended Advertising Packet.

```
#define BLE_GAP_EXT_PROP_ADV_ANONYMOUS
```

Omit the advertiser address from Extended Advertising Packet.

```
#define BLE_GAP_EXT_PROP_ADV_INCLUDE_TX_POWER
```

Indicate that the advertising data includes TX Power.

```
#define BLE_GAP_ADV_ALLOW_SCAN_ANY_CONN_ANY
```

Process scan and connection requests from all devices.

```
#define BLE_GAP_ADV_ALLOW_SCAN_WLST_CONN_ANY
```

Process connection requests from all devices and scan requests from only devices that are in the White List.

```
#define BLE_GAP_ADV_ALLOW_SCAN_ANY_CONN_WLST
```

Process scan requests from all devices and connection requests from only devices that are in the White List.

```
#define BLE_GAP_ADV_ALLOW_SCAN_WLST_CONN_WLST
```

Process scan and connection requests from only devices in the White List.

```
#define BLE_GAP_ADV_PHY_1M
```

Use 1M PHY.

```
#define BLE_GAP_ADV_PHY_2M
```

Use 2M PHY.

```
#define BLE_GAP_ADV_PHY_CD
```

Use Coded PHY.

```
#define BLE_GAP_SCAN_REQ_NTF_DISABLE
```

Disable Scan Request Notification.

```
#define BLE_GAP_SCAN_REQ_NTF_ENABLE
```

Enable Scan Request Notification.

```
#define BLE_GAP_PERD_PROP_TX_POWER
```

Indicate that periodic advertising data includes Tx Power.

```
#define BLE_GAP_INVALID_ADV_HDL
```

Invalid advertising handle.

```
#define BLE_GAP_SET_PHYS_HOST_PREF_1M
```

Use 1M PHY.

```
#define BLE_GAP_SET_PHYS_HOST_PREF_2M
```

Use 2M PHY.

```
#define BLE_GAP_SET_PHYS_HOST_PREF_CD
```

Use Coded PHY.

```
#define BLE_GAP_SET_PHYS_OP_HOST_NO_PREF
```

No preferred coding.

```
#define BLE_GAP_SET_PHYS_OP_HOST_PREF_S_2
```

Use S=2 coding.

```
#define BLE_GAP_SET_PHYS_OP_HOST_PREF_S_8
```

Use S=8 coding.

```
#define BLE_GAP_CONN_UPD_MODE_REQ
```

Request for updating the connection parameters.

`#define BLE_GAP_CONN_UPD_MODE_RSP`  
Reply a connection parameter update request.

`#define BLE_GAP_CONN_UPD_ACCEPT`  
Accept the update request.

`#define BLE_GAP_CONN_UPD_REJECT`  
Reject the update request.

`#define BLE_GAP_CH_MAP_SIZE`  
The size of channel map.

`#define BLE_GAP_INVALID_CONN_HDL`  
Invalid Connection handle.

`#define BLE_GAP_NOT_USE_CONN_HDL`  
This macro indicates that connection handle is not used.

`#define BLE_GAP_INIT_CONN_HDL`  
Initial Connection handle.

`#define BLE_GAP_PAIRING_ACCEPT`  
Accept a request regarding pairing.

`#define BLE_GAP_PAIRING_REJECT`  
Reject a request regarding pairing.

`#define BLE_GAP_LTK_REQ_ACCEPT`  
Reply for the LTK request.

`#define BLE_GAP_LTK_REQ_DENY`  
Reject the LTK request.

`#define BLE_GAP_LESC_PASSKEY_ENTRY_STARTED`

Notify that passkey entry started.

```
#define BLE_GAP_LESC_PASKEY_DIGIT_ENTERED  
Notify that passkey digit entered.
```

```
#define BLE_GAP_LESC_PASKEY_DIGIT_ERASED  
Notify that passkey digit erased.
```

```
#define BLE_GAP_LESC_PASKEY_CLEARED  
Notify that passkey cleared.
```

```
#define BLE_GAP_LESC_PASKEY_ENTRY_COMPLETED  
Notify that passkey entry completed.
```

```
#define BLE_GAP_SEC_MITM_BEST_EFFORT  
MITM Protection not required.
```

```
#define BLE_GAP_SEC_MITM_STRICT  
MITM Protection required.
```

```
#define BLE_GAP_KEY_DIST_ENCKEY  
LTK.
```

```
#define BLE_GAP_KEY_DIST_IDKEY  
IRK and Identity Address.
```

```
#define BLE_GAP_KEY_DIST_SIGNKEY  
CSRK.
```

```
#define BLE_GAP_ID_ADDR_SIZE  
The size of identity address.
```

```
#define BLE_GAP_IRK_SIZE  
The size of IRK.
```

```
#define BLE_GAP_CSRK_SIZE
    The size of CSRK.
```

```
#define BLE_GAP_LTK_SIZE
    The size of LTK.
```

```
#define BLE_GAP_EDIV_SIZE
    The size of EDIV.
```

```
#define BLE_GAP_RAND_64_BIT_SIZE
    The size of Rand.
```

```
#define BLE_GAP_UNAUTH_PAIRING
    Unauthenticated pairing.
```

```
#define BLE_GAP_AUTH_PAIRING
    Authenticated pairing.
```

```
#define BLE_GAP_LEGACY_PAIRING
    Legacy pairing.
```

```
#define BLE_GAP_LESC_PAIRING
    Secure Connections.
```

```
#define BLE_GAP_BONDING_NONE
    The device doesn't support Bonding.
```

```
#define BLE_GAP_BONDING
    The device supports Bonding.
```

```
#define BLE_GAP_IOCAP_DISPLAY_ONLY
    Display Only iocapability. More...
```

```
#define BLE_GAP_IOCAP_DISPLAY_YESNO
    Display Yes/No iocapability. More...
```

```
#define BLE_GAP_IOCAP_KEYBOARD_ONLY
    Keyboard Only iocapability. More...
```

```
#define BLE_GAP_IOCAP_NOINPUT_NOOUTPUT
    No Input No Output iocapability. More...
```

```
#define BLE_GAP_IOCAP_KEYBOARD_DISPLAY
    Keyboard Display iocapability. More...
```

```
#define BLE_GAP_OOB_DATA_NOT_PRESENT
    Reply that No OOB data has been received when pairing.
```

```
#define BLE_GAP_OOB_DATA_PRESENT
    Reply that the OOB data has been received when pairing.
```

```
#define BLE_GAP_SC_BEST_EFFORT
    Accept Legacy pairing and Secure Connections.
```

```
#define BLE_GAP_SC_STRICT
    Accept only Secure Connections.
```

```
#define BLE_GAP_SC_KEY_PRESS_NTF_NOT_SPRT
    Not support for Key Press Notification.
```

```
#define BLE_GAP_SC_KEY_PRESS_NTF_SPRT
    Support for Key Press Notification.
```

```
#define BLE_GAP_LEGACY_OOB_SIZE
    The size of Temporary Key for OOB in legacy pairing.
```

```
#define BLE_GAP_OOB_CONFIRM_VAL_SIZE
```

The size of Confirmation Value for OOB in Secure Connections.

```
#define BLE_GAP_OOB_RANDOM_VAL_SIZE
```

The size of Rand for OOB in Secure Connections.

```
#define BLE_GAP_SEC_DEL_LOC_NONE
```

Delete no local keys.

```
#define BLE_GAP_SEC_DEL_LOC_IRK
```

Delete local IRK.

```
#define BLE_GAP_SEC_DEL_LOC_CSRK
```

Delete local CSRK.

```
#define BLE_GAP_SEC_DEL_LOC_ALL
```

Delete all local keys.

```
#define BLE_GAP_SEC_DEL_REM_NONE
```

Delete no remote device keys.

```
#define BLE_GAP_SEC_DEL_REM_SA
```

Delete a key specified by the p\_addr parameter.

```
#define BLE_GAP_SEC_DEL_REM_NOT_CONN
```

Delete keys of not connected remote devices.

```
#define BLE_GAP_SEC_DEL_REM_ALL
```

Delete all remote device keys.

## Typedefs

```
typedef void(* ble_gap_app_cb_t) (uint16_t event_type, ble_status_t event_result,  
st_ble_evt_data_t *p_event_data)
```

ble\_gap\_app\_cb\_t is the GAP Event callback function type. [More...](#)

```
typedef void(* ble_gap_del_bond_cb_t) (st_ble_dev_addr_t *p_addr)
```

ble\_gap\_del\_bond\_cb\_t is the type of the callback function for delete bonding information stored in non-volatile area.  
This type is used in [R\\_BLE\\_GAP\\_DeleteBondInfo\(\)](#). [More...](#)

```
typedef st_ble_gap_adv_param_t
st_ble_gap_ext_adv_param_t
```

Advertising parameters. [More...](#)

```
typedef st_ble_gap_scan_param_t
st_ble_gap_ext_scan_param_t
```

Scan parameters. [More...](#)

## Enumerations

```
enum e_ble_gap_evt_t
```

GAP Event Identifier. [More...](#)

## Data Structure Documentation

### ◆ st\_ble\_evt\_data\_t

```
struct st_ble_evt_data_t
```

st\_ble\_evt\_data\_t is the type of the data notified in a GAP Event.

#### Data Fields

uint16_t	param_len	The size of GAP Event parameters.
void *	p_param	GAP Event parameters. This parameter differs in each GAP Event.

### ◆ st\_ble\_dev\_addr\_t

```
struct st_ble_dev_addr_t
```

st\_ble\_dev\_addr\_t is the type of bluetooth device address(BD\_ADDR).

#### Note

The BD address setting format is little endian.

If the address is "AA:BB:CC:DD:EE:FF", set the byte array in the order {0xFF, 0xEE, 0xDD, 0xCC, 0xBB, 0xAA}.

#### Data Fields

uint8_t	addr[BLE_BD_ADDR_LEN]	BD_ADDR.
---------	-----------------------	----------

uint8_t	type	Bluetooth address type.	
		macro	description
		BLE_GAP_ADD R_PUBLIC(0x00)	Public Address.
		BLE_GAP_ADD R_RAND(0x01)	Random Address.

◆ st\_ble\_gap\_ext\_adv\_param\_t

struct st_ble_gap_ext_adv_param_t											
Advertising parameters.											
Data Fields											
uint8_t	adv_hdl	Advertising handle identifying the advertising set to be set the advertising parameters.  Valid range is 0x00 - 0x03. In the first advertising parameters setting, the advertising set specified by adv_hdl is generated. The Advertising Set ID(Advertising SID) of the advertising set is same as adv_hdl.									
uint16_t	adv_prop_type	Advertising packet type.  Legacy advertising PDU type, or bitwise or of Extended advertising PDU type and Extended advertising option.									
		<table border="1"> <thead> <tr> <th>category</th> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>Legacy Advertising PDU type</td> <td>BLE_GAP_LEGACY_PROP_ADV_IND(0x0013)</td> <td>Connectable and scannable undirected Legacy Advertising Packet</td> </tr> <tr> <td></td> <td>BLE_GAP_LEGACY_PROP_ADV_DIRECT_IND(LOW_DUTY)</td> <td>Connectable directed (low duty)</td> </tr> </tbody> </table>	category	macro	description	Legacy Advertising PDU type	BLE_GAP_LEGACY_PROP_ADV_IND(0x0013)	Connectable and scannable undirected Legacy Advertising Packet		BLE_GAP_LEGACY_PROP_ADV_DIRECT_IND(LOW_DUTY)	Connectable directed (low duty)
category	macro	description									
Legacy Advertising PDU type	BLE_GAP_LEGACY_PROP_ADV_IND(0x0013)	Connectable and scannable undirected Legacy Advertising Packet									
	BLE_GAP_LEGACY_PROP_ADV_DIRECT_IND(LOW_DUTY)	Connectable directed (low duty)									

		0x0015)	cycle) Legacy A dvertisin g Packet
		BLE_GAP _LEGACY _PROP_A DV_HDC _DIRECT _IND(0x0 01D)	Connect able directed (high duty cycle) Legacy A dvertisin g Packet
		BLE_GAP _LEGACY _PROP_A DV_SCA N_IND(0 x0012)	Scannabl e undire cted Legacy A dvertisin g Packet
		BLE_GAP _LEGACY _PROP_A DV_NON CONN_IN D(0x001 0)	Non-con nectable and non- scannabl e undire cted Legacy A dvertisin g Packet
	Extende d Adverti sing PDU type	BLE_GAP _EXT_PR OP_ADV_ CONN_N OSCAN_ UNDIREC T(0x000 1)	Connect able and non-scan nable un directed Extende d Adverti sing Packet
		BLE_GAP _EXT_PR OP_ADV_ CONN_N OSCAN_ DIRECT( 0x0005)	Connect able and non-scan nable directed (low duty cycle) Extende d Adverti sing Packet
		BLE_GAP _EXT_PR	Connect able and

OP\_ADV\_CONN\_N  
OSCAN\_HDC\_DIR  
ECT(0x00D)

non-scan  
nable  
directed  
(high  
duty  
cycle)  
Extende  
d Adverti  
sing  
Packet

BLE\_GAP\_EXT\_PR  
OP\_ADV\_NOCONN  
\_SCAN\_UNDIRECT  
(0x0002)

Non-con  
nectable  
and scan  
nable un  
directed  
Extende  
d Adverti  
sing  
Packet

BLE\_GAP\_EXT\_PR  
OP\_ADV\_NOCONN  
\_SCAN\_DIRECT(0x  
0006)

Non-con  
nectable  
and scan  
nable  
directed  
(low  
duty  
cycle)  
Extende  
d Adverti  
sing  
Packet

BLE\_GAP\_EXT\_PR  
OP\_ADV\_NOCONN  
\_SCAN\_HDC\_DIRE  
CT(0x000E)

Non-con  
nectable  
and scan  
nable  
directed  
(high  
duty  
cycle)  
Extende  
d Adverti  
sing  
Packet

BLE\_GAP\_EXT\_PR  
OP\_ADV\_NOCONN  
\_NOSCAN\_UNDIR  
ECT(0x000)

Non-con  
nectable  
and non-  
scannabl  
e undire  
cted  
Extende  
d Adverti  
sing

		<p>Packet</p> <p>BLE_GAP_EXT_PR_OP_ADV_NOCONN_NOSCAN_DIRECT(0x0004) Non-connectable and non-scannable directed (low duty cycle) Extended Advertising Packet</p> <p>BLE_GAP_EXT_PR_OP_ADV_NOCONN_NOSCAN_HDC_DIRECT(0x000C) Non-connectable and non-scannable directed (high duty cycle) Extended Advertising Packet</p> <p>Extended Advertising Option BLE_GAP_EXT_PR_OP_ADV_ANONYMOUS(0x0020) Omit the advertiser address from Extended Advertising Packet.</p> <p>BLE_GAP_EXT_PR_OP_ADV_INCLUDE_TX_POWER(0x0040) Indicate that the advertising data includes TX Power.</p>
uint32_t	adv_intv_min	<p>Minimum advertising interval.</p> <p>Time(ms) = adv_intv_min * 0.625.</p> <p>Valid range is 0x00000020 - 0x00FFFFFFF.</p>
uint32_t	adv_intv_max	<p>Maximum Advertising interval.</p>

		<p>Time(ms) = adv_intv_max * 0.625. Valid range is 0x00000020 - 0x00FFFFFF.</p>										
uint8_t	adv_ch_map	<p>The adv_ch_map is channels used in advertising with primary advertising channels.</p> <p>It is a bitwise OR of the following values.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_ADV_CH_37(0x01)</td> <td>Use 37 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CH_38(0x02)</td> <td>Use 38 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CH_39(0x04)</td> <td>Use 39 CH.</td> </tr> <tr> <td>BLE_GAP_ADV_CH_ALL(0x07)</td> <td>Use 37 - 39 CH.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADV_CH_37(0x01)	Use 37 CH.	BLE_GAP_ADV_CH_38(0x02)	Use 38 CH.	BLE_GAP_ADV_CH_39(0x04)	Use 39 CH.	BLE_GAP_ADV_CH_ALL(0x07)	Use 37 - 39 CH.
macro	description											
BLE_GAP_ADV_CH_37(0x01)	Use 37 CH.											
BLE_GAP_ADV_CH_38(0x02)	Use 38 CH.											
BLE_GAP_ADV_CH_39(0x04)	Use 39 CH.											
BLE_GAP_ADV_CH_ALL(0x07)	Use 37 - 39 CH.											
uint8_t	o_addr_type	<p>Own BD Address Type.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_ADDR_PUBLIC(0x00)</td> <td>Public Address</td> </tr> <tr> <td>BLE_GAP_ADDR_RANDOM(0x01)</td> <td>Random Address</td> </tr> <tr> <td>BLE_GAP_ADDR_RPA_ID_PUBLIC(0x02)</td> <td>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.</td> </tr> <tr> <td>BLE_GAP_ADDR_RPA_ID_RANDOM(0x03)</td> <td>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, the random</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADDR_PUBLIC(0x00)	Public Address	BLE_GAP_ADDR_RANDOM(0x01)	Random Address	BLE_GAP_ADDR_RPA_ID_PUBLIC(0x02)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.	BLE_GAP_ADDR_RPA_ID_RANDOM(0x03)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, the random
macro	description											
BLE_GAP_ADDR_PUBLIC(0x00)	Public Address											
BLE_GAP_ADDR_RANDOM(0x01)	Random Address											
BLE_GAP_ADDR_RPA_ID_PUBLIC(0x02)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.											
BLE_GAP_ADDR_RPA_ID_RANDOM(0x03)	Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, the random											

		address specified by the o_addr field is used.						
uint8_t	o_addr[BLE_BD_ADDR_LEN]	<p>Random address set to the advertising set, when the o_addr_type field is BLE_GAP_ADDR_RAND.</p> <p>When the o_addr_type field is other than BLE_GAP_ADDR_RAND, this field is ignored.</p> <p><i>Note</i> The BD address setting format is little endian. If the address is "AA:BB:CC:DD:EE:FF", set the byte array in the order {0xFF, 0xEE, 0xDD, 0xCC, 0xBB, 0xAA}.</p>						
uint8_t	p_addr_type	<p>Peer address type.</p> <p>When the Advertising PDU type is other than directed or the o_addr_type is BLE_GAP_ADDR_PUBLIC or BLE_GAP_ADDR_RAND, this field is ignored.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_ADDR_PUBLIC(0x00)</td> <td>Public Address</td> </tr> <tr> <td>BLE_GAP_ADDR_RAND(0x01)</td> <td>Random Address</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADDR_PUBLIC(0x00)	Public Address	BLE_GAP_ADDR_RAND(0x01)	Random Address
macro	description							
BLE_GAP_ADDR_PUBLIC(0x00)	Public Address							
BLE_GAP_ADDR_RAND(0x01)	Random Address							
uint8_t	p_addr[BLE_BD_ADDR_LEN]	<p>Peer address.</p> <p>When the Advertising PDU type is other than directed or the o_addr_type is BLE_GAP_ADDR_PUBLIC or BLE_GAP_ADDR_RAND, this field is ignored.</p> <p><i>Note</i> The BD address setting format is little endian. If the address is</p>						

		<p><i>"AA:BB:CC:DD:EE:FF", set the byte array in the order {0xFF, 0xEE, 0xDD, 0xCC, 0xBB, 0xAA}.</i></p>										
uint8_t	filter_policy	<p>Advertising Filter Policy.</p> <table border="1"> <thead> <tr> <th data-bbox="1034 392 1252 443">macro</th> <th data-bbox="1252 392 1473 443">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1034 459 1252 593">BLE_GAP_ADV_ALLOW_SCAN_ANY(0x00)</td> <td data-bbox="1252 459 1473 593">Process scan and connection requests from all devices.</td> </tr> <tr> <td data-bbox="1034 638 1252 772">BLE_GAP_ADV_ALLOW_SCAN_WLST_ANY(0x01)</td> <td data-bbox="1252 638 1473 772">Process connection requests from all devices and scan requests from only devices that are in the White List.</td> </tr> <tr> <td data-bbox="1034 952 1252 1086">BLE_GAP_ADV_ALLOW_SCAN_WLST(0x02)</td> <td data-bbox="1252 952 1473 1086">Process scan requests from all devices and connection requests from only devices that are in the White List.</td> </tr> <tr> <td data-bbox="1034 1265 1252 1400">BLE_GAP_ADV_ALLOW_SCAN_WLST(0x03)</td> <td data-bbox="1252 1265 1473 1400">Process scan and connection requests from only devices in the White List.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_ADV_ALLOW_SCAN_ANY(0x00)	Process scan and connection requests from all devices.	BLE_GAP_ADV_ALLOW_SCAN_WLST_ANY(0x01)	Process connection requests from all devices and scan requests from only devices that are in the White List.	BLE_GAP_ADV_ALLOW_SCAN_WLST(0x02)	Process scan requests from all devices and connection requests from only devices that are in the White List.	BLE_GAP_ADV_ALLOW_SCAN_WLST(0x03)	Process scan and connection requests from only devices in the White List.
macro	description											
BLE_GAP_ADV_ALLOW_SCAN_ANY(0x00)	Process scan and connection requests from all devices.											
BLE_GAP_ADV_ALLOW_SCAN_WLST_ANY(0x01)	Process connection requests from all devices and scan requests from only devices that are in the White List.											
BLE_GAP_ADV_ALLOW_SCAN_WLST(0x02)	Process scan requests from all devices and connection requests from only devices that are in the White List.											
BLE_GAP_ADV_ALLOW_SCAN_WLST(0x03)	Process scan and connection requests from only devices in the White List.											
uint8_t	adv_phy	<p>Primary ADV PHY.</p> <p>In this parameter, only 1M PHY and Coded PHY can be specified, and 2M PHY cannot be specified.</p> <table border="1"> <thead> <tr> <th data-bbox="1034 1780 1252 1832">macro</th> <th data-bbox="1252 1780 1473 1832">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1034 1848 1252 1937">BLE_GAP_ADV_PHY_1M(0x01)</td> <td data-bbox="1252 1848 1473 1937">Use 1M PHY as Primary Advertising PHY.</td> </tr> </tbody> </table> <p>When the adv_prop_typ</p>	macro	description	BLE_GAP_ADV_PHY_1M(0x01)	Use 1M PHY as Primary Advertising PHY.						
macro	description											
BLE_GAP_ADV_PHY_1M(0x01)	Use 1M PHY as Primary Advertising PHY.											

		<p>e field is Legacy Advertising PDU type, this field shall be set to BLE_GAP_ADV_PHY_1M.</p> <p><a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a> Use Coded PHY(S=8) as Primary Advertising PHY. Coding scheme is configured by <a href="#">R_BLE_VS_SetCodingScheme()</a>.</p>								
uint8_t	sec_adv_max_skip	<p>Secondary ADV Max Skip.</p> <p>Valid range is 0x00 - 0xFF. When this field is 0x00, AUX_ADV_IND is sent before the next advertising event. When the adv_prop_type field is Legacy Advertising PDU, this field is ignored.</p>								
uint8_t	sec_adv_phy	<p>Secondary ADV Phy.</p> <p>When the adv_prop_type is Legacy Advertising PDU, this field is ignored.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a></td> <td>Use 1M PHY as Secondary Advertising PHY.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_PHY_2M(0x02)</a></td> <td>Use 2M PHY as Secondary Advertising PHY.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a></td> <td>Use Coded PHY(S=8) as Secondary Advertising PHY.</td> </tr> </tbody> </table> <p>Coding scheme is configured by <a href="#">R_BLE_VS_SetCodingScheme()</a>.</p>	macro	description	<a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a>	Use 1M PHY as Secondary Advertising PHY.	<a href="#">BLE_GAP_ADV_PHY_2M(0x02)</a>	Use 2M PHY as Secondary Advertising PHY.	<a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a>	Use Coded PHY(S=8) as Secondary Advertising PHY.
macro	description									
<a href="#">BLE_GAP_ADV_PHY_1M(0x01)</a>	Use 1M PHY as Secondary Advertising PHY.									
<a href="#">BLE_GAP_ADV_PHY_2M(0x02)</a>	Use 2M PHY as Secondary Advertising PHY.									
<a href="#">BLE_GAP_ADV_PHY_CD(0x03)</a>	Use Coded PHY(S=8) as Secondary Advertising PHY.									
uint8_t	scan_req_ntf_flag	Scan Request Notifications Flag.								

When the adv\_prop\_type field is non-scannable Advertising PDU, this field is ignored.

macro	description
<a href="#">BLE_GAP_SCAN_REQ_NTF_DISABLE(0x00)</a>	Disable Scan Request Notification.
<a href="#">BLE_GAP_SCAN_REQ_NTF_ENABLE(0x01)</a>	Enable Scan Request Notification. When a Scan Request Packet from Scanner has been received, the BLE_GAP_EVENT_SCAN_REQ_RECV event is notified.

◆ **st\_ble\_gap\_adv\_data\_t**

struct st_ble_gap_adv_data_t										
Advertising data/scan response data/periodic advertising data.										
Data Fields										
uint8_t	adv_hdl	Advertising handle identifying the advertising set to be set advertising data/scan response/periodic advertising data.  Valid range is 0x00 - 0x03.								
uint8_t	data_type	Data type. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_ADV_DATA_MODE(0x00)</a></td> <td>Advertising data.</td> </tr> <tr> <td><a href="#">BLE_GAP_SCAN_RSP_DATA_MODE(0x01)</a></td> <td>Scan response data.</td> </tr> <tr> <td><a href="#">BLE_GAP_PERIODIC_ADV_DATA_MODE(0x02)</a></td> <td>Periodic advertising data.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_ADV_DATA_MODE(0x00)</a>	Advertising data.	<a href="#">BLE_GAP_SCAN_RSP_DATA_MODE(0x01)</a>	Scan response data.	<a href="#">BLE_GAP_PERIODIC_ADV_DATA_MODE(0x02)</a>	Periodic advertising data.
macro	description									
<a href="#">BLE_GAP_ADV_DATA_MODE(0x00)</a>	Advertising data.									
<a href="#">BLE_GAP_SCAN_RSP_DATA_MODE(0x01)</a>	Scan response data.									
<a href="#">BLE_GAP_PERIODIC_ADV_DATA_MODE(0x02)</a>	Periodic advertising data.									
uint16_t	data_length	The length of advertising								

		<p>data/scan response data/periodic advertising data (in bytes).</p> <p>In case of Legacy Advertising PDU, the length is 0 - 31 bytes. In case of Extended Advertising PDU, the length is 0 - 1650 bytes.</p> <p>Note that the length of the advertising data/scan response data in the BLE_MAX_NO_OF_ADV_SETS_SUPPORTED number of the advertising sets may not exceed the buffer size(4250 bytes) in Controller.</p> <p>In case of periodic advertising data, the length is 0 - 1650 bytes.</p> <p>Note that the length of the periodic advertising data in the BLE_MAX_NO_OF_ADV_SETS_SUPPORTED number of the advertising sets may not exceed the buffer size(4306 bytes) in Controller.</p> <p>When this field is 0, the operations specified by the zero_length_flag is executed.</p>				
uint8_t *	p_data	<p>Advertising data/scan response data/periodic advertising data.</p> <p>When the data_length field is 0, this field is ignored.</p>				
uint8_t	zero_length_flag	<p>Operation when the data_length field is 0.</p> <p>If the data_length is other than 0, this field is ignored.</p> <table border="1" data-bbox="1034 1639 1473 2045"> <thead> <tr> <th data-bbox="1034 1639 1252 1697">macro</th> <th data-bbox="1252 1639 1473 1697">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1034 1697 1252 2045">BLE_GAP_DATA_0_CLEAR(0x01)</td> <td data-bbox="1252 1697 1473 2045">Clear the advertising data/scan response data/periodic advertising data in the advertising set.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_DATA_0_CLEAR(0x01)	Clear the advertising data/scan response data/periodic advertising data in the advertising set.
macro	description					
BLE_GAP_DATA_0_CLEAR(0x01)	Clear the advertising data/scan response data/periodic advertising data in the advertising set.					

		<p><b>BLE_GAP_DATA_0_DID_UPD(0x02)</b> Update Advertising DID without changing advertising data. If the data_type field is BLE_GAP_ADV_DATA_MODE, this value is allowed.</p>
--	--	--

◆ **st\_ble\_gap\_perd\_adv\_param\_t**

struct st_ble_gap_perd_adv_param_t						
Periodic advertising parameter.						
Data Fields						
uint8_t	adv_hdl	<p>Advertising handle identifying the advertising set to be set periodic advertising parameter.</p> <p>Valid range is 0x00 - 0x03.</p>				
uint16_t	prop_type	<p>Periodic ADV Properties.</p> <p>The prop_type field is set to the following values.</p> <p>If the type of the periodic advertising data cannot be applied from the following, set 0x0000.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><b>BLE_GAP_PERIOD_PROP_TX_POWER(0x0040)</b></td> <td>Indicate that periodic advertising data includes Tx Power.</td> </tr> </tbody> </table>	macro	description	<b>BLE_GAP_PERIOD_PROP_TX_POWER(0x0040)</b>	Indicate that periodic advertising data includes Tx Power.
macro	description					
<b>BLE_GAP_PERIOD_PROP_TX_POWER(0x0040)</b>	Indicate that periodic advertising data includes Tx Power.					
uint16_t	perd_intv_min	<p>Minimum Periodic Advertising Interval.</p> <p>Time(ms) = perd_intv_min * 1.25.</p> <p>Valid range is 0x0006 - 0xFFFF.</p>				
uint16_t	perd_intv_max	<p>Maximum Periodic Advertising Interval.</p> <p>Time(ms) = perd_intv_max * 1.25.</p> <p>Valid range is 0x0006 - 0xFFFF.</p>				

◆ **st\_ble\_gap\_scan\_phy\_param\_t**

struct st_ble_gap_scan_phy_param_t						
Scan parameters per scan PHY.						
In case of start scanning with both 1M PHY and Coded PHY, adjust scan windows and scan intervals according to the following. $p\_phy\_param\_1M \rightarrow scan\_window / p\_phy\_param\_1M \rightarrow scan\_intv + p\_phy\_param\_coded \rightarrow scan\_window / p\_phy\_param\_coded \rightarrow scan\_intv \leq 1$						
Data Fields						
uint8_t	scan_type	Scan type.				
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_SCAN_PASSIVE(0x00)</code></td> <td>Passive Scan.</td> </tr> <tr> <td><code>BLE_GAP_SCAN_ACTIVE(0x01)</code></td> <td>Active Scan.</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_SCAN_PASSIVE(0x00)</code>	Passive Scan.
macro	description					
<code>BLE_GAP_SCAN_PASSIVE(0x00)</code>	Passive Scan.					
<code>BLE_GAP_SCAN_ACTIVE(0x01)</code>	Active Scan.					
uint16_t	scan_intv	Scan interval. $interval(ms) = scan\_intv * 0.625.$ Valid range is 0x0000 and 0x0004 - 0xFFFF.				
uint16_t	scan_window	Scan window. $window(ms) = scan\_window * 0.625.$ Valid range is 0x0000 and 0x0004 - 0xFFFF.				

◆ **st\_ble\_gap\_ext\_scan\_param\_t**

struct st_ble_gap_ext_scan_param_t						
Scan parameters.						
Data Fields						
uint8_t	o_addr_type	Own BD Address Type. In case of passive scan, this field is ignored.				
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_ADD_PUBLIC(0x00)</code></td> <td>Public Address</td> </tr> <tr> <td><code>BLE_GAP_ADD_RANDOM(0x01)</code></td> <td>Random Address</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_ADD_PUBLIC(0x00)</code>	Public Address
macro	description					
<code>BLE_GAP_ADD_PUBLIC(0x00)</code>	Public Address					
<code>BLE_GAP_ADD_RANDOM(0x01)</code>	Random Address					

		<p><a href="#">BLE_GAP_ADD_R_RPA_ID_PUBLIC(0x02)</a> Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.</p> <p><a href="#">BLE_GAP_ADD_R_RPA_ID_RANDOM(0x03)</a> Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, the random address set by <a href="#">R_BLE_GAP_SetRandAddr()</a> is used.</p>						
uint8_t	filter_policy	<p>Scan Filter Policy.</p> <table border="1"> <thead> <tr> <th data-bbox="1023 1093 1251 1151">macro</th> <th data-bbox="1251 1093 1474 1151">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1023 1151 1251 1496"><a href="#">BLE_GAP_SCAN_ALLOW_ALL(0x00)</a></td> <td data-bbox="1251 1151 1474 1496">Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.</td> </tr> <tr> <td data-bbox="1023 1496 1251 2047"><a href="#">BLE_GAP_SCAN_ALLOW_WHITE_LIST(0x01)</a></td> <td data-bbox="1251 1496 1474 2047">Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_SCAN_ALLOW_ALL(0x00)</a>	Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.	<a href="#">BLE_GAP_SCAN_ALLOW_WHITE_LIST(0x01)</a>	Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to
macro	description							
<a href="#">BLE_GAP_SCAN_ALLOW_ALL(0x00)</a>	Accept all advertising and scan response PDUs except directed advertising PDUs not addressed to local device.							
<a href="#">BLE_GAP_SCAN_ALLOW_WHITE_LIST(0x01)</a>	Accept only advertising and scan response PDUs from remote devices whose address is registered in the White List. Directed advertising PDUs which are not addressed to							

BLE\_GAP\_SCAN\_ALLOW\_ADVERTISING\_EXCEPT\_DIRECTED(0x02)

local device is ignored.

Accept all advertising and scan response PDUs except directed advertising PDUs whose the target address is identity address but doesn't address local device. However directed advertising PDUs whose the target address is the local resolvable private address are accepted.

BLE\_GAP\_SCAN\_ALLOW\_ADVERTISING\_EXCEPT\_DIRECTED\_WLIST(0x03)

Accept all advertising and scan response PDUs. The following are excluded.

- Advertising and scan response PDUs where the advertiser's identity address is not in the White

		<p>List.</p> <ul style="list-style-type: none"> <li>• Directed advertising PDUs whose the target address is identity address but doesn't address local device. However directed advertising PDUs whose the target address is the local resolvable private address are accepted.</li> </ul>
<a href="#">st_ble_gap_scan_phy_param_t</a> *	p_phy_param_1M	<p>Scan parameters 1M PHY.</p> <p>When this field is NULL, Controller doesn't set the scan parameters for 1M PHY.</p>
<a href="#">st_ble_gap_scan_phy_param_t</a> *	p_phy_param_coded	<p>Scan parameters Coded PHY.</p> <p>When this field is NULL, Controller doesn't set the scan parameters for Coded PHY.</p>

◆ **st\_ble\_gap\_scan\_on\_t**

struct st_ble_gap_scan_on_t								
Parameters configured when scanning starts.								
Data Fields								
uint8_t	proc_type	Procedure type.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_SCAN_PROC_OBS(0x00)</a></td> <td>Observation Procedure. Notify all advertising PDUs.</td> </tr> <tr> <td><a href="#">BLE_GAP_SCAN_PROC_LIM(0x01)</a></td> <td>Limited Discovery Procedure. Notify advertising PDUs from only devices in the limited discoverable mode.</td> </tr> <tr> <td><a href="#">BLE_GAP_SCAN_PROC_GEN(0x02)</a></td> <td>General Discovery Procedure. Notify advertising PDUs from devices in the limited discoverable mode and the general discoverable mode.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_SCAN_PROC_OBS(0x00)</a>	Observation Procedure. Notify all advertising PDUs.	<a href="#">BLE_GAP_SCAN_PROC_LIM(0x01)</a>	Limited Discovery Procedure. Notify advertising PDUs from only devices in the limited discoverable mode.
macro	description							
<a href="#">BLE_GAP_SCAN_PROC_OBS(0x00)</a>	Observation Procedure. Notify all advertising PDUs.							
<a href="#">BLE_GAP_SCAN_PROC_LIM(0x01)</a>	Limited Discovery Procedure. Notify advertising PDUs from only devices in the limited discoverable mode.							
<a href="#">BLE_GAP_SCAN_PROC_GEN(0x02)</a>	General Discovery Procedure. Notify advertising PDUs from devices in the limited discoverable mode and the general discoverable mode.							
uint8_t	filter_dups	Filter duplicates.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)</a></td> <td>Duplicate filter disabled.</td> </tr> <tr> <td><a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE(0x01)</a></td> <td>Duplicate filter enabled.</td> </tr> <tr> <td><a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE_RESET_PERIOD(0x02)</a></td> <td>Duplicate filtering enabled, reset for each scan period</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)</a>	Duplicate filter disabled.	<a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE(0x01)</a>	Duplicate filter enabled.
macro	description							
<a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_DISABLE(0x00)</a>	Duplicate filter disabled.							
<a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE(0x01)</a>	Duplicate filter enabled.							
<a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLE_RESET_PERIOD(0x02)</a>	Duplicate filtering enabled, reset for each scan period							

uint16_t	duration	Scan duration.  Time(ms) = duration * 10. Valid range is 0x0000 - 0xFFFF. If this field is set to 0x0000, scanning is continued until <a href="#">R_BLE_GAP_StopScan()</a> is called. When the period field is zero and the time specified the duration field expires, BLE_GAP_EVENT_SCAN_TO event notifies the application layer that scanning stops.
uint16_t	period	Scan period.  Time(s) = N * 1.28. Valid range is 0x0000 - 0xFFFF. If the duration field is set to 0x0000, this field is ignored.

#### ◆ st\_ble\_gap\_conn\_param\_t

struct st_ble_gap_conn_param_t		
Connection parameters included in connection interval, slave latency, supervision timeout, ce length.  This structure is used in <a href="#">R_BLE_GAP_CreateConn()</a> and <a href="#">R_BLE_GAP_UpdConn()</a> .  Set the fields in this structure to match the following condition.  Supervision_timeout(ms) >= (1 + conn_latency) * conn_intv_max_Time(ms) conn_intv_max_Time(ms) = conn_intv_max * 1.25 Supervision_timeout(ms) = sup_to * 10		
Data Fields		
uint16_t	conn_intv_min	Minimum connection interval.  Time(ms) = conn_intv_min * 1.25. Valid range is 0x0006 - 0x0C80.
uint16_t	conn_intv_max	Maximum connection interval.  Time(ms) = conn_intv_max * 1.25. Valid range is 0x0006 - 0x0C80.
uint16_t	conn_latency	Slave latency.  Valid range is 0x0000 - 0x01F3.
uint16_t	sup_to	Supervision timeout.

		Time(ms) = sup_to * 10. Valid range is 0x000A - 0x0C80.
uint16_t	min_ce_length	Minimum CE Length. Valid range is 0x0000 - 0xFFFF.
uint16_t	max_ce_length	Maximum CE Length. Valid range is 0x0000 - 0xFFFF.

#### ◆ st\_ble\_gap\_conn\_phy\_param\_t

struct st_ble_gap_conn_phy_param_t		
Connection parameters per PHY.		
Data Fields		
uint16_t	scan_intv	Scan interval. Time(ms) = scan_intv * 0.625. Valid range is 0x0004 - 0xFFFF.
uint16_t	scan_window	Scan window. Time(ms) = scan_window * 0.625. Valid range is 0x0004 - 0xFFFF.
st_ble_gap_conn_param_t *	p_conn_param	Connection interval, slave latency, supervision timeout, and CE length.

#### ◆ st\_ble\_gap\_create\_conn\_param\_t

struct st_ble_gap_create_conn_param_t						
Connection parameters used in R_BLE_GAP_CreateConn().						
Data Fields						
uint8_t	init_filter_policy	This field specifies whether the White List is used or not, when connecting with a remote device.				
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_INIT_FILTER_USE_ADDRESS(0x00)</td> <td>White List is not used. The remote device to be connected is specified by the <i>remote_bd_addr</i> field and the</td> </tr> </tbody> </table>	macro	description	BLE_GAP_INIT_FILTER_USE_ADDRESS(0x00)	White List is not used. The remote device to be connected is specified by the <i>remote_bd_addr</i> field and the
macro	description					
BLE_GAP_INIT_FILTER_USE_ADDRESS(0x00)	White List is not used. The remote device to be connected is specified by the <i>remote_bd_addr</i> field and the					

		<p><i>remote_bd_addr_type</i> field is used.</p> <p><b>BLE_GAP_INIT_FILTER_USE_WHITE_LIST(0x01)</b> White List is used. The remote device registered in White List is connected with local device. The <i>remote_bd_addr</i> field and the <i>remote_bd_addr_type</i> field are ignored.</p>						
uint8_t	remote_bd_addr[ <b>BLE_BD_ADDR_LEN</b> ]	<p>Address of the device to be connected.</p> <p><i>Note</i></p> <p>The BD address setting format is little endian.</p> <p>If the address is "AA:BB:CC:DD:EE:FF", set the byte array in the order {0xFF, 0xEE, 0xDD, 0xCC, 0xBB, 0xAA}.</p>						
uint8_t	remote_bd_addr_type	<p>Address type of the device to be connected.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><b>BLE_GAP_ADD_R_PUBLIC(0x00)</b></td> <td>Public Address or Public Identity Address</td> </tr> <tr> <td><b>BLE_GAP_ADD_R_RANDOM(0x01)</b></td> <td>Random Address or Random (Static) Identity Address</td> </tr> </tbody> </table>	macro	description	<b>BLE_GAP_ADD_R_PUBLIC(0x00)</b>	Public Address or Public Identity Address	<b>BLE_GAP_ADD_R_RANDOM(0x01)</b>	Random Address or Random (Static) Identity Address
macro	description							
<b>BLE_GAP_ADD_R_PUBLIC(0x00)</b>	Public Address or Public Identity Address							
<b>BLE_GAP_ADD_R_RANDOM(0x01)</b>	Random Address or Random (Static) Identity Address							
uint8_t	own_addr_type	<p>Address type which local device uses in creating a link with the remote device.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><b>BLE_GAP_ADD_R_PUBLIC(0x00)</b></td> <td>Public Address</td> </tr> </tbody> </table>	macro	description	<b>BLE_GAP_ADD_R_PUBLIC(0x00)</b>	Public Address		
macro	description							
<b>BLE_GAP_ADD_R_PUBLIC(0x00)</b>	Public Address							

		<p>0)</p> <p>BLE_GAP_ADD R_RAND(0x01 )</p> <p>BLE_GAP_ADD R_RPA_ID_PUB LIC(0x02)</p> <p>BLE_GAP_ADD R_RPA_ID_RA NDOM(0x03)</p> <p>Random Address</p> <p>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, public address is used.</p> <p>Resolvable Private Address. If the IRK of local device has not been registered in Resolving List, the random address set by <a href="#">R_BLE_GAP_SetRandAddr()</a>.</p>
<a href="#">st_ble_gap_conn_phy_param_t</a> *	p_conn_param_1M	<p>Connection parameters for 1M PHY.</p> <p>If this field is set to NULL, 1M PHY is not used in connecting.</p>
<a href="#">st_ble_gap_conn_phy_param_t</a> *	p_conn_param_2M	<p>Connection parameters for 2M PHY.</p> <p>If this field is set to NULL, 2M PHY is not used in connecting.</p>
<a href="#">st_ble_gap_conn_phy_param_t</a> *	p_conn_param_coded	<p>Connection parameters for Coded PHY.</p> <p>If this field is set to NULL, Coded PHY is not used in connecting.</p>

◆ [st\\_ble\\_gap\\_rslv\\_list\\_key\\_set\\_t](#)

struct <a href="#">st_ble_gap_rslv_list_key_set_t</a>	
IRK of a remote device and IRK type of local device used in <a href="#">R_BLE_GAP_ConfRslvList()</a> .	
Data Fields	

uint8_t	remote_irk[BLE_GAP_IRK_SIZE]	IRK of a remote device to be registered in the Resolving List.						
uint8_t	local_irk_type	IRK type of the local device to be registered in the Resolving List. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_RL_LOCAL_KEY_ALL_ZERO(0x00)</td> <td>All-zero IRK.</td> </tr> <tr> <td>BLE_GAP_RL_LOCAL_KEY_REGISTERED(0x01)</td> <td>The IRK registered by R_BLE_GAP_SetLocalInfo().</td> </tr> </tbody> </table>	macro	description	BLE_GAP_RL_LOCAL_KEY_ALL_ZERO(0x00)	All-zero IRK.	BLE_GAP_RL_LOCAL_KEY_REGISTERED(0x01)	The IRK registered by R_BLE_GAP_SetLocalInfo().
macro	description							
BLE_GAP_RL_LOCAL_KEY_ALL_ZERO(0x00)	All-zero IRK.							
BLE_GAP_RL_LOCAL_KEY_REGISTERED(0x01)	The IRK registered by R_BLE_GAP_SetLocalInfo().							

### ◆ st\_ble\_gap\_set\_phy\_param\_t

struct st_ble_gap_set_phy_param_t										
PHY configuration parameters used in R_BLE_GAP_SetPhy().										
Data Fields										
uint8_t	tx_phys	Transmitter PHY preference. The tx_phys field is set to a bitwise OR of the following values. All other values are ignored. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)</td> <td>Use 1M PHY for Transmitter PHY.</td> </tr> <tr> <td>BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</td> <td>Use 2M PHY for Transmitter PHY.</td> </tr> <tr> <td>BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</td> <td>Use Coded PHY for Transmitter PHY.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)	Use 1M PHY for Transmitter PHY.	BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)	Use 2M PHY for Transmitter PHY.	BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)	Use Coded PHY for Transmitter PHY.
macro	description									
BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)	Use 1M PHY for Transmitter PHY.									
BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)	Use 2M PHY for Transmitter PHY.									
BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)	Use Coded PHY for Transmitter PHY.									
uint8_t	rx_phys	Receiver PHY preference. The rx_phys field is set to a bitwise OR of the following values. All other values are ignored. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> </table>	macro	description						
macro	description									

		<p><code>BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)</code> Use 1M PHY for Receiver PHY.</p> <p><code>BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</code> Use 2M PHY for Receiver PHY.</p> <p><code>BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</code> Use Coded PHY for Receiver PHY.</p>								
<code>uint16_t</code>	<code>phy_options</code>	<p>Coding scheme used in Coded PHY.</p> <p>Select one of the following.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_SET_PHYS_OP_HOST_NO_PREF(0x00)</code></td> <td>No preferred coding.</td> </tr> <tr> <td><code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_2(0x01)</code></td> <td>Use S=2 coding.</td> </tr> <tr> <td><code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_8(0x02)</code></td> <td>Use S=8 coding.</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_SET_PHYS_OP_HOST_NO_PREF(0x00)</code>	No preferred coding.	<code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_2(0x01)</code>	Use S=2 coding.	<code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_8(0x02)</code>	Use S=8 coding.
macro	description									
<code>BLE_GAP_SET_PHYS_OP_HOST_NO_PREF(0x00)</code>	No preferred coding.									
<code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_2(0x01)</code>	Use S=2 coding.									
<code>BLE_GAP_SET_PHYS_OP_HOST_PREF_S_8(0x02)</code>	Use S=8 coding.									

◆ `st_ble_gap_set_def_phy_param_t`

<code>struct st_ble_gap_set_def_phy_param_t</code>						
PHY preferences which allows a remote device to set used in <code>R_BLE_GAP_SetDefPhy()</code> .						
Data Fields						
<code>uint8_t</code>	<code>tx_phys</code>	<p>Transmitter PHY preferences which a remote device may change.</p> <p>The <code>tx_phys</code> field is set to a bitwise OR of the following values. All other values are ignored.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><code>BLE_GAP_SET_PHYS_HOST_</code></td> <td>Allow a remote device</td> </tr> </tbody> </table>	macro	description	<code>BLE_GAP_SET_PHYS_HOST_</code>	Allow a remote device
macro	description					
<code>BLE_GAP_SET_PHYS_HOST_</code>	Allow a remote device					

		<p><a href="#">PREF_1M(0x01)</a> to set 1M PHY for transmitter PHY.</p> <p><a href="#">BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</a> Allow a remote device to set 2M PHY for transmitter PHY.</p> <p><a href="#">BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</a> Allow a remote device to set Coded PHY for transmitter PHY.</p>								
uint8_t	rx_phys	<p>Receiver PHY preferences which a remote device may change.</p> <p>The rx_phys field is set to a bitwise OR of the following values. All other values are ignored.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)</a></td> <td>Allow a remote device to set 1M PHY for receiver PHY.</td> </tr> <tr> <td><a href="#">BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</a></td> <td>Allow a remote device to set 2M PHY for receiver PHY.</td> </tr> <tr> <td><a href="#">BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</a></td> <td>Allow a remote device to set Coded PHY for receiver PHY.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)</a>	Allow a remote device to set 1M PHY for receiver PHY.	<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</a>	Allow a remote device to set 2M PHY for receiver PHY.	<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</a>	Allow a remote device to set Coded PHY for receiver PHY.
macro	description									
<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_1M(0x01)</a>	Allow a remote device to set 1M PHY for receiver PHY.									
<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_2M(0x02)</a>	Allow a remote device to set 2M PHY for receiver PHY.									
<a href="#">BLE_GAP_SET_PHYS_HOST_PREF_CD(0x04)</a>	Allow a remote device to set Coded PHY for receiver PHY.									

◆ **st\_ble\_gap\_auth\_info\_t**

struct st_ble_gap_auth_info_t		
Pairing parameters required from a remote device or information about keys distributed from a remote device.		
Data Fields		
uint8_t	security	Security level.

		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The remote device requests Unauthenticated pairing.</td> </tr> <tr> <td>0x02</td> <td>The remote device requests Authenticated pairing.</td> </tr> </tbody> </table>	value	description	0x01	The remote device requests Unauthenticated pairing.	0x02	The remote device requests Authenticated pairing.
value	description							
0x01	The remote device requests Unauthenticated pairing.							
0x02	The remote device requests Authenticated pairing.							
uint8_t	pair_mode	Pairing mode. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The remote device requests Legacy pairing.</td> </tr> <tr> <td>0x02</td> <td>The remote device requests Secure Connections.</td> </tr> </tbody> </table>	value	description	0x01	The remote device requests Legacy pairing.	0x02	The remote device requests Secure Connections.
value	description							
0x01	The remote device requests Legacy pairing.							
0x02	The remote device requests Secure Connections.							
uint8_t	bonding	Bonding policy. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>The remote device does not store the Bonding information.</td> </tr> <tr> <td>0x01</td> <td>The remote device stores the Bonding information.</td> </tr> </tbody> </table>	value	description	0x00	The remote device does not store the Bonding information.	0x01	The remote device stores the Bonding information.
value	description							
0x00	The remote device does not store the Bonding information.							
0x01	The remote device stores the Bonding information.							
uint8_t	ekey_size	Encryption key size.						

◆ **st\_ble\_gap\_key\_dist\_t**

struct st_ble_gap_key_dist_t		
Keys distributed from a remote device.		
Data Fields		
uint8_t	enc_info[BLE_GAP_LTK_SIZE]	LTK.
uint8_t	mid_info[BLE_GAP_EDIV_SIZE + BLE_GAP_RAND_64_BIT_SIZE]	Ediv and rand. The first two bytes is ediv, the remaining bytes are rand.

uint8_t	id_info[BLE_GAP_IRK_SIZE]	IRK.
uint8_t	id_addr_info[ BLE_GAP_ID_ADDR_SIZE]	Identity address. The first byte is address type. The remaining bytes are device address.
uint8_t	sign_info[BLE_GAP_CSRK_SIZE]	CSRK.

#### ◆ st\_ble\_gap\_key\_ex\_param\_t

struct st_ble_gap_key_ex_param_t										
This structure includes the distributed keys and negotiated LTK size.										
Data Fields										
st_ble_gap_key_dist_t *	p_keys_info	Key information.								
uint8_t	keys	Type of the distributed keys.  This field is a bitwise OR of the following values.								
		<table border="1"> <thead> <tr> <th>Bit Number</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LTK and Master Identification. LTK is distributed in Secure Connections, even if the bit is 1.</td> </tr> <tr> <td>1</td> <td>IRK and Identity Address Information.</td> </tr> <tr> <td>2</td> <td>CSRK</td> </tr> </tbody> </table>	Bit Number	description	0	LTK and Master Identification. LTK is distributed in Secure Connections, even if the bit is 1.	1	IRK and Identity Address Information.	2	CSRK
Bit Number	description									
0	LTK and Master Identification. LTK is distributed in Secure Connections, even if the bit is 1.									
1	IRK and Identity Address Information.									
2	CSRK									
uint8_t	ekey_size	The negotiated LTK size.								

#### ◆ st\_ble\_gap\_pairing\_param\_t

struct st_ble_gap_pairing_param_t						
Pairing parameters used in <a href="#">R_BLE_GAP_SetPairingParams()</a> .						
Data Fields						
uint8_t	iocap	IO capabilities of local device.  Select one of the following.				
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_IOC</a></td> <td>Output</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_IOC</a>	Output
macro	description					
<a href="#">BLE_GAP_IOC</a>	Output					

AP\_DISPLAY\_ONLY(0x00) function :  
Local device has the ability to display a 6 digit decimal number.  
Input function : None

BLE\_GAP\_IOC AP\_DISPLAY\_YESNO(0x01) Output function :  
Output function :  
Local device has the ability to display a 6 digit decimal number.  
Input function : Local device has the ability to indicate 'yes' or 'no'

BLE\_GAP\_IOC AP\_KEYBOARD\_ONLY(0x02) Output function :  
None  
Input function : Local device has the ability to input the number '0' - '9'.

BLE\_GAP\_IOC AP\_NOINPUT\_NOOUTPUT(0x03) Output function :  
None  
Input function : None

BLE\_GAP\_IOC AP\_KEYBOARD\_DISPLAY(0x04) Output function :  
Output function :  
Local device has the ability to display a 6 digit decimal number.  
Input function : Local device has the ability

		to input the number '0' - '9'.						
uint8_t	mitm	<p>MITM protection policy.</p> <p>Select one of the following.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_SEC_MITM_BEST_EFFORT(0x00)</a></td> <td>MITM Protection not required.</td> </tr> <tr> <td><a href="#">BLE_GAP_SEC_MITM_STRICT(0x01)</a></td> <td>MITM Protection required.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_SEC_MITM_BEST_EFFORT(0x00)</a>	MITM Protection not required.	<a href="#">BLE_GAP_SEC_MITM_STRICT(0x01)</a>	MITM Protection required.
macro	description							
<a href="#">BLE_GAP_SEC_MITM_BEST_EFFORT(0x00)</a>	MITM Protection not required.							
<a href="#">BLE_GAP_SEC_MITM_STRICT(0x01)</a>	MITM Protection required.							
uint8_t	bonding	<p>Bonding policy.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_BONDING_NONE(0x00)</a></td> <td>Local device doesn't store Bonding information.</td> </tr> <tr> <td><a href="#">BLE_GAP_BONDING(0x01)</a></td> <td>Local device stores Bonding information.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_BONDING_NONE(0x00)</a>	Local device doesn't store Bonding information.	<a href="#">BLE_GAP_BONDING(0x01)</a>	Local device stores Bonding information.
macro	description							
<a href="#">BLE_GAP_BONDING_NONE(0x00)</a>	Local device doesn't store Bonding information.							
<a href="#">BLE_GAP_BONDING(0x01)</a>	Local device stores Bonding information.							
uint8_t	max_key_size	<p>Maximum LTK size(in bytes).</p> <p>Valid range is 7 - 16. This field shall be set to a value not less than the min_key_size field.</p>						
uint8_t	min_key_size	<p>Minimum LTK size(in bytes).</p> <p>Valid range is 7 - 16. This field shall be set to a value not more than the max_key_size field.</p>						
uint8_t	loc_key_dist	<p>Type of keys to be distributed from local device.</p> <p>The loc_key_dist field is set to a bitwise OR of the following values.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_KEY_DIST_ENCKEY</a></td> <td>LTK</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_KEY_DIST_ENCKEY</a>	LTK		
macro	description							
<a href="#">BLE_GAP_KEY_DIST_ENCKEY</a>	LTK							

		<p>(0x01)</p> <p>BLE_GAP_KEY_DIST_IDKEY(0x02) IRK and Identity Address.</p> <p>BLE_GAP_KEY_DIST_SIGNKEY(0x04) CSRK</p>								
uint8_t	rem_key_dist	<p>Type of keys which local device requests a remote device to distribute.</p> <p>The rem_key_dist field is set to a bitwise OR of the following values.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_KEY_DIST_ENCKEY(0x01)</td> <td>LTK. In case of Secure Connections, LTK is notified even if this bit is not set.</td> </tr> <tr> <td>BLE_GAP_KEY_DIST_IDKEY(0x02)</td> <td>IRK and Identity Address.</td> </tr> <tr> <td>BLE_GAP_KEY_DIST_SIGNKEY(0x04)</td> <td>CSRK</td> </tr> </tbody> </table>	macro	description	BLE_GAP_KEY_DIST_ENCKEY(0x01)	LTK. In case of Secure Connections, LTK is notified even if this bit is not set.	BLE_GAP_KEY_DIST_IDKEY(0x02)	IRK and Identity Address.	BLE_GAP_KEY_DIST_SIGNKEY(0x04)	CSRK
macro	description									
BLE_GAP_KEY_DIST_ENCKEY(0x01)	LTK. In case of Secure Connections, LTK is notified even if this bit is not set.									
BLE_GAP_KEY_DIST_IDKEY(0x02)	IRK and Identity Address.									
BLE_GAP_KEY_DIST_SIGNKEY(0x04)	CSRK									
uint8_t	key_notf	<p>Support for Key Press Notification in Passkey Entry.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_SC_KEY_PRESS_NOTIFICATION_NOT_SUPPORT(0x00)</td> <td>Not support for Key Press Notification.</td> </tr> <tr> <td>BLE_GAP_SC_KEY_PRESS_NOTIFICATION_SUPPORT(0x01)</td> <td>Support for Key Press Notification.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_SC_KEY_PRESS_NOTIFICATION_NOT_SUPPORT(0x00)	Not support for Key Press Notification.	BLE_GAP_SC_KEY_PRESS_NOTIFICATION_SUPPORT(0x01)	Support for Key Press Notification.		
macro	description									
BLE_GAP_SC_KEY_PRESS_NOTIFICATION_NOT_SUPPORT(0x00)	Not support for Key Press Notification.									
BLE_GAP_SC_KEY_PRESS_NOTIFICATION_SUPPORT(0x01)	Support for Key Press Notification.									
uint8_t	sec_conn_only	<p>Determine whether to accept only Secure Connections or not.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_SC_BEST_EFFORT(0x00)</td> <td>Accept Legacy pairing and Secure</td> </tr> </tbody> </table>	macro	description	BLE_GAP_SC_BEST_EFFORT(0x00)	Accept Legacy pairing and Secure				
macro	description									
BLE_GAP_SC_BEST_EFFORT(0x00)	Accept Legacy pairing and Secure									

		Connections. <b>BLE_GAP_SC_STRICT(0x01)</b> Accept only Secure Connections.
--	--	--

#### ◆ st\_ble\_gap\_oob\_data\_t

struct st_ble_gap_oob_data_t		
Oob data received from the remote device. This is used in <a href="#">R_BLE_GAP_SetRemOobData()</a> .		
Data Fields		
uint8_t	legacy_oob[ <a href="#">BLE_GAP_LEGACY_OOB_SIZE</a> ]	OOB data used in Legacy Pairing.
uint8_t	sc_cnf_val[ <a href="#">BLE_GAP_OOB_CONFIRM_VAL_SIZE</a> ]	OOB confirmation value used in Secure Connections.
uint8_t	sc_rand[ <a href="#">BLE_GAP_OOB_RANDOM_VAL_SIZE</a> ]	OOB rand used in Secure Connections.

#### ◆ st\_ble\_gap\_ver\_num\_t

struct st_ble_gap_ver_num_t		
Version number of host stack.		
Data Fields		
uint8_t	major	Major version number.
uint8_t	minor	Minor version number.
uint8_t	subminor	Subminor version number.

#### ◆ st\_ble\_gap\_loc\_ver\_info\_t

struct st_ble_gap_loc_ver_info_t		
Version number of Controller. Refer Bluetooth SIG Assigned Number( <a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a> ).		
Data Fields		
uint8_t	hci_ver	Bluetooth HCI version.
uint16_t	hci_rev	Bluetooth HCI revision.
uint8_t	imp_ver	Link Layer revision.
uint16_t	mnf_name	Manufacturer ID.
uint16_t	imp_sub_ver	Link Layer subversion.

#### ◆ st\_ble\_gap\_loc\_dev\_info\_evt\_t

struct st_ble_gap_loc_dev_info_evt_t		
--------------------------------------	--	--

Version information of local device.		
Data Fields		
<code>st_ble_dev_addr_t</code>	<code>l_dev_addr</code>	Bluetooth Device Address.
<code>st_ble_gap_ver_num_t</code>	<code>l_ver_num</code>	Version number of host stack in local device.
<code>st_ble_gap_loc_ver_info_t</code>	<code>l_bt_info</code>	Version number of Controller in local device.

◆ `st_ble_gap_hw_err_evt_t`

struct <code>st_ble_gap_hw_err_evt_t</code>		
Hardware error that is notified from Controller.		
Data Fields		
<code>uint8_t</code>	<code>hw_code</code>	The <code>hw_code</code> field indicates the cause of the hardware error.

◆ `st_ble_gap_cmd_err_evt_t`

struct <code>st_ble_gap_cmd_err_evt_t</code>		
HCI Command error.		
Data Fields		
<code>uint16_t</code>	<code>op_code</code>	The opcode of HCI Command which caused the error.
<code>uint32_t</code>	<code>module_id</code>	Module ID which caused the error.

◆ `st_ble_gap_adv_rept_t`

struct <code>st_ble_gap_adv_rept_t</code>								
Advertising Report.								
Data Fields								
<code>uint8_t</code>	<code>num</code>	The number of Advertising Reports received.						
<code>uint8_t</code>	<code>adv_type</code>	Type of Advertising Packet. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">valuer</th> <th style="width: 80%;">description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Connectable and scannable undirected advertising(ADV_IND).</td> </tr> <tr> <td>0x01</td> <td>Connectable directed advertising(ADV_DIRECT_IND).</td> </tr> </tbody> </table>	valuer	description	0x00	Connectable and scannable undirected advertising(ADV_IND).	0x01	Connectable directed advertising(ADV_DIRECT_IND).
valuer	description							
0x00	Connectable and scannable undirected advertising(ADV_IND).							
0x01	Connectable directed advertising(ADV_DIRECT_IND).							

		0x02	Scannable undirected advertising(ADV_SCAN_IND).
		0x03	Non-connectable undirected advertising(ADV_NONCONN_IND).
		0x04	Scan response(SCAN_RSP).
uint8_t	addr_type	Address type of the advertiser.	
		value	description
		0x00	Public Address.
		0x01	Random Address.
		0x02	Public Identity Address which could be resolved in Controller.
		0x03	Random Identity Address which could be resolved in Controller.
uint8_t *	p_addr	Address of the advertiser.	
		<i>Note</i> The BD address setting format is little endian.	
uint8_t	len	Length of Advertising data(in bytes).	
		Valid range is 0 - 31.	
int8_t	rss	RSSI(in dBm).	
		Valid range is -127 <= tx_pwr <= 20 and 127. If the tx_pwr is 127, it means that RSSI could not be retrieved.	
uint8_t *	p_data	Advertising data/Scan Response Data.	

◆ **st\_ble\_gap\_ext\_adv\_rept\_t**

struct st_ble_gap_ext_adv_rept_t																
Extended Advertising Report.																
Data Fields																
uint8_t	num	The number of Advertising Reports received.														
uint16_t	adv_type	Type of Advertising Packet.														
		<table border="1"> <thead> <tr> <th>Bit Number</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Connectable advertising.</td> </tr> <tr> <td>1</td> <td>Scannable advertising.</td> </tr> <tr> <td>2</td> <td>Directed advertising.</td> </tr> <tr> <td>3</td> <td>Scan response.</td> </tr> <tr> <td>4</td> <td>Legacy advertising PDU.</td> </tr> <tr> <td>5-6</td> <td>The status of Advertising Data/Scan Response Data. Data Status: 00b = Complete 01b = Incomplete, more data come 10b = Incomplete, data truncated, no more to come</td> </tr> <tr> <td>All other bits</td> <td>Reserved for future use</td> </tr> </tbody> </table>	Bit Number	description	0	Connectable advertising.	1	Scannable advertising.	2	Directed advertising.	3	Scan response.	4	Legacy advertising PDU.	5-6	The status of Advertising Data/Scan Response Data. Data Status: 00b = Complete 01b = Incomplete, more data come 10b = Incomplete, data truncated, no more to come
Bit Number	description															
0	Connectable advertising.															
1	Scannable advertising.															
2	Directed advertising.															
3	Scan response.															
4	Legacy advertising PDU.															
5-6	The status of Advertising Data/Scan Response Data. Data Status: 00b = Complete 01b = Incomplete, more data come 10b = Incomplete, data truncated, no more to come															
All other bits	Reserved for future use															
uint8_t	addr_type	Address type of the advertiser.														
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Public Address.</td> </tr> <tr> <td>0x01</td> <td>Random</td> </tr> </tbody> </table>	value	description	0x00	Public Address.	0x01	Random								
value	description															
0x00	Public Address.															
0x01	Random															

		<p>Address.</p> <p>0x02 Public Identity Address which could be resolved in Controller.</p> <p>0x03 Random Identity Address which could be resolved in Controller.</p> <p>0xFF Anonymous advertisement</p>								
uint8_t *	p_addr	<p>Address of the advertiser.</p> <p><i>Note</i> The BD address setting format is little endian.</p>								
uint8_t	adv_phy	<p>The primary PHY configuration of the advertiser.</p> <p>The primary PHY configuration of the advertiser.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>1M PHY</td> </tr> <tr> <td>0x03</td> <td>Coded PHY</td> </tr> </tbody> </table>	value	description	0x01	1M PHY	0x03	Coded PHY		
value	description									
0x01	1M PHY									
0x03	Coded PHY									
uint8_t	sec_adv_phy	<p>The secondary PHY configuration of the advertiser.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Nothing has been received with Secondary Advertising Channel.</td> </tr> <tr> <td>0x01</td> <td>The Secondary Advertising PHY configuration was 1M PHY.</td> </tr> <tr> <td>0x02</td> <td>The Secondary Advertising</td> </tr> </tbody> </table>	value	description	0x00	Nothing has been received with Secondary Advertising Channel.	0x01	The Secondary Advertising PHY configuration was 1M PHY.	0x02	The Secondary Advertising
value	description									
0x00	Nothing has been received with Secondary Advertising Channel.									
0x01	The Secondary Advertising PHY configuration was 1M PHY.									
0x02	The Secondary Advertising									

		<p>PHY configuration was 2M PHY.</p> <p>0x03 The Secondary Advertising PHY configuration was Coded PHY.</p>						
uint8_t	adv_sid	<p>Advertising SID included in the received Advertising Report.</p> <p>Valid range is <math>0 \leq \text{adv\_sid} \leq 0x0F</math> and <math>0xFF</math>. If the adv_sid is 0xFF, there is no field which includes SID.</p>						
int8_t	tx_pwr	<p>TX power(in dBm).</p> <p>Valid range is <math>-127 \leq \text{tx\_pwr} \leq 20</math> and <math>127</math>. If the tx_pwr is 127, it means that Tx power could not be retrieved.</p>						
int8_t	rssr	<p>RSSI(in dBm).</p> <p>Valid range is <math>-127 \leq \text{tx\_pwr} \leq 20</math> and <math>127</math>. If the tx_pwr is 127, it means that RSSI could not be retrieved.</p>						
uint16_t	perd_adv_intv	<p>Periodic Advertising interval.</p> <p>If the perd_adv_intv is 0x0000, it means that this advertising is not periodic advertising. If the perd_adv_intv is 0x0006 - 0xFFFF, it means that this field is the Periodic Advertising interval. Periodic Advertising interval = per_adv_intr * 1.25ms.</p>						
uint8_t	dir_addr_type	<p>The address type of Direct Advertising PDU.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Public Address.</td> </tr> <tr> <td>0x01</td> <td>Random Address.</td> </tr> </tbody> </table>	value	description	0x00	Public Address.	0x01	Random Address.
value	description							
0x00	Public Address.							
0x01	Random Address.							

		<p>0x02 Public Identity Address which could be resolved in Controller.</p> <p>0x03 Random Identity Address which could be resolved in Controller.</p> <p>0xFE Resolvable Privacy Address which could not be resolved in Controller.</p>
uint8_t *	p_dir_addr	<p>Address of Direct Advertising PDU.</p> <p><i>Note</i> The BD address setting format is little endian.</p>
uint8_t	len	<p>Length of Advertising data(in bytes).</p> <p>Valid range is 0 - 229.</p>
uint8_t *	p_data	Advertising data/Scan Response Data.

#### ◆ st\_ble\_gap\_perd\_adv\_rept\_t

struct st_ble_gap_perd_adv_rept_t		
Periodic Advertising Report.		
Data Fields		
uint16_t	sync_hdl	<p>Sync handle.</p> <p>Valid range is 0x0000 - 0x0EFF.</p>
int8_t	tx_pwr	<p>TX power(in dBm).</p> <p>Valid range is -127 &lt;= tx_pwr &lt;= 20 and 127. If tx_pwr is 127, it means that Tx power could not be retrieved.</p>
int8_t	rssi	<p>RSSI(in dBm).</p> <p>Valid range is -127 &lt;= rssi &lt;=</p>

		20 and 127. If rssi is 127, it means that RSSI could not be retrieved.								
uint8_t	rfu	Reserved for future use.								
uint8_t	data_status	Reserved for future use. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Data Complete.</td> </tr> <tr> <td>0x01</td> <td>Data incomplete, more data to come.</td> </tr> <tr> <td>0x02</td> <td>Data incomplete, data truncated, no more to come.</td> </tr> </tbody> </table>	value	description	0x00	Data Complete.	0x01	Data incomplete, more data to come.	0x02	Data incomplete, data truncated, no more to come.
value	description									
0x00	Data Complete.									
0x01	Data incomplete, more data to come.									
0x02	Data incomplete, data truncated, no more to come.									
uint8_t	len	Length of Periodic Advertising data(in bytes).  Valid range is 0 - 247.								
uint8_t *	p_data	Periodic Advertising data.								

◆ **st\_ble\_gap\_adv\_rept\_evt\_t**

struct st_ble_gap_adv_rept_evt_t										
Advertising report.										
Data Fields										
uint8_t	adv_rpt_type	Data type. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Advertising Report.</td> </tr> <tr> <td>0x01</td> <td>Extended Advertising Report.</td> </tr> <tr> <td>0x02</td> <td>Periodic Advertising Report.</td> </tr> </tbody> </table> <p>If the BLE Protocol Stack library type is "extended", the adv_rpt_type field in a Legacy Advertising Report event is 0x01.</p>	value	description	0x00	Advertising Report.	0x01	Extended Advertising Report.	0x02	Periodic Advertising Report.
value	description									
0x00	Advertising Report.									
0x01	Extended Advertising Report.									
0x02	Periodic Advertising Report.									

union <a href="#">st_ble_gap_adv_rept_evt_t</a>	param	Advertising Report.
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◆ [st\\_ble\\_gap\\_adv\\_rept\\_evt\\_t.param](#)

union <a href="#">st_ble_gap_adv_rept_evt_t.param</a>		
Advertising Report.		
Data Fields		
<a href="#">st_ble_gap_adv_rept_t</a> *	p_adv_rpt	Advertising Report.
<a href="#">st_ble_gap_ext_adv_rept_t</a> *	p_ext_adv_rpt	Extended Advertising Report.
<a href="#">st_ble_gap_perd_adv_rept_t</a> *	p_per_adv_rpt	Periodic Advertising Report.

◆ [st\\_ble\\_gap\\_adv\\_set\\_evt\\_t](#)

struct <a href="#">st_ble_gap_adv_set_evt_t</a>		
Advertising handle.		
Data Fields		
uint8_t	adv_hdl	Advertising handle specifying the advertising set configured advertising parameters.

◆ [st\\_ble\\_gap\\_adv\\_off\\_evt\\_t](#)

struct <a href="#">st_ble_gap_adv_off_evt_t</a>								
Information about the advertising set which stops advertising.								
Data Fields								
uint8_t	adv_hdl	Advertising handle identifying the advertising set which has stopped advertising.  Valid range is 0x00 - 0x03.						
uint8_t	reason	The reason for stopping advertising. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">value</th> <th style="width: 80%;">description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>Advertising has been stopped by <a href="#">R_BLE_GAP_StopAdv()</a>.</td> </tr> <tr> <td>0x02</td> <td>Because the duration specified by <a href="#">R_BLE_GAP_StartAdv()</a> was expired, advertising</td> </tr> </tbody> </table>	value	description	0x01	Advertising has been stopped by <a href="#">R_BLE_GAP_StopAdv()</a> .	0x02	Because the duration specified by <a href="#">R_BLE_GAP_StartAdv()</a> was expired, advertising
value	description							
0x01	Advertising has been stopped by <a href="#">R_BLE_GAP_StopAdv()</a> .							
0x02	Because the duration specified by <a href="#">R_BLE_GAP_StartAdv()</a> was expired, advertising							

		<p>has terminated.</p> <p>0x03 Because the max_extd_adv_evts parameter specified by <a href="#">R_BLE_GAP_StartAdv()</a> was reached, advertising has terminated.</p> <p>0x04 Because the connection was established with the remote device, advertising has terminated.</p>
uint16_t	conn_hdl	<p>Connection handle.</p> <p>If the reason field is 0x04, this field indicates connection handle identifying the remote device connected with local device. If other reasons, ignore this field.</p>
uint8_t	num_comp_ext_adv_evts	<p>The number of the advertising event that has been received until advertising has terminated.</p> <p>If max_extd_adv_evts by <a href="#">R_BLE_GAP_StartAdv()</a> is not 0, this parameter is valid.</p>

#### ◆ st\_ble\_gap\_adv\_data\_evt\_t

struct st_ble_gap_adv_data_evt_t		
This structure notifies that advertising data has been set to Controller by <a href="#">R_BLE_GAP_SetAdvSresData()</a> .		
Data Fields		
uint8_t	adv_hdl	Advertising handle identifying the advertising set to which advertising data/scan response data/periodic advertising data is set.

uint8_t	data_type	Type of the data set to the advertising set.	
		value	description
		BLE_GAP_ADV_DATA_MODE(0x00)	Advertising data
		BLE_GAP_SCAN_RSP_DATA_MODE(0x01)	Scan response data
		BLE_GAP_PERIODIC_ADV_DATA_MODE(0x02)	Periodic advertising data

#### ◆ st\_ble\_gap\_rem\_adv\_set\_evt\_t

struct st_ble_gap_rem_adv_set_evt_t						
This structure notifies that an advertising set has been removed.						
Data Fields						
uint8_t	remove_op	This field indicates that the advertising set has been removed or cleared.				
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The advertising set has been removed.</td> </tr> <tr> <td>0x02</td> <td>The advertising set has been cleared.</td> </tr> </tbody> </table>	value	description	0x01	The advertising set has been removed.
value	description					
0x01	The advertising set has been removed.					
0x02	The advertising set has been cleared.					
uint8_t	adv_hdl	Advertising handle identifying the advertising set which has been removed.  If the advertising set has been cleared, this field is ignored.				

#### ◆ st\_ble\_gap\_conn\_evt\_t

struct st_ble_gap_conn_evt_t		
This structure notifies that a link has been established.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the created link.
uint8_t	role	The role of the link.

		value	description
		0x00	Master
		0x01	Slave
uint8_t	remote_addr_type	Address type of the remote device.	
		value	description
		0x00	Public Address
		0x01	Random Address
		0x02	Public Identity Address. It indicates that the Controller could resolve the resolvable private address of the remote device.
		0x03	Random Identity Address. It indicates that the Controller could resolve the resolvable private address of the remote device.
uint8_t	remote_addr[ <a href="#">BLE_BD_ADDR_LEN</a> ]	Address of the remote device.	
		<i>Note</i> The BD address setting format is little endian.	
uint8_t	local_rpa[ <a href="#">BLE_BD_ADDR_LEN</a> ]	Resolvable private address that local device used in connection procedure.	
		The local device address used in creating the link when the address type was set to <a href="#">BLE_GAP_ADDR_RPA_ID_PUBLIC</a> or <a href="#">BLE_GAP_ADDR_RPA_ID_RANDOM</a> by	

		<p><a href="#">R_BLE_GAP_SetAdvParam()</a> or <a href="#">R_BLE_GAP_CreateConn()</a>. If the address type was set to other than BLE_GAP_ADDR_RPA_ID_PUBLIC and BLE_GAP_ADDR_RPA_ID_RANDOM, this field is set to all-zero.</p> <p><i>Note</i> The BD address setting format is little endian.</p>														
uint8_t	remote_rpa[BLE_BD_ADDR_LEN]	<p>Resolvable private address that the remote device used in connection procedure.</p> <p>This field indicates the remote resolvable private address when remote_addr_type is 0x02 or 0x03. If remote_addr_type is other than 0x02 and 0x03, this field is set to all-zero.</p> <p><i>Note</i> The BD address setting format is little endian.</p>														
uint16_t	conn_intv	<p>Connection interval.</p> <p>Valid range is 0x0006 - 0x0C80. Time(ms) = conn_intv * 1.25.</p>														
uint16_t	conn_latency	<p>Slave latency.</p> <p>Valid range is 0x0000 - 0x01F3.</p>														
uint16_t	sup_to	<p>Supervision timeout.</p> <p>Valid range is 0x000A - 0x0C80. Time(ms) = sup_to * 10.</p>														
uint8_t	clk_acc	<p>Master_Clock_Accuracy.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>500ppm</td> </tr> <tr> <td>0x01</td> <td>250ppm</td> </tr> <tr> <td>0x02</td> <td>150ppm</td> </tr> <tr> <td>0x03</td> <td>100ppm</td> </tr> <tr> <td>0x04</td> <td>75ppm</td> </tr> <tr> <td>0x05</td> <td>50ppm</td> </tr> </tbody> </table>	value	description	0x00	500ppm	0x01	250ppm	0x02	150ppm	0x03	100ppm	0x04	75ppm	0x05	50ppm
value	description															
0x00	500ppm															
0x01	250ppm															
0x02	150ppm															
0x03	100ppm															
0x04	75ppm															
0x05	50ppm															

		0x06	30ppm
		0x07	20ppm

#### ◆ st\_ble\_gap\_disconn\_evt\_t

struct st_ble_gap_disconn_evt_t		
This structure notifies that a link has been disconnected.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the link disconnected.
uint8_t	reason	The reason for disconnection.  Refer Core Specification Vol.2 Part D , "2 Error Code Descriptions".

#### ◆ st\_ble\_gap\_rd\_ch\_map\_evt\_t

struct st_ble_gap_rd_ch_map_evt_t		
This structure notifies that Channel Map has been retrieved by <a href="#">R_BLE_GAP_ReadChMap()</a> .		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the link whose Channel Map was retrieved.
uint8_t	ch_map[ <a href="#">BLE_GAP_CH_MAP_SIZE</a> ]	Channel Map.

#### ◆ st\_ble\_gap\_rd\_rssi\_evt\_t

struct st_ble_gap_rd_rssi_evt_t		
This structure notifies that RSSI has been retrieved by <a href="#">R_BLE_GAP_ReadRssi()</a> .		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the link whose RSSI was retrieved.
int8_t	rssi	RSSI(in dBm).  Valid range is $-127 < rssi < 20$ and 127. If this field is 127, it indicates that RSSI could not be retrieved.

#### ◆ st\_ble\_gap\_dev\_info\_evt\_t

struct st_ble_gap_dev_info_evt_t		

This structure notifies that information about remote device has been retrieved by [R\\_BLE\\_GAP\\_GetRemDevInfo\(\)](#).

Data Fields												
uint16_t	conn_hdl	Connection handle identifying the remote device whose information has been retrieved.										
uint8_t	get_status	Information about the remote device. This field is a bitwise OR of the following values. <table border="1"> <thead> <tr> <th>Bit Number</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>bit0</td> <td>Address</td> </tr> <tr> <td>bit1</td> <td>Version, company_id, subversion</td> </tr> <tr> <td>bit2</td> <td>Feature</td> </tr> <tr> <td>All other bits</td> <td>Reserved for future use</td> </tr> </tbody> </table>	Bit Number	description	bit0	Address	bit1	Version, company_id, subversion	bit2	Feature	All other bits	Reserved for future use
Bit Number	description											
bit0	Address											
bit1	Version, company_id, subversion											
bit2	Feature											
All other bits	Reserved for future use											
<a href="#">st_ble_dev_addr_t</a>	addr	Address of the remote device.										
uint8_t	version	The version of Link Layer of the remote device.  Refer to Bluetooth SIG Assigned Number ( <a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a> ) regarding defined number.										
uint16_t	company_id	The manufacturer ID of the remote device.  Refer to Bluetooth SIG Assigned Number ( <a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a> ) regarding defined number.										
uint16_t	subversion	The subversion of Link Layer.										
uint8_t	features[ <a href="#">BLE_GAP_REM_FEATURE_SIZE</a> ]	LE feature supported in the remote device.  Refer to Core Spec Vol 6, Part B 4.6 FEATURE SUPPORT.										

#### ◆ [st\\_ble\\_gap\\_conn\\_upd\\_evt\\_t](#)

```
struct st_ble_gap_conn_upd_evt_t
```

This structure notifies that connection parameters has been updated.

Data Fields		
uint16_t	conn_hdl	Connection handle identifying the connection whose parameters has been updated.
uint16_t	conn_intv	Updated Connection Interval. Valid range is 0x0006 - 0x0C80. Time(ms) = conn_intv * 1.25.
uint16_t	conn_latency	Updated slave latency. Valid range is 0x0000 - 0x01F3.
uint16_t	sup_to	Updated supervision timeout. Valid range is 0x000A - 0x0C80. Time(ms) = sup_to * 10.

#### ◆ st\_ble\_gap\_conn\_upd\_req\_evt\_t

```
struct st_ble_gap_conn_upd_req_evt_t
```

This structure notifies that a request for connection parameters update has been received.

Data Fields		
uint16_t	conn_hdl	Connection handle identifying the link that was requested to update connection parameters.
uint16_t	conn_intv_min	Minimum connection interval. Valid range is 0x0006 - 0x0C80. Time(ms) = conn_intv_min * 1.25.
uint16_t	conn_intv_max	Maximum connection interval. Valid range is 0x0006 - 0x0C80. Time(ms) = conn_intv_max * 1.25.
uint16_t	conn_latency	Slave latency. Valid range is 0x0000 - 0x01F3.
uint16_t	sup_to	Supervision timeout. Valid range is 0x000A - 0x0C80. Time(ms) = sup_to * 10

#### ◆ st\_ble\_gap\_conn\_hdl\_evt\_t

```
struct st_ble_gap_conn_hdl_evt_t
```

This structure notifies that a GAP Event that includes only connection handle has occurred.

Data Fields

uint16_t	conn_hdl	Connection handle.
----------	----------	--------------------

◆ **st\_ble\_gap\_data\_len\_chg\_evt\_t**

struct st\_ble\_gap\_data\_len\_chg\_evt\_t

This structure notifies that the packet data length has been updated.

Data Fields

uint16_t	conn_hdl	Connection handle identifying the link that updated Data Length.
uint16_t	tx_octets	Updated transmission packet size(in bytes). Valid range is 0x001B - 0x00FB.
uint16_t	tx_time	Updated transmission time(us). Valid range is 0x0148 - 0x4290.
uint16_t	rx_octets	Updated receive packet size(in bytes). Valid range is 0x001B - 0x00FB.
uint16_t	rx_time	Updated receive time(us). Valid range is 0x0148 - 0x4290.

◆ **st\_ble\_gap\_rd\_rpa\_evt\_t**

struct st\_ble\_gap\_rd\_rpa\_evt\_t

This structure notifies that the local resolvable private address has been retrieved by [R\\_BLE\\_GAP\\_ReadRpa\(\)](#).

Data Fields

<a href="#">st_ble_dev_addr_t</a>	addr	The resolvable private address of local device.
-----------------------------------	------	---

◆ **st\_ble\_gap\_phy\_upd\_evt\_t**

struct st\_ble\_gap\_phy\_upd\_evt\_t

This structure notifies that PHY for a connection has been updated.

Data Fields

uint16_t	conn_hdl	Connection handle identifying
----------	----------	-------------------------------

		the link that has been updated.								
uint8_t	tx_phy	Transmitter PHY. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The transmitter PHY has been updated to 1M PHY.</td> </tr> <tr> <td>0x02</td> <td>The transmitter PHY has been updated to 2M PHY.</td> </tr> <tr> <td>0x03</td> <td>The transmitter PHY has been updated to Coded PHY.</td> </tr> </tbody> </table>	value	description	0x01	The transmitter PHY has been updated to 1M PHY.	0x02	The transmitter PHY has been updated to 2M PHY.	0x03	The transmitter PHY has been updated to Coded PHY.
value	description									
0x01	The transmitter PHY has been updated to 1M PHY.									
0x02	The transmitter PHY has been updated to 2M PHY.									
0x03	The transmitter PHY has been updated to Coded PHY.									
uint8_t	rx_phy	Receiver PHY. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The receiver PHY has been updated to 1M PHY.</td> </tr> <tr> <td>0x02</td> <td>The receiver PHY has been updated to 2M PHY.</td> </tr> <tr> <td>0x03</td> <td>The receiver PHY has been updated to Coded PHY.</td> </tr> </tbody> </table>	value	description	0x01	The receiver PHY has been updated to 1M PHY.	0x02	The receiver PHY has been updated to 2M PHY.	0x03	The receiver PHY has been updated to Coded PHY.
value	description									
0x01	The receiver PHY has been updated to 1M PHY.									
0x02	The receiver PHY has been updated to 2M PHY.									
0x03	The receiver PHY has been updated to Coded PHY.									

#### ◆ st\_ble\_gap\_phy\_rd\_evt\_t

struct st_ble_gap_phy_rd_evt_t						
This structure notifies that the PHY settings has been retrieved by <a href="#">R_BLE_GAP_ReadPhy()</a> .						
Data Fields						
uint16_t	conn_hdl	Connection handle identifying the link that has been retrieved the PHY settings.				
uint8_t	tx_phy	Transmitter PHY. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The transmitter</td> </tr> </tbody> </table>	value	description	0x01	The transmitter
value	description					
0x01	The transmitter					

		<p>0x02 The transmitter PHY has been updated to 1M PHY.</p> <p>0x03 The transmitter PHY has been updated to Coded PHY.</p>								
uint8_t	rx_phy	<p>Receiver PHY.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>The receiver PHY has been updated to 1M PHY.</td> </tr> <tr> <td>0x02</td> <td>The receiver PHY has been updated to 2M PHY.</td> </tr> <tr> <td>0x03</td> <td>The receiver PHY has been updated to Coded PHY.</td> </tr> </tbody> </table>	value	description	0x01	The receiver PHY has been updated to 1M PHY.	0x02	The receiver PHY has been updated to 2M PHY.	0x03	The receiver PHY has been updated to Coded PHY.
value	description									
0x01	The receiver PHY has been updated to 1M PHY.									
0x02	The receiver PHY has been updated to 2M PHY.									
0x03	The receiver PHY has been updated to Coded PHY.									

◆ **st\_ble\_gap\_scan\_req\_rcv\_evt\_t**

struct st_ble_gap_scan_req_rcv_evt_t										
This structure notifies that a Scan Request packet has been received from a Scanner.										
Data Fields										
uint8_t	adv_hdl	Advertising handle identifying the advertising set that has received the Scan Request.								
uint8_t	scanner_addr_type	<p>Address type of the Scanner.</p> <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Public Address.</td> </tr> <tr> <td>0x01</td> <td>Random Address.</td> </tr> <tr> <td>0x02</td> <td>Public Identity Address which could be resolved in</td> </tr> </tbody> </table>	value	description	0x00	Public Address.	0x01	Random Address.	0x02	Public Identity Address which could be resolved in
value	description									
0x00	Public Address.									
0x01	Random Address.									
0x02	Public Identity Address which could be resolved in									

		0x03	Controller. Random Identity Address which could be resolved in Controller.
uint8_t	scanner_addr[ BLE_BD_ADDR_LEN]	Address of the Scanner.  <i>Note</i> The BD address setting format is little endian.	

## ◆ st\_ble\_gap\_sync\_est\_evt\_t

struct st_ble_gap_sync_est_evt_t												
This structure notifies that a Periodic sync has been established.												
Data Fields												
uint16_t	sync_hdl	Sync handle identifying the Periodic Sync that has been established.										
uint8_t	adv_sid	Advertising SID identifying the advertising set that has established the Periodic Sync.										
uint8_t	adv_addr_type	Address type of the advertiser. <table border="1" style="width: 100%;"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Public Address.</td> </tr> <tr> <td>0x01</td> <td>Random Address.</td> </tr> <tr> <td>0x02</td> <td>Public Identity Address which could be resolved in Controller.</td> </tr> <tr> <td>0x03</td> <td>Random Identity Address which could be resolved in Controller.</td> </tr> </tbody> </table>	value	description	0x00	Public Address.	0x01	Random Address.	0x02	Public Identity Address which could be resolved in Controller.	0x03	Random Identity Address which could be resolved in Controller.
value	description											
0x00	Public Address.											
0x01	Random Address.											
0x02	Public Identity Address which could be resolved in Controller.											
0x03	Random Identity Address which could be resolved in Controller.											
uint8_t *	p_adv_addr	Address of the advertiser.  <i>Note</i> The BD address setting format is little endian.										

uint8_t	adv_phy	Advertising PHY.	
		value	description
		0x01	Advertiser PHY is 1M PHY.
		0x02	Advertiser PHY is 2M PHY.
	0x03	Advertiser PHY is Coded PHY.	
uint16_t	perd_adv_intv	Periodic Advertising Interval. Valid range is 0x0006 - 0xFFFF. Time(ms) = perd_adv_intv * 1.25.	
uint8_t	adv_clk_acc	Advertiser Clock Accuracy.	
		value	description
		0x00	500ppm
		0x01	250ppm
		0x02	150ppm
		0x03	100ppm
		0x04	75ppm
		0x05	50ppm
		0x06	30ppm
	0x07	20ppm	

◆ **st\_ble\_gap\_sync\_hdl\_evt\_t**

struct st_ble_gap_sync_hdl_evt_t		
This structure notifies that a GAP Event that includes only sync handle has occurred.		
Data Fields		
uint16_t	sync_hdl	Sync handle.

◆ **st\_ble\_gap\_white\_list\_conf\_evt\_t**

struct st_ble_gap_white_list_conf_evt_t		
This structure notifies that White List has been configured.		
Data Fields		
uint8_t	op_code	The operation for White List.
		value      description

		0x01	A device was added to White List.
		0x02	A device was deleted from White List.
		0x03	White List was cleared.
uint8_t	num	The number of devices which have been added to or deleted from White List.	

#### ◆ st\_ble\_gap\_rslv\_list\_conf\_evt\_t

struct st_ble_gap_rslv_list_conf_evt_t			
This structure notifies that Resolving List has been configured.			
Data Fields			
uint8_t	op_code	The operation for Resolving List.	
		value	description
		0x01	A device was added to Resolving List.
		0x02	A device was deleted from Resolving List.
		0x03	Resolving List was cleared.
uint8_t	num	The number of devices which have been added to or deleted from Resolving List.	

#### ◆ st\_ble\_gap\_perd\_list\_conf\_evt\_t

struct st_ble_gap_perd_list_conf_evt_t			
This structure notifies that Periodic Advertiser List has been configured.			
Data Fields			
uint8_t	op_code	The operation for Periodic Advertiser List.	
		value	description
		0x01	A device was added to Periodic Advertiser List.

		0x02	A device was deleted from Periodic Advertiser List.
		0x03	Periodic Advertiser List was cleared.
uint8_t	num	The number of devices which have been added to or deleted from Periodic Advertiser List.	

#### ◆ st\_ble\_gap\_set\_priv\_mode\_evt\_t

struct st_ble_gap_set_priv_mode_evt_t			
This structure notifies that Privacy Mode has been configured.			
Data Fields			
uint8_t	num	The number of devices which have been set privacy mode.	

#### ◆ st\_ble\_gap\_pairing\_req\_evt\_t

struct st_ble_gap_pairing_req_evt_t			
This structure notifies that a pairing request from a remote device has been received.			
Data Fields			
uint16_t	conn_hdl	Connection handle identifying the remote device that sent the pairing request.	
st_ble_dev_addr_t	bd_addr	The address of the remote device.	
st_ble_gap_auth_info_t	auth_info	The Pairing parameters of the remote device.	

#### ◆ st\_ble\_gap\_passkey\_display\_evt\_t

struct st_ble_gap_passkey_display_evt_t			
This structure notifies that a request for Passkey display in pairing has been received.			
Data Fields			
uint16_t	conn_hdl	Connection handle identifying the remote device that requested Passkey display.	
uint32_t	passkey	Passkey. This field is a 6 digit decimal number(000000-999999).	

#### ◆ st\_ble\_gap\_num\_comp\_evt\_t

struct st_ble_gap_num_comp_evt_t		
This structure notifies that a request for Numeric Comparison in pairing has been received.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the remote device that requested Numeric Comparison.
uint32_t	numeric	The number to be confirmed in Numeric Comparison.  This field is a 6 digit decimal number(000000-999999).

#### ◆ st\_ble\_gap\_key\_press\_ntf\_evt\_t

struct st_ble_gap_key_press_ntf_evt_t														
This structure notifies that the remote device has input a key in Passkey Entry.														
Data Fields														
uint16_t	conn_hdl	Connection handle identifying the remote device that input a key.												
uint8_t	key_type	Type of the key that the remote device input. <table border="1" data-bbox="1034 1137 1471 1624"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Passkey entry started.</td> </tr> <tr> <td>0x01</td> <td>Passkey digit entered.</td> </tr> <tr> <td>0x02</td> <td>Passkey digit erased.</td> </tr> <tr> <td>0x03</td> <td>Passkey cleared.</td> </tr> <tr> <td>0x04</td> <td>Passkey entry completed.</td> </tr> </tbody> </table>	value	description	0x00	Passkey entry started.	0x01	Passkey digit entered.	0x02	Passkey digit erased.	0x03	Passkey cleared.	0x04	Passkey entry completed.
value	description													
0x00	Passkey entry started.													
0x01	Passkey digit entered.													
0x02	Passkey digit erased.													
0x03	Passkey cleared.													
0x04	Passkey entry completed.													

#### ◆ st\_ble\_gap\_pairing\_info\_evt\_t

struct st_ble_gap_pairing_info_evt_t		
This structure notifies that the pairing has completed.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the remote device that the pairing has been done with.
st_ble_dev_addr_t	bd_addr	Address of the remote device.

<a href="#">st_ble_gap_auth_info_t</a>	auth_info	Key information exchanged in pairing.  If local device supports bonding, store the information in non-volatile memory in order to set it to host stack after power re-supply.
--	-----------	---

#### ◆ st\_ble\_gap\_enc\_chg\_evt\_t

struct st_ble_gap_enc_chg_evt_t										
This structure notifies that the encryption status of a link has been changed.										
Data Fields										
uint16_t	conn_hdl	Connection handle identifying the link that has been changed.								
uint8_t	enc_status	Encryption Status. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">value</th> <th style="width: 70%;">description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Encryption OFF.</td> </tr> <tr> <td>0x01</td> <td>Encryption ON.</td> </tr> <tr> <td>0x03</td> <td>Encryption updated by Encryption Key Refresh Completed.</td> </tr> </tbody> </table>	value	description	0x00	Encryption OFF.	0x01	Encryption ON.	0x03	Encryption updated by Encryption Key Refresh Completed.
value	description									
0x00	Encryption OFF.									
0x01	Encryption ON.									
0x03	Encryption updated by Encryption Key Refresh Completed.									

#### ◆ st\_ble\_gap\_peer\_key\_info\_evt\_t

struct st_ble_gap_peer_key_info_evt_t		
This structure notifies that the remote device has distributed the keys.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the remote device that has distributed the keys.
<a href="#">st_ble_dev_addr_t</a>	bd_addr	Address of the remote device.
<a href="#">st_ble_gap_key_ex_param_t</a>	key_ex_param	Distributed keys.  If local device supports bonding, store the keys in non-volatile memory and at power re-supply set to the host stack by <a href="#">R_BLE_GAP_SetBondInfo()</a> .

#### ◆ st\_ble\_gap\_ltk\_req\_evt\_t

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struct st_ble_gap_ltk_req_evt_t		
This structure notifies that a LTK request from a remote device has been received.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the remote device which requests for the LTK.
uint16_t	ediv	Ediv.
uint8_t *	p_peer_rand	Rand.

#### ◆ st\_ble\_gap\_ltk\_rsp\_evt\_t

struct st_ble_gap_ltk_rsp_evt_t								
This structure notifies that local device has replied to the LTK request from the remote device.								
Data Fields								
uint16_t	conn_hdl	Connection handle identifying the remote device to be sent the response to the LTK request.						
uint8_t	response	The response to the LTK request. <table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Local device replied with the stored LTK.</td> </tr> <tr> <td>0x01</td> <td>Local device rejected the LTK request, because the LTK was not found.</td> </tr> </tbody> </table>	value	description	0x00	Local device replied with the stored LTK.	0x01	Local device rejected the LTK request, because the LTK was not found.
value	description							
0x00	Local device replied with the stored LTK.							
0x01	Local device rejected the LTK request, because the LTK was not found.							

#### ◆ st\_ble\_gap\_sc\_oob\_data\_evt\_t

struct st_ble_gap_sc_oob_data_evt_t		
This structure notifies that OOB data for Secure Connections has been generated by <a href="#">R_BLE_GAP_CreateScOobData()</a> .		
Data Fields		
uint8_t *	p_sc_oob_conf	Confirmation value(16 bytes) of OOB Data.
uint8_t *	p_sc_oob_rand	Rand(16bytes) of OOB Data.

#### ◆ st\_ble\_gap\_bond\_info\_t

struct st_ble_gap_bond_info_t		

Bonding information used in `R_BLE_GAP_SetBondInfo()`.

Data Fields		
<code>st_ble_dev_addr_t *</code>	<code>p_addr</code>	Address of the device which exchanged the keys.
<code>st_ble_gap_auth_info_t *</code>	<code>p_auth_info</code>	Information about the keys.
<code>st_ble_gap_key_ex_param_t *</code>	<code>p_keys</code>	Keys distributed from the remote device in pairing.

## Macro Definition Documentation

### ◆ BLE\_BD\_ADDR\_LEN

```
#define BLE_BD_ADDR_LEN
```

Bluetooth Device Address Size

### ◆ BLE\_MASTER

```
#define BLE_MASTER
```

Master Role.

### ◆ BLE\_SLAVE

```
#define BLE_SLAVE
```

Slave Role.

### ◆ BLE\_GAP\_ADDR\_PUBLIC

```
#define BLE_GAP_ADDR_PUBLIC
```

Public Address.

### ◆ BLE\_GAP\_ADDR\_RAND

```
#define BLE_GAP_ADDR_RAND
```

Random Address.

**◆ BLE\_GAP\_ADDR\_RPA\_ID\_PUBLIC**

```
#define BLE_GAP_ADDR_RPA_ID_PUBLIC
```

Resolvable Private Address.

If the IRK of local device has not been registered in Resolving List, public address is used.

**◆ BLE\_GAP\_ADDR\_RPA\_ID\_RANDOM**

```
#define BLE_GAP_ADDR_RPA_ID_RANDOM
```

Resolvable Private Address.

If the IRK of local device has not been registered in Resolving List, random address is used.

**◆ BLE\_GAP\_SCAN\_ALLOW\_ADV\_EXCEPT\_DIRECTED\_WLST**

```
#define BLE_GAP_SCAN_ALLOW_ADV_EXCEPT_DIRECTED_WLST
```

Accept all advertising and scan response PDUs.

The following are excluded.

- Advertising and scan response PDUs where the advertiser's identity address is not in the White List.
- Directed advertising PDUs whose the target address is identity address but doesn't address local device. However directed advertising PDUs whose the target address is the local resolvable private address are accepted.

**◆ BLE\_GAP\_IOCAP\_DISPLAY\_ONLY**

```
#define BLE_GAP_IOCAP_DISPLAY_ONLY
```

Display Only iocapability.

Output function : Local device has the ability to display a 6 digit decimal number.

Input function : None

**◆ BLE\_GAP\_IOCAP\_DISPLAY\_YESNO**

```
#define BLE_GAP_IOCAP_DISPLAY_YESNO
```

Display Yes/No iocapability.

Output function : Output function : Local device has the ability to display a 6 digit decimal number.

Input function : Local device has the ability to indicate 'yes' or 'no'

◆ **BLE\_GAP\_IOCAP\_KEYBOARD\_ONLY**

#define BLE\_GAP\_IOCAP\_KEYBOARD\_ONLY

Keyboard Only iocapability.

Output function : None

Input function : Local device has the ability to input the number '0' - '9'.

◆ **BLE\_GAP\_IOCAP\_NOINPUT\_NOOUTPUT**

#define BLE\_GAP\_IOCAP\_NOINPUT\_NOOUTPUT

No Input No Output iocapability.

Output function : None

Input function : None

◆ **BLE\_GAP\_IOCAP\_KEYBOARD\_DISPLAY**

#define BLE\_GAP\_IOCAP\_KEYBOARD\_DISPLAY

Keyboard Display iocapability.

Output function : Output function : Local device has the ability to display a 6 digit decimal number.

Input function : Local device has the ability to input the number '0' - '9'.

**Typedef Documentation**◆ **ble\_gap\_app\_cb\_t**

ble\_gap\_app\_cb\_t

ble\_gap\_app\_cb\_t is the GAP Event callback function type.

**Parameters**

[in]	event_type	The type of GAP Event.
[in]	event_result	The result of API call which generates the GAP Event.
[in]	p_event_data	Data notified in the GAP Event.

**Returns**

none

◆ **ble\_gap\_del\_bond\_cb\_t**

`ble_gap_del_bond_cb_t`

`ble_gap_del_bond_cb_t` is the type of the callback function for delete bonding information stored in non-volatile area.

This type is used in [R\\_BLE\\_GAP\\_DeleteBondInfo\(\)](#).

**Parameters**

<code>[in]</code>	<code>p_addr</code>	The parameter returns the address of the remote device whose keys are deleted by <a href="#">R_BLE_GAP_DeleteBondInfo()</a> . If <a href="#">R_BLE_GAP_DeleteBondInfo()</a> deletes the keys of all remote devices, the parameter returns NULL.
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**Returns**

none

◆ **st\_ble\_gap\_adv\_param\_t**

`typedef st_ble_gap_ext_adv_param_t st_ble_gap_adv_param_t`

Advertising parameters.

**See also**

[st\\_ble\\_gap\\_ext\\_adv\\_param\\_t](#)

◆ **st\_ble\_gap\_scan\_param\_t**

`typedef st_ble_gap_ext_scan_param_t st_ble_gap_scan_param_t`

Scan parameters.

**See also**

[st\\_ble\\_gap\\_ext\\_scan\\_param\\_t](#)

**Enumeration Type Documentation**

## ◆ e\_ble\_gap\_evt\_t

enum e_ble_gap_evt_t	
GAP Event Identifier.	
Enumerator	
BLE_GAP_EVENT_INVALID	<p>Invalid GAP Event.</p> <p><b>Event Code: 0x1001</b></p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_STACK_ON	<p>Host Stack has been initialized.</p> <p>When initializing host stack by <a href="#">R_BLE_GAP_Init()</a> has been completed, BLE_GAP_EVENT_STACK_ON event is notified.</p> <p><b>Event Code: 0x1002</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_STACK_OFF	<p>Host Stack has been terminated.</p> <p>When terminating host stack by <a href="#">R_BLE_GAP_Terminate()</a> has been completed, BLE_GAP_EVENT_STACK_OFF event is notified.</p> <p><b>Event Code: 0x1003</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p>BLE_ERR_INVALID_STATE(0x0008) When function was called, host stack has not yet been initialized.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_LOC_VER_INFO	<p>Version information of local device.</p>

	<p>When version information of local device has been retrieved by <a href="#">R_BLE_GAP_GetVerInfo()</a>, <a href="#">BLE_GAP_EVENT_LOC_VER_INFO</a> event is notified.</p> <p><b>Event Code: 0x1004</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_loc_dev_info_evt_t</a></p>
BLE_GAP_EVENT_HW_ERR	<p>Hardware Error.</p> <p>When hardware error has been received from Controller, <a href="#">BLE_GAP_EVENT_HW_ERR</a> event is notified.</p> <p><b>Event Code: 0x1005</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_hw_err_evt_t</a></p>
BLE_GAP_EVENT_CMD_ERR	<p>Command Status Error.</p> <p>When the error of HCI Command has occurred after a <a href="#">R_BLE_GAP</a> API call, <a href="#">BLE_GAP_EVENT_CMD_ERR</a> event is notified.</p> <p><b>Event Code: 0x1101</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_cmd_err_evt_t</a></p>
BLE_GAP_EVENT_ADV_REPT_IND	<p>Advertising Report.</p> <p>When advertising PDUs has been received after scanning was started by <a href="#">R_BLE_GAP_StartScan()</a>.</p>

	<p><b>Event Code: 0x1102</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_rept_evt_t</a></p>
BLE_GAP_EVENT_ADV_PARAM_SET_COMP	<p>Advertising parameters have been set.</p> <p>Advertising parameters have been configured by <a href="#">R_BLE_GAP_SetAdvParam()</a>.</p> <p><b>Event Code: 0x1103</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The advertising type that doesn't support advertising data/scan response data was specified to the advertising set which has already set advertising data/scan response data.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) The reason for this error is as follows.</p> <ul style="list-style-type: none"> <li>• Advertising parameters were configured to the advertising set in advertising .</li> <li>• The sec_adv_phy field in adv_param was not</li> </ul>

	<p>specified when Periodic Advertising was started.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_set_evt_t</a></p>
<p>BLE_GAP_EVENT_ADV_DATA_UPD_COMP</p>	<p>Advertising data has been set.</p> <p>This event notifies that Advertising Data/Scan Response Data/Periodic Advertising Data has been set to the advertising set by <a href="#">R_BLE_GAP_SetAdvSresData()</a>.</p> <p><b>Event Code: 0x1104</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) The reason for this error is as follows.</p> <ul style="list-style-type: none"> <li>• The advertising set that doesn't support advertising data/scan response data was set to the data.</li> <li>• The advertising set that supports legacy advertising was set to advertising data/scan response data larger than 31 bytes.</li> </ul>

	<ul style="list-style-type: none"> <li>• The advertising set that has advertising data/scan response data greater than or equal to 252 bytes was set the data in advertising .</li> <li>• The advertising set that has periodic advertising data greater than or equal to 253 bytes was set the data in advertising .</li> </ul> <p>BLE_ERR_MEM_ALL OC_FAILED(0x000C) Length exceeded the length that the advertising set could be set.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_SetAdvSresData()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_data_evt_t</a></p>
<p>BLE_GAP_EVENT_ADV_ON</p>	<p>Advertising has started.</p> <p>When advertising has been started by <a href="#">R_BLE_GAP_StartAdv()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1105</b></p>

**result:**

BLE\_SUCCESS(0x0000) Success

BLE\_ERR\_INVALID\_ARG(0x0003) The reason for this error is as follows.

- The advertising data length set to the advertising set for connectable extended advertising was invalid.
- If `o_addr_type` field in `adv_param` used in [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#) is 0x03, the address which is set in `o_addr` field of `adv_param` has not been registered in Resolving List.

BLE\_ERR\_INVALID\_OPERATION(0x0009) Setting of advertising data/scan response data has not been completed.

BLE\_ERR\_INVALID\_HDL(0x000E) The advertising set specified by [R\\_BLE\\_GAP\\_StartAdv\(\)](#) has not been created.

	<p>BLE_ERR_LIMIT_EXCEEDED(0x0010) When the maximum connections are established, a new connectable advertising tried starting.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_set_evt_t</a></p>
BLE_GAP_EVENT_ADV_OFF	<p>Advertising has stopped.</p> <p>This event notifies the application layer that advertising has stopped.</p> <p><b>Event Code: 0x1106</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_StopAdv()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_off_evt_t</a></p>
BLE_GAP_EVENT_PERD_ADV_PARAM_SET_COMP	<p>Periodic advertising parameters have been set.</p> <p>This event notifies the application layer that Periodic Advertising Parameters has been configured by <a href="#">R_BLE_GAP_SetPerdAdvParam()</a>.</p> <p><b>Event Code: 0x1107</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The advertising set was the setting for anonymous advertising.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) The advertising set was configured to the parameters in</p>

	<p>periodic advertising.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_SetPerdAdvParam()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_set_evt_t</a></p>
BLE_GAP_EVENT_PERD_ADV_ON	<p>Periodic advertising has started.</p> <p>When Periodic Advertising has been started by <a href="#">R_BLE_GAP_StartPerdAdv()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1108</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) The periodic advertising data set in the advertising set has not been completed.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_StartPerdAdv()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_set_evt_t</a></p>
BLE_GAP_EVENT_PERD_ADV_OFF	<p>Periodic advertising has stopped.</p> <p>When Periodic Advertising has terminated by <a href="#">R_BLE_GAP_StopPerdAdv()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1109</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p>

	<p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_StopPerdAdv()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_adv_set_evt_t</a></p>
BLE_GAP_EVENT_ADV_SET_REMOVE_COMP	<p>Advertising set has been deleted.</p> <p>When the advertising set has been removed by <a href="#">R_BLE_GAP_RemoveAdvSet()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x110A</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When the advertising set was in advertising, <a href="#">R_BLE_GAP_RemoveAdvSet()</a> was called.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The advertising set specified by <a href="#">R_BLE_GAP_RemoveAdvSet()</a> has not been created.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_rem_adv_set_evt_t</a></p>
BLE_GAP_EVENT_SCAN_ON	<p>Scanning has started.</p> <p>When scanning has started by <a href="#">R_BLE_GAP_StartScan()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x110B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The reason for this error is as follows:</p>

	<ul style="list-style-type: none"> <li>• Scan interval or scan window was invalid.</li> <li>• When filter_dup field in scan_enable was <a href="#">BLE_GAP_SCAN_FILTER_DUPLICATION_ENABLED_FOR_PERIOD(0x02)</a>, period field in scan_enable was 0.</li> <li>• duration field in scan_enable was larger than period in scan_enable.</li> </ul> <p style="text-align: right;">BLE_ERR_INVALID_OPERATION(0x0009) In scanning, <a href="#">R_BLE_GAP_StartScan()</a> was called.</p> <p><b>Event Data:</b> none</p>
<p>BLE_GAP_EVENT_SCAN_OFF</p>	<p>Scanning has stopped.</p> <p>When scanning has been stopped by <a href="#">R_BLE_GAP_StopScan()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x110C</b></p> <p><b>result:</b></p> <p style="text-align: right;">BLE_SUCCESS(0x0000) Success</p> <p><b>Event Data:</b> none</p>
<p>BLE_GAP_EVENT_SCAN_TO</p>	<p>Scanning has stopped, because duration specified by API expired.</p>

	<p>When the scan duration specified by <a href="#">R_BLE_GAP_StartScan()</a> has expired, this event notifies scanning has stopped.</p> <p><b>Event Code: 0x110D</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0000) Success</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_CREATE_CONN_COMP	<p>Connection Request has been sent to Controller.</p> <p>This event notifies a request for a connection has been sent to Controller.</p> <p><b>Event Code: 0x110E</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0000) Success</p> <p style="padding-left: 40px;">BLE_ERR_INVALID_ARG(0x0003) The reason for this error is as follows:</p> <ul style="list-style-type: none"> <li>• Scan interval or scan windows specified by <a href="#">R_BLE_GAP_CreateConn()</a> is invalid.</li> <li>• Although the own_addr_type field in p_param was set to 0x03, random address had not been registered in Resolving</li> </ul>

	<p>List.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) <a href="#">R_BLE_GAP_CreateConn()</a> was called while creating a link by previous <a href="#">R_BLE_GAP_CreateConn()</a> call .</p> <p>BLE_ERR_LIMIT_EXCEEDED(0x0010) When the maximum connections are established, <a href="#">R_BLE_GAP_CreateConn()</a> was called.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_CONN_IND	<p>Link has been established.</p> <p>This event notifies a link has been established.</p> <p><b>Event Code: 0x110F</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The request for a connection has been cancelled by <a href="#">R_BLE_GAP_CancelCreateConn()</a>.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_evt_t</a></p>
BLE_GAP_EVENT_DISCONN_IND	<p>Link has been disconnected.</p> <p>This event notifies a link has been disconnected.</p> <p><b>Event Code: 0x1110</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_disconn_evt_t</a></p>

<p>BLE_GAP_EVENT_CONN_CANCEL_COMP</p>	<p>Connection Cancel Request has been sent to Controller.</p> <p>This event notifies the request for a connection has been cancelled by <a href="#">R_BLE_GAP_CancelCreateConn()</a>.</p> <p><b>Event Code: 0x1111</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When a request for a connection has not been sent to Controller, <a href="#">R_BLE_GAP_CancelCreateConn()</a> was called.</p> <p><b>Event Data:</b></p> <p>none</p>
<p>BLE_GAP_EVENT_WHITE_LIST_CONF_COMP</p>	<p>The White List has been configured.</p> <p>When White List has been configured, this event is notified to the application layer.</p> <p><b>Event Code: 0x1112</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_STATE(0x0008) The add or delete operation was called, before the previous clear operation has been completed.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) While doing advertising or scanning or creating a link with the White List, <a href="#">R_BLE_GAP_ConfWhiteList()</a> was called.</p> <p>BLE_ERR_MEM_ALLOC_FAILED(0x000C) White List has already registered</p>

	<p>C) the maximum number of devices.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_white_list_conf_evt_t</a></p>
BLE_GAP_EVENT_RAND_ADDR_SET_COMP	<p>Random address has been set to Controller.</p> <p>This event notifies Controller has been set the random address by <a href="#">R_BLE_GAP_SetRandAddr()</a>.</p> <p><b>Event Code: 0x1113</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When local device was in legacy advertising, <a href="#">R_BLE_GAP_SetRandAddr()</a> was called.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_CH_MAP_RD_COMP	<p>Channel Map has been retrieved.</p> <p>This event notifies Channel Map has been retrieved by <a href="#">R_BLE_GAP_ReadChMap()</a>.</p> <p><b>Event Code: 0x1114</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The remote device specified by <a href="#">R_BLE_GAP_ReadChMap()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_rd_ch_map_evt_t</a></p>
BLE_GAP_EVENT_CH_MAP_SET_COMP	<p>Channel Map has set.</p> <p>This event notifies Channel Map has been configured by <a href="#">R_BLE_GAP_SetChMap()</a>.</p>

	<p><b>Event Code: 0x1115</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The channel map specified by <a href="#">R_BLE_GAP_SetChMap()</a> was all-zero.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_RSSI_RD_COMP	<p>RSSI has been retrieved.</p> <p>This event notifies RSSI has been retrieved by <a href="#">R_BLE_GAP_ReadRssi()</a>.</p> <p><b>Event Code: 0x1116</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The remote device specified by <a href="#">R_BLE_GAP_ReadRssi()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_rd_rssi_evt_t</a></p>
BLE_GAP_EVENT_GET_REM_DEV_INFO	<p>Information about the remote device has been retrieved.</p> <p>This event notifies information about the remote device has been retrieved by <a href="#">R_BLE_GAP_GetRemDevInfo()</a>.</p> <p><b>Event Code: 0x1117</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_dev_info_evt_t</a></p>

BLE_GAP_EVENT_CONN_PARAM_UPD_COMP	<p>Connection parameters has been configured.</p> <p>This event notifies the connection parameters has been updated.</p> <p><b>Event Code: 0x1118</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_DATA(0x0002) Local device rejected the request for updating connection parameters.</p> <p>BLE_ERR_INVALID_ARG(0x0003) The remote device rejected the connection parameters suggested from local device.</p> <p>BLE_ERR_UNSUPPORTED(0x0007) The remote device doesn't support connection parameters update feature.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_upd_evt_t</a></p>
BLE_GAP_EVENT_CONN_PARAM_UPD_REQ	<p>Local device has received the request for configuration of connection parameters.</p> <p>This event notifies the request for connection parameters update has been received.</p> <p><b>Event Code: 0x1119</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_upd_req_evt_t</a></p>
BLE_GAP_EVENT_AUTH_PL_TO_EXPIRED	<p>Authenticated Payload Timeout.</p> <p>This event notifies Authenticated Payload</p>

	<p>Timeout has occurred.</p> <p><b>Event Code: 0x111A</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_hdl_evt_t</a></p>
BLE_GAP_EVENT_SET_DATA_LEN_COMP	<p>The request for update transmission packet size and transmission time have been sent to Controller.</p> <p>This event notifies a request for updating packet data length and transmission timer has been sent to Controller.</p> <p><b>Event Code: 0x111B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The tx_octets or tx_time parameter specified by <a href="#">R_BLE_GAP_SetDataLen()</a> is invalid.</p> <p>BLE_ERR_UNSUPPORTED(0x0007) The remote device does not support updating packet data length and transmission time.</p> <p>BLE_ERR_INVALID_HDL(0x000E) When <a href="#">R_BLE_GAP_SetDataLen()</a> was called, the connection was not established.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_hdl_evt_t</a></p>
BLE_GAP_EVENT_DATA_LEN_CHG	<p>Transmission packet size and transmission time have been changed.</p> <p>This event notifies packet data length and transmission time have been updated.</p>

	<p><b>Event Code: 0x111C</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_data_len_chg_evt_t</a></p>
BLE_GAP_EVENT_RSLV_LIST_CONF_COMP	<p>The Resolving List has been configured.</p> <p>When Resolving List has been configured by <a href="#">R_BLE_GAP_ConfRslvList()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x111D</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_STATE(0x0008) The add or delete operation was called, before the previous clear operation has been completed.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) While doing advertising or scanning or creating a link with resolvable private address, <a href="#">R_BLE_GAP_ConfRslvList()</a> was called.</p> <p>BLE_ERR_MEM_ALLOC_FAILED(0x000C) Resolving List has already registered the maximum number of devices.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The specified Identity Address was not found in Resolving List.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_rslv_list_conf_evt_t</a></p>
BLE_GAP_EVENT_RPA_EN_COMP	Resolvable private address function has been

	<p>enabled or disabled.</p> <p>When Resolvable Private Address function in Controller has been enabled by <a href="#">R_BLE_GAP_EnableRpa()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x111E</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) While advertising, scanning, or establishing a link with resolvable private address, <a href="#">R_BLE_GAP_EnableRpa()</a> was called.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_SET_RPA_TO_COMP	<p>The update time of resolvable private address has been changed.</p> <p>When Resolvable Private Address Timeout in Controller has been updated by <a href="#">R_BLE_GAP_SetRpaTo()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x111F</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The rpa_timeout parameter specified by <a href="#">R_BLE_GAP_SetRpaTo()</a> is out of range.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_RD_RPA_COMP	<p>The resolvable private address of local device has been retrieved.</p> <p>When the resolvable private address of local</p>

	<p>device has been retrieved by <a href="#">R_BLE_GAP_ReadRpa()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1120</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The identity address specified by <a href="#">R_BLE_GAP_ReadRpa()</a> was not registered in Resolving List.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_rd_rpa_evt_t</a></p>
BLE_GAP_EVENT_PHY_UPD	<p>PHY for connection has been changed.</p> <p>This event notifies the application layer that PHY for a connection has been updated.</p> <p><b>Event Code: 0x1121</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_phy_upd_evt_t</a></p>
BLE_GAP_EVENT_PHY_SET_COMP	<p>The request for updating PHY for connection has been sent to Controller.</p> <p>When Controller has received a request for updating PHY for a connection by <a href="#">R_BLE_GAP_SetPhy()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1122</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_HDL(0x000E) The remote device specified by</p>

	<p><a href="#">R_BLE_GAP_SetPhy()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_hdl_evt_t</a></p>
BLE_GAP_EVENT_DEF_PHY_SET_COMP	<p>The request for setting default PHY has been sent to Controller.</p> <p>When the PHY preferences which a remote device may change has been configured by <a href="#">R_BLE_GAP_SetDefPhy()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1123</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_PHY_RD_COMP	<p>PHY configuration has been retrieved.</p> <p>When the PHY settings has been retrieved by <a href="#">R_BLE_GAP_ReadPhy()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x1124</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p>BLE_ERR_INVALID_HDL(0x000E) The link specified by <a href="#">R_BLE_GAP_ReadPhy()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_phy_rd_evt_t</a></p>
BLE_GAP_EVENT_SCAN_REQ_RECV	<p>Scan Request has been received.</p> <p>This event notifies the application layer that a Scan Request packet has been received from a Scanner.</p>

	<p><b>Event Code: 0x1125</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_scan_req_rcv_evt_t</a></p>
BLE_GAP_EVENT_CREATE_SYNC_COMP	<p>The request for establishing a periodic sync has been sent to Controller.</p> <p>This event notifies the application layer that Controller has received a request for a Periodic Sync establishment.</p> <p><b>Event Code: 0x1126</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When <a href="#">R_BLE_GAP_CreateSync()</a> was called, this event for previous the API call has not been received.</p> <p>BLE_ERR_ALREADY_IN_PROGRESS(0x000A) The advertising set specified by <a href="#">R_BLE_GAP_CreateSync()</a> has already established a periodic sync.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_SYNC_EST	<p>The periodic advertising sync has been established.</p> <p>This event notifies the application layer that a Periodic sync has been established.</p> <p><b>Event Code: 0x1127</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p>

	<p>BLE_ERR_NOT_YET_READY(0x0012) The request for a Periodic Sync establishment was cancelled by <a href="#">R_BLE_GAP_CancelCreateSync()</a>.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_sync_est_evt_t</a></p>
BLE_GAP_EVENT_SYNC_TERM	<p>The periodic advertising sync has been terminated.</p> <p>This event notifies the application layer that the Periodic Sync has been terminated by <a href="#">R_BLE_GAP_TerminateSync()</a>.</p> <p><b>Event Code: 0x1128</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) While establishing a Periodic Sync by <a href="#">R_BLE_GAP_CreateSync()</a>, <a href="#">R_BLE_GAP_TerminateSync()</a> was called.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The sync handle specified by <a href="#">R_BLE_GAP_TerminateSync()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_sync_hdl_evt_t</a></p>
BLE_GAP_EVENT_SYNC_LOST	<p>The periodic advertising sync has been lost.</p> <p>This event notifies the application layer that the Periodic Sync has been lost.</p> <p><b>Event Code: 0x1129</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p>

	<p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_sync_hdl_evt_t</a></p>
<p>BLE_GAP_EVENT_SYNC_CREATE_CANCEL_COMP</p>	<p>The request for cancel of establishing a periodic advertising sync has been sent to Controller.</p> <p>This event notifies the request for a Periodic Sync establishment has been cancelled by <a href="#">R_BLE_GAP_CancelCreateSync()</a>.</p> <p><b>Event Code: 0x112A</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When <a href="#">R_BLE_GAP_CancelCreateSync()</a> was called, a request for a Periodic Sync establishment by <a href="#">R_BLE_GAP_CreateSync()</a> has not been sent to Controller.</p> <p><b>Event Data:</b></p> <p>none</p>
<p>BLE_GAP_EVENT_PERD_LIST_CONF_COMP</p>	<p>The Periodic Advertiser list has been configured.</p> <p>When Periodic Advertiser List has been configured by <a href="#">R_BLE_GAP_ConfPerdAdvList()</a>, this event is notified to the application layer.</p> <p><b>Event Code: 0x112B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The advertiser has already been registered in Periodic Advertiser List.</p> <p>BLE_ERR_INVALID_STATE(0x0008) The add or delete operation was</p>

	<p>called, before the previous clear operation has been completed.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) When establishing a periodic sync by <a href="#">R_BLE_GAP_CreateSync()</a>, <a href="#">R_BLE_GAP_ConfPerdAdvList()</a> was called.</p> <p>BLE_ERR_MEM_ALLOC_FAILED(0x000C) Periodic Advertiser List has already registered the maximum number of devices.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The device specified by <a href="#">R_BLE_GAP_ConfPerdAdvList()</a> was not found.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_perd_list_conf_evt_t</a></p>
BLE_GAP_EVENT_PRIV_MODE_SET_COMP	<p>Privacy Mode has been configured.</p> <p>This event notifies the application layer that the Privacy Mode has been configured by <a href="#">R_BLE_GAP_SetPrivMode()</a>.</p> <p><b>Event Code: 0x112B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) Address type or privacy mode is out of range.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009) While advertising, scanning, or establishing a link with resolvable private address, <a href="#">R_BLE_GAP_SetPrivMode()</a> was called.</p> <p>BLE_ERR_INVALID_HDL(0x000E) The address specified by</p>

	<p><a href="#">R_BLE_GAP_SetPriVMode()</a> has not been registered in Resolving List.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_GAP_EVENT_PAIRING_REQ	<p>The pairing request from a remote device has been received.</p> <p>This event notifies the application layer that a pairing request from a remote device has been received.</p> <p><b>Event Code: 0x1401</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_pairing_info_evt_t</a></p>
BLE_GAP_EVENT_PASSKEY_ENTRY_REQ	<p>The request for input passkey has been received.</p> <p>This event notifies that a request for Passkey input in pairing has been received.</p> <p><b>Event Code: 0x1402</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_hdl_evt_t</a></p>
BLE_GAP_EVENT_PASSKEY_DISPLAY_REQ	<p>The request for displaying a passkey has been received.</p> <p>This event notifies that a request for Passkey display in pairing has been received.</p> <p><b>Event Code: 0x1403</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success</p>

	<p>000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_passkey_display_evt_t</a></p>
BLE_GAP_EVENT_NUM_COMP_REQ	<p>The request for confirmation with Numeric Comparison has received.</p> <p>This event notifies that a request for Numeric Comparison in pairing has been received.</p> <p><b>Event Code: 0x1404</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_num_comp_evt_t</a></p>
BLE_GAP_EVENT_KEY_PRESS_NTF	<p>Key Notification from a remote device has been received.</p> <p>This event notifies the application layer that the remote device has input a key in Passkey Entry.</p> <p><b>Event Code: 0x1405</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_key_press_ntf_evt_t</a></p>
BLE_GAP_EVENT_PAIRING_COMP	<p>Pairing has been completed.</p> <p>This event notifies the application layer that the pairing has completed.</p> <p><b>Event Code: 0x1406</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p>BLE_ERR_SMP_LE_PASSKEY_ENTRY_F PassKey Entry is failed.</p>

AIL(0x2001)	
BLE_ERR_SMP_LE_OOB_DATA_NOT_AVAILABLE(0x2002)	OOB Data is not available.
BLE_ERR_SMP_LE_AUTH_REQ_NOT_MET(0x2003)	The requested pairing can not be performed because of IO Capability.
BLE_ERR_SMP_LE_CONFIRM_VAL_NOT_MATCH(0x2004)	Confirmation value does not match.
BLE_ERR_SMP_LE_PAIRING_NOT_SUPPORTED(0x2005)	Pairing is not supported.
BLE_ERR_SMP_LE_INSUFFICIENT_ENCRYPTION_KEY_SIZE(0x2006)	Encryption Key Size is insufficient.
BLE_ERR_SMP_LE_CMD_NOT_SUPPORTED(0x2007)	The pairing command received is not supported.
BLE_ERR_SMP_LE_UNSPECIFIED_REASON(0x2008)	Pairing failed with an unspecified reason.
BLE_ERR_SMP_LE_REPEATED_ATTEMPTS(0x2009)	The number of repetition exceeded the upper limit.
BLE_ERR_SMP_LE_INVALID_PARAM(0x200A)	Invalid parameter is set.
BLE_ERR_SMP_LE_DHKEY_CHECK_FAIL(0x200B)	DHKey Check error.
BLE_ERR_SMP_LE_NUMERIC_COMP_FAIL(0x200C)	Numeric Comparison failure.
BLE_ERR_SMP_LE_DISCONNECTED(0x200F)	Disconnection in pairing.
BLE_ERR_SMP_LE_TIMEOUT(0x2011)	Failure due to timeout.
BLE_ERR_SMP_LE_LOC_KEY_MISSING(0x2014)	Pairing/Encryption failure because local device lost the LTK.

	<p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_pairing_info_evt_t</a></p>
BLE_GAP_EVENT_ENC_CHG	<p>Key Notification from a remote device has been received.</p> <p>This event notifies the application layer that the encryption status of a link has been changed.</p> <p><b>Event Code: 0x1407</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_enc_chg_evt_t</a></p>
BLE_GAP_EVENT_PEER_KEY_INFO	<p>Keys has been received from a remote device.</p> <p>This event notifies the application layer that the remote device has distributed the keys.</p> <p><b>Event Code: 0x1408</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_peer_key_info_evt_t</a></p>
BLE_GAP_EVENT_EX_KEY_REQ	<p>The request for key distribution has been received.</p> <p>When local device has been received a request for key distribution to remote device, this event is notified to the application layer.</p> <p><b>Event Code: 0x1409</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_conn_hdl_evt_t</a></p>

BLE_GAP_EVENT_LTK_REQ	<p>LTK has been request from a remote device.</p> <p>When local device has been received a LTK request from a remote device, this event is notified to the application layer.</p> <p><b>Event Code: 0x140A</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_ltk_req_evt_t</a></p>
BLE_GAP_EVENT_LTK_RSP_COMP	<p>LTK reply has been sent to Controller.</p> <p>When local device has replied to the LTK request from the remote device, this event is notified to the application layer.</p> <p><b>Event Code: 0x140B</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_ltk_rsp_evt_t</a></p>
BLE_GAP_EVENT_SC_OOB_CREATE_COMP	<p>The authentication data to be used in Secure Connections OOB has been created.</p> <p>This event notifies OOB data for Secure Connections has been generated by <a href="#">R_BLE_GAP_CreateScOobData()</a>.</p> <p><b>Event Code: 0x140C</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_gap_sc_oob_data_evt_t</a></p>

## Function Documentation

◆ **R\_BLE\_GAP\_Init()**

```
ble_status_t R_BLE_GAP_Init ( ble_gap_app_cb_t gap_cb)
```

Initialize the Host Stack.

Host stack is initialized with this function. Before using All the R\_BLE APIs, it's necessary to call this function. A callback function is registered with this function. In order to receive the GAP event, it's necessary to register a callback function. The result of this API call is notified in BLE\_GAP\_EVENT\_STACK\_ON event.

**Parameters**

[in]	gap_cb	A callback function registered with this function.
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**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	gap_cb is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• Host Stack was already initialized.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_Terminate()**

```
ble_status_t R_BLE_GAP_Terminate ( void )
```

Terminate the Host Stack.

Host stack is terminated with this function. In order to reset all the Bluetooth functions, it's necessary to call this function. The result of this API call is notified in BLE\_GAP\_EVENT\_STACK\_OFF event.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	Host stack hasn't been initialized.

## ◆ R\_BLE\_GAP\_UpdConn()

```
ble_status_t R_BLE_GAP_UpdConn ( uint16_t conn_hdl, uint8_t mode, uint16_t accept,
st_ble_gap_conn_param_t * p_conn_updt_param )
```

Update the connection parameters.

This function updates the connection parameters or replies a request for updating connection parameters notified by BLE\_GAP\_EVENT\_CONN\_PARAM\_UPD\_REQ event. When the connection parameters has been updated, BLE\_GAP\_EVENT\_CONN\_PARAM\_UPD\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link to be updated.						
[in]	mode	Connection parameter update request or response. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_CONN_UPD_MODE_REQ (0x01)</td> <td>Request for updating the connection parameters.</td> </tr> <tr> <td>BLE_GAP_CONN_UPD_MODE_RSP (0x02)</td> <td>Reply a connection parameter update request.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_CONN_UPD_MODE_REQ (0x01)	Request for updating the connection parameters.	BLE_GAP_CONN_UPD_MODE_RSP (0x02)	Reply a connection parameter update request.
macro	description							
BLE_GAP_CONN_UPD_MODE_REQ (0x01)	Request for updating the connection parameters.							
BLE_GAP_CONN_UPD_MODE_RSP (0x02)	Reply a connection parameter update request.							
[in]	accept	When mode is BLE_GAP_CONN_UPD_MODE_RSP, accept or reject the connection parameters update request. If mode is BLE_GAP_CONN_UPD_MODE_REQ, accept is ignored. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_CONN_UPD_ACCEPT (0x0000)</td> <td>Accept the update request.</td> </tr> <tr> <td>BLE_GAP_CONN_UPD_REJECT (0x0001)</td> <td>Reject the update request.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_CONN_UPD_ACCEPT (0x0000)	Accept the update request.	BLE_GAP_CONN_UPD_REJECT (0x0001)	Reject the update request.
macro	description							
BLE_GAP_CONN_UPD_ACCEPT (0x0000)	Accept the update request.							
BLE_GAP_CONN_UPD_REJECT (0x0001)	Reject the update request.							
[in]	p_conn_updt_param	Connection parameters to be updated. When mode is BLE_GAP_CONN_UPD_MODE_RSP and accept is						

		BLE_GAP_CONN_UPD_REJECT , p_conn_updt_param is ignored.
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**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	When accept is BLE_GAP_CONN_UPD_ACCEPT, p_conn_updt_param is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The following is out of range. <ul style="list-style-type: none"> <li>• mode</li> <li>• accept</li> <li>• conn_intv_min field in p_conn_updt_param</li> <li>• conn_intv_max field in p_conn_updt_param</li> <li>• conn_latency in p_conn_updt_param</li> <li>• sup_to in p_conn_updt_param</li> <li>• conn_hdl</li> </ul>
BLE_ERR_INVALID_STATE(0x0008)	Not connected with the remote device.
BLE_ERR_CONTEXT_FULL(0x000B)	Sending a L2CAP command, an error occurred.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

◆ **R\_BLE\_GAP\_SetDataLen()**

```
ble_status_t R_BLE_GAP_SetDataLen ( uint16_t conn_hdl, uint16_t tx_octets, uint16_t tx_time )
```

Update the packet size and the packet transmit time.

This function requests for changing the maximum transmission packet size and the maximum packet transmission time. When Controller has received the request from host stack, BLE\_GAP\_EVENT\_SET\_DATA\_LEN\_COMP event is notified to the application layer. When the transmission packet size or the transmission time has been changed, BLE\_GAP\_EVENT\_DATA\_LEN\_CHG event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link whose the transmission packet size or the transmission time to be changed.
[in]	tx_octets	Maximum transmission packet size. Valid range is 0x001B - 0x00FB.
[in]	tx_time	Maximum transmission time(us). Valid range is 0x0148 - 0x4290.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_Disconnect()**

```
ble_status_t R_BLE_GAP_Disconnect ( uint16_t conn_hdl, uint8_t reason )
```

Disconnect the link.

This function disconnects a link. When the link has disconnected, BLE\_GAP\_EVENT\_DISCONN\_IND event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link to be disconnected.
[in]	reason	The reason for disconnection. Usually, set 0x13 which indicates that a user disconnects the link. If setting other than 0x13, refer the error code described in Core Specification Vol.2 Part D , "2 Error Code Descriptions".

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	conn_hdl is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

## ◆ R\_BLE\_GAP\_SetPhy()

```
ble_status_t R_BLE_GAP_SetPhy ( uint16_t conn_hdl, st_ble_gap_set_phy_param_t * p_phy_param )
```

Set the phy for connection.

This function sets the PHY preferences for the connection. The result of this API call is notified in BLE\_GAP\_EVENT\_PHY\_SET\_COMP event. When the PHY has been updated, BLE\_GAP\_EVENT\_PHY\_UPD event is notified to the application layer.

After PHY update, the PHY accept configuration of local device is the same as the values in BLE\_GAP\_EVENT\_PHY\_UPD event.

For example, after calling R\_BLE\_GAP\_SetPhy(), if tx\_phy, rx\_phy by BLE\_GAP\_EVENT\_PHY\_UPD event are updated to 2M PHY, the PHY accept configuration is 2M PHY only.

Therefore after receiving BLE\_GAP\_EVENT\_PHY\_UPD event, if local device wants to accept the other PHY configuration, it needs to call R\_BLE\_GAP\_SetPhy() with the desired PHY accept configuration.

Because the maximum transmission packet size or the maximum transmission time might be updated by PHY update, if the same packet size or transmission time as the previous one is desired, change the maximum transmission packet size or the maximum transmission time by R\_BLE\_GAP\_SetDataLen().

### Parameters

[in]	conn_hdl	Connection handle identifying the link whose PHY to be updated.
[in]	p_phy_param	PHY preferences.

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_phy_param is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	conn_hdl or option field in p_phy_param is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

## ◆ R\_BLE\_GAP\_SetDefPhy()

```
ble_status_t R_BLE_GAP_SetDefPhy ( st_ble_gap_set_def_phy_param_t* p_def_phy_param)
```

Set the default phy which allows remote device to change.

This function sets the PHY preferences which a remote device may change. The result of this API call is notified in BLE\_GAP\_EVENT\_DEF\_PHY\_SET\_COMP event.

**Parameters**

[in]	p_def_phy_param	The PHY preference which a remote device may change.
------	-----------------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_def_phy_param is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	tx_phys or tx_phys field in p_def_phy_param is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

## ◆ R\_BLE\_GAP\_SetPrivMode()

```
ble_status_t R_BLE_GAP_SetPrivMode ( st_ble_dev_addr_t* p_addr, uint8_t* p_privacy_mode, uint8_t device_num )
```

Set the privacy mode.

This function sets privacy mode for the remote device registered in Resolving List. By default, Network Privacy Mode is set.

The result of this API call is notified in BLE\_GAP\_EVENT\_PRIV\_MODE\_SET\_COMP event.

**Parameters**

[in]	p_addr	An array of identity address of the remote device to set privacy mode. The number of elements is specified by device_num.
[in]	p_privacy_mode	An array of privacy mode to set to remote device. The number of elements is specified by device_num. The following value is set as

the privacy mode.

macro	description
BLE_GAP_NETWORK_PRIVACY_MODE (0x00)	Network Privacy Mode.
BLE_GAP_DEVICE_PRIVACY_MODE (0x01)	Device Privacy Mode.

[in]	device_num	The number of devices to set privacy mode. Valid range is 1-BLE_GAP_RSLV_LIST_MAX_ENTRY.
------	------------	--

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_addr or p_privacy_mode is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The following parameter is out of range. <ul style="list-style-type: none"> <li>The address type in p_addr.</li> <li>The privacy mode specified by p_privacy_mode.</li> <li>device_num</li> </ul>
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>While configuring privacy mode, this function was called.</li> <li>The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

### ◆ R\_BLE\_GAP\_ConfWhiteList()

```
ble_status_t R_BLE_GAP_ConfWhiteList ( uint8_t op_code, st_ble_dev_addr_t* p_addr, uint8_t device_num )
```

Set White List.

This function supports the following operations regarding White List.

- Add the device to White List.
- Delete the device from White List.
- Clear White List.

The total number of White List entries is defined as BLE\_GAP\_WHITE\_LIST\_MAX\_ENTRY. The result of this API call is notified in BLE\_GAP\_EVENT\_WHITE\_LIST\_CONF\_COMP event.

#### Parameters

[in]	op_code	The operation for White List.								
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_LIST_ADD_D EV(0x01)</td> <td>Add the device to the list.</td> </tr> <tr> <td>BLE_GAP_LIST_REMOVE_D EV(0x02)</td> <td>Delete the device from the list.</td> </tr> <tr> <td>BLE_GAP_LIST_CLEAR(0x03)</td> <td>Clear the list.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_LIST_ADD_D EV(0x01)	Add the device to the list.	BLE_GAP_LIST_REMOVE_D EV(0x02)	Delete the device from the list.	BLE_GAP_LIST_CLEAR(0x03)	Clear the list.
macro	description									
BLE_GAP_LIST_ADD_D EV(0x01)	Add the device to the list.									
BLE_GAP_LIST_REMOVE_D EV(0x02)	Delete the device from the list.									
BLE_GAP_LIST_CLEAR(0x03)	Clear the list.									
[in]	p_addr	An array of device address to add / delete to the list. The number of elements is specified by device_num. If op_code is BLE_GAP_LIST_CLR, p_addr is ignored.								
[in]	device_num	The number of devices add / delete to the list. Valid range is 1-BLE_GAP_WHITE_LIST_MAX_ENTRY. If op_code is BLE_GAP_LIST_CLR, device_num is ignored.								

#### Return values

BLE_SUCCESS(0x0000)	Success
---------------------	---------

BLE_ERR_INVALID_PTR(0x0001)	When op_code is BLE_GAP_LIST_ADD_DEV or BLE_GAP_LIST_REMOVE_DEV, p_addr is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	op_code or address type field in p_addr is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• While operating White List, this function was called.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for operating the White List.

### ◆ R\_BLE\_GAP\_GetVerInfo()

ble\_status\_t R\_BLE\_GAP\_GetVerInfo ( void )

Get the version number of the Controller and the host stack.

This function retrieves the version information of local device. The result of this API call is notified in BLE\_GAP\_EVENT\_LOC\_VER\_INFO event.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_ReadPhy()**

```
ble_status_t R_BLE_GAP_ReadPhy ( uint16_t conn_hdl)
```

Get the phy settings.

This function gets the PHY settings for the connection. The result of this API call is notified in BLE\_GAP\_EVENT\_PHY\_RD\_COMP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link whose PHY settings to be retrieved.
------	----------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	conn_hdl is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_ConfRslvList()**

```
ble_status_t R_BLE_GAP_ConfRslvList ( uint8_t op_code, st_ble_dev_addr_t* p_addr,
st_ble_gap_rslv_list_key_set_t* p_peer_irk, uint8_t device_num )
```

Set Resolving List.

This function supports the following operations regarding Resolving List.

- Add the device to Resolving List.
- Delete the device from Resolving List.
- Clear Resolving List.

In order to generate a resolvable private address, a local IRK needs to be registered by [R\\_BLE\\_GAP\\_SetLocIdInfo\(\)](#). If communicating with the identity address, register all-zero IRK as local IRK. In order to resolve resolvable private address of the remote device, the IRK distributed from the remote device needs to be added to Resolving List. The total number of Resolving List entries is defined as BLE\_GAP\_RESOLV\_LIST\_MAX\_ENTRY. The result of this API call is notified in BLE\_GAP\_EVENT\_RSLV\_LIST\_CONF\_COMP event.

**Parameters**

[in]	op_code	The operation for Resolving List.						
		macro   description						
		<table border="1"> <tr> <td>BLE_GAP_LIST_ADD_DEV(0x01)</td> <td>Add the device to the list.</td> </tr> <tr> <td>BLE_GAP_LIST_REMOVE_DEV(0x02)</td> <td>Delete the device from the list.</td> </tr> <tr> <td>BLE_GAP_LIST_CLEAR(0x03)</td> <td>Clear the list.</td> </tr> </table>	BLE_GAP_LIST_ADD_DEV(0x01)	Add the device to the list.	BLE_GAP_LIST_REMOVE_DEV(0x02)	Delete the device from the list.	BLE_GAP_LIST_CLEAR(0x03)	Clear the list.
BLE_GAP_LIST_ADD_DEV(0x01)	Add the device to the list.							
BLE_GAP_LIST_REMOVE_DEV(0x02)	Delete the device from the list.							
BLE_GAP_LIST_CLEAR(0x03)	Clear the list.							
[in]	p_addr	An array of Identity Addresses to add / delete to the list. The number of elements is specified by device_num. If op_code is BLE_GAP_LIST_CLEAR, p_addr is ignored.						
[in]	p_peer_irk	The remote IRK and the type of local IRK added to Resolving List. If op_code is other than BLE_GAP_LIST_ADD_DEV, p_peer_irk is ignored. The number of elements is						

		specified by device_num.
[in]	device_num	The number of devices add / delete to the list. Valid range is 1-BLE_GAP_RSLV_LIST_MAX_ENTRY. If op_code is BLE_GAP_LIST_CLR, device_num is ignored.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• When added to or deleted from the list, p_addr is specified as NULL.</li> <li>• When added to the list, p_peer_irk is specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• op_code is out of range.</li> <li>• When op_code is BLE_GAP_LIST_ADD_DEV or BLE_GAP_LIST_REM_DEV, device_num is out of range.</li> <li>• When op_code is BLE_GAP_LIST_ADD_DEV or BLE_GAP_LIST_REM_DEV, address type field in p_addr is out of range.</li> </ul>
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• While operating Resolving List, this function was called.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for operating the Resolving List.
BLE_ERR_INVALID_HDL(0x000E)	The specified Identity Address was not found in Resolving List.

## ◆ R\_BLE\_GAP\_EnableRpa()

ble\_status\_t R\_BLE\_GAP\_EnableRpa ( uint8\_t enable)

Enable/Disable address resolution and generation of a resolvable private address.

This function enables or disables RPA functionality. The RPA functionality includes the following.

- Generation of local resolvable private address
- Resolution of remote resolvable private address

In order to do advertising, scanning or creating a link with local resolvable private address, the RPA functionality needs to be enabled. After enabling the RPA functionality and the identity address of remote device and the IRKs of local/remote device is registered, local device can generate own resolvable private address in the time interval set by R\_BLE\_GAP\_SetRpaTo(), and can resolve a resolvable private address of a remote device. It is recommended that the RPA functionality is called immediately after the initialization by R\_BLE\_GAP\_Init(). The result of this API call is notified in BLE\_GAP\_EVENT\_RPA\_EN\_COMP event.

### Parameters

[in]	enable	Enable or disable address resolution function.	
		macro	description
		BLE_GAP_RPA_DISABLED (0x00)	Disable RPA generation/resolution.
		BLE_GAP_RPA_ENABLED (0x01)	Enable RPA generation/resolution.

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	enable is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetRpaTo()**

```
ble_status_t R_BLE_GAP_SetRpaTo ( uint16_t rpa_timeout)
```

Set the update time of resolvable private address.

This function sets the time interval to update the resolvable private address. The result of this API call is notified in BLE\_GAP\_EVENT\_SET\_RPA\_TO\_COMP event.

**Parameters**

[in]	rpa_timeout	Time interval to update resolvable private address in seconds. Valid range is 0x003C - 0xA1B8. Default is 900s.
------	-------------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_ReadRpa()**

```
ble_status_t R_BLE_GAP_ReadRpa ( st_ble_dev_addr_t* p_addr)
```

Get the resolvable private address of local device.

This function retrieves the local resolvable private address. Before getting the address, enable the resolvable private address function by [R\\_BLE\\_GAP\\_EnableRpa\(\)](#). The result of this API call is notified in BLE\_GAP\_EVENT\_RD\_RPA\_COMP event.

**Parameters**

[in]	p_addr	Identity address registered in Resolving List.
------	--------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_addr is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	Address type in p_addr is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows. <ul style="list-style-type: none"> <li>• When retrieving the local resolvable private address, this function was called.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_ReadRssi()**

ble\_status\_t R\_BLE\_GAP\_ReadRssi ( uint16\_t conn\_hdl)

Get RSSI.

This function retrieves RSSI. The result of this API call is notified in BLE\_GAP\_EVENT\_RSSI\_RD\_COMP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link whose RSSI to be retrieved.
------	----------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	conn_hdl is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_ReadChMap()**

ble\_status\_t R\_BLE\_GAP\_ReadChMap ( uint16\_t conn\_hdl)

Get the Channel Map.

This function retrieves the channel map. The result of this API call is notified in BLE\_GAP\_EVENT\_CH\_MAP\_RD\_COMP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link whose channel map to be retrieved.
------	----------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	conn_hdl is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetRandAddr()**

```
ble_status_t R_BLE_GAP_SetRandAddr ( uint8_t* p_random_addr)
```

Set a random address.

This function sets static address or non-resolvable private address to Controller. Refer to Core Specification Vol 6, PartB, "1.3.2 Random Device Address" regarding the format of the random address. Resolvable private address cannot set by this API. The result of this API call is notified in BLE\_GAP\_EVENT\_RAND\_ADDR\_SET\_COMP event.

**Parameters**

[in]	p_random_addr	Static address or non-resolvable private address. The BD address setting format is little endian.
------	---------------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_random_addr is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetAdvParam()**

```
ble_status_t R_BLE_GAP_SetAdvParam ( st_ble_gap_adv_param_t * p_adv_param)
```

Set advertising parameters.

This function sets advertising parameters. It's possible to do advertising where the advertising parameters are different every each advertising set. The number of advertising set in the Controller is defined as BLE\_MAX\_NO\_OF\_ADV\_SETS\_SUPPORTED. Each advertising set is identified with advertising handle (0x00-0x03). Create an advertising set with this function before start advertising, setting periodic advertising parameters, start periodic advertising, setting advertising data/scan response data/periodic advertising data. The result of this API call is notified in BLE\_GAP\_EVENT\_ADV\_PARAM\_SET\_COMP event.

**Parameters**

[in]	p_adv_param	Advertising parameters.
------	-------------	-------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_adv_param is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The below p_adv_param field value is out of range. <ul style="list-style-type: none"> <li>• adv_handle</li> <li>• adv_intv_min/adv_intv_max</li> <li>• adv_ch_map</li> <li>• o_addr_type</li> <li>• p_addr_type</li> <li>• adv_phy</li> <li>• sec_adv_phy</li> <li>• scan_req_ntf_flag</li> </ul>
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetAdvSresData()**

```
ble_status_t R_BLE_GAP_SetAdvSresData ( st_ble_gap_adv_data_t * p_adv_srsp_data)
```

Set advertising data/scan response data/periodic advertising data.

This function sets advertising data/scan response data/periodic advertising data to the advertising set. It is necessary to create an advertising set by [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#), before calling this function. Set advertising data/scan response data/periodic advertising data, after allocating the memory for the data. The following shall be applied regarding the adv\_prop\_type field and the data\_type field in st\_ble\_gap\_adv\_param\_t parameter specified in [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#).

The following shall be applied regarding the adv\_prop\_type field and the data\_type field in st\_ble\_gap\_adv\_param\_t parameter specified in [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#).

- When `adv_prop_type` is Legacy Advertising PDU type,
  - it's possible to set advertising data/scan response data up to 31 bytes.
  - advertising data/scan response data can be updated by this function in advertising.
- When `adv_prop_type` is Extended Advertising PDU type,
  - it's possible to set at most 1650 bytes of data as advertising data/scan response data per 1 advertising set.
  - the total buffer size in Controller for advertising data/scan response data is 4250 bytes. Therefore please note that more than 4250 bytes of advertising data/scan response data can not be set to all the advertising sets. Please refer to Figure 1.1 and Figure 1.2 about examples of setting advertising data/scan response data.
  - it's possible to update advertising data/scan response data in advertising, if the `data_length` field in `st_ble_gap_adv_data_t` parameter is up to 251 bytes.

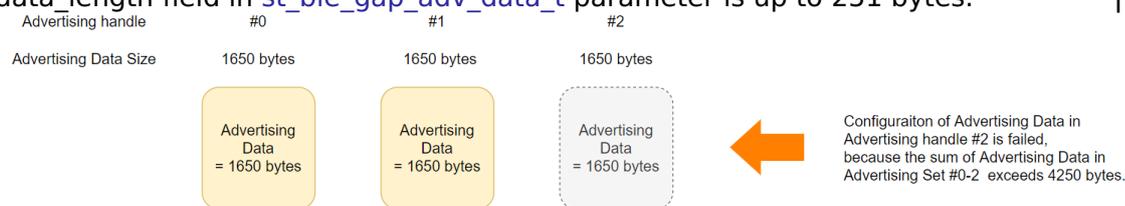


Figure 146: Figure 1.1

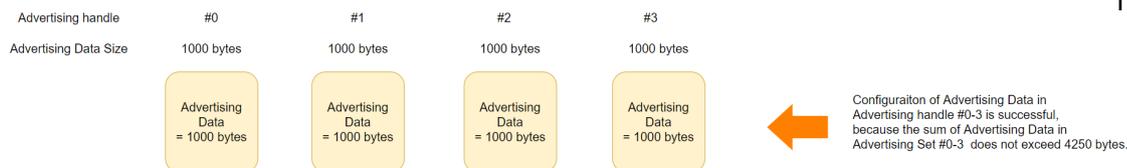


Figure 147: Figure 1.2

- When periodic advertising data is set,
  - At most 1650 bytes of data can be set to 1 advertising set.
  - The total buffer size in Controller for periodic advertising data is 4306 bytes. Therefore please note that more than 4306 bytes of periodic advertising data can not be set to all the advertising sets.
  - it's possible to update periodic advertising data in advertising, if the data\_length field in `st_ble_gap_adv_data_t` parameter is up to 252 bytes.

The result of this API call is notified in `BLE_GAP_EVENT_ADV_DATA_UPD_COMP` event.

### Parameters

[in]	p_adv_srsp_data	Advertising data/scan response data/periodic advertising data.
------	-----------------	--

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• p_adv_srsp_data is specified as NULL.</li> <li>• data_length field in p_adv_srsp_data parameter is not 0 and p_data field is specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	The following field in p_adv_srsp_data parameter is out of range. <ul style="list-style-type: none"> <li>• adv_hdl</li> <li>• data_type</li> <li>• data_length</li> <li>• zero_length_flag</li> </ul>
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

## ◆ R\_BLE\_GAP\_StartAdv()

```
ble_status_t R_BLE_GAP_StartAdv ( uint8_t adv_hdl, uint16_t duration, uint8_t
max_extd_adv_evts )
```

Start advertising.

This function starts advertising. Create the advertising set specified with `adv_hdl` by [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#), before calling this function. The result of this API call is notified in `BLE_GAP_EVENT_ADV_ON` event.

**Parameters**

[in]	adv_hdl	The advertising handle pointing to the advertising set which starts advertising. The valid range is 0x00 - 0x03.
[in]	duration	The duration for which the advertising set identified by <code>adv_hdl</code> is enabled. Time = duration * 10ms. When the duration expires, <code>BLE_GAP_EVENT_ADV_OFF</code> event notifies that advertising is stopped. The valid range is 0x0000 - 0xFFFF. The duration parameter is ignored when the value is set to 0x0000.
[in]	max_extd_adv_evts	The maximum number of advertising events that be sent during advertising. When all the advertising events( <code>max_extd_adv_evts</code> ) have been sent, <code>BLE_GAP_EVENT_ADV_OFF</code> event notifies that advertising is stopped. The <code>max_extd_adv_evts</code> parameter is ignored when the value is set to 0x00.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	adv_hdl is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_StopAdv()**

```
ble_status_t R_BLE_GAP_StopAdv ( uint8_t adv_hdl)
```

Stop advertising.

This function stops advertising. The result of this API call is notified in BLE\_GAP\_EVENT\_ADV\_OFF event.

**Parameters**

[in]	adv_hdl	The advertising handle pointing to the advertising set which stops advertising. The valid range is 0x00 - 0x03.
------	---------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	adv_hdl is out of range.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetPerdAdvParam()**

```
ble_status_t R_BLE_GAP_SetPerdAdvParam ( st_ble_gap_perd_adv_param_t * p_perd_adv_param)
```

Set periodic advertising parameters.

This function sets periodic advertising parameters. Create the advertising set which supports Non-Connectable, Non-Scannable advertising by [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#) before setting periodic advertising parameters. The result of this API call is notified in BLE\_GAP\_EVENT\_PERD\_ADV\_PARAM\_SET\_COMP event.

**Parameters**

[in]	p_perd_adv_param	Periodic advertising parameters.
------	------------------	----------------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_perd_adv_param is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The following field in the p_perd_adv_param parameter is out of range. <ul style="list-style-type: none"> <li>• adv_hdl</li> <li>• per_d_intv_min or per_d_intv_max</li> <li>• prop_type is neither 0x0000 nor 0x0040(BLE_GAP_PERD_PROP_TX_POWER)</li> </ul>
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_StartPerdAdv()**

ble\_status\_t R\_BLE\_GAP\_StartPerdAdv ( uint8\_t adv\_hdl)

Start periodic advertising.

This function starts periodic advertising. Set periodic advertising parameters to the advertising set, before starting periodic advertising. The result of this API call is notified in BLE\_GAP\_EVENT\_PERD\_ADV\_ON event.

**Parameters**

[in]	adv_hdl	Advertising handle identifying the advertising set which starts periodic advertising.
------	---------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	adv_hdl is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_StopPerdAdv()**

```
ble_status_t R_BLE_GAP_StopPerdAdv ( uint8_t adv_hdl)
```

Stop periodic advertising.

This function stops periodic advertising. If the return value of this API is BLE\_SUCCESS, the result is notified in BLE\_GAP\_EVENT\_PERD\_ADV\_OFF event.

**Parameters**

[in]	adv_hdl	Specify the handle of Advertising Set to stop Periodic Advertising.
------	---------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	adv_hdl is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_GetRemainAdvBufSize()**

```
ble_status_t R_BLE_GAP_GetRemainAdvBufSize ( uint16_t* p_remain_adv_data_size, uint16_t*
p_remain_perd_adv_data_size )
```

Get buffer size for advertising data/scan response data/periodic advertising data in the Controller.

This function gets the total size of advertising data/scan response data/periodic advertising data which can be currently set to Controller(all of the advertising sets). The application layer gets the data sizes via the parameters. By this API function call, no events occur.

**Parameters**

[out]	p_remain_adv_data_size	The free buffer size of Controller to which advertising data/scan response data can be currently set.
[out]	p_remain_perd_adv_data_size	The free buffer size of Controller to which periodic advertising data can be currently set.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_remain_adv_data_size or p_remain_perd_adv_data_size is specified as NULL.

## ◆ R\_BLE\_GAP\_RemoveAdvSet()

```
ble_status_t R_BLE_GAP_RemoveAdvSet ( uint8_t op_code, uint8_t adv_hdl )
```

Delete advertising set.

This function deletes an advertising set or deletes all the advertising sets. The result of this API call is notified in BLE\_GAP\_EVENT\_ADV\_SET\_REMOVE\_COMP event.

**Parameters**

[in]	op_code	The operation for delete or clear.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_RM_V_ADV_SET_REM_OP(0x01)</td> <td>Delete an advertising set.</td> </tr> <tr> <td>BLE_GAP_RM_V_ADV_SET_CLR_OP(0x02)</td> <td>Delete all the advertising sets.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_RM_V_ADV_SET_REM_OP(0x01)	Delete an advertising set.	BLE_GAP_RM_V_ADV_SET_CLR_OP(0x02)	Delete all the advertising sets.
macro	description							
BLE_GAP_RM_V_ADV_SET_REM_OP(0x01)	Delete an advertising set.							
BLE_GAP_RM_V_ADV_SET_CLR_OP(0x02)	Delete all the advertising sets.							
[in]	adv_hdl	Advertising handle identifying the advertising set deleted. If op_code is BLE_GAP_RMV_ADV_SET_CLR_OP, adv_hdl is ignored.						

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>op_code is out of range.</li> <li>When op_code is BLE_GAP_RMV_ADV_SET_REM_OP(0x01), adv_hdl is out of range.</li> </ul>
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

## ◆ R\_BLE\_GAP\_CreateConn()

```
ble_status_t R_BLE_GAP_CreateConn ( st_ble_gap_create_conn_param_t* p_param)
```

Request for a link establishment.

This function sends a connection request to a remote device to create a link. When Controller has received a request for establishment of a link from host stack, BLE\_GAP\_EVENT\_CREATE\_CONN\_COMP event is notified to the application layer. When the link is established, BLE\_GAP\_EVENT\_CONN\_IND event is notified to the application layer.

**Parameters**

[in]	p_param	Connection parameters.
------	---------	------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• p_param is specified as NULL.</li> <li>• p_conn_param_1M field and p_conn_param_2M and p_conn_param_coded field in p_param are specified as NULL.</li> <li>• When creating a link with 1M PHY, p_conn_param in p_conn_param_1M field in p_param is specified as NULL.</li> <li>• When creating a link with 2M PHY, p_conn_param in p_conn_param_2M field in p_param is specified as NULL.</li> <li>• When creating a link with coded MPHY, p_conn_param in p_conn_param_coded field in p_param is specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• init_filter_policy in p_param is out of range.</li> <li>• remote_bd_addr_type field or own_addr_type address field in p_param is out of range.</li> </ul>
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_CancelCreateConn()**

```
ble_status_t R_BLE_GAP_CancelCreateConn ( void )
```

Cancel the request for a link establishment.

This function cancels a request for establishing a link. When Controller has received the cancel request from host stack, BLE\_GAP\_EVENT\_CONN\_CANCEL\_COMP event is notified to the application layer. When the cancel procedure has completed, BLE\_GAP\_EVENT\_CONN\_IND event is notified to the application layer.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetChMap()**

```
ble_status_t R_BLE_GAP_SetChMap ( uint8_t* p_channel_map)
```

Set the Channel Map.

This function sets the channel map. The result of this API call is notified in BLE\_GAP\_EVENT\_CH\_MAP\_SET\_COMP event.

**Parameters**

[in]	p_channel_map	Channel map.
------	---------------	--------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_channel_map is specified as NULL.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_StartScan()**

```
ble_status_t R_BLE_GAP_StartScan ( st_ble_gap_scan_param_t* p_scan_param,  
st_ble_gap_scan_on_t* p_scan_enable )
```

Set scan parameter and start scan.

This function starts scanning. When scanning for the first time, set the `p_scan_param`. Setting scan parameters can be omitted by specifying `p_scan_param` as `NULL` after next time. The result of this API call is notified in `BLE_GAP_EVENT_SCAN_ON` event. Advertising report is notified in `BLE_GAP_EVENT_ADV_REPT_IND` event. Figure 1.3 shows the relationship between scan period, scan duration, scan interval and scan window.



Figure 148: Figure 1.3

When scan duration is non-zero, scan period is zero and scan duration expires, BLE\_GAP\_EVENT\_SCAN\_TO event is notified to the application layer.

### Parameters

[in]	p_scan_param	Scan parameter. When p_scan_param is specified as NULL, host stack doesn't set scan parameters and start scanning with the previous parameters.
[in]	p_scan_enable	Scan period, scan duration, duplicate filter and procedure type.

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>p_scan_enable is specified as NULL.</li> <li>p_phy_param_1M field and p_phy_param_coded field in p_scan_param are specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>proc_type field in p_scan_enable is out of range.</li> <li>filter_dups in p_scan_enable is out of range.</li> <li>o_addr_type in p_scan_param is out of range.</li> <li>filter_policy in p_scan_param is out of range.</li> <li>scan_type of p_scan_param's p_phy_param_1M or p_phy_param_coded is out of range.</li> </ul>
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_StopScan()**

```
ble_status_t R_BLE_GAP_StopScan ( void )
```

Stop scan.

This function stops scanning. The result of this API call is notified in BLE\_GAP\_EVENT\_SCAN\_OFF event.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_CreateSync()**

```
ble_status_t R_BLE_GAP_CreateSync ( st_ble_dev_addr_t * p_addr, uint8_t adv_sid, uint16_t skip, uint16_t sync_to )
```

Request for a periodic sync establishment.

This function sends a request for establishment of a periodic sync to a advertiser. In order to create a periodic sync, scan needs to be starting by [R\\_BLE\\_GAP\\_StartScan\(\)](#). When Controller has received the request from host stack, BLE\_GAP\_EVENT\_CREATE\_SYNC\_COMP event is notified to the application layer. When the periodic sync is established, BLE\_GAP\_EVENT\_SYNC\_EST event is notified to the application layer.

**Parameters**

[in]	p_addr	The address of periodic advertiser. When p_addr is specified as NULL, local device creates a periodic sync with the advertiser registered in Periodic Advertiser List.
[in]	adv_sid	Advertising SID. When p_addr is specified as NULL, adv_sid is ignored. Valid range is 0x00 - 0x0F.
[in]	skip	The number of consecutive periodic advertising packets that local device may skip after receiving a periodic advertising packet. Valid range is 0x0000 - 0x01F3.

[in]	sync_to	The maximum permitted time between successful receives. When sync_to expires, the periodic sync is lost. Time(ms) = sync_to * 10. Valid range is 0x000A - 0x4000.
------	---------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_addr is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The following parameter is out of range. <ul style="list-style-type: none"> <li>• address type in p_addr</li> <li>• adv_sid</li> <li>• skip</li> <li>• sync_to</li> </ul>
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

**◆ R\_BLE\_GAP\_CancelCreateSync()**

```
ble_status_t R_BLE_GAP_CancelCreateSync ( void )
```

Cancel the request for a periodic sync establishment.

This function cancels a request for establishing a periodic sync. The result of this API call is notified in BLE\_GAP\_EVENT\_SYNC\_CREATE\_CANCEL\_COMP event.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_TerminateSync()**

```
ble_status_t R_BLE_GAP_TerminateSync ( uint16_t sync_hdl)
```

Terminate the periodic sync.

This function terminates a periodic sync. The result of this API call is notified in BLE\_GAP\_EVENT\_SYNC\_TERM event.

**Parameters**

[in]	sync_hdl	Sync handle identifying the periodic sync to be terminated.
------	----------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	sync_hdl is out of range.
BLE_ERR_UNSUPPORTED(0x0007)	Not supported.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

### ◆ R\_BLE\_GAP\_ConfPerdAdvList()

```
ble_status_t R_BLE_GAP_ConfPerdAdvList ( uint8_t op_code, st_ble_dev_addr_t * p_addr, uint8_t *
p_adv_sid_set, uint8_t device_num )
```

Set Periodic Advertiser List.

This function supports the following operations regarding Periodic Advertiser List.

- Add the device to Periodic Advertiser List.
- Delete the device from Periodic Advertiser List.
- Clear Periodic Advertiser List.

The total number of Periodic Advertiser List entries is defined as BLE\_GAP\_PERD\_LIST\_MAX\_ENTRY. The result of this API call is notified in BLE\_GAP\_EVENT\_PERD\_LIST\_CONF\_COMP event.

#### Parameters

[in]	op_code	The operation for Periodic Advertiser List.								
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_LIST_ADD_D EV(0x01)</td> <td>Add the device to the list.</td> </tr> <tr> <td>BLE_GAP_LIST_REM_D EV(0x02)</td> <td>Delete the device from the list.</td> </tr> <tr> <td>BLE_GAP_LIST_CLR(0x03)</td> <td>Clear the list.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_LIST_ADD_D EV(0x01)	Add the device to the list.	BLE_GAP_LIST_REM_D EV(0x02)	Delete the device from the list.	BLE_GAP_LIST_CLR(0x03)	Clear the list.
macro	description									
BLE_GAP_LIST_ADD_D EV(0x01)	Add the device to the list.									
BLE_GAP_LIST_REM_D EV(0x02)	Delete the device from the list.									
BLE_GAP_LIST_CLR(0x03)	Clear the list.									
[in]	p_addr	An array of device address to add / delete to the list. The number of elements is specified by device_num. If op_code is BLE_GAP_LIST_CLR, p_addr is ignored.								
[in]	p_adv_sid_set	An array of SID of the advertiser to add / delete to the list. The number of elements is specified by device_num. If op_code is BLE_GAP_LIST_CLR, p_adv_sid_set is ignored.								
[in]	device_num	The number of devices add / delete to the list.								

		Valid range is 1- <code>BLE_GAP_PERD_LIST_MAX_ENTRY</code> . If <code>op_code</code> is <code>BLE_GAP_LIST_CLR</code> , <code>device_num</code> is ignored.
--	--	---

**Return values**

<code>BLE_SUCCESS(0x0000)</code>	Success
<code>BLE_ERR_INVALID_PTR(0x0001)</code>	When <code>op_code</code> is <code>BLE_GAP_LIST_ADD_DEV</code> or <code>BLE_GAP_LIST_REM_DEV</code> , <code>p_addr</code> or <code>p_adv_sid_set</code> is specified as <code>NULL</code> .
<code>BLE_ERR_INVALID_ARG(0x0003)</code>	<code>op_code</code> or address type field in <code>p_addr</code> or <code>p_adv_sid_set</code> or <code>device_num</code> is out of range.
<code>BLE_ERR_UNSUPPORTED(0x0007)</code>	Not supported.
<code>BLE_ERR_INVALID_STATE(0x0008)</code>	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• While operating Periodic Advertiser List, this function was called.</li> <li>• The task for host stack is not running.</li> </ul>
<code>BLE_ERR_MEM_ALLOC_FAILED(0x000C)</code>	There are no memories for operating periodic advertiser.

◆ **R\_BLE\_GAP\_AuthorizeDev()**

```
ble_status_t R_BLE_GAP_AuthorizeDev ( uint16_t conn_hdl, uint8_t author_flag )
```

Authorize a remote device.

User authorizes a remote device by this function. This function is used when a remote device accesses a GATT Characteristic in local device which requests user authorization. The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to be authorized or not by user.						
[in]	author_flag	Authorize or not the remote device. <table border="1" data-bbox="1072 831 1469 1167"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_NOT_AUTHORIZE(0x00)</td> <td>Not authorize the remote device.</td> </tr> <tr> <td>BLE_GAP_AUTHORIZED(0x01)</td> <td>Authorize the remote device.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_NOT_AUTHORIZE(0x00)	Not authorize the remote device.	BLE_GAP_AUTHORIZED(0x01)	Authorize the remote device.
macro	description							
BLE_GAP_NOT_AUTHORIZE(0x00)	Not authorize the remote device.							
BLE_GAP_AUTHORIZED(0x01)	Authorize the remote device.							

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	author_flag is out of range.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

◆ **R\_BLE\_GAP\_GetRemDevInfo()**

```
ble_status_t R_BLE_GAP_GetRemDevInfo ( uint16_t conn_hdl)
```

Get the information about remote device.

This function retrieves information about the remote device. The information includes BD\_ADDR, the version number and LE features. The result of this API call is notified in BLE\_GAP\_EVENT\_GET\_REM\_DEV\_INFO event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device whose information to be retrieved.
------	----------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetPairingParams()**

```
ble_status_t R_BLE_GAP_SetPairingParams ( st_ble_gap_pairing_param_t * p_pair_param)
```

Set the parameters using pairing.

This function sets the parameters used in pairing. The parameters set by this API are sent to the remote device when pairing occurred. The result of this API call is returned by a return value.

**Parameters**

[in]	p_pair_param	Pairing parameters.
------	--------------	---------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The following field in p_pair_param is out of range. <ul style="list-style-type: none"> <li>• iocap</li> <li>• max_key_size</li> <li>• mitm</li> <li>• bonding</li> <li>• key_notf</li> <li>• sec_conn_only</li> </ul>

◆ **R\_BLE\_GAP\_SetLocIdInfo()**

```
ble_status_t R_BLE_GAP_SetLocIdInfo ( st_ble_dev_addr_t * p_lc_id_addr, uint8_t * p_lc_irk )
```

Set the IRK and the identity address distributed to a remote device.

This function registers local IRK and identity address of local device in host stack. The IRK and the identity address are distributed to a remote device in pairing. The result of this API call is returned by a return value.

**Parameters**

[in]	p_lc_id_addr	Identity address to be registered in host stack.
[in]	p_lc_irk	IRK to be registered in host stack.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_lc_id_addr or p_lc_irk is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	Address type field in p_lc_id_addr is out of range.

◆ **R\_BLE\_GAP\_SetLocCsrk()**

```
ble_status_t R_BLE_GAP_SetLocCsrk ( uint8_t * p_local_csrk )
```

Set the CSRK distributed to a remote device.

This function registers local CSRK in host stack. The CSRK is distributed to a remote device in pairing. The result of this API call is returned by a return value.

**Parameters**

[in]	p_local_csrk	CSRK to be registered in host stack.
------	--------------	--------------------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_local_csrk is specified as NULL.

◆ **R\_BLE\_GAP\_StartPairing()**

```
ble_status_t R_BLE_GAP_StartPairing ( uint16_t conn_hdl)
```

Start pairing.

This function starts pairing with a remote device. The result of this API call is returned by a return value. The result of pairing is notified in BLE\_GAP\_EVENT\_PAIRING\_COMP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device which local device starts pairing with.
------	----------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	While generating OOB data, this function was called.
BLE_ERR_CONTEXT_FULL(0x000B)	While pairing, this function was called.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

◆ **R\_BLE\_GAP\_ReplyPairing()**

```
ble_status_t R_BLE_GAP_ReplyPairing ( uint16_t conn_hdl, uint8_t response )
```

Reply the pairing request from a remote device.

This function replies to the pairing request from the remote device. The pairing request from the remote device is notified in BLE\_GAP\_EVENT\_PAIRING\_REQ event. The result of this API call is returned by a return value. The result of pairing is notified in BLE\_GAP\_EVENT\_PAIRING\_COMP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device which local device starts pairing with.						
[in]	response	Accept or reject the pairing request from the remote device. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_PAIRING_ACCEPT(0x00)</td> <td>Accept the pairing request.</td> </tr> <tr> <td>BLE_GAP_PAIRING_REJECT(0x01)</td> <td>Reject the pairing request.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_PAIRING_ACCEPT(0x00)	Accept the pairing request.	BLE_GAP_PAIRING_REJECT(0x01)	Reject the pairing request.
macro	description							
BLE_GAP_PAIRING_ACCEPT(0x00)	Accept the pairing request.							
BLE_GAP_PAIRING_REJECT(0x01)	Reject the pairing request.							

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	response is out of range.
BLE_ERR_INVALID_STATE(0x0008)	While generating OOB data, this function was called.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	When this function was called, host stack has not yet received BLE_GAP_EVENT_PAIRING_REQ event.

◆ **R\_BLE\_GAP\_StartEnc()**

```
ble_status_t R_BLE_GAP_StartEnc ( uint16_t conn_hdl)
```

Encryption the link.

This function starts encryption of the link. In case of master device, the local device requests for the encryption to a remote device. In case of slave device, the local device sends a Security Request to a remote device. After receiving the Security Request, the remote device requests for the encryption to the local device. The result of the encryption is returned in BLE\_GAP\_EVENT\_ENC\_CHG event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the link which is encrypted.
------	----------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• Pairing has not been completed.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

### ◆ R\_BLE\_GAP\_ReplyPasskeyEntry()

```
ble_status_t R_BLE_GAP_ReplyPasskeyEntry ( uint16_t conn_hdl, uint32_t passkey, uint8_t response )
```

Reply the passkey entry request.

When BLE\_GAP\_EVENT\_PASSKEY\_ENTRY\_REQ event is notified, the response to passkey entry is sent by this function. The result of this API call is returned by a return value.

#### Parameters

[in]	conn_hdl	Connection handle identifying the remote device which the reply to passkey entry is sent.						
[in]	passkey	Passkey. The valid range is 000000 - 999999 in decimal.						
[in]	response	Active or negative reply to passkey entry. <table border="1" data-bbox="1072 913 1469 1288"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_PAIRING_ACCEPT(0x00)</td> <td>Accept the passkey entry pairing.</td> </tr> <tr> <td>BLE_GAP_PAIRING_REJECT(0x01)</td> <td>Reject the passkey entry pairing.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_PAIRING_ACCEPT(0x00)	Accept the passkey entry pairing.	BLE_GAP_PAIRING_REJECT(0x01)	Reject the passkey entry pairing.
macro	description							
BLE_GAP_PAIRING_ACCEPT(0x00)	Accept the passkey entry pairing.							
BLE_GAP_PAIRING_REJECT(0x01)	Reject the passkey entry pairing.							

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	passkey or response is out of range.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	When this function was called, pairing has not yet started.

## ◆ R\_BLE\_GAP\_ReplyNumComp()

```
ble_status_t R_BLE_GAP_ReplyNumComp ( uint16_t conn_hdl, uint8_t response )
```

Reply the numeric comparison request.

When BLE\_GAP\_EVENT\_NUM\_COMP\_REQ event is notified, the response to Numeric Comparison is sent by this function. The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device which the reply to Numeric Comparison is sent.						
[in]	response	Active or negative reply in Numeric Comparison. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_PAIRING_ACCEPT(0x00)</td> <td>The number displayed in the local is the same as the one of the remote.</td> </tr> <tr> <td>BLE_GAP_PAIRING_REJECT(0x01)</td> <td>The number displayed in the local is differs from the one of the remote.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_PAIRING_ACCEPT(0x00)	The number displayed in the local is the same as the one of the remote.	BLE_GAP_PAIRING_REJECT(0x01)	The number displayed in the local is differs from the one of the remote.
macro	description							
BLE_GAP_PAIRING_ACCEPT(0x00)	The number displayed in the local is the same as the one of the remote.							
BLE_GAP_PAIRING_REJECT(0x01)	The number displayed in the local is differs from the one of the remote.							

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	response is out of range.
BLE_ERR_INVALID_STATE(0x0008)	When this function was called, host stack has not yet received BLE_GAP_EVENT_NUM_COMP_REQ event.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	When this function was called, pairing has not yet started.

◆ **R\_BLE\_GAP\_NotifyKeyPress()**

```
ble_status_t R_BLE_GAP_NotifyKeyPress ( uint16_t conn_hdl, uint8_t key_press )
```

Notify the input key type which a remote device inputs in the passkey entry.

This function notifies the input key type to the remote device in passkey entry. The result is returned from this API.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to which the key notification is sent.												
[in]	key_press	Input key type. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_LE_SC_PASSKEY_ENTRY_STARTED(0x00)</td> <td>Notify that passkey entry started.</td> </tr> <tr> <td>BLE_GAP_LE_SC_PASSKEY_DIGIT_ENTERED(0x01)</td> <td>Notify that passkey digit entered.</td> </tr> <tr> <td>BLE_GAP_LE_SC_PASSKEY_DIGIT_ERASED(0x02)</td> <td>Notify that passkey digit erased.</td> </tr> <tr> <td>BLE_GAP_LE_SC_PASSKEY_CLEARED(0x03)</td> <td>Notify that passkey cleared.</td> </tr> <tr> <td>BLE_GAP_LE_SC_PASSKEY_ENTRY_COMPLETED(0x04)</td> <td>Notify that passkey entry completed.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_LE_SC_PASSKEY_ENTRY_STARTED(0x00)	Notify that passkey entry started.	BLE_GAP_LE_SC_PASSKEY_DIGIT_ENTERED(0x01)	Notify that passkey digit entered.	BLE_GAP_LE_SC_PASSKEY_DIGIT_ERASED(0x02)	Notify that passkey digit erased.	BLE_GAP_LE_SC_PASSKEY_CLEARED(0x03)	Notify that passkey cleared.	BLE_GAP_LE_SC_PASSKEY_ENTRY_COMPLETED(0x04)	Notify that passkey entry completed.
macro	description													
BLE_GAP_LE_SC_PASSKEY_ENTRY_STARTED(0x00)	Notify that passkey entry started.													
BLE_GAP_LE_SC_PASSKEY_DIGIT_ENTERED(0x01)	Notify that passkey digit entered.													
BLE_GAP_LE_SC_PASSKEY_DIGIT_ERASED(0x02)	Notify that passkey digit erased.													
BLE_GAP_LE_SC_PASSKEY_CLEARED(0x03)	Notify that passkey cleared.													
BLE_GAP_LE_SC_PASSKEY_ENTRY_COMPLETED(0x04)	Notify that passkey entry completed.													

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	key_press parameter is out of range.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	When this function was called, pairing has not yet started.

◆ **R\_BLE\_GAP\_GetDevSecInfo()**

```
ble_status_t R_BLE_GAP_GetDevSecInfo ( uint16_t conn_hdl, st_ble_gap_auth_info_t * p_sec_info )
```

Get the security information about the remote device.

This function gets the parameters which has been negotiated with the remote device in pairing. The parameters can be retrieved after pairing. The result is returned by p\_sec\_info.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device whose bonding information is retrieved.
[in]	p_sec_info	Return the security information which has been negotiated in pairing.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_sec_info is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The remote device bonding information has not been set to host stack.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.

◆ **R\_BLE\_GAP\_ReplyExKeyInfoReq()**

ble\_status\_t R\_BLE\_GAP\_ReplyExKeyInfoReq ( uint16\_t conn\_hdl)

Distribute the keys of local device.

When key exchange request is notified by BLE\_GAP\_EVENT\_EX\_KEY\_REQ event at pairing, keys of the local device are distributed. The result is returned from this API.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to which the key is distributed.
------	----------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	When this function was called, pairing has not yet started.

### ◆ R\_BLE\_GAP\_SetRemOobData()

```
ble_status_t R_BLE_GAP_SetRemOobData ( st_ble_dev_addr_t * p_addr, uint8_t oob_data_flag,
st_ble_gap_oob_data_t * p_oob )
```

Set the oob data from a remote device.

This function registers the OOB data received from a remote device. When oob\_data\_flag indicates that the OOB data has been received, the setting regarding OOB data is reflected in pairing. In order to do OOB pairing, set the OOB data received from the remote device before pairing. The result is returned from this API.

#### Parameters

[in]	p_addr	The remote device address.						
[in]	oob_data_flag	This parameter indicates whether the local device has received the OOB data from the remote device or not. <table border="1" data-bbox="1072 864 1468 1388"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GAP_OOB_DATA_NO_T_PRESENT(0x00)</td> <td>Reply that No OOB data has been received when pairing.</td> </tr> <tr> <td>BLE_GAP_OOB_DATA_PRESENT(0x01)</td> <td>Reply that the OOB data has been received when pairing.</td> </tr> </tbody> </table>	macro	description	BLE_GAP_OOB_DATA_NO_T_PRESENT(0x00)	Reply that No OOB data has been received when pairing.	BLE_GAP_OOB_DATA_PRESENT(0x01)	Reply that the OOB data has been received when pairing.
macro	description							
BLE_GAP_OOB_DATA_NO_T_PRESENT(0x00)	Reply that No OOB data has been received when pairing.							
BLE_GAP_OOB_DATA_PRESENT(0x01)	Reply that the OOB data has been received when pairing.							
[in]	p_oob	The OOB data received from the remote device.						

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows. <ul style="list-style-type: none"> <li>• p_addr is specified as NULL.</li> <li>• oob_data_flag is BLE_GAP_OOB_DATA_PRESENT and p_oob is specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	oob_data_flag is out of range.
BLE_ERR_CONTEXT_FULL(0x000B)	There is no room to register the OOB data received from a remote device.

◆ **R\_BLE\_GAP\_CreateScOobData()**

```
ble_status_t R_BLE_GAP_CreateScOobData ( void )
```

Create data for oob in secure connection.

This function generates the OOB data distributed to a remote device in Secure Connections. The result of this API call is notified in BLE\_GAP\_EVENT\_SC\_OOB\_CREATE\_COMP event.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• This function was called in pairing.</li> <li>• The task for host stack is not running.</li> </ul>
BLE_ERR_ALREADY_IN_PROGRESS(0x000A)	This function was called in creating OOB data.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.

◆ **R\_BLE\_GAP\_SetBondInfo()**

```
ble_status_t R_BLE_GAP_SetBondInfo ( st_ble_gap_bond_info_t* p_bond_info, uint8_t device_num,
uint8_t* p_set_num )
```

Set the bonding information stored in non-volatile memory to the host stack.

Set the bonding information of the remote device in the host stack. After power re-supply, when the remote device bonding information stored in non-volatile memory is set to host stack, this function is used. Host stack can be set the number specified by the device\_num parameter of bonding information.

**Parameters**

[in]	p_bond_info	An array of bonding information. The number of elements is specified by device_num.
[in]	device_num	The number of the devices of which host stack registers bonding information.
[in]	p_set_num	The number of the devices whose bonding information was registered in host stack.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	p_bond_info or p_set_num is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	device_num is out of range.
BLE_ERR_CONTEXT_FULL(0x000B)	Host stack already has the maximum number of bonding information.

## ◆ R\_BLE\_GAP\_DeleteBondInfo()

```
void R_BLE_GAP_DeleteBondInfo ( int32_t local, int32_t remote, st_ble_dev_addr_t* p_addr,
ble_gap_del_bond_cb_t gap_del_bond_cb )
```

This function deletes the bonding information in Host Stack.  
When a function for deleting the bonding information stored in non-volatile area is registered by the gap\_del\_bond\_cb parameter, it is deleted as well as the bonding information in Host Stack.

**Parameters**

[in]	local	The type of the local bonding information to be deleted.
[in]	remote	The type of the remote bonding information to be deleted.

macro	description
BLE_GAP_SE C_DEL_LOC_ NONE(0x00)	Delete no local keys.
BLE_GAP_SE C_DEL_LOC_I RK(0x01)	Delete local IRK and identity address.
BLE_GAP_SE C_DEL_LOC_ CSRK(0x02)	Delete local CSRK.
BLE_GAP_SE C_DEL_LOC_ ALL(0x03)	Delete all local keys.

macro	description
BLE_GAP_SE C_DEL_REM_ NONE(0x00)	Delete no remote device keys.
BLE_GAP_SE C_DEL_REM_ SA(0x01)	Delete the keys specified by the p_addr parameter.
BLE_GAP_SE C_DEL_REM_ NOT_CONN( 0x02)	Delete keys of not connected remote devices.
BLE_GAP_SE C_DEL_REM_ ALL(0x03)	Delete all remote device keys.

[in]	p_addr	p_addr is specified as the address of the remote device whose keys are deleted when the rem_info parameter is set to <a href="#">BLE_GAP_SEC_DEL_REM_SA(0x01)</a> .
[in]	gap_del_bond_cb	This parameter is a callback function which deletes the bonding information stored in non-volatile area. After deleting the bonding information stored in Host Stack, the callback function is called. If no bonding information is stored in non-volatile area, specify the parameter as NULL.
<b>Return values</b>		
none		

### ◆ R\_BLE\_GAP\_ReplyLtkReq()

```
ble_status_t R_BLE_GAP_ReplyLtkReq ( uint16_t conn_hdl, uint16_t ediv, uint8_t* p_peer_rand,
uint8_t response )
```

Reply the LTK request from a remote device.

This function replies to the LTK request in BLE\_GAP\_EVENT\_LTK\_REQ event from a remote device. The result of the LTK reply is returned in BLE\_GAP\_EVENT\_LTK\_RSP\_COMP event. When the link encryption has completed, BLE\_GAP\_EVENT\_ENC\_CHG event is notified.

#### Parameters

[in]	conn_hdl	Connection handle identifying the remote device which sent the LTK request.
[in]	ediv	Ediv notified in BLE_GAP_EVENT_LTK_REQ event.
[in]	p_peer_rand	Rand notified in BLE_GAP_EVENT_LTK_REQ event.
[in]	response	Response to the LTK request. If

"BLE\_GAP\_LTK\_REQ\_ACCEPT" is specified, when no LTK has been exchanged in pairing, reject the LTK request.

macro	description
<a href="#">BLE_GAP_LTK_REQ_ACCEPT</a>	Reply for the LTK request.
<a href="#">BLE_GAP_LTK_REQ_DENY</a>	Reject the LTK request.

### Return values

<a href="#">BLE_SUCCESS</a> (0x0000)	Success
<a href="#">BLE_ERR_INVALID_PTR</a> (0x0001)	p_peer_rand is specified as NULL in case of legacy pairing.
<a href="#">BLE_ERR_INVALID_ARG</a> (0x0003)	response is out of range.
<a href="#">BLE_ERR_INVALID_STATE</a> (0x0008)	The task for host stack is not running.
<a href="#">BLE_ERR_MEM_ALLOC_FAILED</a> (0x000C)	Insufficient memory is needed to generate this function.
<a href="#">BLE_ERR_INVALID_HDL</a> (0x000E)	The remote device specified by conn_hdl is not found.

## 4.2.5.2 GATT\_COMMON

Modules » [Bluetooth Low Energy Library \(r\\_ble\)](#)

### Functions

ble\_status\_t [R\\_BLE\\_GATT\\_GetMtu](#) (uint16\_t conn\_hdl, uint16\_t \*p\_mtu)

This function gets the current MTU used in GATT communication.

[More...](#)

### Detailed Description

### Function Documentation

### ◆ R\_BLE\_GATT\_GetMtu()

```
ble_status_t R_BLE_GATT_GetMtu ( uint16_t conn_hdl, uint16_t* p_mtu )
```

This function gets the current MTU used in GATT communication.

Both GATT server and GATT Client can use this function.

The result of this API call is returned by a return value.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server or the GATT Client.
[in]	p_mtu	The Current MTU. Before MTU exchange, this parameter is 23 bytes. After MTU exchange, this parameter is the negotiated MTU.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The mtu parameter is NULL.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server or the GATT Client specified by conn_hdl was not found.

### 4.2.5.3 GATT\_SERVER

Modules » [Bluetooth Low Energy Library \(r\\_ble\)](#)

#### Functions

```
ble_status_t R_BLE_GATTS_Init (uint8_t cb_num)
```

This function initializes the GATT Server and registers the number of the callbacks for GATT Server event. [More...](#)

```
ble_status_t R_BLE_GATTS_SetDbInst (st_ble_gatts_db_cfg_t *p_db_inst)
```

This function sets GATT Database to host stack. [More...](#)

```
ble_status_t R_BLE_GATTS_RegisterCb (ble_gatts_app_cb_t cb, uint8_t priority)
```

This function registers a callback for GATT Server event. [More...](#)

```
ble_status_t R_BLE_GATTS_DeregisterCb (ble_gatts_app_cb_t cb)
```

This function deregisters the callback function for GATT Server event. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_Notification](#) (uint16\_t conn\_hdl,  
st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_ntf\_data)

This function sends a notification of an attribute's value. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_Indication](#) (uint16\_t conn\_hdl,  
st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_ind\_data)

This function sends a indication of an attribute's value. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_GetAttr](#) (uint16\_t conn\_hdl, uint16\_t attr\_hdl,  
st\_ble\_gatt\_value\_t \*p\_value)

This function gets a attribute value from the GATT Database. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_SetAttr](#) (uint16\_t conn\_hdl, uint16\_t attr\_hdl,  
st\_ble\_gatt\_value\_t \*p\_value)

This function sets an attribute value to the GATT Database. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_SendErrRsp](#) (uint16\_t error\_code)

This function sends an error response to a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_RspExMtu](#) (uint16\_t conn\_hdl, uint16\_t mtu)

This function replies to a MTU Exchange Request from a remote device. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTS\\_SetPrepareQueue](#) (st\_ble\_gatt\_pre\_queue\_t  
\*p\_pre\_queues, uint8\_t queue\_num)

Register prepare queue and buffer in Host Stack. [More...](#)

## Detailed Description

### Data Structures

struct [st\\_ble\\_gatt\\_value\\_t](#)  
Attribute Value. [More...](#)

struct [st\\_ble\\_gatt\\_hdl\\_value\\_pair\\_t](#)  
Attribute handle and attribute Value. [More...](#)

struct [st\\_ble\\_gatt\\_queue\\_att\\_val\\_t](#)  
Queued writes Attribute Value. [More...](#)

struct [st\\_ble\\_gatt\\_queue\\_pair\\_t](#)  
Queued writes Attribute Value. [More...](#)

struct [st\\_ble\\_gatt\\_queue\\_elm\\_t](#)  
Prepare Write Queue element for long characteristic. [More...](#)

struct [st\\_ble\\_gatt\\_pre\\_queue\\_t](#)  
Prepare Write Queue for long characteristic. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_params\\_t](#)  
Attribute value to be set to or retrieved from the GATT Database and the access type from the GATT Client. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_conn\\_hdl\\_t](#)  
Information about the service or the characteristic that the attribute belongs to. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_access\\_evt\\_t](#)  
This structure notifies that the GATT Database has been accessed from a GATT Client. [More...](#)

struct [st\\_ble\\_gatts\\_conn\\_evt\\_t](#)  
This structure notifies that the link with the GATT Client has been established. [More...](#)

struct [st\\_ble\\_gatts\\_disconn\\_evt\\_t](#)  
This structure notifies that the link with the GATT Client has been disconnected. [More...](#)

struct [st\\_ble\\_gatts\\_ex\\_mtu\\_req\\_evt\\_t](#)

This structure notifies that a MTU Exchange Request PDU has been received from a GATT Client. [More...](#)

struct [st\\_ble\\_gatts\\_cfm\\_evt\\_t](#)

This structure notifies that a Confirmation PDU has been received from a GATT Client. [More...](#)

struct [st\\_ble\\_gatts\\_read\\_by\\_type\\_rsp\\_evt\\_t](#)

This structure notifies that a Read By Type Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_read\\_rsp\\_evt\\_t](#)

This structure notifies that a Read Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_read\\_blob\\_rsp\\_evt\\_t](#)

This structure notifies that a Read Blob Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_read\\_multi\\_rsp\\_evt\\_t](#)

This structure notifies that a Read Multiple Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_write\\_rsp\\_evt\\_t](#)

This structure notifies that a Write Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_prepare\\_write\\_rsp\\_evt\\_t](#)

This structure notifies that a Prepare Write Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_exe\\_write\\_rsp\\_evt\\_t](#)

This structure notifies that a Execute Write Response PDU has been sent from GATT Server. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_uuid\\_cfg\\_t](#)

A structure that defines the information on the position where UUIDs

are used. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_attr\\_cfg\\_t](#)

A structure that defines the detailed information of the attributes. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_attr\\_list\\_t](#)

The number of attributes are stored. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_char\\_cfg\\_t](#)

A structure that defines the detailed information of the characteristics. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_serv\\_cfg\\_t](#)

A structure that defines the detailed information of the characteristics. [More...](#)

struct [st\\_ble\\_gatts\\_db\\_cfg\\_t](#)

This is the structure of GATT Database that is specified in [R\\_BLE\\_GATTS\\_SetDbInst\(\)](#). [More...](#)

struct [st\\_ble\\_gatts\\_evt\\_data\\_t](#)

[st\\_ble\\_gatts\\_evt\\_data\\_t](#) is the type of the data notified in a GATT Server Event. [More...](#)

## Macros

`#define` [BLE\\_GATT\\_DEFAULT\\_MTU](#)

GATT Default MTU.

`#define` [BLE\\_GATT\\_16\\_BIT\\_UUID\\_FORMAT](#)

GATT Identification for 16-bit UUID Format.

`#define` [BLE\\_GATT\\_128\\_BIT\\_UUID\\_FORMAT](#)

GATT Identification for 128-bit UUID Format.

`#define` [BLE\\_GATT\\_16\\_BIT\\_UUID\\_SIZE](#)

GATT 16-bit UUID Size.

```
#define BLE_GATT_128_BIT_UUID_SIZE  
GATT 128-bit UUID Size.
```

```
#define BLE_GATT_INVALID_ATTR_HDL_VAL  
GATT Invalid Attribute Handle Value.
```

```
#define BLE_GATT_ATTR_HDL_START_RANGE  
GATT Attribute Handle Start Range.
```

```
#define BLE_GATT_ATTR_HDL_END_RANGE  
GATT Attribute Handle End Range.
```

```
#define BLE_GATTS_CLI_CNFG_NOTIFICATION  
GATT Client Configuration values. Enable Notification.
```

```
#define BLE_GATTS_CLI_CNFG_INDICATION  
GATT Client Configuration values. Enable Indication.
```

```
#define BLE_GATTS_CLI_CNFG_DEFAULT  
GATT Client Configuration values. Default value or disable  
notification/indication.
```

```
#define BLE_GATTS_SER_CNFG_BROADCAST  
GATT Server Configuration values. Enable broadcast.
```

```
#define BLE_GATTS_SER_CNFG_DEFAULT  
GATT Server Configuration values. Default value.
```

```
#define BLE_GATTS_MAX_CB  
GATT Server Callback Number.
```

```
#define BLE_GATTS_OP_CHAR_VALUE_READ_REQ
```

Characteristic Value Local Read Operation.

```
#define BLE_GATTS_OP_CHAR_VALUE_WRITE_REQ
```

Characteristic Value Local Write Operation.

```
#define BLE_GATTS_OP_CHAR_VALUE_WRITE_WITHOUT_REQ
```

Characteristic Value Local Write Without Response Operation.

```
#define BLE_GATTS_OP_CHAR_CLI_CNFG_READ_REQ
```

Characteristic Client Configuration Local Read Operation.

```
#define BLE_GATTS_OP_CHAR_CLI_CNFG_WRITE_REQ
```

Characteristic Client Configuration Local Write Operation.

```
#define BLE_GATTS_OP_CHAR_SER_CNFG_READ_REQ
```

Characteristic Server Configuration Local Read Operation.

```
#define BLE_GATTS_OP_CHAR_SER_CNFG_WRITE_REQ
```

Characteristic Server Configuration Local Write Operation.

```
#define BLE_GATTS_OP_CHAR_PEER_READ_REQ
```

Characteristic Value Peer Read Operation.

```
#define BLE_GATTS_OP_CHAR_PEER_WRITE_REQ
```

Characteristic Value Peer Write Operation.

```
#define BLE_GATTS_OP_CHAR_PEER_WRITE_CMD
```

Characteristic Value Peer Write Command.

```
#define BLE_GATTS_OP_CHAR_PEER_CLI_CNFG_READ_REQ
```

Characteristic Client Configuration Peer Read Operation.

```
#define BLE_GATTS_OP_CHAR_PEER_CLI_CNFG_WRITE_REQ
```

Characteristic Client Configuration Peer Write Operation.

```
#define BLE_GATTS_OP_CHAR_PEER_SER_CNFG_READ_REQ  
Characteristic Server Configuration Peer Read Operation.
```

```
#define BLE_GATTS_OP_CHAR_PEER_SER_CNFG_WRITE_REQ  
Characteristic Server Configuration Peer Write Operation.
```

```
#define BLE_GATTS_OP_CHAR_PEER_USR_DESC_READ_REQ  
Characteristic User Description Peer Read Operation.
```

```
#define BLE_GATTS_OP_CHAR_PEER_USR_DESC_WRITE_REQ  
Characteristic User Description Peer Write Operation.
```

```
#define BLE_GATTS_OP_CHAR_PEER_HLD_DESC_READ_REQ  
Characteristic Higher Layer Defined Descriptor Peer Read Operation.
```

```
#define BLE_GATTS_OP_CHAR_PEER_HLD_DESC_WRITE_REQ  
Characteristic Higher Layer Defined Descriptor Peer Write Operation.
```

```
#define BLE_GATTS_OP_CHAR_REQ_AUTHOR  
Operation Required Authorization.
```

```
#define BLE_GATT_DB_READ  
Allow clients to read.
```

```
#define BLE_GATT_DB_WRITE  
Allow clients to write.
```

```
#define BLE_GATT_DB_WRITE_WITHOUT_RSP  
Allow clients to write without response.
```

```
#define BLE_GATT_DB_READ_WRITE  
Allow clients to access of all.
```

```
#define BLE_GATT_DB_NO_AUXILIARY_PROPERTY
```

No auxiliary properties.

```
#define BLE_GATT_DB_FIXED_LENGTH_PROPERTY
```

Fixed length attribute value.

```
#define BLE_GATT_DB_AUTHORIZATION_PROPERTY
```

Attributes requiring authorization.

```
#define BLE_GATT_DB_ATTR_DISABLED
```

The attribute is disabled. If this value is set, the attribute cannot be found and accessed by a GATT Client.

```
#define BLE_GATT_DB_128_BIT_UUID_FORMAT
```

Attribute with 128 bit UUID.

```
#define BLE_GATT_DB_PEER_SPECIFIC_VAL_PROPERTY
```

Attribute managed by each GATT Client.

```
#define BLE_GATT_DB_CONST_ATTR_VAL_PROPERTY
```

Fixed attribute value.

```
#define BLE_GATT_DB_SER_SECURITY_UNAUTH
```

Unauthenticated pairing(Security Mode1 Security Level 2, Security Mode 2 Security Level 1). Unauthenticated pairing is required to access the service.

```
#define BLE_GATT_DB_SER_SECURITY_AUTH
```

Authenticated pairing(Security Mode1 Security Level 3, Security Mode 2 Security Level 2). Authenticated pairing is required to access the service.

```
#define BLE_GATT_DB_SER_SECURITY_SECONN
```

Authenticated LE secure connections that generates 16bytes LTK(Security Mode1 Security Level 4). Authenticated LE secure connections pairing that generates 16bytes LTK is required to access the service. If this bit is set, bit24-27 are ignored.

```
#define BLE_GATT_DB_SER_SECURITY_ENC  
Encryption. Encryption by the LTK exchanged in pairing is required to access.
```

```
#define BLE_GATT_DB_SER_NO_SECURITY_PROPERTY  
No Security(Security Mode1 Security Level 1).
```

```
#define BLE_GATT_DB_SER_ENC_KEY_SIZE_DONT_CARE  
7-byte or larger encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_7  
7-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_8  
8-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_9  
9-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_10  
10-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_11  
11-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_12  
12-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_13  
13-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_14  
14-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_15
    15-byte encryption key.
```

```
#define BLE_GATT_DB_SER_ENCRYPT_KEY_SIZE_16
    16-byte encryption key.
```

## Typedefs

```
typedef void(* ble_gatts_app_cb_t) (uint16_t event_type, ble_status_t event_result,
    st_ble_gatts_evt_data_t *p_event_data)

ble_gatts_app_cb_t is the GATT Server Event callback function type.
More...
```

## Enumerations

```
enum e_r_ble_gatts_evt_t
    GATT Server Event Identifier. More...
```

## Data Structure Documentation

### ◆ st\_ble\_gatt\_value\_t

struct st_ble_gatt_value_t		
Attribute Value.		
Data Fields		
uint16_t	value_len	Length of the attribute value.
uint8_t *	p_value	Attribute Value.

### ◆ st\_ble\_gatt\_hdl\_value\_pair\_t

struct st_ble_gatt_hdl_value_pair_t		
Attribute handle and attribute Value.		
Data Fields		
uint16_t	attr_hdl	Attribute Handle.
<a href="#">st_ble_gatt_value_t</a>	value	Attribute Value.

### ◆ st\_ble\_gatt\_queue\_att\_val\_t

struct st_ble_gatt_queue_att_val_t		
Queued writes Attribute Value.		
Data Fields		

uint8_t *	p_value	Attribute Value for Queued Write .
uint16_t	value_len	Length of the attribute value.
uint16_t	padding	padding.

#### ◆ st\_ble\_gatt\_queue\_pair\_t

struct st_ble_gatt_queue_pair_t		
Queued writes Attribute Value.		
Data Fields		
st_ble_gatt_queue_att_val_t	queue_value	Attribute Value for Queued Write.
uint16_t	attr_hdl	Attribute Handle.

#### ◆ st\_ble\_gatt\_queue\_elm\_t

struct st_ble_gatt_queue_elm_t		
Prepare Write Queue element for long characteristic.		
Data Fields		
st_ble_gatt_queue_pair_t	queue_value_pair	Part of Long Characteristic Value and Characteristic Value Handle.
uint16_t	offset	Offset that indicates the location to be written.

#### ◆ st\_ble\_gatt\_pre\_queue\_t

struct st_ble_gatt_pre_queue_t		
Prepare Write Queue for long characteristic.		
Data Fields		
uint8_t *	p_buf_start	Buffer start address for Write Long Characteristic Request.
st_ble_gatt_queue_elm_t *	p_queue	Prepare Write Queue for Long Characteristic Value.
uint16_t	buffer_len	Buffer length.
uint16_t	conn_hdl	Connection Handle.
uint16_t	buf_offset	Current buffer offset.
uint8_t	queue_size	Number of elements in the prepare write queue.
uint8_t	queue_idx	Index of Prepare Write Queue.

#### ◆ st\_ble\_gatts\_db\_params\_t

struct st_ble_gatts_db_params_t		
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Attribute value to be set to or retrieved from the GATT Database and the access type from the GATT Client.		
Data Fields		
<a href="#">st_ble_gatt_value_t</a>	value	Attribute value to be set to or retrieved from the GATT Database. Note that the address of the value field in the value field is invalid in case of read access.
uint16_t	attr_hdl	Attribute handle identifying the attribute to be set or retrieved.
uint8_t	db_op	Type of the access to GATT Database from the GATT Client.  See also <a href="#">access_type_to_gatt_database</a>

#### ◆ [st\\_ble\\_gatts\\_db\\_conn\\_hdl\\_t](#)

struct <a href="#">st_ble_gatts_db_conn_hdl_t</a>		
Information about the service or the characteristic that the attribute belongs to.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the GATT Client that accesses to the GATT DataBase.
uint8_t	service_id	ID of the service that the attribute belongs to.
uint8_t	char_id	ID of the Characteristic that the attribute belongs to.

#### ◆ [st\\_ble\\_gatts\\_db\\_access\\_evt\\_t](#)

struct <a href="#">st_ble_gatts_db_access_evt_t</a>		
This structure notifies that the GATT Database has been accessed from a GATT Client.		
Data Fields		
<a href="#">st_ble_gatts_db_conn_hdl_t</a> *	p_handle	Information about the service or the characteristic that the attribute belongs to.
<a href="#">st_ble_gatts_db_params_t</a> *	p_params	Attribute value to be set to or retrieved from the GATT Database and the access type from the GATT Client.

#### ◆ [st\\_ble\\_gatts\\_conn\\_evt\\_t](#)

struct <a href="#">st_ble_gatts_conn_evt_t</a>		
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This structure notifies that the link with the GATT Client has been established.

Data Fields		
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<code>st_ble_dev_addr_t*</code>	<code>p_addr</code>	Address of the GATT Client.
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#### ◆ `st_ble_gatts_disconn_evt_t`

<code>struct st_ble_gatts_disconn_evt_t</code>
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This structure notifies that the link with the GATT Client has been disconnected.

Data Fields		
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<code>st_ble_dev_addr_t*</code>	<code>p_addr</code>	Address of the GATT Client.
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#### ◆ `st_ble_gatts_ex_mtu_req_evt_t`

<code>struct st_ble_gatts_ex_mtu_req_evt_t</code>
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This structure notifies that a MTU Exchange Request PDU has been received from a GATT Client.

Data Fields		
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<code>uint16_t</code>	<code>mtu</code>	Maximum receive MTU size by GATT Client.
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#### ◆ `st_ble_gatts_cfm_evt_t`

<code>struct st_ble_gatts_cfm_evt_t</code>
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This structure notifies that a Confirmation PDU has been received from a GATT Client.

Data Fields		
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<code>uint16_t</code>	<code>attr_hdl</code>	Attribute handle identifying the Characteristic sent by the Indication PDU.
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#### ◆ `st_ble_gatts_read_by_type_rsp_evt_t`

<code>struct st_ble_gatts_read_by_type_rsp_evt_t</code>
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This structure notifies that a Read By Type Response PDU has been sent from GATT Server.

Data Fields		
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<code>uint16_t</code>	<code>attr_hdl</code>	Attribute handle identifying the Characteristic read by the Read By Type Request PDU.
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#### ◆ `st_ble_gatts_read_rsp_evt_t`

<code>struct st_ble_gatts_read_rsp_evt_t</code>
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This structure notifies that a Read Response PDU has been sent from GATT Server.

Data Fields		
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<code>uint16_t</code>	<code>attr_hdl</code>	Attribute handle identifying the Characteristic read by the Read Request PDU.
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◆ **st\_ble\_gatts\_read\_blob\_rsp\_evt\_t**

struct st_ble_gatts_read_blob_rsp_evt_t		
This structure notifies that a Read Blob Response PDU has been sent from GATT Server.		
Data Fields		
uint16_t	attr_hdl	Attribute handle identifying the Characteristic read by the Read Blob Request PDU.

◆ **st\_ble\_gatts\_read\_multi\_rsp\_evt\_t**

struct st_ble_gatts_read_multi_rsp_evt_t		
This structure notifies that a Read Multiple Response PDU has been sent from GATT Server.		
Data Fields		
uint8_t	count	The number of attribute read by the Read Multiple Request PDU.
uint16_t*	p_attr_hdl_list	The list of attribute read by the Read Multiple Request PDU.

◆ **st\_ble\_gatts\_write\_rsp\_evt\_t**

struct st_ble_gatts_write_rsp_evt_t		
This structure notifies that a Write Response PDU has been sent from GATT Server.		
Data Fields		
uint16_t	attr_hdl	Attribute handle identifying the Characteristic written by the Write Request PDU.

◆ **st\_ble\_gatts\_prepare\_write\_rsp\_evt\_t**

struct st_ble_gatts_prepare_write_rsp_evt_t		
This structure notifies that a Prepare Write Response PDU has been sent from GATT Server.		
Data Fields		
uint16_t	attr_hdl	Attribute handle identifying the Characteristic written by the Prepare Write Request PDU.
uint16_t	length	The length of written bytes by the Prepare Write Request PDU.
uint16_t	offset	The offset of the first octet to be written.

◆ **st\_ble\_gatts\_exe\_write\_rsp\_evt\_t**

struct st_ble_gatts_exe_write_rsp_evt_t		
This structure notifies that a Execute Write Response PDU has been sent from GATT Server.		
Data Fields		

uint8_t	exe_flag	The flag that indicates whether execution or cancellation.	
		value	description
		0x00	Cancellation.
		0x01	Execution.

#### ◆ st\_ble\_gatts\_db\_uuid\_cfg\_t

struct st_ble_gatts_db_uuid_cfg_t		
A structure that defines the information on the position where UUIDs are used.		
Data Fields		
uint16_t	offset	The position of the defined UUID is specified by offset value in uuid_table of <a href="#">st_ble_gatts_db_cfg_t</a> .
uint16_t	first	The attribute handle that indicates the first position in <a href="#">st_ble_gatts_db_attr_cfg_t</a> for the defined UUID is specified.
uint16_t	last	The attribute handle that indicates the last position in <a href="#">st_ble_gatts_db_attr_cfg_t</a> for the defined UUID is specified.

#### ◆ st\_ble\_gatts\_db\_attr\_cfg\_t

struct st_ble_gatts_db_attr_cfg_t			
A structure that defines the detailed information of the attributes.			
Data Fields			
uint8_t	desc_prop	The properties of attribute are specified.	
		Set the following properties by a bitwise OR.	
		macro	description
		<a href="#">BLE_GATT_DB_READ(0x01)</a>	Allow clients to read.
		<a href="#">BLE_GATT_DB_WRITE(0x02)</a>	Allow clients to write.
<a href="#">BLE_GATT_DB_WRITE_WITH_OUT_RSP(0x04)</a>	Allow clients to write.		
<a href="#">BLE_GATT_DB</a>	Allow clients		

		<p><code>_READ_WRITE (0x07)</code> to access of all.</p>														
<p>uint8_t</p>	<p>aux_prop</p>	<p>The auxiliary properties of attribute are specified.</p> <p>Set the following properties by a bitwise OR.</p> <table border="1" data-bbox="1034 501 1473 555"> <thead> <tr> <th data-bbox="1034 501 1254 555">macro</th> <th data-bbox="1254 501 1473 555">description</th> </tr> </thead> <tbody> <tr> <td data-bbox="1034 566 1254 696"> <p><code>BLE_GATT_DB_NO_AUXILIARY_PROPERTY(0x00)</code></p> </td> <td data-bbox="1254 566 1473 831"> <p>No auxiliary properties. It is invalid when used with other properties at the same time.</p> </td> </tr> <tr> <td data-bbox="1034 853 1254 983"> <p><code>BLE_GATT_DB_FIXED_LENGTH_PROPERTY(0x01)</code></p> </td> <td data-bbox="1254 853 1473 952"> <p>Fixed length attribute value.</p> </td> </tr> <tr> <td data-bbox="1034 1005 1254 1135"> <p><code>BLE_GATT_DB_AUTHORIZATION_PROPERTY(0x02)</code></p> </td> <td data-bbox="1254 1005 1473 1104"> <p>Attributes requiring authorization.</p> </td> </tr> <tr> <td data-bbox="1034 1158 1254 1256"> <p><code>BLE_GATT_DB_ATTR_DISABLED(0x10)</code></p> </td> <td data-bbox="1254 1158 1473 1655"> <p>The attribute is disabled. If this value is set, the attribute cannot be found and accessed by a GATT Client. It is invalid when used with other properties at the same time.</p> </td> </tr> <tr> <td data-bbox="1034 1677 1254 1807"> <p><code>BLE_GATT_DB_128_BIT_UUID_FORMAT(0x20)</code></p> </td> <td data-bbox="1254 1677 1473 1910"> <p>Attribute with 128 bit UUID. If this macro is not set, the attribute value is 16-bits UUID.</p> </td> </tr> <tr> <td data-bbox="1034 1933 1254 2031"> <p><code>BLE_GATT_DB_PEER_SPECIFIC_VALUE_PROPERTY</code></p> </td> <td data-bbox="1254 1933 1473 2031"> <p>Attribute managed by each GATT</p> </td> </tr> </tbody> </table>	macro	description	<p><code>BLE_GATT_DB_NO_AUXILIARY_PROPERTY(0x00)</code></p>	<p>No auxiliary properties. It is invalid when used with other properties at the same time.</p>	<p><code>BLE_GATT_DB_FIXED_LENGTH_PROPERTY(0x01)</code></p>	<p>Fixed length attribute value.</p>	<p><code>BLE_GATT_DB_AUTHORIZATION_PROPERTY(0x02)</code></p>	<p>Attributes requiring authorization.</p>	<p><code>BLE_GATT_DB_ATTR_DISABLED(0x10)</code></p>	<p>The attribute is disabled. If this value is set, the attribute cannot be found and accessed by a GATT Client. It is invalid when used with other properties at the same time.</p>	<p><code>BLE_GATT_DB_128_BIT_UUID_FORMAT(0x20)</code></p>	<p>Attribute with 128 bit UUID. If this macro is not set, the attribute value is 16-bits UUID.</p>	<p><code>BLE_GATT_DB_PEER_SPECIFIC_VALUE_PROPERTY</code></p>	<p>Attribute managed by each GATT</p>
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		<p>RTY(0x40) Client.</p> <p>BLE_GATT_DB_FIXED_ATTR_VAL_PROPERTY(0x80) Fixed attribute value. Writing from Client and setting from Server are prohibited.</p>
uint16_t	length	The length of the attribute value is specified.
uint16_t	next	The position of the next attribute with the same UUID as the defined attribute is specified by an attribute handle.
uint16_t	uuid_offset	<p>The storage area of attribute value.</p> <p>UUID of the defined attribute is set by specifying the position of the UUID registered in <code>uuid_table</code> of <code>st_ble_gatts_db_cfg_t</code> with the array offset value.</p>
uint8_t *	p_data_offset	<p>Storage area of attribute value.</p> <p>The address in the array registered in No.1-No.4 is specified to set the attribute value storage area of the defined attribute.</p>

#### ◆ st\_ble\_gatts\_db\_attr\_list\_t

struct st_ble_gatts_db_attr_list_t		
The number of attributes are stored.		
Data Fields		
uint8_t	count	The number of the services or the characteristics.

#### ◆ st\_ble\_gatts\_db\_char\_cfg\_t

struct st_ble_gatts_db_char_cfg_t		
A structure that defines the detailed information of the characteristics.		
Data Fields		
st_ble_gatts_db_attr_list_t	list	The total number of attributes in the defined characteristic is

		specified.
uint16_t	start_hdl	The first attribute handle of the characteristic is specified.
uint8_t	service_id	The index of service to which the characteristic belongs is specified.

#### ◆ st\_ble\_gatts\_db\_serv\_cfg\_t

struct st_ble_gatts_db_serv_cfg_t								
A structure that defines the detailed information of the characteristics.								
Data Fields								
st_ble_gatts_db_attr_list_t	list	The total number of service declarations in the defined service is specified.						
uint32_t	desc	<p>The properties of the defined service are specified.</p> <p>Set the security level, the security mode and the key size with a bitwise OR. The bit0-bit3 are specified as the security level. Select one of the following.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GATT_DB_SER_SECURITY_UNAUTH(0x00000001)</a></td> <td>Unauthenticated pairing(Security Mode1 Security Level 2, Security Mode 2 Security Level 1) Unauthenticated pairing is required to access the service.</td> </tr> <tr> <td><a href="#">BLE_GATT_DB_SER_SECURITY_AUTH(0x00000002)</a></td> <td>Authenticated pairing(Security Mode1 Security Level 3, Security Mode 2 Security Level 2) Authenticated pairing is required to</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GATT_DB_SER_SECURITY_UNAUTH(0x00000001)</a>	Unauthenticated pairing(Security Mode1 Security Level 2, Security Mode 2 Security Level 1) Unauthenticated pairing is required to access the service.	<a href="#">BLE_GATT_DB_SER_SECURITY_AUTH(0x00000002)</a>	Authenticated pairing(Security Mode1 Security Level 3, Security Mode 2 Security Level 2) Authenticated pairing is required to
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<a href="#">BLE_GATT_DB_SER_SECURITY_AUTH(0x00000002)</a>	Authenticated pairing(Security Mode1 Security Level 3, Security Mode 2 Security Level 2) Authenticated pairing is required to							

access the service.

**BLE\_GATT\_DB\_SER\_SECURITY\_SECONN(0x00000004)** Authenticated LE secure connections that generates 16bytes LTK(Security Mode1 Security Level 4) Authenticated LE secure connections pairing that generates 16bytes LTK is required to access the service. If this bit is set, bit24-27 are ignored.

The bit4 is specified as the security mode.

macro	description
<b>BLE_GATT_DB_SER_SECURITY_ENC(0x00000010)</b>	Encryption Encryption by the LTK exchanged in pairing is required to access.

If the security requirement of the service is not needed, specify the bit0-bit4 to **BLE\_GATT\_DB\_SER\_NO\_SECURITY\_PROPERTY(0x00000000)** (Security Mode1 Security Level 1)

The bit24-bit27 are specified as the key size required by the defined service.

Select one of the following.

macro	description
<b>BLE_GATT_DB_SER_ENCRYP</b>	7-byte encryption

T_KEY_SIZE_7(0x01000000)	key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_8(0x02000000)	8-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_9(0x03000000)	9-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_10(0x04000000)	10-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_11(0x05000000)	11-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_12(0x06000000)	12-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_13(0x07000000)	13-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_14(0x08000000)	14-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_15(0x09000000)	15-byte encryption key.
BLE_GATT_DB_SER_ENCRYP_T_KEY_SIZE_16(0x0A000000)	16-byte encryption key.
BLE_GATT_DB_SER_ENC_KEY_SIZE_DONT_CARE(0x0000)	7-byte or larger encryption key.

		0000) Other bits are reserved.
uint16_t	start_hdl	The start attribute handle of the defined service is specified.
uint16_t	end_hdl	The end attribute handle of the defined service is specified.
uint8_t	char_start_idx	The start index of the characteristic that belongs to the defined service is specified.
uint8_t	char_end_idx	The end index of the characteristic that belongs to the defined service is specified.

#### ◆ st\_ble\_gatts\_db\_cfg\_t

struct st_ble_gatts_db_cfg_t		
This is the structure of GATT Database that is specified in <a href="#">R_BLE_GATTS_SetDbInst()</a> .		
Data Fields		
const uint8_t *	p_uuid_table	The array to register the UUID to be used.
uint8_t *	p_attr_val_table	The array to register variable attribute values.
const uint8_t *	p_const_attr_val_table	The array to register fixed attribute values.
uint8_t *	p_rem_spec_val_table	The array to manage the attribute values handled for each GATT client.
const uint8_t *	p_const_rem_spec_val_table	The array to register the default of the attribute value handled by each GATT client.
const <a href="#">st_ble_gatts_db_uuid_cfg_t</a> *	p_uuid_cfg	The array to register information on the position where UUIDs are used.
const <a href="#">st_ble_gatts_db_attr_cfg_t</a> *	p_attr_cfg	The array to register the detailed information of attributes.
const <a href="#">st_ble_gatts_db_char_cfg_t</a> *	p_char_cfg	The array to register the detailed information of characteristics.
const <a href="#">st_ble_gatts_db_serv_cfg_t</a> *	p_serv_cfg	The array to register the detailed information of services.
uint8_t	serv_cnt	The number of services included in the GATT Database.

uint8_t	char_cnt	The number of characteristics included in the GATT Database.
uint8_t	uuid_type_cnt	The number of UUIDs included in the GATT Database.
uint8_t	peer_spec_val_cnt	The total size of attribute value that needs to be managed for each GATT client.

#### ◆ st\_ble\_gatts\_evt\_data\_t

struct st_ble_gatts_evt_data_t		
st_ble_gatts_evt_data_t is the type of the data notified in a GATT Server Event.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the GATT Client.
uint16_t	param_len	The size of GATT Server Event parameters.
void *	p_param	GATT Server Event parameters. This parameter differs in each GATT Server Event.

### Typedef Documentation

#### ◆ ble\_gatts\_app\_cb\_t

ble_gatts_app_cb_t		
ble_gatts_app_cb_t is the GATT Server Event callback function type.		
<b>Parameters</b>		
[in]	event_type	The type of GATT Server Event.
[in]	event_result	The result of GATT Server Event
[in]	p_event_data	Data notified by GATT Server Event.
<b>Returns</b>		
none		

### Enumeration Type Documentation

## ◆ e\_r\_ble\_gatts\_evt\_t

enum e_r_ble_gatts_evt_t	
GATT Server Event Identifier.	
Enumerator	
BLE_GATTS_EVENT_EX_MTU_REQ	<p>MTU Exchange Request has been received.</p> <p>This event notifies the application layer that a MTU Exchange Request PDU has been received from a GATT Client. Need to reply to the request by <a href="#">R_BLE_GATTS_RspExMtu()</a>.</p> <p><b>Event Code: 0x3002</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_ex_mtu_req_evt_tBLE_GATTS_EVENT_EX_MTU_REQ</p>
BLE_GATTS_EVENT_READ_BY_TYPE_RSP_COMP	<p>Read By Type Response has been sent.</p> <p>This event notifies the application layer that a Read By Type Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x3009</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_read_by_type_rsp_evt_tBLE_GATTS_EVENT_READ_BY_TYPE_RSP_COMP</p>
BLE_GATTS_EVENT_READ_RSP_COMP	<p>Read Response has been sent.</p> <p>This event notifies the application layer that a Read Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x300B</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_read_rsp_evt_tBLE_GATTS_EVENT_READ_RSP_COMP</p>
BLE_GATTS_EVENT_READ_BLOB_RSP_COMP	<p>Read Blob Response has been sent.</p> <p>This event notifies the application layer that a Read Blob Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x300D</b></p> <p><b>Event Data:</b></p>

	st_ble_gatts_read_blob_rsp_evt_tBLE_GATTS_EVENT_READ_BLOB_RSP_COMP
BLE_GATTS_EVENT_READ_MULTI_RSP_COMP	<p>Read Multiple Response has been sent.</p> <p>This event notifies the application layer that a Read Multiple Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x300F</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_read_multi_rsp_evt_tBLE_GATTS_EVENT_READ_MULTI_RSP_COMP</p>
BLE_GATTS_EVENT_WRITE_RSP_COMP	<p>Write Response has been sent.</p> <p>This event notifies the application layer that a Write Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x3013</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_write_rsp_evt_tBLE_GATTS_EVENT_WRITE_RSP_COMP</p>
BLE_GATTS_EVENT_PREPARE_WRITE_RSP_COMP	<p>Prepare Write Response has been sent.</p> <p>This event notifies the application layer that a Prepare Write Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x3017</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_prepare_write_rsp_evt_tBLE_GATTS_EVENT_PREPARE_WRITE_RSP_COMP</p>
BLE_GATTS_EVENT_EXE_WRITE_RSP_COMP	<p>Execute Write Response has been sent.</p> <p>This event notifies the application layer that a Execute Write Response PDU has been sent from GATT Server to the GATT Client.</p> <p><b>Event Code: 0x3019</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_exe_write_rsp_evt_tBLE_GATTS_EVENT_EXE_WRITE_RSP_COMP</p>
BLE_GATTS_EVENT_HDL_VAL_CNF	<p>Confirmation has been received.</p> <p>This event notifies the application layer that a</p>

	<p>Confirmation PDU has been received from a GATT Client.</p> <p><b>Event Code: 0x301E</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_cfm_evt_tBLE_GATTS_EVENT_HDL_VAL_CNF</p>
BLE_GATTS_EVENT_DB_ACCESS_IND	<p>The GATT Database has been accessed from a GATT Client.</p> <p>This event notifies the application layer that the GATT Database has been accessed from a GATT Client.</p> <p><b>Event Code: 0x3040</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_db_access_evt_tBLE_GATTS_EVENT_DB_ACCESS_IND</p>
BLE_GATTS_EVENT_CONN_IND	<p>A connection has been established.</p> <p>This event notifies the application layer that the link with the GATT Client has been established.</p> <p><b>Event Code: 0x3081</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_conn_evt_tBLE_GATTS_EVENT_CONN_IND</p>
BLE_GATTS_EVENT_DISCONN_IND	<p>A connection has been disconnected.</p> <p>This event notifies the application layer that the link with the GATT Client has been disconnected.</p> <p><b>Event Code: 0x3082</b></p> <p><b>Event Data:</b></p> <p>st_ble_gatts_disconn_evt_tBLE_GATTS_EVENT_DISCONN_IND</p>
BLE_GATTS_EVENT_INVALID	<p>Invalid GATT Server Event.</p> <p><b>Event Code: 0x30FF</b></p> <p><b>Event Data:</b></p> <p>noneBLE_GATTS_EVENT_INVALID</p>

## Function Documentation

### ◆ R\_BLE\_GATTS\_Init()

```
ble_status_t R_BLE_GATTS_Init ( uint8_t cb_num)
```

This function initializes the GATT Server and registers the number of the callbacks for GATT Server event.

Specify the `cb_num` parameter to a value between 1 and `BLE_GATTS_MAX_CB`.

[R\\_BLE\\_GATTS\\_RegisterCb\(\)](#) registers the callback.

The result of this API call is returned by a return value.

#### Parameters

[in]	<code>cb_num</code>	The number of callbacks to be registered.
------	---------------------	---

#### Return values

<code>BLE_SUCCESS(0x0000)</code>	Success
<code>BLE_ERR_INVALID_ARG(0x0003)</code>	The <code>cb_num</code> parameter is out of range.

### ◆ R\_BLE\_GATTS\_SetDbInst()

```
ble_status_t R_BLE_GATTS_SetDbInst ( st_ble_gatts_db_cfg_t * p_db_inst)
```

This function sets GATT Database to host stack.

The result of this API call is returned by a return value.

#### Parameters

[in]	<code>p_db_inst</code>	GATT Database to be set.
------	------------------------	--------------------------

#### Return values

<code>BLE_SUCCESS(0x0000)</code>	Success
<code>BLE_ERR_INVALID_PTR(0x0001)</code>	The reason for this error is as follows. <ul style="list-style-type: none"> <li>• The <code>db_inst</code> parameter is specified as NULL.</li> <li>• The array in the <code>db_inst</code> is specified as NULL.</li> </ul>

◆ **R\_BLE\_GATTS\_RegisterCb()**

```
ble_status_t R_BLE_GATTS_RegisterCb ( ble_gatts_app_cb_t cb, uint8_t priority )
```

This function registers a callback for GATT Server event.

The number of the callback that may be registered by this function is the value specified by [R\\_BLE\\_GATTS\\_Init\(\)](#).

The result of this API call is returned by a return value.

**Parameters**

[in]	cb	Callback function for GATT Server event.
[in]	priority	The priority of the callback function. Valid range is $1 \leq \text{priority} \leq \text{BLE\_GATTS\_MAX\_CB}$ . A lower priority number means a higher priority level.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The cb parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The priority parameter is out of range.
BLE_ERR_CONTEXT_FULL(0x000B)	Host stack has already registered the maximum number of callbacks.

◆ **R\_BLE\_GATTS\_DeregisterCb()**

```
ble_status_t R_BLE_GATTS_DeregisterCb ( ble_gatts_app_cb_t cb)
```

This function deregisters the callback function for GATT Server event.

The result of this API call is returned by a return value.

**Parameters**

[in]	cb	The callback function to be deregistered.
------	----	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The cb parameter is specified as NULL.
BLE_ERR_NOT_FOUND(0x000D)	The callback has not been registered.

◆ **R\_BLE\_GATTS\_Notification()**

```
ble_status_t R_BLE_GATTS_Notification ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t *
p_ntf_data )
```

This function sends a notification of an attribute's value.

The maximum length of the attribute value that can be sent with notification is MTU-3.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to be sent the notification.
[in]	p_ntf_data	The attribute value to send.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_ntf_data parameter or the value field in the value field in the p_ntf_data parameter is NULL.
BLE_ERR_INVALID_ARG(0x0003)	The value_len field in the value field in the p_ntf_data parameter is 0 or the attr_hdl field in the p_ntf_data parameters is 0.
BLE_ERR_INVALID_OPERATION(0x0009)	This function was called while processing other request.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTS\_Indication()

```
ble_status_t R_BLE_GATTS_Indication ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t *
p_ind_data )
```

This function sends a indication of an attribute's value.

The maximum length of the attribute value that can be sent with indication is MTU-3.

The result of this API call is returned by a return value.

The remote device that receives a indication sends a confirmation.

BLE\_GATTS\_EVENT\_HDL\_VAL\_CNF event notifies the application layer that the confirmation has been received.

#### Parameters

[in]	conn_hdl	Connection handle identifying the remote device to be sent the indication.
[in]	p_ind_data	The attribute value to send.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_ind_data parameter or the value field in the value field in the p_ind_data parameter is NULL.
BLE_ERR_INVALID_ARG(0x0003)	The value_len field in the value field in the p_ind_data parameter is 0 or the attr_hdl field in the p_ind_data parameters is 0.
BLE_ERR_INVALID_OPERATION(0x0009)	This function was called while processing other request.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTS\_GetAttr()

```
ble_status_t R_BLE_GATTS_GetAttr ( uint16_t conn_hdl, uint16_t attr_hdl, st_ble_gatt_value_t *
p_value )
```

This function gets a attribute value from the GATT Database.

The result of this API call is returned by a return value.

#### Parameters

[in]	conn_hdl	If the attribute value that has information about the remote device is retrieved, specify the remote device with the conn_hdl parameter. When information about the remote device is not required, set the conn_hdl parameter to BLE_GAP_INVALID_CONN_HDL.
[in]	attr_hdl	The attribute handle of the attribute value to be retrieved.
[out]	p_value	The attribute value to be retrieved.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_value parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The attr_hdl parameter is 0 or larger than the last attribute handle of GATT Database.
BLE_ERR_INVALID_STATE(0x0008)	The attribute is not in a state to be read.
BLE_ERR_INVALID_OPERATION(0x0009)	The attribute cannot be read.
BLE_ERR_NOT_FOUND(0x000D)	The attribute specified by the attr_hdl parameter is not belonging to any services or characteristics.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by the conn_hdl parameter was not found.

### ◆ R\_BLE\_GATTS\_SetAttr()

```
ble_status_t R_BLE_GATTS_SetAttr ( uint16_t conn_hdl, uint16_t attr_hdl, st_ble_gatt_value_t *
p_value )
```

This function sets an attribute value to the GATT Database.

The result of this API call is returned by a return value.

#### Parameters

[in]	conn_hdl	If the attribute value that has information about the remote device is retrieved, specify the remote device with the conn_hdl parameter. When information about the remote device is not required, set the conn_hdl parameter to BLE_GAP_INVALID_CONN_HDL.
[in]	attr_hdl	The attribute handle of the attribute value to be set.
[in]	p_value	The attribute value to be set.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_value parameter is specified as NULL.
BLE_ERR_INVALID_DATA(0x0002)	The write size is larger than the length of the attribute value.
BLE_ERR_INVALID_ARG(0x0003)	The attr_hdl parameter is 0 or larger than the last attribute handle of GATT Database.
BLE_ERR_INVALID_STATE(0x0008)	The attribute is not in a state to be written.
BLE_ERR_INVALID_OPERATION(0x0009)	The attribute cannot be written.
BLE_ERR_NOT_FOUND(0x000D)	The attribute specified by the attr_hdl parameter is not belonging to any services or characteristics.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by the conn_hdl parameter was not found.

### ◆ R\_BLE\_GATTS\_SendErrRsp()

```
ble_status_t R_BLE_GATTS_SendErrRsp ( uint16_t error_code)
```

This function sends an error response to a remote device.

The result is returned from the API.  
 The error code specified in the callback is notified as Error Response to the remote device.  
 The result of this API call is returned by a return value.

### Parameters

[in]	error_code	The error codes to be notified the client. It is a bitwise OR of GATT Error Group ID : 0x3000 and the following error codes defined in Core Spec and Core Spec Supplement.		
		<table border="1"> <thead> <tr> <th data-bbox="1074 629 1273 689">Error Code</th> <th data-bbox="1273 629 1469 689">description</th> </tr> </thead> </table>	Error Code	description
Error Code	description			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 689 1273 846">BLE_ERR_GATT_INVALID_HANDLE(0x3001)</td> <td data-bbox="1273 689 1469 846">Invalid attribute handle</td> </tr> </tbody> </table>	BLE_ERR_GATT_INVALID_HANDLE(0x3001)	Invalid attribute handle
BLE_ERR_GATT_INVALID_HANDLE(0x3001)	Invalid attribute handle			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 846 1273 1003">BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)</td> <td data-bbox="1273 846 1469 1003">The attribute cannot be read.</td> </tr> </tbody> </table>	BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)	The attribute cannot be read.
BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)	The attribute cannot be read.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1003 1273 1160">BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)</td> <td data-bbox="1273 1003 1469 1160">The attribute cannot be written.</td> </tr> </tbody> </table>	BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)	The attribute cannot be written.
BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)	The attribute cannot be written.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1160 1273 1317">BLE_ERR_GATT_INVALID_PDU(0x3004)</td> <td data-bbox="1273 1160 1469 1317">Invalid PDU.</td> </tr> </tbody> </table>	BLE_ERR_GATT_INVALID_PDU(0x3004)	Invalid PDU.
BLE_ERR_GATT_INVALID_PDU(0x3004)	Invalid PDU.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1317 1273 1496">BLE_ERR_GATT_INSUFFICIENT_AUTHENTICATION(0x3005)</td> <td data-bbox="1273 1317 1469 1496">The authentication to access the attribute is insufficient.</td> </tr> </tbody> </table>	BLE_ERR_GATT_INSUFFICIENT_AUTHENTICATION(0x3005)	The authentication to access the attribute is insufficient.
BLE_ERR_GATT_INSUFFICIENT_AUTHENTICATION(0x3005)	The authentication to access the attribute is insufficient.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1496 1273 1675">BLE_ERR_GATT_REQUEST_NOT_SUPPORTED(0x3006)</td> <td data-bbox="1273 1496 1469 1675">The request is not supported.</td> </tr> </tbody> </table>	BLE_ERR_GATT_REQUEST_NOT_SUPPORTED(0x3006)	The request is not supported.
BLE_ERR_GATT_REQUEST_NOT_SUPPORTED(0x3006)	The request is not supported.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1675 1273 1944">BLE_ERR_GATT_INVALID_OFFSET(0x3007)</td> <td data-bbox="1273 1675 1469 1944">The specified offset is larger than the length of the attribute value.</td> </tr> </tbody> </table>	BLE_ERR_GATT_INVALID_OFFSET(0x3007)	The specified offset is larger than the length of the attribute value.
BLE_ERR_GATT_INVALID_OFFSET(0x3007)	The specified offset is larger than the length of the attribute value.			
		<table border="1"> <tbody> <tr> <td data-bbox="1074 1944 1273 2045">BLE_ERR_GATT_INSUFFICIENT_AUTHORIZATION(0x3008)</td> <td data-bbox="1273 1944 1469 2045">Authorization is required to access</td> </tr> </tbody> </table>	BLE_ERR_GATT_INSUFFICIENT_AUTHORIZATION(0x3008)	Authorization is required to access
BLE_ERR_GATT_INSUFFICIENT_AUTHORIZATION(0x3008)	Authorization is required to access			

			RIZATION(0x3008)	the attribute.
			BLE_ERR_GATT_PREPARE_WRITE_QUEUE_FULL(0x3009)	The Write Queue in the GATT Server is full.
			BLE_ERR_GATT_ATTRIBUTE_NOT_FOUND(0x300A)	The specified attribute is not found.
			BLE_ERR_GATT_ATTRIBUTE_NOT_READABLE(0x300B)	The attribute cannot be read by Read Blob Request.
			BLE_ERR_GATT_INSUFFICIENT_KEY_SIZE(0x300C)	The Encryption Key Size is insufficient.
			BLE_ERR_GATT_INVALID_ATTRIBUTE_LENGTH(0x300D)	The length of the specified attribute is invalid.
			BLE_ERR_GATT_UNLIKELY_ERROR(0x300E)	Because an error has occurred, the process cannot be advanced.
			BLE_ERR_GATT_INSUFFICIENT_ENCRYPTION(0x300F)	Encryption is required to access the attribute.
			BLE_ERR_GATT_UNSUPPORTED_GROUP_TYPE(0x3010)	The type of the specified attribute is not supported.
			BLE_ERR_GATT_INSUFFICIENT_RESOURCES(0x3011)	The resource to complete the request is insufficient.
			0x3080 -	Application

			0x309F	Error. The upper layer defines the error codes.
			0x30E0 - 0x30FF	The error code defined in Common Profile and Service Error Core Specification Supplement(CSS). CSS ver.7 defines the error codes from 0x30FC to 0x30FF.
			BLE_ERR_GATT_WRITE_REQUEST_REJECTED(0x30FC)	The Write Request has not been completed due to the reason other than Permission.
			BLE_ERR_GATT_CCCD_IMPROPERLY_CONFIGURED(0x30FD)	The CCCD is set to be invalid.
			BLE_ERR_GATT_PROC_ALREADY_IN_PROGRESS(0x30FE)	The request is now in progress.
			BLE_ERR_GATT_OUT_OF_RANGE(0x30FF)	The attribute value is out of range.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The Group ID of the error_code parameter is not 0x3000, or it is 0x3000.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other error response, this function was called.

◆ **R\_BLE\_GATTS\_RspExMtu()**

```
ble_status_t R_BLE_GATTS_RspExMtu ( uint16_t conn_hdl, uint16_t mtu )
```

This function replies to a MTU Exchange Request from a remote device.

BLE\_GATTS\_EVENT\_EX\_MTU\_REQ event notifies the application layer that a MTU Exchange Request has been received. Therefore when the callback has received the event, call this function.

The new MTU is the minimum of the mtu parameter specified by this function and the mtu field in BLE\_GATTS\_EVENT\_EX\_MTU\_REQ event.

Default MTU size is 23 bytes.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to be sent MTU Exchange Response.
[in]	mtu	The maximum size(in bytes) of the GATT PDU that GATT Server can receive. Valid range is 23 <= mtu <= 247.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The mtu parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	This function was called while processing other request.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTS\_SetPrepareQueue()

```
ble_status_t R_BLE_GATTS_SetPrepareQueue ( st_ble_gatt_pre_queue_t * p_pre_queues, uint8_t queue_num )
```

Register prepare queue and buffer in Host Stack.

This function registers the prepare queue and buffer for long characteristic write and reliable writes. The result of this API call is returned by a return value.

#### Parameters

[in]	p_pre_queues	The prepare write queues to be registered.
[in]	queue_num	The number of prepare write queues to be registered.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_pre_queue parameter is specified as NULL.

## 4.2.5.4 GATT\_CLIENT

Modules » [Bluetooth Low Energy Library \(r\\_ble\)](#)

### Functions

ble\_status\_t [R\\_BLE\\_GATTC\\_Init](#) (uint8\_t cb\_num)

This function initializes the GATT Client and registers the number of the callbacks for GATT Client event. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_RegisterCb](#) (ble\_gattc\_app\_cb\_t cb, uint8\_t priority)

This function registers a callback function for GATT Client event. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DeregisterCb](#) (ble\_gattc\_app\_cb\_t cb)

This function deregisters the callback function for GATT Client event. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReqExMtu](#) (uint16\_t conn\_hdl, uint16\_t mtu)

This function sends a MTU Exchange Request PDU to a GATT Server

in order to change the current MTU. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscAllPrimServ](#) (uint16\_t conn\_hdl)

This function discovers all Primary Services in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscPrimServ](#) (uint16\_t conn\_hdl, uint8\_t \*p\_uuid, uint8\_t uuid\_type)

This function discovers Primary Service specified by p\_uuid in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscAllSecondServ](#) (uint16\_t conn\_hdl)

This function discovers all Secondary Services in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscInclServ](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_range\_t \*p\_range)

This function discovers Included Services within the specified attribute handle range in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscAllChar](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_range\_t \*p\_range)

This function discovers Characteristic within the specified attribute handle range in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscCharByUuid](#) (uint16\_t conn\_hdl, uint8\_t \*p\_uuid, uint8\_t uuid\_type, st\_ble\_gatt\_hdl\_range\_t \*p\_range)

This function discovers Characteristic specified by uuid within the specified attribute handle range in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_DiscAllCharDesc](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_range\_t \*p\_range)

This function discovers Characteristic Descriptor within the specified attribute handle range in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReadChar](#) (uint16\_t conn\_hdl, uint16\_t value\_hdl)

This function reads a Characteristic/Characteristic Descriptor in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReadCharUsingUuid](#) (uint16\_t conn\_hdl, uint8\_t \*p\_uuid, uint8\_t uuid\_type, st\_ble\_gatt\_hdl\_range\_t \*p\_range)

This function reads a Characteristic in a GATT Server using a specified UUID. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReadLongChar](#) (uint16\_t conn\_hdl, uint16\_t value\_hdl, uint16\_t offset)

This function reads a Long Characteristic in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReadMultiChar](#) (uint16\_t conn\_hdl, st\_ble\_gattc\_rd\_multi\_req\_param\_t \*p\_list)

This function reads multiple Characteristics in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_WriteCharWithoutRsp](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_write\_data)

This function writes a Characteristic in a GATT Server without response. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_SignedWriteChar](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_write\_data)

This function writes Signed Data to a Characteristic in a GATT Server without response. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_WriteChar](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_write\_data)

This function writes a Characteristic in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_WriteLongChar](#) (uint16\_t conn\_hdl, st\_ble\_gatt\_hdl\_value\_pair\_t \*p\_write\_data, uint16\_t offset)

This function writes a Long Characteristic in a GATT Server. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ReliableWrites](#) (uint16\_t conn\_hdl, st\_ble\_gattc\_reliable\_writes\_char\_pair\_t \*p\_char\_pair, uint8\_t pair\_num, uint8\_t auto\_flag)

This function performs the Reliable Writes procedure described in GATT Specification. [More...](#)

ble\_status\_t [R\\_BLE\\_GATTC\\_ExecWrite](#) (uint16\_t conn\_hdl, uint8\_t exe\_flag)

If the auto execute of Reliable Writes is not specified by

[R\\_BLE\\_GATTC\\_ReliableWrites\(\)](#), this function is used to execute a write to Characteristic. [More...](#)

## Detailed Description

### Data Structures

struct [st\\_ble\\_gatt\\_hdl\\_range\\_t](#)  
Attribute handle range. [More...](#)

struct [st\\_ble\\_gattc\\_reliable\\_writes\\_char\\_pair\\_t](#)  
This is used in [R\\_BLE\\_GATTC\\_ReliableWrites\(\)](#) to specify the pair of Characteristic Value and Characteristic Value Handle. [More...](#)

struct [st\\_ble\\_gattc\\_conn\\_evt\\_t](#)  
This structure notifies that the link with the GATT Server has been established. [More...](#)

struct [st\\_ble\\_gattc\\_disconn\\_evt\\_t](#)  
This structure notifies that the link with the GATT Server has been disconnected. [More...](#)

struct [st\\_ble\\_gattc\\_ex\\_mtu\\_rsp\\_evt\\_t](#)  
This structure notifies that a MTU Exchange Response PDU has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_serv\\_16\\_evt\\_t](#)  
This structure notifies that a 16-bit UUID Service has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_serv\\_128\\_evt\\_t](#)  
This structure notifies that a 128-bit UUID Service has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_inc\\_serv\\_16\\_evt\\_t](#)  
This structure notifies that a 16-bit UUID Included Service has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_inc\\_serv\\_128\\_evt\\_t](#)

This structure notifies that a 128-bit UUID Included Service has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_char\\_16\\_evt\\_t](#)

This structure notifies that a 16-bit UUID Characteristic has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_char\\_128\\_evt\\_t](#)

This structure notifies that a 128-bit UUID Characteristic has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_char\\_desc\\_16\\_evt\\_t](#)

This structure notifies that a 16-bit UUID Characteristic Descriptor has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_char\\_desc\\_128\\_evt\\_t](#)

This structure notifies that a 128-bit UUID Characteristic Descriptor has been discovered. [More...](#)

struct [st\\_ble\\_gattc\\_err\\_rsp\\_evt\\_t](#)

This structure notifies that a Error Response PDU has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_ntf\\_evt\\_t](#)

This structure notifies that a Notification PDU has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_ind\\_evt\\_t](#)

This structure notifies that a Indication PDU has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_rd\\_char\\_evt\\_t](#)

This structure notifies that read response to [R\\_BLE\\_GATTC\\_ReadChar\(\)](#) or [R\\_BLE\\_GATTC\\_ReadCharUsingUuid\(\)](#) has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_wr\\_char\\_evt\\_t](#)

This structure notifies that write response to [R\\_BLE\\_GATTC\\_WriteChar\(\)](#) has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_rd\\_multi\\_char\\_evt\\_t](#)

This structure notifies that read response to [R\\_BLE\\_GATTC\\_ReadMultiChar\(\)](#) has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_char\\_part\\_wr\\_evt\\_t](#)

This structure notifies that write response to [R\\_BLE\\_GATTC\\_WriteLongChar\(\)](#) or [R\\_BLE\\_GATTC\\_ReliableWrites\(\)](#) has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_reliable\\_writes\\_comp\\_evt\\_t](#)

This structure notifies that a response to [R\\_BLE\\_GATTC\\_ExecWrite\(\)](#) has been received from a GATT Server. [More...](#)

struct [st\\_ble\\_gattc\\_rd\\_multi\\_req\\_param\\_t](#)

This is used in [R\\_BLE\\_GATTC\\_ReadMultiChar\(\)](#) to specify multiple Characteristics to be read. [More...](#)

struct [st\\_ble\\_gattc\\_evt\\_data\\_t](#)

[st\\_ble\\_gattc\\_evt\\_data\\_t](#) is the type of the data notified in a GATT Client Event. [More...](#)

struct [st\\_ble\\_gatt\\_value\\_t](#)

Attribute Value. [More...](#)

struct [st\\_ble\\_gatt\\_hdl\\_value\\_pair\\_t](#)

Attribute handle and attribute Value. [More...](#)

## Macros

#define [BLE\\_GATTC\\_EXECUTE\\_WRITE\\_CANCEL\\_FLAG](#)

#define [BLE\\_GATTC\\_EXECUTE\\_WRITE\\_EXEC\\_FLAG](#)

#define [BLE\\_GATTC\\_MAX\\_CB](#)

GATT Client Callback Number.

```
#define BLE_GATTC_EXEC_AUTO
```

Auto execution.

```
#define BLE_GATTC_EXEC_NOT_AUTO
```

Not auto execution.

```
#define BLE_GATTC_RELIABLE_WRITES_MAX_CHAR_PAIR
```

Length of the Queue used with Prepare Write procedure to write a characteristic whose size is larger than MTU.

## Typedefs

```
typedef void(* ble_gattc_app_cb_t) (uint16_t event_type, ble_status_t event_result,
st_ble_gattc_evt_data_t *p_event_data)
```

ble\_gattc\_app\_cb\_t is the GATT Client Event callback function type.  
More...

## Enumerations

```
enum e_r_ble_gattc_evt_t
```

GATT Client Event Identifier. More...

## Data Structure Documentation

### ◆ st\_ble\_gatt\_hdl\_range\_t

struct st_ble_gatt_hdl_range_t		
Attribute handle range.		
Data Fields		
uint16_t	start_hdl	Start Attribute Handle.
uint16_t	end_hdl	End Attribute Handle.

### ◆ st\_ble\_gattc\_reliable\_writes\_char\_pair\_t

struct st_ble_gattc_reliable_writes_char_pair_t		
This is used in <a href="#">R_BLE_GATTC_ReliableWrites()</a> to specify the pair of Characteristic Value and Characteristic Value Handle.		
Data Fields		

<a href="#">st_ble_gatt_hdl_value_pair_t</a>	write_data	Pair of Characteristic Value and Characteristic Value Handle.
uint16_t	offset	Offset that indicates the location to be written.  Normally, set 0 to this parameter. If this parameter sets to a value other than 0, Adjust the offset parameter and the length of the value to be written not to exceed the length of the Characteristic.

#### ◆ st\_ble\_gattc\_conn\_evt\_t

struct st_ble_gattc_conn_evt_t		
This structure notifies that the link with the GATT Server has been established.		
Data Fields		
<a href="#">st_ble_dev_addr_t</a> *	p_addr	Address of the GATT Server.

#### ◆ st\_ble\_gattc\_disconn\_evt\_t

struct st_ble_gattc_disconn_evt_t		
This structure notifies that the link with the GATT Server has been disconnected.		
Data Fields		
<a href="#">st_ble_dev_addr_t</a> *	p_addr	Address of the GATT Server.

#### ◆ st\_ble\_gattc\_ex\_mtu\_rsp\_evt\_t

struct st_ble_gattc_ex_mtu_rsp_evt_t		
This structure notifies that a MTU Exchange Response PDU has been received from a GATT Server.		
Data Fields		
uint16_t	mtu	MTU size(in bytes) that GATT Server can receive.

#### ◆ st\_ble\_gattc\_serv\_16\_evt\_t

struct st_ble_gattc_serv_16_evt_t		
This structure notifies that a 16-bit UUID Service has been discovered.		
Data Fields		
<a href="#">st_ble_gatt_hdl_range_t</a>	range	Attribute handle range of the 16-bit UUID service.
uint16_t	uuid_16	Service UUID.

#### ◆ st\_ble\_gattc\_serv\_128\_evt\_t

struct st_ble_gattc_serv_128_evt_t		
------------------------------------	--	--

This structure notifies that a 128-bit UUID Service has been discovered.		
Data Fields		
<a href="#">st_ble_gatt_hdl_range_t</a>	range	Attribute handle range of the 128-bit UUID service.
uint8_t	uuid_128[ <a href="#">BLE_GATT_128_BIT_UUID_SIZE</a> ]	Service UUID.

#### ◆ [st\\_ble\\_gattc\\_inc\\_serv\\_16\\_evt\\_t](#)

struct <a href="#">st_ble_gattc_inc_serv_16_evt_t</a>		
This structure notifies that a 16-bit UUID Included Service has been discovered.		
Data Fields		
uint16_t	decl_hdl	Service Declaration handle of the 16-bit UUID Included Service.
<a href="#">st_ble_gattc_serv_16_evt_t</a>	service	The contents of the Included Service.

#### ◆ [st\\_ble\\_gattc\\_inc\\_serv\\_128\\_evt\\_t](#)

struct <a href="#">st_ble_gattc_inc_serv_128_evt_t</a>		
This structure notifies that a 128-bit UUID Included Service has been discovered.		
Data Fields		
uint16_t	decl_hdl	Service Declaration handle of the 128-bit UUID Included Service.
<a href="#">st_ble_gattc_serv_128_evt_t</a>	service	The contents of the Included Service.

#### ◆ [st\\_ble\\_gattc\\_char\\_16\\_evt\\_t](#)

struct <a href="#">st_ble_gattc_char_16_evt_t</a>		
This structure notifies that a 16-bit UUID Characteristic has been discovered.		
Data Fields		
uint16_t	decl_hdl	Attribute handle of Characteristic Declaration.
uint8_t	cproperty	Characteristic Properties.  It is a bitwise OR of the following values. Refer to Core Spec [Vol.3] Generic Attribute Profile(GATT) "3.3.1.1 Characteristic Properties" regarding the details of the Characteristic Properties.

		value	description
		0x01	Broadcast property
		0x02	Read property
		0x04	Write Without Response property
		0x08	Write property
		0x10	Notify property
		0x20	Indicate property
		0x40	Authenticated Signed Writes property
		0x80	Extended Properties property
uint16_t	value_hdl	Value Handle of the Characteristic.	
uint16_t	uuid_16	Characteristic UUID.	

◆ **st\_ble\_gattc\_char\_128\_evt\_t**

struct st_ble_gattc_char_128_evt_t						
This structure notifies that a 128-bit UUID Characteristic has been discovered.						
Data Fields						
uint16_t	decl_hdl	Attribute Handle of Characteristic Declaration.				
uint8_t	cproperty	Characteristic Properties.  It is a bitwise OR of the following values. Refer to Core Spec [Vol.3] Generic Attribute Profile(GATT) "3.3.1.1 Characteristic Properties" regarding the details of the Characteristic Properties.				
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x01</td> <td>Broadcast property</td> </tr> </tbody> </table>	value	description	0x01	Broadcast property
value	description					
0x01	Broadcast property					

		0x02	Read property
		0x04	Write Without Response property
		0x08	Write property
		0x10	Notify property
		0x20	Indicate property
		0x40	Authenticated Signed Writes property
		0x80	Extended Properties property
uint16_t	value_hdl	Value Handle of the Characteristic.	
uint8_t	uuid_128[ BLE_GATT_128_BIT_UUID_SIZE]	Characteristic UUID.	

#### ◆ st\_ble\_gattc\_char\_desc\_16\_evt\_t

struct st_ble_gattc_char_desc_16_evt_t		
This structure notifies that a 16-bit UUID Characteristic Descriptor has been discovered.		
Data Fields		
uint16_t	desc_hdl	Attribute Handle of Characteristic Descriptor.
uint16_t	uuid_16	Characteristic Descriptor UUID.

#### ◆ st\_ble\_gattc\_char\_desc\_128\_evt\_t

struct st_ble_gattc_char_desc_128_evt_t		
This structure notifies that a 128-bit UUID Characteristic Descriptor has been discovered.		
Data Fields		
uint16_t	desc_hdl	Attribute Handle of Characteristic Descriptor.
uint8_t	uuid_128[ BLE_GATT_128_BIT_UUID_SIZE]	Characteristic Descriptor UUID.

#### ◆ st\_ble\_gattc\_err\_rsp\_evt\_t

struct st_ble_gattc_err_rsp_evt_t		
This structure notifies that a Error Response PDU has been received from a GATT Server.		

Data Fields												
uint8_t	op_code	<p>The op code of the ATT Request that causes the Error Response.</p> <table border="1"> <tr> <td>op_code</td> </tr> </table> <p>Exchange MTU Request(0x02)                      Find Information Request(0x04)                      Find By Type Value Request(0x06)                      Read By Type Request(0x08)                      Read Request(0x0A)                      Read Blob Request(0x0C)                      Read Multiple Request(0x0E)                      Read by Group Type Request(0x10)                      Write Request(0x12)                      Prepare Write Request(0x16)                      Execute Write Request(0x18)</p>	op_code									
op_code												
uint16_t	attr_hdl	Attribute handle that is target for the request.										
uint16_t	rsp_code	<p>The error codes notified from the GATT Server.</p> <p>It is a bitwise OR of GATT Error Group ID : 0x3000 and the following error codes defined in Core Spec and Core Spec Supplement.</p> <table border="1"> <thead> <tr> <th>Error Code</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_ERR_GATT_INVALID_HANDLE(0x3001)</td> <td>Invalid attribute handle</td> </tr> <tr> <td>BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)</td> <td>The attribute cannot be read.</td> </tr> <tr> <td>BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)</td> <td>The attribute cannot be written.</td> </tr> <tr> <td>BLE_ERR_GATT_INVALID_PDU</td> <td>Invalid PDU.</td> </tr> </tbody> </table>	Error Code	description	BLE_ERR_GATT_INVALID_HANDLE(0x3001)	Invalid attribute handle	BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)	The attribute cannot be read.	BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)	The attribute cannot be written.	BLE_ERR_GATT_INVALID_PDU	Invalid PDU.
Error Code	description											
BLE_ERR_GATT_INVALID_HANDLE(0x3001)	Invalid attribute handle											
BLE_ERR_GATT_READ_NOT_PERMITTED(0x3002)	The attribute cannot be read.											
BLE_ERR_GATT_WRITE_NOT_PERMITTED(0x3003)	The attribute cannot be written.											
BLE_ERR_GATT_INVALID_PDU	Invalid PDU.											

T_INVALID_PD U(0x3004)	
BLE_ERR_GATT_INSUFFICIENT_AUTHENTICATION(0x3005)	The authentication to access the attribute is insufficient.
BLE_ERR_GATT_REQUEST_NOT_SUPPORTED(0x3006)	The request is not supported.
BLE_ERR_GATT_INVALID_OFFSET(0x3007)	The specified offset is larger than the length of the attribute value.
BLE_ERR_GATT_INSUFFICIENT_AUTHORIZATION(0x3008)	Authorization is required to access the attribute.
BLE_ERR_GATT_PREPARE_WRITE_QUEUE_FULL(0x3009)	The Write Queue in the GATT Server is full.
BLE_ERR_GATT_ATTRIBUTE_NOT_FOUND(0x300A)	The specified attribute is not found.
BLE_ERR_GATT_ATTRIBUTE_NOT_LONG(0x300B)	The attribute cannot be read by Read Blob Request.
BLE_ERR_GATT_INSUFFICIENT_ENCRYPTION_KEY_SIZE(0x300C)	The Encryption Key Size is insufficient.
BLE_ERR_GATT_INVALID_ATTRIBUTE_LENGTH(0x300D)	The length of the specified attribute is invalid.
BLE_ERR_GATT_UNLIKELY_ERROR(0x300E)	Because an error has occurred, the process cannot be advanced.

BLE_ERR_GATT_INSUFFICIENT_ENCRYPTION(0x300F)	Encryption is required to access the attribute.
BLE_ERR_GATT_UNSUPPORTED_GROUP_TYPE(0x3010)	The type of the specified attribute is not supported.
BLE_ERR_GATT_INSUFFICIENT_RESOURCES(0x3011)	The resource to complete the request is insufficient.
0x3080 - 0x309F	Application Error. The upper layer defines the error codes.
0x30E0 - 0x30FF	The error code defined in Common Profile and Service Error Core Specification Supplement(CSS). CSS ver.7 defines the error codes from 0x30FC to 0x30FF.
BLE_ERR_GATT_WRITE_REQUEST_REJECTED(0x30FC)	The Write Request has not been completed due to the reason other than Permission.
BLE_ERR_GATT_INVALID_CONFIG(0x30FD)	The CCCD is set to be invalid.
BLE_ERR_GATT_ALREADY_IN_PROGRESS(0x30FE)	The request is now in progress.
BLE_ERR_GATT_OUT_OF_RANGE	The attribute value is out of

		NGE(0x30FF) range.
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#### ◆ st\_ble\_gattc\_ntf\_evt\_t

struct st_ble_gattc_ntf_evt_t		
This structure notifies that a Notification PDU has been received from a GATT Server.		
Data Fields		
st_ble_gatt_hdl_value_pair_t	data	Characteristic that causes the Notification.

#### ◆ st\_ble\_gattc\_ind\_evt\_t

struct st_ble_gattc_ind_evt_t		
This structure notifies that a Indication PDU has been received from a GATT Server.		
Data Fields		
st_ble_gatt_hdl_value_pair_t	data	Characteristic that causes the Indication.

#### ◆ st\_ble\_gattc\_rd\_char\_evt\_t

struct st_ble_gattc_rd_char_evt_t		
This structure notifies that read response to <a href="#">R_BLE_GATTC_ReadChar()</a> or <a href="#">R_BLE_GATTC_ReadCharUsingUuid()</a> has been received from a GATT Server.		
Data Fields		
st_ble_gatt_hdl_value_pair_t	read_data	The contents of the Characteristic that has been read.

#### ◆ st\_ble\_gattc\_wr\_char\_evt\_t

struct st_ble_gattc_wr_char_evt_t		
This structure notifies that write response to <a href="#">R_BLE_GATTC_WriteChar()</a> has been received from a GATT Server.		
Data Fields		
uint16_t	value_hdl	Value Handle of the Characteristic/Characteristic Descriptor that has been written.

#### ◆ st\_ble\_gattc\_rd\_multi\_char\_evt\_t

struct st_ble_gattc_rd_multi_char_evt_t		
This structure notifies that read response to <a href="#">R_BLE_GATTC_ReadMultiChar()</a> has been received from a GATT Server.		
Data Fields		
uint16_t	value_hdl_num	The number of Value Handles of the Characteristics that has

		been read.
<a href="#">st_ble_gatt_value_t</a>	multi_char_val	The contents of multiple Characteristics that have been read.

#### ◆ st\_ble\_gattc\_char\_part\_wr\_evt\_t

struct st_ble_gattc_char_part_wr_evt_t		
This structure notifies that write response to <a href="#">R_BLE_GATTC_WriteLongChar()</a> or <a href="#">R_BLE_GATTC_ReliableWrites()</a> has been received from a GATT Server.		
Data Fields		
<a href="#">st_ble_gatt_hdl_value_pair_t</a>	write_data	The data to be written to the Characteristic/Long Characteristic/Long Characteristic Descriptor.
uint16_t	offset	Offset that indicates the location to be written.

#### ◆ st\_ble\_gattc\_reliable\_writes\_comp\_evt\_t

struct st_ble_gattc_reliable_writes_comp_evt_t								
This structure notifies that a response to <a href="#">R_BLE_GATTC_ExecWrite()</a> has been received from a GATT Server.								
Data Fields								
uint8_t	exe_flag	This field indicates the command of the Execute Write that has been done.						
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Cancel the write.</td> </tr> <tr> <td>0x01</td> <td>Execute the write.</td> </tr> </tbody> </table>	value	description	0x00	Cancel the write.	0x01	Execute the write.
		value	description					
0x00	Cancel the write.							
0x01	Execute the write.							

#### ◆ st\_ble\_gattc\_rd\_multi\_req\_param\_t

struct st_ble_gattc_rd_multi_req_param_t		
This is used in <a href="#">R_BLE_GATTC_ReadMultiChar()</a> to specify multiple Characteristics to be read.		
Data Fields		
uint16_t *	p_hdl_list	List of Value Handles that point the Characteristics to be read.
uint16_t	list_count	The number of Value Handles included in the hdl_list parameter.

#### ◆ st\_ble\_gattc\_evt\_data\_t

struct st_ble_gattc_evt_data_t
--------------------------------

`st_ble_gattc_evt_data_t` is the type of the data notified in a GATT Client Event.

Data Fields		
uint16_t	conn_hdl	Connection handle identifying the GATT Server.
uint16_t	param_len	The size of GATT Client Event parameters.
void *	p_param	GATT Client Event parameters. This parameter differs in each GATT Client Event.

#### ◆ `st_ble_gatt_value_t`

Data Fields		
uint16_t	value_len	Length of the attribute value.
uint8_t *	p_value	Attribute Value.

#### ◆ `st_ble_gatt_hdl_value_pair_t`

Data Fields		
uint16_t	attr_hdl	Attribute Handle.
<code>st_ble_gatt_value_t</code>	value	Attribute Value.

### Macro Definition Documentation

#### ◆ `BLE_GATTC_EXECUTE_WRITE_CANCEL_FLAG`

<code>#define BLE_GATTC_EXECUTE_WRITE_CANCEL_FLAG</code>
GATT Execute Write Cancel Flag.

#### ◆ `BLE_GATTC_EXECUTE_WRITE_EXEC_FLAG`

<code>#define BLE_GATTC_EXECUTE_WRITE_EXEC_FLAG</code>
GATT Execute Write Execute Flag.

### Typedef Documentation

## ◆ ble\_gattc\_app\_cb\_t

ble_gattc_app_cb_t		
ble_gattc_app_cb_t is the GATT Client Event callback function type.		
<b>Parameters</b>		
[in]	event_type	The type of GATT Client Event.
[in]	event_result	The result of GATT Client Event
[in]	p_event_data	Data notified by GATT Client Event.
<b>Returns</b>		
none		

## Enumeration Type Documentation

## ◆ e\_r\_ble\_gattc\_evt\_t

enum e_r_ble_gattc_evt_t	
GATT Client Event Identifier.	
Enumerator	
BLE_GATTC_EVENT_ERROR_RSP	<p>This event notifies the application layer that a problem has occurred in the GATT Server while processing a request from GATT Client.</p> <p>When GATT Client has received a Error Response PDU from a GATT Server, BLE_GATTC_EVENT_ERROR_RSP event is notified the application layer.</p> <p><b>Event Code: 0x4001</b></p> <p><b>result:</b></p> <p style="text-align: center;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_err_rsp_evt_tBLE_GATTC_EVENT_ERROR_RSP</p>
BLE_GATTC_EVENT_EX_MTU_RSP	<p>This event notifies the application layer that a MTU Exchange Response PDU has been received from a GATT Server.</p>

	<p><b>Event Code: 0x4003</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a Exchange MTU Response since GATT Client sent a Exchange MTU Request PDU to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_ex_mtu_rsp_evt_tBLE_GATTC_EVENT_EX_MTU_RSP</p>
BLE_GATTC_EVENT_CHAR_READ_BY_UUID_RSP	<p>When the read of Characteristic specified by UUID has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x4009</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a Exchange MTU Response since GATT Client sent a Exchange MTU Request PDU to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_rd_char_evt_tBLE_GATTC_EVENT_CHAR_READ_BY_UUID_RSP</p>
BLE_GATTC_EVENT_CHAR_READ_RSP	<p>When the read of Characteristic/Characteristic Descriptor has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x400B</b></p> <p><b>result:</b></p>

	<p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a read response since GATT Client sent a request for read by <a href="#">R_BLE_GATTC_ReadCharUsingUuid()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_rd_char_evt_tBLE_GATTC_EVENT_CHAR_READ_RSP</p>
BLE_GATTC_EVENT_CHAR_PART_READ_RSP	<p>After calling <a href="#">R_BLE_GATTC_ReadLongChar()</a>, this event notifies the application layer that the partial contents of Long Characteristic/Long Characteristic Descriptor has been received from the GATT Server.</p> <p><b>Event Code: 0x400D</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a read response since GATT Client sent a request for read by <a href="#">R_BLE_GATTC_ReadLongChar()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_rd_char_evt_tBLE_GATTC_EVENT_CHAR_PART_READ_RSP</p>
BLE_GATTC_EVENT_MULTI_CHAR_READ_RSP	<p>This event notifies the application layer that the read of multiple Characteristics has been completed.</p> <p><b>Event Code: 0x400F</b></p>

	<p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a read response since GATT Client sent a request for read by <a href="#">R_BLE_GATTC_ReadMultiChar()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_rd_multi_char_evt_tBLE_GATTC_EVENT_MULTI_CHAR_READ_RSP</p>
BLE_GATTC_EVENT_CHAR_WRITE_RSP	<p>This event notifies the application layer that the write of Characteristic/Characteristic Descriptor has been completed.</p> <p><b>Event Code: 0x4013</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a write response since GATT Client sent a request for write by <a href="#">R_BLE_GATTC_WriteChar()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_wr_char_evt_tBLE_GATTC_EVENT_CHAR_WRITE_RSP</p>
BLE_GATTC_EVENT_CHAR_PART_WRITE_RSP	<p>This event notifies the application layer of the one of the following.</p> <ul style="list-style-type: none"> <li>• A segmentation to be written to Long Characteristic/Long Characteristic Descriptor has been sent to the GATT</li> </ul>

	<p>Server.</p> <ul style="list-style-type: none"> <li>The data written to one Characteristic by Reliable Writes has been sent to the GATT Server.</li> </ul> <p><b>Event Code: 0x4017</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a response since GATT Client sent a request for segmentation write by <a href="#">R_BLE_GATTC_WriteLongChar()</a>, or 1 Characteristic write by <a href="#">R_BLE_GATTC_ReliableWrites()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_char_part_wr_evt_tBLE_GATTC_EVENT_CHAR_PART_WRITE_RSP</p>
BLE_GATTC_EVENT_HDL_VAL_NTF	<p>This event notifies the application layer that a Notification has been received from a GATT Server.</p> <p><b>Event Code: 0x401B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_ntf_evt_tBLE_GATTC_EVENT_HDL_VAL_NTF</p>
BLE_GATTC_EVENT_HDL_VAL_IND	<p>This event notifies the application layer that a Indication has been received from a GATT Server.</p> <p>When the GATT Client has received a Indication, host stack automatically sends a</p>

	<p>Confirmation to the GATT Server.</p> <p><b>Event Code: 0x401D</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_MEM_ALLOC_FAILED(0x000C) Insufficient resource is needed to generate the confirmation packet.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_ind_evt_tBLE_GATTC_EVENT_HDL_VAL_IND</p>
BLE_GATTC_EVENT_CONN_IND	<p>This event notifies the application layer that the link with the GATT Server has been established.</p> <p><b>Event Code: 0x4081</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_conn_evt_tBLE_GATTC_EVENT_CONN_IND</p>
BLE_GATTC_EVENT_DISCONN_IND	<p>This event notifies the application layer that the link with the GATT Server has been disconnected.</p> <p><b>Event Code: 0x4082</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_disconn_evt_tBLE_GATTC_EVENT_DISCONN_IND</p>
BLE_GATTC_EVENT_PRIM_SERV_16_DISC_IND	<p>This event notifies the application layer that 16-bit UUID Primary Service has been</p>

	<p>discovered.</p> <p><b>Event Code: 0x40E0</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_serv_16_evt_tBLE_GATTC_EVENT_PRIM_SERV_16_DISC_IND</p>
BLE_GATTC_EVENT_PRIM_SERV_128_DISC_IND	<p>This event notifies the application layer that 128-bit UUID Primary Service has been discovered.</p> <p><b>Event Code: 0x40E1</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_serv_128_evt_tBLE_GATTC_EVENT_PRIM_SERV_128_DISC_IND</p>
BLE_GATTC_EVENT_ALL_PRIM_SERV_DISC_COMP	<p>When the Primary Service discovery by <a href="#">R_BLE_GATTC_DiscAllPrimServ()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40E2</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_ALL_PRIM_SERV_DISC_COMP</p>
BLE_GATTC_EVENT_PRIM_SERV_DISC_COMP	<p>When the Primary Service discovery by <a href="#">R_BLE_GATTC_DiscPrimServ()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40E3</b></p>

	<p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_PRIM_SERV_DISC_COM P</p>
BLE_GATTC_EVENT_SECOND_SERV_16_DISC_IND	<p>This event notifies the application layer that 16-bit UUID Secondary Service has been discovered.</p> <p><b>Event Code: 0x40E4</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_serv_16_evt_tBLE_GATTC_EVENT_ SECOND_SERV_16_DISC_IND</p>
BLE_GATTC_EVENT_SECOND_SERV_128_DISC_IND	<p>This event notifies the application layer that 128-bit UUID Secondary Service has been discovered.</p> <p><b>Event Code: 0x40E5</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_serv_128_evt_tBLE_GATTC_EVENT_ _SECOND_SERV_128_DISC_IND</p>
BLE_GATTC_EVENT_ALL_SECOND_SERV_DISC_COMPLETE	<p>When the Primary Service discovery by <a href="#">R_BLE_GATTC_DiscAllSecondServ()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40E6</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p>

	<p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_ALL_SECOND_SERV_DISC_COMP</p>
BLE_GATTC_EVENT_INC_SERV_16_DISC_IND	<p>This event notifies the application layer that Included Service that includes 16-bit UUID Service has been discovered.</p> <p><b>Event Code: 0x40E7</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_inc_serv_16_evt_tBLE_GATTC_EVENT_INC_SERV_16_DISC_IND</p>
BLE_GATTC_EVENT_INC_SERV_128_DISC_IND	<p>This event notifies the application layer that Included Service that includes 128-bit UUID Service has been discovered.</p> <p><b>Event Code: 0x40E8</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_inc_serv_128_evt_tBLE_GATTC_EVENT_INC_SERV_128_DISC_IND</p>
BLE_GATTC_EVENT_INC_SERV_DISC_COMP	<p>When the Included Service discovery by <a href="#">R_BLE_GATTC_DiscIncServ()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40E9</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_INC_SERV_DISC_COMP</p>

BLE_GATTC_EVENT_CHAR_16_DISC_IND	<p>This event notifies the application layer that 16-bit UUID Characteristic has been discovered.</p> <p><b>Event Code: 0x40EA</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_char_16_evt_tBLE_GATTC_EVENT_CHAR_16_DISC_IND</p>
BLE_GATTC_EVENT_CHAR_128_DISC_IND	<p>This event notifies the application layer that 128-bit UUID Characteristic has been discovered.</p> <p><b>Event Code: 0x40EB</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_char_128_evt_tBLE_GATTC_EVENT_CHAR_128_DISC_IND</p>
BLE_GATTC_EVENT_ALL_CHAR_DISC_COMP	<p>When the Characteristic discovery by <a href="#">R_BLE_GATTC_DiscAllChar()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40EC</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_ALL_CHAR_DISC_COMP</p>
BLE_GATTC_EVENT_CHAR_DISC_COMP	<p>When the Characteristic discovery by <a href="#">R_BLE_GATTC_DiscCharByUuid()</a> has been completed, this event is notified to the application layer.</p>

	<p><b>Event Code: 0x40ED</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_CHAR_DISC_COMP</p>
BLE_GATTC_EVENT_CHAR_DESC_16_DISC_IND	<p>This event notifies the application layer that 16-bit UUID Characteristic Descriptor has been discovered.</p> <p><b>Event Code: 0x40EE</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_char_desc_16_evt_tBLE_GATTC_EVENT_CHAR_DESC_16_DISC_IND</p>
BLE_GATTC_EVENT_CHAR_DESC_128_DISC_IND	<p>This event notifies the application layer that 128-bit UUID Characteristic Descriptor has been discovered.</p> <p><b>Event Code: 0x40EF</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_char_desc_128_evt_tBLE_GATTC_EVENT_CHAR_DESC_128_DISC_IND</p>
BLE_GATTC_EVENT_ALL_CHAR_DESC_DISC_COMP	<p>When the Characteristic Descriptor discovery by <a href="#">R_BLE_GATTC_DiscAllCharDesc()</a> has been completed, this event is notified to the application layer.</p> <p><b>Event Code: 0x40F0</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success</p>

	<p>000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_ALL_CHAR_DESC_DISC _COMP</p>
BLE_GATTC_EVENT_LONG_CHAR_READ_COMP	<p>After calling <a href="#">R_BLE_GATTC_ReadLongChar()</a>, this event notifies the application layer that all of the contents of the Characteristic/Long Characteristic Descriptor has been received from the GATT Server.</p> <p><b>Event Code: 0x40F1</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_LONG_CHAR_READ_C OMP</p>
BLE_GATTC_EVENT_LONG_CHAR_WRITE_COMP	<p>This event notifies that the application layer that the write of Long Characteristic/Long Characteristic Descriptor has been completed.</p> <p><b>Event Code: 0x40F2</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0 Success 000)</p> <p>BLE_ERR_RSP_TIM 30 seconds or EOUT(0x0011) more have passed without receiving a response since GATT Client sent a request for write by <a href="#">R_BLE_GATTC_WriteLongChar()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_LONG_CHAR_WRITE_C OMP</p>
BLE_GATTC_EVENT_RELIABLE_WRITES_TX_COMP	<p>This event notifies that the application layer that the GATT Server has received the data to</p>

	<p>be written to the Characteristics.</p> <p><b>Event Code: 0x40F3</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_RELIABLE_WRITES_TX_COMP</p>
BLE_GATTC_EVENT_RELIABLE_WRITES_COMP	<p>This event notifies the application layer that the Reliable Writes has been completed.</p> <p><b>Event Code: 0x40F4</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_RSP_TIMEOUT(0x0011) 30 seconds or more have passed without receiving a response since GATT Client sent a request for execute write by <a href="#">R_BLE_GATTC_ReliableWrites()</a> or <a href="#">R_BLE_GATTC_ExecWrite()</a> to the GATT Server.</p> <p><b>Event Data:</b></p> <p>st_ble_gattc_reliable_writes_comp_evt_tBLE_GATTC_EVENT_RELIABLE_WRITES_COMP</p>
BLE_GATTC_EVENT_INVALID	<p>Invalid GATT Client Event.</p> <p><b>Event Code: 0x40FF</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>noneBLE_GATTC_EVENT_INVALID</p>

## Function Documentation

### ◆ R\_BLE\_GATTC\_Init()

```
ble_status_t R_BLE_GATTC_Init ( uint8_t cb_num)
```

This function initializes the GATT Client and registers the number of the callbacks for GATT Client event.

Specify the `cb_num` parameter to a value between 1 and `BLE_GATTC_MAX_CB`.

[R\\_BLE\\_GATTC\\_RegisterCb\(\)](#) registers the callback.

The result of this API call is returned by a return value.

#### Parameters

[in]	<code>cb_num</code>	The number of callbacks to be registered.
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#### Return values

<code>BLE_SUCCESS(0x0000)</code>	Success
<code>BLE_ERR_INVALID_ARG(0x0003)</code>	The <code>cb_num</code> parameter is out of range.

◆ **R\_BLE\_GATTC\_RegisterCb()**

```
ble_status_t R_BLE_GATTC_RegisterCb ( ble_gattc_app_cb_t cb, uint8_t priority )
```

This function registers a callback function for GATT Client event.

The number of the callback that may be registered by this function is the value specified by [R\\_BLE\\_GATTC\\_Init\(\)](#).

The result of this API call is returned by a return value.

**Parameters**

[in]	cb	Callback function for GATT Client event.
[in]	priority	The priority of the callback function. Valid range is $1 \leq \text{priority} \leq \text{BLE\_GATTC\_MAX\_CB}$ . A lower priority number means a higher priority level.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The cb parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The priority parameter is out of range.
BLE_ERR_CONTEXT_FULL(0x000B)	Host stack has already registered the maximum number of callbacks.

◆ **R\_BLE\_GATTC\_DeregisterCb()**

```
ble_status_t R_BLE_GATTC_DeregisterCb ( ble_gattc_app_cb_t cb)
```

This function deregisters the callback function for GATT Client event.

The result of this API call is returned by a return value.

**Parameters**

[in]	cb	The callback function to be deregistered.
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**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The cb parameter is specified as NULL.
BLE_ERR_NOT_FOUND(0x000D)	The callback has not been registered.

◆ **R\_BLE\_GATTC\_ReqExMtu()**

```
ble_status_t R_BLE_GATTC_ReqExMtu ( uint16_t conn_hdl, uint16_t mtu )
```

This function sends a MTU Exchange Request PDU to a GATT Server in order to change the current MTU.

MTU Exchange Response is notified by BLE\_GATTC\_EVENT\_EX\_MTU\_RSP event.

The new MTU is the minimum value of the mtu parameter specified by this function and the mtu field in BLE\_GATTC\_EVENT\_EX\_MTU\_RSP event. Default MTU size is 23 bytes.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be sent.
[in]	mtu	The maximum size(in bytes) of the GATT PDU that GATT Client can receive. Valid range is 23 <= mtu <= 247.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The mtu parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_DiscAllPrimServ()**

```
ble_status_t R_BLE_GATTC_DiscAllPrimServ ( uint16_t conn_hdl)
```

This function discovers all Primary Services in a GATT Server.

When 16-bit UUID Primary Service has been discovered,  
 BLE\_GATTC\_EVENT\_PRIM\_SERV\_16\_DISC\_IND event is notified to the application layer.  
 When 128-bit UUID Primary Service has been discovered,  
 BLE\_GATTC\_EVENT\_PRIM\_SERV\_128\_DISC\_IND event is notified to the application layer.  
 When the Primary Service discovery has been completed,  
 BLE\_GATTC\_EVENT\_ALL\_PRIM\_SERV\_DISC\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.
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**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_OPERATION(0x0009)	This function was called while processing other request.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_DiscPrimServ()**

```
ble_status_t R_BLE_GATTC_DiscPrimServ ( uint16_t conn_hdl, uint8_t* p_uuid, uint8_t uuid_type )
```

This function discovers Primary Service specified by p\_uuid in a GATT Server.

When Primary Service whose uuid is the same as the specified uuid has been discovered, BLE\_GATTC\_EVENT\_PRIM\_SERV\_16\_DISC\_IND event or BLE\_GATTC\_EVENT\_PRIM\_SERV\_128\_DISC\_IND event is notified to the application layer. When the Primary Service discovery has been completed, BLE\_GATTC\_EVENT\_PRIM\_SERV\_DISC\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.						
[in]	p_uuid	UUID of Primary Service to be discovered.						
[in]	uuid_type	<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)</td> <td>16-bit UUID</td> </tr> <tr> <td>BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)</td> <td>128-bit UUID</td> </tr> </tbody> </table>	macro	description	BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	16-bit UUID	BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	128-bit UUID
macro	description							
BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	16-bit UUID							
BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	128-bit UUID							

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_uuid parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The uuid_type parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_DiscAllSecondServ()**

```
ble_status_t R_BLE_GATTC_DiscAllSecondServ ( uint16_t conn_hdl)
```

This function discovers all Secondary Services in a GATT Server.

When a 16-bit UUID Secondary Service has been discovered, BLE\_GATTC\_EVENT\_SECOND\_SERV\_16\_DISC\_IND event is notified to the application layer.  
 When a 128-bit UUID Secondary Service has been discovered, BLE\_GATTC\_EVENT\_SECOND\_SERV\_128\_DISC\_IND event is notified to the application layer.  
 When the Secondary Service discovery has been completed, BLE\_GATTC\_EVENT\_ALL\_SECOND\_SERV\_DISC\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.
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**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_DiscIncServ()**

```
ble_status_t R_BLE_GATTC_DiscIncServ ( uint16_t conn_hdl, st_ble_gatt_hdl_range_t* p_range )
```

This function discovers Included Services within the specified attribute handle range in a GATT Server.

When Included Service that includes 16-bit UUID Service has been discovered, BLE\_GATTC\_EVENT\_INC\_SERV\_16\_DISC\_IND event is notified to the application layer.  
 When Included Service that includes 128-bit UUID Service has been discovered, BLE\_GATTC\_EVENT\_INC\_SERV\_128\_DISC\_IND event is notified to the application layer.  
 When the Included Service discovery has been completed, BLE\_GATTC\_EVENT\_INC\_SERV\_DISC\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.
[in]	p_range	Retrieval range of Included Service.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_range parameter is specified as NULL.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_DiscAllChar()

```
ble_status_t R_BLE_GATTC_DiscAllChar ( uint16_t conn_hdl, st_ble_gatt_hdl_range_t* p_range )
```

This function discovers Characteristic within the specified attribute handle range in a GATT Server.

When 16-bit UUID Characteristic has been discovered, BLE\_GATTC\_EVENT\_CHAR\_16\_DISC\_IND event is notified to the application layer.

When 128-bit UUID Characteristic has been discovered, BLE\_GATTC\_EVENT\_CHAR\_128\_DISC\_IND event is notified to the application layer.

When the Characteristic discovery has been completed, BLE\_GATTC\_EVENT\_ALL\_CHAR\_DISC\_COMP event is notified to the application layer.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.
[in]	p_range	Retrieval range of Characteristic.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_range parameter is specified as NULL.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_DiscCharByUuid()

```
ble_status_t R_BLE_GATTC_DiscCharByUuid ( uint16_t conn_hdl, uint8_t* p_uuid, uint8_t uuid_type, st_ble_gatt_hdl_range_t* p_range )
```

This function discovers Characteristic specified by uuid within the specified attribute handle range in a GATT Server.

When 16-bit UUID Characteristic has been discovered, BLE\_GATTC\_EVENT\_CHAR\_16\_DISC\_IND event is notified to the application layer.

When 128-bit UUID Characteristic has been discovered, BLE\_GATTC\_EVENT\_CHAR\_128\_DISC\_IND event is notified to the application layer.

When the Characteristic discovery has been completed, BLE\_GATTC\_EVENT\_CHAR\_DISC\_COMP event is notified to the application layer.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.						
[in]	p_uuid	UUID of Characteristic to be discovered.						
[in]	uuid_type	<p>UUID type of Characteristic to be discovered.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)</td> <td>The p_uuid parameter is 16-bit UUID.</td> </tr> <tr> <td>BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)</td> <td>The p_uuid parameter is 128-bit UUID.</td> </tr> </tbody> </table>	macro	description	BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	The p_uuid parameter is 16-bit UUID.	BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	The p_uuid parameter is 128-bit UUID.
macro	description							
BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	The p_uuid parameter is 16-bit UUID.							
BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	The p_uuid parameter is 128-bit UUID.							
[in]	p_range	Retrieval range of Characteristic.						

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_uuid parameter or the p_range parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The uuid_type parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_DiscAllCharDesc()

```
ble_status_t R_BLE_GATTC_DiscAllCharDesc ( uint16_t conn_hdl, st_ble_gatt_hdl_range_t *
p_range )
```

This function discovers Characteristic Descriptor within the specified attribute handle range in a GATT Server.

When 16-bit UUID Characteristic Descriptor has been discovered, BLE\_GATTC\_EVENT\_CHAR\_DESC\_16\_DISC\_IND event is notified to the application layer. When 128-bit UUID Characteristic Descriptor has been discovered, BLE\_GATTC\_EVENT\_CHAR\_DESC\_128\_DISC\_IND event is notified to the application layer. When the Characteristic Descriptor discovery has been completed, BLE\_GATTC\_EVENT\_ALL\_CHAR\_DESC\_DISC\_COMP event is notified to the application layer.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be discovered.
[in]	p_range	Retrieval range of Characteristic Descriptor.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_range parameter is specified as NULL.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_ReadChar()**

```
ble_status_t R_BLE_GATTC_ReadChar ( uint16_t conn_hdl, uint16_t value_hdl )
```

This function reads a Characteristic/Characteristic Descriptor in a GATT Server.

The result of the read is notified in BLE\_GATTC\_EVENT\_CHAR\_READ\_RSP event.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be read.
[in]	value_hdl	Value handle of the Characteristic/Characteristic Descriptor to be read.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	0 is specified in the value_hdl parameter.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_ReadCharUsingUuid()

```
ble_status_t R_BLE_GATTC_ReadCharUsingUuid ( uint16_t conn_hdl, uint8_t* p_uuid, uint8_t
uuid_type, st_ble_gatt_hdl_range_t* p_range )
```

This function reads a Characteristic in a GATT Server using a specified UUID.

The result of the read is notified in BLE\_GATTC\_EVENT\_CHAR\_READ\_BY\_UUID\_RSP event.

#### Parameters

[in]	conn_hdl	Connection handle that identifies Characteristic to be read to GATT Server.						
[in]	p_uuid	UUID of the Characteristic to be read.						
[in]	uuid_type	UUID type of the Characteristic to be read. <table border="1" data-bbox="1075 853 1469 1227"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)</td> <td>The p_uuid parameter is 16-bit UUID.</td> </tr> <tr> <td>BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)</td> <td>The p_uuid parameter is 128-bit UUID.</td> </tr> </tbody> </table>	macro	description	BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	The p_uuid parameter is 16-bit UUID.	BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	The p_uuid parameter is 128-bit UUID.
macro	description							
BLE_GATT_1_6_BIT_UUID_FORMAT(0x01)	The p_uuid parameter is 16-bit UUID.							
BLE_GATT_1_28_BIT_UUID_FORMAT(0x02)	The p_uuid parameter is 128-bit UUID.							
[in]	p_range	Retrieval range of Characteristic.						

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_uuid parameter or the p_range parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The uuid_type parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_ReadLongChar()

```
ble_status_t R_BLE_GATTC_ReadLongChar ( uint16_t conn_hdl, uint16_t value_hdl, uint16_t offset )
```

This function reads a Long Characteristic in a GATT Server.

The contents of the Long Characteristic that has been read is notified every MTU-1 bytes to the application layer by BLE\_GATTC\_EVENT\_CHAR\_READ\_RSP event.

When all of the contents has been received in GATT Client, BLE\_GATTC\_EVENT\_LONG\_CHAR\_READ\_COMP event is notified to the application layer.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be read.
[in]	value_hdl	Value handle of the Long Characteristic to be read.
[in]	offset	Offset that indicates the location to be read. Normally, set 0 to this parameter.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	0 is specified in the value_hdl parameter.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_ReadMultiChar()

```
ble_status_t R_BLE_GATTC_ReadMultiChar ( uint16_t conn_hdl, st_ble_gattc_rd_multi_req_param_t
* p_list )
```

This function reads multiple Characteristics in a GATT Server.

The contents of the multiple Characteristics that has been read is notified to the application layer by BLE\_GATTC\_EVENT\_MULTI\_CHAR\_READ\_RSP event.

#### Parameters

[in]	conn_hdl	Connection handle that identifies Characteristic to be read to GATT Server.
[in]	p_list	List of Value Handles that point the Characteristics to be read.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_list parameter or the p_hdl_list field in the p_list parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	0 is specified in the list_count field in the p_list parameter.
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_WriteCharWithoutRsp()

```
ble_status_t R_BLE_GATTC_WriteCharWithoutRsp ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t
* p_write_data )
```

This function writes a Characteristic in a GATT Server without response.

The result is returned from the API.

#### Parameters

[in]	conn_hdl	Connection handle that identifies Characteristic to be read to GATT Server.
[in]	p_write_data	Value to be written to the Characteristic.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_write_data parameter or the p_value field in the value field in the p_write_data parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• 0 is specified in the value_len field in the p_value field in the p_write_data parameter.</li> <li>• 0 is specified in the attr_hdl field in the p_write_data parameter.</li> </ul>
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

◆ **R\_BLE\_GATTC\_SignedWriteChar()**

```
ble_status_t R_BLE_GATTC_SignedWriteChar ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t *
p_write_data )
```

This function writes Signed Data to a Characteristic in a GATT Server without response.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be written.
[in]	p_write_data	Signed Data to be written to the Characteristic.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_write_data parameter or the p_value field in the value field in the p_write_data parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• 0 is specified in the value_len field in the value field in the p_write_data parameter.</li> <li>• 0 is specified in the attr_hdl field in the p_write_data parameter.</li> </ul>
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function or Signed Data.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_WriteChar()

```
ble_status_t R_BLE_GATTC_WriteChar ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t *
p_write_data )
```

This function writes a Characteristic in a GATT Server.

The result of the write is notified in BLE\_GATTC\_EVENT\_CHAR\_WRITE\_RSP event.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be written.
[in]	p_write_data	Value to be written to the Characteristic.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_write_data parameter or the p_value field in the value field in the p_write_data parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• 0 is specified in the value_len field in the value field in the p_write_data parameter.</li> <li>• 0 is specified in the attr_hdl field in the p_write_data parameter.</li> </ul>
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_WriteLongChar()

```
ble_status_t R_BLE_GATTC_WriteLongChar ( uint16_t conn_hdl, st_ble_gatt_hdl_value_pair_t *
p_write_data, uint16_t offset )
```

This function writes a Long Characteristic in a GATT Server.

The result of a write that has been done every segmentation is notified to the application layer in BLE\_GATTC\_EVENT\_CHAR\_PART\_WRITE\_RSP event.

The maximum writable size to a Long Characteristic with this function is 512 bytes.

When all of the contents has been written to the Long Characteristic,

BLE\_GATTC\_EVENT\_LONG\_CHAR\_WRITE\_COMP event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the GATT Server to be written.
[in]	p_write_data	Value to be written to the Long Characteristic.
[in]	offset	Offset that indicates the location to be written. Normally, set 0 to this parameter. If this parameter sets to a value other than 0, adjust the offset parameter and the length of the value to be written not to exceed the length of the Long Characteristic.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_write_data parameter or the p_value field in the value field in the p_write_data parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>• The value_len field in the value field in the p_write_data parameter is 0.</li> <li>• The sum of the value_len field in the value field in the p_write_data parameter and the offset parameter larger than 512.</li> <li>• The attr_hdl field in the p_write_data parameter is 0.</li> </ul>
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

### ◆ R\_BLE\_GATTC\_ReliableWrites()

```
ble_status_t R_BLE_GATTC_ReliableWrites ( uint16_t conn_hdl,
st_ble_gattc_reliable_writes_char_pair_t* p_char_pair, uint8_t pair_num, uint8_t auto_flag )
```

This function performs the Reliable Writes procedure described in GATT Specification.

When the data written to the Characteristic has been transmitted, BLE\_GATTC\_EVENT\_CHAR\_PART\_WRITE\_RSP event is notified to the application layer. If the data included in the event is different from the data that GATT Client has sent, host stack automatically cancels the Reliable Writes.

After all of the contents has been sent to the GATT Server, if the auto\_flag parameter has been set to BLE\_GATTC\_EXEC\_AUTO, the GATT Server automatically writes the data to the Characteristic. If the auto\_flag parameter has been set to BLE\_GATTC\_EXEC\_NOT\_AUTO, BLE\_GATTC\_EVENT\_RELIABLE\_WRITES\_TX\_COMP event notifies the application layer in GATT Client that all of the contents has been sent to the GATT Server. Then GATT Client requests for writing the data to the Characteristic to the GATT Server with R\_BLE\_GATTC\_ExecWrite(). When the write has been done, BLE\_GATTC\_EVENT\_RELIABLE\_WRITES\_COMP event is notified to the application layer.

#### Parameters

[in]	conn_hdl	Connection handle identifying the GATT Server to be written.						
[in]	p_char_pair	Pair of Characteristic Value and Characteristic Value Handle identifying the Characteristic to be written by Reliable Writes.						
[in]	pair_num	The number of the pairs specified by the p_char_pair parameter. Valid range is 0 < pair_num ≤ BLE_GATTC_RELIABLE_WRITES_MAX_CHAR_PAIR.						
[in]	auto_flag	The flag that indicates whether auto execution or not. <table border="1" data-bbox="1072 1570 1469 1874"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_GATTC_EXEC_AUTO(0x01)</td> <td>Auto execution.</td> </tr> <tr> <td>BLE_GATTC_EXEC_NOT_AUTO (0x02)</td> <td>Not auto execution.</td> </tr> </tbody> </table>	macro	description	BLE_GATTC_EXEC_AUTO(0x01)	Auto execution.	BLE_GATTC_EXEC_NOT_AUTO (0x02)	Not auto execution.
macro	description							
BLE_GATTC_EXEC_AUTO(0x01)	Auto execution.							
BLE_GATTC_EXEC_NOT_AUTO (0x02)	Not auto execution.							

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The reason for this error is as follows:

	<ul style="list-style-type: none"> <li>The p_char_pair parameter is specified as NULL.</li> <li>The p_value field in the value field in the write_data field in the p_char_pair parameter is specified as NULL.</li> </ul>
BLE_ERR_INVALID_ARG(0x0003)	<p>The reason for this error is as follows:</p> <ul style="list-style-type: none"> <li>The pair_num parameter or the auto_flag parameter is out of range.</li> <li>The value_len field in the value field in the write_data field in the p_char_pair parameter is 0.</li> </ul>
BLE_ERR_INVALID_OPERATION(0x0009)	While processing other request, this function was called.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function or to store the temporary write data.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

## ◆ R\_BLE\_GATTC\_ExecWrite()

```
ble_status_t R_BLE_GATTC_ExecWrite ( uint16_t conn_hdl, uint8_t exe_flag )
```

If the auto execute of Reliable Writes is not specified by [R\\_BLE\\_GATTC\\_ReliableWrites\(\)](#), this function is used to execute a write to Characteristic.

When all of the contents has been sent to the GATT Server, BLE\_GATTC\_EVENT\_RELIABLE\_WRITES\_TX\_COMP event notifies the application layer. After this event has been received, execute the write by this function. The result of the write is notified by BLE\_GATTC\_EVENT\_RELIABLE\_WRITES\_COMP event.

### Parameters

[in]	conn_hdl	Connection handle identifying the target GATT Server.						
[in]	exe_flag	The flag that indicates whether execution or cancellation. <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GATTC_EXECUTE_WRITE_CANCEL_FLAG(0x00)</a></td> <td>Execute the write.</td> </tr> <tr> <td><a href="#">BLE_GATTC_EXECUTE_WRITE_FLAG(0x01)</a></td> <td>Cancel the write.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GATTC_EXECUTE_WRITE_CANCEL_FLAG(0x00)</a>	Execute the write.	<a href="#">BLE_GATTC_EXECUTE_WRITE_FLAG(0x01)</a>	Cancel the write.
macro	description							
<a href="#">BLE_GATTC_EXECUTE_WRITE_CANCEL_FLAG(0x00)</a>	Execute the write.							
<a href="#">BLE_GATTC_EXECUTE_WRITE_FLAG(0x01)</a>	Cancel the write.							

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The exe_flag parameter is out of range.
BLE_ERR_INVALID_OPERATION(0x0009)	The reason for this error is as follows: <ul style="list-style-type: none"> <li>GATT Client has not requested for Reliable Writes by <a href="#">R_BLE_GATTC_ReliableWrites()</a>.</li> <li>Although auto execution has been specified by <a href="#">R_BLE_GATTC_ReliableWrites()</a>, this function was called.</li> </ul>
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The GATT Server specified by conn_hdl was not found.

#### 4.2.5.5 L2CAP

Modules » [Bluetooth Low Energy Library \(r\\_ble\)](#)

##### Functions

`ble_status_t` [R\\_BLE\\_L2CAP\\_RegisterCfPsm](#) ([ble\\_l2cap\\_cf\\_app\\_cb\\_t](#) cb, `uint16_t` psm, `uint16_t` lwm)

This function registers PSM that uses L2CAP CBFC Channel and a callback for L2CAP event. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_DeregisterCfPsm](#) (`uint16_t` psm)

This function stops the use of the L2CAP CBFC Channel specified by the psm parameter and deregisters the callback function for L2CAP event. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_ReqCfConn](#) (`uint16_t` conn\_hdl, [st\\_ble\\_l2cap\\_conn\\_req\\_param\\_t](#) \*p\_conn\_req\_param)

This function sends a connection request for L2CAP CBFC Channel. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_RspCfConn](#) ([st\\_ble\\_l2cap\\_conn\\_rsp\\_param\\_t](#) \*p\_conn\_rsp\_param)

This function replies to the connection request for L2CAP CBFC Channel from the remote device. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_DisconnectCf](#) (`uint16_t` lcid)

This function sends a disconnection request for L2CAP CBFC Channel. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_SendCfCredit](#) (`uint16_t` lcid, `uint16_t` credit)

This function sends credit to a remote device. [More...](#)

`ble_status_t` [R\\_BLE\\_L2CAP\\_SendCfData](#) (`uint16_t` conn\_hdl, `uint16_t` lcid, `uint16_t` data\_len, `uint8_t` \*p\_sdu)

This function sends the data to a remote device via L2CAP CBFC Channel. [More...](#)

## Detailed Description

### Data Structures

struct [st\\_ble\\_l2cap\\_conn\\_req\\_param\\_t](#)  
L2CAP CBFC Channel connection request parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_conn\\_rsp\\_param\\_t](#)  
L2CAP CBFC Channel connection response parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_cf\\_conn\\_evt\\_t](#)  
L2CAP CBFC Channel connection parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_cf\\_data\\_evt\\_t](#)  
Sent/Received Data parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_cf\\_credit\\_evt\\_t](#)  
Credit parameters of local or remote device. [More...](#)

struct [st\\_ble\\_l2cap\\_cf\\_disconn\\_evt\\_t](#)  
Disconnection parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_rej\\_evt\\_t](#)  
Command Reject parameters. [More...](#)

struct [st\\_ble\\_l2cap\\_cf\\_evt\\_data\\_t](#)  
[st\\_ble\\_l2cap\\_cf\\_evt\\_data\\_t](#) is the type of the data notified in a L2CAP Event. [More...](#)

### Macros

#define [BLE\\_L2CAP\\_MAX\\_CBFC\\_PSM](#)  
The maximum number of callbacks that host stack can register.

#define [BLE\\_L2CAP\\_CF\\_RSP\\_SUCCESS](#)  
Notify the remote device that the connection can be established.

```
#define BLE_L2CAP_CF_RSP_RFSD_INSF_AUTH
```

Notify the remote device that the connection can not be established because of insufficient authentication.

```
#define BLE_L2CAP_CF_RSP_RFSD_INSF_AUTRZ
```

Notify the remote device that the connection can not be established because of insufficient Authorization.

```
#define BLE_L2CAP_CF_RSP_RFSD_INSF_ENC_KEY
```

Notify the remote device that the connection can not be established because of Encryption Key Size.

```
#define BLE_L2CAP_CF_RSP_RFSD_INSF_ENC
```

Notify the remote device that the connection can not be established because of Encryption.

```
#define BLE_L2CAP_CF_RSP_RFSD_UNAC_PARAM
```

Notify the remote device that the connection can not be established because the parameters is unacceptable to local device.

## Typedefs

```
typedef void(* ble_l2cap_cf_app_cb_t) (uint16_t event_type, ble_status_t event_result, st_ble_l2cap_cf_evt_data_t *p_event_data)
```

ble\_l2cap\_cf\_app\_cb\_t is the L2CAP Event callback function type.  
[More...](#)

## Enumerations

```
enum e_r_ble_l2cap_cf_evt_t
```

L2CAP Event Identifier. [More...](#)

## Data Structure Documentation

### ◆ st\_ble\_l2cap\_conn\_req\_param\_t

struct st_ble_l2cap_conn_req_param_t		
L2CAP CBFC Channel connection request parameters.		
Data Fields		
uint16_t	local_psm	Identifier indicating the

		protocol/profile that uses L2CAP CBFC Channel on local device.
uint16_t	remote_psm	Identifier indicating the protocol/profile that uses L2CAP CBFC Channel on remote device.
uint16_t	mtu	MTU size(byte) receivable on L2CAP CBFC Channel.
uint16_t	mps	MPS size(byte) receivable on L2CAP CBFC Channel.
uint16_t	credit	The number of LE-Frame that local device can receive.

◆ **st\_ble\_l2cap\_conn\_rsp\_param\_t**

struct st_ble_l2cap_conn_rsp_param_t										
L2CAP CBFC Channel connection response parameters.										
Data Fields										
uint16_t	lcid	CID identifying the L2CAP CBFC Channel on local device. The valid range is 0x40-0x40 + BLE_L2CAP_MAX_CBFC_PSM - 1.								
uint16_t	response	<p>The response to the connection request. Select one of the following.</p> <table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_L2CAP_CF_RSP_SUCCESS(0x0000)</a></td> <td>Notify the remote device that the connection can be established.</td> </tr> <tr> <td><a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTH(0x0005)</a></td> <td>Notify the remote device that the connection can not be established because of insufficient authentication</td> </tr> <tr> <td><a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTHZ(0x0006)</a></td> <td>Notify the remote device that the connection can not be established</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_L2CAP_CF_RSP_SUCCESS(0x0000)</a>	Notify the remote device that the connection can be established.	<a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTH(0x0005)</a>	Notify the remote device that the connection can not be established because of insufficient authentication	<a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTHZ(0x0006)</a>	Notify the remote device that the connection can not be established
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<a href="#">BLE_L2CAP_CF_RSP_SUCCESS(0x0000)</a>	Notify the remote device that the connection can be established.									
<a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTH(0x0005)</a>	Notify the remote device that the connection can not be established because of insufficient authentication									
<a href="#">BLE_L2CAP_CF_RSP_RFSD_INSUF_AUTHZ(0x0006)</a>	Notify the remote device that the connection can not be established									

		<p>because of insufficient Authorization.</p> <p><a href="#">BLE_L2CAP_C_F_RSP_RFSD_I_NSF_ENC_KEY(0x0007)</a> Notify the remote device that the connection can not be established because of Encryption Key Size.</p> <p><a href="#">BLE_L2CAP_C_F_RSP_RFSD_I_NSF_ENC(0x0008)</a> Notify the remote device that the connection can not be established because of Encryption.</p> <p><a href="#">BLE_L2CAP_C_F_RSP_RFSD_UNAC_PARAM(0x000B)</a> Notify the remote device that the connection can not be established because the parameters is unacceptable to local device.</p>
uint16_t	mtu	MTU(byte) of packet that L2CAP CBFC Channel on local device can receive.
uint16_t	mps	MPS(byte) of packet that L2CAP CBFC Channel on local device can receive.
uint16_t	credit	The number of LE-Frame that L2CAP CBFC Channel on local device can receive.

◆ **st\_ble\_l2cap\_cf\_conn\_evt\_t**

struct st_ble_l2cap_cf_conn_evt_t		
L2CAP CBFC Channel connection parameters.		
Data Fields		
uint16_t	cid	CID identifying the L2CAP CBFC Channel.
uint16_t	psm	PSM allocated by the cid field.

uint16_t	mtu	MTU of local/remote device.
uint16_t	mps	MPS of local/remote device.
uint16_t	credit	Credit of local/remote device.

#### ◆ st\_ble\_l2cap\_cf\_data\_evt\_t

struct st_ble_l2cap_cf_data_evt_t		
Sent/Received Data parameters.		
Data Fields		
uint16_t	cid	CID identifying the L2CAP CBFC Channel that has sent or received the data .
uint16_t	psm	PSM allocated by the cid field.
uint16_t	data_len	Data length.
uint8_t*	p_data	Sent/Received data.

#### ◆ st\_ble\_l2cap\_cf\_credit\_evt\_t

struct st_ble_l2cap_cf_credit_evt_t		
Credit parameters of local or remote device.		
Data Fields		
uint16_t	cid	CID identifying the L2CAP CBFC Channel.
uint16_t	psm	PSM allocated by the cid field.
uint16_t	credit	Current credit of local/remote device.

#### ◆ st\_ble\_l2cap\_cf\_disconn\_evt\_t

struct st_ble_l2cap_cf_disconn_evt_t		
Disconnection parameters.		
Data Fields		
uint16_t	cid	CID identifying the L2CAP CBFC Channel that has been disconnected.

#### ◆ st\_ble\_l2cap\_rej\_evt\_t

struct st_ble_l2cap_rej_evt_t		
Command Reject parameters.		
Data Fields		
uint16_t	reason	The reason that the remote device has sent Command Reject.

uint16_t	data_1	Optional information about the reason that the remote device has sent Command Reject.
uint16_t	data_2	Optional information about the reason that the remote device has sent Command Reject.

#### ◆ st\_ble\_l2cap\_cf\_evt\_data\_t

struct st_ble_l2cap_cf_evt_data_t		
st_ble_l2cap_cf_evt_data_t is the type of the data notified in a L2CAP Event.		
Data Fields		
uint16_t	conn_hdl	Connection handle identifying the remote device.
uint16_t	param_len	The size of L2CAP Event parameters.
void *	p_param	L2CAP Event parameters. This parameter differs in each L2CAP Event.

### Typedef Documentation

#### ◆ ble\_l2cap\_cf\_app\_cb\_t

ble_l2cap_cf_app_cb_t		
ble_l2cap_cf_app_cb_t is the L2CAP Event callback function type.		
<b>Parameters</b>		
[in]	event_type	The type of L2CAP Event.
[in]	event_result	The result of L2CAP Event
[in]	p_event_data	Data notified by L2CAP Event.
<b>Returns</b>		
none		

### Enumeration Type Documentation

## ◆ e\_r\_ble\_l2cap\_cf\_evt\_t

enum e\_r\_ble\_l2cap\_cf\_evt\_t

L2CAP Event Identifier.

## Enumerator

BLE\_L2CAP\_EVENT\_CF\_CONN\_CNF

After the connection request for L2CAP CBFC Channel has been sent with [R\\_BLE\\_L2CAP\\_ReqCfConn\(\)](#), when the L2CAP CBFC Channel connection response has been received, BLE\_L2CAP\_EVENT\_CF\_CONN\_CNF event occurs.

**Event Code: 0x5001****result:**

BLE_SUCCESS(0x000)	Success
BLE_ERR_RSP_TIMEOUT(0x0011)	L2CAP Command timeout.
BLE_ERR_L2CAP_PSM_NOT_SUPPORTED(0x4002)	PSM specified by <a href="#">R_BLE_L2CAP_ReqCfConn()</a> is not supported.
BLE_ERR_L2CAP_NO_RESOURCE(0x4004)	No resource for connection.
BLE_ERR_L2CAP_INSUF_AUTHEN(0x4005)	Insufficient authentication.
BLE_ERR_L2CAP_INSUF_AUTHOR(0x4006)	Insufficient authorization.
BLE_ERR_L2CAP_INSUF_ENC_KEY_SIZE(0x4007)	Insufficient encryption key size.
BLE_ERR_L2CAP_INSUF_ENC(0x4008)	Insufficient encryption.
BLE_ERR_L2CAP_INVALID_SOURCE_CID(0x4009)	Invalid Source CID.
BLE_ERR_L2CAP_SOURCE_CID_ALREADY_ALLOCATED(0x400A)	Source CID already allocated.

	<p>BLE_ERR_L2CAP_R EFUSE_UNACCEPT ABLE_PARAM(0x40 0B)</p> <p>Unacceptable parameters.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_conn_evt_t</a></p>
BLE_L2CAP_EVENT_CF_CONN_IND	<p>When a connection request for L2CAP CBFC Channel has been received from a remote device, BLE_L2CAP_EVENT_CF_CONN_IND event occurs.</p> <p><b>Event Code: 0x5002</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_NOT_FOUND(0x000D) CF connection request has not been received or lcid not found.</p> <p>BLE_ERR_L2CAP_PSM_NOT_SUPPORTED(0x4002) PSM specified by <a href="#">R_BLE_L2CAP_ReqCfConn()</a> is not supported.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_conn_evt_t</a></p>
BLE_L2CAP_EVENT_CF_DISCONN_CNF	<p>After local device has sent a disconnection request for L2CAP CBFC Channel by <a href="#">R_BLE_L2CAP_DisconnectCf()</a>, when the local device has received the response, BLE_L2CAP_EVENT_CF_DISCONN_CNF event occurs.</p> <p><b>Event Code: 0x5003</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_disconn_evt_t</a></p>
BLE_L2CAP_EVENT_CF_DISCONN_IND	<p>When local device has received a disconnection request for L2CAP CBFC Channel</p>

	<p>from the remote device, BLE_L2CAP_EVENT_CF_DISCONN_IND event occurs. Host stack automatically replies the to the disconnection request.</p> <p><b>Event Code: 0x5004</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_disconn_evt_t</a></p>
BLE_L2CAP_EVENT_CF_RX_DATA_IND	<p>When local device has received data on L2CAP CBFC Channel, BLE_L2CAP_EVENT_CF_RX_DATA_IND event occurs.</p> <p><b>Event Code: 0x5005</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_data_evt_t</a></p>
BLE_L2CAP_EVENT_CF_LOW_RX_CRD_IND	<p>When the credit of the L2CAP CBFC Channel has reached the Low Water Mark, BLE_L2CAP_EVENT_CF_LOW_RX_CRD_IND event occurs.</p> <p><b>Event Code: 0x5006</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_credit_evt_t</a></p>
BLE_L2CAP_EVENT_CF_TX_CRD_IND	<p>When local device has received credit from a remote device, BLE_L2CAP_EVENT_CF_TX_CRD_IND event occurs.</p>

	<p><b>Event Code: 0x5007</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_credit_evt_t</a></p>
BLE_L2CAP_EVENT_CF_TX_DATA_CNF	<p>When the data transmission has been completed from host stack to Controller, BLE_L2CAP_EVENT_CF_TX_DATA_CNF event occurs.</p> <p><b>Event Code: 0x5008</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p style="padding-left: 40px;">BLE_ERR_DISCONN While transmitting ECTED(0x000F) data, L2CAP CBFC Channel has been disconnected.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_cf_data_evt_t</a></p>
BLE_L2CAP_EVENT_CMD_REJ	<p>When local device has received Command Reject PDU, BLE_L2CAP_EVENT_CMD_REJ event occurs.</p> <p><b>Event Code: 0x5009</b></p> <p><b>result:</b></p> <p style="padding-left: 40px;">BLE_SUCCESS(0x0 Success 000)</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_l2cap_rej_evt_t</a></p>

## Function Documentation

---

◆ **R\_BLE\_L2CAP\_RegisterCfPsm()**

```
ble_status_t R_BLE_L2CAP_RegisterCfPsm ( ble_l2cap_cf_app_cb_t cb, uint16_t psm, uint16_t lwm )
```

This function registers PSM that uses L2CAP CBFC Channel and a callback for L2CAP event.

Only one callback is available per PSM. Configure in each PSM the Low Water Mark of the LE-Frames that the local device can receive.

When the number of the credit reaches the Low Water Mark, BLE\_L2CAP\_EVENT\_CF\_LOW\_RX\_CRD\_IND event is notified to the application layer.

The number of PSM is defined as BLE\_L2CAP\_MAX\_CBFC\_PSM.

The result of this API call is returned by a return value.

**Parameters**

	[in]	cb	Callback function for L2CAP event.									
	[in]	psm	Identifier indicating the protocol/profile that uses L2CAP CBFC Channel. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="width: 20%;">type</th> <th style="width: 20%;">range</th> <th style="width: 60%;">description</th> </tr> </thead> <tbody> <tr> <td>Fixed, SIG assigned</td> <td>0x0001 - 0x007F</td> <td>PSM defined by SIG. For more information on PSM, refer Bluetooth SIG Assigned Number (<a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a>).</td> </tr> <tr> <td>Dynamically allocated</td> <td>0x0080 - 0x00FF</td> <td>Statically allocated PSM by custom protocol or dynamically</td> </tr> </tbody> </table>	type	range	description	Fixed, SIG assigned	0x0001 - 0x007F	PSM defined by SIG. For more information on PSM, refer Bluetooth SIG Assigned Number ( <a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a> ).	Dynamically allocated	0x0080 - 0x00FF	Statically allocated PSM by custom protocol or dynamically
type	range	description										
Fixed, SIG assigned	0x0001 - 0x007F	PSM defined by SIG. For more information on PSM, refer Bluetooth SIG Assigned Number ( <a href="https://www.bluetooth.com/specifications/assigned-numbers">https://www.bluetooth.com/specifications/assigned-numbers</a> ).										
Dynamically allocated	0x0080 - 0x00FF	Statically allocated PSM by custom protocol or dynamically										

			y allocated PSM by GATT Service.
[in]	lwm		Low Water Mark that indicates the LE-Frame numbers that the local device can receive.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The cb parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The psm parameter is out of range.
BLE_ERR_CONTEXT_FULL(0x000B)	More than BLE_L2CAP_MAX_CBFC_PSM+1 PSMs, callbacks has been registered.

**◆ R\_BLE\_L2CAP\_DeregisterCfPsm()**

```
ble_status_t R_BLE_L2CAP_DeregisterCfPsm ( uint16_t psm)
```

This function stops the use of the L2CAP CBFC Channel specified by the psm parameter and deregisters the callback function for L2CAP event.

The result of this API call is returned by a return value.

**Parameters**

[in]	psm	PSM that is to be stopped to use the L2CAP CBFC Channel. Set the PSM registered by <a href="#">R_BLE_L2CAP_RegisterCfPsm()</a> .
------	-----	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_NOT_FOUND(0x000D)	The callback function allocated by the psm parameter is not found.

◆ **R\_BLE\_L2CAP\_ReqCfConn()**

```
ble_status_t R_BLE_L2CAP_ReqCfConn ( uint16_t conn_hdl, st_ble_l2cap_conn_req_param_t *
p_conn_req_param )
```

This function sends a connection request for L2CAP CBFC Channel.

The connection response is notified by BLE\_L2CAP\_EVENT\_CF\_CONN\_CNF event.

The result of this API call is returned by a return value.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device that the connection request is sent to.
[in]	p_conn_req_param	Connection request parameters.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_conn_req_param parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The mtu parameter or the mps parameter is out of range.
BLE_ERR_INVALID_STATE(0x0008)	CF Channel connection has not been established.
BLE_ERR_CONTEXT_FULL(0x000B)	New CF Channel can not be registered or other L2CAP Command is processing.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	Insufficient memory is needed to generate this function.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by conn_hdl is not found.
BLE_ERR_NOT_YET_READY(0x0012)	The psm parameter is not registered.

◆ **R\_BLE\_L2CAP\_RspCfConn()**

```
ble_status_t R_BLE_L2CAP_RspCfConn ( st_ble_l2cap_conn_rsp_param_t* p_conn_rsp_param)
```

This function replies to the connection request for L2CAP CBFC Channel from the remote device.

The connection request is notified by BLE\_L2CAP\_EVENT\_CF\_CONN\_IND event. The result of this API call is returned by a return value.

**Parameters**

[in]	p_conn_rsp_param	Connection response parameters.
------	------------------	---------------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_conn_rsp_param parameter is specified as NULL.
BLE_ERR_NOT_FOUND(0x000D)	A connection request for L2CAP CBFC Channel has not been received, or CID specified by the lcid field in the p_conn_rsp_param parameter is not found.

◆ **R\_BLE\_L2CAP\_DisconnectCf()**

```
ble_status_t R_BLE_L2CAP_DisconnectCf ( uint16_t lcid)
```

This function sends a disconnection request for L2CAP CBFC Channel.

When L2CAP CBFC Channel has been disconnected, BLE\_L2CAP\_EVENT\_CF\_DISCONN\_CNF event is notified to the application layer.

**Parameters**

[in]	lcid	CID identifying the L2CAP CBFC Channel that has been disconnected. The valid range is 0x40 - (0x40 + BLE_L2CAP_MAX_CBFC_PSM - 1).
------	------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_OPERATION(0x0009)	CF Channel connection has not been established.
BLE_ERR_CONTEXT_FULL(0x000B)	This function was called while processing other L2CAP command.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for L2CAP Command.
BLE_ERR_NOT_FOUND(0x000D)	CID specified the lcid parameter is not found.

◆ **R\_BLE\_L2CAP\_SendCfCredit()**

```
ble_status_t R_BLE_L2CAP_SendCfCredit ( uint16_t lcid, uint16_t credit )
```

This function sends credit to a remote device.

In L2CAP CBFC communication, if credit is 0, the remote device stops data transmission. Therefore when processing the received data has been completed and local device affords to receive data, the remote device is notified of the number of LE-Frame that local device can receive by this function and local device can continue to receive data from the remote device. The result of this API call is returned by a return value.

**Parameters**

[in]	lcid	CID identifying the L2CAP CBFC Channel on local device that sends credit.
[in]	credit	Credit to be sent to the remote device.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The credit parameter is set to 0.
BLE_ERR_CONTEXT_FULL(0x000B)	This function was called while processing other L2CAP command.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for L2CAP Command.

◆ **R\_BLE\_L2CAP\_SendCfData()**

```
ble_status_t R_BLE_L2CAP_SendCfData ( uint16_t conn_hdl, uint16_t lcid, uint16_t data_len,
uint8_t * p_sdu )
```

This function sends the data to a remote device via L2CAP CBFC Channel.

When the data transmission to Controller has been completed, BLE\_L2CAP\_EVENT\_CF\_TX\_DATA\_CNF event is notified to the application layer.

**Parameters**

[in]	conn_hdl	Connection handle identifying the remote device to be sent the data.
[in]	lcid	CID identifying the L2CAP CBFC Channel on local device used in the data transmission.
[in]	data_len	Length of the data.
[in]	p_sdu	Service Data Unit. Input the data length specified by the data_len parameter to the first 2 bytes (Little Endian).

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_data parameter is specified as NULL.
BLE_ERR_INVALID_ARG(0x0003)	The length parameter is out of range.
BLE_ERR_INVALID_STATE(0x0008)	CF Channel connection has not been established or the data whose length exceeds the MTU has been sent.
BLE_ERR_ALREADY_IN_PROGRESS(0x000A)	Data transmission has been already started.
BLE_ERR_CONTEXT_FULL(0x000B)	L2CAP task queue is full.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for L2CAP Command.
BLE_ERR_NOT_FOUND(0x000D)	CID specified the lcid parameter is not found.
BLE_ERR_INVALID_HDL(0x000E)	The remote device specified by the conn_hdl parameter is not found.

### 4.2.5.6 VS

#### Modules » Bluetooth Low Energy Library (r\_ble)

#### Functions

ble_status_t	<a href="#">R_BLE_VS_Init</a> (ble_vs_app_cb_t vs_cb) This function initializes Vendor Specific API and registers a callback function for Vendor Specific Event. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_StartTxTest</a> (st_ble_vs_tx_test_param_t *p_tx_test_param) This function starts extended Transmitter Test. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_StartRxTest</a> (st_ble_vs_rx_test_param_t *p_rx_test_param) This function starts extended Receiver Test. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_EndTest</a> (void) This function terminates the extended transmitter or receiver test. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_SetTxPower</a> (uint16_t conn_hdl, uint8_t tx_power) This function configures transmit power. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_GetTxPower</a> (uint16_t conn_hdl) This function gets transmit power. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_SetCodingScheme</a> (uint8_t coding_scheme) This function configure default Coding scheme(S=8 or S=2) that is used in the case of selecting Coded PHY in Primary advertising PHY or Secondary advertising PHY advertising or request for link establishment. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_SetRfControl</a> (st_ble_vs_set_rf_ctrl_param_t *p_rf_ctrl) This function performs power control on RF. <a href="#">More...</a>
ble_status_t	<a href="#">R_BLE_VS_SetBdAddr</a> (uint8_t area, st_ble_dev_addr_t *p_addr) This function sets public/random address of local device to the area specified by the parameter. <a href="#">More...</a>

ble\_status\_t [R\\_BLE\\_VS\\_GetBdAddr](#) (uint8\_t area, uint8\_t addr\_type)  
This function gets currently configured public/random address. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_GetRand](#) (uint8\_t rand\_size)  
This function generates 4-16 bytes of random number used in creating keys. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_StartTxFlowEvtNtf](#) (void)  
This function starts the notification(BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event) of the state transition of TxFlow. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_StopTxFlowEvtNtf](#) (void)  
This function stops the notification(BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event) of the state transition of TxFlow. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_GetTxBufferNum](#) (uint32\_t \*p\_buffer\_num)  
This function retrieves the number of the available transmission packet buffers. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_SetTxLimit](#) (uint32\_t tx\_queue\_lwm, uint32\_t tx\_queue\_hwm)  
This function sets the threshold for notifying the application layer of the TxFlow state. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_SetScanChMap](#) (uint16\_t ch\_map)  
This function sets the scan channel map. [More...](#)

ble\_status\_t [R\\_BLE\\_VS\\_GetScanChMap](#) (void)  
This function gets currently scan channel map. [More...](#)

## Detailed Description

### Data Structures

struct [st\\_ble\\_vs\\_tx\\_test\\_param\\_t](#)

This is the extended transmitter test parameters used in [R\\_BLE\\_VS\\_StartTxTest\(\)](#). [More...](#)

struct [st\\_ble\\_vs\\_rx\\_test\\_param\\_t](#)

This is the extended receiver test parameters used in [R\\_BLE\\_VS\\_StartRxTest\(\)](#). [More...](#)

struct [st\\_ble\\_vs\\_set\\_rf\\_ctrl\\_param\\_t](#)

This is the RF parameters used in [R\\_BLE\\_VS\\_SetRfControl\(\)](#). [More...](#)

struct [st\\_ble\\_vs\\_test\\_end\\_evt\\_t](#)

This structure notifies that the extended test has been terminated. [More...](#)

struct [st\\_ble\\_vs\\_set\\_tx\\_pwr\\_comp\\_evt\\_t](#)

This structure notifies that tx power has been set. [More...](#)

struct [st\\_ble\\_vs\\_get\\_tx\\_pwr\\_comp\\_evt\\_t](#)

This structure notifies that tx power has been retrieved. [More...](#)

struct [st\\_ble\\_vs\\_set\\_rf\\_ctrl\\_comp\\_evt\\_t](#)

This structure notifies that RF has been configured. [More...](#)

struct [st\\_ble\\_vs\\_get\\_bd\\_addr\\_comp\\_evt\\_t](#)

This structure notifies that BD\_ADDR has been retrieved. [More...](#)

struct [st\\_ble\\_vs\\_get\\_rand\\_comp\\_evt\\_t](#)

This structure notifies that random number has been generated. [More...](#)

struct [st\\_ble\\_vs\\_tx\\_flow\\_chg\\_evt\\_t](#)

This structure notifies that the state transition of TxFlow has been changed. [More...](#)

struct [st\\_ble\\_vs\\_evt\\_data\\_t](#)

[st\\_ble\\_vs\\_evt\\_data\\_t](#) is the type of the data notified in a Vendor

Specific Event. [More...](#)

struct [st\\_ble\\_vs\\_get\\_scan\\_ch\\_map\\_comp\\_evt\\_t](#)

This structure notifies that current scan channel map. [More...](#)

## Macros

`#define` [BLE\\_VS\\_TX\\_POWER\\_HIGH](#)

High power level.

`#define` [BLE\\_VS\\_TX\\_POWER\\_MID](#)

Middle power level.

`#define` [BLE\\_VS\\_TX\\_POWER\\_LOW](#)

Low power level.

`#define` [BLE\\_VS\\_ADDR\\_AREA\\_REG](#)

Address in register is written or read.

`#define` [BLE\\_VS\\_ADDR\\_AREA\\_DATA\\_FLASH](#)

Address in DataFlash is written or read.

`#define` [BLE\\_VS\\_EH\\_TX\\_PL\\_PRBS9](#)

PRBS9 sequence '1111111100000111101..'.  
'1111111100000111101..'

`#define` [BLE\\_VS\\_EH\\_TX\\_PL\\_11110000](#)

Repeated '11110000'.

`#define` [BLE\\_VS\\_EH\\_TX\\_PL\\_10101010](#)

Repeated '10101010'.

`#define` [BLE\\_VS\\_EH\\_TX\\_PL\\_PRBS15](#)

PRBS15 sequence.

`#define` [BLE\\_VS\\_EH\\_TX\\_PL\\_11111111](#)

Repeated '11111111'.

```
#define BLE_VS_EH_TX_PL_00000000  
Repeated '00000000'.
```

```
#define BLE_VS_EH_TX_PL_00001111  
Repeated '00001111'.
```

```
#define BLE_VS_EH_TX_PL_01010101  
Repeated '01010101'.
```

```
#define BLE_VS_EH_TEST_PHY_1M  
1M PHY used in Transmitter/Receiver test.
```

```
#define BLE_VS_EH_TEST_PHY_2M  
2M PHY used in Transmitter/Receiver test.
```

```
#define BLE_VS_EH_TEST_PHY_CODED  
Coded PHY used in Receiver test.
```

```
#define BLE_VS_EH_TEST_PHY_CODED_S_8  
Coded PHY(S=8) used in Transmitter test.
```

```
#define BLE_VS_EH_TEST_PHY_CODED_S_2  
Coded PHY(S=2) used in Transmitter test.
```

```
#define BLE_VS_RF_OFF  
RF power off.
```

```
#define BLE_VS_RF_ON  
RF power on.
```

```
#define BLE_VS_RF_INIT_PARAM_NOT_CHG  
The parameters are not changed in RF power on.
```

```
#define BLE_VS_RF_INIT_PARAM_CHG
```

The parameters are changed in RF power on.

```
#define BLE_VS_CS_PRIM_ADV_S_8
```

Coding scheme for Primary Advertising PHY(S=8).

```
#define BLE_VS_CS_PRIM_ADV_S_2
```

Coding scheme for Primary Advertising PHY(S=2).

```
#define BLE_VS_CS_SECOND_ADV_S_8
```

Coding scheme for Secondary Advertising PHY(S=8).

```
#define BLE_VS_CS_SECOND_ADV_S_2
```

Coding scheme for Secondary Advertising PHY(S=2).

```
#define BLE_VS_CS_CONN_S_8
```

Coding scheme for request for link establishment(S=8).

```
#define BLE_VS_CS_CONN_S_2
```

Coding scheme for request for link establishment(S=2).

```
#define BLE_VS_TX_FLOW_CTL_ON
```

It means that the number of buffer has reached the High Water Mark from flow off state.

```
#define BLE_VS_TX_FLOW_CTL_OFF
```

It means that the number of buffer has reached the Low Water Mark from flow on state.

## Typedefs

```
typedef void(* ble_vs_app_cb_t) (uint16_t event_type, ble_status_t event_result,  
st_ble_vs_evt_data_t *p_event_data)
```

ble\_vs\_app\_cb\_t is the Vendor Specific Event callback function type.  
[More...](#)

## Enumerations

```
enum e_r_ble_vs_evt_t
```

Vendor Specific Event Identifier. [More...](#)

## Data Structure Documentation

### ◆ st\_ble\_vs\_tx\_test\_param\_t

struct st_ble_vs_tx_test_param_t		
This is the extended transmitter test parameters used in <a href="#">R_BLE_VS_StartTxTest()</a> .		
Data Fields		
uint8_t	ch	Channel used in Tx test.
uint8_t	test_data_len	Length(in bytes) of the packet used in Tx Test.
uint8_t	packet_payload	Packet Payload.
uint8_t	phy	Transmitter PHY used in test.
uint8_t	tx_power	Tx Power Level used in DTM Tx Test.
uint8_t	option	Option.
uint16_t	num_of_packet	The number of packet to be sent.

### ◆ st\_ble\_vs\_rx\_test\_param\_t

struct st_ble_vs_rx_test_param_t		
This is the extended receiver test parameters used in <a href="#">R_BLE_VS_StartRxTest()</a> .		
Data Fields		
uint8_t	ch	Channel used in Rx test.
uint8_t	phy	Receiver PHY used in the test.

### ◆ st\_ble\_vs\_set\_rf\_ctrl\_param\_t

struct st_ble_vs_set_rf_ctrl_param_t		
This is the RF parameters used in <a href="#">R_BLE_VS_SetRfControl()</a> .		
Data Fields		
uint8_t	power	RF power on/off.
uint8_t	option	This field indicates whether the parameters change in RF power on.
uint8_t	clval	RF rapid clock frequency adjust value(OSC internal CL adjust).

uint8_t	slow_clock	RF slow clock configurations.
uint8_t	tx_power	Set tx power in power on.
uint8_t	rf_option	Set RF option.

#### ◆ st\_ble\_vs\_test\_end\_evt\_t

struct st_ble_vs_test_end_evt_t		
This structure notifies that the extended test has been terminated.		
Data Fields		
uint16_t	num_of_packet	The number of packet successfully received in the receiver test.
uint16_t	num_of_crc_err_packet	The number of CRC error packets in the receiver test.
int8_t	ave_rssi	Average RSSI(dBm) in the receiver test.
int8_t	max_rssi	Maximum RSSI(dBm) in the receiver test.
int8_t	min_rssi	Minimum RSSI(dBm) in the receiver test.

#### ◆ st\_ble\_vs\_set\_tx\_pwr\_comp\_evt\_t

struct st_ble_vs_set_tx_pwr_comp_evt_t		
This structure notifies that tx power has been set.		
Data Fields		
uint16_t	conn_hdl	Connection handle that identifying the link whose tx power has been set.
int8_t	curr_tx_pwr	Tx power that has been set(dBm).

#### ◆ st\_ble\_vs\_get\_tx\_pwr\_comp\_evt\_t

struct st_ble_vs_get_tx_pwr_comp_evt_t		
This structure notifies that tx power has been retrieved.		
Data Fields		
uint16_t	conn_hdl	Connection handle that identifying the link whose tx power has been retrieved.
int8_t	curr_tx_pwr	Current tx power(dBm).
int8_t	max_tx_pwr	Maximum tx power(dBm).

#### ◆ st\_ble\_vs\_set\_rf\_ctrl\_comp\_evt\_t

struct st_ble_vs_set_rf_ctrl_comp_evt_t		
This structure notifies that RF has been configured.		
Data Fields		
uint8_t	ctrl	The result of RF power control.

#### ◆ st\_ble\_vs\_get\_bd\_addr\_comp\_evt\_t

struct st_ble_vs_get_bd_addr_comp_evt_t						
This structure notifies that BD_ADDR has been retrieved.						
Data Fields						
uint8_t	area	The area that public/random address has been retrieved.				
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_VS_ADDR_AREA_REG(0x00)</td> <td>Register.</td> </tr> <tr> <td>BLE_VS_ADDR_AREA_DATA_FLASH(0x01)</td> <td>Data Flash.</td> </tr> </tbody> </table>	value	description	BLE_VS_ADDR_AREA_REG(0x00)	Register.
value	description					
BLE_VS_ADDR_AREA_REG(0x00)	Register.					
BLE_VS_ADDR_AREA_DATA_FLASH(0x01)	Data Flash.					
st_ble_dev_addr_t	addr	The address that has been retrieved.				

#### ◆ st\_ble\_vs\_get\_rand\_comp\_evt\_t

struct st_ble_vs_get_rand_comp_evt_t		
This structure notifies that random number has been generated.		
Data Fields		
uint8_t	rand_size	Length of random number.
uint8_t *	p_rand	Random number.

#### ◆ st\_ble\_vs\_tx\_flow\_chg\_evt\_t

struct st_ble_vs_tx_flow_chg_evt_t				
This structure notifies that the state transition of TxFlow has been changed.				
Data Fields				
uint8_t	state	The state of the flow control.		
		<table border="1"> <thead> <tr> <th>value</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_VS_TX_FLOW_CTL_ON(0x00)</td> <td>The number of buffer has reached the High Water Mark from flow off state.</td> </tr> </tbody> </table>	value	description
value	description			
BLE_VS_TX_FLOW_CTL_ON(0x00)	The number of buffer has reached the High Water Mark from flow off state.			

		<a href="#">BLE_VS_TX_FLOW_CTL_OFF(0x01)</a> The number of buffer has reached the Low Water Mark from flow on state.
uint32_t	buffer_num	The number of the current transmission buffers.

◆ **st\_ble\_vs\_evt\_data\_t**

struct st_ble_vs_evt_data_t		
st_ble_vs_evt_data_t is the type of the data notified in a Vendor Specific Event.		
Data Fields		
uint16_t	param_len	The size of Vendor Specific Event parameters.
void *	p_param	Vendor Specific Event parameters. This parameter differs in each Vendor Specific Event.

◆ **st\_ble\_vs\_get\_scan\_ch\_map\_comp\_evt\_t**

struct st_ble_vs_get_scan_ch_map_comp_evt_t		
This structure notifies that current scan channel map.		
Data Fields		
uint8_t	ch_map	The result of current scan channel map.

**Typedef Documentation**◆ **ble\_vs\_app\_cb\_t**

ble_vs_app_cb_t		
ble_vs_app_cb_t is the Vendor Specific Event callback function type.		
<b>Parameters</b>		
[in]	event_type	The type of Vendor Specific Event.
[in]	event_result	The result of API call which generates the Vendor Specific Event.
[in]	p_event_data	Data notified in the Vendor Specific Event.
<b>Returns</b>		
none		

## Enumeration Type Documentation

### ◆ e\_r\_ble\_vs\_evt\_t

enum e_r_ble_vs_evt_t							
Vendor Specific Event Identifier.							
Enumerator							
BLE_VS_EVENT_SET_TX_POWER	<p>This event notifies that the tx power has been set by <a href="#">R_BLE_VS_SetTxPower()</a>.</p> <p><b>Event Code: 0x8001</b></p> <p><b>result:</b></p> <table> <tr> <td>BLE_SUCCESS(0x000)</td> <td>Success</td> </tr> <tr> <td>BLE_ERR_INVALID_ARG(0x0003)</td> <td>The tx_power parameter specified by <a href="#">R_BLE_VS_SetTxPower()</a> is out of range.</td> </tr> <tr> <td>BLE_ERR_INVALID_HDL(0x000E)</td> <td>The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_SetTxPower()</a> is not found.</td> </tr> </table> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_set_tx_pwr_comp_evt_t</a></p>	BLE_SUCCESS(0x000)	Success	BLE_ERR_INVALID_ARG(0x0003)	The tx_power parameter specified by <a href="#">R_BLE_VS_SetTxPower()</a> is out of range.	BLE_ERR_INVALID_HDL(0x000E)	The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_SetTxPower()</a> is not found.
BLE_SUCCESS(0x000)	Success						
BLE_ERR_INVALID_ARG(0x0003)	The tx_power parameter specified by <a href="#">R_BLE_VS_SetTxPower()</a> is out of range.						
BLE_ERR_INVALID_HDL(0x000E)	The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_SetTxPower()</a> is not found.						
BLE_VS_EVENT_GET_TX_POWER	<p>This event notifies that the tx power has been retrieved by <a href="#">R_BLE_VS_GetTxPower()</a>.</p> <p><b>Event Code: 0x8002</b></p> <p><b>result:</b></p> <table> <tr> <td>BLE_SUCCESS(0x000)</td> <td>Success</td> </tr> <tr> <td>BLE_ERR_INVALID_HDL(0x000E)</td> <td>The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_GetTxPower()</a> is not found.</td> </tr> </table> <p><b>Event Data:</b></p>	BLE_SUCCESS(0x000)	Success	BLE_ERR_INVALID_HDL(0x000E)	The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_GetTxPower()</a> is not found.		
BLE_SUCCESS(0x000)	Success						
BLE_ERR_INVALID_HDL(0x000E)	The link identified with the conn_hdl specified by <a href="#">R_BLE_VS_GetTxPower()</a> is not found.						

	st_ble_vs_get_tx_pwr_comp_evt_t
BLE_VS_EVENT_TX_TEST_START	<p>This event notifies that the extended transmitter test has been started by <a href="#">R_BLE_VS_StartTxTest()</a>.</p> <p><b>Event Code: 0x8003</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The parameter specified by <a href="#">R_BLE_VS_StartTxTest()</a> is out of range.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_TX_TEST_TERM	<p>This event notifies that the number specified by <a href="#">R_BLE_VS_StartTxTest()</a> of packets has been sent.</p> <p><b>Event Code: 0x8004</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_RX_TEST_START	<p>This event notifies that the extended receiver test has been started by <a href="#">R_BLE_VS_StartRxTest()</a>.</p> <p><b>Event Code: 0x8005</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The parameter specified by <a href="#">R_BLE_VS_StartRxTest()</a> is out of range.</p>

	<p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_TEST_END	<p>This event notifies that the extended test has been terminated by <a href="#">R_BLE_VS_EndTest()</a>.</p> <p><b>Event Code: 0x8006</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_test_end_evt_t</a></p>
BLE_VS_EVENT_SET_CODING_SCHEME_COMP	<p>This event notifies that the coding scheme has been configured by <a href="#">R_BLE_VS_SetCodingScheme()</a>.</p> <p><b>Event Code: 0x8007</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The coding_scheme parameter specified by <a href="#">R_BLE_VS_SetCodingScheme()</a> is out of range.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_RF_CONTROL_COMP	<p>This event notifies that the RF has been configured by <a href="#">R_BLE_VS_SetRfControl()</a>.</p> <p><b>Event Code: 0x8008</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The parameter specified by <a href="#">R_BLE_VS_SetRfControl()</a> is out of</p>

	<p>range.</p> <p>BLE_ERR_INVALID_OPERATION(0x0009)</p> <p>During the power on or the power off, the same power state is specified by <a href="#">R_BLE_VS_SetRfControl()</a>.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_set_rf_ctrl_comp_evt_t</a></p>
BLE_VS_EVENT_SET_ADDR_COMP	<p>This event notifies that public/random address has been set by <a href="#">R_BLE_VS_SetBdAddr()</a>.</p> <p><b>Event Code: 0x8009</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The area parameter or the type field in the p_addr parameter specified by <a href="#">R_BLE_VS_SetBdAddr()</a> is out of range.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_GET_ADDR_COMP	<p>This event notifies that public/random address has been retrieved by <a href="#">R_BLE_VS_GetBdAddr()</a>.</p> <p><b>Event Code: 0x800A</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x0000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The area parameter or the type field in the p_addr parameter specified by <a href="#">R_BLE_VS_GetBdAddr()</a> is out of range.</p>

	<p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_get_bd_addr_comp_evt_t</a></p>
BLE_VS_EVENT_GET_RAND	<p>This event notifies the application layer that random number has been generated by <a href="#">R_BLE_VS_GetRand()</a>.</p> <p><b>Event Code: 0x800B</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The rand_size parameter specified by <a href="#">R_BLE_VS_GetRand()</a> is out of range.</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_get_rand_comp_evt_t</a></p>
BLE_VS_EVENT_TX_FLOW_STATE_CHG	<p>This event notifies the application layer of the state transition of TxFlow.</p> <p><b>Event Code: 0x800C</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_tx_flow_chg_evt_t</a></p>
BLE_VS_EVENT_FAIL_DETECT	<p>This event notifies a failure occurs in RF. After receiving the event, reset MCU or RF.</p> <p><b>Event Code: 0x800D</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>None</p>
BLE_VS_EVENT_SET_SCAN_CH_MAP	<p>This event notifies that scan channel map has</p>

	<p>been set by <a href="#">R_BLE_VS_SetScanChMap()</a>.</p> <p><b>Event Code: 0x800E</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p>BLE_ERR_INVALID_ARG(0x0003) The ch_map parameter specified by <a href="#">R_BLE_VS_SetScanChMap()</a> is out of range.</p> <p><b>Event Data:</b></p> <p>none</p>
BLE_VS_EVENT_GET_SCAN_CH_MAP	<p>This event notifies that scan channel map has been retrieved by <a href="#">R_BLE_VS_GetScanChMap()</a>.</p> <p><b>Event Code: 0x800F</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p><a href="#">st_ble_vs_get_scan_ch_map_comp_evt_t</a></p>
BLE_VS_EVENT_INVALID	<p>Invalid VS Event.</p> <p><b>Event Code: 0x80FF</b></p> <p><b>result:</b></p> <p>BLE_SUCCESS(0x000) Success</p> <p><b>Event Data:</b></p> <p>none</p>

## Function Documentation

**◆ R\_BLE\_VS\_Init()**

```
ble_status_t R_BLE_VS_Init ( ble_vs_app_cb_t vs_cb)
```

This function initializes Vendor Specific API and registers a callback function for Vendor Specific Event.

The result of this API call is returned by a return value.

**Parameters**

[in]	vs_cb	Callback function to be registered.
------	-------	-------------------------------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The vs_cb parameter is specified as NULL.
BLE_ERR_CONTEXT_FULL(0x000B)	Callback function has already been registered.

## ◆ R\_BLE\_VS\_StartTxTest()

```
ble_status_t R_BLE_VS_StartTxTest ( st_ble_vs_tx_test_param_t * p_tx_test_param)
```

This function starts extended Transmitter Test.

The following extended transmitter test functions of DTM Tx are supported by this function.

- Tx Power
- Tx Modulation Enable/Modulation Disable
- Tx packet transmission/continuous transmission
- Tx packets count

The result of this API call is notified in BLE\_VS\_EVENT\_TX\_TEST\_START event.

If the num\_of\_packet field in the p\_tx\_test\_param parameter is other than 0x0000, BLE\_VS\_EVENT\_TX\_TEST\_TERM event notifies the application layer that the number of packet has been sent.

If R\_BLE\_VS\_EndTest() is called before the specified number of packets completions, BLE\_VS\_EVENT\_TX\_TEST\_TERM event is not notified to the application layer.

The condition that phy field in the p\_tx\_test\_param parameter is BLE\_VS\_EH\_TEST\_PHY\_CODED\_S\_8(0x03) and option field is modulation(bit0:0) & continuous transmission(bit1:1) is not supported.

### Parameters

[in]	p_tx_test_param	Tx Test parameters.
------	-----------------	---------------------

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_tx_test_param parameter is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_StartRxTest()**

```
ble_status_t R_BLE_VS_StartRxTest ( st_ble_vs_rx_test_param_t* p_rx_test_param)
```

This function starts extended Receiver Test.

The result of this API call is notified in BLE\_VS\_EVENT\_RX\_TEST\_START event. The following extended receiver test functions of DTM Rx are supported by this function.

- Calculating the maximum, the minimum and the average of RSSI in the receiver test.
- The number of CRC error packets in the receiver test.

The transmitter is configured to one of the following, the receiver can't receive the packets by this function.

- Tx Non-Modulation Enable
- Tx continuous transmission

After [R\\_BLE\\_VS\\_EndTest\(\)](#) has been called, the receiver test result value are notified in BLE\_VS\_EVENT\_TEST\_END event.

**Parameters**

[in]	p_rx_test_param	The extended receiver test parameters.
------	-----------------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_rx_test_param parameter is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_EndTest()**

```
ble_status_t R_BLE_VS_EndTest ( void )
```

This function terminates the extended transmitter or receiver test.

The result of this API call is notified in BLE\_VS\_EVENT\_TEST\_END event. In case of extended receiver test, this event notifies the application layer of the result of the extended receiver test.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

## ◆ R\_BLE\_VS\_SetTxPower()

```
ble_status_t R_BLE_VS_SetTxPower ( uint16_t conn_hdl, uint8_t tx_power )
```

This function configures transmit power.

This function configures the following transmit power.

- The transmit power used in sending advertising PDU, scan request PDU, connection request PDU (in not connected state)
- The transmit power used in sending PDU in connected state. When configuring the transmit power used in not connected state, set the conn\_hdl parameter to

[BLE\\_GAP\\_INIT\\_CONN\\_HDL\(0xFFFF\)](#).

When the transmit power used in connected state is configured, set the conn\_hdl parameter to the connection handle of the link.

Select one of the following transmit power levels.

- High
- Middle
- Low

Max transmit power of "High" is dependent on the configuration of the firmware. The result of this API call is notified in BLE\_VS\_EVENT\_SET\_TX\_POWER event.

### Parameters

[in]	conn_hdl	Connection handle identifying the link whose transmit power to be configured. If non connected state, set <a href="#">BLE_GAP_INIT_CONN_HDL(0xFFFF)</a> .
[in]	tx_power	Transmission power. Select one of the following. <ul style="list-style-type: none"> <li>• BLE_VS_TX_POWER_HIGH(0x00)</li> <li>• BLE_VS_TX_POWER_MID(0x01)</li> <li>• BLE_VS_TX_POWER_LOW(0x02)</li> </ul>

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

### ◆ R\_BLE\_VS\_GetTxPower()

ble\_status\_t R\_BLE\_VS\_GetTxPower ( uint16\_t conn\_hdl)

This function gets transmit power.

This function gets the following transmit power.

- The transmit power used in sending advertising PDU, scan request PDU, connection request PDU (in not connected state)
- The transmit power used in sending PDU in connected state. When getting the transmit power used in not connected state, set the conn\_hdl parameter to

[BLE\\_GAP\\_INIT\\_CONN\\_HDL\(0xFFFF\)](#).

When the transmit power used in connected state is retrieved, set the conn\_hdl parameter to the connection handle of the link. The result of this API call is notified in BLE\_VS\_EVENT\_GET\_TX\_POWER event.

#### Parameters

[in]	conn_hdl	Connection handle identifying the link whose transmit power to be retrieved. If non connected state, set <a href="#">BLE_GAP_INIT_CONN_HDL(0xFFFF)</a> .
------	----------	--

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

### ◆ R\_BLE\_VS\_SetCodingScheme()

ble\_status\_t R\_BLE\_VS\_SetCodingScheme ( uint8\_t coding\_scheme)

This function configure default Coding scheme(S=8 or S=2) that is used in the case of selecting Coded PHY in Primary advertising PHY or Secondary advertising PHY advertising or request for link establishment.

After setting the default Coding scheme by this function, configure the advertising parameters by [R\\_BLE\\_GAP\\_SetAdvParam\(\)](#) or send a request for link establishment.

The result of this API call is notified in BLE\_VS\_EVENT\_SET\_CODING\_SCHEME\_COMP event.

#### Parameters

[in]	coding_scheme	Coding scheme for Primary advertising PHY, Secondary advertising PHY, request for link establishment. The coding_scheme field is set to a bitwise OR of the following values.	
		bit	description
		bit0	Coding scheme for Primary Advertising PHY(0:S=8/1:S=2).
		bit1	Coding scheme for Secondary Advertising PHY(0:S=8/1:S=2).
		bit2	Coding scheme for request for link establishment(0:S=8/1:S=2).
		All other bits	Reserved for future use.

#### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_SetRfControl()**

```
ble_status_t R_BLE_VS_SetRfControl ( st_ble_vs_set_rf_ctrl_param_t * p_rf_ctrl)
```

This function performs power control on RF.

If BLE communication is not used for a long time, RF reduces the power consumption by moving to the RF Power-Down Mode.

When RF power on, RF initialization processing is executed.

After RF power off by this function, API functions other than this are not available until RF power on again.

The result of this API call is notified in BLE\_VS\_EVENT\_RF\_CONTROL\_COMP event. After RF power on again with this function, call [R\\_BLE\\_GAP\\_Terminate\(\)](#), [R\\_BLE\\_GAP\\_Init\(\)](#) in order to restart the host stack.

**Parameters**

[in]	p_rf_ctrl	RF parameters.
------	-----------	----------------

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_rf_ctrl parameter is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_SetBdAddr()**

```
ble_status_t R_BLE_VS_SetBdAddr ( uint8_t area, st_ble_dev_addr_t* p_addr )
```

This function sets public/random address of local device to the area specified by the parameter.

If the address is written in non-volatile area, the address is used as default address on the next MCU reset.

For more information on the random address, refer to Core Specification Vol 6, PartB, "1.3.2 Random Device Address".

The result of this API call is notified in BLE\_VS\_EVENT\_SET\_ADDR\_COMP event.

**Parameters**

[in]	area	The area that the address is to be written in. Select one of the following.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td>BLE_VS_ADDR_AREA_REG (0x00)</td> <td>Address writing to non-volatile area is not performed. Only the address in register is written.</td> </tr> <tr> <td>BLE_VS_ADDR_AREA_DAT_FLASH(0x01)</td> <td>Address writing to DataFlash area is performed.</td> </tr> </tbody> </table>	macro	description	BLE_VS_ADDR_AREA_REG (0x00)	Address writing to non-volatile area is not performed. Only the address in register is written.	BLE_VS_ADDR_AREA_DAT_FLASH(0x01)	Address writing to DataFlash area is performed.
macro	description							
BLE_VS_ADDR_AREA_REG (0x00)	Address writing to non-volatile area is not performed. Only the address in register is written.							
BLE_VS_ADDR_AREA_DAT_FLASH(0x01)	Address writing to DataFlash area is performed.							
[in]	p_addr	The address to be set to the area. Set BLE_GAP_ADDR_PUBLIC(0x00) or BLE_GAP_ADDR_RANDOM(0x01) to the type field in the p_addr parameter.						

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_addr parameter is specified as NULL.
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_GetBdAddr()**

```
ble_status_t R_BLE_VS_GetBdAddr ( uint8_t area, uint8_t addr_type )
```

This function gets currently configured public/random address.

The area parameter specifies the place where this function retrieves public/random address. The result of this API call is notified in BLE\_VS\_EVENT\_GET\_ADDR\_COMP event.

**Parameters**

[in]	area	The area that the address is to be retrieved. Select one of the following.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_VS_ADD_R_AREA_REG(0x00)</a></td> <td>Retrieve the address in register.</td> </tr> <tr> <td><a href="#">BLE_VS_ADD_R_AREA_DATA_FLASH(0x01)</a></td> <td>Retrieve the address in DataFlash area.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_VS_ADD_R_AREA_REG(0x00)</a>	Retrieve the address in register.	<a href="#">BLE_VS_ADD_R_AREA_DATA_FLASH(0x01)</a>	Retrieve the address in DataFlash area.
macro	description							
<a href="#">BLE_VS_ADD_R_AREA_REG(0x00)</a>	Retrieve the address in register.							
<a href="#">BLE_VS_ADD_R_AREA_DATA_FLASH(0x01)</a>	Retrieve the address in DataFlash area.							
[in]	addr_type	The address type that is type of the address to be retrieved.						
		<table border="1"> <thead> <tr> <th>macro</th> <th>description</th> </tr> </thead> <tbody> <tr> <td><a href="#">BLE_GAP_ADDR_PUBLIC(0x00)</a></td> <td>Public address.</td> </tr> <tr> <td><a href="#">BLE_GAP_ADDR_RANDOM(0x01)</a></td> <td>Random address.</td> </tr> </tbody> </table>	macro	description	<a href="#">BLE_GAP_ADDR_PUBLIC(0x00)</a>	Public address.	<a href="#">BLE_GAP_ADDR_RANDOM(0x01)</a>	Random address.
macro	description							
<a href="#">BLE_GAP_ADDR_PUBLIC(0x00)</a>	Public address.							
<a href="#">BLE_GAP_ADDR_RANDOM(0x01)</a>	Random address.							

**Return values**

<a href="#">BLE_SUCCESS(0x0000)</a>	Success
<a href="#">BLE_ERR_INVALID_STATE(0x0008)</a>	The task for host stack is not running.
<a href="#">BLE_ERR_MEM_ALLOC_FAILED(0x000C)</a>	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_GetRand()**

```
ble_status_t R_BLE_VS_GetRand ( uint8_t rand_size)
```

This function generates 4-16 bytes of random number used in creating keys.

The result of this API call is notified in BLE\_VS\_EVENT\_GET\_RAND event.

**Parameters**

[in]	rand_size	Length of the random number (byte). The valid range is 4<=rand_size<=16.
------	-----------	---

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_STATE(0x0008)	The task for host stack is not running.
BLE_ERR_MEM_ALLOC_FAILED(0x000C)	There are no memories for Vendor Specific Command.

◆ **R\_BLE\_VS\_StartTxFlowEvtNtf()**

```
ble_status_t R_BLE_VS_StartTxFlowEvtNtf ( void )
```

This function starts the notification(BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event) of the state transition of TxFlow.

If the number of the available transmission packet buffers is the following, BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event notifies the application layer of the state of the TxFlow.

- The number of the available transmission packet buffers is less than Low Water Mark.
- The number of the available transmission packet buffers is more than High Water Mark. The result of this API call is returned by a return value.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

◆ **R\_BLE\_VS\_StopTxFlowEvtNtf()**

```
ble_status_t R_BLE_VS_StopTxFlowEvtNtf ( void )
```

This function stops the notification(BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event) of the state transition of TxFlow.

The result of this API call is returned by a return value.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

◆ **R\_BLE\_VS\_GetTxBufferNum()**

```
ble_status_t R_BLE_VS_GetTxBufferNum ( uint32_t * p_buffer_num)
```

This function retrieves the number of the available transmission packet buffers.

The maximum number of the available buffers is 10.

The result of this API call is returned by a return value.

**Parameters**

[out]	p_buffer_num	The number of the available transmission packet buffers.
-------	--------------	--

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_PTR(0x0001)	The p_buffer_num parameter is specified as NULL.

◆ **R\_BLE\_VS\_SetTxLimit()**

```
ble_status_t R_BLE_VS_SetTxLimit ( uint32_t tx_queue_lwm, uint32_t tx_queue_hwm )
```

This function sets the threshold for notifying the application layer of the TxFlow state.

Call this function before the notification(BLE\_VS\_EVENT\_TX\_FLOW\_STATE\_CHG event) has been started by [R\\_BLE\\_VS\\_StartTxFlowEvtNtf\(\)](#).

The result is returned from this API.

Vendor Specific API supports the flow control function(TxFlow) for the transmission on L2CAP fixed channel in Basic Mode such as GATT.

Host stack has 10 transmission packet buffers for the transmission.

When the number of the available transmission packet buffers has been less than Low Water Mark, the state of TxFlow transmits into the TxFlow OFF state from the TxFlow ON state that is the initial state and host stack notifies the application layer of timing to stop packet transmission.

When host stack has sent the transmission packets to Controller and the number of the available transmission packet buffers has been more than High Water Mark, the state of TxFlow transmits into the TxFlow ON state from the TxFlow OFF state and host stack notifies the application layer of

timing to restart packet transmission.

It is possible to perform flow control on a fixed channel by using the event notification.

### Parameters

[in]	tx_queue_lwm	Low Water Mark. Set 0-9 less than tx_queue_hwm to the parameter. When the number of the available transmission packet buffers has been less than the value specified by the tx_queue_lwm parameter, host stack notifies the application layer of the timing to stop packet transmission.
[in]	tx_queue_hwm	High Water Mark. Set 1-10 more than tx_queue_lwm to the parameter. When the number of the available transmission packet buffers has been more than the value specified by the tx_queue_hwm parameter, host stack notifies the application layer of the timing to restart packet transmission.

### Return values

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The tx_queue_lwm parameter or the tx_queue_hwm parameter is out of range.

◆ **R\_BLE\_VS\_SetScanChMap()**

```
ble_status_t R_BLE_VS_SetScanChMap ( uint16_t ch_map)
```

This function sets the scan channel map.

Set specify the scan channel for use.  
At least one channel must be enabled.

**Note**

*Calling this API while Scan is already running will not change the channel map.*

**Parameters**

[in]	ch_map	Specify the channel map for use.	
		bit	description
		bit0	Enable channel 37 for use (0:disable, 1:enable)
		bit1	Enable channel 38 for use (0:disable, 1:enable)
		bit2	Enable channel 39 for use (0:disable, 1:enable)
		All other bits	Reserved for future use.

**Return values**

BLE_SUCCESS(0x0000)	Success
BLE_ERR_INVALID_ARG(0x0003)	The ch_map parameter is out of range.

**◆ R\_BLE\_VS\_GetScanChMap()**

```
ble_status_t R_BLE_VS_GetScanChMap ( void )
```

This function gets currently scan channel map.

The result of this API call is notified in BLE\_VS\_EVENT\_GET\_SCAN\_CH\_MAP event.

**Return values**

BLE_SUCCESS(0x0000)	Success
---------------------	---------

**4.2.6 Clock Frequency Accuracy Measurement Circuit (r\_cac)**

## Modules

**Functions**

```
fsp_err_t R_CAC_Open (cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CAC_StartMeasurement (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_StopMeasurement (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_Read (cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
```

```
fsp_err_t R_CAC_Close (cac_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CAC_CallbackSet (cac_ctrl_t *const p_ctrl,
void(*p_callback)(cac_callback_args_t *), void const *const
p_context, cac_callback_args_t *const p_callback_memory)
```

**Detailed Description**

Driver for the CAC peripheral on RA MCUs. This module implements the [CAC Interface](#).

**Overview**

The interface for the clock frequency accuracy measurement circuit (CAC) peripheral is used to check a system clock frequency with a reference clock signal by counting the number of measurement clock edges that occur between two edges of the reference clock.

**Features**

- Supports clock frequency-measurement and monitoring based on a reference signal input
- Reference can be either an externally supplied clock source or an internal clock source
- An interrupt request may optionally be generated by a completed measurement, a detected

frequency error, or a counter overflow.

- A digital filter is available for an externally supplied reference clock, and dividers are available for both internally supplied measurement and reference clocks.
- Edge-detection options for the reference clock are configurable as rising, falling, or both.

## Configuration

### Build Time Configurations for r\_cac

The following build time configurations are defined in fsp\_cfg/r\_cac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Clock Accuracy Circuit Driver on r\_cac

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Clock Accuracy Circuit Driver on r\_cac. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_cac0	Module name.
Reference clock divider	<ul style="list-style-type: none"> <li>• 32</li> <li>• 128</li> <li>• 1024</li> <li>• 8192</li> </ul>	32	Reference clock divider.
Reference clock source	<ul style="list-style-type: none"> <li>• Main Oscillator</li> <li>• Sub-clock</li> <li>• HOCO</li> <li>• MOCO</li> <li>• LOCO</li> <li>• PCLKB</li> <li>• IWDT</li> <li>• External</li> </ul>	Main Oscillator	Reference clock source.
Reference clock digital filter	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Sampling clock =Measuring freq</li> <li>• Sampling clock =Measuring freq/4</li> <li>• Sampling clock =Measuring freq/16</li> </ul>	Disabled	Reference clock digital filter.
Reference clock edge	<ul style="list-style-type: none"> <li>• Rising</li> </ul>	Rising	Reference clock edge

detect	<ul style="list-style-type: none"> <li>Falling</li> <li>Both</li> </ul>		detection.
Measurement clock divider	<ul style="list-style-type: none"> <li>1</li> <li>4</li> <li>8</li> <li>32</li> </ul>	1	Measurement clock divider.
Measurement clock source	<ul style="list-style-type: none"> <li>Main Oscillator</li> <li>Sub-clock</li> <li>HOCO</li> <li>MOCO</li> <li>LOCO</li> <li>PCLKB</li> <li>IWDT</li> </ul>	HOCO	Measurement clock source.
Upper Limit Threshold	Value must be a non-negative integer, between 0 to 65535	0	Top end of allowable range for measurement completion.
Lower Limit Threshold	Value must be a non-negative integer, between 0 to 65535	0	Bottom end of allowable range for measurement completion.
Frequency Error Interrupt Priority	MCU Specific Options		CAC frequency error interrupt priority.
Measurement End Interrupt Priority	MCU Specific Options		CAC measurement end interrupt priority.
Overflow Interrupt Priority	MCU Specific Options		CAC overflow interrupt priority.
Callback	Name must be a valid C symbol	NULL	Function name for callback

## Clock Configuration

The CAC measurement clock source can be configured as the following:

1. MAIN\_OSC
2. SUBCLOCK
3. HOCO
4. MOCO
5. LOCO
6. PCLKB
7. IWDT

The CAC reference clock source can be configured as the following:

1. MAIN\_OSC
2. SUBCLOCK
3. HOCO
4. MOCO
5. LOCO
6. PCLKB
7. IWDT

## 8. External Clock Source (CACREF)

### Pin Configuration

The CACREF pin can be configured to provide the reference clock for CAC measurements.

## Usage Notes

### Measurement Accuracy

The clock measurement result may be off by up to one pulse depending on the phase difference between the edge detection circuit, digital filter, and CACREF pin signal, if applicable.

### Frequency Error Interrupt

The frequency error interrupt is only triggered at the end of a CAC measurement. This means that there will be a measurement complete interrupt in addition to the frequency error interrupt.

## Examples

### Basic Example

This is a basic example of minimal use of the CAC in an application.

```
volatile uint32_t g_callback_complete;
void cac_basic_example ()
{
    g_callback_complete = 0;
    fsp_err_t err = R_CAC_Open(&g_cac_ctrl, &g_cac_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    (void) R_CAC_StartMeasurement(&g_cac_ctrl);
    /* Wait for measurement to complete. */
    while (0 == g_callback_complete)
    {
    }
    uint16_t value;
    /* Read the CAC measurement. */
    (void) R_CAC_Read(&g_cac_ctrl, &value);
}
/* Called when measurement is completed. */
static void r_cac_callback (cac_callback_args_t * p_args)
{
```

```

if (CAC_EVENT_MEASUREMENT_COMPLETE == p_args->event)
{
    g_callback_complete = 1U;
}
}

```

## Data Structures

struct `cac_instance_ctrl_t`

## Data Structure Documentation

### ◆ `cac_instance_ctrl_t`

struct `cac_instance_ctrl_t`

CAC instance control block. DO NOT INITIALIZE.

## Function Documentation

### ◆ `R_CAC_Open()`

`fsp_err_t R_CAC_Open ( cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg )`

The Open function configures the CAC based on the provided user configuration settings.

#### Return values

FSP_SUCCESS	CAC is available and available for measurement(s).
FSP_ERR_ASSERTION	An argument is invalid.
FSP_ERR_ALREADY_OPEN	The CAC has already been opened.

#### Note

*There is only a single CAC peripheral.*

◆ **R\_CAC\_StartMeasurement()**

```
fsp_err_t R_CAC_StartMeasurement ( cac_ctrl_t *const p_ctrl)
```

Start the CAC measurement process.

**Return values**

FSP_SUCCESS	CAC measurement started.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_StopMeasurement()**

```
fsp_err_t R_CAC_StopMeasurement ( cac_ctrl_t *const p_ctrl)
```

Stop the CAC measurement process.

**Return values**

FSP_SUCCESS	CAC measuring has been stopped.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_Read()**

```
fsp_err_t R_CAC_Read ( cac_ctrl_t *const p_ctrl, uint16_t *const p_counter )
```

Read and return the CAC status and counter registers.

**Return values**

FSP_SUCCESS	CAC read successful.
FSP_ERR_ASSERTION	An argument is NULL.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_Close()**

```
fsp_err_t R_CAC_Close ( cac_ctrl_t *const p_ctrl)
```

Release any resources that were allocated by the Open() or any subsequent CAC operations.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	NULL provided for p_instance_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	R_CAC_Open() has not been successfully called.

◆ **R\_CAC\_CallbackSet()**

```
fsp_err_t R_CAC_CallbackSet ( cac_ctrl_t *const p_ctrl, void (*)(cac_callback_args_t *) p_callback,
void const *const p_context, cac_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `cac_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

**4.2.7 Controller Area Network (r\_can)**

## Modules

**Functions**

```
fsp_err_t R_CAN_Open (can_ctrl_t *const p_api_ctrl, can_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_CAN_Close (can_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_CAN_Write (can_ctrl_t *const p_api_ctrl, uint32_t const mailbox,
can_frame_t *const p_frame)
```

```
fsp_err_t R_CAN_Read (can_ctrl_t *const p_api_ctrl, uint32_t mailbox,
                    can_frame_t *const p_frame)
```

```
fsp_err_t R_CAN_ModeTransition (can_ctrl_t *const p_api_ctrl,
                               can_operation_mode_t operation_mode, can_test_mode_t test_mode)
```

```
fsp_err_t R_CAN_InfoGet (can_ctrl_t *const p_api_ctrl, can_info_t *const p_info)
```

```
fsp_err_t R_CAN_CallbackSet (can_ctrl_t *const p_api_ctrl,
                             void(*p_callback)(can_callback_args_t *), void const *const
                             p_context, can_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the CAN peripheral on RA MCUs. This module implements the [CAN Interface](#).

## Overview

The Controller Area network (CAN) HAL module provides a high-level API for CAN applications and supports the CAN peripherals available on RA microcontroller hardware. A user-callback function must be defined that the driver will invoke when transmit, receive or error interrupts are received. The callback is passed a parameter which indicates the channel, mailbox and event as well as the received data (if available).

## Features

- Supports both standard (11-bit) and extended (29-bit) messaging formats
- Supports speeds upto 1 Mbps
- Support for bit timing configuration as defined in the CAN specification
- Supports up to 32 transmit or receive mailboxes with standard or extended ID frames
- Optional support for a 4-stage transmit and receive FIFO
- Receive mailboxes can be configured to capture either data or remote CAN Frames
- Receive mailboxes can be configured to receive a range of IDs using mailbox masks
- Mailboxes can be configured with Overwrite or Overrun mode
- Supports a user-callback function when transmit, receive, or error interrupts are received

## Configuration

### Build Time Configurations for r\_can

The following build time configurations are defined in fsp\_cfg/r\_can\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
FIFO Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	When FIFOs are enabled, a transmit FIFO replaces

mailboxes 24-27 and a receive FIFO replaces mailboxes 28-31.

### Configurations for Driver > Connectivity > CAN Driver on r\_can

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > CAN Driver on r\_can. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_can0	Module name.
General > Channel	Channel should be 0 or 1	0	Specify the CAN channel to use.
General > Clock Source	MCU Specific Options		Select the CAN clock source.
General > Overwrite/Overrrun Mode	<ul style="list-style-type: none"> <li>• Overwrite Mode</li> <li>• Overrrun Mode</li> </ul>	Overwrite Mode	Select whether receive mailbox will be overwritten or overrun if data is not read in time.
General > Global ID Mode	<ul style="list-style-type: none"> <li>• Standard ID Mode</li> <li>• Extended ID Mode</li> <li>• Mixed ID Mode</li> </ul>	Standard ID Mode	Select whether the driver will use CAN Standard IDs, Extended IDs or a mix of both.
General > Number of Mailboxes	<ul style="list-style-type: none"> <li>• 4 Mailboxes</li> <li>• 8 Mailboxes</li> <li>• 16 Mailboxes</li> <li>• 24 Mailboxes</li> <li>• 32 Mailboxes</li> </ul>	32 Mailboxes	Select 4, 8, 16, 24 or 32 mailboxes. In FIFO mailbox mode up to 24 mailboxes are available.
Baud Rate Settings > Auto-generated Settings > Sample-Point (%)	Must be a valid integer between 0 and 100. Ignore when Override Baud Settings is Enabled.	75	Sample-Point = $(TSEG1 + 1) / (TSEG1 + TSEG2 + 1)$ .
Baud Rate Settings > Auto-generated Settings > CAN Baud Rate (Hz)	Must be a valid integer configurable upto maximum 1MHz. Ignore when Override Baud Settings is Enabled.	500000	Specify baud rate in Hz.  If the requested baud rate cannot be achieved, the settings with the largest possible baud rate that is less than or equal to the requested baud rate is used. If multiple combinations would result in the best baud

rate, the combination with the least absolute error for the ratio is chosen. The theoretical calculated baud rate and ratio are printed in a comment in the generated `can_bit_timing_cfg_t` structure.

Override calculated baudrate parameters and instead use the ones specified below. This option ignores the parameters specified under Sample-Point (%) and CAN Baud Rate (Hz)

Specify division value of baud rate prescaler (baud rate prescalar + 1).

Select the time segment 1 value. (4-16). Check module usage notes for how to calculate this value.

Select the time segment 2 value (2-8). Check module usage notes for how to calculate this value.

Select the Synchronization Jump Width value (1-4). Check module usage notes for how to calculate this value.

A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time any interrupt occurs.

Transmit/Receive/Error interrupt priority.

Baud Rate Settings > Override Auto-generated Settings > Override Baud Settings

- Enabled
- Disabled

Disabled

Baud Rate Settings > Override Auto-generated Settings > Baud Rate Prescaler

Value must be a non-negative integer between 1 and 1024.

1

Baud Rate Settings > Override Auto-generated Settings > Time Segment 1

Refer to the RA Configuration tool for available options.

4 Time Quanta

Baud Rate Settings > Override Auto-generated Settings > Time Segment 2

- 2 Time Quanta
- 3 Time Quanta
- 4 Time Quanta
- 5 Time Quanta
- 6 Time Quanta
- 7 Time Quanta
- 8 Time Quanta

2 Time Quanta

Baud Rate Settings > Override Auto-generated Settings > Synchronization Jump Width

- 1 Time Quanta
- 2 Time Quanta
- 3 Time Quanta
- 4 Time Quanta

1 Time Quanta

Interrupts > Callback

Name must be a valid C symbol

`can_callback`

Interrupts > Interrupt Priority Level

MCU Specific Options

Interrupts > Transmit FIFO Interrupt Mode	<ul style="list-style-type: none"> <li>• Every Message</li> <li>• Empty</li> </ul>	Every Message	Select whether the receive FIFO should throw an interrupt on every received message or when it becomes empty.
Input > Receive FIFO > Receive ID 1 > ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0	Select the first ID for the receive FIFO, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs.
Input > Receive FIFO > Receive ID 1 > ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the receive FIFO is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Receive FIFO > Receive ID 1 > Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Remote Mailbox	Select whether the receive FIFO is used to capture data frames or remote frames.
Input > Receive FIFO > Receive ID 1 > Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for the receive FIFO. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Receive FIFO > Receive ID 2 > ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0	Select the second ID for the receive FIFO, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs.
Input > Receive FIFO > Receive ID 2 > ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the receive FIFO is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Receive FIFO > Receive ID 2 > Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Remote Mailbox	Select whether the receive FIFO is used to capture data frames or remote frames.

Input > Receive FIFO > Receive ID 2 > Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for the receive FIFO. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 0 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0	Select the receive ID for mailbox 0, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 1 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	1	Select the receive ID for mailbox 1, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 2 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	2	Select the receive ID for mailbox 2, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID > Mailbox 3 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	3	Select the receive ID for mailbox 3, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 0-3 Group > Mailbox ID Mode > Mailbox 0 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 0-3	<ul style="list-style-type: none"> <li>Standard ID</li> </ul>	Standard ID	Select whether the

Group > Mailbox ID Mode > Mailbox 1 ID Mode	<ul style="list-style-type: none"> <li>Extended ID</li> </ul>		mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 0-3 Group > Mailbox ID Mode > Mailbox 2 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 0-3 Group > Mailbox ID Mode > Mailbox 3 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 0 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Transmit Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 1 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 2 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Type > Mailbox 3 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 0 Frame Type	<ul style="list-style-type: none"> <li>Data Mailbox</li> <li>Remote Mailbox</li> </ul>	Remote Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 1 Frame Type	<ul style="list-style-type: none"> <li>Data Mailbox</li> <li>Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit

Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 2 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	mailboxes). Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox Frame Type > Mailbox 3 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 0-3 Group > Mailbox 0-3 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 0-3. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 4 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	4	Select the receive ID for mailbox 4, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 5 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	5	Select the receive ID for mailbox 5, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 6 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	6	Select the receive ID for mailbox 6, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID > Mailbox 7 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	7	Select the receive ID for mailbox 7, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF

Input > Mailbox 4-7 Group > Mailbox ID Mode > Mailbox 4 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 4-7 Group > Mailbox ID Mode > Mailbox 5 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 4-7 Group > Mailbox ID Mode > Mailbox 6 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 4-7 Group > Mailbox ID Mode > Mailbox 7 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 4 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 5 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type > Mailbox 6 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for

> Mailbox 7 Type	<ul style="list-style-type: none"> <li>• Transmit Mailbox</li> </ul>		receive or transmit.
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 4 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 5 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 6 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox Frame Type > Mailbox 7 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 4-7 Group > Mailbox 4-7 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	>Select the Mask for mailboxes 4-7. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 8 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	8	Select the receive ID for mailbox 8, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 9 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	9	Select the receive ID for mailbox 9, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 10 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	10	Select the receive ID for mailbox 10, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID > Mailbox 11 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	11	Select the receive ID for mailbox 11, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 8-11 Group > Mailbox ID Mode > Mailbox 8 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 8-11 Group > Mailbox ID Mode > Mailbox 9 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 8-11 Group > Mailbox ID Mode > Mailbox 10 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 8-11 Group > Mailbox ID Mode > Mailbox 11 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.

Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 8 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 9 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 10 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Type > Mailbox 11 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 8 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 9 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 10 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox Frame Type > Mailbox 11 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 8-11 Group > Mailbox 8-11 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 8-11. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 12 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	12	Select the receive ID for mailbox 12, between 0 and 0x7ff

when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 13, between 0 and 0x7fff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 14, between 0 and 0x7fff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 15, between 0 and 0x7fff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.

Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed

Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 13 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      13

Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 14 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      14

Input > Mailbox 12-15 Group > Mailbox ID > Mailbox 15 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      15

Input > Mailbox 12-15 Group > Mailbox ID Mode > Mailbox 12 ID Mode      • Standard ID      Standard ID  
• Extended ID

Input > Mailbox 12-15 Group > Mailbox ID Mode > Mailbox 13 ID Mode      • Standard ID      Standard ID  
• Extended ID

Input > Mailbox 12-15 Group > Mailbox ID Mode > Mailbox 14 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	ID Mode'. Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 12-15 Group > Mailbox ID Mode > Mailbox 15 ID Mode	<ul style="list-style-type: none"> <li>Standard ID</li> <li>Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 12 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 13 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 14 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Type > Mailbox 15 Type	<ul style="list-style-type: none"> <li>Receive Mailbox</li> <li>Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 12 Frame Type	<ul style="list-style-type: none"> <li>Data Mailbox</li> <li>Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 13 Frame Type	<ul style="list-style-type: none"> <li>Data Mailbox</li> <li>Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 14 Frame Type	<ul style="list-style-type: none"> <li>Data Mailbox</li> <li>Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored

Input > Mailbox 12-15 Group > Mailbox Frame Type > Mailbox 15 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	for transmit mailboxes).
Input > Mailbox 12-15 Group > Mailbox 12-15 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes). Select the Mask for mailboxes 12-15. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 16 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	16	Select the receive ID for mailbox 16, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 17 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	17	Select the receive ID for mailbox 17, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 18 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	18	Select the receive ID for mailbox 18, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID > Mailbox 19 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	19	Select the receive ID for mailbox 19, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is

Input > Mailbox 16-19 Group > Mailbox ID Mode > Mailbox 16 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	not used when the mailbox is set as transmit type.
Input > Mailbox 16-19 Group > Mailbox ID Mode > Mailbox 17 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 16-19 Group > Mailbox ID Mode > Mailbox 18 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 16-19 Group > Mailbox ID Mode > Mailbox 19 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 16 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 17 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 18 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 16-19 Group > Mailbox Type > Mailbox 19 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.

## Mailbox

Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 16 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 17 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 18 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox Frame Type > Mailbox 19 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 16-19 Group > Mailbox 16-19 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 16-19. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 20 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	20	Select the receive ID for mailbox 20, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 21 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	21	Select the receive ID for mailbox 21, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 22 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	22	Select the receive ID for mailbox 22, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID > Mailbox 23 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	23	Select the receive ID for mailbox 23, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 20-23 Group > Mailbox ID Mode > Mailbox 20 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 20-23 Group > Mailbox ID Mode > Mailbox 21 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 20-23 Group > Mailbox ID Mode > Mailbox 22 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 20-23 Group > Mailbox ID Mode > Mailbox 23 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.

Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 20 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 21 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 22 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 20-23 Group > Mailbox Type > Mailbox 23 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 20 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 21 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 22 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 20-23 Group > Mailbox Frame Type > Mailbox 23 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 20-23 Group > Mailbox 20-23 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 20-23. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 24 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	24	Select the receive ID for mailbox 24, between 0 and 0x7ff

when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 25, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 26, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select the receive ID for mailbox 27, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.

Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.

Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 25 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      25

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 26 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      26

Input > Mailbox 24-27 Group > Mailbox ID > Mailbox 27 ID      Value must be decimal or HEX integer of 0x1FFFFFFF or less.      27

Input > Mailbox 24-27 Group > Mailbox ID Mode > Mailbox 24 ID Mode      • Standard ID      Standard ID  
• Extended ID

Input > Mailbox 24-27 Group > Mailbox ID Mode > Mailbox 25 ID Mode      • Standard ID      Standard ID  
• Extended ID

Input > Mailbox 24-27 Group > Mailbox ID Mode > Mailbox 26 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	ID Mode'. Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 24-27 Group > Mailbox ID Mode > Mailbox 27 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 24 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 25 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 26 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 24-27 Group > Mailbox Type > Mailbox 27 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 24 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 25 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 26 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored

Input > Mailbox 24-27 Group > Mailbox Frame Type > Mailbox 27 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	for transmit mailboxes).
Input > Mailbox 24-27 Group > Mailbox 24-27 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).  Select the Mask for mailboxes 24-27. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 28 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	28	Select the receive ID for mailbox 28, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 29 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	29	Select the receive ID for mailbox 29, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 30 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	30	Select the receive ID for mailbox 30, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID > Mailbox 31 ID	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	31	Select the receive ID for mailbox 31, between 0 and 0x7ff when using standard IDs, between 0 and 0x1FFFFFFF when using extended IDs. Value is

Input > Mailbox 28-31 Group > Mailbox ID Mode > Mailbox 28 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	not used when the mailbox is set as transmit type.
Input > Mailbox 28-31 Group > Mailbox ID Mode > Mailbox 29 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 28-31 Group > Mailbox ID Mode > Mailbox 30 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 28-31 Group > Mailbox ID Mode > Mailbox 31 ID Mode	<ul style="list-style-type: none"> <li>• Standard ID</li> <li>• Extended ID</li> </ul>	Standard ID	Select whether the mailbox is used to receive Standard or Extended ID messages. This setting is only valid when Global ID Mode is set to 'Mixed ID Mode'.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 28 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 29 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 30 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit Mailbox</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.
Input > Mailbox 28-31 Group > Mailbox Type > Mailbox 31 Type	<ul style="list-style-type: none"> <li>• Receive Mailbox</li> <li>• Transmit</li> </ul>	Receive Mailbox	Select whether the mailbox is used for receive or transmit.

## Mailbox

Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 28 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 29 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 30 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox Frame Type > Mailbox 31 Frame Type	<ul style="list-style-type: none"> <li>• Data Mailbox</li> <li>• Remote Mailbox</li> </ul>	Data Mailbox	Select whether the mailbox is used to capture data frames or remote frames (ignored for transmit mailboxes).
Input > Mailbox 28-31 Group > Mailbox 28-31 Group Mask	Value must be decimal or HEX integer of 0x1FFFFFFF or less.	0x1FFFFFFF	Select the Mask for mailboxes 28-31. In Mixed ID Mode the Standard ID mask is the upper 11 bits of the full 29-bit mask value.

## Clock Configuration

The CAN peripheral uses the CANMCLK (main-clock oscillator) or PCLKB as its clock source (fCAN, CAN System Clock.) The default CAN configuration will provide a CAN bit rate of 500 Kbit using CANMCLK as the clock source. To set the PCLKB frequency, use the **Clocks** tab of the RA Configuration editor. To change the clock frequency at run-time, use the CGC Interface. Refer to the CGC module guide for more information on configuring clocks.

## Clock Limitations

The following clock limitations apply when using the CAN peripheral:

- When using the main oscillator (CANMCLK) as the clock source:
  - $f_{PCLKB} \geq f_{CANCLK}$  ( $f_{CANCLK} = XTAL / \text{Baud Rate Prescaler}$ )
  - The user application must start the main-clock oscillator (XTAL) at run-time using the CGC Interface if it has not already started (for example, if it is not used as the MCU clock source.)
- When using PCLKB as the clock source:
  - For RA6 and RA4 MCUs, the source of the peripheral module clocks must be PLL for the CAN HAL module.

- For RA4M1 and RA4W1 MCUs, the clock frequency ratio of PCLKA and PCLKB must be 2:1 when using the CAN HAL module. Operation is not guaranteed for other settings.
- For RA2 MCUs only CANMCLK (XTAL) may be used as a clock source. The clock frequency ratio of ICLK and PCLKB must be 2:1 when using the CAN HAL module. Operation is not guaranteed for other settings.

*Note*

*When using CANMCLK (XTAL) as the CAN clock source while running at a reduced main clock speed (under 2x XTAL) be sure to confirm that the XTAL frequency divided by the baud rate prescaler is equal to or less than PCLKB.*

## Pin Configuration

The CAN peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. A CAN channel would consist of two pins - CRX and CTX for data transmission/reception.

## Usage Notes

### Bit Rate Calculation

For convenience, the baudrate of the CAN peripheral is automatically set through the RA Configuration editor using a best effort approach. If the auto-generated baud settings cause deviation that is not tolerable by the application, the user can override the auto-generated settings and put in manually calculated values through RA Configuration editor. For more details on how the baudrate is set refer to section 37.4 "Data Transfer Rate Configuration" of the RA6M3 User's Manual (R01UH0886EJ0100).

### FIFO Support

When FIFO Support is enabled, mailboxes 24-27 form a 4-stage transmit FIFO and mailboxes 28-31 form a 4-stage receive FIFO. The receive FIFO supports two independent ID/mask settings for acceptance filtering.

*Note*

*Only the base mailbox of each FIFO may be accessed. When writing to the TX FIFO it is recommended to use CAN\_MAILBOX\_ID\_TX\_FIFO.*

### Limitations

Developers should be aware of the following limitations when using CAN:

- The `can_frame_t::id_mode` field is only used when Global ID Mode is set to Mixed ID. It is ignored in all other modes.

## Examples

### Basic Example

This is a basic example of minimal use of the CAN in an application.

```
can_frame_t g_can_tx_frame;  
can_frame_t g_can_rx_frame;
```

```
volatile bool    g_rx_flag = false;
volatile bool    g_tx_flag = false;
volatile bool    g_err_flag = false;
volatile uint32_t g_rx_id;
void can_callback (can_callback_args_t * p_args)
{
    switch (p_args->event)
    {
        case CAN_EVENT_RX_COMPLETE:    /* Receive complete event. */
            {
                g_rx_flag = true;
                g_rx_id  = p_args->frame.id;
                /* Read received frame */
                g_can_rx_frame = p_args->frame;
            }
            break;
        case CAN_EVENT_TX_COMPLETE:    /* Transmit complete event. */
            {
                g_tx_flag = true;
            }
            break;
        case CAN_EVENT_ERR_BUS_OFF:    /* Bus error event. (bus off) */
        case CAN_EVENT_ERR_PASSIVE:    /* Bus error event. (error passive) */
        case CAN_EVENT_ERR_WARNING:    /* Bus error event. (error warning) */
        case CAN_EVENT_BUS_RECOVERY:    /* Bus error event. (bus recovery) */
        case CAN_EVENT_MAILBOX_MESSAGE_LOST: /* Overwrite/overrun error */
            {
                /* Set error flag */
                g_err_flag = true;
            }
            break;
        default:
            {
                break;
            }
    }
}
```

```
    }
}
}
void basic_example (void)
{
    fsp_err_t err;
    uint32_t i;
    uint32_t timeout_ms = CAN_BUSY_DELAY;
    /* Initialize the CAN module */
    err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    g_can_tx_frame.id = CAN_DESTINATION_DEVICE_MAILBOX_NUMBER; /* CAN
Destination Device ID */
    g_can_tx_frame.type = CAN_FRAME_TYPE_DATA;
    g_can_tx_frame.data_length_code = CAN_FRAME_TRANSMIT_DATA_BYTES;
    /* Write some data to the transmit frame */
    for (i = 0; i < sizeof(g_can_tx_frame.data); i++)
    {
        g_can_tx_frame.data[i] = (uint8_t) i;
    }
    /* Send data on the bus */
    g_tx_flag = false;
    g_err_flag = false;
    err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
    assert(FSP_SUCCESS == err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((true != g_tx_flag) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (true == g_err_flag)
    {
```

```
    __BKPT(0);  
}  
}
```

## External Loop-back Test

This example requires the CTX and CRX pins to be connected. If a CAN transceiver is onboard a 120 Ohm resistor should be connected across CANH and CANL instead. The mailbox numbers are arbitrarily chosen.

```
void can_external_loopback_example (void)  
{  
    fsp_err_t          err;  
    uint32_t          timeout_ms      = CAN_BUSY_DELAY;  
    can_operation_mode_t operation_mode = CAN_OPERATION_MODE_NORMAL;  
    can_test_mode_t   test_mode      = CAN_TEST_MODE_LOOPBACK_EXTERNAL;  
    int               diff = 0;  
    uint32_t i          = 0;  
    err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    assert(FSP_SUCCESS == err);  
    err = R_CAN_ModeTransition(&g_can0_ctrl, operation_mode, test_mode);  
    assert(FSP_SUCCESS == err);  
    /* Clear the data part of receive frame */  
    memset(g_can_rx_frame.data, 0, CAN_FRAME_TRANSMIT_DATA_BYTES);  
    /* CAN Destination Device ID, in this case it is the same device with another  
mailbox */  
    g_can_tx_frame.id          = CAN_MAILBOX_NUMBER_4;  
    g_can_tx_frame.type       = CAN_FRAME_TYPE_DATA;  
    g_can_tx_frame.data_length_code = CAN_FRAME_TRANSMIT_DATA_BYTES;  
    /* Write some data to the transmit frame */  
    for (i = 0; i < sizeof(g_can_tx_frame.data); i++)  
    {  
        g_can_tx_frame.data[i] = (uint8_t) i;  
    }  
    /* Send data on the bus */
```

```
g_rx_flag = false;
g_err_flag = false;
err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
assert(FSP_SUCCESS == err);
/* Since there is nothing else to do, block until Callback triggers*/
while ((true != g_rx_flag) && timeout_ms)
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (true == g_err_flag)
{
    __BKPT(0);
}
/* Verify received data */
diff = memcmp(&g_can_rx_frame.data[0], &g_can_tx_frame.data[0],
CAN_FRAME_TRANSMIT_DATA_BYTES);
if (0 != diff)
{
    __BKPT(0);
}
}
```

## Data Structures

struct [can\\_mailbox\\_t](#)

struct [can\\_fifo\\_interrupt\\_cfg\\_t](#)

struct [can\\_rx\\_fifo\\_cfg\\_t](#)

struct [can\\_extended\\_cfg\\_t](#)

## Enumerations

enum [can\\_status\\_t](#)

enum [can\\_error\\_t](#)

enum [can\\_mailbox\\_number\\_t](#)

enum [can\\_mailbox\\_send\\_receive\\_t](#)enum [can\\_global\\_id\\_mode\\_t](#)enum [can\\_message\\_mode\\_t](#)enum [can\\_clock\\_source\\_t](#)enum [can\\_fifo\\_interrupt\\_mode\\_t](#)

## Data Structure Documentation

### ◆ can\_mailbox\_t

struct can_mailbox_t		
CAN Mailbox		
Data Fields		
uint32_t	mailbox_id	Mailbox ID.
<a href="#">can_id_mode_t</a>	id_mode	Standard or Extended ID. Only used in Mixed ID mode.
<a href="#">can_frame_type_t</a>	frame_type	Frame type for receive mailbox.
<a href="#">can_mailbox_send_receive_t</a>	mailbox_type	Receive or Transmit mailbox type.

### ◆ can\_fifo\_interrupt\_cfg\_t

struct can_fifo_interrupt_cfg_t		
CAN FIFO interrupt configuration		
Data Fields		
<a href="#">can_fifo_interrupt_mode_t</a>	fifo_int_mode	FIFO interrupts mode (RX and TX combined).
IRQn_Type	tx_fifo_irq	TX FIFO IRQ.
IRQn_Type	rx_fifo_irq	RX FIFO IRQ.

### ◆ can\_rx\_fifo\_cfg\_t

struct can_rx_fifo_cfg_t		
CAN RX FIFO configuration		
Data Fields		
uint32_t	rx_fifo_mask1	RX FIFO acceptance filter mask 1.
uint32_t	rx_fifo_mask2	RX FIFO acceptance filter mask 1.

<a href="#">can_mailbox_t</a>	rx_fifo_id1	RX FIFO acceptance filter ID 1.
<a href="#">can_mailbox_t</a>	rx_fifo_id2	RX FIFO acceptance filter ID 2.

### ◆ can\_extended\_cfg\_t

struct can_extended_cfg_t		
CAN extended configuration		
Data Fields		
<a href="#">can_clock_source_t</a>	clock_source	Source of the CAN clock.
uint32_t *	p_mailbox_mask	Mailbox mask, one for every 4 mailboxes.
<a href="#">can_mailbox_t</a> *	p_mailbox	Pointer to mailboxes.
<a href="#">can_global_id_mode_t</a>	global_id_mode	Standard or Extended ID mode.
uint32_t	mailbox_count	Number of mailboxes.
<a href="#">can_message_mode_t</a>	message_mode	Overwrite message or overrun.
<a href="#">can_fifo_interrupt_cfg_t</a> const *	p_fifo_int_cfg	Pointer to FIFO interrupt configuration.
<a href="#">can_rx_fifo_cfg_t</a> *	p_rx_fifo_cfg	Pointer to RX FIFO configuration.

## Enumeration Type Documentation

## ◆ can\_status\_t

enum can_status_t	
CAN Status	
Enumerator	
CAN_STATUS_NEW_DATA	New Data status flag.
CAN_STATUS_SENT_DATA	Sent Data status flag.
CAN_STATUS_RECEIVE_FIFO	Receive FIFO status flag.
CAN_STATUS_TRANSMIT_FIFO	Transmit FIFO status flag.
CAN_STATUS_NORMAL_MBOX_MESSAGE_LOST	Normal mailbox message lost status flag.
CAN_STATUS_FIFO_MBOX_MESSAGE_LOST	FIFO mailbox message lost status flag.
CAN_STATUS_TRANSMISSION_ABORT	Transmission abort status flag.
CAN_STATUS_ERROR	Error status flag.
CAN_STATUS_RESET_MODE	Reset mode status flag.
CAN_STATUS_HALT_MODE	Halt mode status flag.
CAN_STATUS_SLEEP_MODE	Sleep mode status flag.
CAN_STATUS_ERROR_PASSIVE	Error-passive status flag.
CAN_STATUS_BUS_OFF	Bus-off status flag.

◆ **can\_error\_t**

enum <code>can_error_t</code>	
CAN Error Code	
Enumerator	
<code>CAN_ERROR_STUFF</code>	Stuff Error.
<code>CAN_ERROR_FORM</code>	Form Error.
<code>CAN_ERROR_ACK</code>	ACK Error.
<code>CAN_ERROR_CRC</code>	CRC Error.
<code>CAN_ERROR_BIT_RECESSIVE</code>	Bit Error (recessive) Error.
<code>CAN_ERROR_BIT_DOMINANT</code>	Bit Error (dominant) Error.
<code>CAN_ERROR_ACK_DELIMITER</code>	ACK Delimiter Error.

◆ **can\_mailbox\_number\_t**

enum <code>can_mailbox_number_t</code>
CAN Mailbox IDs (MB + FIFO)

◆ **can\_mailbox\_send\_receive\_t**

enum <code>can_mailbox_send_receive_t</code>	
CAN Mailbox type	
Enumerator	
<code>CAN_MAILBOX_RECEIVE</code>	Mailbox is for receiving.
<code>CAN_MAILBOX_TRANSMIT</code>	Mailbox is for sending.

◆ **can\_global\_id\_mode\_t**

enum <a href="#">can_global_id_mode_t</a>	
Global CAN ID mode settings	
Enumerator	
CAN_GLOBAL_ID_MODE_STANDARD	Standard IDs of 11 bits used.
CAN_GLOBAL_ID_MODE_EXTENDED	Extended IDs of 29 bits used.
CAN_GLOBAL_ID_MODE_MIXED	Both Standard and Extended IDs used.

◆ **can\_message\_mode\_t**

enum <a href="#">can_message_mode_t</a>	
CAN Message Modes	
Enumerator	
CAN_MESSAGE_MODE_OVERWRITE	Receive data will be overwritten if not read before the next frame.
CAN_MESSAGE_MODE_OVERRUN	Receive data will be retained until it is read.

◆ **can\_clock\_source\_t**

enum <a href="#">can_clock_source_t</a>	
CAN Source Clock	
Enumerator	
CAN_CLOCK_SOURCE_PCLKB	PCLKB is the source of the CAN Clock.
CAN_CLOCK_SOURCE_CANMCLK	CANMCLK is the source of the CAN Clock.

◆ **can\_fifo\_interrupt\_mode\_t**

enum <a href="#">can_fifo_interrupt_mode_t</a>	
CAN FIFO Interrupt Modes	

**Function Documentation**

◆ **R\_CAN\_Open()**

```
fsp_err_t R_CAN_Open ( can_ctrl_t*const p_api_ctrl, can_cfg_t const*const p_cfg )
```

Open and configure the CAN channel for operation.

Example:

```
/* Initialize the CAN module */
err = R_CAN_Open(&g_can0_ctrl, &g_can0_cfg);
```

**Return values**

FSP_SUCCESS	Channel opened successfully
FSP_ERR_ALREADY_OPEN	Driver already open.
FSP_ERR_CAN_INIT_FAILED	Channel failed to initialize.
FSP_ERR_ASSERTION	Null pointer presented.

◆ **R\_CAN\_Close()**

```
fsp_err_t R_CAN_Close ( can_ctrl_t*const p_api_ctrl)
```

Close the CAN channel.

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented.

◆ **R\_CAN\_Write()**

```
fsp_err_t R_CAN_Write ( can_ctrl_t *const p_api_ctrl, uint32_t mailbox, can_frame_t *const p_frame )
```

Write data to the CAN channel. Write up to eight bytes to the channel mailbox.

Example:

```
err = R_CAN_Write(&g_can0_ctrl, CAN_MAILBOX_NUMBER_31, &g_can_tx_frame);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_CAN_TRANSMIT_NOT_READY	Transmit in progress, cannot write data at this time.
FSP_ERR_CAN_TRANSMIT_FIFO_FULL	Transmit FIFO is full.
FSP_ERR_CAN_RECEIVE_MAILBOX	Mailbox is setup for receive and cannot send.
FSP_ERR_INVALID_ARGUMENT	Data length or frame type invalid.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_Read()**

```
fsp_err_t R_CAN_Read ( can_ctrl_t *const p_api_ctrl, uint32_t mailbox, can_frame_t *const p_frame )
```

Read data from a mailbox or FIFO.

**Note**

*This function is not supported.*

**Return values**

FSP_ERR_UNSUPPORTED	Function not supported.
---------------------	-------------------------

◆ **R\_CAN\_ModeTransition()**

```
fsp_err_t R_CAN_ModeTransition ( can_ctrl_t *const p_api_ctrl, can_operation_mode_t
operation_mode, can_test_mode_t test_mode )
```

CAN Mode Transition is used to change CAN driver state.

Example:

```
err = R_CAN_ModeTransition(&g_can0_ctrl, operation_mode, test_mode);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_InfoGet()**

```
fsp_err_t R_CAN_InfoGet ( can_ctrl_t *const p_api_ctrl, can_info_t *const p_info )
```

Get CAN state and status information for the channel.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CAN\_CallbackSet()**

```
fsp_err_t R_CAN_CallbackSet ( can_ctrl_t *const p_api_ctrl, void (*)(can_callback_args_t *)
p_callback, void const *const p_context, can_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `can_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.8 Controller Area Network - Flexible Data (r\_canfd)**

## Modules

**Functions**

```
fsp_err_t R_CANFD_Open (can_ctrl_t *const p_api_ctrl, can_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_CANFD_Close (can_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_CANFD_Write (can_ctrl_t *const p_api_ctrl, uint32_t const buffer,
can_frame_t *const p_frame)
```

```
fsp_err_t R_CANFD_Read (can_ctrl_t *const p_api_ctrl, uint32_t const buffer,
can_frame_t *const p_frame)
```

```
fsp_err_t R_CANFD_ModeTransition (can_ctrl_t *const p_api_ctrl,
can_operation_mode_t operation_mode, can_test_mode_t test_mode)
```

```
fsp_err_t R_CANFD_InfoGet (can_ctrl_t *const p_api_ctrl, can_info_t *const
p_info)
```

```
fsp_err_t R_CANFD_CallbackSet (can_ctrl_t *const p_api_ctrl,
void (*p_callback)(can_callback_args_t *), void const *const
p_context, can_callback_args_t *const p_callback_memory)
```

**Detailed Description**

Driver for the CANFD peripheral on RA MCUs. This module implements the [CAN Interface](#).

## Overview

The CANFD module can be used to communicate over CAN networks, optionally using Flexible Data (CAN-FD) to accelerate the data phase. A variety of message filtering and buffer options are available.

### Features

- Compatibility
  - Send and receive CAN 2.0 and CAN-FD frames on the same channel
  - Bitrate up to 1 Mbps with FD data phase speeds up to 8 Mbps
  - Supports both ISO 11898-1 and Bosch V1.0 CAN-FD specifications
- Buffers
  - 32 global receive Message Buffers (RX MBs)
  - 8 global receive FIFOs (RX FIFOs)
  - 16 transmit Message Buffers (TX MBs) per channel
- Filtering
  - Up to 128 filter rules across both channels
  - Each rule can be individually configured to filter based on:
    - ID
    - Standard or Extended ID (IDE bit)
    - Data or Remote Frame (RTR bit)
    - ID/IDE/RTR mask
    - Minimum DLC (data length) value
- Interrupts
  - Configurable Global RX FIFO Interrupt
    - Configurable per FIFO
    - Interrupt at a certain depth or on every received message
  - Channel TX Interrupt
  - Global Error
    - DLC Check
    - Message Lost
    - FD Payload Overflow
  - Channel Error
    - Bus Error
    - Error Warning
    - Error Passive
    - Bus-Off Entry
    - Bus-Off Recovery
    - Overload
    - Bus Lock
    - Arbitration Loss
    - Transmission Aborted

## Configuration

### Build Time Configurations for r\_canfd

The following build time configurations are defined in `fsp_cfg/r_canfd_cfg.h`:

Configuration	Options	Default	Description
Global Error Interrupt > Priority	MCU Specific Options		This interrupt is fired for each of the error sources selected below.
Global Error Interrupt > Sources	<ul style="list-style-type: none"> <li>DLC Check</li> <li>Message Lost</li> <li>FD Payload Overflow</li> </ul>	0U	Select which errors should trigger an interrupt.
Global Error Interrupt > Callback Channel	<ul style="list-style-type: none"> <li>Channel 0</li> <li>Channel 1</li> </ul>	Channel 1	Specify which channel callback should be called to handle global errors. When starting the driver this channel must be opened first.
Flexible Data (FD) > FD Frame Format	<ul style="list-style-type: none"> <li>ISO 11898-1</li> <li>Bosch CAN FD Specification V1.0</li> </ul>	ISO 11898-1	Select whether to use the FD frame standard provided by ISO or Bosch.
Flexible Data (FD) > Protocol Exceptions	<ul style="list-style-type: none"> <li>Enabled (ISO 11898-1)</li> <li>Disabled</li> </ul>	Enabled (ISO 11898-1)	Select whether to enter the protocol exception handling state when a RES bit is sampled recessive as defined in ISO 11898-1.
Flexible Data (FD) > Payload Overflow	<ul style="list-style-type: none"> <li>Reject</li> <li>Truncate</li> </ul>	Reject	Configure whether received messages larger than the destination buffer should be truncated or rejected.
Reception > Message Buffers > Number of Buffers	RX Message Buffer number must be an integer between 0 and 32.	0	Number of message buffers available for reception.  As there is no interrupt for message buffer reception it is recommended to use RX FIFOs instead. Set this value to 0 to disable RX Message Buffers.
Reception > Message Buffers > Payload Size	<ul style="list-style-type: none"> <li>8 bytes</li> <li>12 bytes</li> <li>16 bytes</li> <li>20 bytes</li> <li>24 bytes</li> <li>32 bytes</li> <li>48 bytes</li> </ul>	8 bytes	Payload size for all RX Message Buffers.

	<ul style="list-style-type: none"> <li>• 64 bytes</li> </ul>		
Reception > FIFOs > FIFO 0 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable or disable RX FIFO 0.
Reception > FIFOs > FIFO 0 > Interrupt Mode	MCU Specific Options		Set the interrupt mode for RX FIFO 0. Threshold mode will only fire an interrupt each time an incoming message crosses the threshold value set below.
Reception > FIFOs > FIFO 0 > Interrupt Threshold	MCU Specific Options		Set the interrupt threshold value for RX FIFO 0. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 0 > Payload Size	MCU Specific Options		Select the message payload size for RX FIFO 0.
Reception > FIFOs > FIFO 0 > Depth	MCU Specific Options		Select the number of stages for RX FIFO 0.
Reception > FIFOs > FIFO 1 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable RX FIFO 1.
Reception > FIFOs > FIFO 1 > Interrupt Mode	MCU Specific Options		Set the interrupt mode for RX FIFO 1. Threshold mode will only fire an interrupt each time an incoming message crosses the threshold value set below.
Reception > FIFOs > FIFO 1 > Interrupt Threshold	MCU Specific Options		Set the interrupt threshold value for RX FIFO 1. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 1 > Payload Size	MCU Specific Options		Select the message payload size for RX FIFO 1.
Reception > FIFOs > FIFO 1 > Depth	MCU Specific Options		Select the number of stages for RX FIFO 1.
Reception > FIFOs > FIFO 2 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable RX FIFO 2.

Reception > FIFOs > FIFO 2 > Interrupt Mode	MCU Specific Options		Set the interrupt mode for RX FIFO 2. Threshold mode will only fire an interrupt each time an incoming message crosses the threshold value set below.
Reception > FIFOs > FIFO 2 > Interrupt Threshold	MCU Specific Options		Set the interrupt threshold value for RX FIFO 2. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 2 > Payload Size	MCU Specific Options		Select the message payload size for RX FIFO 2.
Reception > FIFOs > FIFO 2 > Depth	MCU Specific Options		Select the number of stages for RX FIFO 2.
Reception > FIFOs > FIFO 3 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable RX FIFO 3.
Reception > FIFOs > FIFO 3 > Interrupt Mode	MCU Specific Options		Set the interrupt mode for RX FIFO 3. Threshold mode will only fire an interrupt each time an incoming message crosses the threshold value set below.
Reception > FIFOs > FIFO 3 > Interrupt Threshold	MCU Specific Options		Set the interrupt threshold value for RX FIFO 3. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 3 > Payload Size	MCU Specific Options		Select the message payload size for RX FIFO 3.
Reception > FIFOs > FIFO 3 > Depth	MCU Specific Options		Select the number of stages for RX FIFO 3.
Reception > FIFOs > FIFO 4 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable or disable RX FIFO 4.
Reception > FIFOs > FIFO 4 > Interrupt Mode	MCU Specific Options		Set the interrupt mode for RX FIFO 4. Threshold mode will only fire an interrupt each time an incoming



FIFO 6 > Interrupt Threshold				threshold value for RX FIFO 6. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 6 > Payload Size	MCU Specific Options			Select the message payload size for RX FIFO 6.
Reception > FIFOs > FIFO 6 > Depth	MCU Specific Options			Select the number of stages for RX FIFO 6.
Reception > FIFOs > FIFO 7 > Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled		Enable or disable RX FIFO 7.
Reception > FIFOs > FIFO 7 > Interrupt Mode	MCU Specific Options			Set the interrupt mode for RX FIFO 7. Threshold mode will only fire an interrupt each time an incoming message crosses the threshold value set below.
Reception > FIFOs > FIFO 7 > Interrupt Threshold	MCU Specific Options			Set the interrupt threshold value for RX FIFO 7. This setting is only applicable when the Interrupt Mode is set to 'At Threshold Value'.
Reception > FIFOs > FIFO 7 > Payload Size	MCU Specific Options			Select the message payload size for RX FIFO 7.
Reception > FIFOs > FIFO 7 > Depth	MCU Specific Options			Select the number of stages for RX FIFO 7.
Reception > FIFOs > Interrupt Priority	MCU Specific Options			This priority level will apply to all FIFO interrupts globally.
Reception > Acceptance Filtering > Channel 0 Rule Count	The number of AFL rules must be an integer between 0 and 128.	64		Number of acceptance filter list rules dedicated to Channel 0.
Reception > Acceptance Filtering > Channel 1 Rule Count	The number of AFL rules must be an integer between 0 and 128.	64		Number of acceptance filter list rules dedicated to Channel 1.
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)		If selected code for parameter checking is included in the build.

Transmission Priority	<ul style="list-style-type: none"> <li>• Message ID</li> <li>• Buffer Number</li> </ul>	Buffer Number	Select how messages should be prioritized for transmission. In either case, lower numbers indicate higher priority.
DLC Check	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> <li>• Enabled w/truncate</li> </ul>	config.driver.canfd.dlc_check.disabled	When enabled received messages will be rejected if their DLC field is less than the value configured in the associated AFL rule. If 'Enabled w/truncate' is selected and a message passes the DLC check the DLC field is set to the value in the associated AFL rule and any excess data is discarded.

### Configurations for Driver > Connectivity > CANFD Driver on r\_canfd

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > CANFD Driver on r\_canfd. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_canfd0	Module name.
General > Channel	Channel should be 0 or 1	0	Specify the CAN channel to use.
Bitrate > Automatic > Nominal Rate (bps)	Must be a valid integer with a maximum of 1MHz.	500000	Specify nominal bitrate in bits per second.
Bitrate > Automatic > Data Rate (bps)	Must be a valid integer with a maximum of 8MHz.	2000000	Specify data bitrate in bits per second.
Bitrate > Automatic > Sample Point (%)	Must be a valid integer between 60 and 99.	75	Specify desired sample point.
Bitrate > Manual > Nominal > Prescaler (divisor)	Value must be a non-negative integer between 1 and 1024.	1	Specify clock divisor for nominal bitrate.
Bitrate > Manual > Nominal > Time Segment 1 (Tq)	Value must be a non-negative integer between 2 and 256.	29	Select the Time Segment 1 value. Check module usage notes for how to calculate this value.
Bitrate > Manual >	Value must be a non-	10	Select the Time

Nominal > Time Segment 2 (Tq)	negative integer between 2 and 128.		Segment 2 value. Check module usage notes for how to calculate this value.
Bitrate > Manual > Nominal > Sync Jump Width (Tq)	Value must be a non-negative integer between 1 and 128.	4	Select the Synchronization Jump Width value. Check module usage notes for how to calculate this value.
Bitrate > Manual > Data > Prescaler (divisor)	Value must be a non-negative integer between 1 and 1024.	1	Specify clock divisor for data bitrate.
Bitrate > Manual > Data > Time Segment 1 (Tq)	Value must be a non-negative integer between 2 and 256.	2	Select the Time Segment 1 value. Check module usage notes for how to calculate this value.
Bitrate > Manual > Data > Time Segment 2 (Tq)	Value must be a non-negative integer between 2 and 128.	2	Select the Time Segment 2 value. Check module usage notes for how to calculate this value.
Bitrate > Manual > Data > Sync Jump Width (Tq)	Value must be a non-negative integer between 1 and 128.	1	Select the Synchronization Jump Width value. Check module usage notes for how to calculate this value.
Bitrate > Manual > Use manual settings	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Select whether or not to override automatic baudrate generation and instead use the values specified here.
Bitrate > Delay Compensation	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Enable	When enabled the CANFD module will automatically compensate for any transceiver or bus delay between transmitted and received bits. When manually supplying bit timing values with delay compensation enabled be sure the data prescaler is 2 or smaller for correct operation.
Interrupts > Callback	Name must be a valid	canfd0_callback	A user callback

	C symbol		function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time any interrupt occurs.
Interrupts > Channel Interrupt Priority Level	MCU Specific Options		Channel Error/Transmit interrupt priority.
Transmit Interrupts	Refer to the RA Configuration tool for available options.	0ULL	Select which TX Message Buffers should trigger an interrupt when transmission is complete.
Channel Error Interrupts	<ul style="list-style-type: none"> <li>• Error Warning</li> <li>• Error Passive</li> <li>• Bus-Off Entry</li> <li>• Bus-Off Recovery</li> <li>• Overload</li> </ul>	0U	Select which channel error interrupt sources to enable.
Filter List Array	Name must be a valid C symbol	p_canfd0_afl	Acceptance Filter List (AFL) rule array symbol name.

## Clock Configuration

The CANFD peripheral uses either PLL, PLL2 or the main oscillator as its clock source. The RA Configuration editor will attempt to get as close as possible to the supplied bitrate with the configured clock source. To achieve an exact bitrate the CANFD source clock or divisor may need to be adjusted to meet the criteria in the formula below:

```
bitrate = canfd_clock_hz / ((time_segment_1 + time_segment_2 + 1) * prescalar)
```

For CANFD, the possible values for each element are as follows:

Element	Min	Max (Nominal)	Max (Data)
Bitrate	-	1 Mbps	8 Mbps
Time Segment 1	2 Tq	256 Tq	32 Tq
Time Segment 2	2 Tq	128 Tq	16 Tq
Sync Jump Width	1 Tq	Time Segment 2	Time Segment 2
Prescalar	1	1024	256

Use the **Clocks** tab of the RA Configuration editor to configure the CANFD clock source/divisor as well as to set the frequency of PLL or PLL2. To change the clock frequency at run-time, use the CGC Interface. Refer to the CGC module guide for more information on configuring clocks.

## Pin Configuration

CANFD channels each control two pins: CRX (receive) and CTX (transmit).

## Usage Notes

### Buffers

The CANFD driver provides three types of buffers: Transmit Message Buffers (TX MBs), Receive Message Buffers (RX MBs) and Receive FIFOs (RX FIFOs).

### TX Message Buffers

TX MBs are used for transmission only. Refer to the hardware manual for your device for information on which TX MBs are available.

#### Note

*The CANFD peripheral continually scans TX MBs for new data. Depending on the provided clock it may be possible to write to multiple TX MBs before transmission begins. In this case, messages will be sent in the priority specified by the Transmission Priority option in the RA Configuration editor.*

### RX Message Buffers

RX MBs are for reception only and may only hold one message at a time. 32 total RX MBs are available and are shared across all channels.

No interrupts are provided for RX MBs. Use [R\\_CANFD\\_InfoGet](#) and [R\\_CANFD\\_Read](#) to poll and read them, respectively.

### RX FIFOs

RX FIFOs provide interrupt-driven queue functionality for receiving messages. 8 RX FIFOs are available, shared across all channels. All FIFOs have the following capabilities:

- Up to 64 byte payloads
- Up to 128 message capacity
- Interrupt events:
  - On every received frame OR when filled to a specified fraction of its capacity
  - When a message is overwritten (message received on full FIFO)

Once an interrupt is fired it will continue to fire until the FIFO is emptied and all messages have been passed to user code via the callback. When using the threshold interrupt mode a FIFO can be checked for data and read between interrupts by calling [R\\_CANFD\\_InfoGet](#) and [R\\_CANFD\\_Read](#), respectively.

### RX Buffer Pool

The CANFD peripheral has a limited amount of buffer pool RAM available for allocating RX MBs and FIFO stages. The RA Configuration editor will provide a warning when the limit is exceeded.

The number of bytes used by RX MBs and individual FIFOs can be calculated as follows:

```
Total RX MB bytes used = (number of RX MBs enabled) * (RX MB payload size + 12 bytes)
RX FIFO bytes used = (number of FIFO stages) * (FIFO payload size + 12 bytes)
```

## Message Filtering (Acceptance Filter List)

To filter messages to the desired message buffer or FIFO the CANFD peripheral uses an Acceptance Filter List (AFL). Each entry in the AFL provides a rule to check a message against along with destination and other filtering information. When a message is received the CANFD peripheral internally checks against every configured AFL rule for the channel. If a match is found the message is transferred to the destination(s) specified in the rule. The default template with one entry is shown below:

```
static const canfd_afl_entry_t p_canfd0_afl[CANFD_CFG_AFL_CHO_RULE_NUM] =
{
    {
        .id =
        {
            /* Specify the ID, ID type and frame type to accept. */
            .id          = 0x00000000,
            .frame_type = CAN_FRAME_TYPE_DATA,
            .id_mode     = CAN_ID_MODE_EXTENDED,
        },
        .mask =
        {
            /* These values mask which ID/mode bits to compare when filtering messages. */
            .mask_id          = 0x1FFFFFFF,
            .mask_frame_type = 1,
            .mask_id_mode     = 1,
        },
        .destination =
        {
            /* If DLC checking is enabled any messages shorter than the below setting will be
            rejected. */
            .minimum_dlc = CANFD_MINIMUM_DLC_0,
            /* Optionally specify a Receive Message Buffer (RX MB) to store accepted frames. RX
            MBs do not have an
            * interrupt or overwrite protection and must be checked with R_CANFD_InfoGet and
            R_CANFD_Read. */
            .rx_buffer = CANFD_RX_MB_NONE,
            /* Specify which FIFO(s) to send filtered messages to. Multiple FIFOs can be OR'd
```

```

together. */

        .fifo_select_flags = CANFD_RX_FIFO_0,

    }

}

};
    
```

AFL templates can be easily added to a project using the Developer Assistance feature in e2 studio. Once the CANFD module is added to a project, drag and drop the elements circled below to build a filter list:

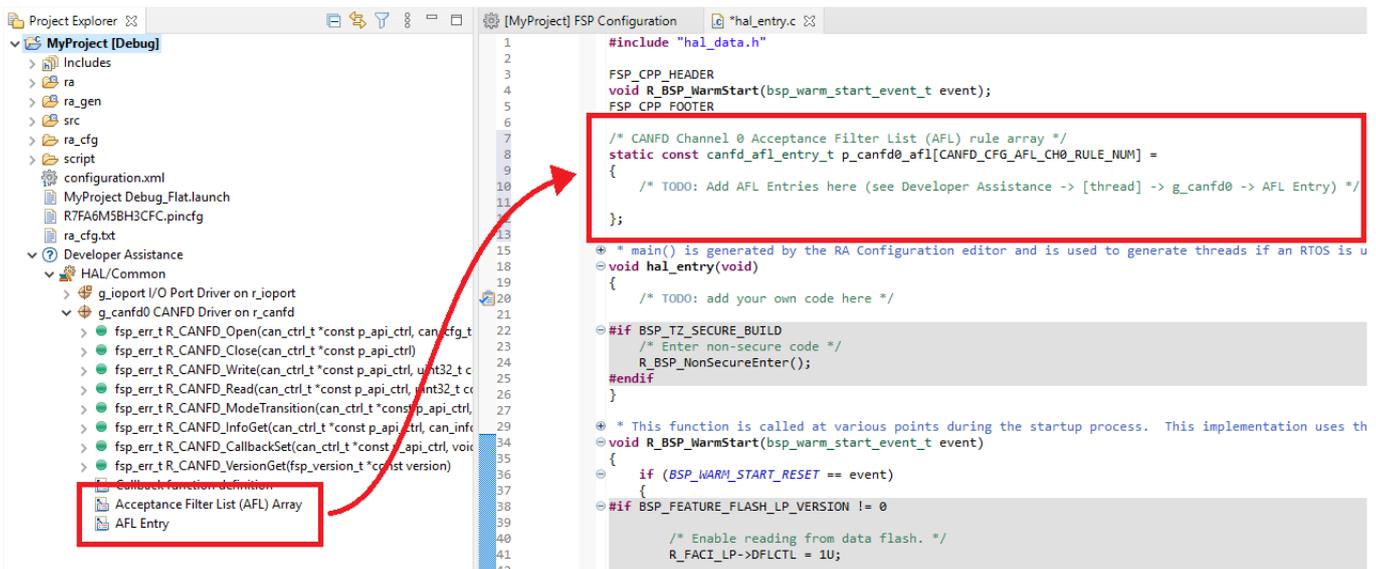


Figure 149: CANFD Developer Assistance AFL Templates

For an example configuration refer to the [AFL Example](#) below.

### Flexible Data (FD)

Flexible Data is an extension of the CAN protocol allowing for messages up to 64 bytes and higher data bitrates, among other features. The CANFD driver supports the following:

- Sending and receiving FD messages
- Bitrate switching for data phase (up to 8 MHz)
- Manual and automatic setting of the error state (ESI) bit

To specify one or more of these options when transmitting set `can_frame_t::options` with combined values from `canfd_frame_options_t`. Received messages will automatically have this field filled, if applicable.

```

/* Configure a frame to write 64 bytes with bitrate switching (BRS) enabled */
g_can_tx_frame.id = CAN_EXAMPLE_ID;
    
```

```
g_can_tx_frame.id_mode           = CAN_ID_MODE_STANDARD ;
g_can_tx_frame.type              = CAN_FRAME_TYPE_DATA ;
g_can_tx_frame.data_length_code  = CAN_EXAMPLE_64_BYTES ;
g_can_tx_frame.options           = CANFD_FRAME_OPTION_FD | CANFD_FRAME_OPTION_BRS ;
```

#### Note

When using bitrate switching be sure to configure the Data Bitrate as desired in the RA Configuration editor.

## Bit Rate Calculation

For convenience, the baudrate of the CAN peripheral is automatically set through the RA Configuration editor using a best effort approach. To increase compliance and reliability two extra options are provided: Link Prescalers and Delay Compensation.

When Link Prescalers is enabled the prescalers for Nominal and Data bitrates will be kept the same, improving clock tolerance in networks using FD frames. This option somewhat limits the available options for bitrate settings, so be sure to check that the automatically generated values are acceptable.

Enabling Delay Compensation instructs the CANFD peripheral to measure TX to RX transceiver delay and automatically adjust for it, improving the reliability of high-speed FD messages. This option may severely limit available bitrate settings depending on the source clock; it is highly recommended to check the generated values when enabled.

If the auto-generated baud settings cause deviation that is not tolerable by the application the user can override the auto-generated settings and put in manually calculated values through the RA Configuration editor. For more details on how the bitrate is calculated refer to the [Clock Configuration](#) section above.

## Sync Jump Width

The Sync Jump Width option specifies the maximum number of time quanta that the sample point may be delayed by to account for differences in oscillators on the bus. It should be set to a value between 1 and the configured Time Segment 2 value depending on the maximum permissible clock error.

## Error Handling

The CANFD peripheral provides two types of error interrupts: Channel and Global. As the names imply, each channel has its own Channel Error interrupt but there is only one Global Error interrupt. Only the configured channel will receive callbacks for Global Errors.

Error interrupt callbacks will pass either [CAN\\_EVENT\\_ERR\\_CHANNEL](#) or [CAN\\_EVENT\\_ERR\\_GLOBAL](#) in the `can_callback_args_t::event` field. A second field, `can_callback_args_t::error`, provides the actual error code as `canfd_error_t`. Cast to this enum to retrieve the error condition. See the callback in the [Basic Example](#) below for a demonstration.

## DLC Checking

When DLC Checking is enabled messages are checked against the `destination.minimum_dlc` value of each AFL rule. If the data length of a message is less than this value the message will be rejected.

When DLC checking is set to "Enabled w/truncate" in the RA Configuration editor any data in excess of the minimum DLC setting will be truncated and the DLC value for the frame will be set to match.

## FD Payload Overflow

When an FD message is received with a DLC larger than the destination buffer an FD Payload Overflow interrupt is thrown (if configured). When Payload Overflow is set to "Truncate" the message will still be accepted but only data up to the buffer capacity will be preserved. The DLC value is unchanged in this case; any data beyond this value in the `can_frame_t::data` array should not be used.

## Test Modes

The CANFD peripheral provides three basic test modes: Listen Only, Internal Loopback and External Loopback. Use [R\\_CANFD\\_ModeTransition](#) to switch to a test mode.

An additional "Internal Bus" test mode is available that allows connecting both CANFD channels together on an internal bus, effectively creating an internal CAN network. See the [Internal Bus](#) example below for details.

## Limitations

Developers should be aware of the following limitations when using CANFD:

- RX Message Buffers do not have an associated interrupt. To use them in an application one of the following is recommended:
  - Use [R\\_CANFD\\_InfoGet](#) to determine if any RX MBs have received data, then use [R\\_CANFD\\_Read](#) to obtain it
  - Select an RX FIFO as an additional destination for the relevant filter rules and configure the FIFO interrupt/callback as desired
- The CANFD peripheral has a limited amount of buffer pool RAM available for allocating RX MBs and FIFO stages. See the [RX Buffer Pool](#) section above for more information.
- When switching modes with [R\\_CANFD\\_ModeTransition](#) a delay of up to several CAN frames may be incurred. Consult Section 32.3.4.2 "Timing of Channel Mode Change" in the RA6M5 User's Manual (R01UH0891EJ0100) for details.
- Only one channel will receive callbacks for Global Errors. If a different channel is opened first these error interrupts will be suppressed until the specified handler channel is opened.

## Examples

### AFL Example

The below is an example Acceptance Filter List (AFL) declaration with two rules.

```
const canfd_afl_entry_t p_canfd0_afl[CANFD_CFG_AFL_CH1_RULE_NUM] =
{
    /* Store all data frames with at least 4 bytes from Standard IDs 0x40-0x4F in RX
    FIFO 0 and RX FIFO 1 */
    {
        .id =
```

```

    {
        .id          = 0x40,
        .frame_type = CAN_FRAME_TYPE_DATA,
        .id_mode     = CAN_ID_MODE_STANDARD
    },
    .mask =
    {
        .mask_id      = 0x7F0,
        .mask_frame_type = 1,
        .mask_id_mode = 1
    },
    .destination =
    {
        .minimum_dlc      = CANFD_MINIMUM_DLC_4,
        .rx_buffer        = CANFD_RX_MB_NONE,
        .fifo_select_flags = (canfd_rx_fifo_t) (CANFD_RX_FIFO_0 |
CANFD_RX_FIFO_1)
    }
},
/* Store all frames from Extended ID 0x1100 in RX FIFO 2 and RX MB 0 */
{
    .id =
    {
        .id          = 0x1100,
        .frame_type = CAN_FRAME_TYPE_DATA, // This setting is ignored by the mask
        .id_mode     = CAN_ID_MODE_EXTENDED
    },
    .mask =
    {
        .mask_id      = 0x1FFFFFFF,
        .mask_frame_type = 0,
        .mask_id_mode = 1
    },
    .destination =

```

```
{
    .minimum_dlc      = CANFD_MINIMUM_DLC_0,
    .rx_buffer        = CANFD_RX_MB_0,
    .fifo_select_flags = CANFD_RX_FIFO_2
}
};
```

## Basic Example

This is a basic example of minimal use of the CANFD module in an application.

### Note

*It is recommended to use RX FIFOs for reception as there are no interrupts for RX message buffers.*

```
#define CAN_EXAMPLE_ID (0x20)
can_frame_t g_can_tx_frame;
can_frame_t g_can_rx_frame;
volatile canfd_error_t g_err_status = (canfd_error_t) 0;
void canfd_callback (can_callback_args_t * p_args)
{
    switch (p_args->event)
    {
        case CAN_EVENT_RX_COMPLETE: /* Receive complete event. */
        {
            /* Read received frame */
            memcpy(&g_can_rx_frame, p_args->p_frame, sizeof(can_frame_t));
            /* Handle event */
            break;
        }
        case CAN_EVENT_TX_COMPLETE: /* Transmit complete event. */
        {
            /* Handle event */
            break;
        }
        case CAN_EVENT_ERR_GLOBAL: /* Global error. */
```

```
case CAN_EVENT_ERR_CHANNEL:                                /* Channel error. */
{
/* Get error status */
    g_err_status = (canfd_error_t) p_args->error; /* Check error code with
canfd_error_t. */
/* Handle event */
break;
}
default:
{
break;
}
}
}

void canfd_basic_example (void)
{
    fsp_err_t err;
/* Initialize the CAN module */
    err = R_CANFD_Open(&g_canfd0_ctrl, &g_canfd0_cfg);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
/* Setup frame to write to CAN ID 0x20 */
    g_can_tx_frame.id           = CAN_EXAMPLE_ID;
    g_can_tx_frame.id_mode     = CAN_ID_MODE_STANDARD;
    g_can_tx_frame.type        = CAN_FRAME_TYPE_DATA;
    g_can_tx_frame.data_length_code = 8;
    g_can_tx_frame.options     = 0;
/* Write some data to the transmit frame */
for (uint32_t i = 0; i < 8; i++)
{
    g_can_tx_frame.data[i] = (uint8_t) i;
}
/* Send data on the bus */
    err = R_CANFD_Write(&g_canfd0_ctrl, CANFD_TX_MB_0, &g_can_tx_frame);
```

```
    assert(FSP_SUCCESS == err);

    /* Wait for a transmit callback event */
}
```

## Flexible Data

This example demonstrates sending an FD message with bitrate switching over external loopback. The CTX and CRX pins must be connected when using external loopback, though if a CAN transceiver is onboard a 120 Ohm resistor should be connected across CANH and CANL instead.

```
#define CAN_EXAMPLE_64_BYTES 64

void canfd_fd_loopback_example (void)
{
    fsp_err_t err;

    err = R_CANFD_Open(&g_canfd0_ctrl, &g_canfd0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Switch to external loopback mode */
    err = R_CANFD_ModeTransition(&g_canfd0_ctrl, CAN_OPERATION_MODE_NORMAL,
CAN_TEST_MODE_LOOPBACK_EXTERNAL);
    assert(FSP_SUCCESS == err);

    /* Configure a frame to write 64 bytes with bitrate switching (BRS) enabled */
    g_can_tx_frame.id           = CAN_EXAMPLE_ID;
    g_can_tx_frame.id_mode      = CAN_ID_MODE_STANDARD;
    g_can_tx_frame.type         = CAN_FRAME_TYPE_DATA;
    g_can_tx_frame.data_length_code = CAN_EXAMPLE_64_BYTES;
    g_can_tx_frame.options      = CANFD_FRAME_OPTION_FD | CANFD_FRAME_OPTION_BRS;

    /* Write some data to the transmit frame */
    for (uint32_t i = 0; i < CAN_DATA_BUFFER_LENGTH; i++)
    {
        g_can_tx_frame.data[i] = (uint8_t) i;
    }

    /* Send data on the bus */
    err = R_CANFD_Write(&g_canfd0_ctrl, CANFD_TX_MB_0, &g_can_tx_frame);
    assert(FSP_SUCCESS == err);

    /* Wait for a transmit and/or receive callback event */
}
```

```
}

```

## Internal Bus

In this example two CANFD channels are connected to the Internal Bus test mode. API error checking has been omitted for clarity.

### Note

*Use of Global Modes for any other purpose is not recommended without consulting the device User's Manual.*

## Data Structures

struct [canfd\\_afl\\_entry\\_t](#)

struct [canfd\\_global\\_cfg\\_t](#)

struct [canfd\\_extended\\_cfg\\_t](#)

## Enumerations

enum [canfd\\_status\\_t](#)

enum [canfd\\_error\\_t](#)

enum [canfd\\_tx\\_mb\\_t](#)

enum [canfd\\_rx\\_buffer\\_t](#)

enum [canfd\\_rx\\_mb\\_t](#)

enum [canfd\\_rx\\_fifo\\_t](#)

enum [canfd\\_minimum\\_dlc\\_t](#)

enum [canfd\\_frame\\_options\\_t](#)

## Data Structure Documentation

### ◆ canfd\_afl\_entry\_t

struct canfd\_afl\_entry\_t

AFL Entry (based on R\_CANFD\_CFDGAFL\_Type in renesas.h)

### ◆ canfd\_global\_cfg\_t

struct canfd\_global\_cfg\_t

CANFD Global Configuration

Data Fields		
uint32_t	global_interrupts	Global control options (CFDGCTR register setting)
uint32_t	global_config	Global configuration options (CFDGCFCG register setting)
uint32_t	rx_fifo_config[8]	RX FIFO configuration (CFDRFCCn register settings)
uint32_t	rx_mb_config	Number and size of RX Message Buffers (CFDRMNB register setting)
uint8_t	global_err_ipl	Global Error interrupt priority.
uint8_t	rx_fifo_ipl	RX FIFO interrupt priority.

#### ◆ canfd\_extended\_cfg\_t

struct canfd_extended_cfg_t		
CANFD Extended Configuration		
Data Fields		
canfd_afl_entry_t const *	p_afl	AFL rules list.
uint64_t	txmb_txi_enable	Array of TX Message Buffer enable bits.
uint32_t	error_interrupts	Error interrupt enable bits.
can_bit_timing_cfg_t *	p_data_timing	FD Data Rate (when bitrate switching is used)
uint8_t	delay_compensation	FD Transceiver Delay Compensation (enable or disable)
canfd_global_cfg_t *	p_global_cfg	Global configuration (global error callback channel only)

## Enumeration Type Documentation

◆ **canfd\_status\_t**

enum <code>canfd_status_t</code>	
CANFD Status	
Enumerator	
<code>CANFD_STATUS_RESET_MODE</code>	Channel in Reset mode.
<code>CANFD_STATUS_HALT_MODE</code>	Channel in Halt mode.
<code>CANFD_STATUS_SLEEP_MODE</code>	Channel in Sleep mode.
<code>CANFD_STATUS_ERROR_PASSIVE</code>	Channel in error-passive state.
<code>CANFD_STATUS_BUS_OFF</code>	Channel in bus-off state.
<code>CANFD_STATUS_TRANSMITTING</code>	Channel is transmitting.
<code>CANFD_STATUS_RECEIVING</code>	Channel is receiving.
<code>CANFD_STATUS_READY</code>	Channel is ready for communication.
<code>CANFD_STATUS_ESI</code>	At least one CAN-FD message was received with the ESI flag set.

◆ **canfd\_error\_t**

enum <code>canfd_error_t</code>	
CANFD Error Code	
Enumerator	
<code>CANFD_ERROR_CHANNEL_BUS</code>	Bus Error.
<code>CANFD_ERROR_CHANNEL_WARNING</code>	Error Warning (TX/RX error count over 0x5F)
<code>CANFD_ERROR_CHANNEL_PASSIVE</code>	Error Passive (TX/RX error count over 0x7F)
<code>CANFD_ERROR_CHANNEL_BUS_OFF_ENTRY</code>	Bus-Off State Entry.
<code>CANFD_ERROR_CHANNEL_BUS_OFF_RECOVERY</code>	Recovery from Bus-Off State.
<code>CANFD_ERROR_CHANNEL_OVERLOAD</code>	Overload.
<code>CANFD_ERROR_CHANNEL_BUS_LOCK</code>	Bus Locked.
<code>CANFD_ERROR_CHANNEL_ARBITRATION_LOSS</code>	Arbitration Lost.

CANFD_ERROR_CHANNEL_STUFF	Stuff Error.
CANFD_ERROR_CHANNEL_FORM	Form Error.
CANFD_ERROR_CHANNEL_ACK	ACK Error.
CANFD_ERROR_CHANNEL_CRC	CRC Error.
CANFD_ERROR_CHANNEL_BIT_RECESSIVE	Bit Error (recessive) Error.
CANFD_ERROR_CHANNEL_BIT_DOMINANT	Bit Error (dominant) Error.
CANFD_ERROR_CHANNEL_ACK_DELIMITER	ACK Delimiter Error.
CANFD_ERROR_GLOBAL_DLC	DLC Error.
CANFD_ERROR_GLOBAL_MESSAGE_LOST	Message Lost.
CANFD_ERROR_GLOBAL_PAYLOAD_OVERFLOW	FD Payload Overflow.
CANFD_ERROR_GLOBAL_TXQ_OVERWRITE	TX Queue Message Overwrite.
CANFD_ERROR_GLOBAL_TXQ_MESSAGE_LOST	TX Queue Message Lost.
CANFD_ERROR_GLOBAL_CH0_SCAN_FAIL	Channel 0 RX Scan Failure.
CANFD_ERROR_GLOBAL_CH1_SCAN_FAIL	Channel 1 RX Scan Failure.
CANFD_ERROR_GLOBAL_CH0_ECC	Channel 0 ECC Error.
CANFD_ERROR_GLOBAL_CH1_ECC	Channel 1 ECC Error.

#### ◆ canfd\_tx\_mb\_t

enum <a href="#">canfd_tx_mb_t</a>
CANFD Transmit Message Buffer (TX MB)

#### ◆ canfd\_rx\_buffer\_t

enum <a href="#">canfd_rx_buffer_t</a>
CANFD Receive Buffer (MB + FIFO)

◆ **canfd\_rx\_mb\_t**

enum <a href="#">canfd_rx_mb_t</a>
CANFD Receive Message Buffer (RX MB)

◆ **canfd\_rx\_fifo\_t**

enum <a href="#">canfd_rx_fifo_t</a>
CANFD Receive FIFO (RX FIFO)

◆ **canfd\_minimum\_dlc\_t**

enum <a href="#">canfd_minimum_dlc_t</a>
CANFD AFL Minimum DLC settings

◆ **canfd\_frame\_options\_t**

enum <a href="#">canfd_frame_options_t</a>	
CANFD Frame Options	
Enumerator	
CANFD_FRAME_OPTION_ERROR	Error state set (ESI).
CANFD_FRAME_OPTION_BRS	Bit Rate Switching (BRS) enabled.
CANFD_FRAME_OPTION_FD	Flexible Data frame (FDF).

**Function Documentation**

◆ **R\_CANFD\_Open()**

```
fsp_err_t R_CANFD_Open ( can_ctrl_t *const p_api_ctrl, can_cfg_t const *const p_cfg )
```

Open and configure the CANFD channel for operation.

Example:

```
/* Initialize the CAN module */
err = R_CANFD_Open(&g_canfd0_ctrl, &g_canfd0_cfg);
```

**Return values**

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ALREADY_OPEN	Driver already open.
FSP_ERR_IN_USE	Channel is already in use.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel does not exist on this MCU.
FSP_ERR_ASSERTION	A required pointer was NULL.
FSP_ERR_CAN_INIT_FAILED	The provided nominal or data bitrate is invalid.
FSP_ERR_CLOCK_INACTIVE	CANFD source clock is disabled (PLL or PLL2).

◆ **R\_CANFD\_Close()**

```
fsp_err_t R_CANFD_Close ( can_ctrl_t *const p_api_ctrl)
```

Close the CANFD channel.

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented.

◆ **R\_CANFD\_Write()**

```
fsp_err_t R_CANFD_Write ( can_ctrl_t*const p_api_ctrl, uint32_t buffer, can_frame_t*const p_frame )
```

Write data to the CANFD channel.

Example:

```
/* Send data on the bus */
err = R_CANFD_Write(&g_canfd0_ctrl, CANFD_TX_MB_0, &g_can_tx_frame);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_CAN_TRANSMIT_NOT_READY	Transmit in progress, cannot write data at this time.
FSP_ERR_INVALID_ARGUMENT	Data length or buffer number invalid.
FSP_ERR_INVALID_MODE	An FD option was set on a non-FD frame.
FSP_ERR_ASSERTION	Null pointer presented

◆ **R\_CANFD\_Read()**

```
fsp_err_t R_CANFD_Read ( can_ctrl_t*const p_api_ctrl, uint32_t buffer, can_frame_t*const p_frame )
```

Read data from a CANFD Message Buffer or FIFO.

Example: snippet r\_canfd\_example.c R\_CANFD\_Read

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_ARGUMENT	Buffer number invalid.
FSP_ERR_ASSERTION	p_api_ctrl or p_frame is NULL.
FSP_ERR_BUFFER_EMPTY	Buffer or FIFO is empty.

◆ **R\_CANFD\_ModeTransition()**

```
fsp_err_t R_CANFD_ModeTransition ( can_ctrl_t *const p_api_ctrl, can_operation_mode_t
operation_mode, can_test_mode_t test_mode )
```

Switch to a different channel, global or test mode.

Example:

```
/* Switch to external loopback mode */
err = R_CANFD_ModeTransition(&g_canfd0_ctrl, CAN_OPERATION_MODE_NORMAL,
CAN_TEST_MODE_LOOPBACK_EXTERNAL);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented
FSP_ERR_INVALID_MODE	Cannot change to the requested mode from the current global mode.

◆ **R\_CANFD\_InfoGet()**

```
fsp_err_t R_CANFD_InfoGet ( can_ctrl_t *const p_api_ctrl, can_info_t *const p_info )
```

Get CANFD state and status information for the channel.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	Null pointer presented

### ◆ R\_CANFD\_CallbackSet()

```
fsp_err_t R_CANFD_CallbackSet ( can_ctrl_t *const p_api_ctrl, void(*) (can_callback_args_t *)
p_callback, void const *const p_context, can_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `can_api_t::callbackSet`.

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.9 Consumer Electronics Control (r\_cec)

### Modules

#### Functions

```
fsp_err_t R_CEC_Open (cec_ctrl_t *const p_ctrl, cec_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CEC_MediaInit (cec_ctrl_t *const p_ctrl, cec_addr_t local_address)
```

```
fsp_err_t R_CEC_Close (cec_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CEC_Write (cec_ctrl_t *const p_ctrl, cec_message_t const *const
p_message, uint32_t message_size)
```

```
fsp_err_t R_CEC_StatusGet (cec_ctrl_t *const p_ctrl, cec_status_t *const
p_status)
```

```
fsp_err_t R_CEC_CallbackSet (cec_ctrl_t *const p_ctrl,
void(*p_callback)(cec_callback_args_t *), void const *const
p_context, cec_callback_args_t *const p_callback_memory)
```

#### Detailed Description

Driver for the CEC peripheral on RA MCUs. This module implements the [CEC Interface](#).

## Overview

The HDMI CEC HAL module provides a high-level API for CEC applications and supports the CEC peripheral available on RA microcontroller hardware. A user-callback function must be defined that the driver will invoke when data received, transmission complete, or error interrupts are received. The callback is passed a parameter which indicates the event as well as received data (if available).

## Features

- Conforms to High Definition Multimedia Interface (HDMI) Consumer Electronics Control (CEC) standard Ver. 1.4b.
- Full range of local address settings (TV, Recording Device, Playback Device, etc.)
- Data filtering based on matching destination address and local address.
- Supports a user-callback function (required), invoked when transmit, receive, or error interrupts are received.

## Configuration

### Build Time Configurations for r\_cec

The following build time configurations are defined in fsp\_cfg/r\_cec\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
CEC Message Max Data Size	Manual Entry	14	Maximum Data Size for CEC Message Transmission/Reception.

### Configurations for Driver > Connectivity > CEC Driver on r\_cec

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > CEC Driver on r\_cec. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_cec0	Module name
General > Callback Function	Manual Entry	g_rm_cec0_callback	Callback function
Control Configuration > Clock Select	<ul style="list-style-type: none"> <li>• PCLKB / 32</li> <li>• PCLKB / 64</li> <li>• PCLKB / 128</li> <li>• PCLKB / 256</li> <li>• PCLKB / 512</li> <li>• PCLKB / 1024</li> </ul>	PCLKB / 1024	CEC Clock Select Configuration
Control Configuration > Ack Bit Timing Error Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	CEC Ack Bit Timing Error Enable

Control Configuration > Signal-Free Time Bit Width	<ul style="list-style-type: none"> <li>• 3-data bit width</li> <li>• 5-data bit width</li> <li>• 7-data bit width</li> <li>• Does not detect signal-free time.</li> </ul>	7-data bit width	Signal-Free Time Data Bit Width Select
Control Configuration > Start Bit Error Detection Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Enable to detect timing errors during start bit reception.
Control Configuration > Bus Lock Detection Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Enable to detect sticking of receive data to high or low.
Control Configuration > Digital Filter Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Enable to use a digital filter.
Control Configuration > Long Bit Width Error Pulse Output Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable to output an error handling pulse when a long bit width error is detected.
Control Configuration > Start Detection Reception Restart Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Enable to restart reception after a start bit error is detected.
Bit Width Timing > Transmit > Start Bit Low Time	CEC transmission start bit low width setting must be a positive integer.	180	CEC transmission start bit low width setting (CEC Clock Cycles).
Bit Width Timing > Transmit > Start Bit High Time	CEC transmission start bit high width setting must be a positive integer.	220	CEC transmission start bit high width setting (CEC Clock Cycles).
Bit Width Timing > Transmit > Logical Zero Low Time	CEC transmission logical zero low width setting must be a positive integer.	73	CEC transmission logical zero low width setting (CEC Clock Cycles).
Bit Width Timing > Transmit > Logical One Low Time	CEC transmission logical one low width setting must be a positive integer.	29	CEC transmission logical one low width setting (CEC Clock Cycles).
Bit Width Timing > Transmit > Overall Bit Width Time	CEC transmission overall data bit width time setting must be a positive integer.	117	CEC transmission overall data bit width time setting (CEC Clock Cycles).
Bit Width Timing > Receive > Data Sample Time	CEC reception data sampling time must be a positive integer.	49	CEC reception data sampling time setting (CEC Clock Cycles).
Bit Width Timing > Receive > Data Bit	CEC reception data sampling time must be	117	CEC data bit reference width setting (CEC

Reference Width	a positive integer.		Clock Cycles).
Bit Width Timing > Receive > Start Bit Low Min Time	CEC reception start bit minimum low width setting must be a positive integer.	171	CEC reception start bit minimum low width setting (CEC Clock Cycles). Not used when Start Bit Error Detection and restart Rx on Error are not enabled.
Bit Width Timing > Receive > Start Bit Low Max Time	CEC reception start bit maximum low width setting must be a positive integer.	190	CEC reception start bit maximum low width setting (CEC Clock Cycles). Not used when Start Bit Error Detection and restart Rx on Error are not enabled.
Bit Width Timing > Receive > Start Bit Min Time	CEC start bit minimum time setting must be a positive integer.	210	CEC start bit minimum time setting (CEC Clock Cycles). Not used when Start Bit Error Detection and restart Rx on Error are not enabled.
Bit Width Timing > Receive > Start Bit Max Time	CEC reception start bit maximum time setting must be a positive integer.	229	CEC start bit maximum time setting (CEC Clock Cycles). Not used when Start Bit Error Detection and restart Rx on Error are not enabled.
Bit Width Timing > Receive > Logical Zero Low Min Time	CEC reception logical zero minimum low width setting must be a positive integer.	64	CEC reception logical zero minimum low width setting (CEC Clock Cycles).
Bit Width Timing > Receive > Logical Zero Low Max Time	CEC reception logical zero maximum low width setting must be a positive integer.	83	CEC reception logical zero maximum low width setting (CEC Clock Cycles).
Bit Width Timing > Receive > Logical One Low Min Time	CEC reception logical one minimum low width setting must be a positive integer.	20	CEC reception logical one minimum low width setting (CEC Clock Cycles).
Bit Width Timing > Receive > Logical One Low Max Time	CEC reception logical one maximum low width setting must be a positive integer.	39	CEC reception logical one maximum low width (CEC Clock Cycles).
Bit Width Timing > Receive > Overall Bit	CEC reception overall minimum bit width	100	CEC reception overall minimum bit width

Width Min Time	setting must be a positive integer.		setting (CEC Clock Cycles).
Bit Width Timing > Receive > Overall Bit Width Max Time	CEC reception overall maximum bit width setting must be a positive integer.	134	CEC reception overall maximum bit width setting (CEC Clock Cycles).
Interrupts > Interrupt Priority Level	MCU Specific Options		Error/Data/Message interrupt priority level.
Interrupts > Communication Complete Interrupt Timing	<ul style="list-style-type: none"> <li>• After Last Frame and Signal Free Time</li> <li>• After Last Frame</li> <li>• After Signal Free Time</li> </ul>	After Last Frame and Signal Free Time	Communication Complete Interrupt (INTCE) Generation Timing Select
Interrupts > Address Mismatch Interrupt Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable to generate an interrupt when the addresses do not match.
Interrupts > Data Interrupt Timing Selection	<ul style="list-style-type: none"> <li>• EOM timing (9th bit of data)</li> <li>• ACK Timing (10th bit of data)</li> </ul>	EOM timing (9th bit of data)	INTDA reception interrupt timing selection (EOM or ACK).

## Clock Configuration

The CEC peripheral uses the CECCLK or PCLKB as its clock source. To set the PCLKB frequency, use the Clocks tab of the RA Configuration editor.

### Note

*The selected clock and configured divider must be configured in the range of 23.4375 to 78.125 kHz.*

## Pin Configuration

A CEC channel uses one data pin - CECIO for data transmission and reception.

The output type for each pin should be set to **n-ch open drain** for most hardware designs. This can be configured in **Pins** tab of the RA Configuration editor by selecting the pin under Pin Selection->Ports.

## Usage Notes

### CEC Device Addresses

The CEC standard provides 13 device addresses that may be requested based on a device's primary function. Use R\_CEC\_Medialnit to request a specific address before starting communication with other devices.

### Note

*Address 0 is always the primary display (TV). Do not attempt to allocate this address unless your device is intended to function as a display.*

## Limitations

Developers should be aware of the following limitations when using the CEC module:

- R\_CEC\_MediaInit may return FSP\_ERR\_IN\_USE for up to 45 milliseconds after R\_CEC\_Open while the hardware initializes.
- The CECIO pin must be set to n-ch open drain mode.

## Examples

### Basic Example

This is a basic example of minimal use of the CEC in an application.

```

/*****
*****
 * Application defined callback
 * - May be assigned at compile-time via the e2 Studio configuration tool or set at
run-time via R_CEC_CallbackSet()
*****
*****/
void cec_callback (cec_callback_args_t * p_args)
{
    switch (p_args->event)
    {
        case CEC_EVENT_READY:
            {
                /* Application processing for address allocation success. */
                break;
            }
        case CEC_EVENT_TX_COMPLETE:
            {
                /* Any required processing after transmission has completed. */
                break;
            }
        case CEC_EVENT_ERR:
            {

```

```
/* Error processing. See cec_error_t for possible errors. */
break;
    }

case CEC_EVENT_RX_DATA:
    {
/* Application to store and process received data bytes. */
break;
    }

case CEC_EVENT_RX_COMPLETE:
    {
/* Application processing for message reception complete. */
    }
}

/*****
*****

* Basic example
*****
*****/

#define CEC_TIMEOUT_MS (50)
#define CEC_MSG_STANDBY (0X36) /* See CEC Specification for message definitions */
void basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

/* Open the CEC module */
    err = R_CEC_Open(&g_cec0_ctrl, &g_cec0_cfg);
    assert(FSP_SUCCESS == err);

/* Initialize the CEC module and allocate an address */
    uint32_t timeout_ms = CEC_TIMEOUT_MS;

do
    {
/* R_CEC_MediaInit may return FSP_ERR_IN_USE for up to 45 milliseconds after calling
R_CEC_Open */
        err = R_CEC_MediaInit(&g_cec0_ctrl, CEC_ADDR_TV);
```

```
R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_MILLISECONDS);
} while ((FSP_ERR_IN_USE == err) && --timeout_ms);
assert(timeout_ms);
assert(FSP_SUCCESS == err);
/* Wait for local address allocation and CEC bus to be free */
cec_status_t status;
err = R_CEC_StatusGet(&g_cec0_ctrl, &status);
while ((FSP_SUCCESS == err) && (CEC_STATE_READY != status.state))
{
    err = R_CEC_StatusGet(&g_cec0_ctrl, &status);
    assert(FSP_SUCCESS == err);
}
cec_message_t cec_msg;
uint8_t      total_transmit_size;
cec_msg.destination = CEC_ADDR_BROADCAST;      /* For this example, send message
to all devices on the bus */
cec_msg.opcode      = CEC_MSG_STANDBY;        /* Send Standby Request */
memset(cec_msg.data, 0U, sizeof(cec_msg.data)); /* See CEC Specification for
other message data structures */
total_transmit_size = 2U;                      /* Total message size, including
header, opcode, and data */
/* Send asynchronous message.
* - Application will then be free for other processing while message is being sent.
* - Do not modify the message buffer until transmission has completed. */
err = R_CEC_Write(&g_cec0_ctrl, &cec_msg, total_transmit_size);
assert(FSP_SUCCESS == err);
}
```

## Function Documentation

---

**◆ R\_CEC\_Open()**

```
fsp_err_t R_CEC_Open ( cec_ctrl_t *const p_ctrl, cec_cfg_t const *const p_cfg )
```

Open and configure the CEC module for operation.

Example:

```
/* Open the CEC module */  
err = R_CEC_Open(&g_cec0_ctrl, &g_cec0_cfg);  
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	CEC Module opened successfully.
FSP_ERR_ALREADY_OPEN	Driver already open.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_IRQ_BSP_DISABLED	Interrupts are not enabled.

◆ **R\_CEC\_MediaInit()**

```
fsp_err_t R_CEC_MediaInit ( cec_ctrl_t*const p_ctrl, cec_addr_t local_address )
```

Allocate provided CEC Local Address and Initialize the CEC module for operation.

**Note**

*After calling R\_CEC\_Open this function may return FSP\_ERR\_IN\_USE for up to 45 milliseconds.*

**Example:**

```
/* Initialize the CEC module and allocate an address */
uint32_t timeout_ms = CEC_TIMEOUT_MS;
do
{
/* R_CEC_MediaInit may return FSP_ERR_IN_USE for up to 45 milliseconds after calling
R_CEC_Open */
err = R_CEC_MediaInit(&g_cec0_ctrl, CEC_ADDR_TV);
R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_MILLISECONDS);
} while ((FSP_ERR_IN_USE == err) && --timeout_ms);
assert(timeout_ms);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	CEC Module Initialized successfully.
FSP_ERR_ASSERTION	An input argument is invalid or callback has not been set.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_IN_USE	HDMI CEC Bus is currently in use. Try again later.

◆ **R\_CEC\_Close()**

```
fsp_err_t R_CEC_Close ( cec_ctrl_t*const p_ctrl)
```

Close the CEC module.

**Return values**

FSP_SUCCESS	CEC Module closed successfully.
FSP_ERR_ASSERTION	An input argument is invalid.

## ◆ R\_CEC\_Write()

```
fsp_err_t R_CEC_Write ( cec_ctrl_t *const p_ctrl, cec_message_t const *const p_message, uint32_t message_size )
```

Write data to the CEC bus. Data transmission is asynchronous. Provided message buffer should not be modified until transmission is complete.

Data Transmission follows the pattern defined by the HDMI CEC Specification:

Data	Description	Size
Start Bit	Managed by Hardware, per config	N/A
Header Block	Source/Destination Identifier	1 Byte
Data Block 1	Opcode Value (Optional)	1 Byte
Data Block 2	Operands (Optional)	Variable (0-14 Bytes Typical)

Example:

```
cec_message_t cec_msg;

uint8_t      total_transmit_size;

cec_msg.destination = CEC_ADDR_BROADCAST;          /* For this example, send message
to all devices on the bus */

cec_msg.opcode      = CEC_MSG_STANDBY;            /* Send Standby Request */

memset(cec_msg.data, 0U, sizeof(cec_msg.data)); /* See CEC Specification for
other message data structures */

total_transmit_size = 2U;                          /* Total message size, including
header, opcode, and data */

/* Send asynchronous message.
* - Application will then be free for other processing while message is being sent.
* - Do not modify the message buffer until transmission has completed. */

err = R_CEC_Write(&g_cec0_ctrl, &cec_msg, total_transmit_size);
assert(FSP_SUCCESS == err);
```

## Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_NOT_INITIALIZED	Module has not been successfully initialized.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_INVALID_SIZE	Invalid message size.
FSP_ERR_IN_USE	HDMI CEC Bus is currently in use. Try again

later.

◆ **R\_CEC\_StatusGet()**

```
fsp_err_t R_CEC_StatusGet ( cec_ctrl_t *const p_ctrl, cec_status_t *const p_status )
```

Provides the state and status information according to the provided CEC control instance.

**Return values**

FSP_SUCCESS	Operation succeeded.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_ASSERTION	An input argument is invalid.

◆ **R\_CEC\_CallbackSet()**

```
fsp_err_t R_CEC_CallbackSet ( cec_ctrl_t *const p_ctrl, void(*) (cec_callback_args_t *) p_callback, void const *const p_context, cec_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `cec_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.10 Clock Generation Circuit (r\_cgc)**

## Modules

**Functions**

```
fsp_err_t R_CGC_Open (cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CGC_ClocksCfg (cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg)
```

```
fsp_err_t R_CGC_ClockStart (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source,
```

	<code>cgc_pll_cfg_t</code>	<code>const *const p_pll_cfg)</code>
<code>fsp_err_t</code>	<code>R_CGC_ClockStop</code>	<code>(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)</code>
<code>fsp_err_t</code>	<code>R_CGC_ClockCheck</code>	<code>(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)</code>
<code>fsp_err_t</code>	<code>R_CGC_SystemClockSet</code>	<code>(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)</code>
<code>fsp_err_t</code>	<code>R_CGC_SystemClockGet</code>	<code>(cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source, cgc_divider_cfg_t *const p_divider_cfg)</code>
<code>fsp_err_t</code>	<code>R_CGC_OscStopDetectEnable</code>	<code>(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t</code>	<code>R_CGC_OscStopDetectDisable</code>	<code>(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t</code>	<code>R_CGC_OscStopStatusClear</code>	<code>(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t</code>	<code>R_CGC_CallbackSet</code>	<code>(cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t</code>	<code>R_CGC_Close</code>	<code>(cgc_ctrl_t *const p_ctrl)</code>

## Detailed Description

Driver for the CGC peripheral on RA MCUs. This module implements the [CGC Interface](#).

### Note

***This module is not required for the initial clock configuration. Initial clock settings are configurable on the **Clocks** tab of the RA Configuration editor. The initial clock settings are applied by the BSP during the startup process before main.***

## Overview

### Features

The CGC module supports runtime modifications of clock settings. Key features include the following:

- Supports changing the system clock source to any of the following options (provided they are supported on the MCU):
  - High-speed on-chip oscillator (HOCO)
  - Middle-speed on-chip oscillator (MOCO)
  - Low-speed on-chip oscillator (LOCO)
  - Main oscillator (external resonator or external clock input frequency)
  - Sub-clock oscillator (external resonator)
  - PLL/PLL2 (not available on all MCUs)
- When the system core clock frequency changes, the following things are updated:
  - The CMSIS standard global variable `SystemCoreClock` is updated to reflect the new clock frequency.

- Wait states for ROM and RAM are adjusted to the minimum supported value for the new clock frequency.
- The operating power control mode is updated to the minimum supported value for the new clock settings.
- Supports starting or stopping any of the system clock sources
- Supports changing dividers for the internal clocks
- Supports the oscillation stop detection feature

## Internal Clocks

The RA microcontrollers have up to seven internal clocks. Not all internal clocks exist on all MCUs. Each clock domain has its own divider that can be updated in `R_CGC_SystemClockSet()`. The dividers are subject to constraints described in the footnote of the table "Specifications of the Clock Generation Circuit for the internal clocks" in the hardware manual.

The internal clocks include:

- System clock (ICLK): core clock used for CPU, flash, internal SRAM, DTC, and DMAC
- PCLKA/PCLKB/PCLKC/PCLKD: Peripheral clocks, refer to the table "Specifications of the Clock Generation Circuit for the internal clocks" in the hardware manual to see which peripherals are controlled by which clocks.
- FCLK: Clock source for reading data flash and for programming/erasure of both code and data flash.
- BCLK: External bus clock

## Configuration

### Note

*The initial clock settings are configurable on the **Clocks** tab of the RA Configuration editor.*

*There is a configuration to enable the HOCO on reset in the OFS1 settings on the BSP tab.*

*The following clock related settings are configurable in the RA Common section on the BSP tab:*

- Main Oscillator Wait Time
- Main Oscillator Clock Source (external oscillator or crystal/resonator)
- Subclock Populated
- Subclock Drive
- Subclock Stabilization Time (ms)

*The default stabilization times are determined based on development boards provided by Renesas, but are generally valid for most designs. Depending on the target board hardware configuration and requirements these values may need to be adjusted for reliability or startup speed.*

### Build Time Configurations for r\_cgc

The following build time configurations are defined in `fsp_cfg/r_cgc_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > System > CGC Driver on r\_cgc

This module can be added to the Stacks tab via New Stack > Driver > System > CGC Driver on r\_cgc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_cgc0	Module name.
NMI Callback	Name must be a valid C symbol	NULL	A user callback function must be provided if oscillation stop detection is used. If this callback function is provided, it is called from the NMI handler if the main oscillator stops.

## Clock Configuration

This module is used to configure the system clocks. There are no module specific clock configurations required to use it.

## Pin Configuration

The CGC module controls the output of the CLOCKOUT signal.

If an external oscillator is used the XTAL and EXTAL pins must be configured accordingly. When running from an on chip oscillator there is no requirement for the main clock external oscillator. In this case, the XTAL and EXTAL pins can be set to a different function in the RA Configuration editor.

The functionality of the subclock external oscillator pins XCIN and XCOU is fixed.

## Usage Notes

### NMI Interrupt

The CGC timer uses the NMI for oscillation stop detection of the main oscillator after `R_CGC_OscStopDetectEnable` is called. The NMI is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during `R_CGC_Open()` is called.

### Starting or Stopping the Subclock

If the Subclock Populated property is set to Populated on the BSP configuration tab, then the subclock is started in the BSP startup routine. Otherwise, it is stopped in the BSP startup routine. Starting and stopping the subclock at runtime is not recommended since the stabilization requirements typically negate the negligible power savings.

The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

### Warning

The subclock can take up to several seconds to stabilize. RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. In this case the default wait time is 1000ms (1 second). When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation. Because there is no hardware stabilization status bit for the subclock `R_CGC_ClockCheck` cannot be used to optimize this wait.

Changing the subclock state during `R_CGC_ClocksCfg()` is not supported.

## Low Power Operation

If "Use Low Voltage Mode" is enabled in the BSP MCU specific properties (not available on all MCUs), the MCU is always in low voltage mode and no other power modes are considered. The following conditions must be met for the MCU to run in low voltage mode:

- Requires HOCO to be running, so HOCO cannot be stopped in low voltage mode
- Requires PLL to be stopped, so PLL APIs are not available in low voltage mode
- Requires ICLK  $\leq$  4 MHz
- If oscillation stop detection is used, dividers of 1 or 2 cannot be used for any clock

If "Use Low Voltage Mode" is not enabled, the MCU applies the lowest power mode by searching through the following list in order and applying the first power mode that is supported under the current conditions:

- Subosc-speed mode (lowest power)
  - Requires system clock to be LOCO or subclock
  - Requires MOCO, HOCO, main oscillator, and PLL (if present) to be stopped
  - Requires ICLK and FCLK dividers to be 1
- Low-speed mode
  - Requires PLL to be stopped
  - Requires ICLK  $\leq$  1 MHz
  - If oscillation stop detection is used, dividers of 1, 2, 4, or 8 cannot be used for any clock
- Middle-speed mode (not supported on all MCUs)
  - Requires ICLK  $\leq$  8 MHz
- High-speed mode
  - Default mode if no other operating mode is supported

Refer to the section "Function for Lower Operating Power Consumption" in the "Low Power Modes" chapter of the hardware manual for MCU specific information about operating power control modes.

### Note

*The DCDC regulator (if present) is only available in Middle- and High-speed modes. The BSP will automatically switch between DCDC and LDO when switching between compatible and incompatible modes if the DCDC regulator is in use. Switching to the LDO incurs a 60 microsecond critical section wherein all interrupts AND peripherals are stopped. Switching back to DCDC from the LDO incurs an additional 22 microsecond critical section (peripherals running).*

When low voltage mode is not used, the following functions adjust the operating power control mode to ensure it remains within the hardware specification and to ensure the MCU is running at the optimal operating power control mode:

- `R_CGC_ClockStart()`
- `R_CGC_ClockStop()`
- `R_CGC_SystemClockSet()`
- `R_CGC_OscStopDetectEnable()`
- `R_CGC_OscStopDetectDisable()`

### Note

*FSP APIs, including these APIs, are not thread safe. These APIs and any other user code that modifies the operating power control mode must not be allowed to interrupt each other. Proper care must be taken during application design if these APIs are used in threads or interrupts to ensure this constraint is met.*

No action is required by the user of these APIs. This section is provided for informational purposes only.

## Examples

### Basic Example

This is a basic example of minimal use of the CGC in an application.

```
void cgc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the CGC module. */
    err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Change the system clock to LOCO for power saving. */
    /* Start the LOCO. */
    err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_LOCO, NULL);
    assert(FSP_SUCCESS == err);
    /* Wait for the LOCO stabilization wait time.
     *
     * NOTE: The MOCO, LOCO and subclock do not have stabilization status bits, so any
    stabilization time must be
     * performed via a software wait when starting these oscillators. For all other
    oscillators, R_CGC_ClockCheck can
     * be used to verify stabilization status.
     */
    R_BSP_SoftwareDelay(BSP_FEATURE_CGC_LOCO_STABILIZATION_MAX_US,
    BSP_DELAY_UNITS_MICROSECONDS);
    /* Set divisors. Divisors for clocks that don't exist on the MCU are ignored. */
    cgc_divider_cfg_t dividers =
    {
        /* PCLKB is not used in this application, so select the maximum divisor for lowest
    power. */
        .pclk_div = CGC_SYS_CLOCK_DIV_64,
        /* PCLKD is not used in this application, so select the maximum divisor for lowest
```

```
power. */
    .pclkd_div = CGC_SYS_CLOCK_DIV_64,
/* ICLK is the MCU clock, allow it to run as fast as the LOCO is capable. */
    .iclk_div = CGC_SYS_CLOCK_DIV_1,
/* These clocks do not exist on some devices. If any clocks don't exist, set the
divider to 1. */
    .pclka_div = CGC_SYS_CLOCK_DIV_1,
    .pclkc_div = CGC_SYS_CLOCK_DIV_1,
    .fclk_div = CGC_SYS_CLOCK_DIV_1,
    .bclk_div = CGC_SYS_CLOCK_DIV_1,
};
/* Switch the system clock to LOCO. */
err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_LOCO, &dividers);
assert(FSP_SUCCESS == err);
}
```

## Configuring Multiple Clocks

This example demonstrates switching to a new source clock and stopping the previous source clock in a single function call using [R\\_CGC\\_ClocksCfg\(\)](#).

```
void cgc_clocks_cfg_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
/* Initializes the CGC module. */
    err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
/* Change the system clock to PLL running from the main oscillator. */
/* Assuming the system clock is MOCO, switch to HOCO. */
    cgc_clocks_cfg_t clocks_cfg;
    clocks_cfg.system_clock          = CGC_CLOCK_PLL;
    clocks_cfg.pll_state             = CGC_CLOCK_CHANGE_NONE;
    clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC; // unused
    clocks_cfg.pll_cfg.multiplier   = CGC_PLL_MUL_10_0;   // unused
}
```

```
clocks_cfg.pll_cfg.divider      = CGC_PLL_DIV_2;          // unused
clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;
clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.mainosc_state       = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.hoco_state          = CGC_CLOCK_CHANGE_START;
clocks_cfg.moco_state          = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.loco_state          = CGC_CLOCK_CHANGE_NONE;

err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
assert(FSP_SUCCESS == err);

#if BSP_FEATURE_CGC_HAS_PLL
/* Assuming the system clock is HOCO, switch to PLL running from main oscillator and
stop MOCO. */
clocks_cfg.system_clock        = CGC_CLOCK_PLL;
clocks_cfg.pll_state           = CGC_CLOCK_CHANGE_START;
clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC;
clocks_cfg.pll_cfg.multiplier   = (cgc_pll_mul_t) BSP_CFG_PLL_MUL;
clocks_cfg.pll_cfg.divider      = (cgc_pll_div_t) BSP_CFG_PLL_DIV;
clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;
clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.mainosc_state       = CGC_CLOCK_CHANGE_START;
clocks_cfg.hoco_state          = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.moco_state          = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.loco_state          = CGC_CLOCK_CHANGE_NONE;

err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
```

```
    assert(FSP_SUCCESS == err);
#endif
}
```

## Oscillation Stop Detection

This example demonstrates registering a callback for oscillation stop detection of the main oscillator.

```
/* Example callback called when oscillation stop is detected. */
void oscillation_stop_callback (cgc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    fsp_err_t err = FSP_SUCCESS;

    /* (Optional) If the MCU was running on the main oscillator, the MCU is now running
on MOCO. Switch clocks if
    * desired. This example shows switching to HOCO. */
    err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_HOCO, NULL);
    assert(FSP_SUCCESS == err);

    do
    {
        /* Wait for HOCO to stabilize. */
        err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_HOCO);
    } while (FSP_SUCCESS != err);

    cgc_divider_cfg_t dividers =
    {
        .pclk_div = CGC_SYS_CLOCK_DIV_4,
        .pclkd_div = CGC_SYS_CLOCK_DIV_4,
        .iclk_div = CGC_SYS_CLOCK_DIV_1,
        .pclka_div = CGC_SYS_CLOCK_DIV_4,
        .pclkc_div = CGC_SYS_CLOCK_DIV_4,
        .fclk_div = CGC_SYS_CLOCK_DIV_4,
        .bclk_div = CGC_SYS_CLOCK_DIV_4,
    };

    err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_HOCO, &dividers);
    assert(FSP_SUCCESS == err);
}
```

```
#if BSP_FEATURE_CGC_HAS_PLL
/* (Optional) If the MCU was running on the PLL, the PLL is now in free-running
mode. Switch clocks if
* desired. This example shows switching to the PLL running on HOCO. */
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_HOCO, NULL);
assert(FSP_SUCCESS == err);
do
{
/* Wait for HOCO to stabilize. */
err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_HOCO);
} while (FSP_SUCCESS != err);
cgc_pll_cfg_t pll_cfg =
{
.source_clock = CGC_CLOCK_HOCO,
.multiplier   = (cgc_pll_mul_t) BSP_CFG_PLL_MUL,
.divider      = (cgc_pll_div_t) BSP_CFG_PLL_DIV,
};
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_PLL, &pll_cfg);
assert(FSP_SUCCESS == err);
do
{
/* Wait for PLL to stabilize. */
err = R_CGC_ClockCheck(&g_cgc0_ctrl, CGC_CLOCK_PLL);
} while (FSP_SUCCESS != err);
cgc_divider_cfg_t pll_dividers =
{
.pclkb_div = CGC_SYS_CLOCK_DIV_4,
.pclkd_div = CGC_SYS_CLOCK_DIV_4,
.iclk_div  = CGC_SYS_CLOCK_DIV_1,
.pclka_div = CGC_SYS_CLOCK_DIV_4,
.pclkc_div = CGC_SYS_CLOCK_DIV_4,
.fclk_div  = CGC_SYS_CLOCK_DIV_4,
.bclk_div  = CGC_SYS_CLOCK_DIV_4,
};
};
```

```
err = R_CGC_SystemClockSet(&g_cgc0_ctrl, CGC_CLOCK_PLL, &pll_dividers);
assert(FSP_SUCCESS == err);
#endif

/* (Optional) Clear the error flag. Only clear this flag after switching the MCU
clock source away from the main
* oscillator and if the main oscillator is stable again. */
err = R_CGC_OscStopStatusClear(&g_cgc0_ctrl);
assert(FSP_SUCCESS == err);
}

void cgc_osc_stop_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Open the module. */
    err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable oscillation stop detection. The main oscillator must be running at this
point. */
    err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
    assert(FSP_SUCCESS == err);
    /* (Optional) Oscillation stop detection must be disabled before entering any low
power mode. */
    err = R_CGC_OscStopDetectDisable(&g_cgc0_ctrl);
    assert(FSP_SUCCESS == err);
    __WFI();
    /* (Optional) Reenable oscillation stop detection after waking from low power mode.
*/
    err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
    assert(FSP_SUCCESS == err);
}
```

## Data Structures

struct [cgc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

◆ **cgc\_instance\_ctrl\_t**

```
struct cgc_instance_ctrl_t
```

CGC private control block. DO NOT MODIFY. Initialization occurs when [R\\_CGC\\_Open\(\)](#) is called.

**Data Fields**

void const *	<a href="#">p_context</a>
--------------	---------------------------

**Field Documentation**◆ **p\_context**

```
void const* cgc_instance_ctrl_t::p_context
```

Placeholder for user data. Passed to the user callback in [cgc\\_callback\\_args\\_t](#).

**Function Documentation**◆ **R\_CGC\_Open()**

```
fsp_err_t R_CGC_Open ( cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg )
```

Initialize the CGC API. Implements [cgc\\_api\\_t::open](#).

Example:

```
/* Initializes the CGC module. */
err = R_CGC_Open(&g_cgc0_ctrl, &g_cgc0_cfg);
```

**Return values**

FSP_SUCCESS	CGC successfully initialized.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_ALREADY_OPEN	Module is already open.

## ◆ R\_CGC\_ClocksCfg()

```
fsp_err_t R_CGC_ClocksCfg ( cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg )
```

Reconfigures all main system clocks. This API can be used for any of the following purposes:

- start or stop clocks
- change the system clock source
- configure the PLL/PLL2 multiplication and division ratios when starting the PLL
- change the system dividers

If the requested system clock source has a stabilization flag, this function blocks waiting for the stabilization flag of the requested system clock source to be set. If the requested system clock source was just started and it has no stabilization flag, this function blocks for the stabilization time required by the requested system clock source according to the Electrical Characteristics section of the hardware manual. If the requested system clock source has no stabilization flag and it is already running, it is assumed to be stable and this function will not block. If the requested system clock is the subclock, the subclock must be stable prior to calling this function.

The internal dividers (`cgc_clocks_cfg_t::divider_cfg`) are subject to constraints described in footnotes of the hardware manual table detailing specifications for the clock generation circuit for the internal clocks for the MCU. For example:

- RA6M3: see footnotes of Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100
- RA2A1: see footnotes of Table 9.2 "Clock generation circuit specifications for the internal clocks" in the RA2A1 manual R01UH0888EJ0100

Do not attempt to stop the requested clock source or the source of a PLL if the PLL will be running after this operation completes.

Implements `cgc_api_t::clocksCfg`.

Example:

```
/* Assuming the system clock is MOCO, switch to HOCO. */
cgc_clocks_cfg_t clocks_cfg;

clocks_cfg.system_clock          = CGC_CLOCK_PLL;

clocks_cfg.pll_state             = CGC_CLOCK_CHANGE_NONE;

clocks_cfg.pll_cfg.source_clock = CGC_CLOCK_MAIN_OSC; // unused

clocks_cfg.pll_cfg.multiplier   = CGC_PLL_MUL_10_0;   // unused

clocks_cfg.pll_cfg.divider      = CGC_PLL_DIV_2;      // unused

clocks_cfg.divider_cfg.iclk_div = CGC_SYS_CLOCK_DIV_1;

clocks_cfg.divider_cfg.pclka_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkb_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkc_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.pclkd_div = CGC_SYS_CLOCK_DIV_4;

clocks_cfg.divider_cfg.bclk_div = CGC_SYS_CLOCK_DIV_4;
```

```

clocks_cfg.divider_cfg.fclk_div = CGC_SYS_CLOCK_DIV_4;
clocks_cfg.mainosc_state         = CGC_CLOCK_CHANGE_NONE;
clocks_cfg.hoco_state           = CGC_CLOCK_CHANGE_START;
clocks_cfg.moco_state           = CGC_CLOCK_CHANGE_STOP;
clocks_cfg.loco_state           = CGC_CLOCK_CHANGE_NONE;
err = R_CGC_ClocksCfg(&g_cgc0_ctrl, &clocks_cfg);
assert(FSP_SUCCESS == err);

```

### Return values

FSP_SUCCESS	Clock configuration applied successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	Attempt to stop the current system clock or the PLL source clock.
FSP_ERR_CLOCK_ACTIVE	PLL configuration cannot be changed while PLL is running.
FSP_ERR_OSC_STOP_DET_ENABLED	PLL multiplier must be less than 20 if oscillation stop detect is enabled and the input frequency is less than 12.5 MHz.
FSP_ERR_NOT_STABILIZED	PLL clock source is not stable.
FSP_ERR_PLL_SRC_INACTIVE	PLL clock source is not running.
FSP_ERR_INVALID_STATE	The subclock must be running before activating HOCO with FLL.

◆ **R\_CGC\_ClockStart()**

```
fsp_err_t R_CGC_ClockStart ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg )
```

Start the specified clock if it is not currently active. The PLL configuration cannot be changed while the PLL is running. Implements `cgc_api_t::clockStart`.

The PLL source clock must be operating and stable prior to starting the PLL.

Example:

```
/* Start the LOCO. */
err = R_CGC_ClockStart(&g_cgc0_ctrl, CGC_CLOCK_LOCO, NULL);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Clock initialized successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_STABILIZED	The clock source is not stabilized after being turned off or PLL clock source is not stable.
FSP_ERR_PLL_SRC_INACTIVE	PLL clock source is not running.
FSP_ERR_CLOCK_ACTIVE	PLL configuration cannot be changed while PLL is running.
FSP_ERR_OSC_STOP_DET_ENABLED	PLL multiplier must be less than 20 if oscillation stop detect is enabled and the input frequency is less than 12.5 MHz.
FSP_ERR_INVALID_STATE	The subclock must be running before activating HOCO with FLL.

◆ **R\_CGC\_ClockStop()**

```
fsp_err_t R_CGC_ClockStop ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source )
```

Stop the specified clock if it is active. Implements `cgc_api_t::clockStop`.

Do not attempt to stop the current system clock source. Do not attempt to stop the source clock of a PLL if the PLL is running.

**Return values**

FSP_SUCCESS	Clock stopped successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	Attempt to stop the current system clock or the PLL source clock.
FSP_ERR_OSC_STOP_DET_ENABLED	Attempt to stop MOCO when Oscillation stop is enabled.
FSP_ERR_NOT_STABILIZED	Clock not stabilized after starting.

◆ **R\_CGC\_ClockCheck()**

```
fsp_err_t R_CGC_ClockCheck ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source )
```

Check the specified clock for stability. Implements `cgc_api_t::clockCheck`.

**Return values**

FSP_SUCCESS	Clock is running and stable.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_STABILIZED	Clock not stabilized.
FSP_ERR_CLOCK_INACTIVE	Clock not turned on.

## ◆ R\_CGC\_SystemClockSet()

```
fsp_err_t R_CGC_SystemClockSet ( cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source,
cgc_divider_cfg_t const *const p_divider_cfg )
```

Set the specified clock as the system clock and configure the internal dividers for ICLK, PCLKA, PCLKB, PCLKC, PCLKD, BCLK, and FCLK. Implements `cgc_api_t::systemClockSet`.

The requested clock source must be running and stable prior to calling this function. The internal dividers are subject to constraints described in the hardware manual table "Specifications of the Clock Generation Circuit for the internal clocks".

The internal dividers (`p_divider_cfg`) are subject to constraints described in footnotes of the hardware manual table detailing specifications for the clock generation circuit for the internal clocks for the MCU. For example:

- RA6M3: see footnotes of Table 9.2 "Specifications of the clock generation circuit for the internal clocks" in the RA6M3 manual R01UH0886EJ0100
- RA2A1: see footnotes of Table 9.2 "Clock generation circuit specifications for the internal clocks" in the RA2A1 manual R01UH0888EJ0100

This function also updates the RAM and ROM wait states, the operating power control mode, and the SystemCoreClock CMSIS global variable.

Example:

```
/* Set divisors. Divisors for clocks that don't exist on the MCU are ignored. */
cgc_divider_cfg_t dividers =
{
/* PCLKB is not used in this application, so select the maximum divisor for lowest
power. */
.pclkb_div = CGC_SYS_CLOCK_DIV_64,
/* PCLKD is not used in this application, so select the maximum divisor for lowest
power. */
.pclkd_div = CGC_SYS_CLOCK_DIV_64,
/* ICLK is the MCU clock, allow it to run as fast as the LOCO is capable. */
.iclk_div = CGC_SYS_CLOCK_DIV_1,
/* These clocks do not exist on some devices. If any clocks don't exist, set the
divider to 1. */
.pclka_div = CGC_SYS_CLOCK_DIV_1,
.pclkc_div = CGC_SYS_CLOCK_DIV_1,
.fclk_div = CGC_SYS_CLOCK_DIV_1,
.bclk_div = CGC_SYS_CLOCK_DIV_1,
};
/* Switch the system clock to LOCO. */
```

```
err = R_CGC_SystemClockSet(&g_cg0_ctrl, CGC_CLOCK_LOCO, &dividers);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CLOCK_INACTIVE	The specified clock source is inactive.
FSP_ERR_NOT_STABILIZED	The clock source has not stabilized

**◆ R\_CGC\_SystemClockGet()**

```
fsp_err_t R_CGC_SystemClockGet ( cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source,
cgc_divider_cfg_t *const p_divider_cfg )
```

Return the current system clock source and configuration. Implements `cgc_api_t::systemClockGet`.

**Return values**

FSP_SUCCESS	Parameters returned successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ R\_CGC\_OscStopDetectEnable()

```
fsp_err_t R_CGC_OscStopDetectEnable ( cgc_ctrl_t *const p_ctrl)
```

Enable the oscillation stop detection for the main clock. Implements `cgc_api_t::oscStopDetectEnable`.

The MCU will automatically switch the system clock to MOCO when a stop is detected if Main Clock is the system clock. If the system clock is the PLL, then the clock source will not be changed and the PLL free running frequency will be the system clock frequency.

Example:

```
/* Enable oscillation stop detection. The main oscillator must be running at this
point. */
err = R_CGC_OscStopDetectEnable(&g_cgc0_ctrl);
assert(FSP_SUCCESS == err);
```

#### Return values

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_LOW_VOLTAGE_MODE	Settings not allowed in low voltage mode.

◆ **R\_CGC\_OscStopDetectDisable()**

```
fsp_err_t R_CGC_OscStopDetectDisable ( cgc_ctrl_t *const p_ctrl)
```

Disable the oscillation stop detection for the main clock. Implements `cgc_api_t::oscStopDetectDisable`.

Example:

```
/* (Optional) Oscillation stop detection must be disabled before entering any low
power mode. */
err = R_CGC_OscStopDetectDisable(&g_cgc0_ctrl);
assert(FSP_SUCCESS == err);
__WFI();
```

**Return values**

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_OSC_STOP_DETECTED	The Oscillation stop detect status flag is set. Under this condition it is not possible to disable the Oscillation stop detection function.

◆ **R\_CGC\_OscStopStatusClear()**

```
fsp_err_t R_CGC_OscStopStatusClear ( cgc_ctrl_t *const p_ctrl)
```

Clear the Oscillation Stop Detection Status register. This register is not cleared automatically if the stopped clock is restarted. Implements `cgc_api_t::oscStopStatusClear`.

After clearing the status, oscillation stop detection is no longer enabled.

This register cannot be cleared while the main oscillator is the system clock or the PLL source clock.

Example:

```
/* (Optional) Clear the error flag. Only clear this flag after switching the MCU
clock source away from the main
* oscillator and if the main oscillator is stable again. */
err = R_CGC_OscStopStatusClear(&g_cgc0_ctrl);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Operation performed successfully.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CLOCK_INACTIVE	Main oscillator must be running to clear the oscillation stop detection flag.
FSP_ERR_OSC_STOP_CLOCK_ACTIVE	The Oscillation Detect Status flag cannot be cleared if the Main Osc or PLL is set as the system clock. Change the system clock before attempting to clear this bit.
FSP_ERR_INVALID_HW_CONDITION	Oscillation stop status was not cleared. Check preconditions and try again.

◆ **R\_CGC\_CallbackSet()**

```
fsp_err_t R_CGC_CallbackSet ( cgc_ctrl_t *const p_api_ctrl, void(*) (cgc_callback_args_t *)
p_callback, void const *const p_context, cgc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `cgc_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **R\_CGC\_Close()**

```
fsp_err_t R_CGC_Close ( cgc_ctrl_t *const p_ctrl)
```

Closes the CGC module. Implements `cgc_api_t::close`.

**Return values**

FSP_SUCCESS	The module is successfully closed.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Module is not open.

**4.2.11 Cyclic Redundancy Check (CRC) Calculator (r\_crc)**

## Modules

**Functions**

```
fsp_err_t R_CRC_Open (crc_ctrl_t *const p_ctrl, crc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_CRC_Close (crc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_CRC_Calculate (crc_ctrl_t *const p_ctrl, crc_input_t *const
p_crc_input, uint32_t *calculatedValue)
```

```
fsp_err_t R_CRC_CalculatedValueGet (crc_ctrl_t *const p_ctrl, uint32_t
*calculatedValue)
```

```
fsp_err_t R_CRC_SnoopEnable (crc_ctrl_t *const p_ctrl, uint32_t crc_seed)
```

```
fsp_err_t R_CRC_SnoopDisable (crc_ctrl_t *const p_ctrl)
```

## Detailed Description

Driver for the CRC peripheral on RA MCUs. This module implements the [CRC Interface](#).

## Overview

The CRC module provides a API to calculate 8, 16 and 32-bit CRC values on a block of data in memory or a stream of data over a Serial Communication Interface (SCI) channel using industry-standard polynomials.

### Features

- CRC module supports the following 8 and 16 bit CRC polynomials which operates on 8-bit data in parallel
  - $X^8+X^2+X+1$  (CRC-8)
  - $X^{16}+X^{15}+X^2+1$  (CRC-16)
  - $X^{16}+X^{12}+X^5+1$  (CRC-CCITT)
- CRC module supports the following 32 bit CRC polynomials which operates on 32-bit data in parallel
  - $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$  (CRC-32)
  - $X^{32}+X^{28}+X^{27}+X^{26}+X^{25}+X^{23}+X^{22}+X^{20}+X^{19}+X^{18}+X^{14}+X^{13}+X^{11}+X^{10}+X^9+X^8+X^6+1$  (CRC-32C)
- CRC module can calculate CRC with LSB first or MSB first bit order.

## Configuration

### Build Time Configurations for r\_crc

The following build time configurations are defined in fsp\_cfg/r\_crc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > CRC Driver on r\_crc

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > CRC Driver on r\_crc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Name	Name must be a valid C symbol	g_crc0	Module name.
CRC Polynomial	<ul style="list-style-type: none"> <li>• CRC-8</li> <li>• CRC-16</li> <li>• CRC-CCITT</li> <li>• CRC-32</li> <li>• CRC-32C</li> </ul>	CRC-32C	Select the CRC polynomial.
Bit Order	<ul style="list-style-type: none"> <li>• LSB</li> <li>• MSB</li> </ul>	MSB	Select the CRC bit order.
Snoop Address	Refer to the RA Configuration tool for available options.	NONE	Select the SCI register address CRC snoop

## Clock Configuration

There is no clock configuration for the CRC module.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## CRC Snoop

The CRC snoop function monitors reads from and writes to a specified I/O register address and performs CRC calculation on the data read from and written to the register address automatically. Instead of calling R\_CRC\_Calculate on a block of data, R\_CRC\_SnoopEnable is called to start monitoring reads/writes and R\_CRC\_CalculatedValueGet is used to obtain the current CRC.

### Note

*Snoop mode is available for transmit/receive operations on SCI only.*

## Limitations

When using CRC32 polynomial functions the CRC module produces the same results as popular online CRC32 calculators, but it is important to remember a few important points.

- Online CRC32 calculators allow the input to be any number of bytes. The FSP CRC32 API function uses 32-bit words. This means the online calculations must be 'padded' to end on a 32-bit boundary.
- Online CRC32 calculators usually invert the output prior to presenting it as a result. It is up to the application program to include this step if needed.
- The seed value of 0xFFFFFFFF needs to be used by both the online calculator and the R\_CRC module API (CRC32 polynomials)
- Make sure the bit orientation of the R\_CRC CRC32 is set for LSB and that you have CRC32 selected and not CRC32C.
- Some online CRC tools XOR the final result with 0xFFFFFFFF.

## Examples

## Basic Example

This is a basic example of minimal use of the CRC module in an application.

```
void crc_example ()
{
    uint32_t length;
    uint32_t uint8_calculated_value;
    length = sizeof(g_data_8bit) / sizeof(g_data_8bit[0]);
    crc_input_t example_input =
    {
        .p_input_buffer = g_data_8bit,
        .num_bytes      = length,
        .crc_seed       = 0,
    };
    /* Open CRC module with 8 bit polynomial */
    R_CRC_Open(&crc_ctrl, &g_crc_test_cfg);
    /* 8-bit CRC calculation */
    R_CRC_Calculate(&crc_ctrl, &example_input, &uint8_calculated_value);
}
```

## Snoop Example

This example demonstrates CRC snoop operation.

```
void crc_snoop_example ()
{
    /* Open CRC module with 8 bit polynomial */
    R_CRC_Open(&crc_ctrl, &g_crc_test_cfg);
    /* Open SCI Driver */
    /* Configure Snoop address and enable snoop mode */
    R_CRC_SnoopEnable(&crc_ctrl, 0);
    /* Perform SCI read/write operation depending on the SCI snoop address configure */
    /* Read CRC value */
    R_CRC_CalculatedValueGet(&crc_ctrl, &g_crc_buff);
}
```

## Data Structures

struct [crc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [crc\\_instance\\_ctrl\\_t](#)

struct [crc\\_instance\\_ctrl\\_t](#)

Driver instance control structure.

## Function Documentation

### ◆ [R\\_CRC\\_Open\(\)](#)

[fsp\\_err\\_t](#) [R\\_CRC\\_Open](#) ( [crc\\_ctrl\\_t](#) \*const *p\_ctrl*, [crc\\_cfg\\_t](#) const \*const *p\_cfg* )

Open the CRC driver module

Implements [crc\\_api\\_t::open](#)

Open the CRC driver module and initialize the driver control block according to the passed-in configuration structure.

#### Return values

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	<i>p_ctrl</i> or <i>p_cfg</i> is NULL.
FSP_ERR_ALREADY_OPEN	Module already open

### ◆ [R\\_CRC\\_Close\(\)](#)

[fsp\\_err\\_t](#) [R\\_CRC\\_Close](#) ( [crc\\_ctrl\\_t](#) \*const *p\_ctrl* )

Close the CRC module driver.

Implements [crc\\_api\\_t::close](#)

#### Return values

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	<i>p_ctrl</i> is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_Calculate()**

```
fsp_err_t R_CRC_Calculate ( crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *
calculatedValue )
```

Perform a CRC calculation on a block of 8-bit/32-bit (for 32-bit polynomial) data.

Implements `crc_api_t::calculate`

This function performs a CRC calculation on an array of 8-bit/32-bit (for 32-bit polynomial) values and returns an 8-bit/32-bit (for 32-bit polynomial) calculated value

**Return values**

FSP_SUCCESS	Calculation successful.
FSP_ERR_ASSERTION	Either p_ctrl, inputBuffer, or calculatedValue is NULL.
FSP_ERR_INVALID_ARGUMENT	length value is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_CalculatedValueGet()**

```
fsp_err_t R_CRC_CalculatedValueGet ( crc_ctrl_t *const p_ctrl, uint32_t * calculatedValue )
```

Return the current calculated value.

Implements `crc_api_t::crcResultGet`

CRC calculation operates on a running value. This function returns the current calculated value.

**Return values**

FSP_SUCCESS	Return of calculated value successful.
FSP_ERR_ASSERTION	Either p_ctrl or calculatedValue is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_SnoopEnable()**

```
fsp_err_t R_CRC_SnoopEnable ( crc_ctrl_t *const p_ctrl, uint32_t crc_seed )
```

Configure the snoop channel and set the CRC seed.

Implements [crc\\_api\\_t::snoopEnable](#)

The CRC calculator can operate on reads and writes over any of the first ten SCI channels. For example, if set to channel 0, transmit, every byte written out SCI channel 0 is also sent to the CRC calculator as if the value was explicitly written directly to the CRC calculator.

**Return values**

FSP_SUCCESS	Snoop configured successfully.
FSP_ERR_ASSERTION	Pointer to control structure is NULL
FSP_ERR_NOT_OPEN	The driver is not opened.

◆ **R\_CRC\_SnoopDisable()**

```
fsp_err_t R_CRC_SnoopDisable ( crc_ctrl_t *const p_ctrl)
```

Disable snooping.

Implements [crc\\_api\\_t::snoopDisable](#)

**Return values**

FSP_SUCCESS	Snoop disabled.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The driver is not opened.

**4.2.12 Capacitive Touch Sensing Unit (r\_ctsu)**

## Modules

**Functions**

```
fsp_err_t R_CTSU_Open (ctsu_ctrl_t *const p_ctrl, ctstu_cfg_t const *const p_cfg)
```

Opens and configures the CTSU driver module. Implements [ctsu\\_api\\_t::open](#). [More...](#)

```
fsp_err_t R_CTSU_ScanStart (ctsu_ctrl_t *const p_ctrl)
```

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with [R\\_CTSU\\_DataGet\(\)](#). If a different control block scan should be run, check the scan is complete before executing. Implements [ctsu\\_api\\_t::scanStart](#). [More...](#)

`fsp_err_t R_CTSU_DataGet (ctsu_ctrl_t *const p_ctrl, uint16_t *p_data)`

This function gets the sensor values as scanned by the CTSU. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [ctsu\\_api\\_t::dataGet](#). [More...](#)

`fsp_err_t R_CTSU_CallbackSet (ctsu_ctrl_t *const p_api_ctrl, void(*p_callback)(ctsu_callback_args_t *), void const *const p_context, ctсу_callback_args_t *const p_callback_memory)`

`fsp_err_t R_CTSU_Diagnosis (ctsu_ctrl_t *const p_ctrl)`

Diagnosis the CTSU peripheral. Implements [ctsu\\_api\\_t::diagnosis](#). [More...](#)

`fsp_err_t R_CTSU_Close (ctsu_ctrl_t *const p_ctrl)`

Disables specified CTSU control block. Implements [ctsu\\_api\\_t::close](#). [More...](#)

## Detailed Description

This HAL driver supports the Capacitive Touch Sensing Unit (CTSUS). It implements the [CTSUS Interface](#).

## Overview

The capacitive touch sensing unit HAL driver (r\_ctsu) provides an API to control the CTSUS peripheral. This module performs capacitance measurement based on various settings defined by the configuration. This module is configured via the [QE for Capacitive Touch](#).

## Features

- Supports both Self-capacitance multi scan mode and Mutual-capacitance full scan mode
- Scans may be started by software or an external trigger
- Returns measured capacitance data on scan completion
- Optional DTC support

## Configuration

*Note*

*This module is configured via the [QE for Capacitive Touch](#). For information on how to use the QE tool, once the tool is installed click [Help](#) -> [Help Contents in e2 studio](#) and search for "QE".*

**Build Time Configurations for r\_ctsu**

The following build time configurations are defined in fsp\_cfg/r\_ctsu\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support for using DTC	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Enable DTC support for the CTSU module.
Interrupt priority level	MCU Specific Options		Priority level of all CTSU interrupt (CSTU_WR, CTSU_RD, CTSU_FN)

**Configurations for Driver > CapTouch > CTSU Driver on r\_ctsu**

This module can be added to the Stacks tab via New Stack > Driver > CapTouch > CTSU Driver on r\_ctsu. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Scan Start Trigger	MCU Specific Options		CTSU Scan Start Trigger Select

**Interrupt Configuration**

The first [R\\_CTSU\\_Open](#) function call sets CTSU peripheral interrupts. The user should provide a callback function to be invoked at the end of the CTSU scan sequence. The callback argument will contain information about the scan status.

**Clock Configuration**

The CTSU peripheral module uses PCLKB as its clock source. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

*Note*

*The CTSU Drive pulse will be calculated and set by the tooling depending on the selected transfer rate.*

**Pin Configuration**

The TSn pins are sensor pins for the CTSU.

The TSCAP pin is used for an internal low-pass filter and must be connected to an external decoupling capacitor.

**Usage Notes**

## CTS U

### Sensor ICO correction

In order to improve the measurement accuracy, the correction coefficient is generated at the first [R\\_CTSU\\_Open](#). Therefore, the first [R\\_CTSU\\_Open](#) process takes about 40ms.

### Initial offset tuning

CTS U has a current offset mechanism to cancel the parasitic capacitance. This module automatically adjusts to be within the dynamic range of the Sensor ICO, taking into account the amount of current that changes with touch. This adjustment uses normal measurement process and requires several [R\\_CTSU\\_ScanStart](#) and [R\\_CTSU\\_DataGet](#). [R\\_CTSU\\_DataGet](#) returns `FSP_ERR_CTSU_INCOMPLETE_TUNING` if it is being adjusted. The member "so" of [cts\\_u\\_element\\_cfg\\_t](#) is used as the starting point for adjustment, so if this value is appropriate, it can be completed quickly. Normally, this value uses the value adjusted by QE for Capacitive Touch.

### Scan trigger

Scanning of sensors may begin by either a software trigger or an external event initiated by the Event Link Controller (ELC). This trigger can be set with the member "cap" of [cts\\_u\\_cfg\\_t](#). Typically, a software trigger is used. Common usage is to have a periodic timer initiate scans. For software triggers, a periodic timer such as the CMT is configured whose interval is large enough to allow for all sensors to be scanned and data to be updated. Software triggers are issued by calling [R\\_CTSU\\_ScanStart](#). Using an external trigger is processed almost identically to using software triggers. Call [R\\_CTSU\\_ScanStart](#) before starting the timer to set the measurement and prepare for external trigger measurement. After that, when the timer is started, the measurement start trigger is applied.

### Self-capacitance multi scan mode

In self-capacitance mode each TS pin is assigned to one touch button. Electrodes of multiple TS pins can be physically aligned to create slider or wheel interfaces.

- Scan Order
  - The hardware scans the specified pins in ascending order.
  - For example, if pins TS05, TS08, TS02, TS03, and TS06 are specified in your application, the hardware will scan them in the order TS02, TS03, TS05, TS06, TS08.
- Element
  - An element refers to the index of a pin within the scan order. Using the previous example, TS05 is element 2.
- Scan Time
  - Scanning is handled directly by the CTS U peripheral and does not utilize any main processor time.
  - It takes approximately 500us to scan a single sensor.
  - If DTC is not used additional overhead is required for the main processor to transfer data to/from registers when each sensor is scanned.

Set `CTS U_MODE_SELF_MULTI_SCAN` to "md" of [cts\\_u\\_cfg\\_t](#). Also, add the number of terminals used for this measurement to `CTS U_CFG_NUM_SELF_ELEMENTS`. For details, refer to the configuration and sample application output by QE for Capacitive Touch.

### Mutual-capacitance full scan mode

In mutual-capacitance mode each TS pin acts as either a 'row' or 'column' in an array of sensors. As a result, this mode uses fewer pins when more than five sensors are configured. Mutual-capacitance mode is ideal for applications where many touch sensors are required, like keypads, button matrices and pads.

As an example, consider a standard phone keypad comprised of a matrix of four rows and three columns.

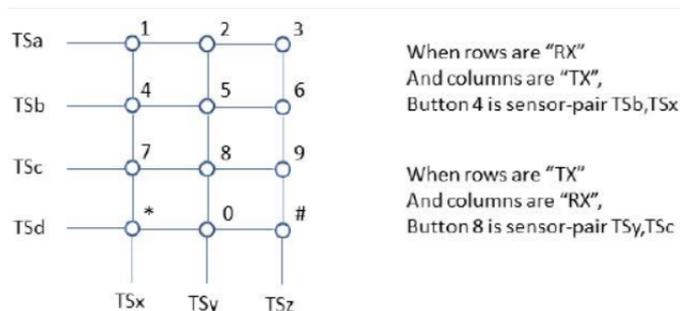


Figure 150: Mutual Button Image

)

In mutual capacitance mode only 7 pins are necessary to scan 12 buttons. In self mode, 12 pins would be required.

- Scan Order
  - The hardware scans the matrix by iterating over the TX pins first and the RX pins second.
  - For example, if pins TS10, TS11, and TS03 are specified as RX sensors and pins TS02, TS07, and TS04 are specified as TX sensors, the hardware will scan them in the following sensor-pair order: TS03-TS02, TS03-TS04, TS03-TS07, TS10-TS02, TS10-TS04, TS10-TS07, TS11-TS02, TS11-TS04, TS11-TS07
- Element
  - An element refers to the index of a sensor-pair within the scan order. Using the previous example, TS10-TS07 is element 5.
- Scan Time
  - Because mutual-capacitance scans two patterns for one element it takes twice as long as self-capacitance (1ms vs 0.5ms per element).

Set `CTSU_MODE_MUTUAL_FULL_SCAN` to "md" of `cts_cfg_t`. Also, add the number of matrix used for this measurement to `CTS_CFG_NUM_MUTUAL_ELEMENTS`. For details, refer to the configuration and sample application output by QE for Capacitive Touch.

## CTS2 (RA2L1)

CTS2 is a peripheral that improves CTSU. For CTS2, this module supports the following in addition to the features described in the CTSU chapter.

### Improved accuracy with more accurate ICO correction

The internal circuit of CTS2 is used to create a correction coefficient with higher accuracy than CTSU. This correction coefficient is created by the first `R_CTSU_Open` like CTSU, but it takes about

100ms. For Mutual-capacitance parallel scan mode, create a correction factor for the CFC circuit. This is also created with the first [R\\_CTSU\\_Open](#). It takes about 40ms.

### Improved noise immunity by multi-frequency measurement

CTS2 can measure up to 4 different drive frequencies to avoid sync noise. This module sets the number of frequencies with `CTS2_CFG_NUM_SUMULTI`. The recommended value is 3. The three frequencies are set according to `CTS2_CFG_SUMULTI0`, `CTS2_CFG_SUMULTI1` and `CTS2_CFG_SUMULTI2`. 0x3F is the center. QE will automatically output the recommended value. From the three results obtained, make a noise removal judgment to determine the measured value. By setting `judge_multifreq_disable` in `cts2_cfg_t` to true, it is possible to get three results without making a majority vote and use your own noise filter. Prepare three times as many buffers for the data to be acquired by [R\\_CTSU\\_DataGet](#).

### Mutual-capacitance parallel scan mode

This mode provides fast measurement time by parallel scanning the RX lines with a CFC circuit. Operation is otherwise identical to normal CTS2 mutual scanning.

- Scan Order
  - The hardware scans all RX pins simultaneously for each TX pin.
  - For example, if sensors TS10, TS11, and TS03 are specified as RX sensors, and sensors TS02, TS07, and TS04 are specified as TX sensors, the hardware will scan them in the following sensor-pair order:  
TS02-(TS03, TS10, TS11), TS04-(TS03, TS10, TS11), TS07-(TS03, TS10, TS11)
- Element
  - An element refers to the index of a sensor-pair within the scan order. Using the previous example, TS07-TS10 is element 7.
- Scan Time
  - Because the RX lines are scanned in parallel, CFC mutual-capacitance scan is the same amount of times faster than a basic mutual matrix scan as the number of RX lines. In other words, on a matrix with N receive lines, CFC mutual scanning is N times faster than basic mutual scanning.

Set `CTS2_MODE_MUTUAL_CFC_SCAN` to "md" of `cts2_cfg_t`. Also, add the number of matrix used for this measurement to `CTS2_CFG_NUM_MUTUAL_ELEMENTS`. In addition, set the number of `CTS2_CFG_NUM_CFC` and `CTS2_CFG_NUM_CFC_TX`. For details, refer to the configuration and sample application output by QE for Capacitive Touch.

### Current scan mode

CTS2 can measure the current input to the TS terminal. This module supports this feature. Set `CTS2_MODE_CURRENT_SCAN` to "md" of `cts2_cfg_t`. Also, add the number of terminals used for this measurement to `CTS2_CFG_NUM_SELF_ELEMENTS`. For details, refer to the configuration and sample application output by QE for Capacitive Touch.

### Active shield

CTS2 can drive a shield signal on a single TS pin. This module can set the shield for each instance. Set the members of `cts2_cfg_t` as shown in the example below. Other configurations omitted

```
.txvsel    = CTS2_TXVSEL_INTERNAL_POWER,  
.txvsel2   = CTS2_TXVSEL_MODE,
```

```
.md          = CTSU_MODE_SELF_MULTI_SCAN,  
.posel       = CTSU_POSEL_SAME_PULSE,  
.ctsuchac0  = 0x0F,  
.ctsuchtrc0 = 0x08,
```

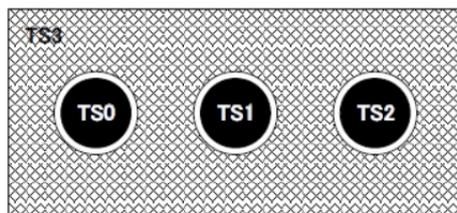


Figure 151: Shield pin Image

#### Note

*This feature is only available in self-capacitance mode.*

## Temperature Correction

The internal circuit of CTSU2 and r\_adc can be used to compensate for temperature drift. This keeps the measured value constant even if the temperature changes. An instance for temperature correction is required to operate this function, and it is also necessary to measure this instance on a regular basis. For details, refer to the configuration and sample application output by QE for Capacitive Touch.

## TrustZone Support

In r\_ctsu and rm\_touch module, Non-Secure Callable Guard Functions are only generated from QE for Capacitive Touch. QE can be used for tuning in secure or flat project, but not in non-secure project. If you want to use in non-secure project, copy the output file from secure or flat project. Refer to QE Help for more information.

## Diagnosis Support

Diagnose the functions inside the chip. It can be implemented by adding an API function [R\\_CTSU\\_Diagnosis](#).

# Examples

## Basic Example

This is a basic example of minimal use of the CTSU in an application.

```
volatile bool g_scan_flag = false;  
void ctsu_callback (ctsu_callback_args_t * p_args)  
{  
    if (CTSU_EVENT_SCAN_COMPLETE == p_args->event)
```

```
{
    g_scan_flag = true;
}
}
void ctsu_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    uint16_t data[CTSU_CFG_NUM_SELF_ELEMENTS];
    err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    while (true)
    {
        err = R_CTSU_ScanStart(&g_ctsu_ctrl);
        assert(FSP_SUCCESS == err);
        while (!g_scan_flag)
        {
            /* Wait for scan end callback */
        }
        g_scan_flag = false;
        err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
        if (FSP_SUCCESS == err)
        {
            /* Application specific data processing. */
        }
    }
}
```

### Multi-configuration Example

This is an optional example of using both Self-capacitance and Mutual-capacitance configurations in the same project.

```
void ctsu_optional_example (void)
{
```

```
fsp_err_t err = FSP_SUCCESS;

uint16_t data[CTSU_CFG_NUM_SELF_ELEMENTS + (CTSU_CFG_NUM_MUTUAL_ELEMENTS * 2)];
err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
assert(FSP_SUCCESS == err);
err = R_CTSU_Open(&g_ctsu_ctrl_mutual, &g_ctsu_cfg_mutual);
assert(FSP_SUCCESS == err);

while (true)
{
R_CTSU_ScanStart(&g_ctsu_ctrl);
while (!g_scan_flag)
{
/* Wait for scan end callback */
}
g_scan_flag = false;
R_CTSU_ScanStart(&g_ctsu_ctrl_mutual);
while (!g_scan_flag)
{
/* Wait for scan end callback */
}
g_scan_flag = false;
err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
assert(FSP_SUCCESS == err);
if (FSP_SUCCESS == err)
{
/* Application specific data processing. */
}
err = R_CTSU_DataGet(&g_ctsu_ctrl_mutual, data);
assert(FSP_SUCCESS == err);
if (FSP_SUCCESS == err)
{
/* Application specific data processing. */
}
}
}
```

## Data Structures

struct [ctsu\\_ctsuwr\\_t](#)

struct [ctsu\\_self\\_buf\\_t](#)

struct [ctsu\\_mutual\\_buf\\_t](#)

struct [ctsu\\_correction\\_info\\_t](#)

struct [ctsu\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [ctsu\\_state\\_t](#)

enum [ctsu\\_tuning\\_t](#)

enum [ctsu\\_correction\\_status\\_t](#)

enum [ctsu\\_range\\_t](#)

## Data Structure Documentation

### ◆ [ctsu\\_ctsuwr\\_t](#)

struct <a href="#">ctsu_ctsuwr_t</a>		
CTSUWR write register value		
Data Fields		
uint16_t	ctsussc	Copy from (ssdiv << 8) by Open API.
uint16_t	ctsus00	Copy from ((snum << 10)   so) by Open API.
uint16_t	ctsus01	Copy from (sdpa << 8) by Open API. ICOG and RICOA is set recommend value.

### ◆ [ctsu\\_self\\_buf\\_t](#)

struct <a href="#">ctsu_self_buf_t</a>		
Scan buffer data formats (Self)		
Data Fields		
uint16_t	sen	Sensor counter data.
uint16_t	ref	Reference counter data (Not used)

### ◆ [ctsu\\_mutual\\_buf\\_t](#)

struct ctsu_mutual_buf_t		
Scan buffer data formats (Mutual)		
Data Fields		
uint16_t	pri_sen	Primary sensor data.
uint16_t	pri_ref	Primary reference data (Not used)
uint16_t	snd_sen	Secondary sensor data.
uint16_t	snd_ref	Secondary reference data (Not used)

◆ **ctsu\_correction\_info\_t**

struct ctsu_correction_info_t		
Correction information		
Data Fields		
ctsu_correction_status_t	status	Correction status.
ctsu_ctsuwr_t	ctsuwr	Correction scan parameter.
volatile ctsu_self_buf_t	scanbuf	Correction scan buffer.
uint16_t	first_val	1st correction value
uint16_t	second_val	2nd correction value
uint32_t	first_coefficient	1st correction coefficient
uint32_t	second_coefficient	2nd correction coefficient
uint32_t	ctsu_clock	CTSU clock [MHz].

◆ **ctsu\_instance\_ctrl\_t**

struct ctsu_instance_ctrl_t		
CTSU private control block. DO NOT MODIFY. Initialization occurs when <a href="#">R_CTSU_Open()</a> is called.		
Data Fields		
uint32_t	<a href="#">open</a>	
		Whether or not driver is open.
volatile <a href="#">ctsu_state_t</a>	<a href="#">state</a>	
		CTSU run state.
<a href="#">ctsu_tuning_t</a>	<a href="#">tuning</a>	
		CTSU Initial offset tuning status.

uint16_t	<a href="#">num_elements</a>
	Number of elements to scan.
uint16_t	<a href="#">wr_index</a>
	Word index into ctsuwr register array.
uint16_t	<a href="#">rd_index</a>
	Word index into scan data buffer.
uint8_t *	<a href="#">p_tuning_count</a>
	Pointer to tuning count of each element. g_ctsu_tuning_count[] is set by Open API.
int32_t *	<a href="#">p_tuning_diff</a>
	Pointer to difference from base value of each element. g_ctsu_tuning_diff[] is set by Open API.
uint16_t	<a href="#">average</a>
	CTSUs Moving average counter.
uint16_t	<a href="#">num_moving_average</a>
	Copy from config by Open API.
uint8_t	<a href="#">ctsucr1</a>
	Copy from (atune1 << 3, md << 6) by Open API. CLK, ATUNE0, CSW, and PON is set by HAL driver.
<a href="#">ctsu_ctsuwr_t *</a>	<a href="#">p_ctsuwr</a>
	CTSUWR write register value. g_ctsu_ctsuwr[] is set by Open API.

<a href="#">ctsu_self_buf_t *</a>	<a href="#">p_self_raw</a>
	Pointer to Self raw data. g_ctsu_self_raw[] is set by Open API.
<a href="#">uint16_t *</a>	<a href="#">p_self_data</a>
	Pointer to Self moving average data. g_ctsu_self_data[] is set by Open API.
<a href="#">ctsu_mutual_buf_t *</a>	<a href="#">p_mutual_raw</a>
	Pointer to Mutual raw data. g_ctsu_mutual_raw[] is set by Open API.
<a href="#">uint16_t *</a>	<a href="#">p_mutual_pri_data</a>
	Pointer to Mutual primary moving average data. g_ctsu_mutual_pri_data[] is set by Open API.
<a href="#">uint16_t *</a>	<a href="#">p_mutual_snd_data</a>
	Pointer to Mutual secondary moving average data. g_ctsu_mutual_snd_data[] is set by Open API.
<a href="#">ctsu_correction_info_t *</a>	<a href="#">p_correction_info</a>
	Pointer to correction info.
<a href="#">ctsu_cfg_t const *</a>	<a href="#">p_ctsu_cfg</a>
	Pointer to initial configurations.
<a href="#">IRQn_Type</a>	<a href="#">write_irq</a>
	Copy from config by Open API. CTSU_CTSUWR interrupt vector.
<a href="#">IRQn_Type</a>	<a href="#">read_irq</a>
	Copy from config by Open API. CTSU_CTSURD interrupt vector.

IRQn_Type	<a href="#">end_irq</a>
	Copy from config by Open API. CTSU_CTSUFN interrupt vector.
void(*	<a href="#">p_callback</a> )(ctsu_callback_args_t *)
	Callback provided when a CTSUFN occurs.
ctsu_callback_args_t *	<a href="#">p_callback_memory</a>
	Pointer to non-secure memory that can be used to pass arguments to a callback in non-secure memory.
void const *	<a href="#">p_context</a>
	Placeholder for user data.

## Enumeration Type Documentation

### ◆ ctsu\_state\_t

enum <a href="#">ctsu_state_t</a>	
CTSU run state	
Enumerator	
CTSU_STATE_INIT	Not open.
CTSU_STATE_IDLE	Opened.
CTSU_STATE_SCANNING	Scanning now.
CTSU_STATE_SCANNED	Scan end.

◆ **ctsu\_tuning\_t**

enum <a href="#">ctsu_tuning_t</a>	
CTSU Initial offset tuning status	
Enumerator	
CTSU_TUNING_INCOMPLETE	Initial offset tuning incomplete.
CTSU_TUNING_COMPLETE	Initial offset tuning complete.

◆ **ctsu\_correction\_status\_t**

enum <a href="#">ctsu_correction_status_t</a>	
CTSU Correction status	
Enumerator	
CTSU_CORRECTION_INIT	Correction initial status.
CTSU_CORRECTION_RUN	Correction scan running.
CTSU_CORRECTION_COMPLETE	Correction complete.
CTSU_CORRECTION_ERROR	Correction error.

◆ **ctsu\_range\_t**

enum <a href="#">ctsu_range_t</a>	
CTSU range definition	
Enumerator	
CTSU_RANGE_20UA	20uA mode
CTSU_RANGE_40UA	40uA mode
CTSU_RANGE_80UA	80uA mode
CTSU_RANGE_160UA	160uA mode
CTSU_RANGE_NUM	number of range

**Function Documentation**

**◆ R\_CTSU\_Open()**

```
fsp_err_t R_CTSU_Open ( ctsu_ctrl_t *const p_ctrl, ctsu_cfg_t const *const p_cfg )
```

Opens and configures the CTSU driver module. Implements `ctsu_api_t::open`.

Example:

```
err = R_CTSU_Open(&g_ctsu_ctrl, &g_ctsu_cfg);
```

**Return values**

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

**Note**

*In the first Open, measurement for correction works, and it takes several tens of milliseconds.*

## ◆ R\_CTSU\_ScanStart()

`fsp_err_t R_CTSU_ScanStart ( ctsu_ctrl_t *const p_ctrl)`

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with `R_CTSU_DataGet()`. If a different control block scan should be run, check the scan is complete before executing. Implements `ctsu_api_t::scanStart`.

Example:

```
while (true)
{
    err = R_CTSU_ScanStart(&g_ctsu_ctrl);
    assert(FSP_SUCCESS == err);
while (!g_scan_flag)
{
    /* Wait for scan end callback */
}
    g_scan_flag = false;
    err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
if (FSP_SUCCESS == err)
{
    /* Application specific data processing. */
}
}
```

### Return values

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance or other.
FSP_ERR_CTSU_NOT_GET_DATA	The previous data has not been retrieved by DataGet.

◆ **R\_CTSU\_DataGet()**

```
fsp_err_t R_CTSU_DataGet ( ctsu_ctrl_t *const p_ctrl, uint16_t * p_data )
```

This function gets the sensor values as scanned by the CTSU. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [ctsu\\_api\\_t::dataGet](#).

Example:

```
while (true)
{
    err = R_CTSU_ScanStart(&g_ctsu_ctrl);
    assert(FSP_SUCCESS == err);
while (!g_scan_flag)
{
    /* Wait for scan end callback */
}
    g_scan_flag = false;
    err = R_CTSU_DataGet(&g_ctsu_ctrl, data);
if (FSP_SUCCESS == err)
{
    /* Application specific data processing. */
}
}
```

**Return values**

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.
FSP_ERR_CTSU_DIAG_NOT_YET	Diagnosis of data collected no yet.

◆ **R\_CTSU\_CallbackSet()**

```
fsp_err_t R_CTSU_CallbackSet ( ctsu_ctrl_t *const p_api_ctrl, void(*) (ctsu_callback_args_t *)
p_callback, void const *const p_context, ctsu_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `ctsu_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_CTSU\_Diagnosis()**

```
fsp_err_t R_CTSU_Diagnosis ( ctsu_ctrl_t *const p_ctrl)
```

Diagnosis the CTSU peripheral. Implements `ctsu_api_t::diagnosis`.

Example:

```
err = R_CTSU_Diagnosis(&g_cts_u_ctrl_diagnosis);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_NOT_GET_DATA	The previous data has not been retrieved by DataGet.
FSP_ERR_CTSU_DIAG_LDO_OVER_VOLTAGE	Diagnosis of LDO over voltage failed.
FSP_ERR_CTSU_DIAG_CCO_HIGH	Diagnosis of CCO into 19.2uA failed.
FSP_ERR_CTSU_DIAG_CCO_LOW	Diagnosis of CCO into 2.4uA failed.
FSP_ERR_CTSU_DIAG_SSCG	Diagnosis of SSCG frequency failed.
FSP_ERR_CTSU_DIAG_DAC	Diagnosis of non-touch count value failed.
FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE	Diagnosis of LDO output voltage failed.
FSP_ERR_CTSU_DIAG_OVER_VOLTAGE	Diagnosis of over voltage detection circuit failed.
FSP_ERR_CTSU_DIAG_OVER_CURRENT	Diagnosis of over current detection circuit failed.
FSP_ERR_CTSU_DIAG_LOAD_RESISTANCE	Diagnosis of LDO internal resistance value failed.
FSP_ERR_CTSU_DIAG_CURRENT_SOURCE	Diagnosis of LDO internal resistance value failed.
FSP_ERR_CTSU_DIAG_SENSCLK_GAIN	Diagnosis of SENSCLK frequency gain failed.
FSP_ERR_CTSU_DIAG_SUCLK_GAIN	Diagnosis of SUCLK frequency gain failed.
FSP_ERR_CTSU_DIAG_CLOCK_RECOVERY	Diagnosis of SUCLK clock recovery function failed.
FSP_ERR_CTSU_DIAG_CFC_GAIN	Diagnosis of CFC oscillator gain failed.

**◆ R\_CTSU\_Close()**

```
fsp_err_t R_CTSU_Close ( ctsu_ctrl_t *const p_ctrl)
```

Disables specified CTSU control block. Implements `ctsu_api_t::close`.

**Return values**

FSP_SUCCESS	CTSU successfully configured.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

**4.2.13 Digital to Analog Converter (r\_dac)**

## Modules

**Functions**

```
fsp_err_t R_DAC_Open (dac_ctrl_t *p_api_ctrl, dac_cfg_t const *const p_cfg)
```

```
fsp_err_t R_DAC_Write (dac_ctrl_t *p_api_ctrl, uint16_t value)
```

```
fsp_err_t R_DAC_Start (dac_ctrl_t *p_api_ctrl)
```

```
fsp_err_t R_DAC_Stop (dac_ctrl_t *p_api_ctrl)
```

```
fsp_err_t R_DAC_Close (dac_ctrl_t *p_api_ctrl)
```

**Detailed Description**

Driver for the DAC12 peripheral on RA MCUs. This module implements the [DAC Interface](#).

**Overview****Features**

The DAC module outputs one of 4096 voltage levels between the positive and negative reference voltages.

- Supports setting left-justified or right-justified 12-bit value format for the 16-bit input data registers
- Supports output amplifiers on selected MCUs
- Supports charge pump on selected MCUs
- Supports synchronization with the Analog-to-Digital Converter (ADC) module

## Configuration

### Note

For MCUs supporting more than one channel, the following configuration options are shared by all the DAC channels:

- Synchronize with ADC
- Data Format
- Charge Pump

### Build Time Configurations for r\_dac

The following build time configurations are defined in fsp\_cfg/r\_dac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > DAC Driver on r\_dac

This module can be added to the Stacks tab via New Stack > Driver > Analog > DAC Driver on r\_dac. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_dac0	Module name.
Channel	Value must be an integer greater than or equal to 0	0	Specify the hardware channel.
Synchronize with ADC	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable DA/AD synchronization.
Data Format	<ul style="list-style-type: none"> <li>• Right Justified</li> <li>• Left Justified</li> </ul>	Right Justified	Specify the DAC data format.
Output Amplifier	MCU Specific Options		Enable the DAC output amplifier.
Charge Pump (Requires MOCO active)	MCU Specific Options		Enable the DAC charge pump.
ELC Trigger Source	MCU Specific Options		ELC event source that will trigger the DAC to start a conversion.

### Clock Configuration

The DAC peripheral module uses PCLKB as its clock source.

### Pin Configuration

The DAN pins are used as analog outputs. Each DAC channel has one output pin.

The AVCC0 and AVSS0 pins are power and ground supply pins for the DAC and ADC.

The VREFH and VREFL pins are top and ground voltage reference pins for the DAC and ADC.

## Usage Notes

### Charge Pump

The charge pump must be enabled when using DAC pin output while operating at  $AV_{CC} < 2.7V$ .

#### Note

*The MOCO must be running to use the charge pump.*

*If the DAC output is to be routed to an internal signal, do not enable the charge pump.*

### Synchronization with ADC

When ADC synchronization is enabled and an ADC conversion is in progress, if a DAC conversion is started it will automatically be delayed until after the ADC conversion is complete.

### Limitations

- For MCUs supporting ADC unit 1:
  - Once synchronization between DAC and ADC unit 1 is turned on during R\_DAC\_Open synchronization cannot be turned off by the driver. In order to desynchronize DAC with ADC unit 1, manually clear DAADSCR.DAADST to 0 when the ADCSR.ADST bit is 0 and ADC unit 1 is halted.
  - The DAC module can only be synchronized with ADC unit 1.
  - For MCUs having more than 1 DAC channel, both channels are synchronized with ADC unit 1 if synchronization is enabled.
- Pin configuration does not support setting ASEL and PSEL bit fields for the same pin. In order to set the PSEL when DAC pin is enabled, manually update the setting of the DAC pin to `.pin_cfg = ((uint32_t)IOPORT_CFG_ANALOG_ENABLE | IOPORT_CFG_PERIPHERAL_PIN | IOPORT_PERIPHERAL_CAC_AD)`.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_DAC in an application. This example shows how this driver can be used for basic Digital to Analog Conversion operations.

```
void basic_example (void)
{
    fsp_err_t err;
    uint16_t value;
    /* Pin configuration: Output enable DA0 as Analog. */
    /* Initialize the DAC channel */
    err = R_DAC_Open(&g_dac_ctrl, &g_dac_cfg);
    /* Handle any errors. This function should be defined by the user. */
```

```

assert(FSP_SUCCESS == err);

value = (uint16_t) DAC_EXAMPLE_VALUE_ABC;

err = R_DAC_Write(&g_dac_ctrl, value);

assert(FSP_SUCCESS == err);

err = R_DAC_Start(&g_dac_ctrl);

assert(FSP_SUCCESS == err);
}

```

## Data Structures

struct [dac\\_instance\\_ctrl\\_t](#)

struct [dac\\_extended\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ [dac\\_instance\\_ctrl\\_t](#)

struct [dac\\_instance\\_ctrl\\_t](#)

DAC instance control block.

### ◆ [dac\\_extended\\_cfg\\_t](#)

struct [dac\\_extended\\_cfg\\_t](#)

DAC extended configuration

#### Data Fields

bool	<a href="#">enable_charge_pump</a>	Enable DAC charge pump available on selected MCUs.
bool	<a href="#">output_amplifier_enabled</a>	Output amplifier enable available on selected MCUs.
<a href="#">dac_data_format_t</a>	<a href="#">data_format</a>	Data format.

## Function Documentation

◆ **R\_DAC\_Open()**

```
fsp_err_t R_DAC_Open ( dac_ctrl_t* p_api_ctrl, dac_cfg_t const *const p_cfg )
```

Perform required initialization described in hardware manual. Implements [dac\\_api\\_t::open](#). Configures a single DAC channel, starts the channel, and provides a handle for use with the DAC API Write and Close functions. Must be called once prior to calling any other DAC API functions. After a channel is opened, Open should not be called again for the same channel without calling Close first.

**Return values**

FSP_SUCCESS	The channel was successfully opened.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ul style="list-style-type: none"> <li>1. One or both of the following parameters may be NULL: p_api_ctrl or p_cfg</li> <li>2. data_format value in p_cfg is out of range.</li> <li>3. Extended configuration structure is set to NULL for MCU supporting charge pump.</li> </ul>
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel ID requested in p_cfg may not be available on the devices.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.

◆ **R\_DAC\_Write()**

```
fsp_err_t R_DAC_Write ( dac_ctrl_t* p_api_ctrl, uint16_t value )
```

Write data to the D/A converter and enable the output if it has not been enabled.

**Return values**

FSP_SUCCESS	Data is successfully written to the D/A Converter.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Start()**

```
fsp_err_t R_DAC_Start ( dac_ctrl_t * p_api_ctrl)
```

Start the D/A conversion output if it has not been started.

**Return values**

FSP_SUCCESS	The channel is started successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_IN_USE	Attempt to re-start a channel.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Stop()**

```
fsp_err_t R_DAC_Stop ( dac_ctrl_t * p_api_ctrl)
```

Stop the D/A conversion and disable the output signal.

**Return values**

FSP_SUCCESS	The control is successfully stopped.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

◆ **R\_DAC\_Close()**

```
fsp_err_t R_DAC_Close ( dac_ctrl_t * p_api_ctrl)
```

Stop the D/A conversion, stop output, and close the DAC channel.

**Return values**

FSP_SUCCESS	The channel is successfully closed.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_ctrl has not been opened.

**4.2.14 Digital to Analog Converter (r\_dac8)**

## Modules

### Functions

`fsp_err_t R_DAC8_Open (dac_ctrl_t *const p_ctrl, dac_cfg_t const *const p_cfg)`

`fsp_err_t R_DAC8_Close (dac_ctrl_t *const p_ctrl)`

`fsp_err_t R_DAC8_Write (dac_ctrl_t *const p_ctrl, uint16_t value)`

`fsp_err_t R_DAC8_Start (dac_ctrl_t *const p_ctrl)`

`fsp_err_t R_DAC8_Stop (dac_ctrl_t *const p_ctrl)`

### Detailed Description

Driver for the DAC8 peripheral on RA MCUs. This module implements the [DAC Interface](#).

## Overview

### Features

The DAC8 module outputs one of 256 voltage levels between the positive and negative reference voltages. DAC8 on selected MCUs have below features

- Charge pump control
- Synchronization with the Analog-to-Digital Converter (ADC) module
- Multiple Operation Modes
  - Normal
  - Real-Time (Event Link)

## Configuration

### Note

*For MCUs supporting more than one channel, the following configuration options are shared by all the DAC8 channels:*

- *Synchronize with ADC*
- *Charge Pump*

### Build Time Configurations for r\_dac8

The following build time configurations are defined in `fsp_cfg/r_dac8_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Analog > DAC8 Driver on r\_dac8

This module can be added to the Stacks tab via New Stack > Driver > Analog > DAC8 Driver on r\_dac8.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_dac8_0	Module name.
Channel	Value must be an integer greater than or equal to 0	0	Specify the hardware channel.
D/A A/D Synchronous Conversion	MCU Specific Options		Synchronize the DAC8 update with the ADC to reduce interference with A/D conversions.
DAC Mode	MCU Specific Options		Select the DAC operating mode
Real-time Trigger Event	MCU Specific Options		Specify the event used to trigger conversion in Real-time mode. This setting is only valid when Real-time mode is enabled.
Charge Pump (Requires MOCO active)	MCU Specific Options		Enable the DAC charge pump.

### Clock Configuration

The DAC8 peripheral module uses the PCLKB as its clock source.

### Pin Configuration

The DA8\_n pins are used as analog outputs. Each DAC8 channel has one output pin.

The AVCC0 and AVSS0 pins are power and ground supply and reference pins for the DAC8.

## Usage Notes

### Charge Pump

The charge pump must be enabled when using DAC8 pin output while operating at  $AV_{CC} < 2.7V$ .

*Note*

*The MOCO must be running to use the charge pump.*

*If DAC8 output is to be routed to an internal signal, do not enable the charge pump.*

### Synchronization with ADC

When ADC synchronization is enabled and an ADC conversion is in progress, if a DAC8 conversion is started it will automatically be delayed until after the ADC conversion is complete.

## Real-time Mode

When Real-time mode is selected, the DAC8 will perform a conversion each time the selected ELC event is received.

## Limitations

- Synchronization between DAC8 and ADC is activated when calling R\_DAC8\_Open. At this point synchronization cannot be deactivated by the driver. In order to desynchronize DAC8 with ADC, manually clear DACADSCR.DACADST to 0 while the ADCSR.ADST bit is 0 and the ADC is halted.
- For MCUs having more than 1 DAC8 channel, both channels are synchronized with ADC if synchronization is enabled.
- Pin configuration does not support setting ASEL and PSEL bit fields for the same pin. In order to set the PSEL when DAC pin is enabled, manually update the setting of the DAC pin to `.pin_cfg = ((uint32_t)IOPORT_CFG_ANALOG_ENABLE | IOPORT_CFG_PERIPHERAL_PIN | IOPORT_PERIPHERAL_CAC_AD)`.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_DAC8 in an application. This example shows how this driver can be used for basic 8 bit Digital to Analog Conversion operations.

```
dac8_instance_ctrl_t g_dac8_ctrl;
dac_cfg_t g_dac8_cfg =
{
    .channel          = 0U,
    .ad_da_synchronized = false,
    .p_extend        = &g_dac8_cfg_extend
};

void basic_example (void)
{
    fsp_err_t err;
    uint16_t value;
    /* Pin configuration: Output enable DA8_0(RA2A1) as Analog. */
    /* Initialize the DAC8 channel */
    err = R_DAC8_Open(&g_dac8_ctrl, &g_dac8_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    value = (uint8_t) DAC8_EXAMPLE_VALUE_ABC;
    /* Write value to DAC module */
```

```

err = R_DAC8_Write(&g_dac8_ctrl, value);
assert(FSP_SUCCESS == err);
/* Start DAC8 conversion */
err = R_DAC8_Start(&g_dac8_ctrl);
assert(FSP_SUCCESS == err);
}

```

## Data Structures

struct [dac8\\_instance\\_ctrl\\_t](#)

struct [dac8\\_extended\\_cfg\\_t](#)

## Enumerations

enum [dac8\\_mode\\_t](#)

## Data Structure Documentation

### ◆ [dac8\\_instance\\_ctrl\\_t](#)

struct [dac8\\_instance\\_ctrl\\_t](#)

DAC8 instance control block. DO NOT INITIALIZE.

### ◆ [dac8\\_extended\\_cfg\\_t](#)

struct [dac8\\_extended\\_cfg\\_t](#)

DAC8 extended configuration

#### Data Fields

bool	<a href="#">enable_charge_pump</a>	Enable DAC charge pump.
<a href="#">dac8_mode_t</a>	<a href="#">dac_mode</a>	DAC mode.

## Enumeration Type Documentation

### ◆ [dac8\\_mode\\_t](#)

enum [dac8\\_mode\\_t](#)

#### Enumerator

<a href="#">DAC8_MODE_NORMAL</a>	DAC Normal mode.
<a href="#">DAC8_MODE_REAL_TIME</a>	DAC Real-time (event link) mode.

## Function Documentation

### ◆ R\_DAC8\_Open()

```
fsp_err_t R_DAC8_Open ( dac_ctrl_t *const p_ctrl, dac_cfg_t const *const p_cfg )
```

Perform required initialization described in hardware manual.

Implements `dac_api_t::open`.

Configures a single DAC channel. Must be called once prior to calling any other DAC API functions. After a channel is opened, Open should not be called again for the same channel without calling Close first.

#### Return values

FSP_SUCCESS	The channel was successfully opened.
FSP_ERR_ASSERTION	One or both of the following parameters may be NULL: p_ctrl or p_cfg
FSP_ERR_ALREADY_OPEN	The instance control structure has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	An invalid channel was requested.
FSP_ERR_NOT_ENABLED	Setting DACADSCR is not enabled when ADCSR.ADST = 0.

#### Note

*This function is reentrant for different channels. It is not reentrant for the same channel.*

### ◆ R\_DAC8\_Close()

```
fsp_err_t R_DAC8_Close ( dac_ctrl_t *const p_ctrl)
```

Stop the D/A conversion, stop output, and close the DAC channel.

#### Return values

FSP_SUCCESS	The channel is successfully closed.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.

◆ **R\_DAC8\_Write()**

```
fsp_err_t R_DAC8_Write ( dac_ctrl_t *const p_ctrl, uint16_t value )
```

Write data to the D/A converter.

**Return values**

FSP_SUCCESS	Data is successfully written to the D/A Converter.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.
FSP_ERR_OVERFLOW	Data overflow when data value exceeds 8-bit limit.

◆ **R\_DAC8\_Start()**

```
fsp_err_t R_DAC8_Start ( dac_ctrl_t *const p_ctrl)
```

Start the D/A conversion output.

**Return values**

FSP_SUCCESS	The channel is started successfully.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.
FSP_ERR_IN_USE	Attempt to re-start a channel.

◆ **R\_DAC8\_Stop()**

```
fsp_err_t R_DAC8_Stop ( dac_ctrl_t *const p_ctrl)
```

Stop the D/A conversion and disable the output signal.

**Return values**

FSP_SUCCESS	The control is successfully stopped.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Channel associated with p_instance_ctrl has not been opened.

## 4.2.15 Direct Memory Access Controller (r\_dmac)

### Modules

#### Functions

fsp\_err\_t R\_DMAC\_Open (transfer\_ctrl\_t \*const p\_api\_ctrl, transfer\_cfg\_t const \*const p\_cfg)

fsp\_err\_t R\_DMAC\_Reconfigure (transfer\_ctrl\_t \*const p\_api\_ctrl, transfer\_info\_t \*p\_info)

fsp\_err\_t R\_DMAC\_Reset (transfer\_ctrl\_t \*const p\_api\_ctrl, void const \*volatile p\_src, void \*volatile p\_dest, uint16\_t const num\_transfers)

fsp\_err\_t R\_DMAC\_SoftwareStart (transfer\_ctrl\_t \*const p\_api\_ctrl, transfer\_start\_mode\_t mode)

fsp\_err\_t R\_DMAC\_SoftwareStop (transfer\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t R\_DMAC\_Enable (transfer\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t R\_DMAC\_Disable (transfer\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t R\_DMAC\_InfoGet (transfer\_ctrl\_t \*const p\_api\_ctrl, transfer\_properties\_t \*const p\_info)

fsp\_err\_t R\_DMAC\_Close (transfer\_ctrl\_t \*const p\_api\_ctrl)

#### Detailed Description

Driver for the DMAC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

## Overview

The Direct Memory Access Controller (DMAC) transfers data from one memory location to another without using the CPU.

#### Features

- Supports multiple transfer modes
  - Normal transfer
  - Repeat transfer
  - Block transfer
  - Repeat-Block transfer (Not available on all MCUs)
- Address increment, decrement, fixed, or offset modes
- Triggered by ELC events
  - Some exceptions apply, see the Event table in the Event Numbers section of the Interrupt Controller Unit chapter of the hardware manual

- Supports 1, 2, and 4 byte data units

## Configuration

### Build Time Configurations for r\_dmac

The following build time configurations are defined in fsp\_cfg/r\_dmac\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Transfer > Transfer Driver on r\_dmac

This module can be added to the Stacks tab via New Stack > Driver > Transfer > Transfer Driver on r\_dmac .

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_transfer0	Module name.
Channel	Value must be a non-negative integer	0	Specify the hardware channel.
Mode	<ul style="list-style-type: none"> <li>• Normal</li> <li>• Repeat</li> <li>• Block</li> <li>• Repeat-Block</li> </ul>	Normal	Select the transfer mode. Normal: One transfer per activation, transfer ends after Number of Transfers; Repeat: One transfer per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of Blocks; Block: Number of Blocks per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of Blocks.
Transfer Size	<ul style="list-style-type: none"> <li>• 1 Byte</li> <li>• 2 Bytes</li> <li>• 4 Bytes</li> </ul>	2 Bytes	Select the transfer size.
Destination Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Offset addition</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the destination.

Source Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Offset addition</li> <li>• Incremented</li> <li>• Decrement</li> </ul>	Fixed	Select the address mode for the source.
Repeat Area (Unused in Normal Mode)	<ul style="list-style-type: none"> <li>• Destination</li> <li>• Source</li> </ul>	Source	Select the repeat area. Either the source or destination address resets to its initial value after completing Number of Transfers in Repeat or Block mode.
Destination Pointer	Manual Entry	NULL	Specify the transfer destination pointer.
Source Pointer	Manual Entry	NULL	Specify the transfer source pointer.
Number of Transfers	Value must be a non-negative integer	1	Specify the number of transfers for repeat and normal mode or block size for repeat-block transfer mode.
Number of Blocks (Valid only in Repeat,Block or Repeat-Block Mode)	Value must be a non-negative integer	0	Specify the number of blocks to transfer in Repeat,Block or Repeat-Block mode.
Activation Source	MCU Specific Options		Select the DMAC transfer start event. If no ELC event is chosen then software start can be used.
Callback	Name must be a valid C symbol	NULL	A user callback that is called at the end of the transfer.
Context	Manual Entry	NULL	Pointer to the context structure passed through the callback argument.
Transfer End Interrupt Priority	MCU Specific Options		Select the transfer end interrupt priority.
Interrupt Frequency	<ul style="list-style-type: none"> <li>• Interrupt after all transfers have completed</li> <li>• Interrupt after each block, or repeat size is transferred</li> </ul>	Interrupt after all transfers have completed	Select to have interrupt after each transfer or after last transfer.
Offset value (Valid only when address mode is 'Offset')	Value must be a 24 bit signed integer.	1	Offset value is added to the address after each transfer.

Source Buffer Size	Value must be a non-negative integer	1	Specify the size of whole source buffer (valid only for Repeat-Block transfer mode with source address update mode other than offset addition).
--------------------	--------------------------------------	---	---

## Clock Configuration

The DMAC peripheral module uses ICLK as the clock source. The ICLK frequency is set by using the **Clocks** tab of the RA Configuration editor prior to a build, or by using the CGC module at run-time.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Transfer Modes

The DMAC Module supports three modes of operation.

- **Normal Mode** - In normal mode, a single data unit is transferred every time the configured ELC event is received by the DMAC channel. A data unit can be 1-byte, 2-bytes, or 4-bytes. The source and destination addresses can be fixed, increment, decrement, or add an offset to the next data unit after each transfer. A 16-bit counter decrements after each transfer. When the counter reaches 0, transfers will no longer be triggered by the ELC event and the CPU can be interrupted to signal that all transfers have finished.
- **Repeat Mode** - Repeat mode works the same way as normal mode, however the length is limited to an integer in the range[1,1024]. When the transfer counter reaches 0, the counter is reset to its configured value, the repeat area (source or destination address) resets to its starting address and the block count remaining will decrement by 1. When the block count reaches 0, transfers will no longer be triggered by the ELC event and the CPU may be interrupted to signal that all transfers have finished.
- **Block Mode** - In block mode, the amount of data units transferred by each interrupt can be set to an integer in the range [1,1024]. The number of blocks to transfer can also be configured to a 16-bit number. After each block transfer the repeat area (source or destination address) will reset to the original address and the other address will be incremented or decremented to the next block.
- **Repeat-Block Mode** - In repeat-block mode, the amount of data units transferred by each interrupt can be set to an integer in the range [1,1024]. The number of blocks to transfer can be configured to a 16 bit number. If the destination address mode is offset mode, maximum configurable number of blocks is 0xFFFF for block size(length) of one with data transfer size as byte,0x7FFF for block size of one with data transfer size as half word and 0x3FFF for block size of one with data size as word. After each block transfer the source address and the destination address will be incremented or decremented to the next block address. In case of offset address mode for source address, the source address size is the total size of source buffer after which the source area is rolled over, block size can be smaller than the source buffer size.For source address mode as offset mode, the maximum configurable source buffer size is 0xFFFF for transfer data size of a byte,0x7FFF for transfer data size of half word and 0x3FFF for transfer data size of word. Repeat-block mode can be used to implement single ring buffer to multiple ring buffer transfer type design.

## Selecting the DTC or DMAC

The Transfer API is implemented by both DTC and the DMAC so that applications can switch between the DTC and the DMAC. When selecting between them, consider these factors:

	DTC	DMAC
Repeat Mode	<ul style="list-style-type: none"> <li>Repeats forever</li> <li>Max repeat size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Configurable number of repeats</li> <li>Max repeat size is 1024 x 4 bytes</li> </ul>
Block Mode	<ul style="list-style-type: none"> <li>Max block size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Max block size is 1024 x 4 bytes</li> </ul>
Channels	<ul style="list-style-type: none"> <li>One instance per interrupt</li> </ul>	<ul style="list-style-type: none"> <li>MCU specific (8 channels or less)</li> </ul>
Chained Transfers	<ul style="list-style-type: none"> <li>Supported</li> </ul>	<ul style="list-style-type: none"> <li>Not Supported</li> </ul>
Software Trigger	<ul style="list-style-type: none"> <li>Must use the software ELC event</li> </ul>	<ul style="list-style-type: none"> <li>Has support for software trigger without using software ELC event</li> <li>Supports TRANSFER_START_MODE_SINGLE and TRANSFER_START_MODE_REPEAT</li> </ul>
Offset Address Mode	<ul style="list-style-type: none"> <li>Not supported</li> </ul>	<ul style="list-style-type: none"> <li>Supported</li> </ul>

## Interrupts

The DTC and DMAC interrupts behave differently. The DTC uses the configured IELSR event IRQ as the interrupt source whereas each DMAC channel has its own IRQ.

The transfer\_info\_t::irq setting also behaves a little differently depending on which mode is selected.

## Normal Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	N/A
TRANSFER_IRQ_END	Interrupt after last transfer	Interrupt after last transfer

## Repeat Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	Interrupt after each repeat
TRANSFER_IRQ_END	Interrupt after each repeat	Interrupt after last transfer

## Block Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each block	Interrupt after each block
TRANSFER_IRQ_END	Interrupt after last block	Interrupt after last block

## Additional Considerations

- The DTC requires a moderate amount of RAM (one `transfer_info_t` struct per open instance + `DTC_VECTOR_TABLE_SIZE`).
- The DTC stores transfer information in RAM and writes back to RAM after each transfer whereas the DMAC stores all transfer information in registers.
- When transfers are configured for more than one activation source, the DTC must fetch the transfer info from RAM on each interrupt. This can cause a higher latency between transfers.

## Offset Address Mode

When the source or destination mode is configured to offset mode, a configurable offset is added to the source or destination pointer after each transfer. The offset is a signed 24 bit number.

## Examples

### Basic Example

This is a basic example of minimal use of the DMAC in an application. In this case, one or more events have been routed to the DMAC for handling so it only needs to be enabled to start accepting transfers.

```
void dmac_minimal_example (void)
{
    /* Open the transfer instance with initial configuration. */
    fsp_err_t err = R_DMAC_Open(&g_transfer_ctrl, &g_transfer_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable the DMAC so that it responds to transfer requests. */
    err = R_DMAC_Enable(&g_transfer_ctrl);
    assert(FSP_SUCCESS == err);
}
```

### CRC32 Example

In this example the DMAC is used to feed the CRC peripheral to perform a CRC32 operation.

```
volatile bool g_transfer_complete = false;
void dmac_callback (dmac_callback_args_t * cb_data)
{
    FSP_PARAMETER_NOT_USED(cb_data);
    g_transfer_complete = true;
}
```

```
}  
void dmac_crc_example (void)  
{  
    uint8_t p_src[TRANSFER_LENGTH];  
    /* Initialize p_src to [ABC..OP] */  
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)  
    {  
        p_src[i] = (uint8_t) ('A' + (i % 26));  
    }  
    /* Set transfer source address to p_src */  
    g_transfer_cfg.p_info->p_src = (void *) p_src;  
    /* Set transfer destination address to the CRC data input register */  
    g_transfer_cfg.p_info->p_dest = (void *) &R_CRC->CRCDIR;  
    /* Open the transfer instance with initial configuration. */  
    fsp_err_t err = R_DMAC_Open(&g_transfer_ctrl, &g_transfer_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    assert(FSP_SUCCESS == err);  
    /* Enable DMAC transfers. */  
    (void) R_DMAC_Enable(&g_transfer_ctrl);  
    /* Open the CRC module. */  
    err = R_CRC_Open(&g_crc_ctrl, &g_crc_cfg);  
    assert(FSP_SUCCESS == err);  
    /* Clear the transfer complete flag. */  
    g_transfer_complete = false;  
    /* Trigger the transfer using software. */  
    err = R_DMAC_SoftwareStart(&g_transfer_ctrl, TRANSFER_START_MODE_SINGLE);  
    assert(FSP_SUCCESS == err);  
    while (!g_transfer_complete)  
    {  
        /* Wait for transfer complete interrupt */  
    }  
    /* Get CRC result and perform final XOR. */  
    uint32_t crc32;  
    (void) R_CRC_CalculatedValueGet(&g_crc_ctrl, &crc32);  
}
```

```

    crc32 ^= CRC32_FINAL_XOR_VALUE;

/* Verify that the CRC32 is calculated correctly. */
/* CRC32("ABCD...NOP") = 0xE0E8FF4D. */

const uint32_t expected_crc32 = 0xE0E8FF4D;

if (expected_crc32 != crc32)
{
/* Handle any CRC errors. This function should be defined by the user. */
    handle_crc_error();
}
}

```

## Data Structures

struct [dmac\\_instance\\_ctrl\\_t](#)

struct [dmac\\_callback\\_args\\_t](#)

struct [dmac\\_extended\\_cfg\\_t](#)

## Macros

#define [DMAC\\_MAX\\_NORMAL\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_REPEAT\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_BLOCK\\_TRANSFER\\_LENGTH](#)

#define [DMAC\\_MAX\\_REPEAT\\_COUNT](#)

#define [DMAC\\_MAX\\_BLOCK\\_COUNT](#)

## Data Structure Documentation

### ◆ [dmac\\_instance\\_ctrl\\_t](#)

struct [dmac\\_instance\\_ctrl\\_t](#)

Control block used by driver. DO NOT INITIALIZE - this structure will be initialized in [transfer\\_api\\_t::open](#).

### ◆ [dmac\\_callback\\_args\\_t](#)

struct [dmac\\_callback\\_args\\_t](#)

Callback function parameter data.

Data Fields

void const *	p_context	Placeholder for user data. Set in r_transfer_t::open function in transfer_cfg_t.
--------------	-----------	--

#### ◆ dmac\_extended\_cfg\_t

struct dmac_extended_cfg_t		
DMAC transfer configuration extension. This extension is required.		
<b>Data Fields</b>		
uint8_t	channel	
		Channel number, does not apply to all HAL drivers.
IRQn_Type	irq	
		DMAC interrupt number.
uint8_t	ipl	
		DMAC interrupt priority.
int32_t	offset	
		Offset value used with transfer_addr_mode_t::TRANSFER_ADDR_MODE_OFFSET.
uint16_t	src_buffer_size	
elc_event_t	activation_source	
void(*	p_callback )(dmac_callback_args_t *cb_data)	
void const *	p_context	
<b>Field Documentation</b>		

**◆ src\_buffer\_size**

uint16\_t dmac\_extended\_cfg\_t::src\_buffer\_size

Source ring buffer size for [TRANSFER\\_MODE\\_REPEAT\\_BLOCK](#).**◆ activation\_source**

elc\_event\_t dmac\_extended\_cfg\_t::activation\_source

Select which event will trigger the transfer.

*Note**Select ELC\_EVENT\_NONE for software activation in order to use softwareStart and softwareStart to trigger transfers.***◆ p\_callback**

void(\* dmac\_extended\_cfg\_t::p\_callback) (dmac\_callback\_args\_t \*cb\_data)

Callback for transfer end interrupt.

**◆ p\_context**

void const\* dmac\_extended\_cfg\_t::p\_context

Placeholder for user data. Passed to the user p\_callback in [dmac\\_callback\\_args\\_t](#).**Macro Definition Documentation****◆ DMAC\_MAX\_NORMAL\_TRANSFER\_LENGTH**

#define DMAC\_MAX\_NORMAL\_TRANSFER\_LENGTH

Max configurable number of transfers in [TRANSFER\\_MODE\\_NORMAL](#).**◆ DMAC\_MAX\_REPEAT\_TRANSFER\_LENGTH**

#define DMAC\_MAX\_REPEAT\_TRANSFER\_LENGTH

Max number of transfers per repeat for [TRANSFER\\_MODE\\_REPEAT](#).**◆ DMAC\_MAX\_BLOCK\_TRANSFER\_LENGTH**

#define DMAC\_MAX\_BLOCK\_TRANSFER\_LENGTH

Max number of transfers per block in [TRANSFER\\_MODE\\_BLOCK](#)

◆ **DMAC\_MAX\_REPEAT\_COUNT**

#define DMAC\_MAX\_REPEAT\_COUNT

Max configurable number of repeats to transfer in TRANSFER\_MODE\_REPEAT

◆ **DMAC\_MAX\_BLOCK\_COUNT**

#define DMAC\_MAX\_BLOCK\_COUNT

Max configurable number of blocks to transfer in TRANSFER\_MODE\_BLOCK

**Function Documentation**◆ **R\_DMAM\_Open()**

fsp\_err\_t R\_DMAM\_Open ( transfer\_ctrl\_t\*const p\_api\_ctrl, transfer\_cfg\_t const\*const p\_cfg )

Configure a DMAM channel.

**Return values**

FSP_SUCCESS	Successful open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The configured channel is invalid.
FSP_ERR_IRQ_BSP_DISABLED	The IRQ associated with the activation source is not enabled in the BSP.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.

◆ **R\_DMAM\_Reconfigure()**

fsp\_err\_t R\_DMAM\_Reconfigure ( transfer\_ctrl\_t\*const p\_api\_ctrl, transfer\_info\_t\* p\_info )

Reconfigure the transfer with new transfer info.

**Return values**

FSP_SUCCESS	Transfer is configured and will start when trigger occurs.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_ENABLED	DMAM is not enabled. The current configuration must not be valid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.

◆ **R\_DMAM\_Reset()**

```
fsp_err_t R_DMAM_Reset ( transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers )
```

Reset transfer source, destination, and number of transfers.

**Return values**

FSP_SUCCESS	Transfer reset successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_ENABLED	DMAC is not enabled. The current configuration must not be valid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.

◆ **R\_DMAM\_SoftwareStart()**

```
fsp_err_t R_DMAM_SoftwareStart ( transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode )
```

If the mode is TRANSFER\_START\_MODE\_SINGLE initiate a single transfer with software. If the mode is TRANSFER\_START\_MODE\_REPEAT continue triggering transfers until all of the transfers are completed.

**Return values**

FSP_SUCCESS	Transfer started written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAM_Open to initialize the control block.
FSP_ERR_UNSUPPORTED	Handle was not configured for software activation.

◆ **R\_DMAC\_SoftwareStop()**

`fsp_err_t R_DMAC_SoftwareStop ( transfer_ctrl_t *const p_api_ctrl)`

Stop software transfers if they were started with TRANSFER\_START\_MODE\_REPEAT.

**Return values**

FSP_SUCCESS	Transfer stopped written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_Enable()**

`fsp_err_t R_DMAC_Enable ( transfer_ctrl_t *const p_api_ctrl)`

Enable transfers for the configured activation source.

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_Disable()**

`fsp_err_t R_DMAC_Disable ( transfer_ctrl_t *const p_api_ctrl)`

Disable transfers so that they are no longer triggered by the activation source.

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

◆ **R\_DMAC\_InfoGet()**

```
fsp_err_t R_DMAC_InfoGet ( transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_info )
```

Set driver specific information in provided pointer.

**Return values**

FSP_SUCCESS	Information has been written to p_info.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

◆ **R\_DMAC\_Close()**

```
fsp_err_t R_DMAC_Close ( transfer_ctrl_t *const p_api_ctrl)
```

Disable transfer and clean up internal data. Implements `transfer_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DMAC_Open to initialize the control block.

**4.2.16 Data Operation Circuit (r\_doc)**

## Modules

**Functions**

```
fsp_err_t R_DOC_Open (doc_ctrl_t *const p_api_ctrl, doc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_DOC_Close (doc_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DOC_StatusGet (doc_ctrl_t *const p_api_ctrl, doc_status_t *const p_status)
```

```
fsp_err_t R_DOC_Write (doc_ctrl_t *const p_api_ctrl, uint16_t data)
```

```
fsp_err_t R_DOC_CallbackSet (doc_ctrl_t *const p_api_ctrl,
```

```
void(*p_callback)(doc_callback_args_t *), void const *const
p_context, doc_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the DOC peripheral on RA MCUs. This module implements the [DOC Interface](#).

## Overview

### Features

The DOC HAL module peripheral is used to compare, add or subtract 16-bit data and can detect the following events:

- A match or mismatch between data values
- Overflow of an addition operation
- Underflow of a subtraction operation

A user-defined callback can be created to inform the CPU when any of above events occur.

## Configuration

### Build Time Configurations for r\_doc

The following build time configurations are defined in fsp\_cfg/r\_doc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Data Operation Circuit Driver on r\_doc

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Data Operation Circuit Driver on r\_doc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_doc0	Module name.
Event	<ul style="list-style-type: none"> <li>• Comparison mismatch</li> <li>• Comparison match</li> <li>• Addition overflow</li> <li>• Subtraction underflow</li> </ul>	Comparison mismatch	Select the event that will trigger the DOC interrupt.

Reference/Initial Data	Value must be a 16 bit integer between 0 and 65535	0	Enter Initial Value for Addition/Subtraction or enter reference value for comparison.
Callback	Name must be a valid C symbol	NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) when the configured DOC event occurs.
DOC Interrupt Priority	MCU Specific Options		Select the DOC interrupt priority.

## Clock Configuration

The DOC HAL module does not require a specific clock configuration.

## Pin Configuration

The DOC HAL module does not require and specific pin configurations.

# Usage Notes

## DMAC/DTC Integration

DOC can be used with [Direct Memory Access Controller \(r\\_dmac\)](#) or [Data Transfer Controller \(r\\_dtc\)](#) to write to the input register without CPU intervention. DMAC is more useful for most DOC applications because it can be started directly from software. To write DOC input data with DTC/DMAC, set `transfer_info_t::p_dest` to `R_DOC->DODIR`.

# Examples

## Basic Example

This is a basic example of minimal use of the R\_DOC in an application. This example shows how this driver can be used for continuous 16 bit addition operation while reading the result at every overflow event.

```
#define DOC_EXAMPLE_VALUE 0xF000
uint32_t g_callback_event_counter = 0;
/* This callback is called when DOC overflow event occurs. It is registered in
doc_cfg_t when R_DOC_Open is
* called. */
void doc_callback (doc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
}
```

```
    g_callback_event_counter++;
}
void basic_example (void)
{
    fsp_err_t    err;
    doc_status_t result;

    /* Initialize the DOC module for addition with initial value specified in
doc_cfg_t::doc_data. */
    err = R_DOC_Open(&g_doc_ctrl, &g_doc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Write data to the DOC Data Input Register and read the result of addition from
status register when an
    * interrupt occurs. */
    for (int i = 0; i < 5; i++)
    {
        err = R_DOC_Write(&g_doc_ctrl, DOC_EXAMPLE_VALUE);
        assert(FSP_SUCCESS == err);
    }
    if (g_callback_event_counter >= 1)
    {
        /* Read the result of the operation */
        err = R_DOC_StatusGet(&g_doc_ctrl, &result);
        assert(FSP_SUCCESS == err);
    }
}
}
```

## Function Documentation

---

◆ **R\_DOC\_Open()**

```
fsp_err_t R_DOC_Open ( doc_ctrl_t *const p_api_ctrl, doc_cfg_t const *const p_cfg )
```

Opens and configures the Data Operation Circuit (DOC) in comparison, addition or subtraction mode and sets initial data for addition or subtraction, or reference data for comparison.

Example:

```
/* Initialize the DOC module for addition with initial value specified in
doc_cfg_t::doc_data. */
err = R_DOC_Open(&g_doc_ctrl, &g_doc_cfg);
```

**Return values**

FSP_SUCCESS	DOC successfully configured.
FSP_ERR_ALREADY_OPEN	Module already open.
FSP_ERR_ASSERTION	One or more pointers point to NULL or callback is NULL or the interrupt vector is invalid.

◆ **R\_DOC\_Close()**

```
fsp_err_t R_DOC_Close ( doc_ctrl_t *const p_api_ctrl)
```

Closes the module driver. Enables module stop mode.

**Return values**

FSP_SUCCESS	Module successfully closed.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	Pointer pointing to NULL.

**Note**

*This function will disable the DOC interrupt in the NVIC.*

◆ **R\_DOC\_StatusGet()**

```
fsp_err_t R_DOC_StatusGet ( doc_ctrl_t*const p_api_ctrl, doc_status_t*const p_status )
```

Returns the result of addition/subtraction.

Example:

```
/* Read the result of the operation */
    err = R_DOC_StatusGet(&g_doc_ctrl, &result);
    assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Status successfully read.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	One or more pointers point to NULL.

◆ **R\_DOC\_Write()**

```
fsp_err_t R_DOC_Write ( doc_ctrl_t*const p_api_ctrl, uint16_t data )
```

Writes to the DODIR - DOC Input Register.

Example:

```
err = R_DOC_Write(&g_doc_ctrl, DOC_EXAMPLE_VALUE);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Values successfully written to the registers.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	One or more pointers point to NULL.

### ◆ R\_DOC\_CallbackSet()

```
fsp_err_t R_DOC_CallbackSet ( doc_ctrl_t *const p_api_ctrl, void (*)(doc_callback_args_t *)
p_callback, void const *const p_context, doc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `doc_api_t::callbackSet`

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.17 D/AVE 2D Port Interface (r\_drw)

### Modules

Driver for the DRW peripheral on RA MCUs. This module is a port of D/AVE 2D.

## Overview

### Note

*The D/AVE 2D Port Interface (D1 layer) is a HAL layer for the D/AVE D2 layer API and does not provide any interfaces to the user. Consult the [TES Dave2D Driver Documentation](#) for further information on using the D2 API.*

*For cross-platform compatibility purposes the D1 and D2 APIs are not bound by the FSP coding guidelines for function names and general module functionality.*

## Configuration

### Build Time Configurations for r\_drw

The following build time configurations are defined in `fsp_cfg/r_drw_cfg.h`:

Configuration	Options	Default	Description
Allow Indirect Mode	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	Enable indirect mode to allow no-copy mode for <code>d2_adddlist</code> (see the

TES Dave2D Driver Documentation for details).

Set Memory Allocation to Default to use built-in dynamic memory allocation for the D2 heap. This will use an RTOS heap if configured; otherwise, standard C malloc and free will be used. Set to Custom to define your own allocation scheme for the D2 heap. In this case, the developer will need to define the following functions:

```
void * d1_malloc(size_t size)
void d1_free(void * ptr)
```

Memory Allocation      • Default      Default  
                              • Custom

### Configurations for Driver > Graphics > D/AVE 2D Port Interface on r\_drw

This module can be added to the Stacks tab via New Stack > Driver > Graphics > D/AVE 2D Port Interface on r\_drw.

Configuration	Options	Default	Description
D2 Device Handle Name	Name must be a valid C symbol	d2_handle0	Set the name for the d2_device handle used when calling D2 layer functions.
DRW Interrupt Priority	MCU Specific Options		Select the DRW_INT (display list completion) interrupt priority.

### Heap Size

The D1 port layer allows the D2 driver to allocate memory as needed. There are three ways the driver can accomplish this:

1. Allocate memory using the main heap
2. Allocate memory using a heap provided by an RTOS
3. Allocate memory via user-provided functions

When the "Memory Allocation" configuration option is set to "Default" the driver will use an RTOS implementation if available and the main heap otherwise. Setting the option to "Custom" allows the user to define their own scheme using the following prototypes:

```
void * dl_malloc(size_t size);
void dl_free(void * ptr);
```

### Warning

If there is no RTOS-based allocation scheme the main heap will be used. Be sure that it is enabled by setting the "Heap size (bytes)" property under RA Common on the **BSP** tab of the RA Configuration editor.

### Note

*It is recommended to add 32KB of additional heap space for the D2 driver until the actual usage can be determined in your application.*

### Interrupt

The D1 port includes one interrupt to handle various events like display list completion or bus error. This interrupt is managed internally by the D2 driver and no callback function is available.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the DRW engine:

- The DRW module supports two additional interrupt types - bus error and render complete. These interrupts are not needed for D2 layer operation and thus are not supported.
- If the DRW module is stopped during rendering the render will continue once the module is started again. If this behavior is undesirable in your application it is recommended to call `d2_flushframe` before stopping the peripheral.

## 4.2.18 Data Transfer Controller (r\_dtc)

### Modules

#### Functions

fsp_err_t	R_DTC_Open (transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg)
-----------	---

fsp_err_t	R_DTC_Reconfigure (transfer_ctrl_t *const p_api_ctrl, transfer_info_t *p_info)
-----------	--

fsp_err_t	R_DTC_Reset (transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers)
-----------	--

fsp_err_t	R_DTC_SoftwareStart (transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode)
-----------	---

```
fsp_err_t R_DTC_SoftwareStop (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DTC_Enable (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DTC_Disable (transfer_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_DTC_InfoGet (transfer_ctrl_t *const p_api_ctrl, transfer_properties_t
*const p_properties)
```

```
fsp_err_t R_DTC_Close (transfer_ctrl_t *const p_api_ctrl)
```

## Detailed Description

Driver for the DTC peripheral on RA MCUs. This module implements the [Transfer Interface](#).

## Overview

The Data Transfer Controller (DTC) transfers data from one memory location to another without using the CPU.

The DTC uses a RAM based vector table. Each entry in the vector table corresponds to an entry in the ISR vector table. When the DTC is triggered by an interrupt, it reads the DTC vector table, fetches the transfer information, and then executes the transfer. After the transfer is executed, the DTC writes the updated transfer info back to the location pointed to by the DTC vector table.

## Features

- Supports multiple transfer modes
  - Normal transfer
  - Repeat transfer
  - Block transfer
- Chain transfers
- Address increment, decrement or fixed modes
- Can be triggered by any event that has reserved a slot in the interrupt vector table.
  - Some exceptions apply, see the Event table in the Event Numbers section of the Interrupt Controller Unit chapter of the hardware manual
- Supports 1, 2, and 4 byte data units

## Configuration

### Build Time Configurations for r\_dtc

The following build time configurations are defined in fsp\_cfg/r\_dtc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

Linker section to keep DTC vector table      Manual Entry      .fsp\_dtc\_vector\_table      Section to place the DTC vector table.

### Configurations for Driver > Transfer > Transfer Driver on r\_dtc

This module can be added to the Stacks tab via New Stack > Driver > Transfer > Transfer Driver on r\_dtc .

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_transfer0	Module name.
Mode	<ul style="list-style-type: none"> <li>• Normal</li> <li>• Repeat</li> <li>• Block</li> </ul>	Normal	Select the transfer mode. Select the transfer mode. Normal: One transfer per activation, transfer ends after Number of Transfers; Repeat: One transfer per activation, Repeat Area address reset after Number of Transfers, transfer repeats until stopped; Block: Number of Blocks per activation, Repeat Area address reset after Number of Transfers, transfer ends after Number of Blocks.
Transfer Size	<ul style="list-style-type: none"> <li>• 1 Byte</li> <li>• 2 Bytes</li> <li>• 4 Bytes</li> </ul>	2 Bytes	Select the transfer size.
Destination Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the destination.
Source Address Mode	<ul style="list-style-type: none"> <li>• Fixed</li> <li>• Incremented</li> <li>• Decrementd</li> </ul>	Fixed	Select the address mode for the source.
Repeat Area (Unused in Normal Mode)	<ul style="list-style-type: none"> <li>• Destination</li> <li>• Source</li> </ul>	Source	Select the repeat area. Either the source or destination address resets to its initial value after completing Number of Transfers in Repeat or Block mode.
Destination Pointer	Manual Entry	NULL	Specify the transfer destination pointer.
Source Pointer	Manual Entry	NULL	Specify the transfer source pointer.

Interrupt Frequency	<ul style="list-style-type: none"> <li>• After all transfers have completed</li> <li>• After each transfer</li> </ul>	After all transfers have completed	Select to have interrupt after each transfer or after last transfer.
Number of Transfers	Value must be a non-negative integer	0	Specify the number of transfers.
Number of Blocks (Valid only in Block Mode)	Must be a valid non-negative integer with a maximum configurable value of 65536. Applicable only in Block Mode.	0	Specify the number of blocks to transfer in Block mode.
Activation Source	MCU Specific Options		Select the DTC transfer start event.

## Clock Configuration

The DTC peripheral module uses ICLK as the clock source. The ICLK frequency is set by using the **Clocks** tab of the RA Configuration editor prior to a build or by using the CGC module at runtime.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Transfer Modes

The DTC Module supports three modes of operation.

- **Normal Mode** - In normal mode, a single data unit is transferred every time an interrupt is received by the DTC. A data unit can be 1-byte, 2-bytes, or 4-bytes. The source and destination addresses can be fixed, increment or decrement to the next data unit after each transfer. A 16-bit counter (length) decrements after each transfer. When the counter reaches 0, transfers will no longer be triggered by the interrupt source and the CPU can be interrupted to signal that all transfers have finished.
- **Repeat Mode** - Repeat mode works the same way as normal mode, however the length is limited to an integer in the range[1,256]. When the transfer counter reaches 0, the counter is reset to its configured value and the repeat area (source or destination address) resets to its starting address and transfers will still be triggered by the interrupt.
- **Block Mode** - In block mode, the amount of data units transferred by each interrupt can be set to an integer in the range [1,256]. The number of blocks to transfer can also be configured to a 16-bit number. After each block transfer the repeat area (source or destination address) will reset to the original address and the other address will be incremented or decremented to the next block.

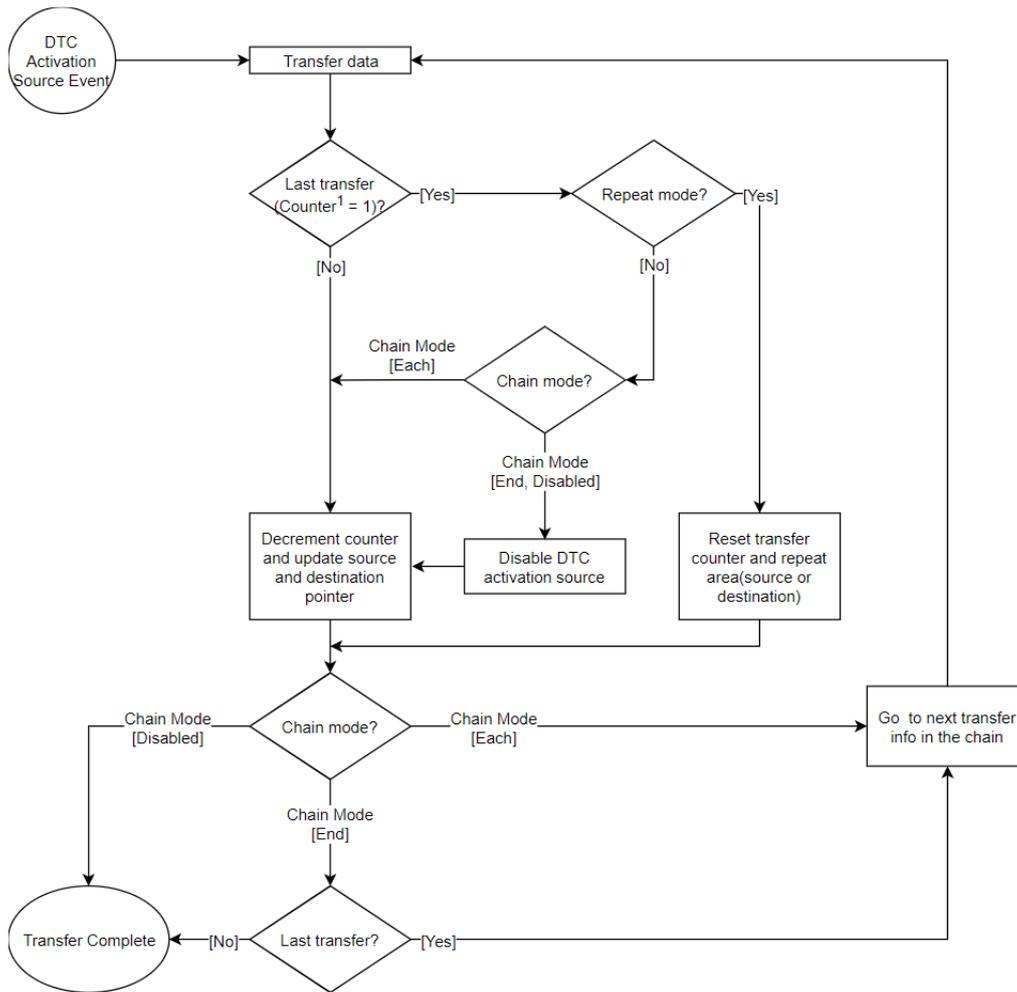
### Note

1. The source and destination address of the transfer must be aligned to the configured data unit.
2. In normal mode the length can be set to [0,65535]. When the length is set to 0, than the transaction will execute 65536 transfers not 0.

3. In block mode, num\_blocks can be set to [0,65535]. When the length is set to 0, than the transaction will execute 65536 transfers not 0.

### Chaining Transfers

Multiple transfers can be configured for the same interrupt source by specifying an array of transfer\_info\_t structs instead of just passing a pointer to one. In this configuration, every transfer\_info\_t struct must be configured for a chain mode except for the last one. There are two types of chain mode; CHAIN\_MODE\_EACH and CHAIN\_MODE\_END. If a transfer is configured in CHAIN\_MODE\_EACH then it triggers the next transfer in the chain after it completes each transfer. If a transfer is configured in CHAIN\_MODE\_END then it triggers the next transfer in the chain after it completes its last transfer.



1. Counter refers to transfer\_info\_t:length in normal and repeat mode and transfer\_info\_t:num\_blocks in block mode.

Figure 152: DTC Transfer Flowchart

### Selecting the DTC or DMAC

The Transfer API is implemented by both DTC and the DMAC so that applications can switch between the DTC and the DMAC. When selecting between them, consider these factors:

	DTC	DMAC
--	-----	------

Repeat Mode	<ul style="list-style-type: none"> <li>Repeats forever</li> <li>Max repeat size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Configurable number of repeats</li> <li>Max repeat size is 1024 x 4 bytes</li> </ul>
Block Mode	<ul style="list-style-type: none"> <li>Max block size is 256 x 4 bytes</li> </ul>	<ul style="list-style-type: none"> <li>Max block size is 1024 x 4 bytes</li> </ul>
Channels	<ul style="list-style-type: none"> <li>One instance per interrupt</li> </ul>	<ul style="list-style-type: none"> <li>MCU specific (8 channels or less)</li> </ul>
Chained Transfers	<ul style="list-style-type: none"> <li>Supported</li> </ul>	<ul style="list-style-type: none"> <li>Not Supported</li> </ul>
Software Trigger	<ul style="list-style-type: none"> <li>Must use the software ELC event</li> </ul>	<ul style="list-style-type: none"> <li>Has support for software trigger without using software ELC event</li> <li>Supports TRANSFER_START_MODE_SINGLE and TRANSFER_START_MODE_REPEAT</li> </ul>
Offset Address Mode	<ul style="list-style-type: none"> <li>Not supported</li> </ul>	<ul style="list-style-type: none"> <li>Supported</li> </ul>

### Additional Considerations

- The DTC requires a moderate amount of RAM (one `transfer_info_t` struct per open instance + `DTC_VECTOR_TABLE_SIZE`).
- The DTC stores transfer information in RAM and writes back to RAM after each transfer whereas the DMAC stores all transfer information in registers.
- When transfers are configured for more than one activation source, the DTC must fetch the transfer info from RAM on each interrupt. This can cause a higher latency between transfers.
- The DTC interrupts the CPU using the activation source's IRQ. Each DMAC channel has its own IRQ.

### Interrupts

The DTC and DMAC interrupts behave differently. The DTC uses the configured IELSR event IRQ as the interrupt source whereas each DMAC channel has its own IRQ.

The `transfer_info_t::irq` setting also behaves a little differently depending on which mode is selected.

### Normal Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	N/A
TRANSFER_IRQ_END	Interrupt after last transfer	Interrupt after last transfer

### Repeat Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each transfer	Interrupt after each repeat
TRANSFER_IRQ_END	Interrupt after each repeat	Interrupt after last transfer

## Block Mode

	DTC	DMAC
TRANSFER_IRQ_EACH	Interrupt after each block	Interrupt after each block
TRANSFER_IRQ_END	Interrupt after last block	Interrupt after last block

Note

$DTC\_VECTOR\_TABLE\_SIZE = (ICU\_NVIC\_IRQ\_SOURCES \times 4) \text{ Bytes}$

## Peripheral Interrupts and DTC

When an interrupt is configured to trigger DTC transfers, the peripheral ISR will trigger on the following conditions:

- Each transfer completed (transfer\_info\_t::irq = TRANSFER\_IRQ\_EACH)
- Last transfer completed (transfer\_info\_t::irq = TRANSFER\_IRQ\_END)

For example, if SCI1\_RXI is configured to trigger DTC transfers and a SCI1\_RXI event occurs, the interrupt will not fire until the DTC transfer is completed. If the DTC transfer\_info\_t::irq is configured to only interrupt on the last transfer, than no RXI interrupts will occur until the last transfer is completed.

Note

1. The DTC activation source must be enabled in the NVIC in order to trigger DTC transfers (Modules that are designed to integrate the R\_DTC module will automatically handle this).
2. The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

## Low Power Modes

DTCST must be set to 0 before transitioning to any of the following:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software Standby mode

Note

1. R\_LPM Module stops the DTC before entering deep software standby mode and software standby without snooze mode transition.
2. For more information see 18.9 and 18.10 in the RA6M3 manual R01UH0886EJ0100.

## Limitations

Developers should be aware of the following limitations when using the DTC:

- If the DTC is configured to service many different activation sources, the system could run in to performance issues due to memory contention. To address this issue, it is recommended that the DTC vector table and transfer information be moved to their own dedicated memory area (Ex: SRAM0, SRAM1, SRAMHS). This allows memory accesses from different BUS Masters (CPU, DTC, DMAC, EDMAC and Graphics IPs) to occur in parallel.

## Examples

## Basic Example

This is a basic example of minimal use of the DTC in an application.

```
void dtc_minimal_example (void)
{
    /* Open the transfer instance with initial configuration. */
    fsp_err_t err = R_DTC_Open(&g_transfer_ctrl, &g_transfer_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Enable the DTC to handle incoming transfer requests. */
    err = R_DTC_Enable(&g_transfer_ctrl);
    assert(FSP_SUCCESS == err);
}
```

## Data Structures

struct [dtc\\_extended\\_cfg\\_t](#)

struct [dtc\\_instance\\_ctrl\\_t](#)

## Macros

#define [DTC\\_MAX\\_NORMAL\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_REPEAT\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_BLOCK\\_TRANSFER\\_LENGTH](#)

#define [DTC\\_MAX\\_BLOCK\\_COUNT](#)

## Data Structure Documentation

### ◆ [dtc\\_extended\\_cfg\\_t](#)

struct <a href="#">dtc_extended_cfg_t</a>		
DTC transfer configuration extension. This extension is required.		
Data Fields		
IRQn_Type	activation_source	Select which IRQ will trigger the transfer.

### ◆ [dtc\\_instance\\_ctrl\\_t](#)

struct <a href="#">dtc_instance_ctrl_t</a>

Control block used by driver. DO NOT INITIALIZE - this structure will be initialized in [transfer\\_api\\_t::open](#).

## Macro Definition Documentation

### ◆ DTC\_MAX\_NORMAL\_TRANSFER\_LENGTH

```
#define DTC_MAX_NORMAL_TRANSFER_LENGTH
```

Max configurable number of transfers in NORMAL MODE

### ◆ DTC\_MAX\_REPEAT\_TRANSFER\_LENGTH

```
#define DTC_MAX_REPEAT_TRANSFER_LENGTH
```

Max number of transfers per repeat for REPEAT MODE

### ◆ DTC\_MAX\_BLOCK\_TRANSFER\_LENGTH

```
#define DTC_MAX_BLOCK_TRANSFER_LENGTH
```

Max number of transfers per block in BLOCK MODE

### ◆ DTC\_MAX\_BLOCK\_COUNT

```
#define DTC_MAX_BLOCK_COUNT
```

Max configurable number of blocks to transfer in BLOCK MODE

## Function Documentation

◆ **R\_DTC\_Open()**

```
fsp_err_t R_DTC_Open ( transfer_ctrl_t *const p_api_ctrl, transfer_cfg_t const *const p_cfg )
```

Configure the vector table if it hasn't been configured, enable the Module and copy the pointer to the transfer info into the DTC vector table. Implements [transfer\\_api\\_t::open](#).

Example:

```
/* Open the transfer instance with initial configuration. */
fsp_err_t err = R_DTC_Open(&g_transfer_ctrl, &g_transfer_cfg);
```

**Return values**

FSP_SUCCESS	Successful open. Transfer transfer info pointer copied to DTC Vector table. Module started. DTC vector table configured.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_UNSUPPORTED	Address Mode Offset is selected.
FSP_ERR_ALREADY_OPEN	The control structure is already opened.
FSP_ERR_IN_USE	The index for this IRQ in the DTC vector table is already configured.
FSP_ERR_IRQ_BSP_DISABLED	The IRQ associated with the activation source is not enabled in the BSP.

◆ **R\_DTC\_Reconfigure()**

```
fsp_err_t R_DTC_Reconfigure ( transfer_ctrl_t *const p_api_ctrl, transfer_info_t * p_info )
```

Copy pointer to transfer info into the DTC vector table and enable transfer in ICU. Implements [transfer\\_api\\_t::reconfigure](#).

**Return values**

FSP_SUCCESS	Transfer is configured and will start when trigger occurs.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_NOT_ENABLED	Transfer source address is NULL or is not aligned correctly. Transfer destination address is NULL or is not aligned correctly.

**Note**

*p\_info must persist until all transfers are completed.*

◆ **R\_DTC\_Reset()**

```
fsp_err_t R_DTC_Reset ( transfer_ctrl_t *const p_api_ctrl, void const *volatile p_src, void *volatile p_dest, uint16_t const num_transfers )
```

Reset transfer source, destination, and number of transfers. Implements [transfer\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Transfer reset successfully (transfers are enabled).
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_NOT_ENABLED	Transfer source address is NULL or is not aligned correctly. Transfer destination address is NULL or is not aligned correctly.

◆ **R\_DTC\_SoftwareStart()**

```
fsp_err_t R_DTC_SoftwareStart ( transfer_ctrl_t *const p_api_ctrl, transfer_start_mode_t mode )
```

Placeholder for unsupported softwareStart function. Implements [transfer\\_api\\_t::softwareStart](#).

**Return values**

FSP_ERR_UNSUPPORTED	DTC software start is not supported.
---------------------	--------------------------------------

◆ **R\_DTC\_SoftwareStop()**

```
fsp_err_t R_DTC_SoftwareStop ( transfer_ctrl_t *const p_api_ctrl)
```

Placeholder for unsupported softwareStop function. Implements [transfer\\_api\\_t::softwareStop](#).

**Return values**

FSP_ERR_UNSUPPORTED	DTC software stop is not supported.
---------------------	-------------------------------------

◆ **R\_DTC\_Enable()**

```
fsp_err_t R_DTC_Enable ( transfer_ctrl_t *const p_api_ctrl)
```

Enable transfers on this activation source. Implements [transfer\\_api\\_t::enable](#).

Example:

```
/* Enable the DTC to handle incoming transfer requests. */
err = R_DTC_Enable(&g_transfer_ctrl);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Transfers will be triggered by the activation source
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_UNSUPPORTED	Address Mode Offset is selected.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.

◆ **R\_DTC\_Disable()**

```
fsp_err_t R_DTC_Disable ( transfer_ctrl_t *const p_api_ctrl)
```

Disable transfer on this activation source. Implements [transfer\\_api\\_t::disable](#).

**Return values**

FSP_SUCCESS	Transfers will not occur on activation events.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

◆ **R\_DTC\_InfoGet()**

```
fsp_err_t R_DTC_InfoGet ( transfer_ctrl_t *const p_api_ctrl, transfer_properties_t *const p_properties )
```

Provides information about this transfer. Implements `transfer_api_t::infoGet`.

**Return values**

FSP_SUCCESS	p_info updated with current instance information.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.
FSP_ERR_ASSERTION	An input parameter is invalid.

◆ **R\_DTC\_Close()**

```
fsp_err_t R_DTC_Close ( transfer_ctrl_t *const p_api_ctrl)
```

Disables DTC activation in the ICU, then clears transfer data from the DTC vector table. Implements `transfer_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_DTC_Open to initialize the control block.

**4.2.19 Event Link Controller (r\_elc)**

## Modules

**Functions**

```
fsp_err_t R_ELC_Open (elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_ELC_Close (elc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_ELC_SoftwareEventGenerate (elc_ctrl_t *const p_ctrl, elc_software_event_t event_number)
```

```
fsp_err_t R_ELC_LinkSet (elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral,
```

`elc_event_t` signal)

`fsp_err_t` `R_ELC_LinkBreak` (`elc_ctrl_t *const p_ctrl`, `elc_peripheral_t peripheral`)

`fsp_err_t` `R_ELC_Enable` (`elc_ctrl_t *const p_ctrl`)

`fsp_err_t` `R_ELC_Disable` (`elc_ctrl_t *const p_ctrl`)

## Detailed Description

Driver for the ELC peripheral on RA MCUs. This module implements the [ELC Interface](#).

## Overview

The event link controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect (link) them to different modules, allowing direct cooperation between the modules without central processing unit (CPU) intervention. The conceptual diagram below illustrates a potential setup where a pin interrupt triggers a timer which later triggers an ADC conversion and CTSU scan, while at the same time a serial communication interrupt automatically starts a data transfer. These tasks would be automatically handled without the need for polling or interrupt management.

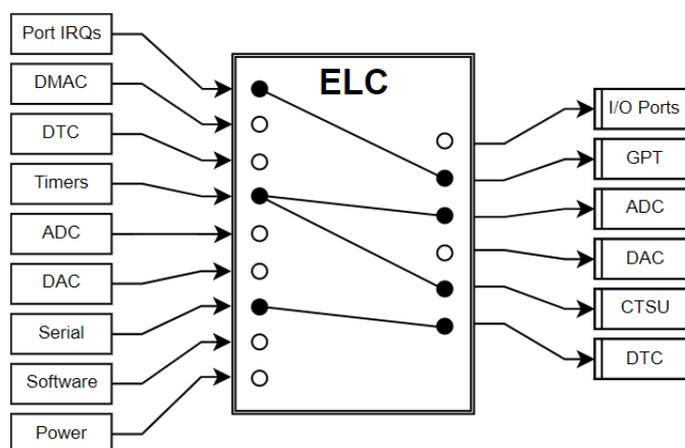


Figure 153: Event Link Controller Conceptual Diagram

In essence, the ELC is an array of multiplexers to route a wide variety of interrupt signals to a subset of peripheral functions. Events are linked by setting the multiplexer for the desired function to the desired signal (through `R_ELC_LinkSet`). The diagram below illustrates one peripheral output of the ELC. In this example, a conversion start is triggered for ADC0 Group A when the GPT0 counter overflows:

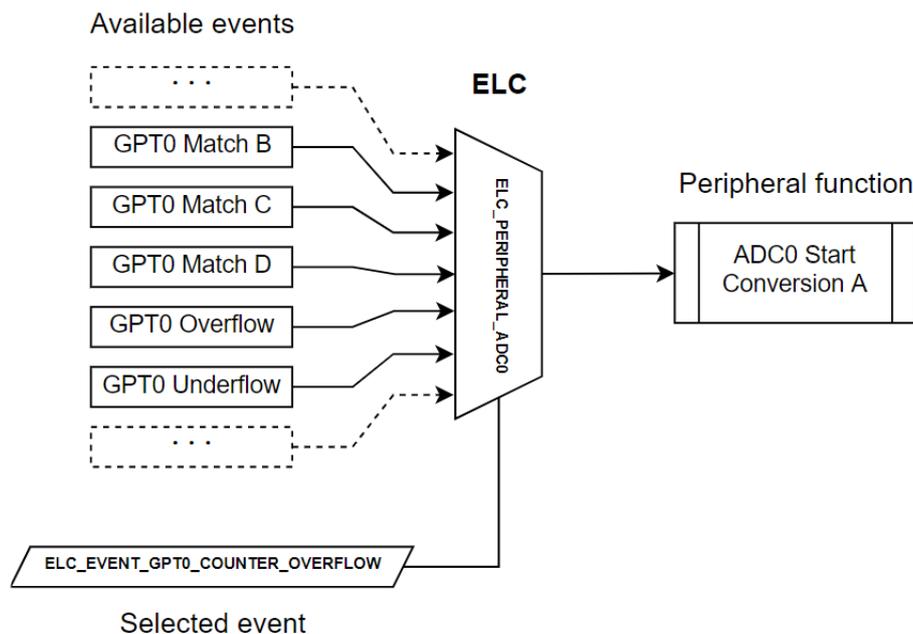


Figure 154: ELC Example

## Features

The ELC HAL module can perform the following functions:

- Initialize the ELC to a pre-defined set of links
- Create an event link between two blocks
- Break an event link between two blocks
- Generate one of two software events that interrupt the CPU
- Globally enable or disable event links

A variety of functions can be activated via events, including:

- General-purpose timer (GPT) control
- ADC and DAC conversion start
- Synchronized I/O port output (ports 1-4 only)
- Capacitive touch unit (CTSU) measurement activation

### Note

*The available sources and peripherals may differ between devices. A full list of selectable peripherals and events is available in the User's Manual for your device.*

*Some peripherals have specific settings related to ELC event generation and/or reception. Details on how to enable event functionality for each peripheral are located in the usage notes for the related module(s) as well as in the User's Manual for your device.*

## Configuration

### Note

*Event links will be automatically generated based on the selections made in module properties. To view the currently linked events check the [Event Links tab in the RA Configuration editor](#).*

*Calling [R\\_ELC\\_Open](#) followed by [R\\_ELC\\_Enable](#) will automatically link all events shown in the Event Links tab.*

To manually link an event to a peripheral at runtime perform the following steps:

1. Configure the operation of the destination peripheral (including any configuration necessary to receive events)
2. Use `R_ELC_LinkSet` to set the desired event link to the peripheral
3. Use `R_ELC_Enable` to enable transmission of event signals
4. Configure the signaling module to output the desired event (typically an interrupt)

To disable the event, either use `R_ELC_LinkBreak` to clear the link for a specific event or `R_ELC_Disable` to globally disable event linking.

#### Note

*The ELC module needs no pin, clocking or interrupt configuration; it is merely a mechanism to connect signals between peripherals. However, when linking I/O Ports via the ELC the relevant I/O pins need to be configured as inputs or outputs.*

### Build Time Configurations for r\_elc

The following build time configurations are defined in `fsp_cfg/r_elc_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > System > ELC Driver on r\_elc

This module can be added to the Stacks tab via New Stack > Driver > System > ELC Driver on r\_elc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	ELC instance name must be <code>g_elc</code> to match <code>elc_cfg_t</code> data structure created in <code>elc_data.c</code>	<code>g_elc</code>	Module name. Fixed to <code>g_elc</code> .

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the ELC:

- To link events it is necessary for the ELC and the related modules to be enabled. The ELC cannot operate if the related modules are in the module stop state or the MCU is in a low power consumption mode for which the module is stopped.
- If two modules are linked across clock domains there may be a 1 to 2 cycle delay between event signaling and reception. The delay timing is based on the frequency of the slowest clock.

## Examples

## Basic Example

Below is a basic example of minimal use of event linking in an application.

```
/* This struct is automatically generated based on the events configured by
peripherals in the RA Configuration editor. */
static const elc_cfg_t g_elc_cfg =
{
    .link[ELC_PERIPHERAL_GPT_A] = ELC_EVENT_ICU_IRQ0,
    .link[ELC_PERIPHERAL_IOPORT1] = ELC_EVENT_GPT4_COUNTER_OVERFLOW
};

void elc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the software and sets the links defined in the control structure. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Create or modify a link between a peripheral function and an event source. */
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,
ELC_EVENT_GPT4_COUNTER_OVERFLOW);
    assert(FSP_SUCCESS == err);
    /* Globally enable event linking in the ELC. */
    err = R_ELC_Enable(&g_elc_ctrl);
    assert(FSP_SUCCESS == err);
}
```

## Software-Generated Events

This example demonstrates how to use a software-generated event to signal a peripheral. This can be useful when the desired event source is not supported by the ELC hardware.

```
/* Interrupt handler for peripheral event not supported by the ELC */
void peripheral_isr (void)
{
    fsp_err_t err;
    /* Generate an event signal through software to the linked peripheral. */
```

```
    err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);
    assert(FSP_SUCCESS == err);
}
void elc_software_event (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Open the module. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Link ADC0 conversion start to software event 0. */
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,
ELC_EVENT_ELC_SOFTWARE_EVENT_0);
    assert(FSP_SUCCESS == err);
    while (true)
    {
        /* Application code here. */
    }
}
```

## Data Structures

struct [elc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [elc\\_instance\\_ctrl\\_t](#)

struct [elc\\_instance\\_ctrl\\_t](#)

ELC private control block. DO NOT MODIFY. Initialization occurs when [R\\_ELC\\_Open\(\)](#) is called.

## Function Documentation

◆ **R\_ELC\_Open()**

```
fsp_err_t R_ELC_Open ( elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg )
```

Initialize all the links in the Event Link Controller. Implements `elc_api_t::open`

The configuration structure passed in to this function includes links for every event source included in the ELC and sets them all at once. To set or clear an individual link use `R_ELC_LinkSet` and `R_ELC_LinkBreak` respectively.

Example:

```
/* Initializes the software and sets the links defined in the control structure. */
err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	p_ctrl or p_cfg was NULL
FSP_ERR_ALREADY_OPEN	The module is currently open

◆ **R\_ELC\_Close()**

```
fsp_err_t R_ELC_Close ( elc_ctrl_t *const p_ctrl)
```

Globally disable ELC linking. Implements `elc_api_t::close`

**Return values**

FSP_SUCCESS	The ELC was successfully disabled
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_SoftwareEventGenerate()**

```
fsp_err_t R_ELC_SoftwareEventGenerate ( elc_ctrl_t *const p_ctrl, elc_software_event_t
event_number )
```

Generate a software event in the Event Link Controller. Implements `elc_api_t::softwareEventGenerate`

Example:

```
/* Generate an event signal through software to the linked peripheral. */
err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	Invalid event number or p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_LinkSet()**

```
fsp_err_t R_ELC_LinkSet ( elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal )
```

Create a single event link. Implements `elc_api_t::linkSet`

Example:

```
/* Create or modify a link between a peripheral function and an event source. */
err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0,
ELC_EVENT_GPT4_COUNTER_OVERFLOW);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Initialization was successful
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_LinkBreak()**

```
fsp_err_t R_ELC_LinkBreak ( elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral )
```

Break an event link. Implements `elc_api_t::linkBreak`

**Return values**

FSP_SUCCESS	Event link broken
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_Enable()**

```
fsp_err_t R_ELC_Enable ( elc_ctrl_t *const p_ctrl)
```

Enable the operation of the Event Link Controller. Implements `elc_api_t::enable`

**Return values**

FSP_SUCCESS	ELC enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_ELC\_Disable()**

```
fsp_err_t R_ELC_Disable ( elc_ctrl_t *const p_ctrl)
```

Disable the operation of the Event Link Controller. Implements `elc_api_t::disable`

**Return values**

FSP_SUCCESS	ELC disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

**4.2.20 Ethernet (r\_ether)**

## Modules

**Functions**

```
fsp_err_t R_ETHER_Open (ether_ctrl_t *const p_ctrl, ether_cfg_t const *const
```

p\_cfg)

After ETHERC, EDMAC and PHY-LSI are reset in software, an auto negotiation of PHY-LSI is begun. Afterwards, the link signal change interrupt is permitted. Implements [ether\\_api\\_t::open](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_Close](#) (ether\_ctrl\_t \*const p\_ctrl)

Disables interrupts. Removes power and releases hardware lock. Implements [ether\\_api\\_t::close](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_Read](#) (ether\_ctrl\_t \*const p\_ctrl, void \*const p\_buffer, uint32\_t \*const length\_bytes)

Receive Ethernet frame. Receives data to the location specified by the pointer to the receive buffer. In zero copy mode, the address of the receive buffer is returned. In non zero copy mode, the received data in the internal buffer is copied to the pointer passed by the argument. Implements [ether\\_api\\_t::read](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_BufferRelease](#) (ether\_ctrl\_t \*const p\_ctrl)

Move to the next buffer in the circular receive buffer list. Implements [ether\\_api\\_t::bufferRelease](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_RxBufferUpdate](#) (ether\_ctrl\_t \*const p\_ctrl, void \*const p\_buffer)

Change the buffer pointer of the current rx buffer descriptor. Implements [ether\\_api\\_t::rxBufferUpdate](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_Write](#) (ether\_ctrl\_t \*const p\_ctrl, void \*const p\_buffer, uint32\_t const frame\_length)

Transmit Ethernet frame. Transmits data from the location specified by the pointer to the transmit buffer, with the data size equal to the specified frame length. In the non zero copy mode, transmits data after being copied to the internal buffer. Implements [ether\\_api\\_t::write](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_LinkProcess](#) (ether\_ctrl\_t \*const p\_ctrl)

The Link up processing, the Link down processing, and the magic packet detection processing are executed. Implements [ether\\_api\\_t::linkProcess](#). [More...](#)

fsp\_err\_t [R\\_ETHER\\_WakeOnLANEnable](#) (ether\_ctrl\_t \*const p\_ctrl)

The setting of ETHERC is changed from normal sending and

receiving mode to magic packet detection mode. Implements [ether\\_api\\_t::wakeOnLANEnable](#). [More...](#)

`fsp_err_t R_ETHER_TxStatusGet(ether_ctrl_t *const p_ctrl, void *const p_buffer_address)`

## Detailed Description

Driver for the Ethernet peripheral on RA MCUs. This module implements the [Ethernet Interface](#).

## Overview

This module performs Ethernet frame transmission and reception using an Ethernet controller and an Ethernet DMA controller.

## Features

The Ethernet module supports the following features:

- Transmit/receive processing
- Optional zero-copy buffering
- Callback function with returned event code
- Magic packet detection mode support
- Auto negotiation support
- Flow control support
- Multicast filtering support
- Broadcast filtering support
- Promiscuous mode support

## Configuration

### Build Time Configurations for r\_ether

The following build time configurations are defined in `fsp_cfg/r_ether_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
ET0_LINKSTA Pin Status Flag	<ul style="list-style-type: none"> <li>• Fall -&gt; Rise</li> <li>• Rise -&gt; Fall</li> </ul>	Fall -> Rise	Specify the polarity of the link signal output by the PHY-LSI. When 0 is specified, link-up and link-down correspond respectively to the fall and rise of the LINKSTA signal. When 1 is specified, link-up and link-down correspond respectively to the rise

and fall of the LINKSTA signal.

Link Signal Change Flag	<ul style="list-style-type: none"> <li>• Unused</li> <li>• Used</li> </ul>	Unused	Use LINKSTA signal for detect link status changes 0 = unused (use PHY-LSI status register) 1 = use (use LINKSTA signal)
-------------------------	--	--------	---

### Configurations for Driver > Network > Ethernet Driver on r\_ether

This module can be added to the Stacks tab via New Stack > Driver > Network > Ethernet Driver on r\_ether.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_ether0	Module name.
General > Channel	0	0	Select the ether channel number.
General > MAC address	Must be a valid MAC address	00:11:22:33:44:55	MAC address of this channel.
General > Zero-copy Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable zero-copy mode.
General > Flow control functionality	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable flow control.
Filters > Multicast Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Enable or disable multicast frame reception.
Filters > Promiscuous Mode	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable this option to receive packets addressed to other NICs.
Filters > Broadcast filter	Must be a valid non-negative integer with maximum configurable value of 65535.	0	Limit of the number of broadcast frames received continuously
Buffers > Number of TX buffer	Must be an integer from 1 to 8	1	Number of transmit buffers
Buffers > Number of RX buffer	Must be an integer from 1 to 8	1	Number of receive buffers
Buffers > Allocate RX buffer	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Allocates the RX buffer when generating the configuration structure
Buffers > Buffer size	Must be at least 1514 which is the maximum Ethernet frame size.	1514	Size of Ethernet buffer

Buffers > Padding size	<ul style="list-style-type: none"> <li>• Disable</li> <li>• 1 Byte</li> <li>• 2 Bytes</li> <li>• 3 Bytes</li> </ul>	Disable	The padding size that is automatically inserted into the received packets
Buffers > Padding offset	Must be less than 64 bytes.	0	The offset into a receive buffer to insert padding bytes.
Interrupts > Interrupt priority	MCU Specific Options		Select the EDMAC interrupt priority.
Interrupts > Callback	Name must be a valid C symbol	NULL	Callback provided when an ISR occurs

## Interrupt Configuration

The first [R\\_ETHER\\_Open](#) function call sets EINT interrupts. The user could provide callback function which would be invoked when EINT interrupt handler has been completed. The callback arguments will contain information about a channel number, the ETHERC and EDMAC status, the event code, and a pointer to the user defined context.

## Callback Configuration

The user could provide callback function which would be invoked when either a magic packet or a link signal change is detected. When the callback function is called, a variable in which the channel number for which the detection occurred and a constant shown in Table 2.4 are stored is passed as an argument. If the value of this argument is to be used outside the callback function, its value should be copied into, for example, a global variable.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA
RA6M5	PCLKA

### Note

1. When using ETHERC, the PCLKA frequency is in the range  $12.5 \text{ MHz} \leq PCLKA \leq 120 \text{ MHz}$ .
2. When using ETHERC,  $PCLKA = ICLK$ .

## Pin Configuration

To use the Ethernet module, input/output signals of the peripheral function have to be allocated to pins with the multi-function pin controller (MPC). Please perform the pin setting before calling the [R\\_ETHER\\_Open](#) function.

## Usage Notes

### Ethernet Frame Format

The Ethernet module supports the Ethernet II/IEEE 802.3 frame format.

#### Frame Format for Data Transmission and Reception

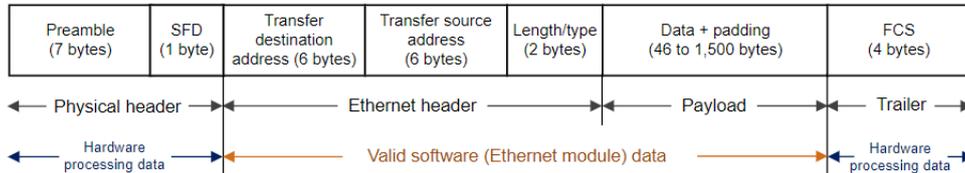


Figure 155: Frame Format Image

The preamble and SFD signal the start of an Ethernet frame. The FCS contains the CRC of the Ethernet frame and is calculated on the transmitting side. When data is received the CRC value of the frame is calculated in hardware, and the Ethernet frame is discarded if the values do not match. When the hardware determines that the data is normal, the valid range of receive data is: (transmission destination address) + (transmission source address) + (length/type) + (data).

### PAUSE Frame Format

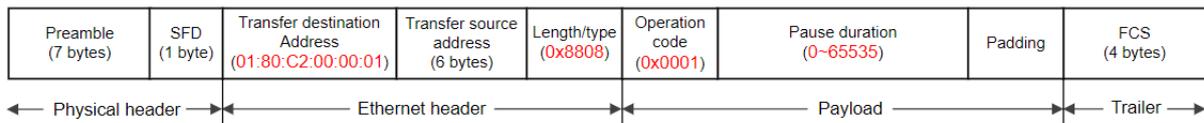


Figure 156: Pause Frame Format Image

The transmission destination address is specified as 01:80:C2:00:00:01 (a multicast address reserved for PAUSE frames). At the start of the payload the length/type is specified as 0x8808 and the operation code as 0x0001. The pause duration in the payload is specified by the value of the automatic PAUSE (AP) bits in the automatic PAUSE frame setting register (APR), or the manual PAUSE time setting (MP) bits in the manual PAUSE frame setting register (MPR).

### Magic Packet Frame Format

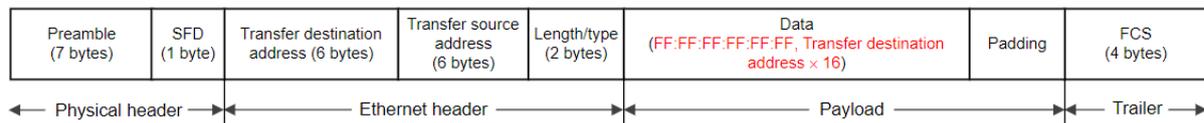


Figure 157: Magic Packet Frame Format Image

In a Magic Packet, the value FF:FF:FF:FF:FF:FF followed by the transmission destination address repeated 16 times is inserted somewhere in the Ethernet frame data.

### Limitations

#### Memory alignment limitation for Ethernet buffer

The Ethernet Driver has several alignment constraints:

- 16-byte alignment for the descriptor
- 32-byte aligned read buffer for `R_ETHER_RxBufferUpdate` when zero copy mode is enabled

### Functional limitations in TrustZone Security Extensions

The Ethernet Driver has several security constraints:

MCU	Has Security Extension	Support Flat project	Support TZ project	
			Secure	Non-Secure
RA6M2	-	x	-	-
RA6M3	-	x	-	-
RA6M4	- *1	x	-	x
RA6M5	- *1	x	-	x

*Note*

1. *ETHERC/EDMAC is always Non-secure peripheral in this MCU.*

## Examples

### ETHER Basic Example

This is a basic example of minimal use of the ETHER in an application.

*Note*

*In this example zero-copy mode is disabled and there are no restrictions on buffer alignment.*

```
#define ETHER_EXAMPLE_MAXIMUM_ETHERNET_FRAME_SIZE (1514)
#define ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE (60)
#define ETHER_EXAMPLE_SOURCE_MAC_ADDRESS 0x74, 0x90, 0x50, 0x00, 0x79, 0x01
#define ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS 0x74, 0x90, 0x50, 0x00, 0x79, 0x02
#define ETHER_EXAMPLE_FRAME_TYPE 0x00, 0x2E
#define ETHER_EXAMPLE_PAYLOAD 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
0x00, \
    0x00, \
    0x00, \
    0x00, \

/* Receive data buffer */
static uint8_t gp_read_buffer[ETHER_EXAMPLE_MAXIMUM_ETHERNET_FRAME_SIZE] = {0};
/* Transmit data buffer */
```

```
static uint8_t gp_send_data[ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE] =
{
    ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS, /* Destination MAC address */
    ETHER_EXAMPLE_SOURCE_MAC_ADDRESS,      /* Source MAC address */
    ETHER_EXAMPLE_FRAME_TYPE,              /* Type field */
    ETHER_EXAMPLE_PAYLOAD                   /* Payload value (46byte) */
};

void ether_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Source MAC Address */
    static uint8_t mac_address_source[6] = {ETHER_EXAMPLE_SOURCE_MAC_ADDRESS};
    uint32_t read_data_size = 0;
    g_ether0_cfg.p_mac_address = mac_address_source;
    /* Open the ether instance with initial configuration. */
    err = R_ETHER_Open(&g_ether0_ctrl, &g_ether0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    do
    {
        /* When the Ethernet link status read from the PHY-LSI Basic Status register is link-
up,
        * Initializes the module and make auto negotiation. */
        err = R_ETHER_LinkProcess(&g_ether0_ctrl);
        } while (FSP_SUCCESS != err);
    /* Transmission is non-blocking. */
    /* User data copy to internal buffer and is transferred by DMA in the background. */
    err = R_ETHER_Write(&g_ether0_ctrl, (void *) gp_send_data, sizeof(gp_send_data));
    assert(FSP_SUCCESS == err);
    /* received data copy to user buffer from internal buffer. */
    err = R_ETHER_Read(&g_ether0_ctrl, (void *) gp_read_buffer, &read_data_size);
    assert(FSP_SUCCESS == err);
    /* Disable transmission and receive function and close the ether instance. */
    R_ETHER_Close(&g_ether0_ctrl);
}
```

```
}
```

## ETHER Advanced Example

The example demonstrates using send and receive function in zero copy mode. Transmit buffers must be 32-byte aligned and the receive buffer must be released once its contents have been used.

```
#define ETHER_EXAMPLE_FLAG_ON (1U)
#define ETHER_EXAMPLE_FLAG_OFF (0U)
#define ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK (1UL << 18)
#define ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK (1UL << 21)
#define ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK (1UL << 1)
#define ETHER_EXAMPLE_ALIGNMENT_32_BYTE (32)

static volatile uint32_t g_example_receive_complete = 0;
static volatile uint32_t g_example_transfer_complete = 0;
static volatile uint32_t g_example_magic_packet_done = 0;
static uint8_t gp_send_data_internal[ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE] =
{
    ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS, /* Destination MAC address */
    ETHER_EXAMPLE_SOURCE_MAC_ADDRESS,      /* Source MAC address */
    ETHER_EXAMPLE_FRAME_TYPE,              /* Type field */
    ETHER_EXAMPLE_PAYLOAD                  /* Payload value (46byte) */
};

void ether_example_callback (ether_callback_args_t * p_args) {
    switch (p_args->event)
    {
    case ETHER_EVENT_INTERRUPT:
        {
            if (ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK == (p_args->status_ecsr &
ETHER_EXAMPLE_ETHER_ISR_EC_MPD_MASK))
            {
                g_example_magic_packet_done = ETHER_EXAMPLE_FLAG_ON;
            }

            if (ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK == (p_args->status_eesr &
ETHER_EXAMPLE_ETHER_ISR_EE_TC_MASK))
```

```
    {
        g_example_transfer_complete = ETHER_EXAMPLE_FLAG_ON;
    }

    if (ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK == (p_args->status_eesr &
ETHER_EXAMPLE_ETHER_ISR_EE_FR_MASK))
    {
        g_example_receive_complete = ETHER_EXAMPLE_FLAG_ON;
    }

    break;
}
default:
    {
    }
}
}

void ether_advanced_use_internal_buffer_example (void) {
    fsp_err_t err = FSP_SUCCESS;
    /* Source MAC Address */
    static uint8_t mac_address_source[6] = {ETHER_EXAMPLE_SOURCE_MAC_ADDRESS};
    static uint8_t * p_read_buffer_nocopy;
    uint32_t      read_data_size = 0;
    g_ether0_cfg.p_mac_address = mac_address_source;
    g_ether0_cfg.zerocopy      = ETHER_ZEROCOPY_ENABLE;
    g_ether0_cfg.p_callback = (void (*)(ether_callback_args_t
*))ether_example_callback;
    /* Open the ether instance with initial configuration. */
    err = R_ETHER_Open(&g_ether0_ctrl, &g_ether0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    do
    {
        /* When the Ethernet link status read from the PHY-LSI Basic Status register is link-
up,
        * Initializes the module and make auto negotiation. */

```

```
    err = R_ETHER_LinkProcess(&g_ether0_ctrl);
} while (FSP_SUCCESS != err);
/* Set user buffer to TX descriptor and enable transmission. */
err = R_ETHER_Write(&g_ether0_ctrl, (void *) gp_send_data_internal, sizeof
(gp_send_data_internal));
if (FSP_SUCCESS == err)
{
/* Wait for the transmission to complete. */
/* Data array should not change in zero copy mode until transfer complete. */
while (ETHER_EXAMPLE_FLAG_ON != g_example_transfer_complete)
{
;
}
}
/* Get receive buffer from RX descriptor. */
err = R_ETHER_Read(&g_ether0_ctrl, (void *) &p_read_buffer_nocopy,
&read_data_size);
assert(FSP_SUCCESS == err);
/* Process received data here */
/* Release receive buffer to RX descriptor. */
err = R_ETHER_BufferRelease(&g_ether0_ctrl);
assert(FSP_SUCCESS == err);
/* Disable transmission and receive function and close the ether instance. */
R_ETHER_Close(&g_ether0_ctrl);
}
```

```
#define ETHER_EXAMPLE_ALIGNMENT_32_BYTE (32)
#define ETHER_EXAMPLE_ETHERNET_FRAME_PAYLOAD_OFFSET (14)
/* The data buffer must be 32-byte aligned when using zero copy mode. */
static uint8_t gp_send_data_external[ETHER_EXAMPLE_TRANSMIT_ETHERNET_FRAME_SIZE] =
{
    ETHER_EXAMPLE_DESTINATION_MAC_ADDRESS, /* Destination MAC address */
    ETHER_EXAMPLE_SOURCE_MAC_ADDRESS,     /* Source MAC address */
    ETHER_EXAMPLE_FRAME_TYPE,             /* Type field */
}
```

```
ETHER_EXAMPLE_PAYLOAD                                /* Payload value (46byte) */
};
typedef struct st_buffer_node
{
    uint8_t          * p_buffer;
    struct st_buffer_node * p_next;
} buffer_node_t;
void ether_advanced_use_external_buffer_example (void) {
    fsp_err_t err = FSP_SUCCESS;
    /* Source MAC Address */
    uint8_t mac_address_source[6] = {ETHER_EXAMPLE_SOURCE_MAC_ADDRESS};
    uint8_t * p_tx_buffer          = NULL;
    uint8_t * p_rx_buffer          = NULL;
    uint8_t * p_rx_allocate_buffer = NULL;
    uint8_t * p_tx_last_sent_buffer = NULL;
    buffer_node_t * p_tx_buffer_head;
    buffer_node_t * p_tx_buffer_tail;
    uint32_t read_data_size = 0;
    uint8_t i;
    g_ether0_cfg.p_mac_address = mac_address_source;
    g_ether0_cfg.zerocopy      = ETHER_ZEROCOPY_ENABLE;
    g_ether0_cfg.pp_ether_buffers = NULL;
    /* Create ring buffer structure to manage transmit buffer.*/
    p_tx_buffer_head = (buffer_node_t *) malloc(sizeof(buffer_node_t));
    p_tx_buffer_tail = p_tx_buffer_head;
    for (i = 0; i < g_ether0_cfg.num_tx_descriptors - 1; i++)
    {
        p_tx_buffer_tail->p_buffer = NULL;
        p_tx_buffer_tail->p_next   = (buffer_node_t *) malloc(sizeof(buffer_node_t));
        p_tx_buffer_tail          = p_tx_buffer_tail->p_next;
    }
    p_tx_buffer_tail->p_buffer = NULL;
    p_tx_buffer_tail->p_next   = p_tx_buffer_head;
    /* Open the ether instance with initial configuration. */
```

```
err = R_ETHER_Open(&g_ether0_ctrl, &g_ether0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

i = 0;
/* Initialize receive buffer in Ethernet driver. */
while (i < g_ether0_cfg.num_rx_descriptors)
{
if (posix_memalign((void **) &p_rx_allocate_buffer,
ETHER_EXAMPLE_ALIGNMENT_32_BYTE,
g_ether0_cfg.ether_buffer_size * sizeof(char)))
{
/* Set receive buffer to Ethernet driver. */
err = R_ETHER_RxBufferUpdate(&g_ether0_ctrl, (void *)
p_rx_allocate_buffer);
if (FSP_SUCCESS == err)
{
i++;
}
}
else
{
assert(0);
}
}
do
{
/* When the Ethernet link status read from the PHY-LSI Basic Status register is link-
up,
* Initializes the module and make auto negotiation. */
err = R_ETHER_LinkProcess(&g_ether0_ctrl);
} while (FSP_SUCCESS != err);
while (1)
{
if (NULL == p_tx_buffer_tail->p_buffer)
```

```
{
/* Allocate memory to transmit buffer */
    p_tx_buffer = (uint8_t *) malloc(sizeof(gp_send_data_external));
/* Process transmit data here. */
    memcpy(p_tx_buffer, gp_send_data_external, sizeof
(gp_send_data_external));
    gp_send_data_external[ETHER_EXAMPLE_ETHERNET_FRAME_PAYLOAD_OFFSET]++;
/* Set user buffer to TX descriptor and enable transmission. */
    err = R_ETHER_Write(&g_ether0_ctrl, (void *) gp_send_data_external,
sizeof(gp_send_data_external));
/* Register transmit buffer to ring buffer. */
    if (FSP_SUCCESS == err)
    {
        p_tx_buffer_tail->p_buffer = p_tx_buffer;
        p_tx_buffer_tail        = p_tx_buffer_tail->p_next;
    }
else
    {
/* Release transmit buffer. */
        free(p_tx_buffer);
    }
}
/* Get receive buffer from RX descriptor. */
    err = R_ETHER_Read(&g_ether0_ctrl, (void *) &p_rx_buffer, &read_data_size);
if (FSP_SUCCESS == err)
    {
/* Allocate new receive buffer and update receive buffer to RX descriptor. */
if (0 == posix_memalign((void **) &p_rx_allocate_buffer,
                        ETHER_EXAMPLE_ALIGNMENT_32_BYTE,
                        g_ether0_cfg.ether_buffer_size * sizeof(char)))
    {
R_ETHER_RxBufferUpdate(&g_ether0_ctrl, p_rx_allocate_buffer);
    }
else
```

```
    {
        assert(0);
    }
/* Process received data here. */
/* Release receive buffer. */
    free(p_rx_buffer);
}
/* Release all transmitted buffer from the ring buffer. */
if (FSP_SUCCESS == R_ETHER_TxStatusGet(&g_ether0_ctrl, (void *)
&p_tx_last_sent_buffer))
    {
        buffer_node_t * p_tx_buffer_current = p_tx_buffer_head;
for (i = 0; i < g_ether0_cfg.num_tx_descriptors; i++)
    {
if (p_tx_last_sent_buffer == p_tx_buffer_current->p_buffer)
    {
do
    {
        free(p_tx_buffer_head->p_buffer);
        p_tx_buffer_head->p_buffer = NULL;
        p_tx_buffer_head          = p_tx_buffer_head->p_next;
    } while (p_tx_buffer_head != p_tx_buffer_current);
        free(p_tx_buffer_head->p_buffer);
        p_tx_buffer_head->p_buffer = NULL;
break;
    }
        p_tx_buffer_current = p_tx_buffer_current->p_next;
    }
}
}
}
```

## Data Structures

struct [ether\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [ether\\_previous\\_link\\_status\\_t](#)

enum [ether\\_link\\_change\\_t](#)

enum [ether\\_magic\\_packet\\_t](#)

enum [ether\\_link\\_establish\\_status\\_t](#)

## Data Structure Documentation

### ◆ ether\_instance\_ctrl\_t

struct ether_instance_ctrl_t		
ETHER control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">ether_api_t::open</a> is called.		
Data Fields		
uint32_t	open	Used to determine if the channel is configured.
<a href="#">ether_cfg_t</a> const *	p_ether_cfg	Pointer to initial configurations.
<a href="#">ether_instance_descriptor_t</a> *	p_rx_descriptor	Pointer to the currently referenced transmit descriptor.
<a href="#">ether_instance_descriptor_t</a> *	p_tx_descriptor	Pointer to the currently referenced receive descriptor.
void *	p_reg_etherc	Base register of ethernet controller for this channel.
void *	p_reg_edmac	Base register of EDMA controller for this channel.
<a href="#">ether_previous_link_status_t</a>	previous_link_status	Previous link status.
<a href="#">ether_link_change_t</a>	link_change	status of link change
<a href="#">ether_magic_packet_t</a>	magic_packet	status of magic packet detection
<a href="#">ether_link_establish_status_t</a>	link_establish_status	Current Link status.

## Enumeration Type Documentation

### ◆ ether\_previous\_link\_status\_t

enum ether_previous_link_status_t	
Enumerator	
ETHER_PREVIOUS_LINK_STATUS_DOWN	Previous link status is down.
ETHER_PREVIOUS_LINK_STATUS_UP	Previous link status is up.

## ◆ ether\_link\_change\_t

enum ether_link_change_t	
Enumerator	
ETHER_LINK_CHANGE_NO_CHANGE	Link status is no change.
ETHER_LINK_CHANGE_LINK_DOWN	Link status changes to down.
ETHER_LINK_CHANGE_LINK_UP	Link status changes to up.

## ◆ ether\_magic\_packet\_t

enum ether_magic_packet_t	
Enumerator	
ETHER_MAGIC_PACKET_NOT_DETECTED	Magic packet is not detected.
ETHER_MAGIC_PACKET_DETECTED	Magic packet is detected.

## ◆ ether\_link\_establish\_status\_t

enum ether_link_establish_status_t	
Enumerator	
ETHER_LINK_ESTABLISH_STATUS_DOWN	Link establish status is down.
ETHER_LINK_ESTABLISH_STATUS_UP	Link establish status is up.

## Function Documentation

---

◆ **R\_ETHER\_Open()**

```
fsp_err_t R_ETHER_Open ( ether_ctrl_t *const p_ctrl, ether_cfg_t const *const p_cfg )
```

After ETHERC, EDMAC and PHY-LSI are reset in software, an auto negotiation of PHY-LSI is begun. Afterwards, the link signal change interrupt is permitted. Implements [ether\\_api\\_t::open](#).

**Return values**

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block or configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Control block has already been opened or channel is being used by another instance. Call close() then open() to reconfigure.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	Initialization of PHY-LSI failed.
FSP_ERR_INVALID_CHANNEL	Invalid channel number is given.
FSP_ERR_INVALID_POINTER	Pointer to MAC address is NULL.
FSP_ERR_INVALID_ARGUMENT	Interrupt is not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of PHY-LSI failed.

◆ **R\_ETHER\_Close()**

```
fsp_err_t R_ETHER_Close ( ether_ctrl_t *const p_ctrl)
```

Disables interrupts. Removes power and releases hardware lock. Implements [ether\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_Read()**

```
fsp_err_t R_ETHER_Read ( ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t *const length_bytes )
```

Receive Ethernet frame. Receives data to the location specified by the pointer to the receive buffer. In zero copy mode, the address of the receive buffer is returned. In non zero copy mode, the received data in the internal buffer is copied to the pointer passed by the argument. Implements [ether\\_api\\_t::read](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_NO_DATA	There is no data in receive buffer.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.
FSP_ERR_ETHER_ERROR_FILTERING	Multicast Frame filter is enable, and Multicast Address Frame is received.
FSP_ERR_INVALID_POINTER	Value of the pointer is NULL.

◆ **R\_ETHER\_BufferRelease()**

```
fsp_err_t R_ETHER_BufferRelease ( ether_ctrl_t *const p_ctrl)
```

Move to the next buffer in the circular receive buffer list. Implements [ether\\_api\\_t::bufferRelease](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.

◆ **R\_ETHER\_RxBufferUpdate()**

```
fsp_err_t R_ETHER_RxBufferUpdate ( ether_ctrl_t *const p_ctrl, void *const p_buffer )
```

Change the buffer pointer of the current rx buffer descriptor. Implements [ether\\_api\\_t::rxBufferUpdate](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	A pointer argument is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_INVALID_POINTER	The pointer of buffer is NULL or not aligned on a 32-bit boundary.
FSP_ERR_INVALID_MODE	Driver is configured to non zero copy mode.
FSP_ERR_ETHER_RECEIVE_BUFFER_ACTIVE	All descriptor is active.

◆ **R\_ETHER\_Write()**

```
fsp_err_t R_ETHER_Write ( ether_ctrl_t *const p_ctrl, void *const p_buffer, uint32_t const frame_length )
```

Transmit Ethernet frame. Transmits data from the location specified by the pointer to the transmit buffer, with the data size equal to the specified frame length. In the non zero copy mode, transmits data after being copied to the internal buffer. Implements [ether\\_api\\_t::write](#).

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_ERROR_MAGIC_PACKET_MODE	As a Magic Packet is being detected, transmission and reception is not enabled.
FSP_ERR_ETHER_ERROR_TRANSMIT_BUFFER_FULL	Transmit buffer is not empty.
FSP_ERR_INVALID_POINTER	Value of the pointer is NULL.
FSP_ERR_INVALID_ARGUMENT	Value of the send frame size is out of range.

◆ **R\_ETHER\_LinkProcess()**

```
fsp_err_t R_ETHER_LinkProcess ( ether_ctrl_t *const p_ctrl)
```

The Link up processing, the Link down processing, and the magic packet detection processing are executed. Implements `ether_api_t::linkProcess`.

**Return values**

FSP_SUCCESS	Link is up.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Link is down.
FSP_ERR_ETHER_ERROR_PHY_COMMUNICATION	When reopening the PHY interface initialization of the PHY-LSI failed.
FSP_ERR_ALREADY_OPEN	When reopening the PHY interface it was already opened.
FSP_ERR_INVALID_CHANNEL	When reopening the PHY interface an invalid channel was passed.
FSP_ERR_INVALID_POINTER	When reopening the PHY interface the MAC address pointer was NULL.
FSP_ERR_INVALID_ARGUMENT	When reopening the PHY interface the interrupt was not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of the PHY-LSI failed.

◆ **R\_ETHER\_WakeOnLANEnable()**

```
fsp_err_t R_ETHER_WakeOnLANEnable ( ether_ctrl_t *const p_ctrl)
```

The setting of ETHERC is changed from normal sending and receiving mode to magic packet detection mode. Implements `ether_api_t::wakeOnLANEnable`.

**Return values**

FSP_SUCCESS	Processing completed successfully.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_ETHER_ERROR_LINK	Auto-negotiation is not completed, and reception is not enabled.
FSP_ERR_ETHER_PHY_ERROR_LINK	Initialization of PHY-LSI failed.

## ◆ R\_ETHER\_TxStatusGet()

```
fsp_err_t R_ETHER_TxStatusGet ( ether_ctrl_t *const p_ctrl, void *const p_buffer_address )
```

Provides status of Ethernet driver in the user provided pointer. Implements [ether\\_api\\_t::txStatusGet](#).

**Return values**

FSP_SUCCESS	Transmit buffer address is stored in provided p_buffer_address.
FSP_ERR_ASSERTION	Pointer to ETHER control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_INVALID_POINTER	p_status is NULL.
FSP_ERR_NOT_FOUND	Transmit buffer address has been overwritten in transmit descriptor.

**4.2.21 Ethernet PHY (r\_ether\_phy)**

## Modules

**Functions**

```
fsp_err_t R_ETHER_PHY_Open (ether_phy_ctrl_t *const p_ctrl, ether_phy_cfg_t const *const p_cfg)
```

Resets Ethernet PHY device. Implements [ether\\_phy\\_api\\_t::open](#). [More...](#)

```
fsp_err_t R_ETHER_PHY_Close (ether_phy_ctrl_t *const p_ctrl)
```

Close Ethernet PHY device. Implements [ether\\_phy\\_api\\_t::close](#). [More...](#)

```
fsp_err_t R_ETHER_PHY_StartAutoNegotiate (ether_phy_ctrl_t *const p_ctrl)
```

Starts auto-negotiate. Implements [ether\\_phy\\_api\\_t::startAutoNegotiate](#). [More...](#)

```
fsp_err_t R_ETHER_PHY_LinkPartnerAbilityGet (ether_phy_ctrl_t *const p_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause)
```

Reports the other side's physical capability. Implements [ether\\_phy\\_api\\_t::linkPartnerAbilityGet](#). [More...](#)

```
fsp_err_t R_ETHER_PHY_LinkStatusGet (ether_phy_ctrl_t *const p_ctrl)
```

Returns the status of the physical link. Implements `ether_phy_api_t::linkStatusGet`. [More...](#)

## Detailed Description

The Ethernet PHY module (r\_ether\_phy) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral. It implements the [Ethernet PHY Interface](#).

## Overview

The Ethernet PHY module is used to setup and manage an external Ethernet PHY device for use with the on-chip Ethernet Controller (ETHERC) peripheral. It performs auto-negotiation to determine the optimal connection parameters between link partners. Once initialized the connection between the external PHY and the onboard controller is automatically managed in hardware.

## Features

The Ethernet PHY module supports the following features:

- Auto negotiation support
- Flow control support
- Link status check support

## Configuration

### Build Time Configurations for r\_ether\_phy

The following build time configurations are defined in `fsp_cfg/r_ether_phy_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Select PHY	<ul style="list-style-type: none"> <li>• Default</li> <li>• Other</li> <li>• KSZ8091RNB</li> <li>• KSZ8041</li> <li>• DP83620</li> </ul>	Default	Select PHY chip to use. Selecting 'Default' will automatically choose the correct option when using a Renesas development board.
Reference Clock	<ul style="list-style-type: none"> <li>• Default</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default	Select whether to use the RMI reference clock. Selecting 'Default' will automatically choose the correct option when using a Renesas development board.

## Configurations for Driver > Network > Ethernet Driver on r\_ether\_phy

This module can be added to the Stacks tab via New Stack > Driver > Network > Ethernet Driver on r\_ether\_phy.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_ether_phy0	Module name.
Channel	<ul style="list-style-type: none"> <li>• 0</li> <li>• 1</li> </ul>	0	Select the Ethernet controller channel number.
PHY-LSI Address	Specify a value between 0 and 31.	0	Specify the address of the PHY-LSI used.
PHY-LSI Reset Completion Timeout	Specify a value between 0x1 and 0xFFFFFFFF.	0x00020000	Specify the number of times to read the PHY-LSI control register while waiting for reset completion. This value should be adjusted experimentally based on the PHY-LSI used.
Select MII type	<ul style="list-style-type: none"> <li>• MII</li> <li>• RMII</li> </ul>	MII	Specify whether to use MII or RMII.
MII/RMII Register Access Wait-time	Specify a value between 0x1 and 0x7FFFFFFF.	8	Specify the bit timing for MII/RMII register accesses during PHY initialization. This value should be adjusted experimentally based on the PHY-LSI used.
Flow Control	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Select whether to enable or disable flow control.

## Usage Notes

### Note

See the [example](#) below for details on how to initialize the Ethernet PHY module.

### Accessing the MII and RMII Registers

Use the PIR register to access the MII and RMII registers in the PHY-LSI. Serial data in the MII and RMII management frame format is transmitted and received through the ET0\_MDC and ET0\_MDIO pins controlled by software.

### MII and RMII management frame format

The below table lists the MII and RMII management frame formats.

Access type	MII and RMII management frame								
	Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
	Number of bits	32	2	2	5	5	2	16	1
Read		1...1	01	10	00001	RRRRR	Z0	DDDDD DDDDD DDDDD D	Z
Write		1...1	01	01	00001	RRRRR	10	DDDDD DDDDD DDDDD D	Z

**Note**

- *PRE (preamble): Send 32 consecutive 1s.*
  - *ST (start of frame): Send 01b.*
  - *OP (operation code): Send 10b for read or 01b for write.*
  - *PHYAD (PHY address): Up to 32 PHY-LSIs can be connected to one MAC. PHY-LSIs are selected with these 5 bits. When the PHY-LSI address is 1, send 00001b.*
  - *REGAD (register address): One register is selected from up to 32 registers in the PHY-LSI. When the register address is 1, send 00001b.*
  - *TA (turnaround): Use 2-bit turnaround time to avoid contention between the register address and data during a read operation.*
- Send 10b during a write operation. Release the bus for 1 bit during a read operation (Z is output). (This is indicated as Z0 because 0 is output from the PHY-LSI on the next clock cycle.)*
- *DATA (data): 16-bit data. Sequentially send or receive starting from the MSB.*
  - *IDLE (IDLE condition): Wait time before inputting the next MII or RMII management format. Release the bus during a write operation (Z is output). No control is required, because a bus was already released during a read operation.*

**Limitations**

- The r\_ether\_phy module may need to be customized for PHY devices other than the ones currently supported (KSZ8091RNB, KSZ8041 and DP83620). Use the existing code as a starting point for creating a custom implementation.

**Examples****ETHER PHY Basic Example**

This is a basic example of minimal use of the ETHER PHY in an application.

```
void ether_phy_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    g_ether_phy0_ctrl.open    = 0U;

    g_ether_phy0_cfg.channel = 0;

    /* Initializes the module. */
}
```

```

err = R_ETHER_PHY_Open(&g_ether_phy0_ctrl, &g_ether_phy0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Start auto negotiation. */
err = R_ETHER_PHY_StartAutoNegotiate(&g_ether_phy0_ctrl);
assert(FSP_SUCCESS == err);
/* Polling until link is established. */
while (FSP_SUCCESS != R_ETHER_PHY_LinkStatusGet(&g_ether_phy0_ctrl))
{
/* Do nothing */
}
/* Get link partner ability from phy interface. */
err = R_ETHER_PHY_LinkPartnerAbilityGet(&g_ether_phy0_ctrl,
                                         &g_ether_phy0_line_speed_duplex,
                                         &g_ether_phy0_local_pause,
                                         &g_ether_phy0_partner_pause);

assert(FSP_SUCCESS == err);
/* Check current link status. */
err = R_ETHER_PHY_LinkStatusGet(&g_ether_phy0_ctrl);
assert(FSP_SUCCESS == err);
}

```

## Data Structures

struct [ether\\_phy\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ ether\_phy\_instance\_ctrl\_t

struct ether_phy_instance_ctrl_t		
ETHER PHY control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">ether_phy_api_t::open</a> is called.		
Data Fields		
uint32_t	open	Used to determine if the channel is configured.
<a href="#">ether_phy_cfg_t</a> const *	p_ether_phy_cfg	Pointer to initial configurations.
volatile uint32_t *	p_reg_pir	Pointer to ETHERC peripheral registers.

uint32_t	local_advertise	Capabilities bitmap for local advertising.
----------	-----------------	--

## Function Documentation

### ◆ R\_ETHER\_PHY\_Open()

```
fsp_err_t R_ETHER_PHY_Open ( ether_phy_ctrl_t *const p_ctrl, ether_phy_cfg_t const *const p_cfg )
```

Resets Ethernet PHY device. Implements `ether_phy_api_t::open`.

#### Return values

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block or configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Control block has already been opened or channel is being used by another instance. Call <code>close()</code> then <code>open()</code> to reconfigure.
FSP_ERR_INVALID_CHANNEL	Invalid channel number is given.
FSP_ERR_INVALID_POINTER	Pointer to <code>p_cfg</code> is NULL.
FSP_ERR_TIMEOUT	PHY-LSI Reset wait timeout.

### ◆ R\_ETHER\_PHY\_Close()

```
fsp_err_t R_ETHER_PHY_Close ( ether_phy_ctrl_t *const p_ctrl)
```

Close Ethernet PHY device. Implements `ether_phy_api_t::close`.

#### Return values

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_PHY\_StartAutoNegotiate()**

```
fsp_err_t R_ETHER_PHY_StartAutoNegotiate ( ether_phy_ctrl_t *const p_ctrl)
```

Starts auto-negotiate. Implements `ether_phy_api_t::startAutoNegotiate`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully starts auto-negotiate.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

◆ **R\_ETHER\_PHY\_LinkPartnerAbilityGet()**

```
fsp_err_t R_ETHER_PHY_LinkPartnerAbilityGet ( ether_phy_ctrl_t *const p_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause )
```

Reports the other side's physical capability. Implements `ether_phy_api_t::linkPartnerAbilityGet`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully get link partner ability.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_INVALID_POINTER	Pointer to arguments are NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY-LSI is not link up.
FSP_ERR_ETHER_PHY_NOT_READY	The auto-negotiation isn't completed

◆ **R\_ETHER\_PHY\_LinkStatusGet()**

```
fsp_err_t R_ETHER_PHY_LinkStatusGet ( ether_phy_ctrl_t *const p_ctrl)
```

Returns the status of the physical link. Implements `ether_phy_api_t::linkStatusGet`.

**Return values**

FSP_SUCCESS	ETHER_PHY successfully get link partner ability.
FSP_ERR_ASSERTION	Pointer to ETHER_PHY control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_ETHER_PHY_ERROR_LINK	PHY-LSI is not link up.

## 4.2.22 High-Performance Flash Driver (r\_flash\_hp)

### Modules

#### Functions

fsp_err_t	R_FLASH_HP_Open (flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg)
fsp_err_t	R_FLASH_HP_Write (flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t flash_address, uint32_t const num_bytes)
fsp_err_t	R_FLASH_HP_Erase (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks)
fsp_err_t	R_FLASH_HP_BlankCheck (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t num_bytes, flash_result_t *blank_check_result)
fsp_err_t	R_FLASH_HP_Close (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_HP_StatusGet (flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status)
fsp_err_t	R_FLASH_HP_AccessWindowSet (flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr, uint32_t const end_addr)
fsp_err_t	R_FLASH_HP_AccessWindowClear (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_HP_IdCodeSet (flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code, flash_id_code_mode_t mode)
fsp_err_t	R_FLASH_HP_Reset (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_HP_UpdateFlashClockFreq (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_HP_StartUpAreaSelect (flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)
fsp_err_t	R_FLASH_HP_CallbackSet (flash_ctrl_t *const p_api_ctrl, void(*p_callback)(flash_callback_args_t *), void const *const p_context, flash_callback_args_t *const p_callback_memory)
fsp_err_t	R_FLASH_HP_BankSwap (flash_ctrl_t *const p_api_ctrl)
fsp_err_t	R_FLASH_HP_InfoGet (flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info)

## Detailed Description

Driver for the flash memory on RA high-performance MCUs. This module implements the [Flash Interface](#).

## Overview

The Flash HAL module APIs allow an application to write, erase and blank check both the data and ROM flash areas that reside within the MCU. The amount of flash memory available varies across MCU parts.

## Features

The R\_FLASH\_HP module has the following key features:

- Blocking and non-blocking erasing, writing and blank-checking of data flash.
- Blocking erasing, writing and blank-checking of code flash.
- Callback functions for completion of non-blocking data flash operations.
- Access window (write protection) for ROM Flash, allowing only specified areas of code flash to be erased or written.
- Boot block-swapping.
- ID code programming support.

## Configuration

### Build Time Configurations for r\_flash\_hp

The following build time configurations are defined in fsp\_cfg/r\_flash\_hp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Code Flash Programming Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Controls whether or not code-flash programming is enabled. Disabling reduces the amount of ROM and RAM used by the API.
Data Flash Programming Enable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Controls whether or not data-flash programming is enabled. Disabling reduces the amount of ROM used by the API.

### Configurations for Driver > Storage > Flash Driver on r\_flash\_hp

This module can be added to the Stacks tab via New Stack > Driver > Storage > Flash Driver on r\_flash\_hp. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_flash0	Module name.
Data Flash Background Operation	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	Enabling allows Flash API calls that reference data-flash to return immediately, with the operation continuing in the background.
Callback	Name must be a valid C symbol	NULL	A user callback function can be specified. Callback function called when a Data Flash Background Operation completes or errors.
Flash Ready Interrupt Priority	MCU Specific Options		Select the flash ready interrupt priority.
Flash Error Interrupt Priority	MCU Specific Options		Select the flash error interrupt priority.

## Clock Configuration

Flash uses FCLK as the clock source depending on the MCU. When writing and erasing the clock source must be at least 4 MHz.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Warning

It is highly recommended that the developer reviews sections 5 and 6 of the Flash Memory section of the target MCUs Hardware User's Manual prior to using the r\_flash\_hp module. In particular, understanding ID Code and Access Window functionality can help avoid unrecoverable flash scenarios.

## Data Flash Background Operation (BGO) Precautions

When using the data flash BGO (Background Operation) mode, you can still access the user ROM, RAM and external memory. You must ensure that the data flash is not accessed during a data flash operation. This includes interrupts that may access the data flash.

## Code Flash Precautions

Code flash cannot be accessed while writing, erasing or blank checking code flash. Code flash cannot be accessed while modifying the access window, selecting the startup area or setting the ID code. In order to support modifying code flash all supporting code must reside in RAM. This is only done when code flash programming is enabled. BGO mode is not supported for code flash, so a code flash operation will not return before the operation has completed. By default, the vector table resides in

the code flash. If an interrupt occurs during the code flash operation, then code flash will be accessed to fetch the interrupt's starting address and an error will occur. The simplest work-around is to disable interrupts during code flash operations. Another option is to copy the vector table to RAM, update the VTOR (Vector Table Offset Register) accordingly and ensure that any interrupt service routines execute out of RAM. Similarly, you must insure that if in a multi-threaded environment, threads running from code flash cannot become active while a code flash operation is in progress.

## Flash Clock (FCLK)

The flash clock source is the clock used by the Flash peripheral in performing all Flash operations. As part of the `flash_api_t::open` function the Flash clock source is checked will return `FSP_ERR_FCLK` if it is invalid. Once the Flash API has been opened, if the flash clock source frequency is changed, the `flash_api_t::updateFlashClockFreq` API function must be called to inform the API of the change. Failure to do so could result in flash operation failures and possibly damage the part.

## Interrupts

Enable the flash ready interrupt only if you plan to use the data flash BGO. In this mode, the application can initiate a data flash operation and then be asynchronously notified of its completion, or an error, using a user supplied-callback function. The callback function is passed a structure containing event information that indicates the source of the callback event (for example, `flash_api_t::FLASH_EVENT_ERASE_COMPLETE`) When the FLASH FRDYI interrupt is enabled, the corresponding ISR will be defined in the flash driver. The ISR will call a user-callback function if one was registered with the `flash_api_t::open` API.

### Note

*The Flash HP supports an additional flash-error interrupt and if the BGO mode is enabled for the FLASH HP then both the Flash Ready Interrupt and Flash Error Interrupts must be enabled (assigned a priority).*

## Limitations

- Write operations must be aligned on page boundaries and must be a multiple of the page boundary size.
- Erase operations will erase the entire block the provided address resides in.
- Data flash is better suited for storing data as it can be erased and written to while code is still executing from code flash. Data flash is also guaranteed for a larger number of reprogramming/erasure cycles than code flash.
- Read values of erased data flash blocks are not guaranteed to be 0xFF. Blank check should be used to determine if memory has been erased but not yet programmed.

## Examples

### High-Performance Flash Basic Example

This is a basic example of erasing and writing to data flash and code flash.

```
#define FLASH_DF_BLOCK_0 0x40100000U /* 64 B: 0x40100000 - 0x4010003F */
#define FLASH_CF_BLOCK_8 0x00010000 /* 32 KB: 0x00010000 - 0x00017FFF */
#define FLASH_DATA_BLOCK_SIZE (1024)
#define FLASH_HP_EXAMPLE_WRITE_SIZE 32
```

```
uint8_t      g_dest[TRANSFER_LENGTH];
uint8_t      g_src[TRANSFER_LENGTH];
flash_result_t blank_check_result;
void r_flash_hp_basic_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the flash hp instance. */
    fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_cfg);
    assert(FSP_SUCCESS == err);

    /* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    assert(FSP_SUCCESS == err);

    /* Check if block 0 is erased. */
    err = R_FLASH_HP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
    assert(FSP_SUCCESS == err);

    /* Verify the previously erased area is blank */
    assert(FLASH_RESULT_BLANK == blank_check_result);

    /* Write 32 bytes to the first block of data flash. */
    err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);
    assert(FSP_SUCCESS == err);
    assert(0 == memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE));

    /* Disable interrupts to prevent vector table access while code flash is in P/E
mode. */
    __disable_irq();

    /* Erase 1 block of code flash starting at block 10. */
    err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_CF_BLOCK_8, 1);
    assert(FSP_SUCCESS == err);
}
```

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_CF_BLOCK_8,
FLASH_HP_EXAMPLE_WRITE_SIZE);

assert(FSP_SUCCESS == err);

/* Enable interrupts after code flash operations are complete. */
__enable_irq();

assert(0 == memcmp(g_src, (uint8_t *) FLASH_CF_BLOCK_8,
FLASH_HP_EXAMPLE_WRITE_SIZE));
}
```

## High-Performance Flash Advanced Example

This example demonstrates using BGO to do non-blocking operations on the data flash.

```
bool interrupt_called;
flash_event_t flash_event;
static flash_cfg_t g_flash_bgo_example_cfg =
{
    .p_callback    = flash_callback,
    .p_context     = 0,
    .p_extend      = NULL,
    .data_flash_bgo = true,
    .ipl           = 5,
    .irq           = BSP_VECTOR_FLASH_HP_FRDYI_ISR,
};

void r_flash_hp_bgo_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the flash hp instance. */
    fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_bgo_example_cfg);

    /* Handle any errors. */
}
```

```
    assert(FSP_SUCCESS == err);
    interrupt_called = false;
/* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    assert(FSP_SUCCESS == err);
while (!interrupt_called)
    {
        ;
    }
    assert(FLASH_EVENT_ERASE_COMPLETE == flash_event);
    interrupt_called = false;
/* Write 32 bytes to the first block of data flash. */
    err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);
    assert(FSP_SUCCESS == err);
    flash_status_t status;
/* Wait until the current flash operation completes. */
do
    {
        err = R_FLASH_HP_StatusGet(&g_flash_ctrl, &status);
    } while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
/* If the interrupt wasn't called process the error. */
    assert(interrupt_called);
/* If the event wasn't a write complete process the error. */
    assert(FLASH_EVENT_WRITE_COMPLETE == flash_event);
/* Verify the data was written correctly. */
    assert(0 == memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE));
}
void flash_callback (flash_callback_args_t * p_args)
{
    interrupt_called = true;
    flash_event      = p_args->event;
}
```

## High-Performance Flash Bank Swap Example

This example demonstrates swapping which flash bank is located at address 0. This feature is only on select MCUs.

```
void r_flash_hp_bankswap_example (void)
{
    /* Open the flash hp instance. */
    fsp_err_t err = R_FLASH_HP_Open(&g_flash_ctrl, &g_flash_cfg);
    /* Handle any errors. */
    assert(FSP_SUCCESS == err);
    /* Write the new application starting at 0x00200000. */
    /* Swap the block at address 0 with the one at 0x00200000 after the next restart.
     * The application at 0x00200000 must be written there by application code. */
    err = R_FLASH_HP_BankSwap(&g_flash_ctrl);
    /* Handle any errors. */
    assert(FSP_SUCCESS == err);
    /* Handle any pre-reset operations here */
    /* Reset the MCU to swap to the other bank */
    __NVIC_SystemReset();
}
```

### Data Structures

struct [flash\\_hp\\_instance\\_ctrl\\_t](#)

### Enumerations

enum [flash\\_bgo\\_operation\\_t](#)

### Data Structure Documentation

#### ◆ flash\_hp\_instance\_ctrl\_t

struct flash\_hp\_instance\_ctrl\_t

Flash HP instance control block. DO NOT INITIALIZE.

#### Data Fields

uint32_t	<a href="#">opened</a>
	To check whether api has been opened or not.

<code>flash_bgo_operation_t</code>	<code>current_operation</code>
	Operation in progress, for example, FLASH_OPERATION_CF_ERASE.

## Enumeration Type Documentation

### ◆ `flash_bgo_operation_t`

enum <code>flash_bgo_operation_t</code>
Possible Flash operation states

## Function Documentation

### ◆ `R_FLASH_HP_Open()`

<code>fsp_err_t R_FLASH_HP_Open ( flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg )</code>	
Initializes the high performance flash peripheral. Implements <code>flash_api_t::open</code> .	
The Open function initializes the Flash.	
Example:	
<pre>/* Open the flash hp instance. */ fsp_err_t err = R_FLASH_HP_Open(&amp;g_flash_ctrl, &amp;g_flash_cfg);</pre>	
<b>Return values</b>	
<code>FSP_SUCCESS</code>	Initialization was successful and timer has started.
<code>FSP_ERR_ALREADY_OPEN</code>	The flash control block is already open.
<code>FSP_ERR_ASSERTION</code>	NULL provided for <code>p_ctrl</code> or <code>p_cfg</code> .
<code>FSP_ERR_IRQ_BSP_DISABLED</code>	Caller is requesting BGO but the Flash interrupts are not enabled.
<code>FSP_ERR_FCLK</code>	FCLK must be a minimum of 4 MHz for Flash operations.

### ◆ R\_FLASH\_HP\_Write()

```
fsp_err_t R_FLASH_HP_Write ( flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t
flash_address, uint32_t const num_bytes )
```

Writes to the specified Code or Data Flash memory area. Implements `flash_api_t::write`.

Example:

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_HP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_HP_EXAMPLE_WRITE_SIZE);
```

#### Return values

FSP_SUCCESS	Operation successful. If BGO is enabled this means the operation was started successfully.
FSP_ERR_IN_USE	The Flash peripheral is busy with a prior on-going transaction.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Write an area that is protected by an Access Window.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation. This may be returned if the requested Flash area is not blank.
FSP_ERR_TIMEOUT	Timed out waiting for FCU operation to complete.
FSP_ERR_INVALID_SIZE	Number of bytes provided was not a multiple of the programming size or exceeded the maximum range.
FSP_ERR_INVALID_ADDRESS	Invalid address was input or address not on programming boundary.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.

### ◆ R\_FLASH\_HP\_Erase()

```
fsp_err_t R_FLASH_HP_Erase ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks )
```

Erases the specified Code or Data Flash blocks. Implements `flash_api_t::erase` by the `block_erase_address`.

#### Note

*Code flash may contain blocks of different sizes. When erasing code flash it is important to take this into consideration to prevent erasing a larger address space than desired.*

#### Example:

```
/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_HP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
```

#### Return values

FSP_SUCCESS	Successful open.
FSP_ERR_INVALID_BLOCKS	Invalid number of blocks specified
FSP_ERR_INVALID_ADDRESS	Invalid address specified. If the address is in code flash then code flash programming must be enabled.
FSP_ERR_IN_USE	Other flash operation in progress, or API not initialized
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Erase an area that is protected by an Access Window.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_ERASE_FAILED	Status is indicating a Erase error.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.

### ◆ R\_FLASH\_HP\_BlankCheck()

```
fsp_err_t R_FLASH_HP_BlankCheck ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t
num_bytes, flash_result_t * p_blank_check_result )
```

Performs a blank check on the specified address area. Implements `flash_api_t::blankCheck`.

Example:

```
/* Check if block 0 is erased. */
err = R_FLASH_HP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
assert(FSP_SUCCESS == err);
```

#### Return values

FSP_SUCCESS	Blank check operation completed with result in <code>p_blank_check_result</code> , or blank check started and in-progress (BGO mode).
FSP_ERR_INVALID_ADDRESS	Invalid data flash address was input.
FSP_ERR_INVALID_SIZE	'num_bytes' was either too large or not aligned for the CF/DF boundary size.
FSP_ERR_IN_USE	Other flash operation in progress or API not initialized.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> .
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of attempting to Erase an area that is protected by an Access Window.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.
FSP_ERR_BLANK_CHECK_FAILED	Blank check operation failed.

◆ **R\_FLASH\_HP\_Close()**

```
fsp_err_t R_FLASH_HP_Close ( flash_ctrl_t *const p_api_ctrl)
```

Releases any resources that were allocated by the Open() or any subsequent Flash operations. Implements `flash_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_cfg.

◆ **R\_FLASH\_HP\_StatusGet()**

```
fsp_err_t R_FLASH_HP_StatusGet ( flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status )
```

Query the FLASH peripheral for its status. Implements `flash_api_t::statusGet`.

Example:

```
flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
    err = R_FLASH_HP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
```

**Return values**

FSP_SUCCESS	FLASH peripheral is ready to use.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The Flash API is not Open.

### ◆ R\_FLASH\_HP\_AccessWindowSet()

```
fsp_err_t R_FLASH_HP_AccessWindowSet ( flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr,
uint32_t const end_addr )
```

Configure an access window for the Code Flash memory using the provided start and end address. An access window defines a contiguous area in Code Flash for which programming/erase is enabled. This area is on block boundaries. The block containing start\_addr is the first block. The block containing end\_addr is the last block. The access window then becomes first block -> last block inclusive. Anything outside this range of Code Flash is then write protected.

#### Note

*If the start address and end address are set to the same value, then the access window is effectively removed. This accomplishes the same functionality as R\_FLASH\_HP\_AccessWindowClear().*

Implements [flash\\_api\\_t::accessWindowSet](#).

#### Return values

FSP_SUCCESS	Access window successfully configured.
FSP_ERR_INVALID_ADDRESS	Invalid settings for start_addr and/or end_addr.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_AccessWindowClear()**

```
fsp_err_t R_FLASH_HP_AccessWindowClear ( flash_ctrl_t *const p_api_ctrl)
```

Remove any access window that is currently configured in the Code Flash. Subsequent to this call all Code Flash is writable. Implements `flash_api_t::accessWindowClear`.

**Return values**

FSP_SUCCESS	Access window successfully removed.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_IdCodeSet()**

```
fsp_err_t R_FLASH_HP_IdCodeSet ( flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code,
flash_id_code_mode_t mode )
```

Implements `flash_api_t::idCodeSet`.

**Return values**

FSP_SUCCESS	ID Code successfully configured.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_Reset()**

```
fsp_err_t R_FLASH_HP_Reset ( flash_ctrl_t *const p_api_ctrl)
```

Reset the FLASH peripheral. Implements `flash_api_t::reset`.

No attempt is made to check if the flash is busy before executing the reset since the assumption is that a reset will terminate any existing operation.

**Return values**

FSP_SUCCESS	Flash circuit successfully reset.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_PE_FAILURE	Failed to enter or exit P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

**◆ R\_FLASH\_HP\_UpdateFlashClockFreq()**

`fsp_err_t R_FLASH_HP_UpdateFlashClockFreq ( flash_ctrl_t *const p_api_ctrl)`

Indicate to the already open Flash API that the FCLK has changed. Implements `flash_api_t::updateFlashClockFreq`.

This could be the case if the application has changed the system clock, and therefore the FCLK. Failure to call this function subsequent to changing the FCLK could result in damage to the flash macro.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_FCLK	FCLK is not within the acceptable range.

### ◆ R\_FLASH\_HP\_StartUpAreaSelect()

```
fsp_err_t R_FLASH_HP_StartUpAreaSelect ( flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary )
```

Selects which block, Default (Block 0) or Alternate (Block 1), is used as the startup area block. The provided parameters determine which block will become the active startup block and whether that action will be immediate (but temporary), or permanent subsequent to the next reset. Doing a temporary switch might appear to have limited usefulness. If there is an access window in place such that Block 0 is write protected, then one could do a temporary switch, update the block and switch them back without having to touch the access window. Implements [flash\\_api\\_t::startupAreaSelect](#).

#### Return values

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_CallbackSet()**

```
fsp_err_t R_FLASH_HP_CallbackSet ( flash_ctrl_t *const p_api_ctrl, void(*) (flash_callback_args_t *)
p_callback, void const *const p_context, flash_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `flash_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_FLASH\_HP\_BankSwap()**

```
fsp_err_t R_FLASH_HP_BankSwap ( flash_ctrl_t *const p_api_ctrl)
```

Swaps the flash bank located at address 0x00000000 and address 0x00200000. This can only be done when in dual bank mode. Dual bank mode can be enabled in the FSP Configuration Tool under BSP Properties. After a bank swap is done the MCU will need to be reset for the changes to take place. `flash_api_t::bankSwap`.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> .
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_PE_FAILURE	Failed to enter or exit Code Flash P/E mode.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_INVALID_MODE	Cannot switch banks while flash is in Linear mode.
FSP_ERR_WRITE_FAILED	Flash write operation failed.
FSP_ERR_CMD_LOCKED	FCU is in locked state, typically as a result of having received an illegal command.

◆ **R\_FLASH\_HP\_InfoGet()**

```
fsp_err_t R_FLASH_HP_InfoGet ( flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info )
```

Returns the information about the flash regions. Implements `flash_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Successful retrieved the request information.
FSP_ERR_NOT_OPEN	The control block is not open.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_info.

**4.2.23 Low-Power Flash Driver (r\_flash\_lp)**

## Modules

**Functions**

```
fsp_err_t R_FLASH_LP_Open (flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg)
```

```
fsp_err_t R_FLASH_LP_Write (flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t flash_address, uint32_t const num_bytes)
```

```
fsp_err_t R_FLASH_LP_Erase (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks)
```

```
fsp_err_t R_FLASH_LP_BlankCheck (flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t num_bytes, flash_result_t *blank_check_result)
```

```
fsp_err_t R_FLASH_LP_Close (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_LP_StatusGet (flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status)
```

```
fsp_err_t R_FLASH_LP_AccessWindowSet (flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr, uint32_t const end_addr)
```

```
fsp_err_t R_FLASH_LP_AccessWindowClear (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_LP_IdCodeSet (flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code, flash_id_code_mode_t mode)
```

```
fsp_err_t R_FLASH_LP_Reset (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_LP_StartUpAreaSelect (flash_ctrl_t *const p_api_ctrl,
flash_startup_area_swap_t swap_type, bool is_temporary)
```

```
fsp_err_t R_FLASH_LP_CallbackSet (flash_ctrl_t *const p_api_ctrl,
void(*p_callback)(flash_callback_args_t *), void const *const
p_context, flash_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_FLASH_LP_BankSwap (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_LP_UpdateFlashClockFreq (flash_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_FLASH_LP_InfoGet (flash_ctrl_t *const p_api_ctrl, flash_info_t *const
p_info)
```

## Detailed Description

Driver for the flash memory on RA low-power MCUs. This module implements the [Flash Interface](#).

## Overview

The Flash HAL module APIs allow an application to write, erase and blank check both the data and code flash areas that reside within the MCU. The amount of flash memory available varies across MCU parts.

## Features

The Low-Power Flash HAL module has the following key features:

- Blocking and non-blocking erasing, writing and blank-checking of data flash.
- Blocking erasing, writing and blank checking of code flash.
- Callback functions for completion of non-blocking data flash operations.
- Access window (write protection) for code flash, allowing only specified areas of code flash to be erased or written.
- Boot block-swapping.
- ID code programming support.

## Configuration

### Build Time Configurations for r\_flash\_lp

The following build time configurations are defined in fsp\_cfg/r\_flash\_lp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Code Flash Programming	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Controls whether or not code-flash programming is

enabled. Disabling reduces the amount of ROM and RAM used by the API.

Data Flash Programming	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Controls whether or not data-flash programming is enabled. Disabling reduces the amount of ROM used by the API.
------------------------	---	---------	---

## Configurations for Driver > Storage > Flash Driver on r\_flash\_lp

This module can be added to the Stacks tab via New Stack > Driver > Storage > Flash Driver on r\_flash\_lp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_flash0	Module name.
Data Flash Background Operation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enabling allows Flash API calls that reference data-flash to return immediately, with the operation continuing in the background.
Callback	Name must be a valid C symbol	NULL	A user callback function can be specified. Callback function called when a Data Flash Background Operation completes or errors.
Flash Ready Interrupt Priority	MCU Specific Options		Select the flash ready interrupt priority.

## Clock Configuration

Flash either uses FCLK or ICLK as the clock source depending on the MCU. When writing and erasing the clock source must be at least 4 MHz.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Warning

It is highly recommended that the developer reviews sections 5 and 6 of the Flash Memory section of the target MCUs Hardware User's Manual prior to using the r\_flash\_lp module. In particular, understanding ID Code and Access Window functionality can help avoid unrecoverable flash scenarios.

## Data Flash Background Operation (BGO) Precautions

When using the data flash BGO, the code flash, RAM and external memory can still be accessed. You must ensure that the data flash is not accessed during a data flash operation. This includes interrupts that may access the data flash.

## Code Flash Precautions

Code flash cannot be accessed while writing, erasing or blank checking code flash. Code flash cannot be accessed while modifying the access window, selecting the startup area or setting the ID code. In order to support modifying code flash all supporting code must reside in RAM. This is only done when code flash programming is enabled. BGO mode is not supported for code flash, so a code flash operation will not return before the operation has completed. By default, the vector table resides in the code flash. If an interrupt occurs during the code flash operation, then code flash will be accessed to fetch the interrupt's starting address and an error will occur. The simplest work-around is to disable interrupts during code flash operations. Another option is to copy the vector table to RAM, update the VTOR (Vector Table Offset Register) accordingly and ensure that any interrupt service routines execute out of RAM. Similarly, you must insure that if in a multi-threaded environment, threads running from code flash cannot become active while a code flash operation is in progress.

## Flash Clock Source

The flash clock source is the clock used by the Flash peripheral in performing all Flash operations. As part of the `flash_api_t::open` function the Flash clock source is checked will return `FSP_ERR_FCLK` if it is invalid. Once the Flash API has been opened, if the flash clock source frequency is changed, the `flash_api_t::updateFlashClockFreq` API function must be called to inform the API of the change. Failure to do so could result in flash operation failures and possibly damage the part.

## Interrupts

Enable the flash ready interrupt only if you plan to use the data flash BGO. In this mode, the application can initiate a data flash operation and then be asynchronously notified of its completion, or an error, using a user supplied-callback function. The callback function is passed a structure containing event information that indicates the source of the callback event (for example, `flash_api_t::FLASH_EVENT_ERASE_COMPLETE`) When the FLASH FRDYI interrupt is enabled, the corresponding ISR will be defined in the flash driver. The ISR will call a user-callback function if one was registered with the `flash_api_t::open` API.

### Note

*The Flash HP supports an additional flash-error interrupt and if the BGO mode is enabled for the FLASH HP then both the Flash Ready Interrupt and Flash Error Interrupts must be enabled (assigned a priority).*

## Limitations

- Write operations must be aligned on page boundaries and must be a multiple of the page boundary size.
- Erase operations will erase the entire block the provided address resides in.
- Data flash is better suited for storing data as it can be erased and written to while code is still executing from code flash. Data flash is also guaranteed for a larger number of reprogramming/erasure cycles than code flash.
- Read values of erased blocks are not guaranteed to be 0xFF. Blank check should be used to determine if memory has been erased but not yet programmed.

## Examples

### Low-Power Flash Basic Example

This is a basic example of erasing and writing to data flash and code flash.

```
#define FLASH_DF_BLOCK_0 0x40100000U /* 1 KB: 0x40100000 - 0x401003FF */
#define FLASH_CF_BLOCK_10 0x00005000 /* 2 KB: 0x00005000 - 0x000057FF */
#define FLASH_DATA_BLOCK_SIZE (1024)
#define FLASH_LP_EXAMPLE_WRITE_SIZE 32
uint8_t      g_dest[TRANSFER_LENGTH];
uint8_t      g_src[TRANSFER_LENGTH];
flash_result_t blank_check_result;
void R_FLASH_LP_basic_example (void)
{
    /* Initialize p_src to known data */
    for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the flash lp instance. */
    fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_cfg);
    assert(FSP_SUCCESS == err);
    /* Erase 1 block of data flash starting at block 0. */
    err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
    assert(FSP_SUCCESS == err);
    /* Check if block 0 is erased. */
    err = R_FLASH_LP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
    assert(FSP_SUCCESS == err);
    /* Verify the previously erased area is blank */
    assert(FLASH_RESULT_BLANK == blank_check_result);
    /* Write 32 bytes to the first block of data flash. */
    err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
    assert(FSP_SUCCESS == err);
}
```

```
    assert(0 == memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE));

    /* Disable interrupts to prevent vector table access while code flash is in P/E
mode. */
    __disable_irq();

    /* Erase 1 block of code flash starting at block 10. */
    err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_CF_BLOCK_10, 1);
    assert(FSP_SUCCESS == err);

    /* Write 32 bytes to the first block of data flash. */
    err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_CF_BLOCK_10,
FLASH_LP_EXAMPLE_WRITE_SIZE);
    assert(FSP_SUCCESS == err);

    /* Enable interrupts after code flash operations are complete. */
    __enable_irq();

    assert(0 == memcmp(g_src, (uint8_t *) FLASH_CF_BLOCK_10,
FLASH_LP_EXAMPLE_WRITE_SIZE));
}
```

## Low-Power Flash Advanced Example

This example demonstrates using BGO to do non-blocking operations on the data flash.

```
bool interrupt_called;
flash_event_t flash_event;
static flash_cfg_t g_flash_bgo_example_cfg =
{
    .p_callback    = flash_callback,
    .p_context     = 0,
    .p_extend      = NULL,
    .data_flash_bgo = true,
    .ipl           = 5,
    .irq           = BSP_VECTOR_FLASH_LP_FRDYI_ISR,
};

void R_FLASH_LP_bgo_example (void)
{
```

```
/* Initialize p_src to known data */
for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
{
    g_src[i] = (uint8_t) ('A' + (i % 26));
}

/* Open the flash lp instance. */
fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_bgo_example_cfg);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

interrupt_called = false;

/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
assert(FSP_SUCCESS == err);

while (!interrupt_called)
{
    ;
}

assert(FLASH_EVENT_ERASE_COMPLETE == flash_event);

interrupt_called = false;

/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
assert(FSP_SUCCESS == err);

flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
    err = R_FLASH_LP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));

/* If the interrupt wasn't called process the error. */
assert(interrupt_called);

/* If the event wasn't a write complete process the error. */
assert(FLASH_EVENT_WRITE_COMPLETE == flash_event);

/* Verify the data was written correctly. */
```

```
    assert(0 == memcmp(g_src, (uint8_t *) FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE));
}
void flash_callback (flash_callback_args_t * p_args)
{
    interrupt_called = true;
    flash_event      = p_args->event;
}
```

## Data Structures

struct [flash\\_lp\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ flash\_lp\_instance\_ctrl\_t

struct flash\_lp\_instance\_ctrl\_t

Flash instance control block. DO NOT INITIALIZE. Initialization occurs when [R\\_FLASH\\_LP\\_Open\(\)](#) is called.

## Function Documentation

◆ **R\_FLASH\_LP\_Open()**

```
fsp_err_t R_FLASH_LP_Open ( flash_ctrl_t *const p_api_ctrl, flash_cfg_t const *const p_cfg )
```

Initialize the Low Power flash peripheral. Implements `flash_api_t::open`.

The Open function initializes the Flash.

This function must be called once prior to calling any other FLASH API functions. If a user supplied callback function is supplied, then the Flash Ready interrupt will be configured to call the users callback routine with an Event type describing the source of the interrupt for Data Flash operations.

Example:

```
/* Open the flash lp instance. */
fsp_err_t err = R_FLASH_LP_Open(&g_flash_ctrl, &g_flash_cfg);
```

**Note**

*Providing a callback function in the supplied `p_cfg->callback` field automatically configures the Flash for Data Flash to operate in non-blocking background operation (BGO) mode.*

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	NULL provided for <code>p_ctrl</code> , <code>p_cfg</code> or <code>p_callback</code> if BGO is enabled.
FSP_ERR_IRQ_BSP_DISABLED	Caller is requesting BGO but the Flash interrupts are not enabled.
FSP_ERR_FCLK	FCLK must be a minimum of 4 MHz for Flash operations.
FSP_ERR_ALREADY_OPEN	Flash Open() has already been called.
FSP_ERR_TIMEOUT	Failed to exit P/E mode after configuring flash.

◆ **R\_FLASH\_LP\_Write()**

```
fsp_err_t R_FLASH_LP_Write ( flash_ctrl_t *const p_api_ctrl, uint32_t const src_address, uint32_t
flash_address, uint32_t const num_bytes )
```

Write to the specified Code or Data Flash memory area. Implements `flash_api_t::write`.

Example:

```
/* Write 32 bytes to the first block of data flash. */
err = R_FLASH_LP_Write(&g_flash_ctrl, (uint32_t) g_src, FLASH_DF_BLOCK_0,
FLASH_LP_EXAMPLE_WRITE_SIZE);
```

**Return values**

FSP_SUCCESS	Operation successful. If BGO is enabled this means the operation was started successfully.
FSP_ERR_IN_USE	The Flash peripheral is busy with a prior on-going transaction.
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation. This may be returned if the requested Flash area is not blank.
FSP_ERR_TIMEOUT	Timed out waiting for FCU operation to complete.
FSP_ERR_INVALID_SIZE	Number of bytes provided was not a multiple of the programming size or exceeded the maximum range.
FSP_ERR_INVALID_ADDRESS	Invalid address was input or address not on programming boundary.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.

◆ **R\_FLASH\_LP\_Erase()**

```
fsp_err_t R_FLASH_LP_Erase ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t const num_blocks )
```

Erase the specified Code or Data Flash blocks. Implements `flash_api_t::erase`.

Example:

```
/* Erase 1 block of data flash starting at block 0. */
err = R_FLASH_LP_Erase(&g_flash_ctrl, FLASH_DF_BLOCK_0, 1);
```

**Return values**

FSP_SUCCESS	Successful open.
FSP_ERR_INVALID_BLOCKS	Invalid number of blocks specified
FSP_ERR_INVALID_ADDRESS	Invalid address specified
FSP_ERR_IN_USE	Other flash operation in progress, or API not initialized
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	The Flash API is not Open.
FSP_ERR_TIMEOUT	Timed out waiting for FCU to be ready.
FSP_ERR_ERASE_FAILED	Status is indicating a Erase error.

◆ **R\_FLASH\_LP\_BlankCheck()**

```
fsp_err_t R_FLASH_LP_BlankCheck ( flash_ctrl_t *const p_api_ctrl, uint32_t const address, uint32_t
num_bytes, flash_result_t * p_blank_check_result )
```

Perform a blank check on the specified address area. Implements `flash_api_t::blankCheck`.

Example:

```
/* Check if block 0 is erased. */
err = R_FLASH_LP_BlankCheck(&g_flash_ctrl, FLASH_DF_BLOCK_0,
FLASH_DATA_BLOCK_SIZE, &blank_check_result);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Blankcheck operation completed with result in p_blank_check_result, or blankcheck started and in-progress (BGO mode).
FSP_ERR_INVALID_ADDRESS	Invalid data flash address was input
FSP_ERR_INVALID_SIZE	'num_bytes' was either too large or not aligned for the CF/DF boundary size.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_BLANK_CHECK_FAILED	An error occurred during blank checking.

◆ **R\_FLASH\_LP\_Close()**

```
fsp_err_t R_FLASH_LP_Close ( flash_ctrl_t *const p_api_ctrl)
```

Release any resources that were allocated by the Flash API. Implements `flash_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_cfg.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_IN_USE	The flash is currently in P/E mode.

### ◆ R\_FLASH\_LP\_StatusGet()

```
fsp_err_t R_FLASH_LP_StatusGet ( flash_ctrl_t *const p_api_ctrl, flash_status_t *const p_status )
```

Query the FLASH for its status. Implements `flash_api_t::statusGet`.

Example:

```
flash_status_t status;

/* Wait until the current flash operation completes. */
do
{
    err = R_FLASH_LP_StatusGet(&g_flash_ctrl, &status);
} while ((FSP_SUCCESS == err) && (FLASH_STATUS_BUSY == status));
```

#### Return values

FSP_SUCCESS	Flash is ready and available to accept commands.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.

### ◆ R\_FLASH\_LP\_AccessWindowSet()

```
fsp_err_t R_FLASH_LP_AccessWindowSet ( flash_ctrl_t *const p_api_ctrl, uint32_t const start_addr,
uint32_t const end_addr )
```

Configure an access window for the Code Flash memory. Implements `flash_api_t::accessWindowSet`.

An access window defines a contiguous area in Code Flash for which programming/erase is enabled. This area is on block boundaries. The block containing `start_addr` is the first block. The block containing `end_addr` is the last block. The access window then becomes first block (inclusive) -> last block (exclusive). Anything outside this range of Code Flash is then write protected. As an example, if you wanted to place an accesswindow on Code Flash Blocks 0 and 1, such that only those two blocks were writable, you would need to specify (address in block 0, address in block 2) as the respective start and end address.

#### Note

*If the start address and end address are set to the same value, then the access window is effectively removed. This accomplishes the same functionality as `R_FLASH_LP_AccessWindowClear()`.*

The invalid address and programming boundaries supported and enforced by this function are dependent on the MCU in use as well as the part package size. Please see the User manual and/or requirements document for additional information.

#### Parameters

	<code>p_api_ctrl</code>	The p api control
[in]	<code>start_addr</code>	The start address
[in]	<code>end_addr</code>	The end address

#### Return values

<code>FSP_SUCCESS</code>	Access window successfully configured.
<code>FSP_ERR_INVALID_ADDRESS</code>	Invalid settings for <code>start_addr</code> and/or <code>end_addr</code> .
<code>FSP_ERR_IN_USE</code>	FLASH peripheral is busy with a prior operation.
<code>FSP_ERR_ASSERTION</code>	NULL provided for <code>p_ctrl</code> .
<code>FSP_ERR_UNSUPPORTED</code>	Code Flash Programming is not enabled.
<code>FSP_ERR_NOT_OPEN</code>	Flash API has not yet been opened.
<code>FSP_ERR_TIMEOUT</code>	Timed out waiting for the FCU to become ready.
<code>FSP_ERR_WRITE_FAILED</code>	Status is indicating a Programming error for the requested operation.

◆ **R\_FLASH\_LP\_AccessWindowClear()**

```
fsp_err_t R_FLASH_LP_AccessWindowClear ( flash_ctrl_t *const p_api_ctrl)
```

Remove any access window that is configured in the Code Flash. Implements `flash_api_t::accessWindowClear`. On successful return from this call all Code Flash is writable.

**Return values**

FSP_SUCCESS	Access window successfully removed.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.

◆ **R\_FLASH\_LP\_IdCodeSet()**

```
fsp_err_t R_FLASH_LP_IdCodeSet ( flash_ctrl_t *const p_api_ctrl, uint8_t const *const p_id_code, flash_id_code_mode_t mode )
```

Write the ID code provided to the id code registers. Implements `flash_api_t::idCodeSet`.

**Return values**

FSP_SUCCESS	ID code successfully configured.
FSP_ERR_IN_USE	FLASH peripheral is busy with a prior operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled.
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for completion of extra command.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.

◆ **R\_FLASH\_LP\_Reset()**

```
fsp_err_t R_FLASH_LP_Reset ( flash_ctrl_t *const p_api_ctrl)
```

Reset the FLASH peripheral. Implements `flash_api_t::reset`.

No attempt is made to check if the flash is busy before executing the reset since the assumption is that a reset will terminate any existing operation.

**Return values**

FSP_SUCCESS	Flash circuit successfully reset.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.

◆ **R\_FLASH\_LP\_StartUpAreaSelect()**

```
fsp_err_t R_FLASH_LP_StartUpAreaSelect ( flash_ctrl_t *const p_api_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary )
```

Select which block is used as the startup area block. Implements `flash_api_t::startupAreaSelect`.

Selects which block - Default (Block 0) or Alternate (Block 1) is used as the startup area block. The provided parameters determine which block will become the active startup block and whether that action will be immediate (but temporary), or permanent subsequent to the next reset. Doing a temporary switch might appear to have limited usefulness. If there is an access window in place such that Block 0 is write protected, then one could do a temporary switch, update the block and switch them back without having to touch the access window.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_WRITE_FAILED	Status is indicating a Programming error for the requested operation.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.
FSP_ERR_UNSUPPORTED	Code Flash Programming is not enabled. Cannot set FLASH_STARTUP_AREA_BTFLG when the temporary flag is false.

◆ **R\_FLASH\_LP\_CallbackSet()**

```
fsp_err_t R_FLASH_LP_CallbackSet ( flash_ctrl_t *const p_api_ctrl, void(*) (flash_callback_args_t *)
p_callback, void const *const p_context, flash_callback_args_t *const p_callback_memory )
```

Stub function Implements `flash_api_t::callbackSet`.

**Return values**

FSP_ERR_UNSUPPORTED	Function has not been implemented.
---------------------	------------------------------------

◆ **R\_FLASH\_LP\_BankSwap()**

```
fsp_err_t R_FLASH_LP_BankSwap ( flash_ctrl_t *const p_api_ctrl)
```

Unsupported `flash_api_t::bankSwap`.

**Return values**

FSP_ERR_UNSUPPORTED	Module does not support Bank Swap.
---------------------	------------------------------------

◆ **R\_FLASH\_LP\_UpdateFlashClockFreq()**

```
fsp_err_t R_FLASH_LP_UpdateFlashClockFreq ( flash_ctrl_t *const p_api_ctrl)
```

Indicate to the already open Flash API that the FCLK has changed. Implements `flash_api_t::updateFlashClockFreq`.

This could be the case if the application has changed the system clock, and therefore the FCLK. Failure to call this function subsequent to changing the FCLK could result in damage to the flash macro.

**Return values**

FSP_SUCCESS	Start-up area successfully toggled.
FSP_ERR_IN_USE	Flash is busy with an on-going operation.
FSP_ERR_FCLK	Invalid flash clock source frequency.
FSP_ERR_ASSERTION	NULL provided for p_ctrl
FSP_ERR_NOT_OPEN	Flash API has not yet been opened.
FSP_ERR_TIMEOUT	Timed out waiting for the FCU to become ready.

◆ **R\_FLASH\_LP\_InfoGet()**

```
fsp_err_t R_FLASH_LP_InfoGet ( flash_ctrl_t *const p_api_ctrl, flash_info_t *const p_info )
```

Returns the information about the flash regions. Implements `flash_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Successful retrieved the request information.
FSP_ERR_ASSERTION	NULL provided for p_ctrl or p_info.
FSP_ERR_NOT_OPEN	The flash is not open.

**4.2.24 Graphics LCD Controller (r\_glcdd)**

## Modules

**Functions**

```
fsp_err_t R_GLCDC_Open (display_ctrl_t *const p_api_ctrl, display_cfg_t const *const p_cfg)
```

```
fsp_err_t R_GLCDC_Close (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_Start (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_Stop (display_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_GLCDC_LayerChange (display_ctrl_t const *const p_api_ctrl, display_runtime_cfg_t const *const p_cfg, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_BufferChange (display_ctrl_t const *const p_api_ctrl, uint8_t *const framebuffer, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_ColorCorrection (display_ctrl_t const *const p_api_ctrl, display_correction_t const *const p_correction)
```

```
fsp_err_t R_GLCDC_ClutUpdate (display_ctrl_t const *const p_api_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer)
```

```
fsp_err_t R_GLCDC_ClutEdit (display_ctrl_t const *const p_api_ctrl, display_frame_layer_t layer, uint8_t index, uint32_t color)
```

```
fsp_err_t R_GLCDC_StatusGet (display_ctrl_t const *const p_api_ctrl, display_status_t *const status)
```

## Detailed Description

Driver for the GLCDC peripheral on RA MCUs. This module implements the [Display Interface](#).

## Overview

The GLCDC is a multi-stage graphics output peripheral designed to automatically generate timing and data signals for LCD panels. As part of its internal pipeline the two internal graphics layers can be repositioned, alpha blended, color corrected, dithered and converted to and from a wide variety of pixel formats.

### Features

The following features are available:

Feature	Options
Input color formats	ARGB8888, ARGB4444, ARGB1555, RGB888 (32-bit), RGB565, CLUT 8bpp, CLUT 4bpp, CLUT 1bpp
Output color formats	RGB888, RGB666, RGB565, Serial RGB888 (8-bit parallel)
Correction processes	Alpha blending, positioning, brightness and contrast, gamma correction, dithering
Timing signals	Dot clock, Vsync, Hsync, Vertical and horizontal data enable (DE)
Maximum resolution	Up to 1020 x 1008 pixels (dependent on sync signal width)
Maximum dot clock	60MHz for serial RGB mode, 54MHz otherwise
Internal clock divisors	1-9, 12, 16, 24, 32
Interrupts	Vsync (line detect), Layer 1 underflow, Layer 2 underflow
Other functions	Byte-order and endianness control, line repeat function

## Configuration

### Build Time Configurations for r\_glcdc

The following build time configurations are defined in fsp\_cfg/r\_glcdc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	• Default (BSP)	Default (BSP)	If selected, code for

	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>		parameter checking is included in the build.
Color Correction	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	If selected, code to adjust brightness, contrast and gamma settings is included in the build. When disabled all color correction configuration options are ignored.

### Configurations for Driver > Graphics > Display Driver on r\_glcdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > Display Driver on r\_glcdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_display0	Module name.
Interrupts > Callback Function	Name must be a valid C symbol	NULL	A user callback function can be defined here.
Interrupts > Line Detect Interrupt Priority	MCU Specific Options		Select the line detect (Vsync) interrupt priority.
Interrupts > Underflow 1 Interrupt Priority	MCU Specific Options		Select the underflow interrupt priority for layer 1.
Interrupts > Underflow 2 Interrupt Priority	MCU Specific Options		Select the underflow interrupt priority for layer 2.
Input > Graphics Layer 1 > General > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	Yes	Specify Used if the graphics layer 1 is used. If so a framebuffer will be automatically generated based on the specified height and horizontal stride.
Input > Graphics Layer 1 > General > Horizontal size	Value must be between 16 and 1016	480	Specify the number of horizontal pixels.
Input > Graphics Layer 1 > General > Vertical size	Value must be between 16 and 1020	272	Specify the number of vertical pixels.
Input > Graphics Layer 1 > General >	Must be a valid non-negative integer with a	0	Specify the horizontal offset in pixels of the

Horizontal position	maximum configurable value of 4091		graphics layer from the background layer.
Input > Graphics Layer 1 > General > Vertical position	Must be a valid non-negative integer with a maximum configurable value of 4094	0	Specify the vertical offset in pixels of the graphics layer from the background layer.
Input > Graphics Layer 1 > General > Color format	<ul style="list-style-type: none"> <li>• ARGB8888 (32-bit)</li> <li>• RGB888 (32-bit)</li> <li>• RGB565 (16-bit)</li> <li>• ARGB1555 (16-bit)</li> <li>• ARGB4444 (16-bit)</li> <li>• CLUT8 (8-bit)</li> <li>• CLUT4 (4-bit)</li> <li>• CLUT1 (1-bit)</li> </ul>	RGB565 (16-bit)	Specify the graphics layer Input format. If selecting CLUT formats, you must write the CLUT table data before starting output.
Input > Graphics Layer 1 > General > Line descending mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select Used if the framebuffer starts from the bottom of the line.
Input > Graphics Layer 1 > Background Color > Alpha	Value must be between 0 and 255	255	Based on the alpha value, either the graphics Layer 2 (foreground graphics layer) is blended into the graphics Layer 1 (background graphics layer) or the graphics Layer 1 is blended into the monochrome background layer.
Input > Graphics Layer 1 > Background Color > Red	Value must be between 0 and 255	255	Red component of the background color for layer 1.
Input > Graphics Layer 1 > Background Color > Green	Value must be between 0 and 255	255	Green component of the background color for layer 1.
Input > Graphics Layer 1 > Background Color > Blue	Value must be between 0 and 255	255	Blue component of the background color for layer 1.
Input > Graphics Layer 1 > Framebuffer > Framebuffer name	This property must be a valid C symbol	fb_background	Specify the name for the framebuffer for Layer 1.
Input > Graphics Layer 1 > Framebuffer > Number of framebuffers	Must be a valid non-negative integer with a maximum configurable value of 65535	2	Number of framebuffers allocated for Graphics Layer 1.
Input > Graphics Layer 1 > Framebuffer >	Manual Entry	.bss	Specify the section in which to allocate the

## Section for framebuffer allocation

framebuffer. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.

Input > Graphics Layer 1 > Line Repeat > Enable	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Select On if the display will be repeated from a smaller section of the framebuffer.
Input > Graphics Layer 1 > Line Repeat > Repeat count	Must be a valid non-negative integer with a maximum configurable value of 65535 i.e (vertical size) x (lines repeat times) must be equal to the panel vertical size	0	Specify the number of times the image is repeated.
Input > Graphics Layer 1 > Fading > Mode	<ul style="list-style-type: none"> <li>• None</li> <li>• Fade-in</li> <li>• Fade-out</li> </ul>	None	Select the fade method.
Input > Graphics Layer 1 > Fading > Speed	Value must be between 0 and 255	0	Specify the number of frames for the fading transition to complete.
Input > Graphics Layer 2 > General > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Specify Used if the graphics layer 2 is used. If so a framebuffer will be automatically generated based on the specified height and horizontal stride.
Input > Graphics Layer 2 > General > Horizontal size	Value must be between 16 and 1016	480	Specify the number of horizontal pixels.
Input > Graphics Layer 2 > General > Vertical size	Value must be between 16 and 1020	272	Specify the number of vertical pixels.
Input > Graphics Layer 2 > General > Horizontal position	Must be a valid non-negative integer with a maximum configurable value of 4091	0	Specify the horizontal offset in pixels of the graphics layer from the background layer.
Input > Graphics Layer 2 > General > Vertical position	Must be a valid non-negative integer with a maximum configurable value of 4094	0	Specify the vertical offset in pixels of the graphics layer from the background layer.

Input > Graphics Layer 2 > General > Color format	<ul style="list-style-type: none"> <li>• ARGB8888 (32-bit)</li> <li>• RGB888 (32-bit)</li> <li>• RGB565 (16-bit)</li> <li>• ARGB1555 (16-bit)</li> <li>• ARGB4444 (16-bit)</li> <li>• CLUT8 (8-bit)</li> <li>• CLUT4 (4-bit)</li> <li>• CLUT1 (1-bit)</li> </ul>	RGB565 (16-bit)	Specify the graphics layer Input format. If selecting CLUT formats, you must write the CLUT table data before starting output.
Input > Graphics Layer 2 > General > Line descending mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select Used if the framebuffer starts from the bottom of the line.
Input > Graphics Layer 2 > Background Color > Alpha	Value must be between 0 and 255	255	Based on the alpha value, either the graphics Layer 2 (foreground graphics layer) is blended into the graphics Layer 1 (background graphics layer) or the graphics Layer 1 is blended into the monochrome background layer.
Input > Graphics Layer 2 > Background Color > Red	Value must be between 0 and 255	255	Red component of the background color for layer 2.
Input > Graphics Layer 2 > Background Color > Green	Value must be between 0 and 255	255	Green component of the background color for layer 2.
Input > Graphics Layer 2 > Background Color > Blue	Value must be between 0 and 255	255	Blue component of the background color for layer 2.
Input > Graphics Layer 2 > Framebuffer > Framebuffer name	This property must be a valid C symbol	fb_foreground	Specify the name for the framebuffer for Layer 2.
Input > Graphics Layer 2 > Framebuffer > Number of framebuffers	Must be a valid non-negative integer with a maximum configurable value of 65535	2	Number of framebuffers allocated for Graphics Layer 2.
Input > Graphics Layer 2 > Framebuffer > Section for framebuffer allocation	Manual Entry	.bss	Specify the section in which to allocate the framebuffer. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming

Input > Graphics Layer 2 > Line Repeat > Enable	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	unnecessary ROM space.
Input > Graphics Layer 2 > Line Repeat > Repeat count	Must be a valid non-negative integer with a maximum configurable value of 65535 i.e (vertical size) x (lines repeat times) must be equal to the panel vertical size	0	Select On if the display will be repeated from a smaller section of the framebuffer.  Specify the number of times the image is repeated.
Input > Graphics Layer 2 > Fading > Mode	<ul style="list-style-type: none"> <li>• None</li> <li>• Fade-in</li> <li>• Fade-out</li> </ul>	None	Select the fade method.
Input > Graphics Layer 2 > Fading > Speed	Value must be between 0 and 255	0	Specify the number of frames for the fading transition to complete.
Output > Timing > Horizontal total cycles	Value must be between 24 and 1024	525	Specify the total cycles in a horizontal line. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system
Output > Timing > Horizontal active video cycles	Value must be between 16 and 1016	480	Specify the number of active video cycles in a horizontal line (including front and back porch). Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.
Output > Timing > Horizontal back porch cycles	Value must be between 6 and 1006	40	Specify the number of back porch cycles in a horizontal line. Back porch starts from the beginning of Hsync cycles, which means back porch cycles contain Hsync cycles. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.
Output > Timing > Horizontal sync signal	Value must be between 0 and 1023	1	Specify the number of Hsync signal assertion

cycles			cycles. Set to the number of cycles defined in the data sheet of LCD panel sheet in your system.
Output > Timing > Horizontal sync signal polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	Low active	Select the polarity of Hsync signal to match your system.
Output > Timing > Vertical total lines	Value must be between 20 and 1024	316	Specify number of total lines in a frame (including front and back porch).
Output > Timing > Vertical active video lines	Value must be between 16 and 1020	272	Specify the number of active video lines in a frame.
Output > Timing > Vertical back porch lines	Value must be between 3 and 1007	8	Specify the number of back porch lines in a frame. Back porch starts from the beginning of Vsync lines, which means back porch lines contain Vsync lines.
Output > Timing > Vertical sync signal lines	Value must be between 0 and 1023	1	Specify the Vsync signal assertion lines in a frame.
Output > Timing > Vertical sync signal polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	Low active	Select the polarity of Vsync signal to match to your system.
Output > Timing > Data Enable Signal Polarity	<ul style="list-style-type: none"> <li>• Low active</li> <li>• High active</li> </ul>	High active	Select the polarity of Data Enable signal to match to your system.
Output > Timing > Sync edge	<ul style="list-style-type: none"> <li>• Rising edge</li> <li>• Falling edge</li> </ul>	Rising edge	Select the polarity of Sync signals to match to your system.
Output > Format > Color format	<ul style="list-style-type: none"> <li>• 24bits RGB888</li> <li>• 18bits RGB666</li> <li>• 16bits RGB565</li> <li>• 8bits serial</li> </ul>	16bits RGB565	Specify the graphics layer output format to match to your LCD panel.
Output > Format > Color order	<ul style="list-style-type: none"> <li>• RGB</li> <li>• BGR</li> </ul>	RGB	Select data order for output signal to LCD panel.
Output > Format > Endian	<ul style="list-style-type: none"> <li>• Little endian</li> <li>• Big endian</li> </ul>	Little endian	Select data endianness for output signal to LCD panel.
Output > Background > Alpha	Value must be between 0 and 255	255	Alpha component of the background color.

Output > Background > Red	Value must be between 0 and 255	0	Red component of the background color.
Output > Background > Green	Value must be between 0 and 255	0	Green component of the background color.
Output > Background > Blue	Value must be between 0 and 255	0	Blue component of the background color.
CLUT > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Specify Used if selecting CLUT formats for a graphics layer input format. If used, a buffer (CLUT_buffer) will be automatically generated based on the selected pixel width.
CLUT > Size	Must be a valid non-negative integer with a maximum configurable value of 256	256	Specify the number of entries for the CLUT source data buffer. Each entry consumes 4 bytes (1 word).
TCON > Hsync pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON0	Select the TCON pin used for the Hsync signal to match to your system.
TCON > Vsync pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON1	Select TCON pin used for Vsync signal to match to your system.
TCON > Data enable (DE) pin select	<ul style="list-style-type: none"> <li>• Not used</li> <li>• LCD_TCON0</li> <li>• LCD_TCON1</li> <li>• LCD_TCON2</li> <li>• LCD_TCON3</li> </ul>	LCD_TCON2	Select TCON pin used for DataEnable signal to match to your system.
TCON > Panel clock source	<ul style="list-style-type: none"> <li>• Internal clock (GLCDCLK)</li> <li>• External clock (LCD_EXTCLK)</li> </ul>	Internal clock (GLCDCLK)	Choose between an internal GLCDCLK generated from PCLKA or an external clock provided to the LCD_EXTCLK pin.
TCON > Panel clock division ratio	Refer to the RA Configuration tool for available options.	1/24	Select the clock source divider value.
Color Correction > Brightness > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable brightness color correction.
Color Correction > Brightness > Red	Value must be between 0 and 1023	512	Red component of the brightness calibration.

channel			This value is divided by 512 to determine gain.
Color Correction > Brightness > Green channel	Value must be between 0 and 1023	512	Green component of the brightness calibration. This value is divided by 512 to determine gain.
Color Correction > Brightness > Blue channel	Value must be between 0 and 1023	512	Blue component of the brightness calibration. This value is divided by 512 to determine gain.
Color Correction > Contrast > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable contrast color correction.
Color Correction > Contrast > Red channel gain	Value must be between 0 and 255	128	Red component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Contrast > Green channel gain	Value must be between 0 and 255	128	Green component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Contrast > Blue channel gain	Value must be between 0 and 255	128	Blue component of the contrast calibration. This value is divided by 128 to determine gain.
Color Correction > Gamma > Red	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the red channel.
Color Correction > Gamma > Green	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the green channel.
Color Correction > Gamma > Blue	<ul style="list-style-type: none"> <li>• On</li> <li>• Off</li> </ul>	Off	Enable gamma color correction for the blue channel.
Color Correction > Process order	<ul style="list-style-type: none"> <li>• Brightness/contrast first</li> <li>• Gamma first</li> </ul>	Brightness/contrast first	Select the color correction processing order.
Dithering > Enabled	<ul style="list-style-type: none"> <li>• Yes</li> <li>• No</li> </ul>	No	Enable dithering to reduce the effect of color banding.
Dithering > Mode	<ul style="list-style-type: none"> <li>• Truncate</li> <li>• Round off</li> <li>• 2x2 Pattern</li> </ul>	Truncate	Select the dithering mode.
Dithering > Pattern A	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> </ul>	Pattern 11	Select the dithering pattern.

Dithering > Pattern B	<ul style="list-style-type: none"> <li>• Pattern 11</li> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.
Dithering > Pattern C	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.
Dithering > Pattern D	<ul style="list-style-type: none"> <li>• Pattern 00</li> <li>• Pattern 01</li> <li>• Pattern 10</li> <li>• Pattern 11</li> </ul>	Pattern 11	Select the dithering pattern.

## Clock Configuration

The peripheral clock for this module is PCLKA.

The dot clock is typically generated from the PLL with a maximum output frequency of 54 MHz in most pixel formats (60 MHz for serial RGB). Optionally, a clock signal can be provided to the LCD\_EXTCLK pin for finer framerate control (60 MHz maximum input). With either clock source dividers of 1-9, 12, 16, 24 and 32 may be used. Clocks must be initialized and settled prior to starting this module.

## Pin Configuration

This module controls a variety of pins necessary for LCD data and timing signal output:

Pin Name	Function	Notes
LCD_EXTCLK	External clock signal input	The maximum input clock frequency is 60MHz.
LCD_CLK	Dot clock output	The maximum output frequency is 54MHz (60MHz in serial RGB mode).
LCD_DATAn	Pixel data output lines	Pin assignment and color order is based on the output block configuration. See the RA6M3 User's Manual (R01UH0886EJ0100) section 58.1.4 "Output Control for Data Format" for details.
LCD_TCONn	Panel timing signal output	These pins can be configured to output vertical and horizontal synchronization and data valid signals.

### Note

*There are two banks of pins listed for the GLCDC in the RA6M3 User's Manual (\_A and \_B). In most cases the \_B bank will be used as \_A conflicts with SDRAM pins. In either case, it is generally recommended to only use pins from only one bank at a time as this allows for superior signal routing both inside and outside the package. If \_A*

and *\_B* pins must be mixed be sure to note the timing precision penalty detailed in Table 60.33 in in the RA6M3 User's Manual.

## Usage Notes

### Overview

The GLCDC peripheral is a combination of several sub-peripherals that form a pixel data processing pipeline. Each block passes pixel data to the next but otherwise they are disconnected from one another - in other words, changing timing block parameters does not affect the output generation block configuration and vice versa.

### Initial Configuration

During R\_GLCDC\_Open all configured parameters are set in the GLCDC peripheral fully preparing it for operation. Once opened, calling R\_GLCDC\_Start is typically all that is needed for basic operation. Background generation, timing and output parameters are not configurable at runtime, though layer control and color correction options can be altered.

### Framebuffer Allocation

The framebuffer should be allocated in the highest-speed region available (excluding SRAMHS) without displacing the stack, heap and other program-critical structures. While the RA6M3 does contain a relatively large 640K of on-chip SRAM, for many screen sizes and color depths SDRAM will be required. Regardless of the placement two rules must be followed to ensure correct operation of the GLCDC:

- The framebuffer must be aligned on a 64-byte boundary
- The horizontal stride of the buffer must be a multiple of 64 bytes

#### Note

*Framebuffers allocated through the RA Configuraton tool automatically follow the alignment and size requirements.*

If your framebuffer will be placed into internal SRAM please note the following best practices:

- The framebuffer should ideally not be placed in the SRAMHS block of SRAM as there is no speed advantage for doing so. In particular, it is important to ensure the framebuffer does not push the stack or any heaps outside of SRAMHS to preserve CPU performance.
- It is recommended to not cross the boundary between SRAM0 and SRAM1 with a single framebuffer for performance reasons.
- If double-buffering is desired (and possible within SRAM), place one framebuffer in SRAM0 and the other in SRAM1.

If you are using SRAM for the framebuffer, to ensure correct placement you will need to edit the linker script to add new sections. Below is an example of the required edits in the GCC and IAR formats:

### GCC Linker

```
/*  
  
Linker File for RA6M3 MCU  
  
*/
```

```
/* Linker script to configure memory regions. */
MEMORY
{
    FLASH (rx)          : ORIGIN = 0x00000000, LENGTH = 0x02000000 /* 2M */
    RAM (rwx)           : ORIGIN = 0x1FFE0000, LENGTH = 0x00A00000 /* 640K */
    FB0 (rwx)           : ORIGIN = 0x20000000, LENGTH = 0x00800000 /* 512K */ // Section
for framebuffer 0 (or only framebuffer)
    FB1 (rwx)           : ORIGIN = 0x20040000, LENGTH = 0x00400000 /* 256K */ // Section
for framebuffer 1
    DATA_FLASH (rx)    : ORIGIN = 0x40100000, LENGTH = 0x00100000 /* 64K */
    QSPI_FLASH (rx)     : ORIGIN = 0x60000000, LENGTH = 0x40000000 /* 64M */
    SDRAM (rwx)         : ORIGIN = 0x90000000, LENGTH = 0x20000000 /* 32M */
    ID_CODE (rx)        : ORIGIN = 0x0100A150, LENGTH = 0x10 /* 16 bytes */
}
// ...

.noinit (NOLOAD):
{
    . = ALIGN(4);
    __noinit_start = .;
    KEEP(*(.noinit*))
    __noinit_end = .;
} > RAM

/* Place framebuffer sections first, then the rest of RAM */
.fb0 :
{
    . = ALIGN(64);
    __fb0_start = .;
    *(.fb0*);
    __fb0_end = .;
} > FB0

.fb1 :
{
    . = ALIGN(64);
    __fb1_start = .;
```

```

    * (.fb1*);
    __fb1_end = .;
} > FB1
.bss :
{
    . = ALIGN(4);
    __bss_start__ = .;
    * (.bss*)
    * (COMMON)
    . = ALIGN(4);
    __bss_end__ = .;
} > RAM
// ...

```

## IAR Linker

### Note

The IAR linker does not place items correctly when sections overlap. As a result, it is advised to place your framebuffer(s) as high as possible in the SRAM region in the linker script to maximize the RAM available for everything else. The below is a general case that should be used unedited only if RAM usage (excluding framebuffers) is less than 128K.

```

/* ... */
/*-Memory Regions-*/
define symbol region_VECT_start      = 0x00000000;
define symbol region_VECT_end        = 0x000003FF;
define symbol region_ROMREG_start    = 0x00000400;
define symbol region_ROMREG_end      = 0x000004FF;
define symbol region_FLASH_start     = 0x00000500;
define symbol region_FLASH_end       = 0x001FFFFFF;
define symbol region_RAM_start       = 0x1FFE0000;
define symbol region_RAM_end         = 0x1FFFFFFF; /* RAM limited to SRAMHS */
define symbol region_FB0_start       = 0x20000000;
define symbol region_FB0_end         = 0x2003FFFF; /* SRAM0 dedicated to framebuffer 0 */
/*
define symbol region_FB1_start       = 0x20040000;
define symbol region_FB1_end         = 0x2007FFFF; /* SRAM1 dedicated to framebuffer 1

```

```
*/
define symbol region_DF_start      = 0x40100000;
define symbol region_DF_end        = 0x4010FFFF;
define symbol region_SDRAM_start   = 0x90000000;
define symbol region_SDRAM_end     = 0x91FFFFFF;
define symbol region_QSPI_start    = 0x60000000;
define symbol region_QSPI_end      = 0x63FFFFFF;
/* ... */
define memory mem with size        = 4G;
define region VECT_region          = mem:[from region_VECT_start   to region_VECT_end];
define region ROMREG_region        = mem:[from region_ROMREG_start to region_ROMREG_end];
define region FLASH_region         = mem:[from region_FLASH_start  to
region_FLASH_end];
define region RAM_region           = mem:[from region_RAM_start    to region_RAM_end];
define region FB0_region           = mem:[from region_FB0_start    to region_FB0_end]; /*
Define framebuffer 0 region */
define region FB1_region           = mem:[from region_FB1_start    to region_FB1_end]; /*
Define framebuffer 1 region */
define region DF_region            = mem:[from region_DF_start     to region_DF_end];
define region SDRAM_region         = mem:[from region_SDRAM_start  to
region_SDRAM_end];
define region QSPI_region          = mem:[from region_QSPI_start   to region_QSPI_end];
/* ... */
define block START_OF_RAM with fixed order { rw section .fsp_dtc_vector_table,
                                             block RAM_CODE };
place at start of RAM_region { block START_OF_RAM };
/* Place framebuffer sections first, then the rest of RAM */
place in FB0_region { rw section .fb0 };
place in FB1_region { rw section .fb1 };
place in RAM_region   { rw,
                       rw section .noinit,
                       rw section .bss,
                       rw section .data,
                       rw section HEAP,
```

```
rw section .stack };
```

### Graphics Layers and Timing Parameters

The GLCDC synthesizes graphics data through two configurable graphics layers onto a background layer. The background is used as a solid-color canvas upon which to composite data from the graphics layers. The two graphics layers are blended on top of each other (Layer 2 above Layer 1) and overlaid on the background layer based on their individual configuration. The placement of the layers (as well as LCD timing parameters) are detailed in Figure 1. The colors of the dimensions indicate which element of the `display_cfg_t` struct is being referenced - for example, the width of the background layer would be `[display_cfg].output.htiming.display_cyc` as shown in the figure below.

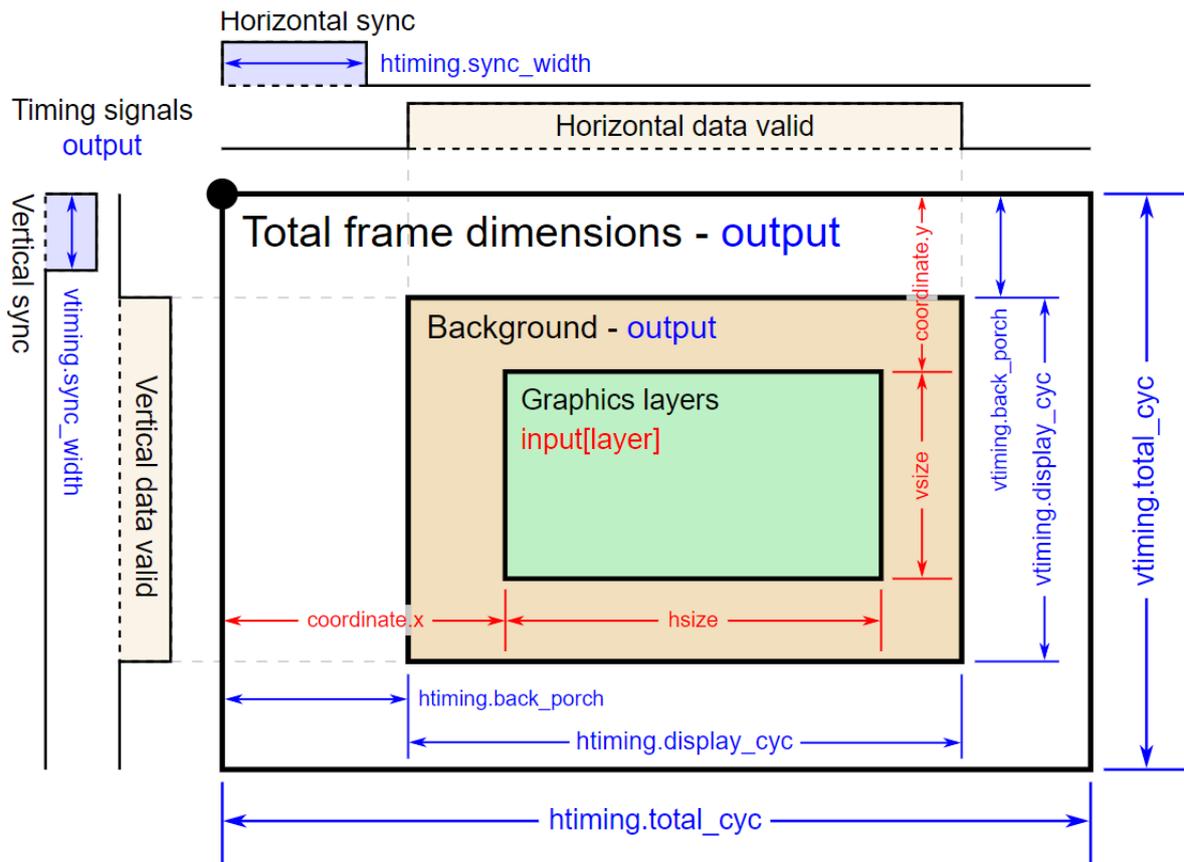


Figure 158: GLCDC layers and timing

*Note*

The data enable signal (if configured) is the logical AND of the horizontal and vertical data valid signals. In the GLCDC layers and timing figure, only one graphics layer is shown for simplicity. Additionally, in most applications the graphics layer(s) will be the same dimensions as the background layer.

### Runtime Configuration Options

*Note*

All runtime configurations detailed below are also automatically configured during `R_GLCDC_Open` based on the options selected in the RA Configuration editor.

## Blend processing

Control of layer positioning, alpha blending and fading is possible at runtime via [R\\_GLCDC\\_LayerChange](#). This function takes a [display\\_runtime\\_cfg\\_t](#) parameter which contains the same input and layer elements as the [display\\_cfg\\_t](#) control block. Refer to the documentation for [display\\_runtime\\_cfg\\_t](#) as well as the [Examples](#) below to see what options are configurable.

## Brightness and contrast

Brightness and contrast correction can be controlled through [R\\_GLCDC\\_ColorCorrection](#). The [display\\_correction\\_t](#) parameter is used to control enabling, disabling and gain values for both corrections as shown below:

```
display_correction_t correction;

/* Brightness values are 0-1023 with +512 offset being neutral */
correction.brightness.r = 512;
correction.brightness.g = 512;
correction.brightness.b = 512;

/* Contrast values are 0-255 representing gain of 0-2 (128 is gain of 1) */
correction.contrast.r = 128;
correction.contrast.g = 128;
correction.contrast.b = 128;

/* Brightness and contrast correction can be enabled or disabled independent of one
another */
correction.brightness.enable = true;
correction.contrast.enable = true;

/* Enable correction */
R_GLCDC_ColorCorrection(&g_disp_ctrl, &correction);
```

## Color Look-Up Table (CLUT) Modes

The GLCDC supports 1-, 4- and 8-bit color look-up table (CLUT) formats for input pixel data. By using these modes the framebuffer size in memory can be reduced significantly, allowing even high-resolution displays to be buffered in on-chip SRAM. To enable CLUT modes for a layer the color format must be set to a CLUT mode (either at startup or through [R\\_GLCDC\\_LayerChange](#)) in addition to filling the CLUT as appropriate via [R\\_GLCDC\\_ClutUpdate](#) as shown below:

```
/* Basic 4-bit (16-color) CLUT definition */
uint32_t clut_4[16] =
{
    0xFF000000, // Black
```

```

0xFFFFFFFF, // White
0xFF0000FF, // Blue
0xFF0080FF, // Turquoise
0xFF00FFFF, // Cyan
0xFF00FF80, // Mint Green
0xFF00FF00, // Green
0xFF80FF00, // Lime Green
0xFFFFFFFF00, // Yellow
0xFFFF8000, // Orange
0xFFFF0000, // Red
0xFFFF0080, // Pink
0xFFFF00FF, // Magenta
0xFF8000FF, // Purple
0xFF808080, // Gray
0x00000000 // Transparent
};

/* Define the CLUT configuration */
display_clut_cfg_t clut_cfg =
{
    .start = 0,
    .size = 16,
    .p_base = clut_4
};

/* Update the CLUT in the GLCDC */
R_GLCDC_ClutUpdate(&g_disp_ctrl, &clut_cfg, DISPLAY_FRAME_LAYER_1);

```

**Note**

*If individual elements of the CLUT must be changed or if elements must be changed one at a time (for instance, when using emWin) it is recommended to use R\_GLCDC\_ClutEdit to avoid repeated memcpy operations.*

**Other Configuration Options****Gamma correction**

Gamma correction is performed based on a gain curve defined in the RA Configuration editor. Each point on the curve is defined by a threshold and a gain value - each gain value represents a multiplier from 0x-2x (set as 0-2047) that sets the Y-value of the slope of the gain curve, while each threshold interval sets the X-value respectively. For a more detailed explanation refer to the RA6M3

User's Manual (R01UH0886EJ0100) Figure 58.12 "Calculation of gamma correction value" and the related description above it.

When setting threshold values three rules must be followed:

- Each threshold value must be greater than the previous value
- Threshold values must be greater than zero and less than 1024
- Threshold values can equal the previous value only if they are 1023 (maximum)

Note

*Gamma correction can only be applied via [R\\_GLCDC\\_Open](#).*

## Dithering

Dithering is a method of pixel blending that allows for smoother transitions between colors when using a limited palette. A full description of dithering is outside the scope of this document. For more information on the pattern settings and how to configure them refer to the RA6M3 User's Manual (R01UH0886EJ0100) Figure 58.13 "Configuration of dither correction block" and Figure 58.14 "Addition value selection method for 2x2 pattern dither".

## Bus Utilization

Note

*The data provided in this section consists of estimates only. Experimentation is necessary to obtain real-world performance data on any platform.*

While the GLCDC is very flexible in size and color depth of displays there are considerations to be made in the tradeoff between color depth, framerate and bus utilization. Below is a table showing estimates of the load at various resolutions, framerates and color depths based on a PLL frequency of 120MHz (default) and an effective SDRAM throughput of 60 MB/sec. Bus utilization percentages are provided for the following use cases:

- Static image display (**GLCDC only**): One read
- Redrawing one framebuffer every display frame (**minimal redraw**): One write, one read
- Blitting one buffer to another then redrawing the entire buffer every display frame (**worst case**): Two writes, three reads

Name	Width	Height	Input color depth (bits)	Framerate (FPS)	Buffer size (bytes)	SRAM use	SRAM bus (GLCDC only)	SDRAM bus (GLCDC only)	SRAM bus (minimal redraw)	SDRAM bus (minimal redraw)	SRAM bus (worst case)	SDRAM bus (worst case)
HQVGA	240	160	8	60	38400	6%	1%	4%	2%	8%	5%	19%
HQVGA	240	160	16	60	76800	12%	2%	8%	4%	15%	10%	38%
QVGA	320	240	16	60	153600	23%	4%	15%	8%	31%	19%	77%
WQVGA	400	240	8	60	96000	15%	2%	10%	5%	19%	12%	48%

WQV GA	400	240	16	60	1920 00	29%	5%	19%	10%	38%	24%	96%
HVGA	480	320	16	60	3072 00	47%	8%	31%	15%	61%	38%	154%
VGA	640	480	16	30	6144 00	—	—	31%	—	61%	—	154%
WVG A	800	480	8	60	3840 00	59%	10%	38%	19%	77%	48%	192%
WVG A	800	480	16	30	7680 00	—	—	38%	—	77%	—	192%
WVG A	800	480	32	15	1536 000	—	—	38%	—	77%	—	192%
FWVG A	960	480	8	30	4608 00	70%	6%	23%	12%	46%	29%	115%
FWVG A	960	480	16	30	9216 00	—	—	46%	—	92%	—	230%
qHD	960	540	8	30	5184 00	79%	6%	26%	13%	52%	32%	130%

**Note**

Bus utilization values over 100% indicate that the bandwidth for that bus is exceeded in that scenario and GLCDC underflow and/or dropped frames may result depending on the bus priority setting. **It is recommended to avoid these scenarios if at all possible by reducing the buffer drawing rate, number of draw/copy operations or the input color depth.** Relaxing vertical timing (increasing total line count) or increasing the clock divider are the easiest ways to increase the time per frame.

**Limitations**

Developers should be aware of the following limitations when using the GLCDC API:

- Due to a limitation of the GLCDC hardware, if the horizontal back porch is less than the number of pixels in a graphics burst read (64 bytes) for a layer and the layer is positioned at a negative X-value then the layer X-position will be locked to the nearest 64-byte boundary, rounded toward zero.
- The GLCDC peripheral offers a chroma-key function that can be used to perform a green-screen-like color replacement. This functionality is not exposed through the GLCDC API. See the descriptions for GRn.AB7 through .AB9 in the RA6M3 User's Manual for further details.
- Use of R\_GLCDC\_ClutUpdate and R\_GLCDC\_ClutEdit may not be mixed on the same frame.

**Examples****Basic Example**

This is a basic example showing the minimum code required to initialize and start the GLCDC module. If the entire display can be drawn within the vertical blanking period no further code may be necessary.

```
void glcdc_init (void)
```

```
{
    fsp_err_t err;
    // Open the GLCDC driver
    err = R_GLCDC_Open(&g_disp_ctrl, &g_disp_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    // Start display output
    err = R_GLCDC_Start(&g_disp_ctrl);
    assert(FSP_SUCCESS == err);
}
```

## Layer Transitions

This example demonstrates how to set up and execute both a sliding and fading layer transition. This is most useful in static image transition scenarios as switching between two actively-drawing graphics layers may require up to four framebuffers to eliminate tearing.

```
volatile uint32_t g_vsync_count = 0;
/* Callback function for GLCDC interrupts */
static void glcdc_callback (display_callback_args_t * p_args)
{
    if (p_args->event == DISPLAY_EVENT_LINE_DETECTION)
    {
        g_vsync_count++;
    }
}
/* Simple wait that returns 1 if no Vsync happened within the timeout period */
uint8_t vsync_wait (void)
{
    uint32_t timeout_timer = GLCDC_VSYNC_TIMEOUT;
    g_vsync_count = 0;
    while (!g_vsync_count && --timeout_timer)
    {
        /* Spin here until DISPLAY_EVENT_LINE_DETECTION callback or timeout */
    }
    return timeout_timer ? 0 : 1;
}
```

```
}
/* Initiate a fade on Layer 2
 *
 * Parameters:
 * direction True for fade in, false for fade out
 * speed number of frames over which to fade
 */
void glcdc_layer_transition_fade (display_runtime_cfg_t * disp_rt_cfg, bool
direction, uint16_t speed)
{
    fsp_err_t err;
    if (direction)
    {
        /* Set the runtime struct to the desired buffer */
        disp_rt_cfg->input.p_base      = (uint32_t *) g_framebuffer_1;
        disp_rt_cfg->layer.fade_control = DISPLAY_FADE_CONTROL_FADEIN;
    }
    else
    {
        disp_rt_cfg->layer.fade_control = DISPLAY_FADE_CONTROL_FADEOUT;
    }
    /* Ensure speed is at least 1 frame */
    if (!speed)
    {
        speed = 1;
    }
    /* Set the fade speed to the desired change in alpha per frame */
    disp_rt_cfg->layer.fade_speed = UINT8_MAX / speed;
    /* Initiate the fade (will start on the next Vsync) */
    err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg, DISPLAY_FRAME_LAYER_2);
    assert(FSP_SUCCESS == err);
}
/* Slide Layer 1 out to the left while sliding Layer 2 in from the right */
void glcdc_layer_transition_sliding (display_runtime_cfg_t * disp_rt_cfg_in,
```

```
display_runtime_cfg_t * disp_rt_cfg_out)
{
    fsp_err_t err;

    /* Set the config for the incoming layer to be just out of bounds on the right side
    */
    disp_rt_cfg_in->input.p_base      = (uint32_t *) g_framebuffer_1;
    disp_rt_cfg_in->layer.coordinate.x = DISPLAY_WIDTH;

    /* Move layer 1 out and layer 2 in at a fixed rate of 4 pixels per frame */
    for (int32_t x = disp_rt_cfg_in->layer.coordinate.x; x >= 0; x -= 4)
    {
        /* Wait for a Vsync before starting */
        vsync_wait();

        /* Set the X-coordinate of both layers then update them */
        disp_rt_cfg_out->layer.coordinate.x = (int16_t) (x - DISPLAY_WIDTH);
        disp_rt_cfg_in->layer.coordinate.x = (int16_t) x;

        err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg_out, DISPLAY_FRAME_LAYER_1
    );

        assert(FSP_SUCCESS == err);

        err = R_GLCDC_LayerChange(&g_disp_ctrl, disp_rt_cfg_in, DISPLAY_FRAME_LAYER_2
    );

        assert(FSP_SUCCESS == err);
    }
}
```

## Double-Buffering

Using a double-buffer allows one to be output to the LCD while the other is being drawn to memory, eliminating tearing and in some cases reducing bus load. The following is a basic example showing integration of the line detect (Vsync) interrupt to set the timing for buffer swapping and drawing.

```
/* User-defined function to draw the current display to a framebuffer */
void display_draw (uint8_t * framebuffer)
{
    FSP_PARAMETER_NOT_USED(framebuffer);

    /* Draw buffer here */
}
```

```
/* This function is an example of a basic double-buffered display thread */
void display_thread (void)
{
    uint8_t * p_framebuffer = NULL;
    fsp_err_t err;
    /* Initialize and start the R_GLCDC module */
    glcdc_init();
    while (1)
    {
        /* Swap the active framebuffer */
        p_framebuffer = (p_framebuffer == g_framebuffer_0) ? g_framebuffer_1 :
g_framebuffer_0;
        /* Draw the new framebuffer now */
        display_draw(p_framebuffer);
        /* Now that the framebuffer is ready, update the GLCDC buffer pointer on the next
Vsync */
        err = R_GLCDC_BufferChange(&g_disp_ctrl, p_framebuffer, DISPLAY_FRAME_LAYER_1
);
        assert(FSP_SUCCESS == err);
        /* Wait for a Vsync event */
        vsync_wait();
    }
}
```

## Data Structures

struct [glcdc\\_instance\\_ctrl\\_t](#)

struct [glcdc\\_extended\\_cfg\\_t](#)

## Enumerations

enum [glcdc\\_clk\\_src\\_t](#)

enum [glcdc\\_panel\\_clk\\_div\\_t](#)

enum [glcdc\\_tcon\\_pin\\_t](#)

enum [glcdc\\_bus\\_arbitration\\_t](#)

enum [glcdc\\_correction\\_proc\\_order\\_t](#)enum [glcdc\\_tcon\\_signal\\_select\\_t](#)enum [glcdc\\_clut\\_plane\\_t](#)enum [glcdc\\_dithering\\_mode\\_t](#)enum [glcdc\\_dithering\\_pattern\\_t](#)enum [glcdc\\_input\\_interface\\_format\\_t](#)enum [glcdc\\_output\\_interface\\_format\\_t](#)enum [glcdc\\_dithering\\_output\\_format\\_t](#)

## Data Structure Documentation

### ◆ [glcdc\\_instance\\_ctrl\\_t](#)

struct [glcdc\\_instance\\_ctrl\\_t](#)

Display control block. DO NOT INITIALIZE.

### ◆ [glcdc\\_extended\\_cfg\\_t](#)

struct [glcdc\\_extended\\_cfg\\_t](#)

GLCDC hardware specific configuration

#### Data Fields

<a href="#">glcdc_tcon_pin_t</a>	tcon_hsync	GLCDC TCON output pin select.
<a href="#">glcdc_tcon_pin_t</a>	tcon_vsync	GLCDC TCON output pin select.
<a href="#">glcdc_tcon_pin_t</a>	tcon_de	GLCDC TCON output pin select.
<a href="#">glcdc_correction_proc_order_t</a>	correction_proc_order	Correction control route select.
<a href="#">glcdc_clk_src_t</a>	clksrc	Clock Source selection.
<a href="#">glcdc_panel_clk_div_t</a>	clock_div_ratio	Clock divide ratio for dot clock.
<a href="#">glcdc_dithering_mode_t</a>	dithering_mode	Dithering mode.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_A	Dithering pattern A.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_B	Dithering pattern B.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_C	Dithering pattern C.
<a href="#">glcdc_dithering_pattern_t</a>	dithering_pattern_D	Dithering pattern D.

## Enumeration Type Documentation

◆ **glcdc\_clk\_src\_t**

enum glcdc_clk_src_t	
Clock source select	
Enumerator	
GLCDC_CLK_SRC_INTERNAL	Internal.
GLCDC_CLK_SRC_EXTERNAL	External.

◆ **glcdc\_panel\_clk\_div\_t**

enum glcdc_panel_clk_div_t	
Clock frequency division ratio	
Enumerator	
GLCDC_PANEL_CLK_DIVISOR_1	Division Ratio 1/1.
GLCDC_PANEL_CLK_DIVISOR_2	Division Ratio 1/2.
GLCDC_PANEL_CLK_DIVISOR_3	Division Ratio 1/3.
GLCDC_PANEL_CLK_DIVISOR_4	Division Ratio 1/4.
GLCDC_PANEL_CLK_DIVISOR_5	Division Ratio 1/5.
GLCDC_PANEL_CLK_DIVISOR_6	Division Ratio 1/6.
GLCDC_PANEL_CLK_DIVISOR_7	Division Ratio 1/7.
GLCDC_PANEL_CLK_DIVISOR_8	Division Ratio 1/8.
GLCDC_PANEL_CLK_DIVISOR_9	Division Ratio 1/9.
GLCDC_PANEL_CLK_DIVISOR_12	Division Ratio 1/12.
GLCDC_PANEL_CLK_DIVISOR_16	Division Ratio 1/16.
GLCDC_PANEL_CLK_DIVISOR_24	Division Ratio 1/24.
GLCDC_PANEL_CLK_DIVISOR_32	Division Ratio 1/32.

◆ **glcdc\_tcon\_pin\_t**

enum <code>glcdc_tcon_pin_t</code>	
LCD TCON output pin select	
Enumerator	
<code>GLCDC_TCON_PIN_NONE</code>	No output.
<code>GLCDC_TCON_PIN_0</code>	LCD_TCON0.
<code>GLCDC_TCON_PIN_1</code>	LCD_TCON1.
<code>GLCDC_TCON_PIN_2</code>	LCD_TCON2.
<code>GLCDC_TCON_PIN_3</code>	LCD_TCON3.

◆ **glcdc\_bus\_arbitration\_t**

enum <code>glcdc_bus_arbitration_t</code>	
Bus Arbitration setting	
Enumerator	
<code>GLCDC_BUS_ARBITRATION_ROUNDROBIN</code>	Round robin.
<code>GLCDC_BUS_ARBITRATION_FIX_PRIORITY</code>	Fixed.

◆ **glcdc\_correction\_proc\_order\_t**

enum <code>glcdc_correction_proc_order_t</code>	
Correction circuit sequence control	
Enumerator	
<code>GLCDC_CORRECTION_PROC_ORDER_BRIGHTNESS_CONTRAST2GAMMA</code>	Brightness -> contrast -> gamma correction.
<code>GLCDC_CORRECTION_PROC_ORDER_GAMMA2BRIGHTNESS_CONTRAST</code>	Gamma correction -> brightness -> contrast.

◆ **glcdc\_tcon\_signal\_select\_t**

enum <a href="#">glcdc_tcon_signal_select_t</a>	
Timing signals for driving the LCD panel	
Enumerator	
GLCDC_TCON_SIGNAL_SELECT_STVA_VS	STVA/VS.
GLCDC_TCON_SIGNAL_SELECT_STVB_VE	STVB/VE.
GLCDC_TCON_SIGNAL_SELECT_STHA_HS	STH/SP/HS.
GLCDC_TCON_SIGNAL_SELECT_STHB_HE	STB/LP/HE.
GLCDC_TCON_SIGNAL_SELECT_DE	DE.

◆ **glcdc\_clut\_plane\_t**

enum <a href="#">glcdc_clut_plane_t</a>	
Clock phase adjustment for serial RGB output	
Enumerator	
GLCDC_CLUT_PLANE_0	GLCDC CLUT plane 0.
GLCDC_CLUT_PLANE_1	GLCDC CLUT plane 1.

◆ **glcdc\_dithering\_mode\_t**

enum <a href="#">glcdc_dithering_mode_t</a>	
Dithering mode	
Enumerator	
GLCDC_DITHERING_MODE_TRUNCATE	No dithering (truncate)
GLCDC_DITHERING_MODE_ROUND_OFF	Dithering with round off.
GLCDC_DITHERING_MODE_2X2PATTERN	Dithering with 2x2 pattern.

◆ **glcdc\_dithering\_pattern\_t**

enum <code>glcdc_dithering_pattern_t</code>	
Dithering mode	
Enumerator	
<code>GLCDC_DITHERING_PATTERN_00</code>	2x2 pattern '00'
<code>GLCDC_DITHERING_PATTERN_01</code>	2x2 pattern '01'
<code>GLCDC_DITHERING_PATTERN_10</code>	2x2 pattern '10'
<code>GLCDC_DITHERING_PATTERN_11</code>	2x2 pattern '11'

◆ **glcdc\_input\_interface\_format\_t**

enum <code>glcdc_input_interface_format_t</code>	
Output interface format	
Enumerator	
<code>GLCDC_INPUT_INTERFACE_FORMAT_RGB565</code>	Input interface format RGB565.
<code>GLCDC_INPUT_INTERFACE_FORMAT_RGB888</code>	Input interface format RGB888.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB1555</code>	Input interface format ARGB1555.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB4444</code>	Input interface format ARGB4444.
<code>GLCDC_INPUT_INTERFACE_FORMAT_ARGB8888</code>	Input interface format ARGB8888.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT8</code>	Input interface format CLUT8.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT4</code>	Input interface format CLUT4.
<code>GLCDC_INPUT_INTERFACE_FORMAT_CLUT1</code>	Input interface format CLUT1.

◆ **glcdc\_output\_interface\_format\_t**

enum <code>glcdc_output_interface_format_t</code>	
Output interface format	
Enumerator	
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB888</code>	Output interface format RGB888.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB666</code>	Output interface format RGB666.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_RGB565</code>	Output interface format RGB565.
<code>GLCDC_OUTPUT_INTERFACE_FORMAT_SERIAL_RGB</code>	Output interface format Serial RGB.

◆ **glcdc\_dithering\_output\_format\_t**

enum <code>glcdc_dithering_output_format_t</code>	
Dithering output format	
Enumerator	
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB888</code>	Dithering output format RGB888.
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB666</code>	Dithering output format RGB666.
<code>GLCDC_DITHERING_OUTPUT_FORMAT_RGB565</code>	Dithering output format RGB565.

**Function Documentation**

◆ **R\_GLCDC\_Open()**

```
fsp_err_t R_GLCDC_Open ( display_ctrl_t *const p_api_ctrl, display_cfg_t const *const p_cfg )
```

Open GLCDC module. Implements `display_api_t::open`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ALREADY_OPEN	Device was already open.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_CLOCK_GENERATION	Dot clock cannot be generated from clock source.
FSP_ERR_INVALID_TIMING_SETTING	Invalid panel timing parameter.
FSP_ERR_INVALID_LAYER_SETTING	Invalid layer setting found.
FSP_ERR_INVALID_ALIGNMENT	Input buffer alignment invalid.
FSP_ERR_INVALID_GAMMA_SETTING	Invalid gamma correction setting found
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid brightness correction setting found

**Note**

*PCLKA must be supplied to Graphics LCD Controller (GLCDC) and GLCDC pins must be set in IOPORT before calling this API.*

◆ **R\_GLCDC\_Close()**

```
fsp_err_t R_GLCDC_Close ( display_ctrl_t *const p_api_ctrl)
```

Close GLCDC module. Implements `display_api_t::close`.

**Return values**

FSP_SUCCESS	Device was closed successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	The function call is performed when the driver state is not equal to <code>DISPLAY_STATE_CLOSED</code> .
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed when the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is not in `DISPLAY_STATE_CLOSED` state. It returns an error if the register update operation for the background screen generation block is being held.*

◆ **R\_GLCDC\_Start()**

```
fsp_err_t R_GLCDC_Start ( display_ctrl_t *const p_api_ctrl)
```

Start GLCDC module. Implements `display_api_t::start`.

**Return values**

FSP_SUCCESS	Device was started successfully.
FSP_ERR_NOT_OPEN	GLCDC module has not been opened.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.

**Note**

*This API can be called when the driver is not in `DISPLAY_STATE_OPENED` status.*

◆ **R\_GLCDC\_Stop()**

```
fsp_err_t R_GLCDC_Stop ( display_ctrl_t *const p_api_ctrl)
```

Stop GLCDC module. Implements `display_api_t::stop`.

**Return values**

FSP_SUCCESS	Device was stopped successfully
FSP_ERR_ASSERTION	Pointer to the control block is NULL
FSP_ERR_INVALID_MODE	Function call is performed when the driver state is not <code>DISPLAY_STATE_DISPLAYING</code> .
FSP_ERR_INVALID_UPDATE_TIMING	The function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in the `DISPLAY_STATE_DISPLAYING` state. It returns an error if the register update operation for the background screen generation blocks, the graphics data I/F blocks, or the output control block is being held.*

◆ **R\_GLCDC\_LayerChange()**

```
fsp_err_t R_GLCDC_LayerChange ( display_ctrl_t const *const p_api_ctrl, display_runtime_cfg_t
const *const p_cfg, display_frame_layer_t layer )
```

Change layer parameters of GLCDC module at runtime. Implements `display_api_t::layerChange`.

**Return values**

FSP_SUCCESS	Changed layer parameters of GLCDC module successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_INVALID_MODE	A function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in DISPLAY\_STATE\_DISPLAYING state. It returns an error if the register update operation for the background screen generation blocks or the graphics data I/F block is being held.*

◆ **R\_GLCDC\_BufferChange()**

```
fsp_err_t R_GLCDC_BufferChange ( display_ctrl_t const *const p_api_ctrl, uint8_t *const
framebuffer, display_frame_layer_t layer )
```

Change the framebuffer pointer for a layer. Implements `display_api_t::bufferChange`.

**Return values**

FSP_SUCCESS	Changed layer parameters of GLCDC module successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_INVALID_MODE	A function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_ALIGNMENT	The framebuffer pointer is not 64-byte aligned.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating register values internally.

**Note**

*This API can be called when the driver is in DISPLAY\_STATE\_OPENED state or higher. It returns an error if the register update operation for the background screen generation blocks or the graphics data I/F block is being held.*

◆ **R\_GLCDC\_ColorCorrection()**

```
fsp_err_t R_GLCDC_ColorCorrection ( display_ctrl_t const *const p_api_ctrl, display_correction_t const *const p_correction )
```

Perform color correction through the GLCDC module. Implements `display_api_t::correction`.

**Return values**

FSP_SUCCESS	Color correction by GLCDC module was performed successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the display correction structure is NULL.
FSP_ERR_INVALID_MODE	Function call is performed when the driver state is not DISPLAY_STATE_DISPLAYING.
FSP_ERR_INVALID_UPDATE_TIMING	A function call is performed while the GLCDC is updating registers internally.
FSP_ERR_INVALID_BRIGHTNESS_SETTING	Invalid brightness correction setting found

**Note**

*This API can be called when the driver is in the DISPLAY\_STATE\_DISPLAYING state. It returns an error if the register update operation for the background screen generation blocks or the output control block is being held.*

◆ **R\_GLCDC\_ClutUpdate()**

```
fsp_err_t R_GLCDC_ClutUpdate ( display_ctrl_t const *const p_api_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer )
```

Write an entire color look-up table (CLUT) in the GLCDC module. Implements `display_api_t::clut`.

**Return values**

FSP_SUCCESS	CLUT written successfully.
FSP_ERR_ASSERTION	Pointer to the control block or CLUT source data is NULL.
FSP_ERR_INVALID_UPDATE_TIMING	R_GLCDC_ClutEdit was already used to edit the specified CLUT this frame.
FSP_ERR_INVALID_CLUT_ACCESS	Illegal CLUT entry or size is specified.

**Note**

*This API can be called any time. The written data will be used after the next vertical sync event.*

◆ **R\_GLCDC\_ClutEdit()**

```
fsp_err_t R_GLCDC_ClutEdit ( display_ctrl_t const *const p_api_ctrl, display_frame_layer_t layer,
uint8_t index, uint32_t color )
```

Update an element of a color look-up table (CLUT) in the GLCDC module. Implements `display_api_t::clutEdit`.

**Return values**

FSP_SUCCESS	CLUT element updated successfully.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.

*Note*

*This API can be called any time. The written data will be used after the next vertical sync event.*

◆ **R\_GLCDC\_StatusGet()**

```
fsp_err_t R_GLCDC_StatusGet ( display_ctrl_t const *const p_api_ctrl, display_status_t *const
p_status )
```

Get status of GLCDC module. Implements `display_api_t::statusGet`.

**Return values**

FSP_SUCCESS	Got status successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the status structure is NULL.

*Note*

*The GLCDC hardware starts the fading processing at the first Vsync after the previous LayerChange() call is held. Due to this behavior of the hardware, this API may not return DISPLAY\_FADE\_STATUS\_FADING\_UNDERWAY as the fading status, if it is called before the first Vsync after LayerChange() is called. In this case, the API returns DISPLAY\_FADE\_STATUS\_PENDING, instead of DISPLAY\_FADE\_STATUS\_NOT\_UNDERWAY.*

**4.2.25 General PWM Timer (r\_gpt)**

## Modules

**Functions**

```
fsp_err_t R_GPT_Open (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_GPT_Stop (timer_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_GPT_Start (timer_ctrl_t *const p_ctrl)
```

fsp_err_t	R_GPT_Reset (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Enable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_Disable (timer_ctrl_t *const p_ctrl)
fsp_err_t	R_GPT_PeriodSet (timer_ctrl_t *const p_ctrl, uint32_t const period_counts)
fsp_err_t	R_GPT_DutyCycleSet (timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin)
fsp_err_t	R_GPT_InfoGet (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
fsp_err_t	R_GPT_StatusGet (timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)
fsp_err_t	R_GPT_CounterSet (timer_ctrl_t *const p_ctrl, uint32_t counter)
fsp_err_t	R_GPT_OutputEnable (timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin)
fsp_err_t	R_GPT_OutputDisable (timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin)
fsp_err_t	R_GPT_AdcTriggerSet (timer_ctrl_t *const p_ctrl, gpt_adc_compare_match_t which_compare_match, uint32_t compare_match_value)
fsp_err_t	R_GPT_CallbackSet (timer_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)
fsp_err_t	R_GPT_Close (timer_ctrl_t *const p_ctrl)

## Detailed Description

Driver for the GPT32 and GPT16 peripherals on RA MCUs. This module implements the [Timer Interface](#).

## Overview

The GPT module can be used to count events, measure external input signals, generate a periodic interrupt, or output a periodic or PWM signal to a GTIOC pin.

This module supports the GPT peripherals GPT32EH, GPT32E, GPT32, and GPT16. GPT16 is a 16-bit timer. The other peripherals (GPT32EH, GPT32E, and GPT32) are 32-bit timers. The 32-bit timers are all treated the same in this module from the API perspective.

## Features

The GPT module has the following features:

- Supports periodic mode, one-shot mode, and PWM mode.
- Supports count source of PCLK, GTETRГ pins, GTIOC pins, or ELC events.
- Supports debounce filter on GTIOC pins.
- Signal can be output to a pin.
- Configurable period (counts per timer cycle).
- Configurable duty cycle in PWM mode.
- Supports runtime reconfiguration of period.
- Supports runtime reconfiguration of duty cycle in PWM mode.
- APIs are provided to start, stop, and reset the counter.
- APIs are provided to get the current period, source clock frequency, and count direction.
- APIs are provided to get the current timer status and counter value.
- Supports start, stop, clear, count up, count down, and capture by external sources from GTETRГ pins, GTIOC pins, or ELC events.
- Supports symmetric and asymmetric PWM waveform generation.
- Supports automatic addition of dead time.
- Supports generating ELC events to start an ADC scan at a compare match value (see [Event Link Controller \(r\\_elc\)](#)) and updating the compare match value.
- Supports linking with a POEG channel to automatically disable GPT output when an error condition is detected.
- Supports setting the counter value while the timer is stopped.
- Supports enabling and disabling output pins.
- Supports skipping up to seven overflow/underflow (crest/trough) interrupts at a time
- Supports generating custom PWM waveforms by configuring the pin's output level at each compare match and cycle end.

## Selecting a Timer

RA MCUs have two timer peripherals: the General PWM Timer (GPT) and the Asynchronous General Purpose Timer (AGT). When selecting between them, consider these factors:

	GPT	AGT
Low Power Modes	The GPT can operate in sleep mode.	The AGT can operate in all low power modes.
Available Channels	The number of GPT channels is device specific. All currently supported MCUs have at least 7 GPT channels.	All MCUs have 2 AGT channels.
Timer Resolution	All MCUs have at least one 32-bit GPT timer.	The AGT timers are 16-bit timers.
Clock Source	The GPT runs off PCLKD with a configurable divider up to 1024. It can also be configured to count ELC events or external pulses.	The AGT runs off PCLKB, LOCO, or subclock.

## Configuration

### Build Time Configurations for r\_gpt

The following build time configurations are defined in fsp\_cfg/r\_gpt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Pin Output Support	<ul style="list-style-type: none"> <li>Disabled</li> <li>Enabled</li> <li>Enabled with Extra Features</li> </ul>	Disabled	Enables or disables support for outputting PWM waveforms on GTIOCx pins. The "Enabled with Extra Features" option enables support for Triangle wave modes and also enables the features located in the "Extra Features" section of each module instance.
Write Protect Enable	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If selected write protection is applied to all GPT channels.

### Configurations for Driver > Timers > Timer Driver on r\_gpt

This module can be added to the Stacks tab via New Stack > Driver > Timers > Timer Driver on r\_gpt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_timer0	Module name.
General > Channel	Channel number must exist on this MCU	0	Specify the hardware channel.
General > Mode	<ul style="list-style-type: none"> <li>Periodic</li> <li>One-Shot</li> <li>PWM</li> <li>Triangle-Wave Symmetric PWM</li> <li>Triangle-Wave Asymmetric PWM</li> <li>Triangle-Wave Asymmetric PWM (Mode 3)</li> </ul>	Periodic	<p>Mode selection.</p> <p>Periodic: Generates periodic interrupts or square waves.</p> <p>One-shot: Generate a single interrupt or a pulse wave. Note: One-shot mode is implemented in software. ISRs must be enabled for one-shot even if callback is unused.</p> <p>PWM: Generates basic PWM waveforms.</p> <p>Triangle-Wave Symmetric PWM: Generates symmetric PWM waveforms with</p>

duty cycle determined by compare match set during a crest interrupt and updated at the next trough.

Triangle-Wave

Asymmetric PWM:

Generates asymmetric PWM waveforms with duty cycle determined by compare match set during a crest/trough interrupt and updated at the next trough/crest.

General > Period	Value must be a non-negative integer less than or equal to 0x400000000000	0x100000000	Specify the timer period in units selected below. Setting the period to 0x100000000 raw counts results in the maximum period. Set the period to 0x100000000 raw counts for a free running timer or an input capture configuration. The period can be set up to 0x400000000000, which will use a divider of 1024 with the maximum period.
General > Period Unit	<ul style="list-style-type: none"> <li>• Raw Counts</li> <li>• Nanoseconds</li> <li>• Microseconds</li> <li>• Milliseconds</li> <li>• Seconds</li> <li>• Hertz</li> <li>• Kilohertz</li> </ul>	Raw Counts	If the requested period cannot be achieved, the settings with the largest possible period that is less than or equal to the requested period are used. The theoretical calculated period is printed in a comment in the generated <a href="#">timer_cfg_t</a> structure.
Output > Custom	<ul style="list-style-type: none"> <li>• Pin Level Low</li> </ul>	Pin Level Low	Unit of the period specified above
			Set the initial output

Waveform > GTIOA > Initial Output Level	<ul style="list-style-type: none"> <li>• Pin Level High</li> </ul>		level of GTIOCxA.
Output > Custom Waveform > GTIOA > Cycle End Output Level	<ul style="list-style-type: none"> <li>• Pin Level Retain</li> <li>• Pin Level Low</li> <li>• Pin Level High</li> <li>• Pin Level Toggle</li> </ul>	Pin Level Retain	Set the output level of GTIOCxA at cycle end.
Output > Custom Waveform > GTIOA > Compare Match Output Level	<ul style="list-style-type: none"> <li>• Pin Level Retain</li> <li>• Pin Level Low</li> <li>• Pin Level High</li> <li>• Pin Level Toggle</li> </ul>	Pin Level Retain	Set the output level of GTIOCxA at compare match.
Output > Custom Waveform > GTIOA > Retain Output Level at Count Stop	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Retain the current GTIOxA output level when counting is stopped.
Output > Custom Waveform > GTIOB > Initial Output Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Set the initial output level of GTIOCxB.
Output > Custom Waveform > GTIOB > Cycle End Output Level	<ul style="list-style-type: none"> <li>• Pin Level Retain</li> <li>• Pin Level Low</li> <li>• Pin Level High</li> <li>• Pin Level Toggle</li> </ul>	Pin Level Retain	Set the output level of GTIOCxB at cycle end.
Output > Custom Waveform > GTIOB > Compare Match Output Level	<ul style="list-style-type: none"> <li>• Pin Level Retain</li> <li>• Pin Level Low</li> <li>• Pin Level High</li> <li>• Pin Level Toggle</li> </ul>	Pin Level Retain	Set the output level of GTIOCxB at compare match.
Output > Custom Waveform > GTIOB > Retain Output Level at Count Stop	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Retain the current GTIOxB output level when counting is stopped.
Output > Custom Waveform > Custom Waveform Enable	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable custom waveform configuration.
Output > Duty Cycle Percent (only applicable in PWM mode)	Value must be between 0 and 100	50	Specify the timer duty cycle percent. Only used in PWM mode.
Output > GTIOCA Output Enabled	<ul style="list-style-type: none"> <li>• True</li> <li>• False</li> </ul>	False	Enable the output of GTIOCA on a pin.
Output > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Output > GTIOCB Output Enabled	<ul style="list-style-type: none"> <li>• True</li> <li>• False</li> </ul>	False	Enable the output of GTIOCB on a pin.

Output > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Input > Count Up Source	MCU Specific Options		Select external source that will increment the counter. If any count up source is selected, the timer will count the external sources only. It will not count PCLKD cycles.
Input > Count Down Source	MCU Specific Options		Select external source that will decrement the counter. If any count down source is selected, the timer will count the external sources only. It will not count PCLKD cycles.
Input > Start Source	MCU Specific Options		Select external source that will start the timer.  For pulse width measurement, set the Start Source and the Clear Source to the trigger edge (the edge to start the measurement), and set the Stop Source and Capture Source (either A or B) to the opposite edge (the edge to stop the measurement).  For pulse period measurement, set the Start Source, the Clear Source, and the Capture Source (either A or B) to the trigger edge (the edge to start the measurement).
Input > Stop Source	MCU Specific Options		Select external source that will stop the timer.
Input > Clear Source	MCU Specific Options		Select external source that will clear the timer.
Input > Capture A Source	MCU Specific Options		Select external source that will trigger a capture A event.

Input > Capture B Source	MCU Specific Options		Select external source that will trigger a capture B event.
Input > Noise Filter A Sampling Clock Select	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter PCLKD / 1</li> <li>• Filter PCLKD / 4</li> <li>• Filter PCLKD / 16</li> <li>• Filter PCLKD / 64</li> </ul>	No Filter	Select the input filter for GTIOCA.
Input > Noise Filter B Sampling Clock Select	<ul style="list-style-type: none"> <li>• No Filter</li> <li>• Filter PCLKD / 1</li> <li>• Filter PCLKD / 4</li> <li>• Filter PCLKD / 16</li> <li>• Filter PCLKD / 64</li> </ul>	No Filter	Select the input filter for GTIOCB.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function can be specified here. If this callback function is provided, it will be called from the interrupt service routine (ISR) each time the timer period elapses
Interrupts > Overflow/Crest Interrupt Priority	MCU Specific Options		Select the overflow interrupt priority. This is the crest interrupt for triangle-wave PWM.
Interrupts > Capture A Interrupt Priority	MCU Specific Options		Select the interrupt priority for capture A.
Interrupts > Capture B Interrupt Priority	MCU Specific Options		Select the interrupt priority for capture B.
Interrupts > Underflow/Trough Interrupt Priority	MCU Specific Options		Select the interrupt priority for the trough interrupt (triangle-wave PWM only).
Extra Features > Output Disable > POEG Link	<ul style="list-style-type: none"> <li>• POEG Channel 0</li> <li>• POEG Channel 1</li> <li>• POEG Channel 2</li> <li>• POEG Channel 3</li> </ul>	POEG Channel 0	Select which POEG to link this GPT channel to.
Extra Features > Output Disable >	<ul style="list-style-type: none"> <li>• Dead Time Error</li> </ul>		Select which errors send an output disable

Output Disable POEG Trigger	<ul style="list-style-type: none"> <li>• GTIOCA and GTIOCB High Level</li> <li>• GTIOCA and GTIOCB Low Level</li> </ul>		trigger to POEG. Dead time error is only available on GPT32E and GPT32EH variants.
Extra Features > Output Disable > GTIOCA Disable Setting	<ul style="list-style-type: none"> <li>• Disable Prohibited</li> <li>• Set Hi Z</li> <li>• Level Low</li> <li>• Level High</li> </ul>	Disable Prohibited	Select the disable setting for GTIOCA.
Extra Features > Output Disable > GTIOCB Disable Setting	<ul style="list-style-type: none"> <li>• Disable Prohibited</li> <li>• Set Hi Z</li> <li>• Level Low</li> <li>• Level High</li> </ul>	Disable Prohibited	Select the disable setting for GTIOCB.
Extra Features > ADC Trigger > Start Event Trigger (GPTE/GPTEH only)	<ul style="list-style-type: none"> <li>• Trigger Event A/D Converter Start Request A During Up Counting</li> <li>• Trigger Event A/D Converter Start Request A During Down Counting</li> <li>• Trigger Event A/D Converter Start Request B During Up Counting</li> <li>• Trigger Event A/D Converter Start Request B During Down Counting</li> </ul>		Select which A/D converter start request interrupts to generate and at which point in the cycle to generate them. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Dead Time > Dead Time Count Up (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the dead time to apply during up counting. This value also applies during down counting for the GPT32 and GPT16 variants.
Extra Features > Dead Time > Dead Time Count Down (Raw Counts) (GPTE/GPTEH only)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the dead time to apply during down counting. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > ADC Trigger (GPTE/GPTEH	Must be a valid non-negative integer with a	0	Select the compare match value that

only) > ADC A Compare Match (Raw Counts)	maximum configurable value of 4294967295 (0xffffffff).		generates a GPTn AD TRIG A event. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > ADC Trigger (GPTE/GPTEH only) > ADC B Compare Match (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the compare match value that generates a GPTn AD TRIG B event. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Interrupt to Count	<ul style="list-style-type: none"> <li>• None</li> <li>• Overflow and Underflow (sawtooth)</li> <li>• Crest (triangle)</li> <li>• Trough (triangle)</li> </ul>	None	Select the count source for interrupt skipping. The interrupt skip counter increments after each source event. All crest/overflow and trough/underflow interrupts are skipped when the interrupt skip counter is non-zero. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Interrupt Skip Count	<ul style="list-style-type: none"> <li>• 0</li> <li>• 1</li> <li>• 2</li> <li>• 3</li> <li>• 4</li> <li>• 5</li> <li>• 6</li> <li>• 7</li> </ul>	0	Select the number of interrupts to skip. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Interrupt Skipping (GPTE/GPTEH only) > Skip ADC Events	<ul style="list-style-type: none"> <li>• None</li> <li>• ADC A Compare Match</li> <li>• ADC B Compare Match</li> <li>• ADC A and B Compare Match</li> </ul>	module.driver.timer.interrupt_skip.adc.none	Select ADC events to suppress when the interrupt skip count is not zero. This value only applies to the GPT32E and GPT32EH variants.
Extra Features > Extra Features	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select whether to enable extra features on this channel.

## Clock Configuration

The GPT clock is based on the PCLKD frequency. You can set the PCLKD frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time.

## Pin Configuration

This module can use GTETRGA, GTETRGB, GTETRGC, GTETRGD, GTIOCA and GTIOCB pins as count sources.

This module can use GTIOCA and GTIOCB pins as output pins for periodic or PWM signals.

This module can use GTIOCA and GTIOCB as input pins to measure input signals.

## Usage Notes

### Maximum Period for GPT32

The RA Configuration editor will automatically calculate the period count value and source clock divider based on the selected period time, units and clock speed.

When the selected period unit is "Raw counts", the maximum period setting is 0x4000000000 on a 32-bit timer or 0x0x4000000 on a 16-bit timer. This will configure the timer with the maximum period and a count clock divisor of 128.

#### Note

*When manually changing the timer period counts the maximum value for a 32-bit GPT is 0x100000000. This number overflows the 32-bit value for `timer_cfg_t::period_counts`. To configure the timer for the maximum period, set `timer_cfg_t::period_counts` to 0.*

### Updating Period and Duty Cycle

The period and duty cycle are updated after the next counter overflow after calling `R_GPT_PeriodSet()` or `R_GPT_DutyCycleSet()`. To force them to update before the next counter overflow, call `R_GPT_Reset()` while the counter is running.

### One-Shot Mode

The GPT timer does not support one-shot mode natively. One-shot mode is achieved by stopping the timer in the interrupt service routine before the callback is called. If the interrupt is not serviced before the timer period expires again, the timer generates more than one event. The callback is only called once in this case, but multiple events may be generated if the timer is linked to the [Data Transfer Controller \(r\\_dtc\)](#).

### One-Shot Mode Output

The output waveform in one-shot mode is one PCLKD cycle less than the configured period. The configured period must be at least 2 counts to generate an output pulse.

Examples of one-shot signals that can be generated by this module are shown below:

## GPT One-Shot Output

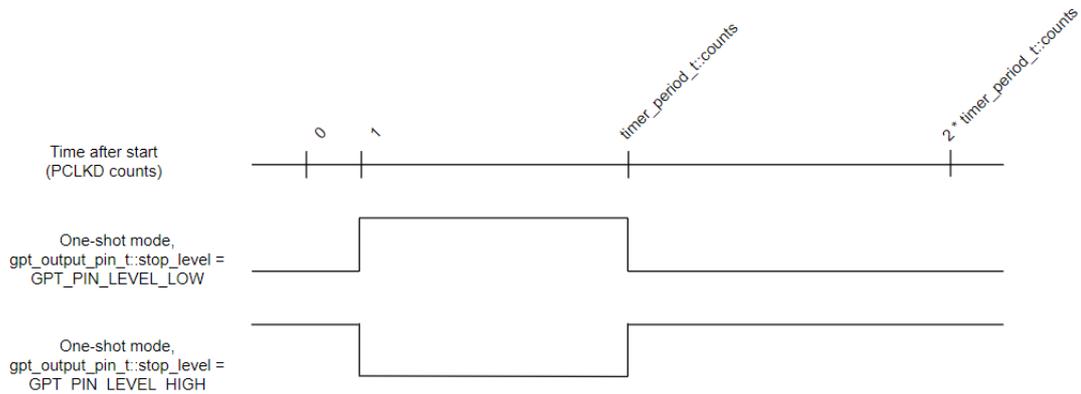


Figure 159: GPT One-Shot Output

## Periodic Output

The GTIOC pin toggles twice each time the timer expires in periodic mode. This is achieved by defining a PWM wave at a 50 percent duty cycle so that the period of the resulting square wave (from rising edge to rising edge) matches the period of the GPT timer. Since the periodic output is actually a PWM output, the time at the stop level is one cycle shorter than the time opposite the stop level for odd period values.

Examples of periodic signals that can be generated by this module are shown below:

## GPT Periodic Output

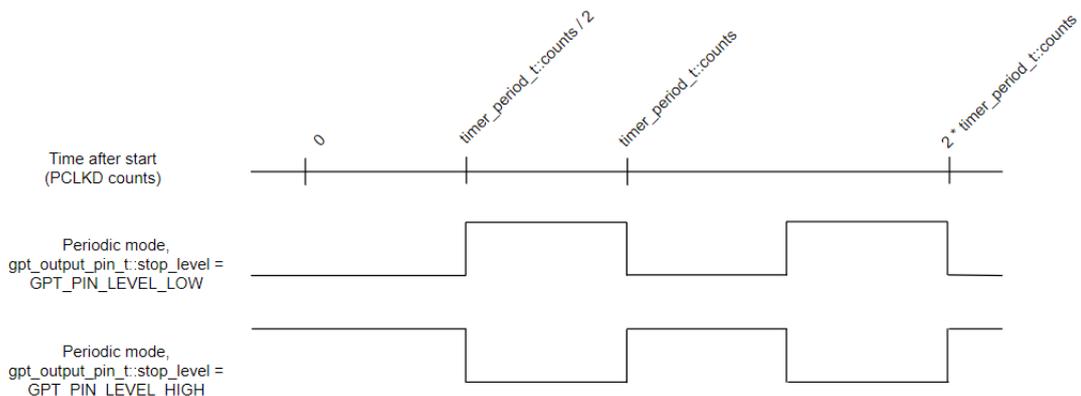


Figure 160: GPT Periodic Output

## PWM Output

The PWM output signal is high at the beginning of the cycle and low at the end of the cycle.

Examples of PWM signals that can be generated by this module are shown below:

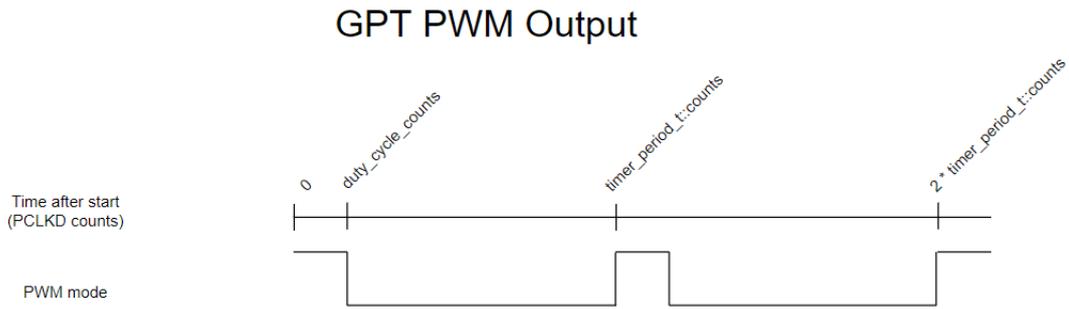


Figure 161: GPT PWM Output

### Triangle-Wave PWM Output

Examples of PWM signals that can be generated by this module are shown below. The `duty_cycle_counts` can be modified using `R_GPT_DutyCycleSet()` in the crest interrupt and updated at the following trough for symmetric PWM or modified in both the crest/trough interrupts and updated at the following trough/crest for asymmetric PWM.

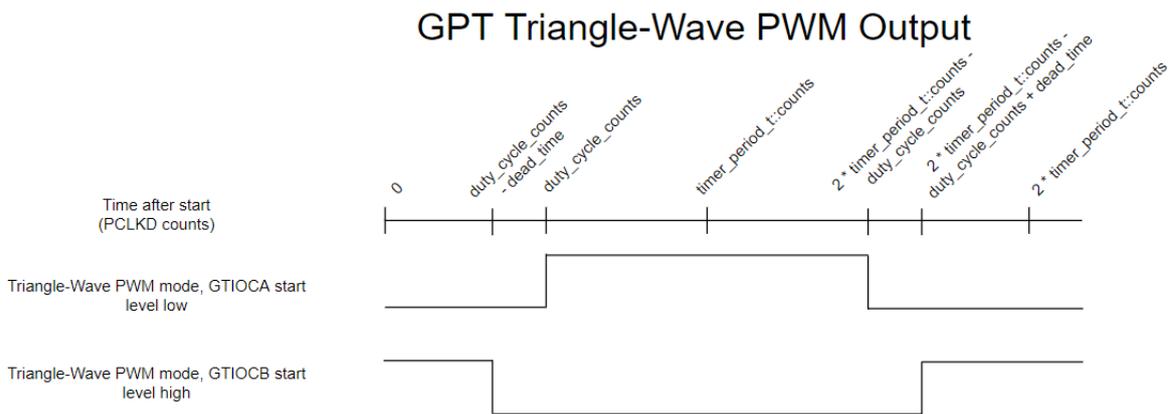


Figure 162: GPT Triangle-Wave PWM Output

### Event Counting

Event counting can be done by selecting up or down counting sources from GTETRG pins, ELC events, or GTIOC pins. In event counting mode, the GPT counter is not affected by PCLKD.

*Note*

*In event counting mode, the application must call `R_GPT_Start()` to enable event counting. The counter will not change after calling `R_GPT_Start()` until an event occurs.*

### Pulse Measurement

If the capture edge occurs before the start edge in pulse measurement, the first capture is invalid (0).

### Controlling GPT with GTETRG Edges

The GPT timer can be configured to stop, start, clear, count up, or count down when a GTETRG rising or falling edge occurs.

*Note*

The GTETRG pins are shared by all GPT channels.  
 GTETRG pins require POEG to be on (example code for this is provided in GPT Free Running Counter Example).  
 If input filtering is required on the GTETRG pins, that must also be handled outside this module.

## Controlling GPT with ELC Events

The GPT timer can be configured to stop, start, clear, count up, or count down when an ELC event occurs.

*Note*

The configurable ELC GPT sources are shared by all GPT channels.  
 The event links for the ELC must be configured outside this module.

## Triggering ELC Events with GPT

The GPT timer can trigger the start of other peripherals. The [Event Link Controller \(r\\_elc\)](#) guide provides a list of all available peripherals.

## Enabling External Sources for Start, Stop, Clear, or Capture

`R_GPT_Enable()` must be called when external sources are used for start, stop, clear, or capture.

## Interrupt Skipping

When an interrupt skipping source is selected a hardware counter will increment each time the selected event occurs. Each interrupt past the first (up to the specified skip count) will be suppressed. If ADC events are selected for skipping they will also be suppressed except during the timer period leading to the selected interrupt skipping event (see below diagram).

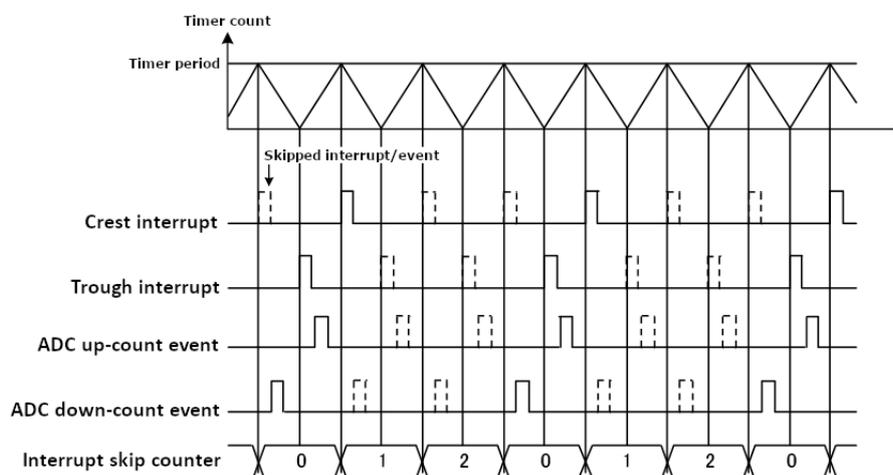


Figure 163: Crest interrupt skipping in triangle-wave PWM modes (skip count 2)

## Complementary Output

By using the Custom Waveform option the output pins can be made to output complementary waveforms. To ensure these waveforms stay in sync, the duty cycle for both pins can be set simultaneously by calling `R_GPT_DutyCycleSet` once with a pin parameter of `GPT_IO_PIN_GTIOCA_AND_GTIOCB`.

**Note**

The pin level for 0% and 100% duty cycle is determined by the Cycle End Output Level in normal PWM mode and the Initial Output Level in triangle PWM modes. 100% duty will output the configured level and 0% will output the opposite. Do not use Pin Level Toggle or Pin Level Retain for the Cycle End Output Level if normal PWM waveforms are desired.

## Examples

### GPT Basic Example

This is a basic example of minimal use of the GPT in an application.

```
void gpt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
}
```

### GPT Callback Example

This is an example of a timer callback.

```
/* Example callback called when timer expires. */
void timer_callback (timer_callback_args_t * p_args)
{
    if (TIMER_EVENT_CYCLE_END == p_args->event)
    {
        /* Add application code to be called periodically here. */
    }
}
```

### GPT Free Running Counter Example

To use the GPT as a free running counter, select periodic mode and set the the Period to 0xFFFFFFFF for a 32-bit timer or 0xFFFF for a 16-bit timer.

```
void gpt_counter_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* (Optional) If event count mode is used to count edges on a GTETRQ pin, POEG must
    be started to use GTETRQ.

    * Reference Note 1 of Table 23.2 "GPT functions" in the RA6M3 manual
    R01UH0886EJ0100. */

    R_BSP_MODULE_START(FSP_IP_POEG, 0U);

    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);

    /* (Optional) Stop the timer. */
    (void) R_GPT_Stop(&g_timer0_ctrl);

    /* Read the current counter value. Counter value is in status.counter. */
    timer_status_t status;

    (void) R_GPT_StatusGet(&g_timer0_ctrl, &status);
}
```

### GPT Input Capture Example

This is an example of using the GPT to capture pulse width or pulse period measurements.

```
/* Example callback called when a capture occurs. */
uint64_t g_captured_time = 0U;
uint32_t g_capture_overflows = 0U;
void timer_capture_callback (timer_callback_args_t * p_args)
{
    if ((TIMER_EVENT_CAPTURE_A == p_args->event) || (TIMER_EVENT_CAPTURE_B ==
p_args->event))
    {
```

```
/* (Optional) Get the current period if not known. */
timer_info_t info;
    (void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
    uint64_t period = info.period_counts;
/* The maximum period is one more than the maximum 32-bit number, but will be
reflected as 0 in
* timer_info_t::period_counts. */
if (0U == period)
    {
        period = UINT32_MAX + 1U;
    }
    g_captured_time    = (period * g_capture_overflows) + p_args->capture;
    g_capture_overflows = 0U;
}
if (TIMER_EVENT_CYCLE_END == p_args->event)
    {
/* An overflow occurred during capture. This must be accounted for at the
application layer. */
        g_capture_overflows++;
    }
}
void gpt_capture_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
/* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
/* Enable captures. Captured values arrive in the interrupt. */
    (void) R_GPT_Enable(&g_timer0_ctrl);
/* (Optional) Disable captures. */
    (void) R_GPT_Disable(&g_timer0_ctrl);
}
```

## GPT Period Update Example

This an example of updating the period.

```
#define GPT_EXAMPLE_MSEC_PER_SEC (1000)
#define GPT_EXAMPLE_DESIRED_PERIOD_MSEC (20)
/* This example shows how to calculate a new period value at runtime. */
void gpt_period_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
    /* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
    * - If the PCLKD frequency has not changed since reset, the source clock frequency
    is
    * BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
    * - Use the R_GPT_InfoGet function (it accounts for the divider).
    * - Calculate the current PCLKD frequency using
    R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) and right shift
    * by timer_cfg_t::source_div.
    *
    * This example uses the 3rd option (R_FSP_SystemClockHzGet).
    */
    uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
g_timer0_cfg.source_div;
    /* Calculate the desired period based on the current clock. Note that this
    calculation could overflow if the
    * desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
    used to prevent this. */
    uint32_t period_counts =
        (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
GPT_EXAMPLE_MSEC_PER_SEC);
```

```
/* Set the calculated period. */
err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
assert(FSP_SUCCESS == err);
}
```

## GPT Duty Cycle Update Example

This an example of updating the duty cycle.

```
#define GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT (25)
#define GPT_EXAMPLE_MAX_PERCENT (100)
/* This example shows how to calculate a new duty cycle value at runtime. */
void gpt_duty_cycle_calculation_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
    (void) R_GPT_Start(&g_timer0_ctrl);
    /* Get the current period setting. */
    timer_info_t info;
    (void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
    uint32_t current_period_counts = info.period_counts;
    /* Calculate the desired duty cycle based on the current period. Note that if the
period could be larger than
    * UINT32_MAX / 100, this calculation could overflow. A cast to uint64_t is used to
prevent this. The cast is
    * not required for 16-bit timers. */
    uint32_t duty_cycle_counts =
        (uint32_t) (((uint64_t) current_period_counts *
GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
                    GPT_EXAMPLE_MAX_PERCENT);
    /* Set the calculated duty cycle. */
```

```
err = R_GPT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, GPT_IO_PIN_GTIOCB);
assert(FSP_SUCCESS == err);
}
```

## GPT A/D Converter Start Request Example

This is an example of using the GPT to start the ADC at a configurable A/D converter compare match value.

```
#if ((1U << GPT_EXAMPLE_CHANNEL) & (BSP_FEATURE_GPTEH_CHANNEL_MASK |
BSP_FEATURE_GPTE_CHANNEL_MASK))
/* This example shows how to configure the GPT to generate an A/D start request at an
A/D start request compare
* match value. This example can only be used with GPTE or GPTEH variants. */
void gpt_adc_start_request_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize and configure the ELC. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Configure the ELC to start a scan on ADC unit 0 when GPT channel 0. Note: This is
typically configured in
* g_elc_cfg and already set during R_ELC_Open. */
    err = R_ELC_LinkSet(&g_elc_ctrl, ELC_PERIPHERAL_ADC0, ELC_EVENT_GPT0_AD_TRIG_A);
    assert(FSP_SUCCESS == err);
    /* Globally enable ELC events. */
    err = R_ELC_Enable(&g_elc_ctrl);
    assert(FSP_SUCCESS == err);
    /* Initialize the ADC to start a scan based on an ELC event trigger. Set
adc_cfg_t::trigger to
* ADC_TRIGGER_SYNC_ELC. */
    err = R_ADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
    assert(FSP_SUCCESS == err);
    err = R_ADC_ScanCfg(&g_adc0_ctrl, &g_adc0_channel_cfg);
}
```

```

    assert(FSP_SUCCESS == err);

    /* Enable ELC triggers by calling R_ADC_ScanStart(). */
    (void) R_ADC_ScanStart(&g_adc0_ctrl);

    /* Initializes the GPT module. Configure gpt_extended_pwm_cfg_t::adc_trigger to set
when the A/D start request
    * is generated. Set gpt_extended_pwm_cfg_t::adc_a_compare_match to set the desired
compare match value. */
    err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
    assert(FSP_SUCCESS == err);

    /* Start the timer. A/D converter start request events are generated each time the
counter is equal to the
    * A/D start request compare match value. */
    (void) R_GPT_Start(&g_timer0_ctrl);
}
#endif

```

## Data Structures

struct [gpt\\_output\\_pin\\_t](#)

struct [gpt\\_gtior\\_setting\\_t](#)

struct [gpt\\_instance\\_ctrl\\_t](#)

struct [gpt\\_extended\\_pwm\\_cfg\\_t](#)

struct [gpt\\_extended\\_cfg\\_t](#)

## Enumerations

enum [gpt\\_io\\_pin\\_t](#)

enum [gpt\\_pin\\_level\\_t](#)

enum [gpt\\_source\\_t](#)

enum [gpt\\_capture\\_filter\\_t](#)

enum [gpt\\_adc\\_trigger\\_t](#)

enum [gpt\\_poeg\\_link\\_t](#)

enum [gpt\\_output\\_disable\\_t](#)

enum [gpt\\_gtioc\\_disable\\_t](#)enum [gpt\\_adc\\_compare\\_match\\_t](#)enum [gpt\\_interrupt\\_skip\\_source\\_t](#)enum [gpt\\_interrupt\\_skip\\_count\\_t](#)enum [gpt\\_interrupt\\_skip\\_adc\\_t](#)

## Data Structure Documentation

### ◆ [gpt\\_output\\_pin\\_t](#)

struct <a href="#">gpt_output_pin_t</a>		
Configurations for output pins.		
Data Fields		
bool	output_enabled	Set to true to enable output, false to disable output.
<a href="#">gpt_pin_level_t</a>	stop_level	Select a stop level from <a href="#">gpt_pin_level_t</a> .

### ◆ [gpt\\_gtior\\_setting\\_t](#)

struct <a href="#">gpt_gtior_setting_t</a>		
Custom GTIOR settings used for configuring GTIOCxA and GTIOCxB pins.		

### ◆ [gpt\\_instance\\_ctrl\\_t](#)

struct <a href="#">gpt_instance_ctrl_t</a>		
Channel control block. DO NOT INITIALIZE. Initialization occurs when <a href="#">timer_api_t::open</a> is called.		

### ◆ [gpt\\_extended\\_pwm\\_cfg\\_t](#)

struct <a href="#">gpt_extended_pwm_cfg_t</a>		
GPT extension for advanced PWM features.		
Data Fields		
uint8_t	trough_ipr	Trough interrupt priority.
IRQn_Type	trough_irq	Trough interrupt.
<a href="#">gpt_poeg_link_t</a>	poeg_link	Select which POEG channel controls output disable for this GPT channel.
<a href="#">gpt_output_disable_t</a>	output_disable	Select which trigger sources request output disable from

		POEG.
<a href="#">gpt_adc_trigger_t</a>	adc_trigger	Select trigger sources to start A/D conversion.
uint32_t	dead_time_count_up	Set a dead time value for counting up.
uint32_t	dead_time_count_down	Set a dead time value for counting down (available on GPT32E and GPT32EH only)
uint32_t	adc_a_compare_match	Select the compare match value used to trigger an A/D conversion start request using ELC_EVENT_GPT<channel>_AD_TRIG_A.
uint32_t	adc_b_compare_match	Select the compare match value used to trigger an A/D conversion start request using ELC_EVENT_GPT<channel>_AD_TRIG_B.
<a href="#">gpt_interrupt_skip_source_t</a>	interrupt_skip_source	Interrupt source to count for interrupt skipping.
<a href="#">gpt_interrupt_skip_count_t</a>	interrupt_skip_count	Number of interrupts to skip between events.
<a href="#">gpt_interrupt_skip_adc_t</a>	interrupt_skip_adc	ADC events to skip when interrupt skipping is enabled.
<a href="#">gpt_gtioc_disable_t</a>	gtioca_disable_setting	DEPRECATED - Select how to configure GTIOCA when output is disabled.
<a href="#">gpt_gtioc_disable_t</a>	gtiocb_disable_setting	DEPRECATED - Select how to configure GTIOCB when output is disabled.

#### ◆ [gpt\\_extended\\_cfg\\_t](#)

struct <a href="#">gpt_extended_cfg_t</a>		
GPT extension configures the output pins for GPT.		
Data Fields		
<a href="#">gpt_output_pin_t</a>	gtioca	DEPRECATED - Configuration for GPT I/O pin A.
<a href="#">gpt_output_pin_t</a>	gtiocb	DEPRECATED - Configuration for GPT I/O pin B.
<a href="#">gpt_source_t</a>	start_source	Event sources that trigger the timer to start.
<a href="#">gpt_source_t</a>	stop_source	Event sources that trigger the timer to stop.

<a href="#">gpt_source_t</a>	clear_source	Event sources that trigger the timer to clear.
<a href="#">gpt_source_t</a>	capture_a_source	Event sources that trigger capture of GTIOCA.
<a href="#">gpt_source_t</a>	capture_b_source	Event sources that trigger capture of GTIOCB.
<a href="#">gpt_source_t</a>	count_up_source	Event sources that trigger a single up count. If GPT_SOURCE_NONE is selected for both count_up_source and count_down_source, then the timer count source is PCLK.
<a href="#">gpt_source_t</a>	count_down_source	Event sources that trigger a single down count. If GPT_SOURCE_NONE is selected for both count_up_source and count_down_source, then the timer count source is PCLK.
<a href="#">gpt_capture_filter_t</a>	capture_filter_gtioca	
<a href="#">gpt_capture_filter_t</a>	capture_filter_gtiocb	
uint8_t	capture_a_ipi	Capture A interrupt priority.
uint8_t	capture_b_ipi	Capture B interrupt priority.
IRQn_Type	capture_a_irq	Capture A interrupt.
IRQn_Type	capture_b_irq	Capture B interrupt.
<a href="#">gpt_extended_pwm_cfg_t</a> const *	p_pwm_cfg	Advanced PWM features, optional.
<a href="#">gpt_gtior_setting_t</a>	gtior_setting	Custom GTIOR settings used for configuring GTIOCxA and GTIOCxB pins.

## Enumeration Type Documentation

◆ **gpt\_io\_pin\_t**

enum <a href="#">gpt_io_pin_t</a>	
Input/Output pins, used to select which duty cycle to update in <a href="#">R_GPT_DutyCycleSet()</a> .	
Enumerator	
GPT_IO_PIN_GTIOCA	GTIOCA.
GPT_IO_PIN_GTIOCB	GTIOCB.
GPT_IO_PIN_GTIOCA_AND_GTIOCB	GTIOCA and GTIOCB.
GPT_IO_PIN_TROUGH	Used in <a href="#">R_GPT_DutyCycleSet</a> when Triangle-wave PWM Mode 3 is selected.
GPT_IO_PIN_CREST	Used in <a href="#">R_GPT_DutyCycleSet</a> when Triangle-wave PWM Mode 3 is selected.

◆ **gpt\_pin\_level\_t**

enum <a href="#">gpt_pin_level_t</a>	
Level of GPT pin	
Enumerator	
GPT_PIN_LEVEL_LOW	Pin level low.
GPT_PIN_LEVEL_HIGH	Pin level high.

◆ **gpt\_source\_t**

enum <a href="#">gpt_source_t</a>	
Sources can be used to start the timer, stop the timer, count up, or count down. These enumerations represent a bitmask. Multiple sources can be ORed together.	
Enumerator	
GPT_SOURCE_NONE	No active event sources.
GPT_SOURCE_GTETRGA_RISING	Action performed on GTETRGA rising edge.
GPT_SOURCE_GTETRGA_FALLING	Action performed on GTETRGA falling edge.
GPT_SOURCE_GTETRGB_RISING	Action performed on GTETRGB rising edge.
GPT_SOURCE_GTETRGB_FALLING	Action performed on GTETRGB falling edge.

GPT_SOURCE_GTETRGC_RISING	Action performed on GTETRGC rising edge.
GPT_SOURCE_GTETRGC_FALLING	Action performed on GTETRGC falling edge.
GPT_SOURCE_GTETRGD_RISING	Action performed on GTETRGB rising edge.
GPT_SOURCE_GTETRGD_FALLING	Action performed on GTETRGB falling edge.
GPT_SOURCE_GTIOCA_RISING_WHILE_GTIOCB_LOW	Action performed when GTIOCA input rises while GTIOCB is low.
GPT_SOURCE_GTIOCA_RISING_WHILE_GTIOCB_HIGH	Action performed when GTIOCA input rises while GTIOCB is high.
GPT_SOURCE_GTIOCA_FALLING_WHILE_GTIOCB_LOW	Action performed when GTIOCA input falls while GTIOCB is low.
GPT_SOURCE_GTIOCA_FALLING_WHILE_GTIOCB_HIGH	Action performed when GTIOCA input falls while GTIOCB is high.
GPT_SOURCE_GTIOCB_RISING_WHILE_GTIOCA_LOW	Action performed when GTIOCB input rises while GTIOCA is low.
GPT_SOURCE_GTIOCB_RISING_WHILE_GTIOCA_HIGH	Action performed when GTIOCB input rises while GTIOCA is high.
GPT_SOURCE_GTIOCB_FALLING_WHILE_GTIOCA_LOW	Action performed when GTIOCB input falls while GTIOCA is low.
GPT_SOURCE_GTIOCB_FALLING_WHILE_GTIOCA_HIGH	Action performed when GTIOCB input falls while GTIOCA is high.
GPT_SOURCE_GPT_A	Action performed on ELC GPTA event.
GPT_SOURCE_GPT_B	Action performed on ELC GPTB event.
GPT_SOURCE_GPT_C	Action performed on ELC GPTC event.
GPT_SOURCE_GPT_D	Action performed on ELC GPTD event.
GPT_SOURCE_GPT_E	Action performed on ELC GPTE event.
GPT_SOURCE_GPT_F	Action performed on ELC GPTF event.
GPT_SOURCE_GPT_G	Action performed on ELC GPTG event.
GPT_SOURCE_GPT_H	Action performed on ELC GPTH event.

◆ **gpt\_capture\_filter\_t**

enum <code>gpt_capture_filter_t</code>	
Input capture signal noise filter (debounce) setting. Only available for input signals GTIOCxA and GTIOCxB. The noise filter samples the external signal at intervals of the PCLK divided by one of the values. When 3 consecutive samples are at the same level (high or low), then that level is passed on as the observed state of the signal. See "Noise Filter Function" in the hardware manual, GPT section.	
Enumerator	
<code>GPT_CAPTURE_FILTER_NONE</code>	None - no filtering.
<code>GPT_CAPTURE_FILTER_PCLKD_DIV_1</code>	PCLK/1 - fast sampling.
<code>GPT_CAPTURE_FILTER_PCLKD_DIV_4</code>	PCLK/4.
<code>GPT_CAPTURE_FILTER_PCLKD_DIV_16</code>	PCLK/16.
<code>GPT_CAPTURE_FILTER_PCLKD_DIV_64</code>	PCLK/64 - slow sampling.

◆ **gpt\_adc\_trigger\_t**

enum <a href="#">gpt_adc_trigger_t</a>	
Trigger options to start A/D conversion.	
Enumerator	
GPT_ADC_TRIGGER_NONE	None - no output disable request.
GPT_ADC_TRIGGER_UP_COUNT_START_ADC_A	Request A/D conversion from ADC unit 0 at up counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_a_compare_match</a> .
GPT_ADC_TRIGGER_DOWN_COUNT_START_ADC_A	Request A/D conversion from ADC unit 0 at down counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_a_compare_match</a> .
GPT_ADC_TRIGGER_UP_COUNT_START_ADC_B	Request A/D conversion from ADC unit 1 at up counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_b_compare_match</a> .
GPT_ADC_TRIGGER_DOWN_COUNT_START_ADC_B	Request A/D conversion from ADC unit 1 at down counting compare match of <a href="#">gpt_extended_pwm_cfg_t::adc_b_compare_match</a> .

◆ **gpt\_poeg\_link\_t**

enum <a href="#">gpt_poeg_link_t</a>	
POEG channel to link to this channel.	
Enumerator	
GPT_POEG_LINK_POEG0	Link this GPT channel to POEG channel 0 (GTETRGA)
GPT_POEG_LINK_POEG1	Link this GPT channel to POEG channel 1 (GTETRGB)
GPT_POEG_LINK_POEG2	Link this GPT channel to POEG channel 2 (GTETRGC)
GPT_POEG_LINK_POEG3	Link this GPT channel to POEG channel 3 (GTETRGD)

◆ **gpt\_output\_disable\_t**

enum <code>gpt_output_disable_t</code>	
Select trigger to send output disable request to POEG.	
Enumerator	
<code>GPT_OUTPUT_DISABLE_NONE</code>	None - no output disable request.
<code>GPT_OUTPUT_DISABLE_DEAD_TIME_ERROR</code>	Request output disable if a dead time error occurs.
<code>GPT_OUTPUT_DISABLE_GTIOCA_GTIOCB_HIGH</code>	Request output disable if GTIOCA and GTIOCB are high at the same time.
<code>GPT_OUTPUT_DISABLE_GTIOCA_GTIOCB_LOW</code>	Request output disable if GTIOCA and GTIOCB are low at the same time.

◆ **gpt\_gtioc\_disable\_t**

enum <code>gpt_gtioc_disable_t</code>	
Disable level options for GTIOC pins.	
Enumerator	
<code>GPT_GTIOC_DISABLE_PROHIBITED</code>	Do not allow output disable.
<code>GPT_GTIOC_DISABLE_SET_HI_Z</code>	Set GTIOC to high impedance when output is disabled.
<code>GPT_GTIOC_DISABLE_LEVEL_LOW</code>	Set GTIOC level low when output is disabled.
<code>GPT_GTIOC_DISABLE_LEVEL_HIGH</code>	Set GTIOC level high when output is disabled.

◆ **gpt\_adc\_compare\_match\_t**

enum <code>gpt_adc_compare_match_t</code>	
Trigger options to start A/D conversion.	
Enumerator	
<code>GPT_ADC_COMPARE_MATCH_ADC_A</code>	Set A/D conversion start request value for GPT A/D converter start request A.
<code>GPT_ADC_COMPARE_MATCH_ADC_B</code>	Set A/D conversion start request value for GPT A/D converter start request B.

◆ **gpt\_interrupt\_skip\_source\_t**

enum <a href="#">gpt_interrupt_skip_source_t</a>	
Interrupt skipping modes	
Enumerator	
GPT_INTERRUPT_SKIP_SOURCE_NONE	Do not skip interrupts.
GPT_INTERRUPT_SKIP_SOURCE_OVERFLOW_UNDERFLOW	Count and skip overflow and underflow interrupts.
GPT_INTERRUPT_SKIP_SOURCE_CREST	Count crest interrupts for interrupt skipping. Skip the number of crest and trough interrupts configured in <a href="#">gpt_interrupt_skip_count_t</a> . When the interrupt does fire, the trough interrupt fires before the crest interrupt.
GPT_INTERRUPT_SKIP_SOURCE_TROUGH	Count trough interrupts for interrupt skipping. Skip the number of crest and trough interrupts configured in <a href="#">gpt_interrupt_skip_count_t</a> . When the interrupt does fire, the crest interrupt fires before the trough interrupt.

◆ **gpt\_interrupt\_skip\_count\_t**

enum <a href="#">gpt_interrupt_skip_count_t</a>	
Number of interrupts to skip between events	
Enumerator	
GPT_INTERRUPT_SKIP_COUNT_0	Do not skip interrupts.
GPT_INTERRUPT_SKIP_COUNT_1	Skip one interrupt.
GPT_INTERRUPT_SKIP_COUNT_2	Skip two interrupts.
GPT_INTERRUPT_SKIP_COUNT_3	Skip three interrupts.
GPT_INTERRUPT_SKIP_COUNT_4	Skip four interrupts.
GPT_INTERRUPT_SKIP_COUNT_5	Skip five interrupts.
GPT_INTERRUPT_SKIP_COUNT_6	Skip six interrupts.
GPT_INTERRUPT_SKIP_COUNT_7	Skip seven interrupts.

**◆ gpt\_interrupt\_skip\_adc\_t**

enum gpt_interrupt_skip_adc_t	
ADC events to skip during interrupt skipping	
Enumerator	
GPT_INTERRUPT_SKIP_ADC_NONE	Do not skip ADC events.
GPT_INTERRUPT_SKIP_ADC_A	Skip ADC A events.
GPT_INTERRUPT_SKIP_ADC_B	Skip ADC B events.
GPT_INTERRUPT_SKIP_ADC_A_AND_B	Skip ADC A and B events.

**Function Documentation**

◆ **R\_GPT\_Open()**

```
fsp_err_t R_GPT_Open ( timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg )
```

Initializes the timer module and applies configurations. Implements `timer_api_t::open`.

GPT hardware does not support one-shot functionality natively. When using one-shot mode, the timer will be stopped in an ISR after the requested period has elapsed.

The GPT implementation of the general timer can accept a `gpt_extended_cfg_t` extension parameter.

Example:

```
/* Initializes the module. */
err = R_GPT_Open(&g_timer0_ctrl, &g_timer0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and timer has started.
FSP_ERR_ASSERTION	A required input pointer is NULL or the source divider is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IRQ_BSP_DISABLED	<code>timer_cfg_t::mode</code> is <code>TIMER_MODE_ONE_SHOT</code> or <code>timer_cfg_t::p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use one-shot mode or callback.
FSP_ERR_INVALID_MODE	Triangle wave PWM is only supported if <code>GPT_CFG_OUTPUT_SUPPORT_ENABLE</code> is 2.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in the <code>p_cfg</code> parameter is not available on this device.

◆ **R\_GPT\_Stop()**

```
fsp_err_t R_GPT_Stop ( timer_ctrl_t *const p_ctrl)
```

Stops timer. Implements `timer_api_t::stop`.

Example:

```
/* (Optional) Stop the timer. */
(void) R_GPT_Stop(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer successfully stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Start()**

```
fsp_err_t R_GPT_Start ( timer_ctrl_t *const p_ctrl)
```

Starts timer. Implements `timer_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_GPT_Start(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	Timer successfully started.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Reset()**

```
fsp_err_t R_GPT_Reset ( timer_ctrl_t *const p_ctrl)
```

Resets the counter value to 0. Implements `timer_api_t::reset`.

**Note**

*This function also updates to the new period if no counter overflow has occurred since the last call to `R_GPT_PeriodSet()`.*

**Return values**

FSP_SUCCESS	Counter value written successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Enable()**

```
fsp_err_t R_GPT_Enable ( timer_ctrl_t *const p_ctrl)
```

Enables external event triggers that start, stop, clear, or capture the counter. Implements `timer_api_t::enable`.

Example:

```
/* Enable captures. Captured values arrive in the interrupt. */
(void) R_GPT_Enable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully enabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_Disable()**

```
fsp_err_t R_GPT_Disable ( timer_ctrl_t *const p_ctrl)
```

Disables external event triggers that start, stop, clear, or capture the counter. Implements `timer_api_t::disable`.

**Note**

*The timer could be running after `R_GPT_Disable()`. To ensure it is stopped, call `R_GPT_Stop()`.*

Example:

```
/* (Optional) Disable captures. */
(void) R_GPT_Disable(&g_timer0_ctrl);
```

**Return values**

FSP_SUCCESS	External events successfully disabled.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_PeriodSet()**

```
fsp_err_t R_GPT_PeriodSet ( timer_ctrl_t *const p_ctrl, uint32_t const period_counts )
```

Sets period value provided. If the timer is running, the period will be updated after the next counter overflow. If the timer is stopped, this function resets the counter and updates the period. Implements `timer_api_t::periodSet`.

**Warning**

If periodic output is used, the duty cycle buffer registers are updated after the period buffer register. If this function is called while the timer is running and a GPT overflow occurs during processing, the duty cycle will not be the desired 50% duty cycle until the counter overflow after processing completes.

Example:

```
/* Get the source clock frequency (in Hz). There are 3 ways to do this in FSP:
 * - If the PCLKD frequency has not changed since reset, the source clock frequency
is
 * BSP_STARTUP_PCLKD_HZ >> timer_cfg_t::source_div
 * - Use the R_GPT_InfoGet function (it accounts for the divider).
 * - Calculate the current PCLKD frequency using
R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) and right shift
 * by timer_cfg_t::source_div.
 *
```

```

* This example uses the 3rd option (R_FSP_SystemClockHzGet).
*/
uint32_t pclkd_freq_hz = R_FSP_SystemClockHzGet(FSP_PRIV_CLOCK_PCLKD) >>
g_timer0_cfg.source_div;
/* Calculate the desired period based on the current clock. Note that this
calculation could overflow if the
* desired period is larger than UINT32_MAX / pclkd_freq_hz. A cast to uint64_t is
used to prevent this. */
uint32_t period_counts =
    (uint32_t) (((uint64_t) pclkd_freq_hz * GPT_EXAMPLE_DESIRED_PERIOD_MSEC) /
GPT_EXAMPLE_MSEC_PER_SEC);
/* Set the calculated period. */
err = R_GPT_PeriodSet(&g_timer0_ctrl, period_counts);
assert(FSP_SUCCESS == err);

```

**Return values**

FSP_SUCCESS	Period value written successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

**◆ R\_GPT\_DutyCycleSet()**

```

fsp_err_t R_GPT_DutyCycleSet ( timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts,
uint32_t const pin )

```

Sets duty cycle on requested pin. Implements [timer\\_api\\_t::dutyCycleSet](#).

Duty cycle is updated in the buffer register. The updated duty cycle is reflected after the next cycle end (counter overflow).

**Example:**

```

/* Get the current period setting. */
timer_info_t info;
(void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
uint32_t current_period_counts = info.period_counts;
/* Calculate the desired duty cycle based on the current period. Note that if the
period could be larger than
* UINT32_MAX / 100, this calculation could overflow. A cast to uint64_t is used to

```

```

prevent this. The cast is
 * not required for 16-bit timers. */
uint32_t duty_cycle_counts =
    (uint32_t) (((uint64_t) current_period_counts *
GPT_EXAMPLE_DESIRED_DUTY_CYCLE_PERCENT) /
                GPT_EXAMPLE_MAX_PERCENT);
/* Set the calculated duty cycle. */
err = R_GPT_DutyCycleSet(&g_timer0_ctrl, duty_cycle_counts, GPT_IO_PIN_GTIOCB);
assert(FSP_SUCCESS == err);

```

### Parameters

[in]	p_ctrl	Pointer to instance control block.
[in]	duty_cycle_counts	Duty cycle to set in counts.
[in]	pin	Use gpt_io_pin_t to select GPT_IO_PIN_GTIOCA or GPT_IO_PIN_GTIOCB

### Return values

FSP_SUCCESS	Duty cycle updated successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL or the pin is not one of gpt_io_pin_t
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_INVALID_ARGUMENT	Duty cycle is larger than period.
FSP_ERR_INVALID_MODE	GPT_IO_PIN_TROUGH, and GPT_IO_PIN_CREST settings are invalid in the this mode.
FSP_ERR_UNSUPPORTED	GPT_CFG_OUTPUT_SUPPORT_ENABLE is 0.

## ◆ R\_GPT\_InfoGet()

```
fsp_err_t R_GPT_InfoGet ( timer_ctrl_t *const p_ctrl, timer_info_t *const p_info )
```

Get timer information and store it in provided pointer p\_info. Implements `timer_api_t::infoGet`.

Example:

```
/* (Optional) Get the current period if not known. */
timer_info_t info;
(void) R_GPT_InfoGet(&g_timer0_ctrl, &info);
uint64_t period = info.period_counts;

/* The maximum period is one more than the maximum 32-bit number, but will be
reflected as 0 in
* timer_info_t::period_counts. */
if (0U == period)
{
    period = UINT32_MAX + 1U;
}
```

**Return values**

FSP_SUCCESS	Period, count direction, frequency, and ELC event written to caller's structure successfully.
FSP_ERR_ASSERTION	p_ctrl or p_info was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_StatusGet()**

```
fsp_err_t R_GPT_StatusGet ( timer_ctrl_t *const p_ctrl, timer_status_t *const p_status )
```

Get current timer status and store it in provided pointer p\_status. Implements `timer_api_t::statusGet`.

Example:

```
/* Read the current counter value. Counter value is in status.counter. */
timer_status_t status;

(void) R_GPT_StatusGet(&g_timer0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current timer state and counter value set successfully.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_CounterSet()**

```
fsp_err_t R_GPT_CounterSet ( timer_ctrl_t *const p_ctrl, uint32_t counter )
```

Set counter value.

*Note*

*Do not call this API while the counter is counting. The counter value can only be updated while the counter is stopped.*

**Return values**

FSP_SUCCESS	Counter value updated.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_IN_USE	The timer is running. Stop the timer before calling this function.

## ◆ R\_GPT\_OutputEnable()

```
fsp_err_t R_GPT_OutputEnable ( timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin )
```

Enable output for GTIOCA and/or GTIOCB.

**Return values**

FSP_SUCCESS	Output is enabled.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

## ◆ R\_GPT\_OutputDisable()

```
fsp_err_t R_GPT_OutputDisable ( timer_ctrl_t *const p_ctrl, gpt_io_pin_t pin )
```

Disable output for GTIOCA and/or GTIOCB.

**Return values**

FSP_SUCCESS	Output is disabled.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

## ◆ R\_GPT\_AdcTriggerSet()

```
fsp_err_t R_GPT_AdcTriggerSet ( timer_ctrl_t *const p_ctrl, gpt_adc_compare_match_t  
which_compare_match, uint32_t compare_match_value )
```

Set A/D converter start request compare match value.

**Return values**

FSP_SUCCESS	Counter value updated.
FSP_ERR_ASSERTION	p_ctrl or p_status was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_CallbackSet()**

```
fsp_err_t R_GPT_CallbackSet ( timer_ctrl_t *const p_api_ctrl, void(*) (timer_callback_args_t *)
p_callback, void const *const p_context, timer_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `timer_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **R\_GPT\_Close()**

```
fsp_err_t R_GPT_Close ( timer_ctrl_t *const p_ctrl)
```

Stops counter, disables output pins, and clears internal driver data. Implements `timer_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

## 4.2.26 General PWM Timer Three-Phase Motor Control Driver (r\_gpt\_three\_phase)

Modules

**Functions**

```
fsp_err_t R_GPT_THREE_PHASE_Open (three_phase_ctrl_t *const p_ctrl,
three_phase_cfg_t const *const p_cfg)
```

```
fsp_err_t R_GPT_THREE_PHASE_Stop (three_phase_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_GPT_THREE_PHASE_Start (three_phase_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_GPT_THREE_PHASE_Reset (three_phase_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_GPT_THREE_PHASE_DutyCycleSet (three_phase_ctrl_t *const p_ctrl, three_phase_duty_cycle_t *const p_duty_cycle)
```

```
fsp_err_t R_GPT_THREE_PHASE_CallbackSet (three_phase_ctrl_t *const p_ctrl, void(*p_callback)(timer_callback_args_t*), void const *const p_context, timer_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_GPT_THREE_PHASE_Close (three_phase_ctrl_t *const p_ctrl)
```

## Detailed Description

Driver for 3-phase motor control using the GPT peripheral on RA MCUs. This module implements the [Three-Phase Interface](#).

## Overview

The General PWM Timer (GPT) Three-Phase driver provides basic functionality for synchronously starting and stopping three PWM channels for use in 3-phase motor control applications. A function is additionally provided to allow setting duty cycle values for all three channels, optionally with double-buffering.

## Features

The GPT Three-Phase driver provides the following functions:

- Synchronize configuration of three GPT channels
- Synchronously start, stop and reset all three GPT channels
- Set duty cycle on all three channels with one function

## Configuration

### Build Time Configurations for r\_gpt\_three\_phase

The following build time configurations are defined in fsp\_cfg/r\_gpt\_three\_phase\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Timers > Three-Phase PWM Driver on r\_gpt\_three\_phase

This module can be added to the Stacks tab via New Stack > Driver > Timers > Three-Phase PWM Driver on r\_gpt\_three\_phase. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_three_phase0	Module name.
General > Mode	<ul style="list-style-type: none"> <li>Triangle-Wave Symmetric PWM</li> <li>Triangle-Wave Asymmetric PWM</li> <li>Triangle-Wave Asymmetric PWM (Mode 3)</li> </ul>	Triangle-Wave Symmetric PWM	<p>Mode selection.</p> <p>Triangle-Wave Symmetric PWM: Generates symmetric PWM waveforms with duty cycle determined by compare match set during a crest interrupt and updated at the next trough.</p> <p>Triangle-Wave Asymmetric PWM: Generates asymmetric PWM waveforms with duty cycle determined by compare match set during a crest/trough interrupt and updated at the next trough/crest.</p>
General > Period	Value must be a non-negative integer less than or equal to 0x4000000000	15	<p>Specify the timer period in units selected below. Setting the period to 0x100000000 raw counts results in the maximum period. Set the period to 0x100000000 raw counts for a free running timer or an input capture configuration. The period can be set up to 0x4000000000, which will use a divider of 1024 with the maximum period.</p> <p>If the requested period cannot be achieved, the settings with the largest possible period that is less than or equal to the requested period are used. The theoretical calculated period is printed in a comment in the generated <a href="#">timer_cfg_t</a> structures for each</p>

timer.

General > Period Unit	<ul style="list-style-type: none"> <li>• Raw Counts</li> <li>• Nanoseconds</li> <li>• Microseconds</li> <li>• Milliseconds</li> <li>• Seconds</li> <li>• Hertz</li> <li>• Kilohertz</li> </ul>	Kilohertz	Unit of the period specified above
General > GPT U-Channel	Value must be an integer greater than or equal to 0	0	Specify the GPT channel for U signal output.
General > GPT V-Channel	Value must be an integer greater than or equal to 0	1	Specify the GPT channel for V signal output.
General > GPT W-Channel	Value must be an integer greater than or equal to 0	2	Specify the GPT channel for W signal output.
General > Callback Channel	<ul style="list-style-type: none"> <li>• U-Channel</li> <li>• V-Channel</li> <li>• W-Channel</li> </ul>	U-Channel	Specify the GPT channel to set a callback for when using R_GPT_THREE_PHASE_CallbackSet.
General > Buffer Mode	<ul style="list-style-type: none"> <li>• Single Buffer</li> <li>• Double Buffer</li> </ul>	Single Buffer	When Double Buffer is selected the 'duty_buffer' array in <a href="#">three_phase_duty_cycle_t</a> is used as a buffer for the 'duty' array. This allows setting the duty cycle for the next two crest/trough events in asymmetric mode with only one call to R_GPT_THREE_PHASE_DutyCycleSet.
General > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
General > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level Low	Select the behavior of the output pin when the timer is stopped.
Extra Features > Dead Time > Dead Time Count Up (Raw Counts)	Must be a valid non-negative integer with a maximum configurable value of 4294967295 (0xffffffff).	0	Select the dead time to apply during up counting. This value also applies during down counting for the GPT32 and GPT16 variants.
Extra Features > Dead	Must be a valid non-	0	Select the dead time to

Time > Dead Time Count Down (Raw Counts) (GPTE/GPTEH only)	negative integer with a maximum configurable value of 4294967295 (0xffffffff).	apply during down counting. This value only applies to the GPT32E and GPT32EH variants.
--	--	---

## Clock Configuration

Please refer to the [General PWM Timer \(r\\_gpt\)](#) section for more information.

## Pin Configuration

Please refer to the [General PWM Timer \(r\\_gpt\)](#) section for more information.

## Usage Notes

### Warning

Be sure the GTIOCA/B stop level and dead time values are set appropriately for your application before attempting to drive a motor. Failure to do so may result in damage to the motor drive circuitry and/or the motor itself if the timer is stopped by software.

## Initial Setup

The following should be configured once the GPT Three-Phase module has been added to a project:

1. Set "Pin Output Support" in one of the GPT submodules to "Enabled with Extra Features"
2. Configure common settings in the GPT Three-Phase module properties
3. Set the crest and trough interrupt priority and callback function in **one** of the three GPT submodules (if desired)
4. Set the "Extra Features -> Output Disable" settings in each GPT submodule as needed for your application

### Note

*Because all three modules are operated synchronously with the same period interrupts only need to be enabled in one of the three GPT modules.*

## Buffer Modes

There are two buffering modes available for duty cycle values - single- and double-buffered. In single buffer mode only the values specified in the duty array element of [three\\_phase\\_duty\\_cycle\\_t](#) are used by [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet](#). At the next trough or crest event the output duty cycle will be internally updated to the set values.

In double buffer mode the [duty\\_buffer](#) array values are used as buffer values for the duty elements. Once passed to [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet](#), the next trough or crest event will update the output duty cycle to the values specified in duty as before. However, at the following crest or trough event the output duty cycle will be updated to the values in [duty\\_buffer](#). This allows the duty cycle for both sides of an asymmetric PWM waveform to be set at only one trough or crest event per period instead of at every event.

## Examples

### GPT Three-Phase Basic Example

This is a basic example of minimal use of the GPT Three-Phase module in an application. The duty cycle is updated at every timer trough with the previously loaded buffer value, then the duty cycle buffer is reloaded in the trough interrupt callback.

```
void gpt_callback (timer_callback_args_t * p_args)
{
    fsp_err_t err;
    three_phase_duty_cycle_t duty_cycle;
    if (TIMER_EVENT_TROUGH == p_args->event)
    {
        /* Update duty cycle values (example) */
        duty_cycle.duty[THREE_PHASE_CHANNEL_U] =
get_duty_counts(THREE_PHASE_CHANNEL_U);
        duty_cycle.duty[THREE_PHASE_CHANNEL_V] =
get_duty_counts(THREE_PHASE_CHANNEL_V);
        duty_cycle.duty[THREE_PHASE_CHANNEL_W] =
get_duty_counts(THREE_PHASE_CHANNEL_W);
        /* Update duty cycle values */
        err = R_GPT_THREE_PHASE_DutyCycleSet(&g_gpt_three_phase_ctrl, &duty_cycle);
        assert(FSP_SUCCESS == err);
    }
    else
    {
        /* Handle crest event. */
    }
}

void gpt_three_phase_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = R_GPT_THREE_PHASE_Open(&g_gpt_three_phase_ctrl, &g_gpt_three_phase_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the timer. */
    (void) R_GPT_THREE_PHASE_Start(&g_gpt_three_phase_ctrl);
}
```

## Data Structures

```
struct gpt_three_phase_instance_ctrl_t
```

## Data Structure Documentation

### ◆ gpt\_three\_phase\_instance\_ctrl\_t

```
struct gpt_three_phase_instance_ctrl_t
```

Channel control block. DO NOT INITIALIZE. Initialization occurs when `three_phase_api_t::open` is called.

## Function Documentation

### ◆ R\_GPT\_THREE\_PHASE\_Open()

```
fsp_err_t R_GPT_THREE_PHASE_Open ( three_phase_ctrl_t *const p_ctrl, three_phase_cfg_t const *const p_cfg )
```

Initializes the 3-phase timer module (and associated timers) and applies configurations. Implements `three_phase_api_t::open`.

Example:

```
/* Initializes the module. */
err = R_GPT_THREE_PHASE_Open(&g_gpt_three_phase_ctrl, &g_gpt_three_phase_cfg);
```

### Return values

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	A required input pointer is NULL.
FSP_ERR_ALREADY_OPEN	Module is already open.

### ◆ R\_GPT\_THREE\_PHASE\_Stop()

```
fsp_err_t R_GPT_THREE_PHASE_Stop ( three_phase_ctrl_t *const p_ctrl)
```

Stops all timers synchronously. Implements `three_phase_api_t::stop`.

### Return values

FSP_SUCCESS	Timers successfully stopped.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_THREE\_PHASE\_Start()**

```
fsp_err_t R_GPT_THREE_PHASE_Start ( three_phase_ctrl_t *const p_ctrl)
```

Starts all timers synchronously. Implements `three_phase_api_t::start`.

Example:

```
/* Start the timer. */
(void) R_GPT_THREE_PHASE_Start(&g_gpt_three_phase_ctrl);
```

**Return values**

FSP_SUCCESS	Timers successfully started.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_GPT\_THREE\_PHASE\_Reset()**

```
fsp_err_t R_GPT_THREE_PHASE_Reset ( three_phase_ctrl_t *const p_ctrl)
```

Resets the counter values to 0. Implements `three_phase_api_t::reset`.

**Return values**

FSP_SUCCESS	Counters were reset successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

### ◆ R\_GPT\_THREE\_PHASE\_DutyCycleSet()

```
fsp_err_t R_GPT_THREE_PHASE_DutyCycleSet ( three_phase_ctrl_t *const p_ctrl,
three_phase_duty_cycle_t *const p_duty_cycle )
```

Sets duty cycle for all three timers. Implements `three_phase_api_t::dutyCycleSet`.

In symmetric PWM mode duty cycle values are reflected after the next trough. In asymmetric PWM mode values are reflected at the next trough OR crest, whichever comes first.

When double-buffering is enabled the values in `three_phase_duty_cycle_t::duty_buffer` are set to the double-buffer registers. When values are reflected the first time the single buffer values (`three_phase_duty_cycle_t::duty`) are used. On the second reflection the `duty_buffer` values are used. In asymmetric PWM mode this enables both count-up and count-down PWM values to be set at trough (or crest) exclusively.

#### Note

*It is recommended to call this function in a high-priority callback to ensure that it is not interrupted and that no GPT events occur during setting that would result in a duty cycle buffer load operation.*

#### Example:

```
/* Update duty cycle values */
err = R_GPT_THREE_PHASE_DutyCycleSet(&g_gpt_three_phase_ctrl, &duty_cycle);
assert(FSP_SUCCESS == err);
```

#### Return values

FSP_SUCCESS	Duty cycle updated successfully.
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The instance is not opened.
FSP_ERR_INVALID_ARGUMENT	One or more duty cycle count values was outside the range 0..(period - 1).

### ◆ R\_GPT\_THREE\_PHASE\_CallbackSet()

```
fsp_err_t R_GPT_THREE_PHASE_CallbackSet ( three_phase_ctrl_t *const p_ctrl,
void(*) (timer_callback_args_t *) p_callback, void const *const p_context, timer_callback_args_t
*const p_callback_memory )
```

Updates the user callback for the GPT U-channel with the option to provide memory for the callback argument structure. Implements `three_phase_api_t::callbackSet`.

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

### ◆ R\_GPT\_THREE\_PHASE\_Close()

```
fsp_err_t R_GPT_THREE_PHASE_Close ( three_phase_ctrl_t *const p_ctrl)
```

Stops counters, disables output pins, and clears internal driver data. Implements [three\\_phase\\_api\\_t::close](#).

#### Return values

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

## 4.2.27 Interrupt Controller Unit (r\_icu)

### Modules

#### Functions

```
fsp_err_t R_ICU_ExternalIrqOpen (external_irq_ctrl_t *const p_api_ctrl,
external_irq_cfg_t const *const p_cfg)
```

```
fsp_err_t R_ICU_ExternalIrqEnable (external_irq_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_ICU_ExternalIrqDisable (external_irq_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_ICU_ExternalIrqCallbackSet (external_irq_ctrl_t *const p_api_ctrl,
void(*p_callback)(external_irq_callback_args_t *), void const *const
p_context, external_irq_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_ICU_ExternalIrqClose (external_irq_ctrl_t *const p_api_ctrl)
```

#### Detailed Description

Driver for the ICU peripheral on RA MCUs. This module implements the [External IRQ Interface](#).

## Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC, DTC, and DMAC modules. The R\_ICU software module only implements the [External IRQ Interface](#). The external\_irq interface is for configuring interrupts to fire when a trigger condition is detected on an external IRQ pin.

#### Note

*Multiple instances are used when more than one external interrupt is needed. Configure each instance with different channels and properties as needed for the specific interrupt.*

## Features

- Supports configuring interrupts for IRQ pins on the target MCUs
  - Enabling and disabling interrupt generation.
  - Configuring interrupt trigger on rising edge, falling edge, both edges, or low level signal.
  - Enabling and disabling the IRQ noise filter.
- Supports configuring a user callback function, which will be invoked by the HAL module when an external pin interrupt is generated.

## Configuration

### Build Time Configurations for r\_icu

The following build time configurations are defined in fsp\_cfg/r\_icu\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Input > External IRQ Driver on r\_icu

This module can be added to the Stacks tab via New Stack > Driver > Input > External IRQ Driver on r\_icu. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_external_irq0	Module name.
Channel	Value must be an integer between 0 and 15	0	Specify the hardware channel.
Trigger	<ul style="list-style-type: none"> <li>• Falling</li> <li>• Rising</li> <li>• Both Edges</li> <li>• Low Level</li> </ul>	Rising	Select the signal edge or state that triggers an interrupt.
Digital Filtering	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Select if the digital noise filter should be enabled.
Digital Filtering Sample Clock (Only valid when Digital Filtering is Enabled)	<ul style="list-style-type: none"> <li>• PCLK / 1</li> <li>• PCLK / 8</li> <li>• PCLK / 32</li> <li>• PCLK / 64</li> </ul>	PCLK / 64	Select the clock divider for the digital noise filter.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided here. If this

callback function is provided, it is called from the interrupt service routine (ISR) each time the IRQn triggers

Select the PIN interrupt priority.

Pin Interrupt Priority      MCU Specific Options

## Clock Configuration

The ICU peripheral module doesn't require any specific clock settings.

*Note*

*The digital filter uses PCLKB as the clock source for sampling the IRQ pin.*

## Pin Configuration

The pin for the external interrupt channel must be configured as an input with IRQ Input Enabled.

# Usage Notes

## Digital Filter

The digital filter is used to reject trigger conditions that are too short. The trigger condition must be longer than three periods of the filter clock. The filter clock frequency is determined by PCLKB and the external\_irq\_pclk\_div\_t setting.

$$\text{MIN\_PULSE\_WIDTH} = \text{EXTERNAL\_IRQ\_PCLKB\_DIV} / \text{PCLKB\_FREQUENCY} * 3$$

## DMAC/DTC

When using an External IRQ pin to trigger a DMAC/DTC transfer, the External IRQ pin must be opened before the transfer instance is opened.

# Examples

## Basic Example

This is a basic example of minimal use of the ICU in an application.

```
#define ICU_IRQN_PIN BSP_IO_PORT_02_PIN_06
#define ICU_IRQN 6
/* Called from icu_irq_isr */
void external_irq_callback (external_irq_callback_args_t * p_args)
{
    (void) p_args;
    g_external_irq_complete = 1;
}
```

```

void simple_example ()
{
    /* Example Configuration */
    external_irq_cfg_t icu_cfg =
    {
        .channel      = ICU_IRQN,
        .trigger      = EXTERNAL_IRQ_TRIG_RISING,
        .filter_enable = false,
        .pclk_div     = EXTERNAL_IRQ_PCLK_DIV_BY_1,
        .p_callback   = external_irq_callback,
        .p_context    = 0,
        .ipl          = 0,
        .irq          = (IRQn_Type) 0,
    };

    /* Configure the external interrupt. */
    fsp_err_t err = R_ICU_ExternalIrqOpen(&g_icu_ctrl, &icu_cfg);
    assert(FSP_SUCCESS == err);

    /* Enable the external interrupt. */
    /* Enable not required when used with ELC or DMAC. */
    err = R_ICU_ExternalIrqEnable(&g_icu_ctrl);
    assert(FSP_SUCCESS == err);

    while (0 == g_external_irq_complete)
    {
        /* Wait for interrupt. */
    }
}

```

## Data Structures

struct [icu\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ icu\_instance\_ctrl\_t

struct [icu\\_instance\\_ctrl\\_t](#)

ICU private control block. DO NOT MODIFY. Initialization occurs when R\_ICU\_ExternalIrqOpen is called.

Data Fields	
uint32_t	<a href="#">open</a>
	Used to determine if channel control block is in use.
IRQn_Type	<a href="#">irq</a>
	NVIC interrupt number.
uint8_t	<a href="#">channel</a>
	Channel.
void const *	<a href="#">p_context</a>
<b>Field Documentation</b>	
◆ <b>p_context</b>	
void const* icu_instance_ctrl_t::p_context	
Placeholder for user data. Passed to the user callback in <a href="#">external_irq_callback_args_t</a> .	

## Function Documentation

---

◆ **R\_ICU\_ExternalIrqOpen()**

```
fsp_err_t R_ICU_ExternalIrqOpen ( external_irq_ctrl_t *const p_api_ctrl, external_irq_cfg_t const *const p_cfg )
```

Configure an IRQ input pin for use with the external interrupt interface. Implements [external\\_irq\\_api\\_t::open](#).

The Open function is responsible for preparing an external IRQ pin for operation.

**Return values**

FSP_SUCCESS	Open successful.
FSP_ERR_ASSERTION	One of the following is invalid: <ul style="list-style-type: none"> <li>• p_ctrl or p_cfg is NULL</li> </ul>
FSP_ERR_ALREADY_OPEN	The channel specified has already been opened. No configurations were changed. Call the associated Close function to reconfigure the channel.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in p_cfg is not available on the device selected in r_bsp_cfg.h.
FSP_ERR_INVALID_ARGUMENT	p_cfg->p_callback is not NULL, but ISR is not enabled. ISR must be enabled to use callback function.

**Note**

*This function is reentrant for different channels. It is not reentrant for the same channel.*

◆ **R\_ICU\_ExternalIrqEnable()**

```
fsp_err_t R_ICU_ExternalIrqEnable ( external_irq_ctrl_t *const p_api_ctrl)
```

Enable external interrupt for specified channel at NVIC. Implements [external\\_irq\\_api\\_t::enable](#).

**Return values**

FSP_SUCCESS	Interrupt Enabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_IRQ_BSP_DISABLED	Requested IRQ is not defined in this system

◆ **R\_ICU\_ExternalIrqDisable()**

```
fsp_err_t R_ICU_ExternalIrqDisable ( external_irq_ctrl_t *const p_api_ctrl)
```

Disable external interrupt for specified channel at NVIC. Implements `external_irq_api_t::disable`.

**Return values**

FSP_SUCCESS	Interrupt disabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_IRQ_BSP_DISABLED	Requested IRQ is not defined in this system

◆ **R\_ICU\_ExternalIrqCallbackSet()**

```
fsp_err_t R_ICU_ExternalIrqCallbackSet ( external_irq_ctrl_t *const p_api_ctrl,
void(*) (external_irq_callback_args_t *) p_callback, void const *const p_context,
external_irq_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `external_irq_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **R\_ICU\_ExternalIrqClose()**

```
fsp_err_t R_ICU_ExternalIrqClose ( external_irq_ctrl_t *const p_api_ctrl)
```

Close the external interrupt channel. Implements `external_irq_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The channel is not opened.

## 4.2.28 I2C Master on IIC (r\_licu\_master)

### Modules

#### Functions

`fsp_err_t R_IIC_MASTER_Open (i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg)`

`fsp_err_t R_IIC_MASTER_Read (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)`

`fsp_err_t R_IIC_MASTER_Write (i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart)`

`fsp_err_t R_IIC_MASTER_Abort (i2c_master_ctrl_t *const p_api_ctrl)`

`fsp_err_t R_IIC_MASTER_SlaveAddressSet (i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode)`

`fsp_err_t R_IIC_MASTER_Close (i2c_master_ctrl_t *const p_api_ctrl)`

`fsp_err_t R_IIC_MASTER_CallbackSet (i2c_master_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_master_callback_args_t *), void const *const p_context, i2c_master_callback_args_t *const p_callback_memory)`

`fsp_err_t R_IIC_MASTER_StatusGet (i2c_master_ctrl_t *const p_api_ctrl, i2c_master_status_t *p_status)`

#### Detailed Description

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

## Overview

The I2C master on IIC HAL module supports transactions with an I2C Slave device. Callbacks must be provided which are invoked when a transmit or receive operation has completed. The callback argument will contain information about the transaction status, bytes transferred and a pointer to the user defined context.

#### Features

- Supports multiple transmission rates
  - Standard Mode Support with up to 100-kHz transaction rate.
  - Fast Mode Support with up to 400-kHz transaction rate.
  - Fast Mode Plus Support with up to 1-MHz transaction rate.
- I2C Master Read from a slave device.
- I2C Master Write to a slave device.

- Abort any in-progress transactions.
- Set the address of the slave device.
- Non-blocking behavior is achieved by the use of callbacks.
- Additional build-time features
  - Optional (build time) DTC support for read and write respectively.
  - Optional (build time) support for 10-bit slave addressing.

## Configuration

### Build Time Configurations for r\_iic\_master

The following build time configurations are defined in fsp\_cfg/r\_iic\_master\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC on Transmission and Reception	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, DTC instances will be included in the build for both transmission and reception.
10-bit slave addressing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, the driver will support 10-bit slave addressing mode along with the default 7-bit slave addressing mode.

### Configurations for Driver > Connectivity > I2C Master Driver on r\_iic\_master

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Master Driver on r\_iic\_master. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2c_master0	Module name.
Channel	Value must be a non-negative integer	0	Specify the IIC channel.
Rate	<ul style="list-style-type: none"> <li>• Standard</li> <li>• Fast-mode</li> <li>• Fast-mode plus</li> </ul>	Standard	Select the transfer rate.  If the requested transfer rate cannot be achieved, the settings with the largest possible transfer rate that is less than or equal to the requested

transfer rate are used. The theoretical calculated transfer rate and duty cycle are printed in a comment in the generated `iic_master_extended_cfg_t` structure.

Rise Time (ns)	Value must be a non-negative integer	120	Set the rise time (tr) in nanoseconds.
Fall Time (ns)	Value must be a non-negative integer	120	Set the fall time (tf) in nanoseconds.
Duty Cycle (%)	Value must be an integer between 0 and 100	50	Set the SCL duty cycle.
Slave Address	Value must be non-negative	0x00	Specify the slave address.
Address Mode	<ul style="list-style-type: none"> <li>7-Bit</li> <li>10-Bit</li> </ul>	7-Bit	Select the slave address mode. Ensure 10-bit slave addressing is enabled in the configuration to use 10-Bit setting here.
Timeout Mode	<ul style="list-style-type: none"> <li>Short Mode</li> <li>Long Mode</li> </ul>	Short Mode	Select the timeout mode to detect bus hang.
Timeout during SCL Low	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	Select if the timeout can occur when SCL is held low for a duration longer than what is set in the timeout mode.
Callback	Name must be a valid C symbol	NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) upon IIC transaction completion reporting the transaction status.
Interrupt Priority Level	MCU Specific Options		Select the interrupt priority level. This is set for TXI, RXI, TEI and ERI interrupts.

## Clock Configuration

The IIC peripheral module uses the PCLKB as its clock source. The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate. If the PCLKB is configured

in such a manner that the selected internal rate cannot be achieved, an error will be returned.

## Pin Configuration

The IIC peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two pins - SDA and SCL for data/address and clock respectively.

## Usage Notes

### Interrupt Configuration

- The IIC error (EEI), receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel used must be enabled in the properties of the selected device.
- Set equal priority levels for all the interrupts mentioned above. Setting the interrupts to different priority levels could result in improper operation.

### IIC Master Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLKB settings is calculated and used.
- If a valid clock rate could not be calculated, an error is returned by the tool.

### Enabling DTC with the IIC

- DTC transfer support is configurable and is disabled from the build by default. IIC driver provides two DTC instances for transmission and reception respectively. The DTC instances can be enabled individually during configuration.
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

### Multiple Devices on the Bus

- A single IIC instance can be used to communicate with multiple slave devices on the same channel by using the SlaveAddressSet API.

### Multi-Master Support

- If multiple masters are connected on the same bus, the I2C Master is capable of detecting bus busy state before initiating the communication.

### Restart

- IIC master can hold the the bus after an I2C transaction by issuing Restart. This will mimic a stop followed by start condition.

## Examples

### Basic Example

This is a basic example of minimal use of the r\_iic\_master in an application. This example shows how this driver can be used for basic read and write operations.

```
iic_master_instance_ctrl_t g_i2c_device_ctrl_1;
i2c_master_cfg_t g_i2c_device_cfg_1 =
{
    .channel      = I2C_CHANNEL,
    .rate        = I2C_MASTER_RATE_FAST,
    .slave       = I2C_SLAVE_EEPROM,
    .addr_mode   = I2C_MASTER_ADDR_MODE_7BIT,
    .p_callback  = i2c_callback,    // Callback
    .p_context   = &g_i2c_device_ctrl_1,
    .p_transfer_tx = NULL,
    .p_transfer_rx = NULL,
    .p_extend    = &g_iic_master_cfg_extend
};

void i2c_callback (i2c_master_callback_args_t * p_args)
{
    g_i2c_callback_event = p_args->event;
}

void basic_example (void)
{
    fsp_err_t err;
    uint32_t i;
    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
    /* Initialize the IIC module */
    err = R_IIC_MASTER_Open(&g_i2c_device_ctrl_1, &g_i2c_device_cfg_1);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Write some data to the transmit buffer */
    for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)
    {
        g_i2c_tx_buffer[i] = (uint8_t) i;
    }
    /* Send data to I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    err = R_IIC_MASTER_Write(&g_i2c_device_ctrl_1, &g_i2c_tx_buffer[0],
```

```
I2C_BUFFER_SIZE_BYTES, false);
    assert(FSP_SUCCESS == err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }
    /* Read data back from the I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    timeout_ms          = I2C_TRANSACTION_BUSY_DELAY;
    err = R_IIC_MASTER_Read(&g_i2c_device_ctrl_1, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    assert(FSP_SUCCESS == err);
    /* Since there is nothing else to do, block until Callback triggers*/
    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
    if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }
    /* Verify the read data */
    if (0U != memcmp(g_i2c_tx_buffer, g_i2c_rx_buffer, I2C_BUFFER_SIZE_BYTES))
    {
        __BKPT(0);
    }
}
```

## Multiple Slave devices on the same channel (bus)

This example demonstrates how a single IIC driver can be used to communicate with different slave devices which are on the same channel.

### Note

*The callback function from the first example applies to this example as well.*

```
iic_master_instance_ctrl_t g_i2c_device_ctrl_2;
i2c_master_cfg_t g_i2c_device_cfg_2 =
{
    .channel          = I2C_CHANNEL,
    .rate             = I2C_MASTER_RATE_STANDARD,
    .slave            = I2C_SLAVE_TEMP_SENSOR,
    .addr_mode        = I2C_MASTER_ADDR_MODE_7BIT,
    .p_callback       = i2c_callback,    // Callback
    .p_context        = &g_i2c_device_ctrl_2,
    .p_transfer_tx    = NULL,
    .p_transfer_rx    = NULL,
    .p_extend         = &g_iic_master_cfg_extend
};

void single_channel_multi_slave (void)
{
    fsp_err_t err;

    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

    err = R_IIC_MASTER_Open(&g_i2c_device_ctrl_2, &g_i2c_device_cfg_2);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Clear the receive buffer */
    memset(g_i2c_rx_buffer, '0', I2C_BUFFER_SIZE_BYTES);

    /* Read data from I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;

    err = R_IIC_MASTER_Read(&g_i2c_device_ctrl_2, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    assert(FSP_SUCCESS == err);

    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
```

```

    {
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }
/* Send data to I2C slave on the same channel */
err = R_IIC_MASTER_SlaveAddressSet(&g_i2c_device_ctrl_2,
I2C_SLAVE_DISPLAY_ADAPTER, I2C_MASTER_ADDR_MODE_7BIT);
assert(FSP_SUCCESS == err);
g_i2c_tx_buffer[0] = 0xAA; // NOLINT
g_i2c_tx_buffer[1] = 0xBB; // NOLINT
g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
err = R_IIC_MASTER_Write(&g_i2c_device_ctrl_2, &g_i2c_tx_buffer[0], 2U, false);
assert(FSP_SUCCESS == err);
while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
    {
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
        timeout_ms--;
    }
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
    {
        __BKPT(0);
    }
}

```

## Data Structures

struct iic\_master\_clock\_settings\_t

struct iic\_master\_instance\_ctrl\_t

struct iic\_master\_extended\_cfg\_t

## Enumerations

```
enum iic_master_timeout_mode_t
```

```
enum iic_master_timeout_scl_low_t
```

## Data Structure Documentation

### ◆ iic\_master\_clock\_settings\_t

struct iic_master_clock_settings_t		
I2C clock settings		
Data Fields		
uint8_t	cks_value	Internal Reference Clock Select.
uint8_t	brh_value	High-level period of SCL clock.
uint8_t	brl_value	Low-level period of SCL clock.

### ◆ iic\_master\_instance\_ctrl\_t

struct iic_master_instance_ctrl_t		
I2C control structure. DO NOT INITIALIZE.		

### ◆ iic\_master\_extended\_cfg\_t

struct iic_master_extended_cfg_t		
R_IIC extended configuration		
Data Fields		
<a href="#">iic_master_timeout_mode_t</a>	timeout_mode	Timeout Detection Time Select: Long Mode = 0 and Short Mode = 1.
<a href="#">iic_master_timeout_scl_low_t</a>	timeout_scl_low	Allows timeouts to occur when SCL is held low.
<a href="#">iic_master_clock_settings_t</a>	clock_settings	I2C Clock settings.

## Enumeration Type Documentation

◆ **iic\_master\_timeout\_mode\_t**

enum iic_master_timeout_mode_t	
I2C Timeout mode parameter definition	
Enumerator	
IIC_MASTER_TIMEOUT_MODE_LONG	Timeout Detection Time Select: Long Mode -> TMOS = 0.
IIC_MASTER_TIMEOUT_MODE_SHORT	Timeout Detection Time Select: Short Mode -> TMOS = 1.

◆ **iic\_master\_timeout\_scl\_low\_t**

enum iic_master_timeout_scl_low_t	
Enumerator	
IIC_MASTER_TIMEOUT_SCL_LOW_DISABLED	Timeout detection during SCL low disabled.
IIC_MASTER_TIMEOUT_SCL_LOW_ENABLED	Timeout detection during SCL low enabled.

**Function Documentation**◆ **R\_IIC\_MASTER\_Open()**

fsp_err_t R_IIC_MASTER_Open ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg )	
Opens the I2C device.	
<b>Return values</b>	
FSP_SUCCESS	Requested clock rate was set exactly.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel is not available on this MCU.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ol style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Set the rate to fast mode plus on a channel which does not support it.</li> <li>5. Invalid IRQ number assigned</li> </ol>

◆ **R\_IIC\_MASTER\_Read()**

```
fsp_err_t R_IIC_MASTER_Read ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t
const bytes, bool const restart )
```

Performs a read from the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_RX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl, p_dest or bytes is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_IN_USE	Bus busy condition. Another transfer was in progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Write()**

```
fsp_err_t R_IIC_MASTER_Write ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes, bool const restart )
```

Performs a write to the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_TX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl or p_src is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_IN_USE	Bus busy condition. Another transfer was in progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Abort()**

```
fsp_err_t R_IIC_MASTER_Abort ( i2c_master_ctrl_t *const p_api_ctrl)
```

Safely aborts any in-progress transfer and forces the IIC peripheral into ready state.

**Return values**

FSP_SUCCESS	Channel was reset successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

*Note*

*A callback will not be invoked in case an in-progress transfer gets aborted by calling this API.*

◆ **R\_IIC\_MASTER\_SlaveAddressSet()**

```
fsp_err_t R_IIC_MASTER_SlaveAddressSet ( i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode )
```

Sets address and addressing mode of the slave device. This function is used to set the device address and addressing mode of the slave without reconfiguring the entire bus.

**Return values**

FSP_SUCCESS	Address of the slave is set correctly.
FSP_ERR_ASSERTION	Pointer to control structure is NULL.
FSP_ERR_IN_USE	Another transfer was in-progress.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

◆ **R\_IIC\_MASTER\_Close()**

```
fsp_err_t R_IIC_MASTER_Close ( i2c_master_ctrl_t *const p_api_ctrl)
```

Closes the I2C device. May power down IIC peripheral. This function will safely terminate any in-progress I2C transfers.

**Return values**

FSP_SUCCESS	Device closed without issue.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Handle is not initialized. Call R_IIC_MASTER_Open to initialize the control block.

*Note*

*A callback will not be invoked in case an in-progress transfer gets aborted by calling this API.*

◆ **R\_IIC\_MASTER\_CallbackSet()**

```
fsp_err_t R_IIC_MASTER_CallbackSet ( i2c_master_ctrl_t *const p_api_ctrl,
void(*) (i2c_master_callback_args_t *) p_callback, void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_master_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

**◆ R\_IIC\_MASTER\_StatusGet()**

```
fsp_err_t R_IIC_MASTER_StatusGet ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_status_t *
p_status )
```

Provides driver status.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.

**4.2.29 I2C Slave on IIC (r\_iic\_slave)**

## Modules

**Functions**

```
fsp_err_t R_IIC_SLAVE_Open (i2c_slave_ctrl_t *const p_api_ctrl, i2c_slave_cfg_t
const *const p_cfg)
```

```
fsp_err_t R_IIC_SLAVE_Read (i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const
p_dest, uint32_t const bytes)
```

```
fsp_err_t R_IIC_SLAVE_Write (i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const
p_src, uint32_t const bytes)
```

```
fsp_err_t R_IIC_SLAVE_Close (i2c_slave_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_IIC_SLAVE_CallbackSet (i2c_slave_ctrl_t *const p_api_ctrl,
void(*p_callback)(i2c_slave_callback_args_t *), void const *const
p_context, i2c_slave_callback_args_t *const p_callback_memory)
```

**Detailed Description**

Driver for the IIC peripheral on RA MCUs. This module implements the [I2C Slave Interface](#).

**Overview****Features**

- Supports multiple transmission rates
  - Standard Mode Support with up to 100-kHz transaction rate.
  - Fast Mode Support with up to 400-kHz transaction rate.
  - Fast Mode Plus Support with up to 1-MHz transaction rate.
- Reads data written by master device.
- Write data which is read by master device.

- Can accept 0x00 as slave address.
- Can be assigned a 10-bit address.
- Clock stretching is supported and can be implemented via callbacks.
- Provides Transmission/Reception transaction size in the callback.
- I2C Slave can notify the following events via callbacks: Transmission/Reception Request, Transmission/Reception Request for more data, Transmission/Reception Completion, Error Condition.

## Configuration

### Build Time Configurations for r\_iic\_slave

The following build time configurations are defined in fsp\_cfg/r\_iic\_slave\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Connectivity > I2C Slave Driver on r\_iic\_slave

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Slave Driver on r\_iic\_slave. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Interrupt Priority Level > Transmit, Receive, and Transmit End	MCU Specific Options		Select the interrupt priority level. This is set for TXI, RXI, and TEI interrupts.
Interrupt Priority Level > Error	MCU Specific Options		Select the interrupt priority level. This is set for ERI interrupt.
Name	Name must be a valid C symbol	g_i2c_slave0	Module name.
Channel	Value must be a non-negative integer	0	Specify the IIC channel.
Rate	<ul style="list-style-type: none"> <li>• Standard</li> <li>• Fast-mode</li> <li>• Fast-mode plus</li> </ul>	Standard	Select the transfer rate.  If the delay for the requested transfer rate cannot be achieved, the settings with the largest possible transfer rate that is less than or equal to the requested transfer rate are used. The theoretical calculated

delay is printed in a comment in the generated `iic_slave_extended_cfg_t` structure.

Internal Reference Clock	<ul style="list-style-type: none"> <li>• PCLKB / 1</li> <li>• PCLKB / 2</li> <li>• PCLKB / 4</li> <li>• PCLKB / 8</li> <li>• PCLKB / 16</li> <li>• PCLKB / 32</li> <li>• PCLKB / 64</li> <li>• PCLKB / 128</li> </ul>	PCLKB / 1	Select the internal reference clock for IIC slave. The internal reference clock is used only to determine the clock frequency of the noise filter samples.
Digital Noise Filter Stage Select	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Single-stage filter</li> <li>• 2-stage filter</li> <li>• 3-stage filter</li> <li>• 4-stage filter</li> </ul>	3-stage filter	Select the number of digital filter stages for IIC Slave.
Slave Address	Value must be non-negative	0x00	Specify the slave address.
General Call	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Allows the slave to respond to general call address: 0x00.
Address Mode	<ul style="list-style-type: none"> <li>• 7-Bit</li> <li>• 10-Bit</li> </ul>	7-Bit	Select the slave address mode.
Clock Stretching	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configure Clock Stretching.
Callback	Name must be a valid C symbol	NULL	A user callback function must be provided. This will be called from the interrupt service routine (ISR) to report I2C Slave transaction events and status.

## Clock Configuration

The IIC peripheral module uses the PCLKB as its clock source. The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate. If the PCLKB is configured in such a manner that the selected transfer rate cannot be achieved, an error will be returned.

## Pin Configuration

The IIC peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two pins - SDA and SCL for data/address and clock respectively.

## Usage Notes

## Interrupt Configuration

- The IIC error (EEI), receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel must be enabled in the properties of the selected device.
- The interrupt priority of ERI can be set higher than or equal to the interrupt priorities of RXI, TXI and TEI.

### Note

: During master-write slave-read type of operations if the slave device requires to perform clock stretching after the last data byte is received, a higher priority ERI will ensure that the ongoing transaction is completed (by accepting the Stop/Restart condition from the master) before the next transaction is initiated.

: To support clock stretching (Holding SCL low after the falling edge of the 9th clock cycle), 'Clock Stretching' configuration must be enabled.

## Callback

- A callback function must be provided which will be invoked for the cases below:
  - An I2C Master initiates a transmission or reception:  
I2C\_SLAVE\_EVENT\_TX\_REQUEST; I2C\_SLAVE\_EVENT\_RX\_REQUEST
  - A Transmission or reception has been completed:  
I2C\_SLAVE\_EVENT\_TX\_COMPLETE; I2C\_SLAVE\_EVENT\_RX\_COMPLETE
  - An I2C Master is requesting to read or write more data:  
I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST; I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST
  - Error conditions: I2C\_SLAVE\_EVENT\_ABORTED
  - An I2C Master initiates a general call by passing 0x00 as slave address:  
I2C\_SLAVE\_EVENT\_GENERAL\_CALL
- The callback arguments will contain information about the transaction status/events, bytes transferred and a pointer to the user defined context.
- Clock stretching is enabled by the use of callbacks. This means that the IIC slave can hold the clock line SCL LOW to force the I2C Master into a wait state.
- The table below shows I2C Slave event handling expected in user code:

IIC Slave Callback Event	IIC Slave API expected to be called
I2C_SLAVE_EVENT_ABORTED	Handle event based on application
I2C_SLAVE_EVENT_RX_COMPLETE	Handle event based on application
I2C_SLAVE_EVENT_TX_COMPLETE	Handle event based on application
I2C_SLAVE_EVENT_RX_REQUEST	R_IIC_SLAVE_Read API. If the slave is a Write Only device call this API with 0 bytes to send a NACK to the master.
I2C_SLAVE_EVENT_TX_REQUEST	R_IIC_SLAVE_Write API
I2C_SLAVE_EVENT_RX_MORE_REQUEST	R_IIC_SLAVE_Read API. If the slave cannot read any more data call this API with 0 bytes to send a NACK to the master.
I2C_SLAVE_EVENT_TX_MORE_REQUEST	R_IIC_SLAVE_Write API
I2C_SLAVE_EVENT_GENERAL_CALL	R_IIC_SLAVE_Read

- If parameter checking is enabled and R\_IIC\_SLAVE\_Read API is not called for I2C\_SLAVE\_EVENT\_RX\_REQUEST and/or I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST, the slave will send a NACK to the master and would eventually timeout.
- R\_IIC\_SLAVE\_Write API is not called for I2C\_SLAVE\_EVENT\_TX\_REQUEST and/or I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST:
  - Slave timeout is less than Master timeout: The slave will timeout and release the bus causing the master to read 0xFF for every remaining byte.
  - Slave timeout is more than Master timeout: The master will timeout first followed by the slave.

## IIC Slave Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLKB settings is calculated and used.

## Limitations

- When 'Clock Stretching' configuration is enabled, the receive operation will not utilize the double buffer arrangement in hardware for a continuous read. This means that the read operation would happen in single byte units such that the active master would send the next byte only when the slave has read the current byte of data.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_IIC\_SLAVE in an application. This example shows how this driver can be used for basic read and write operations.

```
iic_master_instance_ctrl_t g_i2c_master_ctrl;
i2c_master_cfg_t g_i2c_master_cfg =
{
    .channel      = I2C_MASTER_CHANNEL_2,
    .rate         = I2C_MASTER_RATE_STANDARD,
    .slave        = I2C_7BIT_ADDR_IIC_SLAVE,
    .addr_mode    = I2C_MASTER_ADDR_MODE_7BIT,
    .p_callback   = i2c_master_callback, // Callback
    .p_context    = &g_i2c_master_ctrl,
    .p_transfer_tx = NULL,
    .p_transfer_rx = NULL,
    .p_extend     = &g_iic_master_cfg_extend_standard_mode
};
iic_slave_instance_ctrl_t g_i2c_slave_ctrl;
i2c_slave_cfg_t g_i2c_slave_cfg =
```

```
{
    .channel      = I2C_SLAVE_CHANNEL_0,
    .rate        = I2C_SLAVE_RATE_STANDARD,
    .slave       = I2C_7BIT_ADDR_IIC_SLAVE,
    .addr_mode   = I2C_SLAVE_ADDR_MODE_7BIT,
    .p_callback  = i2c_slave_callback, // Callback
    .p_context   = &g_i2c_slave_ctrl,
    .p_extend    = &g_iic_slave_cfg_extend_standard_mode
};

void i2c_master_callback (i2c_master_callback_args_t * p_args)
{
    g_i2c_master_callback_event = p_args->event;
}

void i2c_slave_callback (i2c_slave_callback_args_t * p_args)
{
    g_i2c_slave_callback_event = p_args->event;
    if ((p_args->event == I2C_SLAVE_EVENT_RX_COMPLETE) || (p_args->event ==
I2C_SLAVE_EVENT_TX_COMPLETE))
    {
        /* Transaction Successful */
    }
    else if ((p_args->event == I2C_SLAVE_EVENT_RX_REQUEST) || (p_args->event ==
I2C_SLAVE_EVENT_RX_MORE_REQUEST))
    {
        /* Read from Master */
        err = R_IIC_SLAVE_Read(&g_i2c_slave_ctrl, g_i2c_slave_buffer,
g_slave_transfer_length);
        assert(FSP_SUCCESS == err);
    }
    else if ((p_args->event == I2C_SLAVE_EVENT_TX_REQUEST) || (p_args->event ==
I2C_SLAVE_EVENT_TX_MORE_REQUEST))
    {
        /* Write to master */
        err = R_IIC_SLAVE_Write(&g_i2c_slave_ctrl, g_i2c_slave_buffer,
```

```
g_slave_transfer_length);
    assert(FSP_SUCCESS == err);
}
else
{
    /* Error Event - reported through g_i2c_slave_callback_event */
}
}

void basic_example (void)
{
    uint32_t i;
    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
    g_slave_transfer_length = I2C_BUFFER_SIZE_BYTES;
    /* Pin connections:
    * Channel 0 SDA <--> Channel 2 SDA
    * Channel 0 SCL <--> Channel 2 SCL
    */
    /* Initialize the IIC Slave module */
    err = R_IIC_SLAVE_Open(&g_i2c_slave_ctrl, &g_i2c_slave_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Initialize the IIC Master module */
    err = R_IIC_MASTER_Open(&g_i2c_master_ctrl, &g_i2c_master_cfg);
    assert(FSP_SUCCESS == err);
    /* Write some data to the transmit buffer */
    for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)
    {
        g_i2c_master_tx_buffer[i] = (uint8_t) i;
    }
    /* Send data to I2C slave */
    g_i2c_master_callback_event = I2C_MASTER_EVENT_ABORTED;
    g_i2c_slave_callback_event = I2C_SLAVE_EVENT_ABORTED;
    err = R_IIC_MASTER_Write(&g_i2c_master_ctrl, &g_i2c_master_tx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
```

```
    assert(FSP_SUCCESS == err);

    /* Since there is nothing else to do, block until Callback triggers
     * The Slave Callback will call the R_IIC_SLAVE_Read API to service the Master Write
    Request.
     */

    while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_master_callback_event ||
           I2C_SLAVE_EVENT_RX_COMPLETE != g_i2c_slave_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

        timeout_ms--;
    }

    if ((I2C_MASTER_EVENT_ABORTED == g_i2c_master_callback_event) ||
        (I2C_SLAVE_EVENT_ABORTED == g_i2c_slave_callback_event))
    {
        __BKPT(0);
    }

    /* Read data back from the I2C slave */

    g_i2c_master_callback_event = I2C_MASTER_EVENT_ABORTED;

    g_i2c_slave_callback_event = I2C_SLAVE_EVENT_ABORTED;

    timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

    err = R_IIC_MASTER_Read(&g_i2c_master_ctrl, &g_i2c_master_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);

    assert(FSP_SUCCESS == err);

    /* Since there is nothing else to do, block until Callback triggers
     * The Slave Callback will call the R_IIC_SLAVE_Write API to service the Master Read
    Request.
     */

    while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_master_callback_event ||
           I2C_SLAVE_EVENT_TX_COMPLETE != g_i2c_slave_callback_event) && timeout_ms)
    {
        R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

        timeout_ms--;
    }

    if ((I2C_MASTER_EVENT_ABORTED == g_i2c_master_callback_event) ||
```

```

    (I2C_SLAVE_EVENT_ABORTED == g_i2c_slave_callback_event))
{
    __BKPT(0);
}

/* Verify the read data */
if (0U != memcmp(g_i2c_master_tx_buffer, g_i2c_master_rx_buffer,
I2C_BUFFER_SIZE_BYTES))
{
    __BKPT(0);
}
}

```

## Data Structures

struct [iic\\_slave\\_clock\\_settings\\_t](#)

struct [iic\\_slave\\_extended\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ [iic\\_slave\\_clock\\_settings\\_t](#)

struct <a href="#">iic_slave_clock_settings_t</a>		
I2C clock settings		
Data Fields		
uint8_t	cks_value	Internal Reference Clock Select.
uint8_t	brl_value	Low-level period of SCL clock.
uint8_t	digital_filter_stages	Number of digital filter stages based on brl_value.

### ◆ [iic\\_slave\\_extended\\_cfg\\_t](#)

struct <a href="#">iic_slave_extended_cfg_t</a>		
R_IIC_SLAVE extended configuration		
Data Fields		
<a href="#">iic_slave_clock_settings_t</a>	clock_settings	I2C Clock settings.

## Function Documentation

◆ **R\_IIC\_SLAVE\_Open()**

```
fsp_err_t R_IIC_SLAVE_Open ( i2c_slave_ctrl_t *const p_api_ctrl, i2c_slave_cfg_t const *const p_cfg )
```

Opens the I2C slave device.

**Return values**

FSP_SUCCESS	I2C slave device opened successfully.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel is not available on this MCU.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ul style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Set the rate to fast mode plus on a channel which does not support it.</li> <li>5. Invalid IRQ number assigned</li> </ul>

◆ **R\_IIC\_SLAVE\_Read()**

```
fsp_err_t R_IIC_SLAVE_Read ( i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes )
```

Performs a read from the I2C Master device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C slave read operation will begin. The caller will be notified when the operation has finished by an I2C\_SLAVE\_EVENT\_RX\_COMPLETE in the callback. In case the master continues to write more data, an I2C\_SLAVE\_EVENT\_RX\_MORE\_REQUEST will be issued via callback. In case of errors, an I2C\_SLAVE\_EVENT\_ABORTED will be issued via callback.

**Return values**

FSP_SUCCESS	Function executed without issue
FSP_ERR_ASSERTION	p_api_ctrl, bytes or p_dest is NULL.
FSP_ERR_IN_USE	Another transfer was in progress.
FSP_ERR_NOT_OPEN	Device is not open.

◆ **R\_IIC\_SLAVE\_Write()**

```
fsp_err_t R_IIC_SLAVE_Write ( i2c_slave_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes )
```

Performs a write to the I2C Master device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C slave write operation will begin. The caller will be notified when the operation has finished by an I2C\_SLAVE\_EVENT\_TX\_COMPLETE in the callback. In case the master continues to read more data, an I2C\_SLAVE\_EVENT\_TX\_MORE\_REQUEST will be issued via callback. In case of errors, an I2C\_SLAVE\_EVENT\_ABORTED will be issued via callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_api_ctrl or p_src is NULL.
FSP_ERR_IN_USE	Another transfer was in progress.
FSP_ERR_NOT_OPEN	Device is not open.

◆ **R\_IIC\_SLAVE\_Close()**

```
fsp_err_t R_IIC_SLAVE_Close ( i2c_slave_ctrl_t *const p_api_ctrl)
```

Closes the I2C device.

**Return values**

FSP_SUCCESS	Device closed successfully.
FSP_ERR_NOT_OPEN	Device not opened.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.

### ◆ R\_IIC\_SLAVE\_CallbackSet()

```
fsp_err_t R_IIC_SLAVE_CallbackSet ( i2c_slave_ctrl_t *const p_api_ctrl,
void(*) (i2c_slave_callback_args_t *) p_callback, void const *const p_context,
i2c_slave_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_slave_api_t::callbackSet`

#### Return values

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.30 I/O Ports (r\_ioport)

### Modules

#### Functions

```
fsp_err_t R_IOPORT_Open (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
```

```
fsp_err_t R_IOPORT_Close (ioport_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_IOPORT_PinsCfg (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
```

```
fsp_err_t R_IOPORT_PinCfg (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
```

```
fsp_err_t R_IOPORT_PinEventInputRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_event)
```

```
fsp_err_t R_IOPORT_PinEventOutputWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t pin_value)
```

```
fsp_err_t R_IOPORT_PinRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)
```

```
fsp_err_t R_IOPORT_PinWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)
```

```
fsp_err_t R_IOPORT_PortDirectionSet (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)
```

```
fsp_err_t R_IOPORT_PortEventInputRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *event_data)
```

```
fsp_err_t R_IOPORT_PortEventOutputWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t event_data, ioport_size_t mask_value)
```

```
fsp_err_t R_IOPORT_PortRead (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)
```

```
fsp_err_t R_IOPORT_PortWrite (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)
```

```
fsp_err_t R_IOPORT_EthernetModeCfg (ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t channel, ioport_ethernet_mode_t mode)
```

## Detailed Description

Driver for the I/O Ports peripheral on RA MCUs. This module implements the [I/O Port Interface](#).

## Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC, or bus control pins.

### Features

The IOPORT HAL module can configure the following pin settings:

- Pin direction
- Default output state
- Pull-up
- NMOS/PMOS
- Drive strength
- Event edge trigger (falling, rising or both)
- Whether the pin is to be used as an IRQ pin
- Whether the pin is to be used as an analog pin
- Peripheral connection

The module also provides the following functionality:

- Read/write GPIO pins/ports
- Sets event output data
- Reads event input data

## Configuration

The I/O PORT HAL module must be configured by the user for the desired operation. The operating

state of an I/O pin can be set via the RA Configuraton tool. When the project is built a pin configuration file is created. The BSP will automatically configure the MCU IO ports accordingly at startup using the same API functions mentioned in this document.

## Build Time Configurations for r\_ioport

The following build time configurations are defined in fsp\_cfg/r\_ioport\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > System > I/O Port Driver on r\_ioport

This module can be added to the Stacks tab via New Stack > Driver > System > I/O Port Driver on r\_ioport.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_ioport	Module name.
Port 1 ELC Trigger Source	MCU Specific Options		ELC source that will trigger PORT1
Port 2 ELC Trigger Source	MCU Specific Options		ELC source that will trigger PORT2
Port 3 ELC Trigger Source	MCU Specific Options		ELC source that will trigger PORT3
Port 4 ELC Trigger Source	MCU Specific Options		ELC source that will trigger PORT4
Pin Configuration Name	Name must be a valid C symbol	g_bsp_pin_cfg	Name for pin configuration structure

## Clock Configuration

The I/O PORT HAL module does not require a specific clock configuration.

## Pin Configuration

The IOPORT module is used for configuring pins.

# Usage Notes

## Port Group Function for ELC

Depending on pin configuration, the IOPORT module can perform automatic reads and writes on ports 1-4 on receipt of an ELC event.

When an event is received by a port, the state of the input pins on the port is saved in a hardware register. Simultaneously, the state of output pins on the port is set or cleared based on settings

configured by the user. The functions [R\\_IOPORT\\_PinEventInputRead](#) and [R\\_IOPORT\\_PortEventInputRead](#) allow reading the last event input state of a pin or port, and event-triggered pin output can be configured through [R\\_IOPORT\\_PinEventOutputWrite](#) and [R\\_IOPORT\\_PortEventOutputWrite](#).

In addition, each pin on ports 1-4 can be configured to trigger an ELC event on rising, falling or both edges. This event can be used to activate other modules when the pin changes state.

#### Note

*The number of ELC-aware ports vary across MCUs. Refer to the Hardware User's Manual for your device for more details.*

## Examples

### Basic Example

This is a basic example of minimal use of the IOPORT in an application.

```
void basic_example ()
{
    bsp_io_level_t readLevel;
    fsp_err_t      err;

    /* Initialize the IOPORT module and configure the pins
     * Note: The default pin configuration name in the RA Configuraton tool is
     * g_bsp_pin_cfg */
    err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Call R_IOPORT_PinsCfg if the configuration was not part of initial configurations
    made in open */
    err = R_IOPORT_PinsCfg(&g_ioport_ctrl, &g_runtime_pin_cfg);
    assert(FSP_SUCCESS == err);

    /* Set Pin 00 of Port 06 to High */
    err = R_IOPORT_PinWrite(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, BSP_IO_LEVEL_HIGH
);
    assert(FSP_SUCCESS == err);

    /* Read Pin 00 of Port 06*/
    err = R_IOPORT_PinRead(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, &readLevel);
    assert(FSP_SUCCESS == err);
}
```

## Blinky Example

This example uses IOPORT to configure and toggle a pin to blink an LED.

```
void blinky_example ()
{
    fsp_err_t err;

    /* Initialize the IOPORT module and configure the pins */
    err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Configure Pin as output
     * Call the R_IOPORT_PinCfg if the configuration was not part of initial
    configurations made in open */
    err = R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00,
BSP_IO_DIRECTION_OUTPUT);
    assert(FSP_SUCCESS == err);

    bsp_io_level_t level = BSP_IO_LEVEL_LOW;

    while (1)
    {
        /* Determine the next state of the LEDs */
        if (BSP_IO_LEVEL_LOW == level)
        {
            level = BSP_IO_LEVEL_HIGH;
        }
        else
        {
            level = BSP_IO_LEVEL_LOW;
        }

        /* Update LED on RA6M3-PK */
        err = R_IOPORT_PinWrite(&g_ioport_ctrl, BSP_IO_PORT_06_PIN_00, level);
        assert(FSP_SUCCESS == err);

        /* Delay */
        R_BSP_SoftwareDelay(100, BSP_DELAY_UNITS_MILLISECONDS); // NOLINT
    }
}
```

```
}
```

## ELC Example

This is an example of using IOPORT with ELC events. The ELC event system allows the captured data to be stored when it occurs and then read back at a later time.

```
static elc_instance_ctrl_t g_elc_ctrl;
static elc_cfg_t g_elc_cfg;
void ioport_elc_example ()
{
    bsp_io_level_t eventValue;
    fsp_err_t      err;

    /* Initializes the software and sets the links defined in the control structure. */
    err = R_ELC_Open(&g_elc_ctrl, &g_elc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Create or modify a link between a peripheral function and an event source. */
    err = R_ELC_LinkSet(&g_elc_ctrl, (elc_peripheral_t) ELC_PERIPHERAL_IOPORT2,
ELC_EVENT_ELC_SOFTWARE_EVENT_0);
    assert(FSP_SUCCESS == err);

    /* Globally enable event linking in the ELC. */
    err = R_ELC_Enable(&g_elc_ctrl);
    assert(FSP_SUCCESS == err);

    /* Initialize the IOPORT module and configure the pins */
    err = R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
    assert(FSP_SUCCESS == err);

    /* Call the R_IOPORT_PinCfg if the configuration was not part of initial
configurations made in open */
    err = R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_02_PIN_00,
BSP_IO_DIRECTION_INPUT);
    assert(FSP_SUCCESS == err);

    /* Generate an event signal through software to the linked peripheral. */
    err = R_ELC_SoftwareEventGenerate(&g_elc_ctrl, ELC_SOFTWARE_EVENT_0);
    assert(FSP_SUCCESS == err);
}
```

```

/* Read Pin Event Input. The data(BSP_IO_LEVEL_HIGH/ BSP_IO_LEVEL_LOW) from
BSP_IO_PORT_02_PIN_00 is read into the
 * EIDR bit */
err = R_IOPORT_PinEventInputRead(&g_ioport_ctrl, BSP_IO_PORT_02_PIN_00,
&eventValue);
assert(FSP_SUCCESS == err);
}

```

## Data Structures

struct [ioport\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [ioport\\_port\\_pin\\_t](#)

## Data Structure Documentation

### ◆ ioport\_instance\_ctrl\_t

struct [ioport\\_instance\\_ctrl\\_t](#)

IOPORT private control block. DO NOT MODIFY. Initialization occurs when [R\\_IOPORT\\_Open\(\)](#) is called.

## Enumeration Type Documentation

### ◆ ioport\_port\_pin\_t

enum [ioport\\_port\\_pin\\_t](#)

Superset list of all possible IO port pins.

Enumerator	
<a href="#">IOPORT_PORT_00_PIN_00</a>	IO port 0 pin 0.
<a href="#">IOPORT_PORT_00_PIN_01</a>	IO port 0 pin 1.
<a href="#">IOPORT_PORT_00_PIN_02</a>	IO port 0 pin 2.
<a href="#">IOPORT_PORT_00_PIN_03</a>	IO port 0 pin 3.
<a href="#">IOPORT_PORT_00_PIN_04</a>	IO port 0 pin 4.
<a href="#">IOPORT_PORT_00_PIN_05</a>	IO port 0 pin 5.
<a href="#">IOPORT_PORT_00_PIN_06</a>	IO port 0 pin 6.

IOPORT_PORT_00_PIN_07	IO port 0 pin 7.
IOPORT_PORT_00_PIN_08	IO port 0 pin 8.
IOPORT_PORT_00_PIN_09	IO port 0 pin 9.
IOPORT_PORT_00_PIN_10	IO port 0 pin 10.
IOPORT_PORT_00_PIN_11	IO port 0 pin 11.
IOPORT_PORT_00_PIN_12	IO port 0 pin 12.
IOPORT_PORT_00_PIN_13	IO port 0 pin 13.
IOPORT_PORT_00_PIN_14	IO port 0 pin 14.
IOPORT_PORT_00_PIN_15	IO port 0 pin 15.
IOPORT_PORT_01_PIN_00	IO port 1 pin 0.
IOPORT_PORT_01_PIN_01	IO port 1 pin 1.
IOPORT_PORT_01_PIN_02	IO port 1 pin 2.
IOPORT_PORT_01_PIN_03	IO port 1 pin 3.
IOPORT_PORT_01_PIN_04	IO port 1 pin 4.
IOPORT_PORT_01_PIN_05	IO port 1 pin 5.
IOPORT_PORT_01_PIN_06	IO port 1 pin 6.
IOPORT_PORT_01_PIN_07	IO port 1 pin 7.
IOPORT_PORT_01_PIN_08	IO port 1 pin 8.
IOPORT_PORT_01_PIN_09	IO port 1 pin 9.
IOPORT_PORT_01_PIN_10	IO port 1 pin 10.
IOPORT_PORT_01_PIN_11	IO port 1 pin 11.
IOPORT_PORT_01_PIN_12	IO port 1 pin 12.
IOPORT_PORT_01_PIN_13	IO port 1 pin 13.
IOPORT_PORT_01_PIN_14	IO port 1 pin 14.

IOPORT_PORT_01_PIN_15	IO port 1 pin 15.
IOPORT_PORT_02_PIN_00	IO port 2 pin 0.
IOPORT_PORT_02_PIN_01	IO port 2 pin 1.
IOPORT_PORT_02_PIN_02	IO port 2 pin 2.
IOPORT_PORT_02_PIN_03	IO port 2 pin 3.
IOPORT_PORT_02_PIN_04	IO port 2 pin 4.
IOPORT_PORT_02_PIN_05	IO port 2 pin 5.
IOPORT_PORT_02_PIN_06	IO port 2 pin 6.
IOPORT_PORT_02_PIN_07	IO port 2 pin 7.
IOPORT_PORT_02_PIN_08	IO port 2 pin 8.
IOPORT_PORT_02_PIN_09	IO port 2 pin 9.
IOPORT_PORT_02_PIN_10	IO port 2 pin 10.
IOPORT_PORT_02_PIN_11	IO port 2 pin 11.
IOPORT_PORT_02_PIN_12	IO port 2 pin 12.
IOPORT_PORT_02_PIN_13	IO port 2 pin 13.
IOPORT_PORT_02_PIN_14	IO port 2 pin 14.
IOPORT_PORT_02_PIN_15	IO port 2 pin 15.
IOPORT_PORT_03_PIN_00	IO port 3 pin 0.
IOPORT_PORT_03_PIN_01	IO port 3 pin 1.
IOPORT_PORT_03_PIN_02	IO port 3 pin 2.
IOPORT_PORT_03_PIN_03	IO port 3 pin 3.
IOPORT_PORT_03_PIN_04	IO port 3 pin 4.
IOPORT_PORT_03_PIN_05	IO port 3 pin 5.
IOPORT_PORT_03_PIN_06	IO port 3 pin 6.

IOPORT_PORT_03_PIN_07	IO port 3 pin 7.
IOPORT_PORT_03_PIN_08	IO port 3 pin 8.
IOPORT_PORT_03_PIN_09	IO port 3 pin 9.
IOPORT_PORT_03_PIN_10	IO port 3 pin 10.
IOPORT_PORT_03_PIN_11	IO port 3 pin 11.
IOPORT_PORT_03_PIN_12	IO port 3 pin 12.
IOPORT_PORT_03_PIN_13	IO port 3 pin 13.
IOPORT_PORT_03_PIN_14	IO port 3 pin 14.
IOPORT_PORT_03_PIN_15	IO port 3 pin 15.
IOPORT_PORT_04_PIN_00	IO port 4 pin 0.
IOPORT_PORT_04_PIN_01	IO port 4 pin 1.
IOPORT_PORT_04_PIN_02	IO port 4 pin 2.
IOPORT_PORT_04_PIN_03	IO port 4 pin 3.
IOPORT_PORT_04_PIN_04	IO port 4 pin 4.
IOPORT_PORT_04_PIN_05	IO port 4 pin 5.
IOPORT_PORT_04_PIN_06	IO port 4 pin 6.
IOPORT_PORT_04_PIN_07	IO port 4 pin 7.
IOPORT_PORT_04_PIN_08	IO port 4 pin 8.
IOPORT_PORT_04_PIN_09	IO port 4 pin 9.
IOPORT_PORT_04_PIN_10	IO port 4 pin 10.
IOPORT_PORT_04_PIN_11	IO port 4 pin 11.
IOPORT_PORT_04_PIN_12	IO port 4 pin 12.
IOPORT_PORT_04_PIN_13	IO port 4 pin 13.
IOPORT_PORT_04_PIN_14	IO port 4 pin 14.

IOPORT_PORT_04_PIN_15	IO port 4 pin 15.
IOPORT_PORT_05_PIN_00	IO port 5 pin 0.
IOPORT_PORT_05_PIN_01	IO port 5 pin 1.
IOPORT_PORT_05_PIN_02	IO port 5 pin 2.
IOPORT_PORT_05_PIN_03	IO port 5 pin 3.
IOPORT_PORT_05_PIN_04	IO port 5 pin 4.
IOPORT_PORT_05_PIN_05	IO port 5 pin 5.
IOPORT_PORT_05_PIN_06	IO port 5 pin 6.
IOPORT_PORT_05_PIN_07	IO port 5 pin 7.
IOPORT_PORT_05_PIN_08	IO port 5 pin 8.
IOPORT_PORT_05_PIN_09	IO port 5 pin 9.
IOPORT_PORT_05_PIN_10	IO port 5 pin 10.
IOPORT_PORT_05_PIN_11	IO port 5 pin 11.
IOPORT_PORT_05_PIN_12	IO port 5 pin 12.
IOPORT_PORT_05_PIN_13	IO port 5 pin 13.
IOPORT_PORT_05_PIN_14	IO port 5 pin 14.
IOPORT_PORT_05_PIN_15	IO port 5 pin 15.
IOPORT_PORT_06_PIN_00	IO port 6 pin 0.
IOPORT_PORT_06_PIN_01	IO port 6 pin 1.
IOPORT_PORT_06_PIN_02	IO port 6 pin 2.
IOPORT_PORT_06_PIN_03	IO port 6 pin 3.
IOPORT_PORT_06_PIN_04	IO port 6 pin 4.
IOPORT_PORT_06_PIN_05	IO port 6 pin 5.
IOPORT_PORT_06_PIN_06	IO port 6 pin 6.

IOPORT_PORT_06_PIN_07	IO port 6 pin 7.
IOPORT_PORT_06_PIN_08	IO port 6 pin 8.
IOPORT_PORT_06_PIN_09	IO port 6 pin 9.
IOPORT_PORT_06_PIN_10	IO port 6 pin 10.
IOPORT_PORT_06_PIN_11	IO port 6 pin 11.
IOPORT_PORT_06_PIN_12	IO port 6 pin 12.
IOPORT_PORT_06_PIN_13	IO port 6 pin 13.
IOPORT_PORT_06_PIN_14	IO port 6 pin 14.
IOPORT_PORT_06_PIN_15	IO port 6 pin 15.
IOPORT_PORT_07_PIN_00	IO port 7 pin 0.
IOPORT_PORT_07_PIN_01	IO port 7 pin 1.
IOPORT_PORT_07_PIN_02	IO port 7 pin 2.
IOPORT_PORT_07_PIN_03	IO port 7 pin 3.
IOPORT_PORT_07_PIN_04	IO port 7 pin 4.
IOPORT_PORT_07_PIN_05	IO port 7 pin 5.
IOPORT_PORT_07_PIN_06	IO port 7 pin 6.
IOPORT_PORT_07_PIN_07	IO port 7 pin 7.
IOPORT_PORT_07_PIN_08	IO port 7 pin 8.
IOPORT_PORT_07_PIN_09	IO port 7 pin 9.
IOPORT_PORT_07_PIN_10	IO port 7 pin 10.
IOPORT_PORT_07_PIN_11	IO port 7 pin 11.
IOPORT_PORT_07_PIN_12	IO port 7 pin 12.
IOPORT_PORT_07_PIN_13	IO port 7 pin 13.
IOPORT_PORT_07_PIN_14	IO port 7 pin 14.

IOPORT_PORT_07_PIN_15	IO port 7 pin 15.
IOPORT_PORT_08_PIN_00	IO port 8 pin 0.
IOPORT_PORT_08_PIN_01	IO port 8 pin 1.
IOPORT_PORT_08_PIN_02	IO port 8 pin 2.
IOPORT_PORT_08_PIN_03	IO port 8 pin 3.
IOPORT_PORT_08_PIN_04	IO port 8 pin 4.
IOPORT_PORT_08_PIN_05	IO port 8 pin 5.
IOPORT_PORT_08_PIN_06	IO port 8 pin 6.
IOPORT_PORT_08_PIN_07	IO port 8 pin 7.
IOPORT_PORT_08_PIN_08	IO port 8 pin 8.
IOPORT_PORT_08_PIN_09	IO port 8 pin 9.
IOPORT_PORT_08_PIN_10	IO port 8 pin 10.
IOPORT_PORT_08_PIN_11	IO port 8 pin 11.
IOPORT_PORT_08_PIN_12	IO port 8 pin 12.
IOPORT_PORT_08_PIN_13	IO port 8 pin 13.
IOPORT_PORT_08_PIN_14	IO port 8 pin 14.
IOPORT_PORT_08_PIN_15	IO port 8 pin 15.
IOPORT_PORT_09_PIN_00	IO port 9 pin 0.
IOPORT_PORT_09_PIN_01	IO port 9 pin 1.
IOPORT_PORT_09_PIN_02	IO port 9 pin 2.
IOPORT_PORT_09_PIN_03	IO port 9 pin 3.
IOPORT_PORT_09_PIN_04	IO port 9 pin 4.
IOPORT_PORT_09_PIN_05	IO port 9 pin 5.
IOPORT_PORT_09_PIN_06	IO port 9 pin 6.

IOPORT_PORT_09_PIN_07	IO port 9 pin 7.
IOPORT_PORT_09_PIN_08	IO port 9 pin 8.
IOPORT_PORT_09_PIN_09	IO port 9 pin 9.
IOPORT_PORT_09_PIN_10	IO port 9 pin 10.
IOPORT_PORT_09_PIN_11	IO port 9 pin 11.
IOPORT_PORT_09_PIN_12	IO port 9 pin 12.
IOPORT_PORT_09_PIN_13	IO port 9 pin 13.
IOPORT_PORT_09_PIN_14	IO port 9 pin 14.
IOPORT_PORT_09_PIN_15	IO port 9 pin 15.
IOPORT_PORT_10_PIN_00	IO port 10 pin 0.
IOPORT_PORT_10_PIN_01	IO port 10 pin 1.
IOPORT_PORT_10_PIN_02	IO port 10 pin 2.
IOPORT_PORT_10_PIN_03	IO port 10 pin 3.
IOPORT_PORT_10_PIN_04	IO port 10 pin 4.
IOPORT_PORT_10_PIN_05	IO port 10 pin 5.
IOPORT_PORT_10_PIN_06	IO port 10 pin 6.
IOPORT_PORT_10_PIN_07	IO port 10 pin 7.
IOPORT_PORT_10_PIN_08	IO port 10 pin 8.
IOPORT_PORT_10_PIN_09	IO port 10 pin 9.
IOPORT_PORT_10_PIN_10	IO port 10 pin 10.
IOPORT_PORT_10_PIN_11	IO port 10 pin 11.
IOPORT_PORT_10_PIN_12	IO port 10 pin 12.
IOPORT_PORT_10_PIN_13	IO port 10 pin 13.
IOPORT_PORT_10_PIN_14	IO port 10 pin 14.

IOPORT_PORT_10_PIN_15	IO port 10 pin 15.
IOPORT_PORT_11_PIN_00	IO port 11 pin 0.
IOPORT_PORT_11_PIN_01	IO port 11 pin 1.
IOPORT_PORT_11_PIN_02	IO port 11 pin 2.
IOPORT_PORT_11_PIN_03	IO port 11 pin 3.
IOPORT_PORT_11_PIN_04	IO port 11 pin 4.
IOPORT_PORT_11_PIN_05	IO port 11 pin 5.
IOPORT_PORT_11_PIN_06	IO port 11 pin 6.
IOPORT_PORT_11_PIN_07	IO port 11 pin 7.
IOPORT_PORT_11_PIN_08	IO port 11 pin 8.
IOPORT_PORT_11_PIN_09	IO port 11 pin 9.
IOPORT_PORT_11_PIN_10	IO port 11 pin 10.
IOPORT_PORT_11_PIN_11	IO port 11 pin 11.
IOPORT_PORT_11_PIN_12	IO port 11 pin 12.
IOPORT_PORT_11_PIN_13	IO port 11 pin 13.
IOPORT_PORT_11_PIN_14	IO port 11 pin 14.
IOPORT_PORT_11_PIN_15	IO port 11 pin 15.

## Function Documentation

---

◆ **R\_IOPORT\_Open()**

```
fsp_err_t R_IOPORT_Open ( ioport_ctrl_t *const p_ctrl, const ioport_cfg_t * p_cfg )
```

Initializes internal driver data, then calls pin configuration function to configure pins.

**Return values**

FSP_SUCCESS	Pin configuration data written to PFS register(s)
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_ALREADY_OPEN	Module is already open.

◆ **R\_IOPORT\_Close()**

```
fsp_err_t R_IOPORT_Close ( ioport_ctrl_t *const p_ctrl)
```

Resets IOPORT registers. Implements `ioport_api_t::close`

**Return values**

FSP_SUCCESS	The IOPORT was successfully uninitialized
FSP_ERR_ASSERTION	p_ctrl was NULL
FSP_ERR_NOT_OPEN	The module has not been opened

◆ **R\_IOPORT\_PinsCfg()**

```
fsp_err_t R_IOPORT_PinsCfg ( ioport_ctrl_t *const p_ctrl, const ioport_cfg_t * p_cfg )
```

Configures the functions of multiple pins by loading configuration data into pin PFS registers. Implements `ioport_api_t::pinsCfg`.

This function initializes the supplied list of PmnPFS registers with the supplied values. This data can be generated by the Pins tab of the RA Configuration editor or manually by the developer. Different pin configurations can be loaded for different situations such as low power modes and testing.

**Return values**

FSP_SUCCESS	Pin configuration data written to PFS register(s)
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

## ◆ R\_IOPORT\_PinCfg()

```
fsp_err_t R_IOPORT_PinCfg ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg )
```

Configures the settings of a pin. Implements `ioport_api_t::pinCfg`.

**Return values**

FSP_SUCCESS	Pin configured
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

**Note**

*This function is re-entrant for different pins. This function will change the configuration of the pin with the new configuration. For example it is not possible with this function to change the drive strength of a pin while leaving all the other pin settings unchanged. To achieve this the original settings with the required change will need to be written using this function.*

## ◆ R\_IOPORT\_PinEventInputRead()

```
fsp_err_t R_IOPORT_PinEventInputRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t * p_pin_event )
```

Reads the value of the event input data of a specific pin. Implements `ioport_api_t::pinEventInputRead`.

The pin event data is captured in response to a trigger from the ELC. This function enables this data to be read. Using the event system allows the captured data to be stored when it occurs and then read back at a later time.

**Return values**

FSP_SUCCESS	Pin read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_INVALID_ARGUMENT	Port is not valid ELC PORT.

**Note**

*This function is re-entrant.*

◆ **R\_IOPORT\_PinEventOutputWrite()**

```
fsp_err_t R_IOPORT_PinEventOutputWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t pin_value )
```

This function writes the event output data value to a pin. Implements `ioport_api_t::pinEventOutputWrite`.

Using the event system enables a pin state to be stored by this function in advance of being output on the pin. The output to the pin will occur when the ELC event occurs.

**Return values**

FSP_SUCCESS	Pin event data written
FSP_ERR_INVALID_ARGUMENT	Port or Pin or value not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

**Note**

*This function is re-entrant for different ports.*

◆ **R\_IOPORT\_PinRead()**

```
fsp_err_t R_IOPORT_PinRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *
p_pin_value )
```

Reads the level on a pin. Implements `ioport_api_t::pinRead`.

**Return values**

FSP_SUCCESS	Pin read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

**Note**

*This function is re-entrant for different pins.*

◆ **R\_IOPORT\_PinWrite()**

```
fsp_err_t R_IOPORT_PinWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level )
```

Sets a pin's output either high or low. Implements `ioport_api_t::pinWrite`.

**Return values**

FSP_SUCCESS	Pin written to
FSP_ERR_INVALID_ARGUMENT	The pin and/or level not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

*Note*

*This function is re-entrant for different pins. This function makes use of the PCNTR3 register to atomically modify the level on the specified pin on a port.*

◆ **R\_IOPORT\_PortDirectionSet()**

```
fsp_err_t R_IOPORT_PortDirectionSet ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask )
```

Sets the direction of individual pins on a port. Implements `ioport_api_t::portDirectionSet()`.

Multiple pins on a port can be set to inputs or outputs at once. Each bit in the mask parameter corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. If a bit is set to 1 then the corresponding pin will be changed to an input or an output as specified by the direction values. If a mask bit is set to 0 then the direction of the pin will not be changed.

**Return values**

FSP_SUCCESS	Port direction updated
FSP_ERR_INVALID_ARGUMENT	The port and/or mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

*Note*

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortEventInputRead()

```
fsp_err_t R_IOPORT_PortEventInputRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t * p_event_data )
```

Reads the value of the event input data. Implements `ioport_api_t::portEventInputRead()`.

The event input data for the port will be read. Each bit in the returned value corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on.

The port event data is captured in response to a trigger from the ELC. This function enables this data to be read. Using the event system allows the captured data to be stored when it occurs and then read back at a later time.

#### Return values

FSP_SUCCESS	Port read
FSP_ERR_INVALID_ARGUMENT	Port not a valid ELC port
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

#### Note

*This function is re-entrant for different ports.*

### ◆ R\_IOPORT\_PortEventOutputWrite()

```
fsp_err_t R_IOPORT_PortEventOutputWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t event_data, ioport_size_t mask_value )
```

This function writes the set and reset event output data for a port. Implements `ioport_api_t::portEventOutputWrite`.

Using the event system enables a port state to be stored by this function in advance of being output on the port. The output to the port will occur when the ELC event occurs.

The input value will be written to the specified port when an ELC event configured for that port occurs. Each bit in the value parameter corresponds to a bit on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. Each bit in the mask parameter corresponds to a pin on the port.

#### Return values

FSP_SUCCESS	Port event data written
FSP_ERR_INVALID_ARGUMENT	Port or Mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is re-entrant for different ports.*

◆ **R\_IOPORT\_PortRead()**

```
fsp_err_t R_IOPORT_PortRead ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *
p_port_value )
```

Reads the value on an IO port. Implements `ioport_api_t::portRead`.

The specified port will be read, and the levels for all the pins will be returned. Each bit in the returned value corresponds to a pin on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on.

**Return values**

FSP_SUCCESS	Port read
FSP_ERR_ASSERTION	NULL pointer
FSP_ERR_NOT_OPEN	The module has not been opened

**Note**

*This function is re-entrant for different ports.*

◆ **R\_IOPORT\_PortWrite()**

```
fsp_err_t R_IOPORT_PortWrite ( ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value,
ioport_size_t mask )
```

Writes to multiple pins on a port. Implements `ioport_api_t::portWrite`.

The input value will be written to the specified port. Each bit in the value parameter corresponds to a bit on the port. For example, bit 7 corresponds to pin 7, bit 6 to pin 6, and so on. Each bit in the mask parameter corresponds to a pin on the port.

Only the bits with the corresponding bit in the mask value set will be updated. For example, value = 0xFFFF, mask = 0x0003 results in only bits 0 and 1 being updated.

**Return values**

FSP_SUCCESS	Port written to
FSP_ERR_INVALID_ARGUMENT	The port and/or mask not valid
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointerd

**Note**

*This function is re-entrant for different ports. This function makes use of the PCNTR3 register to atomically modify the levels on the specified pins on a port.*

### ◆ R\_IOPORT\_EthernetModeCfg()

```
fsp_err_t R_IOPORT_EthernetModeCfg ( ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t channel, ioport_ethernet_mode_t mode )
```

Configures Ethernet channel PHY mode. Implements `ioport_api_t::pinEthernetModeCfg`.

#### Return values

FSP_SUCCESS	Ethernet PHY mode set
FSP_ERR_INVALID_ARGUMENT	Channel or mode not valid
FSP_ERR_UNSUPPORTED	Ethernet configuration not supported on this device.
FSP_ERR_NOT_OPEN	The module has not been opened
FSP_ERR_ASSERTION	NULL pointer

#### Note

*This function is not re-entrant.*

## 4.2.31 Independent Watchdog Timer (r\_iwdt)

### Modules

#### Functions

```
fsp_err_t R_IWDT_Refresh (wdt_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_IWDT_Open (wdt_ctrl_t *const p_api_ctrl, wdt_cfg_t const *const p_cfg)
```

```
fsp_err_t R_IWDT_StatusClear (wdt_ctrl_t *const p_api_ctrl, const wdt_status_t status)
```

```
fsp_err_t R_IWDT_StatusGet (wdt_ctrl_t *const p_api_ctrl, wdt_status_t *const p_status)
```

```
fsp_err_t R_IWDT_CounterGet (wdt_ctrl_t *const p_api_ctrl, uint32_t *const p_count)
```

```
fsp_err_t R_IWDT_TimeoutGet (wdt_ctrl_t *const p_api_ctrl, wdt_timeout_values_t *const p_timeout)
```

```
fsp_err_t R_IWDT_CallbackSet (wdt_ctrl_t *const p_ctrl, void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the IWDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

## Overview

The independent watchdog timer is used to recover from unexpected errors in an application. The timer must be refreshed periodically in the permitted count window by the application. If the count is allowed to underflow or refresh occurs outside of the valid refresh period, the IWDT resets the device or generates an NMI.

## Features

The IWDT HAL module has the following key features:

- When the IWDT underflows or is refreshed outside of the permitted refresh window, one of the following events can occur:
  - Resetting of the device
  - Generation of an NMI
- The IWDT begins counting at reset.

## Selecting a Watchdog

RA MCUs have two watchdog peripherals: the watchdog timer (WDT) and the independent watchdog timer (IWDT). When selecting between them, consider these factors:

	WDT	IWDT
Start Mode	The WDT can be started from the application (register start mode) or configured by hardware to start automatically (auto start mode).	The IWDT can only be configured by hardware to start automatically.
Clock Source	The WDT runs off a peripheral clock.	The IWDT has its own clock source which improves safety.

## Configuration

### Build Time Configurations for r\_iwdt

The following build time configurations are defined in fsp\_cfg/r\_iwdt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Monitoring > Watchdog Driver on r\_iwdt

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Watchdog Driver on r\_iwdt. Non-secure callable guard functions can be generated for this module by right clicking the

module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_wdt0	Module name.
NMI callback	Name must be a valid C symbol	NULL	A user callback function can be provided here. If this callback function is provided, it is called from the interrupt service routine (ISR) when the watchdog triggers.

#### Note

The IWDT has additional configurable settings in the OFS0 register in the **BSP** tab properties window. These settings include the following:

- Start Mode
- Timeout Period
- Dedicated Clock Frequency Divisor
- Window End Position
- Window Start Position
- Reset Interrupt Request Select
- Stop Control

Review the OFS0 properties window to see additional details.

## Clock Configuration

The IWDT clock is based on the IWDTCLK frequency. You can set the IWDTCLK frequency divider using the **BSP** tab of the RA Configuration editor.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## NMI Interrupt

The independent watchdog timer uses the NMI, which is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during open is called.

## Period Calculation

The IWDT operates from IWDTCLK. With a IWDTCLK of 15000 Hz, the maximum time from the last refresh to device reset or NMI generation will be just below 35 seconds as detailed below.

$$\text{IWDTCLK} = 15000 \text{ Hz}$$

$$\text{Clock division ratio} = \text{IWDTCLK} / 256$$

$$\text{Timeout period} = 2048 \text{ cycles}$$

$$\text{WDT clock frequency} = 15000 \text{ Hz} / 256 = 58.59 \text{ Hz}$$

$$\text{Cycle time} = 1 / 58.59 \text{ Hz} = 17.067 \text{ ms}$$

Timeout = 17.067 ms x 2048 cycles = 34.95 seconds

## Limitations

Developers should be aware of the following limitations when using the IWDT:

- When using a J-Link debugger the IWDT counter does not count and therefore will not reset the device or generate an NMI. To enable the watchdog to count and generate a reset or NMI while debugging, add this line of code in the application:

```
/* (Optional) Enable the IWDT to count and generate NMI or reset when the
 * debugger is connected. */
R_DEBUG->DBGSTOPPCR_b.DBGSTOP_IWDT = 0;
```

- If the IWDT is configured to stop the counter in low power mode, then your application must restart the watchdog by calling `R_IWDT_Refresh()` after the MCU wakes from low power mode.

## Examples

### IWDT Basic Example

This is a basic example of minimal use of the IWDT in an application.

```
void iwdt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* In auto start mode, the IWDT starts counting immediately when the MCU is powered
on. */

    /* Initializes the module. */
    err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    while (true)
    {
        /* Application work here. */

        /* Refresh before the counter underflows to prevent reset or NMI based on the
setting. */
        (void) R_IWDT_Refresh(&g_iwdt0_ctrl);
    }
}
```

## IWDT Advanced Example

This example demonstrates using a start window and gives an example callback to handle an NMI generated by an underflow or refresh error.

```
#define IWDT_TIMEOUT_COUNTS (2048U)
#define IWDT_MAX_COUNTER (IWDT_TIMEOUT_COUNTS - 1U)
#define IWDT_START_WINDOW_75 ((IWDT_MAX_COUNTER * 3) / 4)
/* Example callback called when a watchdog NMI occurs. */
void iwdt_callback (wdt_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) Determine the source of the NMI. */
    wdt_status_t status = WDT_STATUS_NO_ERROR;
    err = R_IWDT_StatusGet(&g_iwdt0_ctrl, &status);
    assert(FSP_SUCCESS == err);
    /* (Optional) Log source of NMI and any other debug information. */
    /* (Optional) Clear the error flags. */
    err = R_IWDT_StatusClear(&g_iwdt0_ctrl, status);
    assert(FSP_SUCCESS == err);
    /* (Optional) Issue a software reset to reset the MCU. */
    __NVIC_SystemReset();
}
void iwdt_advanced_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* (Optional) Enable the IWDT to count and generate NMI or reset when the
     * debugger is connected. */
    R_DEBUG->DBGSTOPCR_b.DBGSTOP_IWDT = 0;
    /* (Optional) Check if the IWDTRF flag is set to know if the system is
     * recovering from a IWDT reset. */
    if (R_SYSTEM->RSTSR1_b.IWDTRF)
    {
        /* Clear the flag. */
    }
}
```

```
R_SYSTEM->RSTSR1 = 0U;

}

/* Open the module. */
err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Initialize other application code. */
/* Do not call R_IWDT_Refresh() in auto start mode unless the
 * counter is in the acceptable refresh window. */
(void) R_IWDT_Refresh(&g_iwdt0_ctrl);
while (true)
{
/* Application work here. */
/* (Optional) If there is a chance the application takes less time than
 * the start window, verify the IWDT counter is past the start window
 * before refreshing the IWDT. */
uint32_t iwdt_counter = 0U;
do
{
/* Read the current IWDT counter value. */
err = R_IWDT_CounterGet(&g_iwdt0_ctrl, &iwdt_counter);
assert(FSP_SUCCESS == err);
} while (iwdt_counter >= IWDT_START_WINDOW_75);
/* Refresh before the counter underflows to prevent reset or NMI. */
(void) R_IWDT_Refresh(&g_iwdt0_ctrl);
}
}
```

## Data Structures

struct [iwdt\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ iwdt\_instance\_ctrl\_t

struct iwdt\_instance\_ctrl\_t

IWDT control block. DO NOT INITIALIZE. Initialization occurs when [wdt\\_api\\_t::open](#) is called.

Data Fields	
uint32_t	<a href="#">wdt_open</a>
	Indicates whether the open() API has been successfully called.
void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to the user callback in <a href="#">wdt_callback_args_t</a> .
R_IWDT_Type *	<a href="#">p_reg</a>
	Pointer to register base address.
void(*	<a href="#">p_callback</a> )(wdt_callback_args_t *p_args)
	Callback provided when a WDT NMI ISR occurs.

## Function Documentation

### ◆ R\_IWDT\_Refresh()

```
fsp_err_t R_IWDT_Refresh ( wdt_ctrl_t *const p_api_ctrl)
```

Refresh the Independent Watchdog Timer. If the refresh fails due to being performed outside of the permitted refresh period the device will either reset or trigger an NMI ISR to run.

Example:

```
/* Refresh before the counter underflows to prevent reset or NMI based on the
setting. */
(void) R_IWDT_Refresh(&g_iwdt0_ctrl);
```

#### Return values

FSP_SUCCESS	IWDT successfully refreshed.
FSP_ERR_ASSERTION	One or more parameters are NULL pointers.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_Open()**

```
fsp_err_t R_IWDT_Open ( wdt_ctrl_t *const p_api_ctrl, wdt_cfg_t const *const p_cfg )
```

Register the IWDT NMI callback.

Example:

```
/* Initializes the module. */
err = R_IWDT_Open(&g_iwdt0_ctrl, &g_iwdt0_cfg);
```

**Return values**

FSP_SUCCESS	IWDT successfully configured.
FSP_ERR_ASSERTION	Null Pointer.
FSP_ERR_NOT_ENABLED	An attempt to open the IWDT when the OFS0 register is not configured for auto-start mode.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_STATE	The security state of the NMI and the module do not match.

◆ **R\_IWDT\_StatusClear()**

```
fsp_err_t R_IWDT_StatusClear ( wdt_ctrl_t *const p_api_ctrl, const wdt_status_t status )
```

Clear the IWDT status and error flags. Implements `wdt_api_t::statusClear`.

Example:

```
/* (Optional) Clear the error flags. */
err = R_IWDT_StatusClear(&g_iwdt0_ctrl, status);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	IWDT flag(s) successfully cleared.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_StatusGet()**

```
fsp_err_t R_IWDT_StatusGet ( wdt_ctrl_t*const p_api_ctrl, wdt_status_t*const p_status )
```

Read the IWDT status flags. When the IWDT is configured to output a reset on underflow or refresh error reading the status and error flags can be read after reset to establish if the IWDT caused the reset. Reading the status and error flags in NMI output mode indicates whether the IWDT generated the NMI interrupt.

Indicates both status and error conditions.

Example:

```
/* (Optional) Determine the source of the NMI. */
wdt_status_t status = WDT_STATUS_NO_ERROR;
err = R_IWDT_StatusGet(&g_iwdt0_ctrl, &status);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	IWDT status successfully read.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

◆ **R\_IWDT\_CounterGet()**

```
fsp_err_t R_IWDT_CounterGet ( wdt_ctrl_t*const p_api_ctrl, uint32_t*const p_count )
```

Read the current count value of the IWDT. Implements [wdt\\_api\\_t::counterGet](#).

Example:

```
/* Read the current IWDT counter value. */
err = R_IWDT_CounterGet(&g_iwdt0_ctrl, &iwdt_counter);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	IWDT current count successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <a href="#">R_IWDT_Open()</a> first.

## ◆ R\_IWDT\_TimeoutGet()

```
fsp_err_t R_IWDT_TimeoutGet ( wdt_ctrl_t *const p_api_ctrl, wdt_timeout_values_t *const p_timeout )
```

Read timeout information for the watchdog timer. Implements `wdt_api_t::timeoutGet`.

**Return values**

FSP_SUCCESS	IWDT timeout information retrieved successfully.
FSP_ERR_ASSERTION	One or more parameters are NULL pointers.
FSP_ERR_NOT_OPEN	The driver has not been opened. Perform <code>R_IWDT_Open()</code> first.

## ◆ R\_IWDT\_CallbackSet()

```
fsp_err_t R_IWDT_CallbackSet ( wdt_ctrl_t *const p_ctrl, void (*)(wdt_callback_args_t *) p_callback, void const *const p_context, wdt_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `wdt_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

## 4.2.32 JPEG Codec (r\_jpeg)

### Modules

#### Functions

```
fsp_err_t R_JPEG_Open (jpeg_ctrl_t *const p_api_ctrl, jpeg_cfg_t const *const p_cfg)
```

```
fsp_err_t R_JPEG_OutputBufferSet (jpeg_ctrl_t *p_api_ctrl, void *output_buffer, uint32_t output_buffer_size)
```

fsp_err_t	R_JPEG_InputBufferSet (jpeg_ctrl_t *const p_api_ctrl, void *p_data_buffer, uint32_t data_buffer_size)
fsp_err_t	R_JPEG_StatusGet (jpeg_ctrl_t *p_api_ctrl, jpeg_status_t *p_status)
fsp_err_t	R_JPEG_Close (jpeg_ctrl_t *p_api_ctrl)
fsp_err_t	R_JPEG_EncodeImageSizeSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_encode_image_size_t *p_image_size)
fsp_err_t	R_JPEG_DecodeLinesDecodedGet (jpeg_ctrl_t *const p_api_ctrl, uint32_t *const p_lines)
fsp_err_t	R_JPEG_DecodeHorizontalStrideSet (jpeg_ctrl_t *p_api_ctrl, uint32_t horizontal_stride)
fsp_err_t	R_JPEG_DecodeImageSizeGet (jpeg_ctrl_t *p_api_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)
fsp_err_t	R_JPEG_DecodeImageSubsampleSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_decode_subsample_t horizontal_subsample, jpeg_decode_subsample_t vertical_subsample)
fsp_err_t	R_JPEG_DecodePixelFormatGet (jpeg_ctrl_t *p_api_ctrl, jpeg_color_space_t *p_color_space)
fsp_err_t	R_JPEG_ModeSet (jpeg_ctrl_t *const p_api_ctrl, jpeg_mode_t mode)

## Detailed Description

Driver for the JPEG peripheral on RA MCUs. This module implements the [JPEG Codec Interface](#).

## Overview

The JPEG Codec is a hardware block providing accelerated JPEG image encode and decode functionality independent of the CPU. Images can optionally be partially processed facilitating streaming applications.

### Features

The JPEG Codec provides a number of options useful in a variety of applications:

- Basic encoding and decoding
- Streaming input and/or output
- Decoding JPEGs of unknown size
- Shrink (sub-sample) an image during the decoding process
- Rearrange input and output byte order (byte, word and/or longword swap)
- JPEG error detection

The specifications for the codec are as follows:

Feature	Options
Decompression input formats	Baseline JPEG Y'CbCr 4:4:4, 4:2:2, 4:2:0 and 4:1:1
Decompression output formats	ARGB8888, RGB565
Compression input formats	Raw Y'CbCr 4:2:2 only
Compression output formats	Baseline JPEG Y'CbCr 4:2:2 only
Byte reordering	Byte, halfword and/or word swapping on input and output
Interrupt sources	Image size acquired, input/output data pause, decode complete, error
Compatible image sizes	See <a href="#">Minimum Coded Unit (MCU)</a> below

## Configuration

### Build Time Configurations for r\_jpeg

The following build time configurations are defined in fsp\_cfg/r\_jpeg\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected, code for parameter checking is included in the build.
Decode Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	If selected, code for decoding JPEG images is included in the build.
Encode Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If selected, code for encoding JPEG images is included in the build.

### Configurations for Driver > Graphics > JPEG Codec Driver on r\_jpeg

This module can be added to the Stacks tab via New Stack > Driver > Graphics > JPEG Codec Driver on r\_jpeg.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_jpeg0	Module name.
General > Default mode	<ul style="list-style-type: none"> <li>Decode</li> <li>Encode</li> </ul>	Decode	Set the mode to use when calling R_JPEG_Open. This parameter is only used when both Encode and Decode support are enabled.

Decode > Input byte order	MCU Specific Options		Select the byte order of the input data for decoding.
Decode > Output byte order	MCU Specific Options		Select the byte order of the output data for decoding.
Decode > Output color format	<ul style="list-style-type: none"> <li>• ARGB8888 (32-bit)</li> <li>• RGB565 (16-bit)</li> </ul>	RGB565 (16-bit)	Select the output pixel format for decode operations.
Decode > Output alpha (ARGB8888 only)	Value must be an 8-bit integer (0-255)	255	Specify the alpha value to apply to each output pixel when ARGB8888 format is chosen.
Decode > Callback	Name must be a valid C symbol	NULL	If a callback function is provided it will be called from the interrupt service routine (ISR) each time a related IRQ triggers.
Encode > Horizontal resolution	Value cannot be greater than 65535 and must be a non-negative integer divisible by 16	480	Horizontal resolution of the raw image (in pixels). This value can be configured at runtime via R_JPEG_ImageSizeSet.
Encode > Vertical resolution	Value cannot be greater than 65535 and must be a non-negative integer divisible by 8	272	Vertical resolution of the raw image. This value can be configured at runtime via R_JPEG_ImageSizeSet.
Encode > Horizontal stride	Value cannot be greater than 65535 and must be a non-negative integer	480	Horizontal stride of the raw image buffer (in pixels). This value can be configured at runtime via R_JPEG_ImageSizeSet.
Encode > Input byte order	MCU Specific Options		Select the byte order of the input data for encoding.
Encode > Output byte order	MCU Specific Options		Select the byte order of the output data for encoding.
Encode > Reset interval	Value cannot be greater than 65535 and must be a non-negative integer	512	Set the number of MCUs between RST markers. A value of 0 will disable DRI and RST marker output.

Encode > Quality factor	Value must be between 1 and 100 and must be an integer	50	Set the quality factor for encoding (1-100). Lower values produce smaller images at the cost of image quality.
Encode > Callback	Name must be a valid C symbol	NULL	If a callback function is provided it will be called from the interrupt service routine (ISR) each time a related IRQ triggers.
Interrupts > Decode Process Interrupt Priority	MCU Specific Options		Select the decompression interrupt priority.
Interrupts > Data Transfer Interrupt Priority	MCU Specific Options		Select the data transfer interrupt priority.

## Clock Configuration

The peripheral clock for this module is PCLKA. No clocks are provided by this module.

## Pin Configuration

This module does not have any input or output pin connections.

# Usage Notes

## Overview

The JPEG Codec contains both decode and encode hardware. While these two functions are largely independent in configuration only one can be used at a time.

To switch from decode to encode mode (or vice versa) use [R\\_JPEG\\_ModeSet](#) while the JPEG Codec is idle.

## Status

The status value ([jpeg\\_status\\_t](#)) provided by the callback and by [R\\_JPEG\\_StatusGet](#) is a bitfield that encompasses all potential status indication conditions. One or more statuses can be set simultaneously.

## Decoding Process

JPEG decoding can be performed in several ways depending on the application:

- To perform the simplest decode operation where all dimensions are known:
  - Set the input buffer, stride and output buffer then wait for a callback with status [JPEG\\_STATUS\\_OPERATION\\_COMPLETE](#).
- To pause after decoding the JPEG header (in order to acquire image dimensions and secure an output buffer):
  - Call [R\\_JPEG\\_InputBufferSet](#) before setting the output buffer and wait for a callback with status [JPEG\\_STATUS\\_IMAGE\\_SIZE\\_READY](#).

- To decode a partial JPEG image then pause until the next chunk is available:
  - Specify a size smaller than the full JPEG data when calling `R_JPEG_InputBufferSet`.
- To pause decoding once an output buffer is filled:
  - Specify a size smaller than the full decoded image when calling `R_JPEG_OutputBufferSet`.

The flowchart below illustrates the steps necessary to handle any decode operation. The statuses given in blue are part of `jpeg_status_t` with the `JPEG_DECODE_STATUS` prefix omitted.

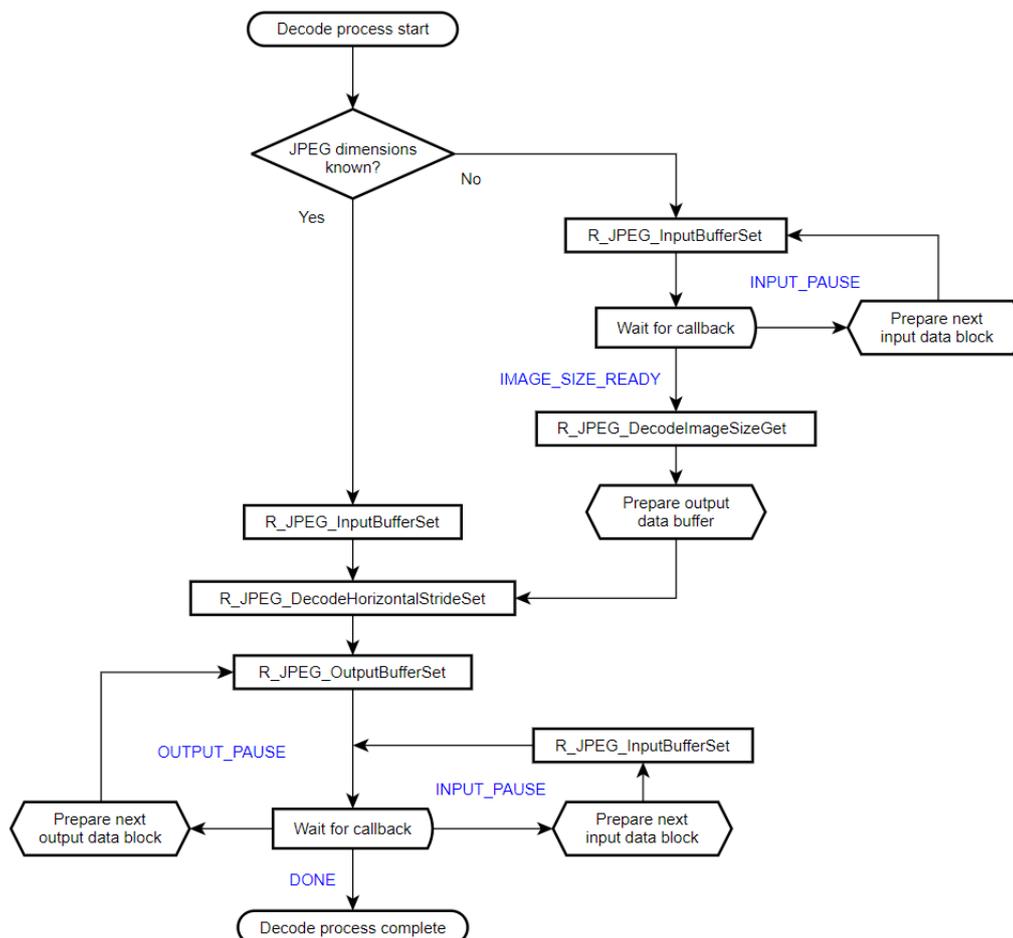


Figure 164: JPEG Decode Operational Flow

## Encoding Process

As compared to decoding, encoding is fairly straightforward. The only option available is to stream input data if desired. The flowchart below details the steps needed to compress an image.

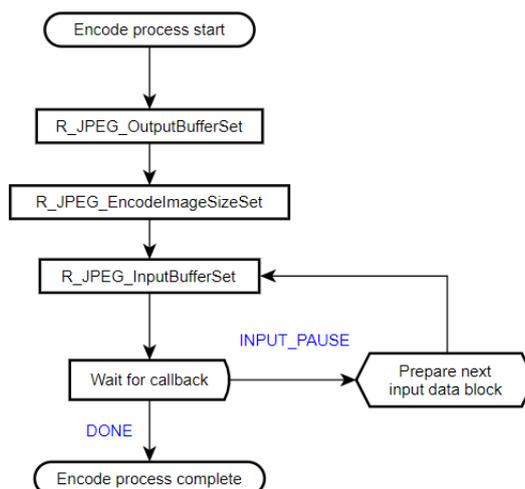


Figure 165: JPEG Encode Operational Flow

## Handling Failed Operations

If an encode or decode operation fails or times out while the codec is running, the peripheral must be reset before it is used again. To reset the JPEG Codec simply close and re-open the module by calling [R\\_JPEG\\_Close](#) followed by [R\\_JPEG\\_Open](#).

## Limitations

Developers should be aware of the following limitations when using the JPEG API.

### Minimum Coded Unit (MCU)

The JPEG Codec can only correctly process images that are an even increment of minimum coded units (MCUs). In other words, depending on the format the width and height of an image to be encoded or decoded must be divisible by the following:

Format	Horizontal	Vertical
Y'CbCr 4:4:4	8 pixels	8 lines
Y'CbCr 4:2:2	16 pixels	8 lines
Y'CbCr 4:1:1	32 pixels	8 lines
Y'CbCr 4:2:0	16 pixels	16 lines

#### Note

*Because encoding is limited to Y'CbCr 4:2:2, raw pixel input data must always be in whole increments of 16x8 pixels.*

## Encoding Input Format

The encoding unit only supports Y'CbCr 4:2:2 input. Raw RGB888 data can be converted to this format as follows:

$$y = (0.299000f * r) + (0.587000f * g) + (0.114000f * b);$$

```
cb = 128 - (0.168736f * r) - (0.331264f * g) + (0.500000f * b);
cr = 128 + (0.500000f * r) - (0.418688f * g) - (0.081312f * b);
```

While these equations are mathematically simple they do use the floating-point unit. To speed things up we can multiply the coefficients by 256 and divide the sum by 256...

```
y = ((76.5440f * r) + (150.272f * g) + (29.1840f * b)) / 256;
cb = 128 - ((43.1964f * r) - (84.8036f * g) + (128.000f * b)) / 256;
cr = 128 + ((128.000f * r) - (107.184f * g) - (20.8159f * b)) / 256;
```

...which allows the formulas to be calculated entirely with shifts and addition (coefficients rounded to the nearest integer):

```
y = ( (r << 6) + (r << 3) + (r << 2) + r
      + (g << 7) + (g << 4) + (g << 2) + (g << 1)
      + (b << 4) + (b << 3) + (b << 2) + b
    ) >> 8;

cb = 128 - ( (r << 5) + (r << 3) + (r << 1) + r
            + (g << 6) + (g << 4) + (g << 2) + g
            - (b << 7)
          ) >> 8;

cr = 128 + ( (r << 7)
            - (g << 6) - (g << 5) - (g << 3) - (g << 1) - g
            - (b << 4) - (b << 2) - b
          ) >> 8;
```

To compose the final Y'CbCr 4:2:2 data the chroma of every two pixels must be averaged. **In addition, the JPEG Codec expects chrominance values to be in the range -127..127 instead of the standard 1..255.**

```
cb = (uint8_t) ((int8_t) ((cb0 + cb1 + 1) >> 1) - 128);
cr = (uint8_t) ((int8_t) ((cr0 + cr1 + 1) >> 1) - 128);
```

Finally, the below equation composes two 4:2:2 output pixels at a time with standard byte order (JPEG\_DATA\_ORDER\_NORMAL):

```
out = y0 + (cb << 8) + (y1 << 16) + (cr << 24);
```

#### Note

RGB565 pixels must be upscaled to RGB888 before using the above formulas. Refer to the below example on *YCbCr Conversion* for implementation details.

## Examples

### Basic Decode Example

This is a basic example showing the minimum code required to initialize the JPEG Codec and decode an image.

```
void jpeg_decode_basic (void)
{
    fsp_err_t err;
    /* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Set input buffer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, JPEG_PTR, JPEG_SIZE_BYTES);
    assert(FSP_SUCCESS == err);
    /* Set horizontal stride of output buffer */
    err = R_JPEG_DecodeHorizontalStrideSet(&g_jpeg_ctrl, JPEG_HSIZE);
    assert(FSP_SUCCESS == err);
    /* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, decode_buffer, sizeof(decode_buffer));
    assert(FSP_SUCCESS == err);
    /* Wait for decode completion */
    jpeg_status_t status = (jpeg_status_t) 0;
    while (!(status & (JPEG_STATUS_OPERATION_COMPLETE | JPEG_STATUS_ERROR)))
    {
        err = R_JPEG_StatusGet(&g_jpeg_ctrl, &status);
        assert(FSP_SUCCESS == err);
    }
}
```

## Streaming Input/Output Example

In this example JPEG data is read in 512-byte chunks. Decoding is paused when a chunk is read and once the JPEG header is decoded. The image is decoded 16 lines at a time.

### Note

*Streaming is always bypassed when a given buffer's size encompasses the entire input or output image, respectively. Though this example decodes via smaller chunks the input and output data are still contiguous for ease of demonstration. Refer to the comments for further insight as to how to implement streaming with different JPEG/output buffer size combinations.*

```
#define JPEG_INPUT_SIZE_BYTES 512U
/* JPEG Codec status */
static volatile jpeg_status_t g_jpeg_status = JPEG_STATUS_NONE;
/* JPEG event flag */
static volatile uint8_t jpeg_event = 0;
/* Callback function for JPEG decode interrupts */
void jpeg_decode_callback (jpeg_callback_args_t * p_args)
{
    /* Get JPEG Codec status */
    g_jpeg_status = p_args->status;
    /* Set JPEG flag */
    jpeg_event = 1;
}
/* Simple wait that returns 1 if no event happened within the timeout period */
static uint8_t jpeg_event_wait (void)
{
    uint32_t timeout_timer = JPEG_EVENT_TIMEOUT;
    while (!jpeg_event && --timeout_timer)
    {
        /* Spin here until an event callback or timeout */
    }
    jpeg_event = 0;
    return timeout_timer ? 0 : 1;
}
/* Decode a JPEG image to a buffer using streaming input and output */
void jpeg_decode_streaming (void)
```

```
{
    uint8_t      * p_jpeg = (uint8_t *) JPEG_PTR;
    jpeg_status_t status = (jpeg_status_t) 0;
    uint8_t      timeout = 0;
    fsp_err_t    err;
    /* Number of input bytes to read at a time */
    uint32_t input_bytes = JPEG_INPUT_SIZE_BYTES;
    /* Open JPEG unit and start decode */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    while (!(status & JPEG_STATUS_ERROR) && !timeout)
    {
        /* Set the input buffer to read `input_bytes` bytes at a time */
        err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_jpeg, input_bytes);
        assert(FSP_SUCCESS == err);
        /* This delay is required for streaming input mode to function correctly.
         * (Without this delay the JPEG Codec will not correctly locate markers in the file
         header.) */
        R_BSP_SoftwareDelay(10, BSP_DELAY_UNITS_MICROSECONDS);
        /* Wait for a callback */
        timeout = jpeg_event_wait();
        /* Get the status from the callback */
        status = g_jpeg_status;
        /* Break if the header has finished decoding */
        if (status & JPEG_STATUS_IMAGE_SIZE_READY)
        {
            break;
        }
        /* Move pointer to next block of input data (if needed) */
        p_jpeg = (uint8_t *) ((uint32_t) p_jpeg + input_bytes);
    }
    /* Get image size */
    uint16_t horizontal;
```

```
uint16_t vertical;
err = R_JPEG_DecodeImageSizeGet(&g_jpeg_ctrl, &horizontal, &vertical);
assert(FSP_SUCCESS == err);
/* Prepare output data buffer here if needed (already allocated in this example) */
uint8_t * p_output = decode_buffer;
/* Set horizontal stride */
err = R_JPEG_DecodeHorizontalStrideSet(&g_jpeg_ctrl, horizontal);
assert(FSP_SUCCESS == err);
/* Calculate the number of bytes that will fit in the buffer (16 lines in this
example) */
uint32_t output_size = horizontal * 16U * 4U;
/* Start decoding by setting the output buffer */
err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, p_output, output_size);
assert(FSP_SUCCESS == err);
while (!(status & JPEG_STATUS_ERROR) && !timeout)
{
/* Wait for a callback */
timeout = jpeg_event_wait();
/* Get the status from the callback */
status = g_jpeg_status;
/* Break if decoding is complete */
if (status & JPEG_STATUS_OPERATION_COMPLETE)
{
break;
}
if (status & JPEG_STATUS_OUTPUT_PAUSE)
{
/* Draw the JPEG work buffer to the framebuffer here (if needed) */
/* Move pointer to next block of output data (if needed) */
p_output += output_size;
/* Set the output buffer to the next 16-line block */
err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, p_output, output_size);
assert(FSP_SUCCESS == err);
}
}
```

```
if (status & JPEG_STATUS_INPUT_PAUSE)
{
/* Get next block of input data */
    p_jpeg = (uint8_t *) ((uint32_t) p_jpeg + input_bytes);
/* Set the new input buffer pointer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_jpeg, input_bytes);
    assert(FSP_SUCCESS == err);
}
}

/* Close driver to allow encode operations if needed */
err = R_JPEG_Close(&g_jpeg_ctrl);
assert(FSP_SUCCESS == err);
}
```

## Encode Example

This is a basic example showing the minimum code required to initialize the JPEG Codec and encode an image.

### Note

*This example assumes image dimensions are provided in the configuration. If this is not the case, [R\\_JPEG\\_EncodeImageSizeSet](#) must be used to set the size before calling [R\\_JPEG\\_InputBufferSet](#).*

```
void jpeg_encode_basic (void)
{
    fsp_err_t err;
/* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
/* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, jpeg_buffer, sizeof(jpeg_buffer));
    assert(FSP_SUCCESS == err);
/* Set input buffer */
    err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, RAW_YCBCR_IMAGE_PTR, IMAGE_SIZE_BYTES);
    assert(FSP_SUCCESS == err);
/* Wait for decode completion */
```

```
jpeg_status_t status = (jpeg_status_t) 0;
while (!(status & JPEG_STATUS_OPERATION_COMPLETE))
{
    err = R_JPEG_StatusGet(&g_jpeg_ctrl, &status);
    assert(FSP_SUCCESS == err);
}
}
```

## Streaming Encode Example

In this example the raw input data is provided in smaller chunks. This can help significantly reduce buffer size and improve throughput when streaming in raw data from an outside source.

```
/* Callback function for JPEG encode interrupts */
void jpeg_encode_callback (jpeg_callback_args_t * p_args)
{
    /* Get JPEG Codec status */
    g_jpeg_status = p_args->status;
    /* Set JPEG flag */
    jpeg_event = 1;
}
void jpeg_encode_streaming (void)
{
    uint8_t timeout = 0;
    uint8_t * p_chunk = (uint8_t *) RAW_YCBCR_IMAGE_PTR;
    fsp_err_t err;
    /* Open JPEG Codec */
    err = R_JPEG_Open(&g_jpeg_ctrl, &g_jpeg_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Set output buffer */
    err = R_JPEG_OutputBufferSet(&g_jpeg_ctrl, jpeg_buffer, sizeof(jpeg_buffer));
    assert(FSP_SUCCESS == err);
    /* Set the image size */
    jpeg_encode_image_size_t image_size;
```

```
image_size.horizontal_resolution    = X_RESOLUTION;
image_size.vertical_resolution      = Y_RESOLUTION;
image_size.horizontal_stride_pixels = H_STRIDE;
err = R_JPEG_EncodeImageSizeSet(&g_jpeg_ctrl, &image_size);
assert(FSP_SUCCESS == err);

/* Calculate the size of the input data chunk (16 lines in this example) */
uint32_t chunk_size = H_STRIDE * 16U * YCBCR_BYTES_PER_PIXEL;

while (!timeout)
{
/* Set the input buffer */
err = R_JPEG_InputBufferSet(&g_jpeg_ctrl, p_chunk, chunk_size);
assert(FSP_SUCCESS == err);

/* Wait for a callback */
timeout = jpeg_event_wait();

if (g_jpeg_status & JPEG_STATUS_OPERATION_COMPLETE)
{
/* Encode complete */
break;
}

if (g_jpeg_status & JPEG_STATUS_INPUT_PAUSE)
{
/* Load next block of input data here (if needed) */
p_chunk += chunk_size;
}
}
}
```

## Y'CbCr Conversion

The below function is provided as a reference for how to convert RGB values to Y'CbCr for use with the JPEG Codec.

### Note

*This function is only partially optimized for clarity. Further application-specific size- or speed-based optimizations should be considered when implementing in an actual project.*

```
#define RGB565_G_MASK 0x07E0
```

```
#define RGB565_B_MASK 0x001F
#define C_0 128
typedef enum e_pixel_format
{
    PIXEL_FORMAT_ARGB8888,
    PIXEL_FORMAT_RGB565
} pixel_format_t;
/* 5-bit to 8-bit LUT */
const uint8_t lut_32[] =
{
    0, 8, 16, 25, 33, 41, 49, 58,
    66, 74, 82, 90, 99, 107, 115, 123,
    132, 140, 148, 156, 165, 173, 181, 189,
    197, 206, 214, 222, 230, 239, 247, 255
};
/* 6-bit to 8-bit LUT */
const uint8_t lut_64[] =
{
    0, 4, 8, 12, 16, 20, 24, 28,
    32, 36, 40, 45, 49, 53, 57, 61,
    65, 69, 73, 77, 81, 85, 89, 93,
    97, 101, 105, 109, 113, 117, 121, 125,
    130, 134, 138, 142, 146, 150, 154, 158,
    162, 166, 170, 174, 178, 182, 186, 190,
    194, 198, 202, 206, 210, 215, 219, 223,
    227, 231, 235, 239, 243, 247, 251, 255
};
void bitmap_rgb2ycbcr(uint32_t * out, uint8_t * in, uint32_t len, pixel_format_t
format);
/*****
*****
* Convert an RGB buffer to Y'CbCr 4:2:2.
*
* NOTE: The width (in pixels) of the image to be converted must be divisible by 2.
```

```
*
* Parameters:
* out Pointer to output buffer
* in Pointer to input buffer
* len Length of input buffer (in pixels)
* format Input buffer format (ARGB8888 or RGB565)
*****
*****/
void bitmap_rgb2ycbcr (uint32_t * out, uint8_t * in, uint32_t len, pixel_format_t
format)
{
    uint16_t in0;
    uint16_t in1;
    uint32_t r0;
    uint32_t g0;
    uint32_t b0;
    uint32_t r1;
    uint32_t g1;
    uint32_t b1;
    uint8_t y0;
    uint8_t y1;
    uint8_t cb0;
    uint8_t cr0;
    uint8_t cb1;
    uint8_t cr1;

    /* Divide length by 2 as we're working with two pixels at a time */
    len >>= 1;

    /* Perform the conversion */
    while (len)
    {
        /* Get R, G and B channel values */
        if (format == PIXEL_FORMAT_RGB565)
        {
            /* Get next two 16-bit values */
```

```
        in0 = *((uint16_t *) in);
        in += 2;
        in1 = *((uint16_t *) in);
        in += 2;

/* Decompose into individual channels */
        r0 = in0 >> 11;
        g0 = (in0 & RGB565_G_MASK) >> 5;
        b0 = in0 & RGB565_B_MASK;
        r1 = in1 >> 11;
        g1 = (in1 & RGB565_G_MASK) >> 5;
        b1 = in1 & RGB565_B_MASK;
    }
else
    {
/* Get each ARGB8888 channel in sequence, skipping alpha */
        b0 = *in++;
        g0 = *in++;
        r0 = *in++;
        in++;
        b1 = *in++;
        g1 = *in++;
        r1 = *in++;
        in++;
    }

/* Convert RGB565 data to RGB888 */
if (PIXEL_FORMAT_RGB565 == format)
    {
        r0 = lut_32[r0];
        g0 = lut_64[g0];
        b0 = lut_32[b0];
        r1 = lut_32[r1];
        g1 = lut_64[g1];
        b1 = lut_32[b1];
    }
}
```

```
/* Calculate Y'CbCr 4:4:4 values for the two pixels */
/* Algorithm based on method shown here: https://sistenix.com/rgb2ycbcr.html */
/* Original coefficients from https://en.wikipedia.org/wiki/YCbCr#JPEG_conversion */
y0 = (uint8_t) (((r0 << 6) + (r0 << 3) + (r0 << 2) + r0 +
                (g0 << 7) + (g0 << 4) + (g0 << 2) + (g0 << 1) +
                (b0 << 4) + (b0 << 3) + (b0 << 2) + b0
                ) >> 8);
cb0 = (uint8_t) (C_0 - (((r0 << 5) + (r0 << 3) + (r0 << 1) + r0 +
                       (g0 << 6) + (g0 << 4) + (g0 << 2) + g0 -
                       (b0 << 7)
                       ) >> 8));
cr0 = (uint8_t) (C_0 + (((r0 << 7) -
                       (g0 << 6) - (g0 << 5) - (g0 << 3) - (g0 << 1) - g0 -
                       (b0 << 4) - (b0 << 2) - b0
                       ) >> 8));
y1 = (uint8_t) (((r1 << 6) + (r1 << 3) + (r1 << 2) + r1 +
                (g1 << 7) + (g1 << 4) + (g1 << 2) + (g1 << 1) +
                (b1 << 4) + (b1 << 3) + (b1 << 2) + b1
                ) >> 8);
cb1 = (uint8_t) (C_0 - (((r1 << 5) + (r1 << 3) + (r1 << 1) + r1 +
                       (g1 << 6) + (g1 << 4) + (g1 << 2) + g1 -
                       (b1 << 7)
                       ) >> 8));
cr1 = (uint8_t) (C_0 + (((r1 << 7) -
                       (g1 << 6) - (g1 << 5) - (g1 << 3) - (g1 << 1) - g1 -
                       (b1 << 4) - (b1 << 2) - b1
                       ) >> 8));

/* The above code is based on the floating point method shown here: */
// y0 = (uint8_t) ((0.299F * (float) r0) + (0.587F * (float) g0) + (0.114F * (float)
b0));
// y1 = (uint8_t) ((0.299F * (float) r1) + (0.587F * (float) g1) + (0.114F * (float)
b1));
// cb0 = (uint8_t) (128.0F - (0.168736F * (float) r0) - (0.331264F * (float) g0) +
(0.5F * (float) b0));
```

```

// cb1 = (uint8_t) (128.0F - (0.168736F * (float) r1) - (0.331264F * (float) g1) +
(0.5F * (float) b1));

// cr0 = (uint8_t) (128.0F + (0.5F * (float) r0) - (0.418688F * (float) g0) -
(0.081312F * (float) b0));

// cr1 = (uint8_t) (128.0F + (0.5F * (float) r1) - (0.418688F * (float) g1) -
(0.081312F * (float) b1));

/* NOTE: The JPEG Codec expects signed instead of unsigned chrominance values. */
/* Convert chrominance to -127..127 instead of 1..255 */

    cb0 = (uint8_t) ((int8_t) ((cb0 + cb1 + 1) >> 1) - C_0);
    cr0 = (uint8_t) ((int8_t) ((cr0 + cr1 + 1) >> 1) - C_0);

/* Convert the two 4:4:4 values into 4:2:2 by averaging the chroma, then write to
output */

    *out++ = (uint32_t) (y0 + (cb0 << 8) + (y1 << 16) + (cr0 << 24));
    len--;
}
}

```

## Data Structures

struct [jpeg\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ jpeg\_instance\_ctrl\_t

struct jpeg_instance_ctrl_t		
JPEG Codec module control block. DO NOT INITIALIZE. Initialization occurs when jpeg_api_t::open is called.		
Data Fields		
uint32_t	open	JPEG Codec driver status.
<a href="#">jpeg_status_t</a>	status	JPEG Codec operational status.
<a href="#">fsp_err_t</a>	error_code	JPEG Codec error code (if any).
jpeg_mode_t	mode	Current mode (decode or encode).
uint32_t	horizontal_stride_bytes	Horizontal Stride settings.
uint32_t	output_buffer_size	Output buffer size.
<a href="#">jpeg_cfg_t</a> const *	p_cfg	JPEG Decode configuration struct.
void const *	p_extend	JPEG Codec hardware

		dependent configuration */.
<a href="#">jpeg_decode_pixel_format_t</a>	pixel_format	Pixel format.
uint16_t	total_lines_decoded	Track the number of lines decoded so far.
<a href="#">jpeg_decode_subsample_t</a>	horizontal_subsample	Horizontal sub-sample setting.
uint16_t	lines_to_encode	Number of lines to encode.
uint16_t	vertical_resolution	vertical size
uint16_t	total_lines_encoded	Number of lines encoded.

## Function Documentation

### ◆ R\_JPEG\_Open()

```
fsp_err_t R_JPEG_Open ( jpeg_ctrl_t *const p_api_ctrl, jpeg_cfg_t const *const p_cfg )
```

Initialize the JPEG Codec module.

#### Note

*This function configures the JPEG Codec for operation and sets up the registers for data format and pixel format based on user-supplied configuration parameters. Interrupts are enabled to support callbacks.*

#### Return values

FSP_SUCCESS	JPEG Codec module is properly configured and is ready to take input data.
FSP_ERR_ALREADY_OPEN	JPEG Codec is already open.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_IRQ_BSP_DISABLED	JEDI interrupt does not have an IRQ number.
FSP_ERR_INVALID_ARGUMENT	(Encode only) Quality factor, horizontal resolution and/or vertical resolution are invalid.
FSP_ERR_INVALID_ALIGNMENT	(Encode only) The horizontal resolution (at 16bpp) is not divisible by 8 bytes.

## ◆ R\_JPEG\_OutputBufferSet()

```
fsp_err_t R_JPEG_OutputBufferSet ( jpeg_ctrl_t * p_api_ctrl, void * p_output_buffer, uint32_t
output_buffer_size )
```

Assign a buffer to the JPEG Codec for storing output data.

### Note

*In Decode mode, the number of image lines to be decoded depends on the size of the buffer and the horizontal stride settings. Once the output buffer size is known, the horizontal stride value is known, and the input pixel format is known (the input pixel format is obtained by the JPEG decoder from the JPEG headers), the driver automatically computes the number of lines that can be decoded into the output buffer. After these lines are decoded, the JPEG engine pauses and a callback function is triggered, so the application is able to provide the next buffer for the JPEG module to resume the operation.*

The JPEG decoding operation automatically starts after both the input buffer and the output buffer are set and the output buffer is big enough to hold at least eight lines of decoded image data.

### Return values

FSP_SUCCESS	The output buffer is properly assigned to JPEG codec device.
FSP_ERR_ASSERTION	Pointer to the control block or output_buffer is NULL or output_buffer_size is 0.
FSP_ERR_INVALID_ALIGNMENT	Buffer starting address is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_JPEG_UNSUPPORTED_IMAGE_SIZE	The number of horizontal pixels exceeds horizontal memory stride.
FSP_ERR_JPEG_BUFFERSIZE_NOT_ENOUGH	Invalid buffer size.
FSP_ERR_IN_USE	The output buffer cannot be changed during codec operation.

## ◆ R\_JPEG\_InputBufferSet()

```
fsp_err_t R_JPEG_InputBufferSet ( jpeg_ctrl_t *const p_api_ctrl, void * p_data_buffer, uint32_t data_buffer_size )
```

Assign an input data buffer to the JPEG codec for processing.

### Note

After the amount of data is processed, the JPEG driver triggers a callback function with the flag `JPEG_PRV_OPERATION_INPUT_PAUSE` set. The application supplies the next chunk of data to the driver so processing can resume.

The JPEG decoding operation automatically starts after both the input buffer and the output buffer are set, and the output buffer is big enough to hold at least one line of decoded image data.

If zero is provided for the decode data buffer size the JPEG Codec will never pause for more input data and will continue to read until either an image has been fully decoded or an error condition occurs.

### Note

When encoding images the minimum data buffer size is 8 lines by 16 Y'CbCr 4:2:2 pixels (256 bytes). This corresponds to one minimum coded unit (MCU) of the resulting JPEG output.

### Return values

FSP_SUCCESS	The input data buffer is properly assigned to JPEG Codec device.
FSP_ERR_ASSERTION	Pointer to the control block is NULL, or the pointer to the input_buffer is NULL, or the input_buffer_size is 0.
FSP_ERR_INVALID_ALIGNMENT	Buffer starting address is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_IN_USE	The input buffer cannot be changed while the codec is running.
FSP_ERR_INVALID_CALL	In encode mode the output buffer must be set first.
FSP_ERR_JPEG_IMAGE_SIZE_ERROR	The buffer size is smaller than the minimum coded unit (MCU).

◆ **R\_JPEG\_StatusGet()**

```
fsp_err_t R_JPEG_StatusGet ( jpeg_ctrl_t* p_api_ctrl, jpeg_status_t* p_status )
```

Get the status of the JPEG codec. This function can also be used to poll the device.

**Return values**

FSP_SUCCESS	The status information is successfully retrieved.
FSP_ERR_ASSERTION	Pointer to the control block or p_status is NULL.
FSP_ERR_NOT_OPEN	JPEG is not opened.

◆ **R\_JPEG\_Close()**

```
fsp_err_t R_JPEG_Close ( jpeg_ctrl_t* p_api_ctrl)
```

Cancel an outstanding JPEG codec operation and close the device.

**Return values**

FSP_SUCCESS	The JPEG unit is stopped and the driver is closed.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.

## ◆ R\_JPEG\_EncodeImageSizeSet()

```
fsp_err_t R_JPEG_EncodeImageSizeSet ( jpeg_ctrl_t *const p_api_ctrl, jpeg_encode_image_size_t *
p_image_size )
```

Set the image dimensions for an encode operation.

**Note**

*Image dimensions must be set before setting the input buffer.*

**Return values**

FSP_SUCCESS	Image size was successfully written to the JPEG Codec.
FSP_ERR_ASSERTION	Pointer to the control block or p_image_size is NULL.
FSP_ERR_INVALID_ALIGNMENT	Horizontal stride is not 8-byte aligned.
FSP_ERR_INVALID_ARGUMENT	Horizontal or vertical resolution is invalid or zero.
FSP_ERR_NOT_OPEN	JPEG not opened.
FSP_ERR_IN_USE	Image parameters cannot be changed while the codec is running.

## ◆ R\_JPEG\_DecodeLinesDecodedGet()

```
fsp_err_t R_JPEG_DecodeLinesDecodedGet ( jpeg_ctrl_t * p_api_ctrl, uint32_t * p_lines )
```

Returns the number of lines decoded into the output buffer.

**Note**

*Use this function to retrieve the number of image lines written to the output buffer after a partial decode operation. Combined with the horizontal stride settings and the output pixel format the application can compute the amount of data to read from the output buffer.*

**Return values**

FSP_SUCCESS	Line count successfully returned.
FSP_ERR_ASSERTION	Pointer to the control block or p_lines is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.

### ◆ R\_JPEG\_DeCodeHorizontalStrideSet()

```
fsp_err_t R_JPEG_DeCodeHorizontalStrideSet ( jpeg_ctrl_t * p_api_ctrl, uint32_t horizontal_stride )
```

Configure horizontal stride setting for decode operations.

#### Note

*If the image size is known prior to the open call and/or the output buffer stride is constant, pass the horizontal stride value in the `jpeg_cfg_t` structure. Otherwise, after the image size becomes available use this function to set the output buffer horizontal stride value.*

#### Return values

FSP_SUCCESS	Horizontal stride value is properly configured.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_INVALID_ALIGNMENT	Horizontal stride is zero or is not 8-byte aligned.
FSP_ERR_NOT_OPEN	JPEG not opened.

### ◆ R\_JPEG\_DeCodeImageSizeGet()

```
fsp_err_t R_JPEG_DeCodeImageSizeGet ( jpeg_ctrl_t * p_api_ctrl, uint16_t * p_horizontal_size, uint16_t * p_vertical_size )
```

Obtain the size of an image being decoded.

#### Return values

FSP_SUCCESS	The image size is available and the horizontal and vertical values are stored in the memory pointed to by <code>p_horizontal_size</code> and <code>p_vertical_size</code> .
FSP_ERR_ASSERTION	Pointer to the control block is NULL and/or size is not ready.
FSP_ERR_NOT_OPEN	JPEG is not opened.

## ◆ R\_JPEG\_DecodeImageSubsampleSet()

```
fsp_err_t R_JPEG_DecodeImageSubsampleSet ( jpeg_ctrl_t *const p_api_ctrl,
jpeg_decode_subsample_t horizontal_subsample, jpeg_decode_subsample_t vertical_subsample )
```

Configure horizontal and vertical subsampling.

**Note**

*This function can be used to scale the output of decoded image data.*

**Return values**

FSP_SUCCESS	Horizontal subsample value is properly configured.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG not opened.

## ◆ R\_JPEG\_DecodePixelFormatGet()

```
fsp_err_t R_JPEG_DecodePixelFormatGet ( jpeg_ctrl_t * p_api_ctrl, jpeg_color_space_t *
p_color_space )
```

Get the color format of the JPEG being decoded.

**Return values**

FSP_SUCCESS	The color format was successfully retrieved.
FSP_ERR_ASSERTION	Pointer to the control block is NULL.
FSP_ERR_NOT_OPEN	JPEG is not opened.

**◆ R\_JPEG\_ModeSet()**

```
fsp_err_t R_JPEG_ModeSet ( jpeg_ctrl_t *const p_api_ctrl, jpeg_mode_t mode )
```

Switch between encode and decode mode (or vice-versa).

**Note**

*The codec must not be idle in order to switch modes.*

**Return values**

FSP_SUCCESS	Mode changed successfully.
FSP_ERR_ASSERTION	p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_IN_USE	JPEG Codec is currently in use.
FSP_ERR_INVALID_ARGUMENT	(Encode only) Quality factor, horizontal resolution and/or vertical resolution are invalid.
FSP_ERR_INVALID_ALIGNMENT	(Encode only) The horizontal resolution (at 16bpp) is not divisible by 8 bytes.

**4.2.33 Key Interrupt (r\_kint)**

## Modules

**Functions**

```
fsp_err_t R_KINT_Open (keymatrix_ctrl_t *const p_api_ctrl, keymatrix_cfg_t
const *const p_cfg)
```

```
fsp_err_t R_KINT_Enable (keymatrix_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_KINT_Disable (keymatrix_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_KINT_Close (keymatrix_ctrl_t *const p_api_ctrl)
```

**Detailed Description**

Driver for the KINT peripheral on RA MCUs. This module implements the [Key Matrix Interface](#).

**Overview**

The KINT module configures the Key Interrupt (KINT) peripheral to detect rising or falling edges on any of the KINT channels. When such an event is detected on any of the configured pins, the module generates an interrupt.

## Features

- Detect rising or falling edges on KINT channels
- Callback for notifying the application when edges are detected on the configured channels

## Configuration

### Build Time Configurations for r\_kint

The following build time configurations are defined in fsp\_cfg/r\_kint\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Input > Key Matrix Driver on r\_kint

This module can be added to the Stacks tab via New Stack > Driver > Input > Key Matrix Driver on r\_kint.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_kint0	Module name.
Input > Key Interrupt Flag Mask	<ul style="list-style-type: none"> <li>• Channel 0</li> <li>• Channel 1</li> <li>• Channel 2</li> <li>• Channel 3</li> <li>• Channel 4</li> <li>• Channel 5</li> <li>• Channel 6</li> <li>• Channel 7</li> </ul>		Select channels to enable.
Interrupts > Trigger Type	<ul style="list-style-type: none"> <li>• Falling Edge</li> <li>• Rising Edge</li> </ul>	Rising Edge	Specifies if the enabled channels detect a rising edge or a falling edge. NOTE: either all channels detecting a rising edge or all channels detecting a falling edge.
Interrupts > Callback	Name must be a valid C symbol	kint_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR) each time the IRQ triggers.

Interrupts > Key  
Interrupt Priority

MCU Specific Options

Select the key interrupt  
priority.

## Clock Configuration

The KINT peripheral runs on PCLKB.

## Pin Configuration

The KRn pins are key switch matrix row input pins.

# Usage Notes

## Connecting a Switch Matrix

The KINT module is designed to scan the rows of a switch matrix where each row is connected to a number of columns through switches. A periodic timer (or other mechanism) sets one column pin high at a time. Any switches that are pressed on the driven column cause a rising (or falling) edge on the row pin (KRn) causing an interrupt.

### Note

*In applications where multiple keys may be pressed at the same time it is recommended to put a diode inline with each switch to prevent ghosting.*

## Handling Multiple Pins

When an edge is detected on multiple pins at the same time, a single IRQ will be generated. A mask of all the pins that detected an edge will be passed to the callback.

# Examples

## Basic Example

This is a basic example of minimal use of the KINT in an application.

```
static volatile uint32_t g_channel_mask;
static volatile uint32_t g_kint_edge_detected = 0U;
/* Called from key_int_isr */
void r_kint_callback (keymatrix_callback_args_t * p_args)
{
    g_channel_mask      = p_args->channel_mask;
    g_kint_edge_detected = 1U;
}
void r_kint_example ()
{
    /* Configure the KINT. */
    fsp_err_t err = R_KINT_Open(&g_kint_ctrl, &g_kint_cfg);
```

```

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Enable the KINT. */
err = R_KINT_Enable(&g_kint_ctrl);
assert(FSP_SUCCESS == err);

while (0 == g_kint_edge_detected)
{
/* Wait for interrupt. */
}
}

```

## Data Structures

struct [kint\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ kint\_instance\_ctrl\_t

struct kint\_instance\_ctrl\_t

Channel instance control block. DO NOT INITIALIZE. Initialization occurs when [keymatrix\\_api\\_t::open](#) is called.

## Function Documentation

### ◆ R\_KINT\_Open()

[fsp\\_err\\_t](#) R\_KINT\_Open ( [keymatrix\\_ctrl\\_t](#)\*const p\_api\_ctrl, [keymatrix\\_cfg\\_t](#) const\*const p\_cfg )

Configure all the Key Input (KINT) channels and provides a handle for use with the rest of the KINT API functions. Implements [keymatrix\\_api\\_t::open](#).

#### Return values

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	One of the following parameters may be NULL: p_cfg, or p_ctrl or the callback.
FSP_ERR_ALREADY_OPEN	The module has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel mask is invalid.

◆ **R\_KINT\_Enable()**

`fsp_err_t R_KINT_Enable ( keymatrix_ctrl_t *const p_api_ctrl)`

This function enables interrupts for the KINT peripheral after clearing any pending requests. Implements `keymatrix_api_t::enable`.

**Return values**

FSP_SUCCESS	Interrupt enabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The peripheral is not opened.

◆ **R\_KINT\_Disable()**

`fsp_err_t R_KINT_Disable ( keymatrix_ctrl_t *const p_api_ctrl)`

This function disables interrupts for the KINT peripheral. Implements `keymatrix_api_t::disable`.

**Return values**

FSP_SUCCESS	Interrupt disabled successfully.
FSP_ERR_ASSERTION	The p_ctrl parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_KINT\_Close()**

`fsp_err_t R_KINT_Close ( keymatrix_ctrl_t *const p_api_ctrl)`

Clear the KINT configuration and disable the KINT IRQ. Implements `keymatrix_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	The module is not opened.

**4.2.34 Low Power Modes (r\_lpm)**

## Modules

## Functions

`fsp_err_t` `R_LPM_Open` (`lpm_ctrl_t *const p_api_ctrl`, `lpm_cfg_t const *const p_cfg`)

`fsp_err_t` `R_LPM_Close` (`lpm_ctrl_t *const p_api_ctrl`)

`fsp_err_t` `R_LPM_LowPowerReconfigure` (`lpm_ctrl_t *const p_api_ctrl`, `lpm_cfg_t const *const p_cfg`)

`fsp_err_t` `R_LPM_LowPowerModeEnter` (`lpm_ctrl_t *const p_api_ctrl`)

`fsp_err_t` `R_LPM_IoKeepClear` (`lpm_ctrl_t *const p_api_ctrl`)

## Detailed Description

Driver for the LPM peripheral on RA MCUs. This module implements the [Low Power Modes Interface](#).

## Overview

The low power modes driver is used to configure and place the device into the desired low power mode. Various sources can be configured to wake from standby, request snooze mode, end snooze mode or end deep standby mode.

## Features

The LPM HAL module has the following key features:

- Supports the following low power modes:
  - Deep Software Standby mode (On supported MCUs)
  - Software Standby mode
  - Sleep mode
  - Snooze mode
- Supports reducing power consumption when in deep software standby mode through internal power supply control and by resetting the states of I/O ports.
- Supports disabling and enabling the MCU's other hardware peripherals

## Configuration

### Build Time Configurations for r\_lpm

The following build time configurations are defined in `fsp_cfg/r_lpm_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Power > Low Power Modes Driver on r\_lpm

This module can be added to the Stacks tab via New Stack > Driver > Power > Low Power Modes Driver on r\_lpm. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_lpm0	Module name.
General > Low Power Mode	MCU Specific Options		Power mode to be entered.
General > Output port state in standby and deep standby	MCU Specific Options		Select the state of output pins during standby. Applies to address output, data output, and other bus control output pins.
Standby Options > Wake Sources	MCU Specific Options		Enable wake from standby from these Sources.
Standby Options > Snooze Request Source	MCU Specific Options		Select the event that will enter snooze.
Standby Options > Snooze End Sources	MCU Specific Options		Enable wake from snooze from these sources.
Standby Options > DTC state in Snooze Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable wake from snooze from this source.
Standby Options > Snooze Cancel Source	MCU Specific Options		Select an interrupt source to cancel snooze.
Deep Standby Options > I/O Port Retention	MCU Specific Options		Select the state of the IO Pins after exiting deep standby mode.
Deep Standby Options > Power-Supply Control	MCU Specific Options		Select the state of the internal power supply in deep standby mode.
Deep Standby Options > Cancel Sources	MCU Specific Options		Enable wake from deep standby using these sources.
Deep Standby Options > Cancel Edges	MCU Specific Options		Falling edge trigger is default. Select sources to enable wake from deep standby with rising edge.

## Clock Configuration

This module does not have any selectable clock sources.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Sleep Mode

At power on, by default sleep is set as the low-power mode. Sleep mode is the most convenient low-power mode available, as it does not require any special configuration (other than configuring and enabling a suitable interrupt or event to wake the MCU from sleep) to return to normal program-execution mode. The states of the SRAM, the processor registers, and the hardware peripherals are all maintained in sleep mode, and the time needed to enter and wake from sleep is minimal. Any interrupt causes the MCU device to wake from sleep mode, including the SysTick interrupt used by the RTOS scheduler.

## Software Standby Mode

In software-standby mode, the CPU, as well as most of the on-chip peripheral functions and all of the internal oscillators, are stopped. The contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions, and I/O Ports are all retained. Software-standby mode allows significant reduction in power consumption, because most of the oscillators are stopped in this mode. Like sleep mode, standby mode requires an interrupt or event be configured and enabled to wake up.

## Snooze Mode

Snooze mode can be used with some MCU peripherals to execute basic tasks while keeping the MCU in a low-power state. Many core peripherals and all clocks can be selected to run during Snooze, allowing for more flexible low-power configuration than Software Standby mode. To enable Snooze, select "Software Standby mode with Snooze mode enabled" for the "Low Power Mode" configuration option. Snooze mode settings (including entry/exit sources) are available under "Standby Options".

## Deep Software Standby Mode

Deep Software Standby Mode is only available on some MCU devices. The MCU always wakes from Deep Software Standby Mode by going through reset, either by the negation of the reset pin or by one of the wakeup sources configurable in the "Deep Standby Options" configuration group.

The Reset Status Registers can be used to determine if the reset occurred after coming out of deep software standby. For example, R\_SYSTEM->RSTSR0\_b.DPSRSTF is set to 1 after a deep software standby reset.

I/O Port Retention can be enabled to maintain I/O port configuration across a deep software standby reset. Retention can be cancelled through the [R\\_LPM\\_IoKeepClear](#) API.

## Limitations

Developers should be aware of the following limitations when using the LPM:

- Flash stop (code flash disable) is not supported. See the section "Flash Operation Control Register (FLSTOP)" of the RA2/RA4 Family Hardware User's Manual.

- Reduced SRAM retention area in software standby mode is not supported. See the section "Power Save Memory Control Register (PSMCR)" of the RA4 Hardware User's Manual.
- Only one Snooze Request Source can be used at a time.
- When using Snooze mode with SCI0 RXD as the snooze source the system clock must be HOCO and the MOCO, Main Oscillator and PLL clocks must be turned off.
- If the main oscillator or PLL with main oscillator source is used for the system clock, the wake time from standby mode can be affected by the Main Oscillator Wait Time Setting in the MOSCWTCR register. This register setting is available to be changed through the Main Oscillator Wait Time setting in the CGC module properties. See the "Wakeup Timing and Duration" table in Electrical Characteristics for more information.
- When using the DC-DC regulator (where available), the MCU will temporarily switch to the LDO if Software Standby or Snooze is requested and back again when it is cancelled. Switching to the LDO incurs a 60 microsecond critical section wherein all interrupts AND peripherals are stopped. Switching back to DCDC from the LDO incurs an additional 22 microsecond critical section (peripherals running).

## Examples

### LPM Sleep Example

This is a basic example of minimal use of the LPM in an application. The LPM instance is opened and the configured low-power mode is entered.

```
void r_lpm_sleep (void)
{
    fsp_err_t err = R_LPM_Open(&g_lpm_ctrl, &g_lpm_cfg_sleep);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    err = R_LPM_LowPowerModeEnter(&g_lpm_ctrl);
    assert(FSP_SUCCESS == err);
}
```

### LPM Deep Software Standby Example

```
void r_lpm_deep_software_standby (void)
{
    fsp_err_t err;
    err = R_LPM_Open(&g_lpm_ctrl, &g_lpm_cfg_deep_software_standby);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Check the Deep Software Standby Reset Flag. */
    if (1U == R_SYSTEM->RSTSR0_b.DPSRSTF)
    {
```

```
/* Clear the IOKEEP bit to allow I/O Port use. */
    err = R_LPM_IoKeepClear(&g_lpm_ctrl);
    assert(FSP_SUCCESS == err);
}
/* Add user code here. */
/* Reconfigure the module to set the IOKEEP bit before entering deep software
standby. */
    err = R_LPM_LowPowerReconfigure(&g_lpm_ctrl, &g_lpm_cfg_deep_software_standby);
    assert(FSP_SUCCESS == err);
    err = R_LPM_LowPowerModeEnter(&g_lpm_ctrl);
/* Code after R_LPM_LowPowerModeEnter when using Deep Software Standby never be
executed.
* Deep software standby exits by resetting the MCU. */
    assert(FSP_SUCCESS == err);
}
```

## Data Structures

struct [lpm\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ lpm\_instance\_ctrl\_t

struct [lpm\\_instance\\_ctrl\\_t](#)

LPM private control block. DO NOT MODIFY. Initialization occurs when [R\\_LPM\\_Open\(\)](#) is called.

## Function Documentation

◆ **R\_LPM\_Open()**

```
fsp_err_t R_LPM_Open ( lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg )
```

Perform any necessary initialization

**Return values**

FSP_SUCCESS	LPM instance opened
FSP_ERR_ASSERTION	Null Pointer
FSP_ERR_ALREADY_OPEN	LPM instance is already open
FSP_ERR_UNSUPPORTED	This MCU does not support Deep Software Standby
FSP_ERR_INVALID_ARGUMENT	One of the following: <ul style="list-style-type: none"> <li>• Invalid snooze entry source</li> <li>• Invalid snooze end sources</li> </ul>
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>• Invalid low power mode</li> <li>• Invalid DTC option for snooze mode</li> <li>• Invalid deep standby end sources</li> <li>• Invalid deep standby end sources edges</li> <li>• Invalid power supply option for deep standby</li> <li>• Invalid IO port option for deep standby</li> <li>• Invalid output port state setting for standby or deep standby</li> <li>• Invalid sources for wake from standby mode</li> <li>• Invalid power supply option for standby</li> <li>• Invalid IO port option for standby</li> <li>• Invalid standby end sources</li> <li>• Invalid standby end sources edges</li> </ul>

**◆ R\_LPM\_Close()**`fsp_err_t R_LPM_Close ( lpm_ctrl_t *const p_api_ctrl)`

Close the LPM Instance

**Return values**

FSP_SUCCESS	LPM driver closed
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_ASSERTION	Null Pointer

### ◆ R\_LPM\_LowPowerReconfigure()

```
fsp_err_t R_LPM_LowPowerReconfigure ( lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg )
```

Configure a low power mode

NOTE: This function does not enter the low power mode, it only configures parameters of the mode. Execution of the WFI instruction is what causes the low power mode to be entered.

#### Return values

FSP_SUCCESS	Low power mode successfully applied
FSP_ERR_ASSERTION	Null Pointer
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_UNSUPPORTED	This MCU does not support Deep Software Standby
FSP_ERR_INVALID_ARGUMENT	One of the following: <ul style="list-style-type: none"> <li>• Invalid snooze entry source</li> <li>• Invalid snooze end sources</li> </ul>
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>• Invalid low power mode</li> <li>• Invalid DTC option for snooze mode</li> <li>• Invalid deep standby end sources</li> <li>• Invalid deep standby end sources edges</li> <li>• Invalid power supply option for deep standby</li> <li>• Invalid IO port option for deep standby</li> <li>• Invalid output port state setting for standby or deep standby</li> <li>• Invalid sources for wake from standby mode</li> <li>• Invalid power supply option for standby</li> <li>• Invalid IO port option for standby</li> <li>• Invalid standby end sources</li> <li>• Invalid standby end sources edges</li> </ul>

◆ **R\_LPM\_LowPowerModeEnter()**

```
fsp_err_t R_LPM_LowPowerModeEnter ( lpm_ctrl_t *const p_api_ctrl)
```

Enter low power mode (sleep/standby/deep standby) using WFI macro.

Function will return after waking from low power mode.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	LPM instance is not open
FSP_ERR_INVALID_MODE	One of the following: <ul style="list-style-type: none"> <li>• HOCO was not system clock when using snooze mode with SCIO/RXD0.</li> <li>• HOCO was not stable when using snooze mode with SCIO/RXD0.</li> <li>• MOCO was running when using snooze mode with SCIO/RXD0.</li> <li>• MAIN OSCILLATOR was running when using snooze mode with SCIO/RXD0.</li> <li>• PLL was running when using snooze mode with SCIO/RXD0.</li> <li>• Unable to disable oscillator stop detect when using standby or deep standby.</li> </ul>

◆ **R\_LPM\_IoKeepClear()**

```
fsp_err_t R_LPM_IoKeepClear ( lpm_ctrl_t *const p_api_ctrl)
```

Clear the IOKEEP bit after deep software standby

**Return values**

FSP_SUCCESS	DPSBYCR_b.IOKEEP bit cleared Successfully.
FSP_ERR_UNSUPPORTED	Deep standby mode not supported on this MCU.

**4.2.35 Low Voltage Detection (r\_lvd)**

## Modules

## Functions

`fsp_err_t` `R_LVD_Open` (`lvd_ctrl_t *const p_api_ctrl`, `lvd_cfg_t const *const p_cfg`)

`fsp_err_t` `R_LVD_Close` (`lvd_ctrl_t *const p_api_ctrl`)

`fsp_err_t` `R_LVD_StatusGet` (`lvd_ctrl_t *const p_api_ctrl`, `lvd_status_t *p_lvd_status`)

`fsp_err_t` `R_LVD_StatusClear` (`lvd_ctrl_t *const p_api_ctrl`)

`fsp_err_t` `R_LVD_CallbackSet` (`lvd_ctrl_t *const p_api_ctrl`, `void(*p_callback)(lvd_callback_args_t*)`, `void const *const p_context`, `lvd_callback_args_t *const p_callback_memory`)

## Detailed Description

Driver for the LVD peripheral on RA MCUs. This module implements the [Low Voltage Detection Interface](#).

## Overview

The Low Voltage Detection module configures the voltage monitors to detect when  $V_{CC}$  crosses a specified threshold.

## Features

The LVD HAL module supports the following functions:

- Two run-time configurable voltage monitors (Voltage Monitor 1, Voltage Monitor 2)
  - Configurable voltage threshold
  - Digital filter (Available on specific MCUs)
  - Support for both interrupt or polling
    - NMI or maskable interrupt can be configured
  - Rising, falling, or both edge event detection
  - Support for resetting the MCU when  $V_{CC}$  falls below configured threshold.

## Configuration

### Build Time Configurations for r\_lvd

The following build time configurations are defined in `fsp_cfg/r_lvd_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Power > Low Voltage Detection Driver on r\_lvd

This module can be added to the Stacks tab via New Stack > Driver > Power > Low Voltage Detection Driver on r\_lvd. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_lvd	Module name.
Monitor Number	MCU Specific Options		Select the LVD monitor.
Digital Filter	MCU Specific Options		Enable the digital filter and select the digital filter clock divider.
Voltage Threshold	MCU Specific Options		Select the low voltage detection threshold.
Detection Response	<ul style="list-style-type: none"> <li>Maskable interrupt</li> <li>Non-maskable interrupt</li> <li>Reset MCU (Only available for falling edge)</li> <li>No response (Voltage monitor status will be polled)</li> </ul>	No response (Voltage monitor status will be polled)	Select what happens when the voltage crosses the threshold voltage.
Voltage Slope	<ul style="list-style-type: none"> <li>Falling voltage</li> <li>Rising voltage</li> <li>Rising or falling voltage</li> </ul>	Falling voltage	Select detection on rising voltage, falling voltage or both.
Negation Delay	<ul style="list-style-type: none"> <li>Delay from reset</li> <li>Delay from voltage returning to normal range</li> </ul>	Delay from reset	Negation of the monitor signal can either be delayed from the reset event or from voltage returning to normal range.
Monitor Interrupt Callback	Name must be a valid C symbol.	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR) each time the IRQ triggers.
LVD Monitor Interrupt Priority	MCU Specific Options		Select the LVD Monitor interrupt priority.

### Clock Configuration

The LOCO clock must be enabled in order to use the digital filter.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Startup Edge Detection

If  $V_{CC}$  is below the threshold prior to configuring the voltage monitor for falling edge detection, the monitor will immediately detect the a falling edge condition. If  $V_{CC}$  is above the threshold prior to configuring the monitor for rising edge detection, the monitor will not detect a rising edge condition until  $V_{CC}$  falls below the threshold and then rises above it again.

## Voltage Monitor 0

The LVD HAL module only supports configuring voltage monitor 1 and voltage monitor 2. Voltage monitor 0 can be configured by setting the appropriate bits in the OFS1 register. This means that voltage monitor 0 settings cannot be changed at runtime.

Voltage monitor 0 supports the following features

- Configurable Voltage Threshold ( $V_{DET0}$ )
- Reset the device when  $V_{CC}$  falls below  $V_{DET0}$

## Limitations

- The digital filter must be disabled when using voltage monitors in Software Standby or Deep Software Standby.
- Deep Software Standby mode is not possible if the voltage monitor is configured to reset the MCU.
- When the detection response is set to reset, only voltage falling edge detection is possible.

# Examples

## Basic Example

This is a basic example of minimal use of the LVD in an application.

```
void basic_example (void)
{
    fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
    assert(FSP_SUCCESS == err);
    while (1)
    {
        lvd_status_t status;
        err = R_LVD_StatusGet(&g_lvd_ctrl, &status);
    }
}
```

```
    assert(FSP_SUCCESS == err);
if (LVD_THRESHOLD_CROSSING_DETECTED == status.crossing_detected)
    {
        err = R_LVD_StatusClear(&g_lvd_ctrl);
        assert(FSP_SUCCESS == err);
    /* Do something */
    }
}
```

## Interrupt Example

This is a basic example of using a LVD instance that is configured to generate an interrupt.

```
void interrupt_example (void)
{
    fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    while (1)
    {
        /* Application Process */
        /* Application will be interrupted when Vcc crosses the configured threshold. */
    }
}
/* Called when Vcc crosses configured threshold. */
void lvd_callback (lvd_callback_args_t * p_args)
{
    if (LVD_CURRENT_STATE_BELOW_THRESHOLD == p_args->current_state)
    {
        /* Do Something */
    }
}
```

## Reset Example

This is a basic example of using a LVD instance that is configured to reset the MCU.

```
void reset_example (void)
{
    if (1U == R_SYSTEM->RSTSR0_b.LVD1RF)
    {
        /* The system is coming out of reset because Vcc crossed configured voltage
        threshold. */
        /* Clear Voltage Monitor 1 Reset Detect Flag. */
        R_SYSTEM->RSTSR0_b.LVD1RF = 0;
    }
    fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    while (1)
    {
        /* Application Process */
        /* Application will reset when Vcc crosses the configured threshold. */
    }
}
```

## Data Structures

struct [lvd\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [lvd\\_instance\\_ctrl\\_t](#)

struct [lvd\\_instance\\_ctrl\\_t](#)

LVD instance control structure

## Function Documentation

◆ **R\_LVD\_Open()**

```
fsp_err_t R_LVD_Open ( lvd_ctrl_t *const p_api_ctrl, lvd_cfg_t const *const p_cfg )
```

Initializes a voltage monitor and detector according to the passed-in configuration structure.

**Parameters**

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
[in]	p_cfg	Pointer to the configuration structure for the driver instance

**Note**

*Digital filter is not to be used with standby modes.*

*Startup time can take on the order of milliseconds for some configurations.*

**Example:**

```
fsp_err_t err = R_LVD_Open(&g_lvd_ctrl, &g_lvd_cfg);
```

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	Requested configuration was invalid
FSP_ERR_ALREADY_OPEN	The instance was already opened
FSP_ERR_IN_USE	Another instance is already using the desired monitor
FSP_ERR_UNSUPPORTED	Digital filter was enabled on a device that does not support it

◆ **R\_LVD\_Close()**

```
fsp_err_t R_LVD_Close ( lvd_ctrl_t *const p_api_ctrl)
```

Disables the LVD peripheral. Closes the driver instance.

**Parameters**

[in]	p_api_ctrl	Pointer to the control block structure for the driver instance
------	------------	--

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_StatusGet()**

```
fsp_err_t R_LVD_StatusGet ( lvd_ctrl_t *const p_api_ctrl, lvd_status_t * p_lvd_status )
```

Get the current state of the monitor (threshold crossing detected, voltage currently above or below threshold).

**Parameters**

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
[out]	p_lvd_status	Pointer to status structure

Example:

```
err = R_LVD_StatusGet(&g_lvd_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_StatusClear()**

```
fsp_err_t R_LVD_StatusClear ( lvd_ctrl_t *const p_api_ctrl)
```

Clears the latched status of the monitor.

**Parameters**

[in]	p_api_ctrl	Pointer to the control structure for the driver instance
------	------------	--

**Return values**

FSP_SUCCESS	Successful
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_NOT_OPEN	Driver is not open

◆ **R\_LVD\_CallbackSet()**

```
fsp_err_t R_LVD_CallbackSet ( lvd_ctrl_t *const p_api_ctrl, void(*)(lvd_callback_args_t *)
p_callback, void const *const p_context, lvd_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `lvd_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

**4.2.36 Operational Amplifier (r\_opamp)**

## Modules

**Functions**

```
fsp_err_t R_OPAMP_Open (opamp_ctrl_t *const p_api_ctrl, opamp_cfg_t const
*const p_cfg)
```

```
fsp_err_t R_OPAMP_InfoGet (opamp_ctrl_t *const p_api_ctrl, opamp_info_t
*const p_info)
```

```
fsp_err_t R_OPAMP_Start (opamp_ctrl_t *const p_api_ctrl, uint32_t const
channel_mask)
```

```
fsp_err_t R_OPAMP_Stop (opamp_ctrl_t *const p_api_ctrl, uint32_t const
channel_mask)
```

```
fsp_err_t R_OPAMP_StatusGet (opamp_ctrl_t *const p_api_ctrl, opamp_status_t
*const p_status)
```

```
fsp_err_t R_OPAMP_Trim (opamp_ctrl_t *const p_api_ctrl, opamp_trim_cmd_t
const cmd, opamp_trim_args_t const *const p_args)
```

```
fsp_err_t R_OPAMP_Close (opamp_ctrl_t *const p_api_ctrl)
```

## Detailed Description

Driver for the OPAMP peripheral on RA MCUs. This module implements the [OPAMP Interface](#).

## Overview

The OPAMP HAL module provides a high level API for signal amplification applications and supports the OPAMP peripheral available on RA MCUs.

### Features

- Low power or high-speed mode
- Start by software or AGT compare match
- Stop by software or ADC conversion end (stop by ADC conversion end only supported on op-amp channels configured to start by AGT compare match)
- Trimming available on some MCUs (see hardware manual)

## Configuration

### Build Time Configurations for r\_opamp

The following build time configurations are defined in fsp\_cfg/r\_opamp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > Operational Amplifier Driver on r\_opamp

This module can be added to the Stacks tab via New Stack > Driver > Analog > Operational

## Amplifier Driver on r\_opamp.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_opamp0	Module name.
AGT Start Trigger Configuration (N/A unless AGT Start Trigger is Selected for the Channel)	<ul style="list-style-type: none"> <li>AGT1 Compare Match Starts OPAMPs 0 and 2 if configured for AGT Start, AGT0 Compare Match Starts OPAMPs 1 and 3 if configured for AGT Start</li> <li>AGT1 Compare Match Starts OPAMPs 0 and 1 if configured for AGT Start, AGT0 Compare Match Starts OPAMPs 2 and 3 if configured for AGT Start</li> <li>AGT1 Compare Match Starts all OPAMPs configured for AGT Start</li> </ul>	AGT1 Compare Match Starts all OPAMPs configured for AGT Start	Configure which AGT channel event triggers which op-amp channel. The AGT compare match event only starts the op-amp channel if the AGT Start trigger is selected in the Trigger configuration for the channel.
Power Mode	MCU Specific Options		Configure the op-amp based on power or speed requirements. This setting affects the minimum required stabilization time. Middle speed is not available for all MCUs.
Trigger Channel 0	MCU Specific Options		Select the event triggers to start or stop op-amp channel 0. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 1	MCU Specific Options		Select the event triggers to start or stop

			op-amp channel 1. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 2	<ul style="list-style-type: none"> <li>• Software Start</li> <li>• Software Stop</li> <li>• AGT Start</li> <li>• Software Stop</li> <li>• AGT Start ADC</li> <li>• Stop</li> </ul>	Software Start Software Stop	Select the event triggers to start or stop op-amp channel 2. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
Trigger Channel 3	MCU Specific Options		Select the event triggers to start or stop op-amp channel 3. If the event trigger is selected for start, the start() API enables the event trigger for this channel. If the event trigger is selected for stop, the stop() API disables the event trigger for this channel.
OPAMP AMP0OS	MCU Specific Options		Select output to connect to AMP0O pin
OPAMP AMP0PS	MCU Specific Options		Select input to connect to AMP0+ pin
OPAMP AMP0MS	MCU Specific Options		Select input to connect to AMP0- pin
OPAMP AMP1PS	MCU Specific Options		Select input to connect to AMP1+ pin
OPAMP AMP1MS	MCU Specific Options		Select input to connect to AMP1- pin
OPAMP AMP2PS	MCU Specific Options		Select input to connect to AMP2+ pin
OPAMP AMP2MS	MCU Specific Options		Select input to connect to AMP2- pin

## Clock Configuration

The OPAMP runs on PCLKB.

## Pin Configuration

To use the OPAMP HAL module, the port pins for the channels receiving the analog input must be set as inputs on the **Pins** tab of the RA Configuration editor.

Refer to the most recent FSP Release Notes for any additional operational limitations for this module.

## Usage Notes

### Trimming the OPAMP

- On MCUs that support trimming, the op-amp trim register is set to the factory default after the Open API is called.
- This function allows the application to trim the operational amplifier to a user setting, which overwrites the factory default trim values.
- Supported on selected MCUs. See hardware manual for details.
- Not supported if configured for low power mode (OPAMP\_MODE\_LOW\_POWER).
- This function is not reentrant. Only one side of one op-amp can be trimmed at a time. Complete the procedure for one side of one channel before calling the trim API with the command OPAMP\_TRIM\_CMD\_START again.
  - The trim procedure works as follows:
    - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_START.
    - Connect a fixed voltage to the Pch (+) input.
    - Connect the Nch (-) input to the op-amp output to create a voltage follower.
    - Ensure the op-amp is operating and stabilized.
    - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_START.
    - Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
  - Iterate over the following loop 5 times:
    - Call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_NEXT\_STEP.
    - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
    - If  $A \leq B$ , call trim() for the Pch (+) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.
  - Call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_START.
  - Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
  - Iterate over the following loop 5 times:
    - Call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_NEXT\_STEP.
    - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
    - If  $A \leq B$ , call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.

## Examples

### Basic Example

This is a basic example of minimal use of the R\_OPAMP in an application. The example demonstrates

configuring OPAMP channel 0 for high speed mode, starting the OPAMP and reading the status of the OPAMP channel running. It also verifies that the stabilization wait time is the expected time for selected power mode

```
#define OPAMP_EXAMPLE_CHANNEL (0U)

void basic_example (void)
{
    fsp_err_t err;

    /* Initialize the OPAMP module. */
    err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Start the OPAMP module. */
    err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);
    assert(FSP_SUCCESS == err);

    /* Look up the required stabilization wait time. */
    opamp_info_t info;
    err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);
    assert(FSP_SUCCESS == err);

    /* Wait for the OPAMP to stabilize. */
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
}

```

## Trim Example

This example demonstrates the typical trimming procedure for opamp channel 0 using [R\\_OPAMP\\_Trim\(\)](#) API.

```
#ifndef OPAMP_EXAMPLE_CHANNEL
#define OPAMP_EXAMPLE_CHANNEL (0U)
#endif

#ifndef OPAMP_EXAMPLE_ADC_CHANNEL
#define OPAMP_EXAMPLE_ADC_CHANNEL (ADC_CHANNEL_2)
#endif

#define ADC_SCAN_END_DELAY (100U)
#define OPAMP_TRIM_LOOP_COUNT (5)
#define ADC_SCAN_END_MAX_TIMEOUT (0xFFFF)

```

```
uint32_t          g_callback_event_counter = 0;
opamp_trim_args_t trim_args_ch =
{
    .channel = OPAMP_EXAMPLE_CHANNEL,
    .input   = OPAMP_TRIM_INPUT_PCH
};
/* This callback is called when ADC Scan Complete event is generated. */
void adc_callback (adc_callback_args_t * p_args)
{
    FSP_PARAMETER_NOT_USED(p_args);
    g_callback_event_counter++;
}
void trimming_example (void)
{
    fsp_err_t err;
    /* On RA2A1, configure negative feedback and put DAC12 signal on AMP0+ Pin. */
    g_opamp_cfg_extend.plus_input_select_opamp0 = OPAMP_PLUS_INPUT_AMPPS7;
    g_opamp_cfg_extend.minus_input_select_opamp0 = OPAMP_MINUS_INPUT_AMPMS7;
    /* Initialize the OPAMP module. */
    err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start the OPAMP module. */
    err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);
    assert(FSP_SUCCESS == err);
    /* Look up the required stabilization wait time. */
    opamp_info_t info;
    err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);
    assert(FSP_SUCCESS == err);
    /* Wait for the OPAMP to stabilize. */
    R_BSP_SoftwareDelay(info.min_stabilization_wait_us, BSP_DELAY_UNITS_MICROSECONDS);
    /* Call trim() for the Pch (+) side input */
    trim_procedure(&trim_args_ch);
    assert(FSP_SUCCESS == err);
}
```

```
    trim_args_ch.input = OPAMP_TRIM_INPUT_NCH;
/* Call trim() for the Nch (-) side input */
    trim_procedure(&trim_args_ch);
}
void trim_procedure (opamp_trim_args_t * trim_args)
{
    fsp_err_t err;
/* Call trim() for the selected channel and input with command OPAMP_TRIM_CMD_START.
*/
    err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_START, trim_args);
    assert(FSP_SUCCESS == err);
/* Measure the fixed voltage connected to the channel input using the SAR ADC and
save the value
* (referred to as result_a later in this procedure). */
/* Reset the ADC callback counter */
    g_callback_event_counter = 0;
    err = R_ADC_ScanStart(&g_adc_ctrl);
    assert(FSP_SUCCESS == err);
/* Wait for ADC scan complete flag */
    uint32_t timeout = ADC_SCAN_END_MAX_TIMEOUT;
while (g_callback_event_counter == 0 && timeout != 0)
    {
        timeout--;
    }
if (0 == timeout)
    {
        err = FSP_ERR_TIMEOUT;
        assert(FSP_SUCCESS == err);
    }
    uint16_t result_a;
    err = R_ADC_Read(&g_adc_ctrl, OPAMP_EXAMPLE_ADC_CHANNEL, &result_a);
    assert(FSP_SUCCESS == err);
/* Iterate over the following loop 5 times: */
/* Call trim() with command OPAMP_TRIM_CMD_NEXT_STEP for the selected channel and
```

```
given input. */
uint8_t count = OPAMP_TRIM_LOOP_COUNT;
while (count > 0)
{
    count--;
    err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_NEXT_STEP, trim_args);
    assert(FSP_SUCCESS == err);
    /* Reset the ADC callback counter */
    g_callback_event_counter = 0;
    /* Read converted value after trim completes. */
    err = R_ADC_ScanStart(&g_adc_ctrl);
    assert(FSP_SUCCESS == err);
    /* Wait for ADC scan complete flag */
    timeout = ADC_SCAN_END_MAX_TIMEOUT;
    while (g_callback_event_counter == 0 && timeout != 0)
    {
        timeout--;
    }
    if (0 == timeout)
    {
        err = FSP_ERR_TIMEOUT;
        assert(FSP_SUCCESS == err);
    }
    uint16_t result_b;
    err = R_ADC_Read(&g_adc_ctrl, OPAMP_EXAMPLE_ADC_CHANNEL, &result_b);
    assert(FSP_SUCCESS == err);
    /* Measure the op-amp output using the SAR ADC (referred to as result_b in the next
step). */
    /* If result_a <= result_b, call trim() for the selected channel and input with
command OPAMP_TRIM_CMD_CLEAR_BIT. */
    if (result_a <= result_b)
    {
        err = R_OPAMP_Trim(&g_opamp_ctrl, OPAMP_TRIM_CMD_CLEAR_BIT, trim_args);
        assert(FSP_SUCCESS == err);
    }
}
```

```

    }
}
}

```

## Data Structures

```
struct opamp_extended_cfg_t
```

```
struct opamp_instance_ctrl_t
```

## Macros

```
#define OPAMP_MASK_CHANNEL_0
```

## Enumerations

```
enum opamp_trigger_t
```

```
enum opamp_agt_link_t
```

```
enum opamp_mode_t
```

```
enum opamp_plus_input_t
```

```
enum opamp_minus_input_t
```

```
enum opamp_output_t
```

## Variables

```
const opamp_api_t g_opamp_on_opamp
```

## Data Structure Documentation

### ◆ opamp\_extended\_cfg\_t

```
struct opamp_extended_cfg_t
```

OPAMP configuration extension. This extension is required and must be provided in [opamp\\_cfg\\_t::p\\_extend](#).

#### Data Fields

<a href="#">opamp_agt_link_t</a>	agt_link	Configure which AGT links are paired to which channel. Only applies to channels if OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP or OPAMP_TRIGGER_AGT_START_ADC_STOP is selected for the channel.
<a href="#">opamp_mode_t</a>	mode	Low power, middle speed, or high speed mode.

<a href="#">opamp_trigger_t</a>	trigger_channel_0	Start and stop triggers for channel 0.
<a href="#">opamp_trigger_t</a>	trigger_channel_1	Start and stop triggers for channel 1.
<a href="#">opamp_trigger_t</a>	trigger_channel_2	Start and stop triggers for channel 2.
<a href="#">opamp_trigger_t</a>	trigger_channel_3	Start and stop triggers for channel 3.
<a href="#">opamp_plus_input_t</a>	plus_input_select_opamp0	OPAMP0+ connection.
<a href="#">opamp_minus_input_t</a>	minus_input_select_opamp0	OPAMP0- connection.
<a href="#">opamp_output_t</a>	output_select_opamp0	OPAMP0O connection.
<a href="#">opamp_plus_input_t</a>	plus_input_select_opamp1	OPAMP1+ connection.
<a href="#">opamp_minus_input_t</a>	minus_input_select_opamp1	OPAMP1- connection.
<a href="#">opamp_plus_input_t</a>	plus_input_select_opamp2	OPAMP2+ connection.
<a href="#">opamp_minus_input_t</a>	minus_input_select_opamp2	OPAMP2- connection.

#### ◆ **opamp\_instance\_ctrl\_t**

struct opamp_instance_ctrl_t
OPAMP instance control block. DO NOT INITIALIZE. Initialized in <a href="#">opamp_api_t::open()</a> .

### Macro Definition Documentation

#### ◆ **OPAMP\_MASK\_CHANNEL\_0**

#define OPAMP_MASK_CHANNEL_0
Version of code that implements the API defined in this file

### Enumeration Type Documentation

◆ **opamp\_trigger\_t**

enum <code>opamp_trigger_t</code>	
Start and stop trigger for the op-amp.	
Enumerator	
<code>OPAMP_TRIGGER_SOFTWARE_START_SOFTWARE_STOP</code>	Start and stop with APIs.
<code>OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP</code>	Start by AGT compare match and stop with API.
<code>OPAMP_TRIGGER_AGT_START_ADC_STOP</code>	Start by AGT compare match and stop after ADC conversion.

◆ **opamp\_agt\_link\_t**

enum <code>opamp_agt_link_t</code>	
Which AGT timer starts the op-amp. Only applies to channels if <code>OPAMP_TRIGGER_AGT_START_SOFTWARE_STOP</code> or <code>OPAMP_TRIGGER_AGT_START_ADC_STOP</code> is selected for the channel. If <code>OPAMP_TRIGGER_SOFTWARE_START_SOFTWARE_STOP</code> is selected for a channel, then no AGT compare match event will start that op-amp channel.	
Enumerator	
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_2_AGT0_OPA_MP_1_3</code>	OPAMP channel 0 and 2 are started by AGT1 compare match. OPAMP channel 1 and 3 are started by AGT0 compare match.
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_1_AGT0_OPA_MP_2_3</code>	OPAMP channel 0 and 1 are started by AGT1 compare match. OPAMP channel 2 and 3 are started by AGT0 compare match.
<code>OPAMP_AGT_LINK_AGT1_OPAMP_0_1_2_3</code>	All OPAMP channels are started by AGT1 compare match.

◆ **opamp\_mode\_t**

enum <code>opamp_mode_t</code>	
Op-amp mode.	
Enumerator	
<code>OPAMP_MODE_LOW_POWER</code>	Low power mode.
<code>OPAMP_MODE_MIDDLE_SPEED</code>	Middle speed mode (not supported on all MCUs)
<code>OPAMP_MODE_HIGH_SPEED</code>	High speed mode.

◆ **opamp\_plus\_input\_t**

enum <code>opamp_plus_input_t</code>	
Options to connect AMPnPS pins.	
Enumerator	
<code>OPAMP_PLUS_INPUT_NONE</code>	No Connection.
<code>OPAMP_PLUS_INPUT_AMPPS0</code>	Set AMPPS0. See hardware manual for channel specific options.
<code>OPAMP_PLUS_INPUT_AMPPS1</code>	Set AMPPS1. See hardware manual for channel specific options.
<code>OPAMP_PLUS_INPUT_AMPPS2</code>	Set AMPPS2. See hardware manual for channel specific options.
<code>OPAMP_PLUS_INPUT_AMPPS3</code>	Set AMPPS3. See hardware manual for channel specific options.
<code>OPAMP_PLUS_INPUT_AMPPS7</code>	Set AMPPS7. See hardware manual for channel specific options.

◆ **opamp\_minus\_input\_t**

enum <code>opamp_minus_input_t</code>	
Options to connect AMPnMS pins.	
Enumerator	
OPAMP_MINUS_INPUT_NONE	No Connection.
OPAMP_MINUS_INPUT_AMPMS0	Set AMPMS0. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS1	Set AMPMS1. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS2	Set AMPMS2. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS3	Set AMPMS3. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS4	Set AMPMS4. See hardware manual for channel specific options.
OPAMP_MINUS_INPUT_AMPMS7	Set AMPMS7. See hardware manual for channel specific options.

◆ **opamp\_output\_t**

enum <code>opamp_output_t</code>	
Options to connect AMP0OS pin.	
Enumerator	
OPAMP_OUTPUT_NONE	No Connection.
OPAMP_OUTPUT_AMPOS0	Set AMPOS0. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS1	Set AMPOS1. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS2	Set AMPOS2. See hardware manual for channel specific options.
OPAMP_OUTPUT_AMPOS3	Set AMPOS3. See hardware manual for channel specific options.

## Function Documentation

### ◆ R\_OPAMP\_Open()

```
fsp_err_t R_OPAMP_Open ( opamp_ctrl_t *const p_api_ctrl, opamp_cfg_t const *const p_cfg )
```

Applies power to the OPAMP and initializes the hardware based on the user configuration. Implements `opamp_api_t::open`.

The op-amp is not operational until the `opamp_api_t::start` is called. If the op-amp is configured to start after AGT compare match, the op-amp is not operational until `opamp_api_t::start` and the associated AGT compare match event occurs.

Some MCUs have switches that must be set before starting the op-amp. These switches must be set in the application code after `opamp_api_t::open` and before `opamp_api_t::start`.

Example:

```
/* Initialize the OPAMP module. */
err = R_OPAMP_Open(&g_opamp_ctrl, &g_opamp_cfg);
```

### Return values

FSP_SUCCESS	Configuration successful.
FSP_ERR_ASSERTION	An input pointer is NULL.
FSP_ERR_ALREADY_OPEN	Control block is already opened.
FSP_ERR_INVALID_ARGUMENT	An attempt to configure OPAMP in middle speed mode on MCU that does not support middle speed mode.

◆ **R\_OPAMP\_InfoGet()**

```
fsp_err_t R_OPAMP_InfoGet ( opamp_ctrl_t*const p_api_ctrl, opamp_info_t*const p_info )
```

Provides the minimum stabilization wait time in microseconds. Implements `opamp_api_t::infoGet`.

• **Example:**

```
/* Look up the required stabilization wait time. */
opamp_info_t info;

err = R_OPAMP_InfoGet(&g_opamp_ctrl, &info);

assert(FSP_SUCCESS == err);

/* Wait for the OPAMP to stabilize. */
R_BSP_SoftwareDelay(info.min_stabilization_wait_us,
BSP_DELAY_UNITS_MICROSECONDS);
```

**Return values**

FSP_SUCCESS	information on <code>opamp_power_mode</code> stored in <code>p_info</code> .
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_OPAMP\_Start()**

```
fsp_err_t R_OPAMP_Start ( opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask )
```

If the OPAMP is configured for hardware triggers, enables hardware triggers. Otherwise, starts the op-amp. Implements `opamp_api_t::start`.

Some MCUs have switches that must be set before starting the op-amp. These switches must be set in the application code after `opamp_api_t::open` and before `opamp_api_t::start`.

Example:

```
/* Start the OPAMP module. */
err = R_OPAMP_Start(&g_opamp_ctrl, 1 << OPAMP_EXAMPLE_CHANNEL);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Op-amp started or hardware triggers enabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_INVALID_ARGUMENT	channel_mask includes a channel that does not exist on this MCU.

◆ **R\_OPAMP\_Stop()**

```
fsp_err_t R_OPAMP_Stop ( opamp_ctrl_t *const p_api_ctrl, uint32_t const channel_mask )
```

Stops the op-amp. If the OPAMP is configured for hardware triggers, disables hardware triggers. Implements `opamp_api_t::stop`.

**Return values**

FSP_SUCCESS	Op-amp stopped or hardware triggers disabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_INVALID_ARGUMENT	channel_mask includes a channel that does not exist on this MCU.

### ◆ R\_OPAMP\_StatusGet()

```
fsp_err_t R_OPAMP_StatusGet ( opamp_ctrl_t *const p_api_ctrl, opamp_status_t *const p_status )
```

Provides the operating status for each op-amp in a bitmask. This bit is set when operation begins, before the stabilization wait time has elapsed. Implements `opamp_api_t::statusGet`.

#### Return values

FSP_SUCCESS	Operating status of each op-amp provided in <code>p_status</code> .
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_OPAMP\_Trim()

```
fsp_err_t R_OPAMP_Trim ( opamp_ctrl_t *const p_api_ctrl, opamp_trim_cmd_t const cmd,
opamp_trim_args_t const *const p_args )
```

On MCUs that support trimming, the op-amp trim register is set to the factory default after `open()`. This function allows the application to trim the operational amplifier to a user setting, which overwrites the factory default factory trim values.

Not supported on all MCUs. See hardware manual for details. Not supported if configured for low power mode (`OPAMP_MODE_LOW_POWER`).

This function is not reentrant. Only one side of one op-amp can be trimmed at a time. Complete the procedure for one side of one channel before calling `trim()` with command `OPAMP_TRIM_CMD_START` again.

Implements `opamp_api_t::trim`.

Reference: Section 37.9 "User Offset Trimming" RA2A1 hardware manual R01UM0008EU0130. The trim procedure works as follows:

- Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_START`.
- Connect a fixed voltage to the Pch (+) input.
- Connect the Nch (-) input to the op-amp output to create a voltage follower.
- Ensure the op-amp is operating and stabilized.
- Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_START`.
- Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
- Iterate over the following loop 5 times:
  - Call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_NEXT_STEP`.
  - Measure the op-amp output using the SAR ADC (referred to as B in the next step).
  - If  $A \leq B$ , call `trim()` for the Pch (+) side input with command `OPAMP_TRIM_CMD_CLEAR_BIT`.
- Call `trim()` for the Nch (-) side input with command `OPAMP_TRIM_CMD_START`.
- Measure the fixed voltage connected to the Pch (+) input using the SAR ADC and save the value (referred to as A later in this procedure).
- Iterate over the following loop 5 times:
  - Call `trim()` for the Nch (-) side input with command `OPAMP_TRIM_CMD_NEXT_STEP`.

- Measure the op-amp output using the SAR ADC (referred to as B in the next step).
- If  $A \leq B$ , call trim() for the Nch (-) side input with command OPAMP\_TRIM\_CMD\_CLEAR\_BIT.

**Return values**

FSP_SUCCESS	Conversion result in p_data.
FSP_ERR_UNSUPPORTED	Trimming is not supported on this MCU.
FSP_ERR_INVALID_STATE	The command is not valid in the current state of the trim state machine.
FSP_ERR_INVALID_ARGUMENT	The requested channel is not operating or the trim procedure is not in progress for this channel/input combination.
FSP_ERR_INVALID_MODE	Trim is not allowed in low power mode.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**◆ R\_OPAMP\_Close()**

```
fsp_err_t R_OPAMP_Close ( opamp_ctrl_t*const p_api_ctrl)
```

Stops the op-amps. Implements `opamp_api_t::close`.

**Return values**

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

**Variable Documentation****◆ g\_opamp\_on\_opamp**

```
const opamp_api_t g_opamp_on_opamp
```

OPAMP Implementation of OPAMP interface.

**4.2.37 Octa Serial Peripheral Interface Flash (r\_ospi)**

Modules

**Functions**

fsp_err_t	R_OSPI_Open (spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
fsp_err_t	R_OSPI_Close (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_OSPI_DirectWrite (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
fsp_err_t	R_OSPI_DirectRead (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t	R_OSPI_DirectTransfer (spi_flash_ctrl_t *p_ctrl, spi_flash_direct_transfer_t *const p_transfer, spi_flash_direct_transfer_dir_t direction)
fsp_err_t	R_OSPI_SpiProtocolSet (spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
fsp_err_t	R_OSPI_XipEnter (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_OSPI_XipExit (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_OSPI_Write (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
fsp_err_t	R_OSPI_Erase (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
fsp_err_t	R_OSPI_StatusGet (spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
fsp_err_t	R_OSPI_BankSet (spi_flash_ctrl_t *p_ctrl, uint32_t bank)

## Detailed Description

Driver for the OSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

## Overview

The OSPI peripheral interfaces with an external OctaFlash chip to perform data I/O Operations.

### Features

The OSPI driver has the following key features:

- Perform data I/O Operation in both SPI and OPI modes
- Can be configured with OctaFlash device on either of the 2 channels
- Memory mapped read access to the OctaFlash
- Programming the OctaFlash device using single continuous write
- Erasing the OctaFlash device

- Sending device specific commands and reading back responses
- Entering and exiting XIP (Single Continuous Read) mode
- 3 byte addressing for SPI
- 4 byte addressing for SPI and OPI
- Auto-calibration for OPI mode (SOPI and DOPI)

Additional build-time features:

- Optional (build-time) DMAC support for data transmission.

#### Note

*Use of DMAC for data transmission is strongly recommended. Without the use of DMAC, due to the high-speed hardware design of the OSPI peripheral, data transmission can be sensitive to timing variance, which could cause software-based memory-mapped operations to fail unexpectedly.*

## Configuration

### Build Time Configurations for r\_ospf

The following build time configurations are defined in driver/r\_ospf\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DMAC Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable DMAC support for the OSPI module.

### Configurations for Driver > Storage > OSPI Driver on r\_ospf

This module can be added to the Stacks tab via New Stack > Driver > Storage > OSPI Driver on r\_ospf.

Configuration	Options	Default	Description
General > Single Continuous Mode > Read Idle Time	Must be an integer greater than 0 with maximum configurable value of 127	100	Specify the read idle time.
General > Single Continuous Mode > Write Idle Time	Must be an integer greater than 0 with maximum configurable value of 127	100	Specify the write idle time.
General > Name	Name must be a valid C symbol	g_ospf0	Module name.
General > Channel	Channel should be 0 or 1	0	Specify the OSPI chip select line to use.
General > Flash Size	Must be an integer greater than 0 with maximum configurable	0x04000000	Specify the OctaFlash size in bytes.

	value of 0x3FFFFFFF		
General > SPI Protocol	<ul style="list-style-type: none"> <li>• SPI</li> <li>• Single data rate OPI</li> <li>• Dual data rate OPI</li> </ul>	SPI	Select the initial SPI protocol. SPI protocol can be changed on the OctaFlash using <a href="#">R_OSPI_DirectTransfer()</a> .
General > Address Bytes	<ul style="list-style-type: none"> <li>• 3</li> <li>• 4</li> </ul>	4	Select the number of address bytes.
OPI Mode > Auto-Calibration > Data latching delay	Must be a valid non-negative integer with maximum configurable value of 0xFF	0x80	Set this to 0 to enable auto-calibration. 0x80 is the default value calculated at 3.3V and 25°C
OPI Mode > Auto-Calibration > Auto-Calibration Address	Must be a valid non-negative integer with maximum configurable value of 0xFFFFFFFF	0x00	Set the address of the read/write destination to be performed for auto-calibration.
OPI Mode > Command Definitions > Page Program Command	Must be a 16-bit OSPI Page Program Command under OPI Mode Command Definitions	0x12ED	The command to program a page in OPI mode.
OPI Mode > Command Definitions > Read Command	Must be a 16-bit OSPI Read Command under OPI Mode Command Definitions	0xEC13	The command to read in SOPI mode (8READ).
OPI Mode > Command Definitions > Dual Read Command	Must be a 16-bit OSPI Dual Read Command under OPI Mode Command Definitions	0xEE11	The command to read in DOPI mode (8DTRD).
OPI Mode > Command Definitions > Write Enable Command	Must be a 16-bit OSPI Write Enable Command under OPI Mode Command Definitions	0x06F9	The command to enable write in OPI mode.
OPI Mode > Command Definitions > Status Command	Must be a 16-bit OSPI Status Command under OPI Mode Command Definitions	0x05FA	The command to query the status of a write or erase command in OPI mode.
OPI Mode > Command Length Bytes	Must be an integer between 1 and 2	2	Command length in bytes
OPI Mode > Memory Read Dummy Cycles	Must be an integer between 6 and 10	10	Memory read dummy cycles
OPI Mode > DOPI Byte Order	<ul style="list-style-type: none"> <li>• Byte0, Byte1, Byte2, Byte3</li> </ul>	Byte0, Byte1, Byte2, Byte3	Byte order on the external bus

	<ul style="list-style-type: none"> <li>Byte1, Byte0, Byte3, Byte2</li> </ul>		
SPI Mode > Command Definitions > Page Program Command	Must be a 8-bit OSPI Page Program Command under SPI Mode Command Definitions	0x12	The command to program a page in SPI mode.
SPI Mode > Command Definitions > Read Command	Must be a 8-bit OSPI Read Command under SPI Mode Command Definitions	0x13	The command to read in SPI mode.
SPI Mode > Command Definitions > Write Enable Command	Must be a 16-bit OSPI Write Enable Command under SPI Mode Command Definitions	0x06	The command to enable write in SPI mode.
SPI Mode > Command Definitions > Status Command	Must be a 16-bit OSPI Status Command under SPI Mode Command Definitions	0x05	The command to query the status of a write or erase command in SPI mode.
Common Command Definitions > Sector Erase Command	Must be a value greater than or equal to 0	0x21DE	The command to erase a sector. Set Sector Erase Size to 0 if unused.
Common Command Definitions > Block Erase Command	Must be a value greater than or equal to 0	0xDC23	The command to erase a block. Set Block Erase Size to 0 if unused.
Common Command Definitions > Chip Erase Command	Must be a value greater than or equal to 0	0xC738	The command to erase the entire chip. Set Chip Erase Command to 0 if unused.
Common Command Definitions > Write Status Bit	Must be an integer between 0 and 7	0	Which bit contains the write in progress status returned from the Write Status Command.
Common Command Definitions > Sector Erase Size	Must be an integer greater than or equal to 0	4096	The sector erase size. Set Sector Erase Size to 0 if Sector Erase is not supported.
Common Command Definitions > Block Erase Size	Must be an integer greater than or equal to 0	65536	The block erase size. Set Block Erase Size to 0 if Block Erase is not supported.
Chip Select Timing Setting > Memory Mapped Read	<ul style="list-style-type: none"> <li>2</li> <li>5</li> <li>7</li> </ul>	2	Memory mapped read command execution interval setting in

Command Interval	<ul style="list-style-type: none"> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> <li>• 17</li> </ul>		OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Command Interval	<ul style="list-style-type: none"> <li>• 2</li> <li>• 5</li> <li>• 7</li> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> <li>• 17</li> </ul>	2	Memory mapped write command execution interval setting in OCTACLK units
Chip Select Timing Setting > Command Interval	<ul style="list-style-type: none"> <li>• 2</li> <li>• 5</li> <li>• 7</li> <li>• 9</li> <li>• 11</li> <li>• 13</li> <li>• 15</li> <li>• 17</li> </ul>	2	Command execution interval setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Read Pull-up Timing	<ul style="list-style-type: none"> <li>• 5 SPI/SOPI</li> <li>• 6 SPI/SOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	5 SPI/SOPI	Memory mapped read signal pull-up timing setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Pull-up Timing	<ul style="list-style-type: none"> <li>• 2 SPI/SOPI, 1.5 DOPI</li> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> <li>• 6 SPI/SOPI, 5.5 DOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	2 SPI/SOPI, 1.5 DOPI	Memory mapped write signal pull-up timing setting in OCTACLK units
Chip Select Timing Setting > Pull-up Timing	<ul style="list-style-type: none"> <li>• 5 SPI/SOPI</li> <li>• 6 SPI/SOPI</li> <li>• 7 SPI/SOPI, 6.5 DOPI</li> <li>• 8 SPI/SOPI, 7.5 DOPI</li> <li>• 9 SPI/SOPI, 8.5 DOPI</li> </ul>	5 SPI/SOPI	Signal pull-up timing setting in OCTACLK units

	DOPI		
Chip Select Timing Setting > Memory Mapped Read Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Memory mapped read signal pull-down timing setting in OCTACLK units
Chip Select Timing Setting > Memory Mapped Write Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Memory mapped write signal pull-down timing setting in OCTACLK units
Chip Select Timing Setting > Pull-down Timing	<ul style="list-style-type: none"> <li>• 3 SPI/SOPI, 2.5 DOPI</li> <li>• 4 SPI/SOPI, 3.5 DOPI</li> <li>• 5 SPI/SOPI, 4.5 DOPI</li> </ul>	3 SPI/SOPI, 2.5 DOPI	Signal pull-down timing setting in OCTACLK units

**Note**

The user is expected to modify the command definitions based on the OctaFlash chip and SPI communication mode. The default mode is SPI mode and default erase commands are set for OPI mode based on Macronix OctaFlash MX25LM51245G.

**Enabling DMAC**

DMAC data transmission support is configurable and is disabled from the build by default. Use of a high-priority (low channel number) DMAC for data transmission is strongly recommended.

For further details on DMAC please refer [Direct Memory Access Controller \(r\\_dmac\)](#).

**Clock Configuration**

PCLKB is the Octal-SPI bus interface, and PCLKA is used to set OSPI registers.

The signals to the OSPI device are derived from OCTASPICLK. The OMSCLK signal is OCTASPICLK / 2. Data can be output at the OCTASPICLK rate if SPI Protocol is set to Dual Data Rate OPI.

The PCLKB, PCLKA, and OCTASPICLK frequencies can be set on the **Clocks** tab of the RA Configuration editor.

**Pin Configuration**

The following pins are available to connect to an external OSPI device:

- OMSCLK: OSPI clock output (OCTASPICLK / 2)
- OMDQS: OSPI data strobe signal
- OMCS0: OSPI device 0 select
- OMCS1: OSPI device 1 select
- OMSIO0: Data 0 I/O
- OMSIO1: Data 1 I/O
- OMSIO2: Data 2 I/O

- OMSIO3: Data 3 I/O
- OMSIO4: Data 4 I/O
- OMSIO5: Data 5 I/O
- OMSIO6: Data 6 I/O
- OMSIO7: Data 7 I/O

#### Note

*Data pins must be configured with IOPORT\_CFG\_DRIVE\_HS\_HIGH.  
Chip Select pins should be configured with at least IOPORT\_CFG\_DRIVE\_MEDIUM.*

## Usage Notes

### OSPI Memory Mapped Access

After [R\\_OSPI\\_Open\(\)](#) completes successfully, the OctaFlash device contents are mapped to address 0x68000000 (channel 0) or 0x70000000 (channel 1) based on the channel configured and can be read like on-chip flash. Channel 0 supports 128 MB while Channel 1 supports 256 MB of address space.

### Auto-calibration

Auto-calibration procedure is triggered automatically when the 'Data latching delay' field in the configurator properties is set to 0. The user application is responsible for setting the appropriate preamble pattern before calling [R\\_OSPI\\_Open\(\)](#) with SOPI/DOPI mode or changing the SPI protocol to SOPI/DOPI using [R\\_OSPI\\_SpiProtocolSet\(\)](#) API. The appropriate preamble pattern can be written to the desired address using the [R\\_OSPI\\_Write\(\)](#) API while in the SPI mode. Ensure that the same address is passed through the configurator. If the OctaFlash chip is already in SOPI/DOPI mode, the preamble pattern must be programmed using the debugger before calling [R\\_OSPI\\_Open\(\)](#).

### Chip Select Latencies

Chip select latencies can be set through the configurator. The default settings support SOPI and SPI at minimum latency. In case the driver is opened in SPI mode and will be switched to DOPI mode later using [R\\_OSPI\\_SpiProtocolSet\(\)](#), please select latencies required for DOPI before calling [R\\_OSPI\\_Open\(\)](#).

### OctaFlash Commands

- Set the erase commands based on intended mode of operation (SPI or OPI). These commands cannot be changed during run-time.
- Read, Write and Status commands for both SPI and OPI are configured allowing switching between the modes at run-time.

### Limitations

Developers should be aware of the following limitations when using the OSPI driver:

- Single continuous read in SPI mode is not supported by the peripheral. The maximum amount of data that can be read using a single read command is 4-bytes (When doing a 32-bit access).
- Fast Reads would be slower than regular reads as the SPI mode cannot be operated with an OMSCLK greater than 50MHz.

## Examples

## Basic Example

This is a basic example of minimal use of the OSPI in an application.

```
#define OSPI_EXAMPLE_DATA_LENGTH (1024)
uint8_t g_dest[OSPI_EXAMPLE_DATA_LENGTH];
/* Place data in the .ospi_flash section to flash it during programming. */
const uint8_t g_src[OSPI_EXAMPLE_DATA_LENGTH] BSP_PLACE_IN_SECTION(".ospi_flash") =
"ABCDEFGHIJKLMNOPQRSTUVWXYZ";
/* Place code in the .code_in_ospi section to flash it during programming. */
void r_ospi_example_function(void) BSP_PLACE_IN_SECTION(".code_in_ospi")
__attribute__((noinline));
void r_ospi_example_function (void)
{
    /* Add code here. */
}
void r_ospi_basic_example (void)
{
    /* Open the OSPI instancee */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
    assert(FSP_SUCCESS == err);
    /* (Optional) Change SPI to DOPI mode */
    r_ospi_example_spi_to_dopi();
    /* After R_OSPI_Open() and any required device specific intiialization, data can be
read directly from the OSPI flash. */
    memcpy(&g_dest[0], &g_src[0], OSPI_EXAMPLE_DATA_LENGTH);
    /* After R_OSPI_Open() and any required device specific intiialization, functions in
the OSPI flash can be called. */
    r_ospi_example_function();
}
```

## Reading Status Register Example (R\_OSPI\_DirectWrite, R\_OSPI\_DirectRead)

This is an example of using R\_OSPI\_DirectWrite followed by R\_OSPI\_DirectRead to send the read status register command and read back the status register from the device.

```
#define OSPI_COMMAND_READ_STATUS_REGISTER (0x05U)
```

```
void r_ospi_direct_example (void)
{
    spi_flash_direct_transfer_t ospi_test_direct_transfer =
    {
        .command      = OSPI_TEST_READ_STATUS_COMMAND_SPI_MODE,
        .address       = 0U,
        .data          = 0U,
        .command_length = 1U,
        .address_length = 0U,
        .data_length   = 0U,
        .dummy_cycles  = 0U
    };
    /* Open the OSPI instance. */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
    assert(FSP_SUCCESS == err);
    /* Write Enable */
    err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_WRITE);
    assert(FSP_SUCCESS == err);
    /* Read Status Register */
    ospi_test_direct_transfer.command = OSPI_TEST_READ_STATUS_COMMAND_SPI_MODE;
    ospi_test_direct_transfer.data_length = 1U;
    err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_READ);
    assert(FSP_SUCCESS == err);
    /* Check if Write Enable is set */
    if (OSPI_WEN_BIT_MASK != (ospi_test_direct_transfer.data & OSPI_WEN_BIT_MASK))
    {
        __BKPT(0);
    }
}
```

### Auto-calibration Example (R\_OSPI\_DirectOpen, R\_OSPI\_DirectWrite, R\_OSPI\_SpiProtocolSet)

This is an example of using `R_OSPI_SpiProtocolSet` to change the operating mode from SPI to SOPI and allow the driver to initiate auto-calibration.

```
#define OSPI_DOPI_PREAMBLE_PATTERN_LENGTH_BYTES (16U)
#define OSPI_EXAMPLE_PREAMBLE_ADDRESS (0x68000000U) /* Device connected to CS0 */
const uint8_t g_preamble_bytes[OSPI_DOPI_PREAMBLE_PATTERN_LENGTH_BYTES] =
{
    0x00, 0x00, 0xFF, 0xFF, 0xFF, 0x00, 0x08, 0x00, 0x00, 0xF7, 0xFF, 0x00, 0x08,
    0xF7, 0x00, 0xF7
};
void ospi_example_wait_until_wip (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    spi_flash_status_t status;
    status.write_in_progress = true;
    uint32_t timeout = UINT32_MAX;
    while ((status.write_in_progress) && (--timeout))
    {
        err = R_OSPI_StatusGet(&g_ospi0_ctrl, &status);
        assert(FSP_SUCCESS == err);
    }
    if (0 == timeout)
    {
        assert(FSP_SUCCESS == err);
    }
}
void r_ospi_auto_calibrate_example (void)
{
    /* Open the OSPI instance. */
    /* Set data_latch_delay_clocks to 0x0 to enable auto-calibration */
    fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
    assert(FSP_SUCCESS == err);
    uint8_t * preamble_pattern_addr = (uint8_t *) OSPI_EXAMPLE_PREAMBLE_ADDRESS;
    err = R_OSPI_Write(&g_ospi0_ctrl, g_preamble_bytes, preamble_pattern_addr,
OSPI_EXAMPLE_PREAMBLE_ADDRESS);
```

```

assert(FSP_SUCCESS == err);

/* Wait until write has been completed */

ospi_example_wait_until_wip();

/* Change from SPI to DOPI mode */

r_ospi_example_spi_to_dopi();
}

```

### Octack Update Example (R\_OSPI\_SpiProtocolSet)

This is an example of using R\_BSP\_OctackUpdate to change the Octal-SPI clock frequency during run time. The OCTACK frequency must be updated before calling the R\_OSPI\_SpiProtocolSet with appropriate clock source and divider settings required to be set for the new SPI protocol mode. Ensure that the clock source selected is started.

```

static void ospi_example_change_omclk (void)
{
/* Ensure clock source (PLL2 in this example) is running before changing the OCTACK
frequency */

bsp_octack_settings_t octack_settings;

octack_settings.source_clock = BSP_CLOCKS_CLOCK_PLL2;

octack_settings.divider      = BSP_CLOCKS_OCTACK_DIV_2;

R_BSP_OctackUpdate(&octack_settings);
}

```

### OSPI Data and IAR

When using the IAR compiler, OSPI data must be const qualified to be downloaded by the debugger.

#### Data Structures

struct [ospi\\_instance\\_ctrl\\_t](#)

#### Enumerations

enum [ospi\\_device\\_number\\_t](#)

enum [ospi\\_command\\_cs\\_pullup\\_clocks\\_t](#)

enum [ospi\\_command\\_cs\\_pulldown\\_clocks\\_t](#)

enum [ospi\\_dopi\\_byte\\_order\\_t](#)

## Data Structure Documentation

### ◆ `ospi_instance_ctrl_t`

```
struct ospi_instance_ctrl_t
```

Instance control block. DO NOT INITIALIZE. Initialization occurs when `spi_flash_api_t::open` is called

## Enumeration Type Documentation

### ◆ `ospi_device_number_t`

```
enum ospi_device_number_t
```

Enumerator

OSPI_DEVICE_NUMBER_0	Device connected to Chip-Select 0.
OSPI_DEVICE_NUMBER_1	Device connected to Chip-Select 1.

### ◆ `ospi_command_cs_pullup_clocks_t`

```
enum ospi_command_cs_pullup_clocks_t
```

Enumerator

OSPI_COMMAND_CS_PULLUP_CLOCKS_2	1.5 clocks DOPI mode; 2 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_3	2.5 clocks DOPI mode; 3 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_4	3.5 clocks DOPI mode; 4 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_5	4.5 clocks DOPI mode; 5 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_6	5.5 clocks DOPI mode; 6 Clocks all other modes; Unsupported for DOPI Read
OSPI_COMMAND_CS_PULLUP_CLOCKS_7	6.5 clocks DOPI mode; 7 Clocks all other modes
OSPI_COMMAND_CS_PULLUP_CLOCKS_8	7.5 clocks DOPI mode; 8 Clocks all other modes
OSPI_COMMAND_CS_PULLUP_CLOCKS_9	8.5 clocks DOPI mode; 9 Clocks all other modes

◆ **ospi\_command\_cs\_pulldown\_clocks\_t**

enum <code>ospi_command_cs_pulldown_clocks_t</code>	
Enumerator	
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_3</code>	2.5 clocks DOPI mode; 3 Clocks all other modes
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_4</code>	3.5 clocks DOPI mode; 4 Clocks all other modes
<code>OSPI_COMMAND_CS_PULLDOWN_CLOCKS_5</code>	4.5 clocks DOPI mode; 5 Clocks all other modes

◆ **ospi\_dopi\_byte\_order\_t**

enum <code>ospi_dopi_byte_order_t</code>	
Enumerator	
<code>OSPI_DOPI_BYTE_ORDER_0123</code>	DOPI byte order byte 0, byte 1, byte 2, byte 3.
<code>OSPI_DOPI_BYTE_ORDER_1032</code>	DOPI byte order byte 1, byte 0, byte 3, byte 2.

**Function Documentation**◆ **R\_OSPI\_Open()**

```
fsp_err_t R_OSPI_Open ( spi_flash_ctrl_t* p_ctrl, spi_flash_cfg_t const *const p_cfg )
```

Open the OSPI driver module. After the driver is open, the OSPI can be accessed like internal flash memory.

Implements `spi_flash_api_t::open`.

Example:

```
/* Open the OSPI instancee */
fsp_err_t err = R_OSPI_Open(&g_ospi0_ctrl, &g_ospi0_cfg);
```

**Return values**

<code>FSP_SUCCESS</code>	Configuration was successful.
<code>FSP_ERR_ASSERTION</code>	The parameter <code>p_ctrl</code> or <code>p_cfg</code> is NULL.
<code>FSP_ERR_ALREADY_OPEN</code>	Driver has already been opened with the same <code>p_ctrl</code> .
<code>FSP_ERR_CALIBRATE_FAILED</code>	Failed to perform auto-calibrate.

◆ **R\_OSPI\_Close()**

```
fsp_err_t R_OSPI_Close ( spi_flash_ctrl_t* p_ctrl)
```

Close the OSPI driver module.

Implements `spi_flash_api_t::close`.

**Return values**

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	p_instance_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_DirectWrite()**

```
fsp_err_t R_OSPI_DirectWrite ( spi_flash_ctrl_t* p_ctrl, uint8_t const*const p_src, uint32_t const bytes, bool const read_after_write )
```

Writes raw data directly to the OctaFlash. API not supported. Use `R_OSPI_DirectTransfer`

Implements `spi_flash_api_t::directWrite`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

◆ **R\_OSPI\_DirectRead()**

```
fsp_err_t R_OSPI_DirectRead ( spi_flash_ctrl_t* p_ctrl, uint8_t*const p_dest, uint32_t const bytes )
```

Reads raw data directly from the OctaFlash. API not supported. Use `R_OSPI_DirectTransfer`.

Implements `spi_flash_api_t::directRead`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

◆ **R\_OSPI\_DirectTransfer()**

```
fsp_err_t R_OSPI_DirectTransfer ( spi_flash_ctrl_t * p_ctrl, spi_flash_direct_transfer_t *const
p_transfer, spi_flash_direct_transfer_dir_t direction )
```

Read/Write raw data directly with the OctaFlash.

Implements `spi_flash_api_t::directTransfer`.

Example:

```
/* Write Enable */
err = R_OSPI_DirectTransfer(&g_ospi0_ctrl, &ospi_test_direct_transfer,
SPI_FLASH_DIRECT_TRANSFER_DIR_WRITE);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_SpiProtocolSet()**

```
fsp_err_t R_OSPI_SpiProtocolSet ( spi_flash_ctrl_t * p_ctrl, spi_flash_protocol_t spi_protocol )
```

Sets the SPI protocol.

Implements `spi_flash_api_t::spiProtocolSet`.

**Return values**

FSP_SUCCESS	SPI protocol updated on MCU peripheral.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_CALIBRATE_FAILED	Failed to perform auto-calibrate.

◆ **R\_OSPI\_XipEnter()**

```
fsp_err_t R_OSPI_XipEnter ( spi_flash_ctrl_t * p_ctrl)
```

Enters Single Continuous Read/Write mode.

Implements `spi_flash_api_t::xipEnter`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_XipExit()**

```
fsp_err_t R_OSPI_XipExit ( spi_flash_ctrl_t * p_ctrl)
```

Exits XIP (execute in place) mode.

Implements `spi_flash_api_t::xipExit`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_Write()**

```
fsp_err_t R_OSPI_Write ( spi_flash_ctrl_t* p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest,
uint32_t byte_count )
```

Program a page of data to the flash.

Implements `spi_flash_api_t::write`.

Example:

```
err = R_OSPI_Write(&g_ospi0_ctrl, g_preamble_bytes, preamble_pattern_addr,
OSPI_EXAMPLE_PREAMBLE_ADDRESS);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	p_instance_ctrl, p_dest or p_src is NULL, or byte_count crosses a page boundary.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_DEVICE_BUSY	Another Write/Erase transaction is in progress.
FSP_ERR_INVALID_SIZE	Write operation crosses page-boundary.

◆ **R\_OSPI\_Erase()**

```
fsp_err_t R_OSPI_Erase ( spi_flash_ctrl_t* p_ctrl, uint8_t *const p_device_address, uint32_t
byte_count )
```

Erase a block or sector of flash. The byte\_count must exactly match one of the erase sizes defined in `spi_flash_cfg_t`. For chip erase, byte\_count must be `SPI_FLASH_ERASE_SIZE_CHIP_ERASE`.

Implements `spi_flash_api_t::erase`.

**Return values**

FSP_SUCCESS	The command to erase the flash was executed successfully.
FSP_ERR_ASSERTION	p_instance_ctrl or p_device_address is NULL, byte_count doesn't match an erase size defined in <code>spi_flash_cfg_t</code> , or byte_count is set to 0.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_OSPI\_StatusGet()**

```
fsp_err_t R_OSPI_StatusGet ( spi_flash_ctrl_t* p_ctrl, spi_flash_status_t*const p_status )
```

Gets the write or erase status of the flash.

Implements `spi_flash_api_t::statusGet`.

Example:

```
err = R_OSPI_StatusGet(&g_ospi0_ctrl, &status);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	The write status is in p_status.
FSP_ERR_ASSERTION	p_instance_ctrl or p_status is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_OSPI\_BankSet()**

```
fsp_err_t R_OSPI_BankSet ( spi_flash_ctrl_t* p_ctrl, uint32_t bank )
```

Selects the bank to access.

Implements `spi_flash_api_t::bankSet`.

**Return values**

FSP_ERR_UNSUPPORTED	API not supported by OSPI.
---------------------	----------------------------

**4.2.38 Parallel Data Capture (r\_pdc)**

## Modules

**Functions**

```
fsp_err_t R_PDC_Open (pdc_ctrl_t*const p_api_ctrl, pdc_cfg_t const*const p_cfg)
```

Powers on PDC, handles required initialization described in the hardware manual. [More...](#)

```
fsp_err_t R_PDC_Close (pdc_ctrl_t*const p_api_ctrl)
```

Stops and closes the transfer interface, disables and powers off the PDC, clears internal driver data and disables interrupts. [More...](#)

```
fsp_err_t R_PDC_CaptureStart (pdc_ctrl_t *const p_api_ctrl, uint8_t *const p_buffer)
```

Starts a capture. Enables interrupts. [More...](#)

## Detailed Description

Driver for the PDC peripheral on RA MCUs. This module implements the [PDC Interface](#).

## Overview

The PDC peripheral supports interfacing with external cameras by accepting timing and data signals in order to capture incoming data. A callback is invoked every time a frame of data is accepted.

### Features

- Capture incoming data into a user defined buffer
- Data bytes per pixel can be configured
- Endianess of the incoming data can be specified
- Supports configuring capture width and height
- Supports configuring vertical and horizontal sync polarity
- Horizontal and Vertical position for image/data capture can be specified
- External clock to the camera module can be adjusted
- Choice between DMA and DTC to transfer out the captured data
- The specified user callback is invoked when a data frame is captured

## Configuration

### Build Time Configurations for r\_pdc

The following build time configurations are defined in fsp\_cfg/r\_pdc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Graphics > PDC Driver on r\_pdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > PDC Driver on r\_pdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_pdc0	Module name.
Input > Signal polarity > HSYNC	<ul style="list-style-type: none"> <li>• High</li> <li>• Low</li> </ul>	High	Specify the active polarity of the HSYNC signal.

Input > Signal polarity > VSYNC	<ul style="list-style-type: none"> <li>• High</li> <li>• Low</li> </ul>	High	Specify the active polarity of the VSYNC signal.
Input > Capture Specifications > Number of pixels to capture horizontally	Value must be an integer greater than 0	640	Specify the number of horizontal pixels to capture.
Input > Capture Specifications > Number of lines to capture vertically	Value must be an integer greater than 0	480	Specify the number of vertical pixels to capture.
Input > Capture Specifications > Horizontal pixel to start capture from	Value must be an integer	0	Specify the horizontal pixel to start capturing image data from. Allows an image smaller than the native resolution of a camera to be captured.
Input > Capture Specifications > Line to start capture from	Value must be an integer	0	Specify the vertical line to start capturing image data from. Allows an image smaller than the native resolution of a camera to be captured.
Input > Bytes per pixel	Value must be an integer greater than 0	2	Specify the number of bytes per pixel of the captured image data.
Input > Clock divider	<ul style="list-style-type: none"> <li>• CLK/2</li> <li>• CLK/4</li> <li>• CLK/6</li> <li>• CLK/8</li> <li>• CLK/10</li> <li>• CLK/12</li> <li>• CLK/14</li> <li>• CLK/16</li> </ul>	CLK/2	Specify the clock divider of the clock input to the PDC peripheral.
Input > Endianness	<ul style="list-style-type: none"> <li>• Little</li> <li>• Big</li> </ul>	Little	Specify the endianness of the captured image data.
Output > Buffer > Image buffer name	Name must be a valid C symbol	g_user_buffer	Specify the name of the data buffer to create or set to NULL, if it is to be created by the user external to the PDC driver.
Output > Buffer > Image buffer section	This property must be a valid section name	.bss	Specify the RAM section for the image data buffer. Typically .bss (internal RAM) or

.sdram. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.

Output > Buffer > Number of image buffers	Value must be an integer greater than 0	1	Specify the number of buffers to create.
Interrupts > Callback	Name must be a valid C symbol	g_pdc_user_callback	A user callback function must be provided. This callback is invoked for every successful frame capture and any error conditions
Interrupts > PDC Interrupt Priority	MCU Specific Options		Select the PDC interrupt priority.
Interrupts > DTC Interrupt Priority	MCU Specific Options		Select the DTC interrupt priority.

## Clock Configuration

The PDC peripheral module uses the PCLKB as its clock source. The maximum clock to the camera module is  $PCLKB / 2$ .

## Pin Configuration

The PCKO pin is a clock output and should be connected to the clock input of the camera. The PIXCLK pin is a clock input and should be connected to the output pixel clock of the camera. Likewise, the HSYNC and VSYNC pins must be connected to the horizontal and vertical sync signals of the camera, respectively. The PIXD0-PIXD7 pins are the 8-bit data bus input and should be connected to the relevant output pins of the camera.

### Note

*Camera control and serial communication pins must be configured separately and are not controlled by this module.*

## Usage Notes

### Interrupt Configuration

- PDC error interrupts are used by this module for reporting errors such as overrun, underrun, vertical line number setting and horizontal byte number setting errors.
- In addition to the PDC error interrupts, DMA or DTC interrupts are also used internally to perform data transfer from this peripheral to the specified image buffer.
- Receive data ready interrupt is used as activation source for DMA and DTC trigger.

### Enabling Transfer Modules

- An option to select between DMAC or DTC is provided with DMA as the default transfer choice.
- For further details on DMA please refer [Direct Memory Access Controller \(r\\_dmac\)](#)
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

### PDC setup with external camera

- Before configuring the external camera device the PDC Open API must be called in order to start clock output.
- Ensure that the memory pointed to by p\_buffer is both valid and large enough to store a complete image.
- The amount of space required (in bytes) can be calculated as: size (bytes) = image width (pixels) \* image height (lines) \* number of bytes per pixel
- Ensure that the size above is divisible by and aligned to 32 bytes.

## Examples

### Basic Example

This is a basic example of minimal use of the PDC in an application. This example shows how this driver can be used for capturing data from an external I/O device such as an image sensor.

```
void g_pdc_user_callback (pdc_callback_args_t * p_args)
{
    if (PDC_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_capture_ready = true;
    }
}

void basic_example (void)
{
    fsp_err_t err;

    /* Initialize the PDC module */
    err = R_PDC_Open(&g_pdc0_ctrl, &g_pdc0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize the camera module at this point. This implementation is camera vendor
specific. */
    camera_module_initialization();

    /* Initialize capture ready flag to false. This gets set to true in PDC callback
upon successful frame capture. */
    g_capture_ready = false;
}
```

```
err = R_PDC_CaptureStart(&g_pdc0_ctrl, g_user_buffer);
assert(FSP_SUCCESS == err);
uint32_t timeout_ms = PDC_DELAY_MS;
/* Since there is nothing else to do, block until Callback triggers*/
while ((true != g_capture_ready) && timeout_ms)
{
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;;
}
if (0U == timeout_ms)
{
    __BKPT(0);
}
}
static void camera_module_initialization (void)
{
/* Camera vendor specific initialization to be done here */
}
```

## Data Structures

struct [pdc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ pdc\_instance\_ctrl\_t

struct pdc\_instance\_ctrl\_t

PDC instance control block. DO NOT INITIALIZE.

## Function Documentation

◆ **R\_PDC\_Open()**

```
fsp_err_t R_PDC_Open ( pdc_ctrl_t *const p_api_ctrl, pdc_cfg_t const *const p_cfg )
```

Powers on PDC, handles required initialization described in the hardware manual.

Implements `pdc_api_t::open`.

The Open function provides initial configuration for the PDC module. It powers on the module and enables the PCLKO output and the PIXCLK input. Further initialization requires the PIXCLK input to be running in order to be able to reset the PDC as part of its initialization. This clock is input from a camera module and so the reset and further initialization is performed in `pdc_api_t::captureStart`. This function should be called once prior to calling any other PDC API functions. After the PDC is opened the Open function should not be called again without first calling the Close function.

Example:

```
/* Initialize the PDC module */
err = R_PDC_Open(&g_pdc0_ctrl, &g_pdc0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	One or more of the following parameters is NULL <ol style="list-style-type: none"> <li>1. p_cfg is NULL</li> <li>2. p_api_ctrl is NULL</li> <li>3. The pointer to the transfer interface in the p_cfg parameter is NULL</li> <li>4. Callback parameter is NULL.</li> <li>5. Invalid IRQ number assigned</li> </ol>
FSP_ERR_INVALID_ARGUMENT	One or more of the following parameters is incorrect <ol style="list-style-type: none"> <li>1. bytes_per_pixel is zero</li> <li>2. x_capture_pixels is zero</li> <li>3. y_capture_pixels is zero</li> <li>4. x_capture_start_pixel + x_capture_pixels is greater than 4095, OR</li> <li>5. y_capture_start_pixel + y_capture_pixels is greater than 4095</li> </ol>
FSP_ERR_ALREADY_OPEN	Module is already open.

◆ **R\_PDC\_Close()**

```
fsp_err_t R_PDC_Close ( pdc_ctrl_t *const p_api_ctrl)
```

Stops and closes the transfer interface, disables and powers off the PDC, clears internal driver data and disables interrupts.

Implements `pdc_api_t::close`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	<code>p_api_ctrl</code> is NULL
FSP_ERR_NOT_OPEN	Open has not been successfully called.

◆ **R\_PDC\_CaptureStart()**

```
fsp_err_t R_PDC_CaptureStart ( pdc_ctrl_t *const p_api_ctrl, uint8_t *const p_buffer )
```

Starts a capture. Enables interrupts.

Implements `pdc_api_t::captureStart`.

Sets up the transfer interface to transfer data from the PDC into the specified buffer. Configures the PDC settings as previously set by the `pdc_api_t::open` API. These settings are configured here as the PIXCLK input must be active for the PDC reset operation. When a capture is complete the callback registered during `pdc_api_t::open` API call will be called.

Example:

```
err = R_PDC_CaptureStart(&g_pdc0_ctrl, g_user_buffer);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Capture start successful.
FSP_ERR_ASSERTION	One or more of the following parameters is NULL <ul style="list-style-type: none"> <li>1. <code>p_api_ctrl</code> is NULL</li> <li>2. <code>p_buffer</code> is NULL while <code>p_buffer</code> field of the control structure is NULL</li> </ul>
FSP_ERR_NOT_OPEN	Open has not been successfully called.
FSP_ERR_IN_USE	PDC transfer is already in progress.
FSP_ERR_TIMEOUT	Reset operation timed out.

## 4.2.39 Port Output Enable for GPT (r\_poeg)

### Modules

#### Functions

`fsp_err_t` `R_POEG_Open` (`poeg_ctrl_t *const p_ctrl`, `poeg_cfg_t const *const p_cfg`)

`fsp_err_t` `R_POEG_StatusGet` (`poeg_ctrl_t *const p_ctrl`, `poeg_status_t *const p_status`)

`fsp_err_t` `R_POEG_CallbackSet` (`poeg_ctrl_t *const p_ctrl`, `void(*p_callback)(poeg_callback_args_t *)`, `void const *const p_context`, `poeg_callback_args_t *const p_callback_memory`)

`fsp_err_t` `R_POEG_OutputDisable` (`poeg_ctrl_t *const p_ctrl`)

`fsp_err_t` `R_POEG_Reset` (`poeg_ctrl_t *const p_ctrl`)

`fsp_err_t` `R_POEG_Close` (`poeg_ctrl_t *const p_ctrl`)

#### Detailed Description

Driver for the POEG peripheral on RA MCUs. This module implements the [POEG Interface](#).

## Overview

The POEG module can be used to configure events to disable GPT GTIOC output pins.

#### Features

The POEG module has the following features:

- Supports disabling GPT output pins based on GTETRGM input pin level.
- Supports disabling GPT output pins based on comparator crossing events (configurable in the [High-Speed Analog Comparator \(r\\_acmphs\)](#) driver).
- Supports disabling GPT output pins when GTIOC pins are the same level (configurable in the [General PWM Timer \(r\\_gpt\)](#) driver).
- Supports disabling GPT output pins when main oscillator stop is detected.
- Supports disabling GPT output pins by software API.
- Supports notifying the application when GPT output pins are disabled by POEG.
- Supports resetting POEG status.

## Configuration

#### Build Time Configurations for r\_poeg

The following build time configurations are defined in `fsp_cfg/r_poeg_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Timers > Port Output Enable for GPT on r\_poeg

This module can be added to the Stacks tab via New Stack > Driver > Timers > Port Output Enable for GPT on r\_poeg. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_poeg0	Module name.
General > Channel	Must be a valid POEG channel	0	Specify the hardware channel.
General > Trigger	MCU Specific Options		Select the trigger sources that will enable POEG. Software disable is always supported. This configuration can only be set once after reset. It cannot be modified after the initial setting.
Input > GTETRGR Polarity	<ul style="list-style-type: none"> <li>Active High</li> <li>Active Low</li> </ul>	Active High	Select the polarity of the GTETRGR pin. Only applicable if GTETRGR pin is selected under Trigger.
Input > GTETRGR Noise Filter	<ul style="list-style-type: none"> <li>Disabled</li> <li>PCLKB/1</li> <li>PCLKB/8</li> <li>PCLKB/32</li> <li>PCLKB/128</li> </ul>	Disabled	Configure the noise filter for the GTETRGR pin. Only applicable if GTETRGR pin is selected under Trigger.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function can be specified here. If this callback function is provided, it will be called from the interrupt service routine (ISR) when GPT output pins are disabled by POEG.
Interrupts > Interrupt Priority	MCU Specific Options		Select the POEG interrupt priority.

### Clock Configuration

The POEG clock is based on the PCLKB frequency.

## Pin Configuration

This module can use GTETRGA, GTETRGB, GTETRGC, or GTETRGD as an input signal to disable GPT output pins.

## Usage Notes

### POEG GTETRGM Pin and Channel

The POEG channel number corresponds to the GTETRGM input pin that can be used with the channel. GTETRGA must be used with POEG channel 0, GTETRGB must be used with POEG channel 1, etc.

### Limitations

The user should be aware of the following limitations when using POEG:

- The POEG trigger source can only be set once per channel. Modifying the POEG trigger source after it is set is not allowed by the hardware.
- The POEG cannot be disabled using this API. The interrupt is disabled in `R_POEG_Close()`, but the POEG will still disable the GPT output pins if a trigger is detected even if the module is closed.

## Examples

### POEG Basic Example

This is a basic example of minimal use of the POEG in an application.

```
void poeg_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the POEG. */
    err = R_POEG_Open(&g_poeg0_ctrl, &g_poeg0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
}
```

### POEG Callback Example

This is an example of a using the POEG callback to restore GPT output operation.

```
/* Example callback called when POEG disables GPT output pins. */
void poeg_callback (poeg_callback_args_t * p_args)
{
```

```
FSP_PARAMETER_NOT_USED(p_args);

/* (Optional) Determine the cause of the POEG event. */
poeg_status_t status;

(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);

/* Correct the cause of the POEG event before resetting POEG. */
/* Reset the POEG before exiting the callback. */
(void) R_POEG_Reset(&g_poeg0_ctrl);

/* Wait for the status to clear after reset before exiting the callback to ensure
the interrupt does not fire
* again. */
do
{
(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
} while (POEG_STATE_NO_DISABLE_REQUEST != status.state);

/* Alternatively, if the POEG cannot be reset, disable the POEG interrupt to prevent
it from firing continuously.
* Update the 0 in the macro below to match the POEG channel number. */
NVIC_DisableIRQ(VECTOR_NUMBER_POEG0_EVENT);
}
```

## Data Structures

struct [poeg\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ poeg\_instance\_ctrl\_t

struct poeg\_instance\_ctrl\_t

Channel control block. DO NOT INITIALIZE. Initialization occurs when [poeg\\_api\\_t::open](#) is called.

## Function Documentation

◆ **R\_POEG\_Open()**

```
fsp_err_t R_POEG_Open ( poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg )
```

Initializes the POEG module and applies configurations. Implements `poeg_api_t::open`.

**Note**

*The `poeg_cfg_t::trigger` setting can only be configured once after reset. Reopening with a different trigger configuration is not possible.*

**Example:**

```
/* Initializes the POEG. */
err = R_POEG_Open(&g_poeg0_ctrl, &g_poeg0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful.
FSP_ERR_ASSERTION	A required input pointer is NULL or the source divider is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_IRQ_BSP_DISABLED	<code>poeg_cfg_t::p_callback</code> is not NULL, but ISR is not enabled. ISR must be enabled to use callback.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel requested in the <code>p_cfg</code> parameter is not available on this device.

◆ **R\_POEG\_StatusGet()**

```
fsp_err_t R_POEG_StatusGet ( poeg_ctrl_t *const p_ctrl, poeg_status_t *const p_status )
```

Get current POEG status and store it in provided pointer `p_status`. Implements `poeg_api_t::statusGet`.

**Example:**

```
/* (Optional) Determine the cause of the POEG event. */
poeg_status_t status;
(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
```

**Return values**

FSP_SUCCESS	Current POEG state stored successfully.
FSP_ERR_ASSERTION	<code>p_ctrl</code> or <code>p_status</code> was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_CallbackSet()**

```
fsp_err_t R_POEG_CallbackSet ( poeg_ctrl_t *const p_ctrl, void(*)(poeg_callback_args_t *)
p_callback, void const *const p_context, poeg_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `poeg_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_POEG\_OutputDisable()**

```
fsp_err_t R_POEG_OutputDisable ( poeg_ctrl_t *const p_ctrl)
```

Disables GPT output pins. Implements `poeg_api_t::outputDisable`.

**Return values**

FSP_SUCCESS	GPT output pins successfully disabled.
FSP_ERR_ASSERTION	<code>p_ctrl</code> was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_Reset()**

```
fsp_err_t R_POEG_Reset ( poeg_ctrl_t *const p_ctrl)
```

Resets status flags. Implements `poeg_api_t::reset`.

**Note**

*Status flags are only reset if the original POEG trigger is resolved. Check the status using `R_POEG_StatusGet` after calling this function to verify the status is cleared.*

**Example:**

```
/* Correct the cause of the POEG event before resetting POEG. */
/* Reset the POEG before exiting the callback. */
(void) R_POEG_Reset(&g_poeg0_ctrl);
/* Wait for the status to clear after reset before exiting the callback to ensure
the interrupt does not fire
* again. */
do
{
(void) R_POEG_StatusGet(&g_poeg0_ctrl, &status);
} while (POEG_STATE_NO_DISABLE_REQUEST != status.state);
```

**Return values**

FSP_SUCCESS	Function attempted to clear status flags.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

◆ **R\_POEG\_Close()**

```
fsp_err_t R_POEG_Close ( poeg_ctrl_t *const p_ctrl)
```

Disables POEG interrupt. Implements `poeg_api_t::close`.

**Note**

*This function does not disable the POEG.*

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	p_ctrl was NULL.
FSP_ERR_NOT_OPEN	The instance is not opened.

## 4.2.40 Precision Time Protocol (r\_ptp)

### Modules

#### Functions

fsp_err_t	R_PTP_Open (ptp_ctrl_t *const p_ctrl, ptp_cfg_t const *const p_cfg)
fsp_err_t	R_PTP_MacAddrSet (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_mac_addr)
fsp_err_t	R_PTP_IpAddrSet (ptp_ctrl_t *const p_ctrl, uint32_t ip_addr)
fsp_err_t	R_PTP_LocalClockIdSet (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id)
fsp_err_t	R_PTP_MasterClockIdSet (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id, uint16_t port_id)
fsp_err_t	R_PTP_MessageFlagsSet (ptp_ctrl_t *const p_ctrl, ptp_message_type_t message_type, ptp_message_flags_t flags)
fsp_err_t	R_PTP_CurrentUtcOffsetSet (ptp_ctrl_t *const p_ctrl, uint16_t offset)
fsp_err_t	R_PTP_PortStateSet (ptp_ctrl_t *const p_ctrl, uint32_t state)
fsp_err_t	R_PTP_MessageSend (ptp_ctrl_t *const p_ctrl, ptp_message_t const *const p_message, uint8_t const *const p_tlv_data, uint16_t tlv_data_size)
fsp_err_t	R_PTP_LocalClockValueSet (ptp_ctrl_t *const p_ctrl, ptp_time_t const *const p_time)
fsp_err_t	R_PTP_LocalClockValueGet (ptp_ctrl_t *const p_ctrl, ptp_time_t *const p_time)
fsp_err_t	R_PTP_PulseTimerCommonConfig (ptp_ctrl_t *const p_ctrl, ptp_pulse_timer_common_cfg_t *const p_timer_cfg)
fsp_err_t	R_PTP_PulseTimerEnable (ptp_ctrl_t *const p_ctrl, uint32_t channel, ptp_pulse_timer_cfg_t *const p_timer_cfg)
fsp_err_t	R_PTP_PulseTimerDisable (ptp_ctrl_t *const p_ctrl, uint32_t channel)
fsp_err_t	R_PTP_Close (ptp_ctrl_t *const p_ctrl)
fsp_err_t	R_PTP_BestMasterClock (ptp_message_t const *const p_announce1, ptp_message_t const *const p_announce2, int8_t *const

p\_comparison)

## Detailed Description

Driver for the PTP peripheral on RA MCUs. This module implements the [PTP Interface](#).

## Overview

PTP allows for multiple devices on a network to synchronize their clocks with very high precision. The PTP peripheral generates and processes PTP messages automatically. In slave mode, it also corrects the local time in order to adjust for any offset from the master clock time.

## Features

- Ordinary clock
  - Master mode
  - Slave mode
- Peer-to-peer
- End-to-end
- Frame formats
  - Ethernet II frames
  - IEEE802.3 + LLC + SNAP frames
  - IPv4 + UDP
- Clock correction modes
  - Mode 1: Add the offsetFromMaster value to the local time whenever it is updated.
  - Mode 2: Calculate a clock gradient and continuously adjust the local time in order to minimize the offsetFromMaster value.

## Configuration

### Build Time Configurations for r\_ptp

The following build time configurations are defined in fsp\_cfg/r\_ptp\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Network > PTP Driver on r\_ptp

This module can be added to the Stacks tab via New Stack > Driver > Network > PTP Driver on r\_ptp.

Configuration	Options	Default	Description
Clock Properties > Priority 1	Value must in the range [0,255].	128	Priority1 field advertised in generated announce packets.
Clock Properties >	Value must in the	248	Class field advertised

Class	range [0,255].		in generated announce packets.
Clock Properties > Accuracy	Value must in the range [0,255].	0xFE	Accuracy field advertised in generated announce packets.
Clock Properties > Variance	Value must in the range [0,65535].	0xFFFF	Variance field advertised in generated announce packets.
Clock Properties > Priority 2	Value must in the range [0,255].	128	Priority2 field advertised in generated announce packets.
Clock Properties > Time Source	Value must in the range [0,255].	160	Time Source field advertised in generated announce packets.
Ethernet > Multicast Filter MAC address	Must be a valid MAC address	01:1B:19:00:00:00	In Multicast Filtered mode, only multicast addresses that match this address are received by the ETHERC EDMAC.
Ethernet > Primary Destination MAC address	Must be a valid MAC address	01:1B:19:00:00:00	The destination MAC address for primary PTP messages.
Ethernet > PDelay Destination MAC address	Must be a valid MAC address	01:80:C2:00:00:0E	The destination MAC address for PDelay messages.
IP > Primary Destination IP address	Must be a valid IP address	224.0.1.129	The destination IPv4 address for primary messages.
IP > PDelay Destination IP address	Must be a valid IP address	224.0.0.107	The destination IPv4 address for PDelay messages.
IP > Event Message TOS	Value must in the range [0,255].	0	The IP packet TOS for event messages.
IP > General Message TOS	Value must in the range [0,255].	0	The IP packet TOS for general messages.
IP > Primary Message TTL	Value must in the range [0,255].	1	The IP packet TTL for primary messages.
IP > PDelay Message TTL	Value must in the range [0,255].	1	The IP packet TTL for p_delay messages.
IP > Event Port	Value must in the range [0,65535].	319	The UDP port for event messages.

IP > General Port	Value must be in the range [0,65535].	320	The UDP port for general messages.
Synchronization Detection > Threshold (Nanoseconds)	Value must be greater than 0.	1000000	The minimum offsetFromMaster value required in order to synchronize with the master clock.
Synchronization Detection > Count	Value must be in the range [0,255].	5	The number of times the calculated offsetFromMaster value must be less than the threshold in order to synchronize with the master clock.
Synchronization Lost Detection > Threshold (Nanoseconds)	Value must be greater than 0.	10000000	The minimum offsetFromMaster value required in order to lose synchronization with the master clock.
Synchronization Lost Detection > Count	Value must be in the range [0,255].	5	The number of times the calculated offsetFromMaster value must be greater than the threshold in order to lose synchronization with the master.
Interrupts > Callback	Name must be a valid C symbol	<code>_\${module.driver.ptp.name}_callback</code>	Called when a STCA/SYNFP event occurs, a PTP message is received, or if a Pulse Timer event occurs.
Interrupts > MINT Interrupt priority	MCU Specific Options		Select the EPTPC MINT interrupt priority.
Interrupts > Pulse Timer Interrupt priority	MCU Specific Options		Select the EPTPC IPLS priority.
Name	Name must be a valid C symbol	<code>g_ptp0</code>	Module name.
Ethernet PHY Interface Type	<ul style="list-style-type: none"> <li>• MII</li> <li>• RMII</li> </ul>	RMII	The interface type used to communicate with the Ethernet PHY.
Frame Filter	<ul style="list-style-type: none"> <li>• Extended Promiscuous Mode</li> <li>• Unicast and Multicast</li> <li>• Unicast and Multicast Filtered</li> <li>• Unicast</li> </ul>	Unicast	Selects how packets are filtered based on their destination MAC address. Packets that pass the filter are transferred to the ETHERC EDMAC.

Frame Format	<ul style="list-style-type: none"> <li>Ethernet II</li> <li>Ethernet II   IPv4   UDP</li> <li>IEEE802.3   LLC   SNAP</li> <li>IEEE802.3   LLC   SNAP   IPv4   UDP</li> </ul>	Ethernet II	The format of the frames that encapsulate the PTP messages.
Clock Domain	Value must in the range [0,255].	0	The PTP clock will only respond to clocks in its domain.
Clock Domain Filter	<ul style="list-style-type: none"> <li>Enable</li> <li>Disable</li> </ul>	Enable	Filter out PTP messages from other clock domains.
Buffer Size	Value must in the range [64,1536].	1536	The maximum Ethernet packet size that can be transmitted or received by the application from the EDMAC.
Number of transmit buffers	Value must in the range [1,16].	4	The number of transmit buffers in the packet queue.
Number of receive buffers	Value must in the range [1,16].	4	The number of receive buffers in the packet queue.
Announce message interval.	MCU Specific Options		The period of time between generated announce messages.
Sync message interval.	MCU Specific Options		The period of time between generated sync messages.
Delay_req message interval.	MCU Specific Options		The period of time between generated delay_req messages.
Message timeout	Value must be greater than 0.	4000	The time in milliseconds needed to generate timeout events after not receiving a sync or delay_resp message.
Clock Source	<ul style="list-style-type: none"> <li>PCLKA / 1</li> <li>PCLKA / 2</li> <li>PCLKA / 3</li> <li>PCLKA / 4</li> <li>PCLKA / 5</li> <li>PCLKA / 6</li> <li>REF50CK0</li> </ul>	PCLKA / 6	The STCA clock source must be 20Mhz, 25Mhz, 50Mhz, or 100Mhz. When REF50CK0 is selected, the STCA frequency is 25Mhz.
Clock Correction Mode	<ul style="list-style-type: none"> <li>Clock</li> </ul>	Clock Correction Mode	Clock correction mode

	Correction Mode 1	1	1 corrects the local clock using the current <code>offsetFromMaster</code> value. Clock correction mode 2 calculates a clock gradient in order to continuously correct the local clock.
	• Clock Correction Mode 2		
Gradient Worst10 Interval	Value must in the range [0,255].	32	The number of sync messages to use when calculating the worst10 gradient values (Only applies to clock correction mode 2).

## Clock Configuration

The STCA input clock can be the following clock sources:

- PCLKA / 1
- PCLKA / 2
- PCLKA / 3
- PCLKA / 4
- PCLKA / 5
- PCLKA / 6
- REF50CK0

The STCA input clock is restricted to the following frequencies:

- 20 Mhz
- 25 Mhz
- 50 Mhz
- 100 Mhz

When REF50CK0 is selected, the input clock frequency is 25 Mhz.

## Pin Configuration

The PTP module requires the [Ethernet \(r\\_ether\)](#) instance in order to initialize the Ethernet PHY. This means that the ETHERC pins must be configured.

## Usage Notes

### PTP Port State

The current PTP port state determines which messages need to be generated and processed by the PTP peripheral. It is the application's responsibility to determine what the current state of the PTP port should be.

The following messages can be generated by the PTP peripheral:

- Announce
- Sync
- Delay\_req

- Delay\_resp
- PDelay\_req
- PDelay\_resp

The following messages can be processed by the PTP peripheral:

- Sync
- Follow\_up
- Delay\_req
- Delay\_resp
- PDelay\_req
- PDelay\_resp
- PDelay\_resp\_follow\_up

The application must receive the following messages in order to determine the current state of its PTP port:

- Announce
- Management
- Signaling

The following messages can only be sent manually:

- Management
- Signaling

The PTP API defines the following states:

State	Generated Messages	Processed Messages	Received Messages
Disabled	N/A	N/A	N/A
Passive	N/A	N/A	Announce, Signaling, Management
E2E/P2P Slave	Delay_req/(PDelay_req, PDelay_resp)	Sync, Follow_up, Delay_resp/(PDelay_req, PDelay_resp)	Announce, Signaling, Management
E2E/P2P Master	Announce, Sync, Delay_resp/(PDelay_req, PDelay_resp)	delay_req/(PDelay_req, PDelay_resp)	Announce, Signaling, Management

## Pulse Timers

Pulse Timers are configurable timers used to generate interrupts and ELC events. Each pulse timer has a configurable start time, pulse, and period. At the start of each timer period, a rising edge occurs. After the pulse time has elapsed, a falling edge occurs. ELC events and IRQs can be generated on rising and/or falling edges for each Pulse Timer. There are two types of interrupts generated by each Pulse Timer; MINT and IPLS.

## MINT Interrupts

MINT IRQs are only generated on the rising edge of a Pulse Timer channel. The callback will provide the channel number of the pulse timer that caused the interrupt.

## IPLS Interrupts

Each Pulse Timer channel can be configured as a source for generating IPLS IRQs. All of the pulse timers that are selected as IPLS sources are OR'd together and rising and falling edge IRQs can be generated from the resulting signal. Below is an example of a resulting signal from two IPLS sources. Unlike MINT interrupts, IPLS interrupts do not provide any information about which Pulse Timer caused the IRQ because the IRQs from all the Pulse Timers are OR'd together.

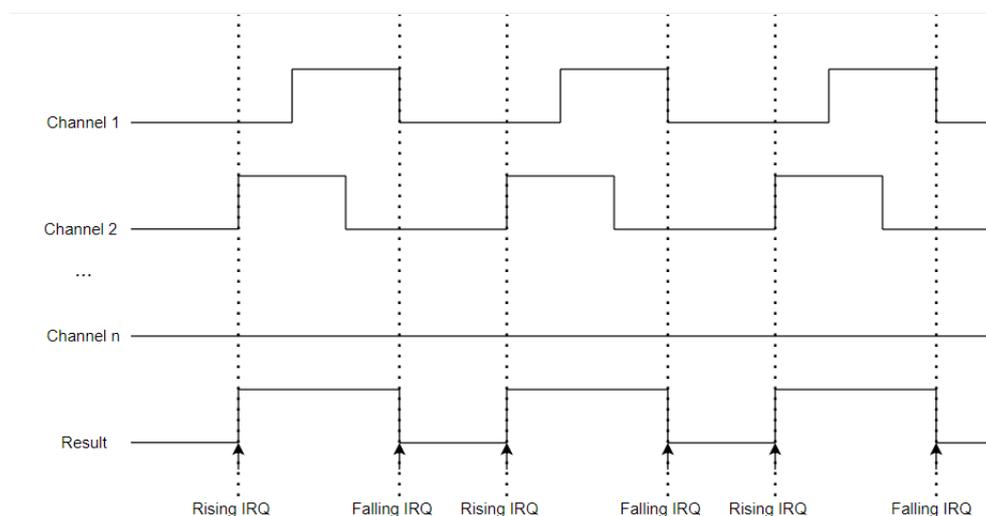


Figure 166: IPLS IRQ Generation

## Ethernet Frame Filter

The PTP driver can filter Ethernet frames that are received by [Ethernet \(r\\_ether\)](#). There are four different filtering modes:

- Extended Promiscuous - All Ethernet frames are received by [Ethernet \(r\\_ether\)](#).
- Unicast and Multicast - All Unicast frames destined for the PTP and Multicast frames are received by [Ethernet \(r\\_ether\)](#).
- Unicast and Multicast Filtered - All Unicast frames destined for the PTP are received by [Ethernet \(r\\_ether\)](#). All multicast frames that match `ptp_synfp_cfg_t::p_multicast_addr_filter` are received by [Ethernet \(r\\_ether\)](#).
- Unicast - Only Unicast frames destined for the PTP are received by [Ethernet \(r\\_ether\)](#).

## Limitations

Developers should be aware of the following limitations when using the PTP:

- PTP will not automatically initialize [Ethernet \(r\\_ether\)](#). This provides flexibility by allowing PTP to be used alongside 3rd party IP stacks (Eg. [FreeRTOS Plus TCP \(rm\\_freertos\\_plus\\_tcp\)](#)), however this means the application must execute the [Ethernet \(r\\_ether\)](#) link process in order to use PTP.
- The driver will not detect announce message timeouts. This functionality must be handled by the application.
- When IP + UDP frame format is selected, the driver will not automatically join the multicast group. This must be done by the application.
- In order to call PTP API functions from ISRs, the MINT and IPLS interrupt priorities must be configured to be lower than `BSP_CFG_IRQ_MASK_LEVEL_FOR_CRITICAL_SECTION`. This is to guarantee that PTP register accesses are atomic.

## Examples

### Slave Mode

This is a basic example of minimal use of PTP in slave mode.

```
volatile bool g_first_announce_message_received = false;
volatile bool g_sync_acquired = false;
void slave_mode_basic_example (void)
{
    /* The PTP Instance must be opened before R_ETHER is opened. */
    fsp_err_t err = R_PTP_Open(&g_ptp_ctrl, &g_ptp_cfg);
    assert(FSP_SUCCESS == err);
    /* Configure the PTP MAC address. */
    err = R_PTP_MacAddrSet(&g_ptp_ctrl, g_ptp_mac_address);
    assert(FSP_SUCCESS == err);
    /* Configure the PTP Local Clock ID (Usually generated from MAC address). */
    err = R_PTP_LocalClockIdSet(&g_ptp_ctrl, g_ptp_clock_id);
    assert(FSP_SUCCESS == err);
    /* Open the r_ether_api instance. */
    err = R_ETHER_Open(&g_ether_ctrl, &g_ether_cfg);
    assert(FSP_SUCCESS == err);
    /* Wait for the link to be established. */
    do
    {
        err = R_ETHER_LinkProcess(&g_ether_ctrl);
    } while (FSP_SUCCESS != err);
    /* Set the PTP instance to passive state and listen for announce message. */
    err = R_PTP_PortStateSet(&g_ptp_ctrl, PTP_PORT_STATE_PASSIVE);
    assert(FSP_SUCCESS == err);
    /* Wait for the first announce message (This will provide the master clock ID). */
    uint32_t timeout = EXAMPLE_TIMEOUT;
    while (!g_first_announce_message_received && --timeout)
    {
        R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_SECONDS);
    }
}
```

```
    assert(0U != timeout);

/* When a master clock is found, change to the slave state to start synchronizing
 * the local clock to the master clock. */

    err = R_PTP_PortStateSet(&g_ptp_ctrl, PTP_PORT_STATE_E2E_SLAVE);
    assert(FSP_SUCCESS == err);

/* Wait for local clock to be synchronized with the master clock. */

    timeout = EXAMPLE_TIMEOUT;

while (!g_sync_acquired && --timeout)
    {
R_BSP_SoftwareDelay(1, BSP_DELAY_UNITS_SECONDS);
    }

    assert(0U != timeout);

/* The local clock is now synchronized with the grand master clock. */
}

/* Callback called whenever a PTP event occurs. */
void g_ptp_slave_callback_example (ptp_callback_args_t * p_args)
{
    switch (p_args->event)
    {
    case PTP_EVENT_SYNC_ACQUIRED:
        {
/* The offsetFromMaster value is now within the configured threshold to be
 * synchronized with the master clock.
 */

            g_sync_acquired = true;

        break;
        }
    case PTP_EVENT_MESSAGE_RECEIVED:
        {
static ptp_message_t g_current_master_announce_message;
switch (p_args->p_message->header.message_type)
    {
case PTP_MESSAGE_TYPE_ANNOUNCE:
        {
```

```
        int8_t comparison = 0;
    if (!g_first_announce_message_received)
    {
        /* If this is the first announce packet, immediately switch to this master clock. */
        comparison = 1;
        g_first_announce_message_received = true;
    }
    else
    {
        /*
         * Run the "Best Master Clock Algorithm" to determine if the clock defined in this
        announce
         * packet is better than the current master clock.
         */
        fsp_err_t err = R_PTP_BestMasterClock(&g_current_master_announce_message,
                                             p_args->p_message,
                                             &comparison);

        assert(FSP_SUCCESS == err);
    }
    if (1 == comparison)
    {
        /* Save the message as the new master announce message. */
        g_current_master_announce_message = *p_args->p_message;
        /* Set the master clock ID and sourcePortID in the PTP instance so that it
         * synchronizes with the new best master clock.
         */
        fsp_err_t err = R_PTP_MasterClockIdSet(&g_ptp_ctrl,
                                              g_current_master_annou
nce_message.header.clock_id,
                                              g_current_master_annou
nce_message.header.source_port_id);
        assert(FSP_SUCCESS == err);
    }
    break;
```

```
    }  
default:  
    {  
break;  
    }  
    }  
break;  
    }  
default:  
    {  
break;  
    }  
    }  
}
```

## Master Mode

This is a basic example of minimal use of PTP in master mode.

```
#define PTP_EXAMPLE_CURRENT_UTC_OFFSET (37)  
void master_mode_basic_example (void)  
{  
    /* The PTP Instance must be opened before R_ETHER is opened. */  
    fsp_err_t err = R_PTP_Open(&g_ptp_ctrl, &g_ptp_cfg);  
    assert(FSP_SUCCESS == err);  
    /* Configure the PTP MAC address. */  
    err = R_PTP_MacAddrSet(&g_ptp_ctrl, g_ptp_mac_address);  
    assert(FSP_SUCCESS == err);  
    /* Configure the PTP Local Clock ID (Usually generated from MAC address). */  
    err = R_PTP_LocalClockIdSet(&g_ptp_ctrl, g_ptp_clock_id);  
    assert(FSP_SUCCESS == err);  
    /* Get the current time from an external time source (Eg. RTC). */  
    ptp_time_t current_time;  
    get_current_time_example(&current_time);  
    /* Set the PTP local time to the current time. */
```

```
err = R_PTP_LocalClockValueSet(&g_ptp_ctrl, &current_time);
assert(FSP_SUCCESS == err);

/* Set the currentUtcOffset field in announce messages. */
err = R_PTP_CurrentUtcOffsetSet(&g_ptp_ctrl, PTP_EXAMPLE_CURRENT_UTC_OFFSET);
assert(FSP_SUCCESS == err);

/* Set message flags in announce messages to indicate that the current UTC offset is
valid and that the PTP timescale is used. */
ptp_message_flags_t flags;

flags.value = 0;
flags.value_b.currentUtcOffsetValid = 1;
flags.value_b.ptpTimescale          = 1;
err = R_PTP_MessageFlagsSet(&g_ptp_ctrl, PTP_MESSAGE_TYPE_ANNOUNCE, flags);
assert(FSP_SUCCESS == err);

/* Open the r_ether_api instance. */
err = R_ETHER_Open(&g_ether_ctrl, &g_ether_cfg);
assert(FSP_SUCCESS == err);

/* Wait for the link to be established. */
do
{
    err = R_ETHER_LinkProcess(&g_ether_ctrl);
} while (FSP_SUCCESS != err);

/* Set the PTP instance to passive state and listen for announce message. */
err = R_PTP_PortStateSet(&g_ptp_ctrl, PTP_PORT_STATE_E2E_MASTER);
assert(FSP_SUCCESS == err);

/*
 * The master clock is now operational and will automatically generate announce and
sync messages
 * as well as respond to delay_req messages.
 */
}
```

## Send PTP Messages

This is a basic example of how to send PTP messages.

```
#define PTP_MANAGEMENT_ACTION_GET (0U)
#define PTP_TLV_TYPE_MANAGEMENT (1U)
#define PTP_TLV_MANAGEMENT_ID_CLOCK_DESCRIPTION (1U)

static uint32_t g_transmit_complete = 0U;

void send_message_example (void)
{
    static ptp_message_t message;
    static uint8_t      p_tlv_data[6];

    memset(&message, 0, sizeof(ptp_message_t));

    /* Fill in the required fields for the message header (Note that appropriate fields
will be endian swapped). */
    message.header.message_type = PTP_MESSAGE_TYPE_MANAGEMENT;
    message.header.version      = 2;

    /* The message length is the total number of bytes in the PTP message (Including the
message header). */
    message.header.message_length = (uint16_t) (sizeof(ptp_message_header_t) +
sizeof(ptp_message_management_t) +
sizeof(p_tlv_data));

    memcpy(message.header.clock_id, g_ptp_clock_id, sizeof(g_ptp_clock_id));
    message.header.control_field = PTP_CTRL_FIELD_MANAGEMENT;

    /* Fill in the required fields for the management message. */
    memcpy(message.management.target_clock_id, g_target_clock_id, sizeof
(g_target_clock_id));

    message.management.target_port_id      = 1;
    message.management.starting_boundary_hops = 1;
    message.management.boundary_hops      = 1;
    message.management.action              = PTP_MANAGEMENT_ACTION_GET;

    /*
    * Fill in TLV data (Note that TLV data is big endian).
    *
    * Type (Management)
    */
    p_tlv_data[0] = 0;
    p_tlv_data[1] = PTP_TLV_TYPE_MANAGEMENT;
```

```
/* Length */
p_tlv_data[2] = 0;
p_tlv_data[3] = 2;

/* Management ID (Clock Description) */
p_tlv_data[4] = 0;
p_tlv_data[5] = PTP_TLV_MANAGEMENT_ID_CLOCK_DESCRIPTION;

/* Send the message. */
fsp_err_t err = R_PTP_MessageSend(&g_ptp_ctrl, &message, p_tlv_data, sizeof
(p_tlv_data));

assert(FSP_SUCCESS == err);

uint32_t timeout = EXAMPLE_TIMEOUT;

while (0U == g_transmit_complete && --timeout)
{
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MICROSECONDS);
}

/* Callback called whenever a PTP event occurs. */
void g_ptp_send_message_callback_example (ptp_callback_args_t * p_args)
{
    switch (p_args->event)
    {
        case PTP_EVENT_MESSAGE_TRANSMIT_COMPLETE:
            {
                g_transmit_complete = 1U;
            }
            break;

        case PTP_EVENT_MESSAGE_RECEIVED:
            {
                switch (p_args->p_message->header.message_type)
                {
                    case PTP_MESSAGE_TYPE_MANAGEMENT:
                        {
                            /* Handle the response message. */
                        }
                    }
                }
            }
            break;
    }
}
```

```

    }
    default:
    {
    break;
    }
    }
    }
    default:
    {
    break;
    }
    }
}

```

## Data Structures

struct [ptp\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ ptp\_instance\_ctrl\_t

struct ptp_instance_ctrl_t		
PTP instance control block.		
Data Fields		
uint32_t	open	Marks if the instance has been opened.
uint32_t	tx_buffer_write_index	Index into the descriptor list to write the next packet.
uint32_t	tx_buffer_complete_index	Index into the descriptor list of the last transmitted packet.
uint32_t	rx_buffer_index	Index into the descriptor of the last received packet.
uint32_t	tslatr	Keep track of whether tslatr was set.
<a href="#">ptp_cfg_t</a> const *	p_cfg	Pointer to the configuration structure.

## Function Documentation

## ◆ R\_PTP\_Open()

```
fsp_err_t R_PTP_Open ( ptp_ctrl_t *const p_ctrl, ptp_cfg_t const *const p_cfg )
```

This function initializes PTP. Implements `ptp_api_t::open`.

This function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Configures the peripheral registers according to the configuration.
- Initialize the control structure for use in other [PTP Interface](#) functions.

**Return values**

FSP_SUCCESS	The instance has been successfully configured.
FSP_ERR_ALREADY_OPEN	Instance was already initialized.
FSP_ERR_NOT_OPEN	The EDMAC instance was not opened correctly.
FSP_ERR_ASSERTION	An invalid argument was given in the configuration structure.

## ◆ R\_PTP\_MacAddrSet()

```
fsp_err_t R_PTP_MacAddrSet ( ptp_ctrl_t *const p_ctrl, uint8_t const *const p_mac_addr )
```

This function sets the MAC address for the PTP instance. Implements `ptp_api_t::macAddrSet`.

*Note*

*This function may only be called while the PTP instance is in `ptp_port_state_t::PTP_PORT_STATE_DISABLE`.*

**Return values**

FSP_SUCCESS	The MAC address has been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_INVALID_MODE	The instance is not in the correct state.

◆ **R\_PTP\_IpAddrSet()**

```
fsp_err_t R_PTP_IpAddrSet ( ptp_ctrl_t *const p_ctrl, uint32_t ip_addr )
```

This function sets the IP address for the PTP instance. Implements [ptp\\_api\\_t::ipAddrSet](#).

**Note**

*This function may only be called while the PTP instance is in [ptp\\_port\\_state\\_t::PTP\\_PORT\\_STATE\\_DISABLE](#).*

**Return values**

FSP_SUCCESS	The IP address has been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL.
FSP_ERR_INVALID_MODE	The configured <a href="#">ptp_synfp_cfg_t::frame_format</a> is not configured to use IP packets, or the instance is not in the correct state.

◆ **R\_PTP\_LocalClockIdSet()**

```
fsp_err_t R_PTP_LocalClockIdSet ( ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id )
```

This function sets the local clock ID for the PTP instance. Implements [ptp\\_api\\_t::localClockIdSet](#).

**Note**

*This function may only be called while the PTP instance is in [ptp\\_port\\_state\\_t::PTP\\_PORT\\_STATE\\_DISABLE](#). Typically the clock ID is derived from the MAC address (E.g. {b1,b2,b3,0xFF,0xFE,b4,b5,b6}).*

**Return values**

FSP_SUCCESS	The local clock ID has been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL
FSP_ERR_INVALID_MODE	The instance is not in the correct state.

◆ **R\_PTP\_MasterClockIdSet()**

```
fsp_err_t R_PTP_MasterClockIdSet ( ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id,
uint16_t port_id )
```

This function sets the master clock ID and port ID that the local clock will synchronize with. Implements [ptp\\_api\\_t::masterClockIdSet](#).

**Return values**

FSP_SUCCESS	The master clock ID and port ID have been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL

◆ **R\_PTP\_MessageFlagsSet()**

```
fsp_err_t R_PTP_MessageFlagsSet ( ptp_ctrl_t *const p_ctrl, ptp_message_type_t message_type,
ptp_message_flags_t flags )
```

This function sets the flags field for the given message type. Implements [ptp\\_api\\_t::messageFlagsSet](#).

**Return values**

FSP_SUCCESS	The master clock ID and port ID have been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_CurrentUtcOffsetSet()**

```
fsp_err_t R_PTP_CurrentUtcOffsetSet ( ptp_ctrl_t *const p_ctrl, uint16_t offset )
```

This function sets the currentUtcOffset value in announce messages. [ptp\\_api\\_t::currentUtcOffsetSet](#).

**Return values**

FSP_SUCCESS	The currentUtcOffset has been updated.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_PortStateSet()**

```
fsp_err_t R_PTP_PortStateSet ( ptp_ctrl_t *const p_ctrl, uint32_t state )
```

This function changes the current state of the PTP instance. Implements `ptp_api_t::portStateSet`.

**Return values**

FSP_SUCCESS	The instance will transition to the new state.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL

◆ **R\_PTP\_MessageSend()**

```
fsp_err_t R_PTP_MessageSend ( ptp_ctrl_t *const p_ctrl, ptp_message_t const *const p_message,
uint8_t const *const p_tlv_data, uint16_t tlv_data_size )
```

This function sends a PTP message. `ptp_api_t::messageSend`.

**Return values**

FSP_SUCCESS	The packet has been written to the transmit descriptor.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.
FSP_ERR_ETHER_ERROR_TRANSMIT_BUFFER_FULL	There is no space for the packet in the transmit queue.

◆ **R\_PTP\_LocalClockValueSet()**

```
fsp_err_t R_PTP_LocalClockValueSet ( ptp_ctrl_t *const p_ctrl, ptp_time_t const *const p_time )
```

This function sets the local clock value. Implements `ptp_api_t::localClockValueSet`.

**Return values**

FSP_SUCCESS	The local clock value has been set.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_LocalClockValueGet()**

```
fsp_err_t R_PTP_LocalClockValueGet ( ptp_ctrl_t *const p_ctrl, ptp_time_t *const p_time )
```

This function gets the local clock value. Implements `ptp_api_t::localClockValueGet`.

**Return values**

FSP_SUCCESS	The local clock value has been written in p_time.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL

◆ **R\_PTP\_PulseTimerCommonConfig()**

```
fsp_err_t R_PTP_PulseTimerCommonConfig ( ptp_ctrl_t *const p_ctrl,
ptp_pulse_timer_common_cfg_t *const p_timer_cfg )
```

This function configures IPLS IRQ settings that are common to all pulse timer channels. Implements `ptp_api_t::pulseTimerCommonConfig`.

**Return values**

FSP_SUCCESS	The pulse timer has been enabled.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_PulseTimerEnable()**

```
fsp_err_t R_PTP_PulseTimerEnable ( ptp_ctrl_t *const p_ctrl, uint32_t channel,
ptp_pulse_timer_cfg_t *const p_timer_cfg )
```

This function enables a pulse timer channel. Implements `ptp_api_t::pulseTimerEnable`.

**Return values**

FSP_SUCCESS	The pulse timer has been enabled.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_PulseTimerDisable()**

```
fsp_err_t R_PTP_PulseTimerDisable ( ptp_ctrl_t *const p_ctrl, uint32_t channel )
```

This function disables a pulse timer channel. Implements `ptp_api_t::pulseTimerDisable`.

**Return values**

FSP_SUCCESS	The pulse timer has been disabled.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_Close()**

```
fsp_err_t R_PTP_Close ( ptp_ctrl_t *const p_ctrl)
```

Disable the PTP instance. Implements `ptp_api_t::close`.

**Return values**

FSP_SUCCESS	The pulse timer has been disabled.
FSP_ERR_NOT_OPEN	The instance has not been opened.
FSP_ERR_ASSERTION	An argument was NULL or invalid.

◆ **R\_PTP\_BestMasterClock()**

```
fsp_err_t R_PTP_BestMasterClock ( ptp_message_t const *const p_announce1, ptp_message_t const *const p_announce2, int8_t *const p_comparison )
```

This function compares two clocks to determine which one is the better master clock.

`p_comparison`:

- Set to -1 if `p_announce1` defines the best master clock.
- Set to 1 if `p_announce2` defines the best master clock.
- Set to 0 if `p_announce1` and `p_announce2` define the same clock.

**Return values**

FSP_SUCCESS	The valid result has been written to <code>p_use_announce_clock</code> .
FSP_ERR_ASSERTION	An argument was NULL.

**4.2.41 Quad Serial Peripheral Interface Flash (r\_qspi)**

## Modules

### Functions

fsp_err_t	R_QSPI_Open (spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
fsp_err_t	R_QSPI_Close (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_QSPI_DirectWrite (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
fsp_err_t	R_QSPI_DirectRead (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t	R_QSPI_SpiProtocolSet (spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
fsp_err_t	R_QSPI_XipEnter (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_QSPI_XipExit (spi_flash_ctrl_t *p_ctrl)
fsp_err_t	R_QSPI_Write (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
fsp_err_t	R_QSPI_Erase (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
fsp_err_t	R_QSPI_StatusGet (spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
fsp_err_t	R_QSPI_BankSet (spi_flash_ctrl_t *p_ctrl, uint32_t bank)

### Detailed Description

Driver for the QSPI peripheral on RA MCUs. This module implements the [SPI Flash Interface](#).

## Overview

### Features

The QSPI driver has the following key features:

- Memory mapped read access to the QSPI flash
- Programming the QSPI flash device
- Erasing the QSPI flash device
- Sending device specific commands and reading back responses
- Entering and exiting QPI mode
- Entering and exiting XIP mode
- 3 or 4 byte addressing

## Configuration

### Build Time Configurations for r\_qspi

The following build time configurations are defined in driver/r\_qspi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support Multiple Line Program in Extended SPI Mode	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If selected code for programming on multiple lines in extended SPI mode is included in the build.

### Configurations for Driver > Storage > QSPI Driver on r\_qspi

This module can be added to the Stacks tab via New Stack > Driver > Storage > QSPI Driver on r\_qspi.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_qspi0	Module name.
General > SPI Protocol	<ul style="list-style-type: none"> <li>Extended SPI</li> <li>QPI</li> </ul>	Extended SPI	Select the initial SPI protocol. SPI protocol can be changed in R_QSPI_Direct().
General > Address Bytes	<ul style="list-style-type: none"> <li>3</li> <li>4</li> <li>4 with 4-byte read code</li> </ul>	3	Select the number of address bytes. Selecting '4 with 4-byte read code' converts the default read code determined in Read Mode to the 4-byte version. If 4-byte mode is selected without using 4-byte commands, the application must issue the EN4B command using R_QSPI_Direct().
General > Read Mode	<ul style="list-style-type: none"> <li>Standard Read</li> <li>Fast Read</li> <li>Fast Read Dual Output</li> <li>Fast Read Dual I/O</li> <li>Fast Read Quad Output</li> </ul>	Fast Read Quad I/O	Select the read mode for memory mapped access.

- Fast Read Quad I/O

General > Dummy Clocks for Fast Read	Refer to the RA Configuration tool for available options.	Default	Select the number of dummy clocks for fast read operations. Default is 6 clocks for Fast Read Quad I/O, 4 clocks for Fast Read Dual I/O, and 8 clocks for other fast read instructions including Fast Read Quad Output, Fast Read Dual Output, and Fast Read
General > Page Size Bytes	Must be an integer greater than 0	256	The maximum number of bytes allowed for a single write.
Command Definitions > Page Program Command	Must be an 8-bit QSPI Page Program Command under Command Definitions	0x02	The command to program a page. If 'Support Multiple Line Program in Extended SPI Mode' is Enabled, this command must use the same number of data lines as the selected read mode.
Command Definitions > Page Program Address Lines	<ul style="list-style-type: none"> <li>• 1</li> <li>• 2</li> <li>• 4</li> </ul>	1	Select the number of lines to use for the address bytes during write operations. This can be determined by referencing the datasheet for the external QSPI. It should either be 1 or match the number of data lines used for memory mapped fast read operations.
Command Definitions > Write Enable Command	Must be an 8-bit QSPI Write Enable Command under Command Definitions	0x06	The command to enable write.
Command Definitions > Status Command	Must be an 8-bit QSPI Status Command under Command Definitions	0x05	The command to query the status of a write or erase command.
Command Definitions > Write Status Bit	Must be an integer between 0 and 7	0	Which bit contains the write in progress status returned from the Write Status Command.

Command Definitions > Sector Erase Command	Must be an 8-bit QSPI Sector Erase Command under Command Definitions	0x20	The command to erase a sector. Set Sector Erase Size to 0 if unused.
Command Definitions > Sector Erase Size	Must be an integer greater than or equal to 0	4096	The sector erase size. Set Sector Erase Size to 0 if Sector Erase is not supported.
Command Definitions > Block Erase Command	Must be an 8-bit QSPI Block Erase Command under Command Definitions	0xD8	The command to erase a block. Set Block Erase Size to 0 if unused.
Command Definitions > Block Erase Size	Must be an integer greater than or equal to 0	65536	The block erase size. Set Block Erase Size to 0 if Block Erase is not supported.
Command Definitions > Block Erase 32KB Command	Must be an 8-bit QSPI Block Erase 32KB Command under Command Definitions	0x52	The command to erase a 32KB block. Set Block Erase Size to 0 if unused.
Command Definitions > Block Erase 32KB Size	Must be an integer greater than or equal to 0	32768	The block erase 32KB size. Set Block Erase 32KB Size to 0 if Block Erase 32KB is not supported.
Command Definitions > Chip Erase Command	Must be an 8-bit QSPI Chip Erase Command under Command Definitions	0xC7	The command to erase the entire chip. Set Chip Erase Command to 0 if unused.
Command Definitions > XIP Enter M7-M0	Must be an 8-bit QSPI XIP Enter M7-M0 command under Command Definitions	0x20	How to set M7-M0 to enter XIP mode.
Command Definitions > XIP Exit M7-M0	Must be an 8-bit QSPI XIP Exit M7-M0 command under Command Definitions	0xFF	How to set M7-M0 exit XIP mode.
Bus Timing > QSPKCLK Divisor	Refer to the RA Configuration tool for available options.	2	Select the divisor to apply to PCLK to get QSPCLK.
Bus Timing > Minimum QSSL Deselect Cycles	Refer to the RA Configuration tool for available options.	4 QSPCLK	Define the minimum number of QSPCLK cycles for QSSL to remain high between operations.

## Clock Configuration

The QSPI clock is derived from PCLKA.

## Pin Configuration

The following pins are available to connect to an external QSPI device:

- QSPCLK: QSPI clock output
- QSSL: QSPI slave select
- QIO0: Data 0 I/O
- QIO1: Data 1 I/O
- QIO2: Data 2 I/O
- QIO3: Data 3 I/O

*Note*

*It is recommended to configure the pins with IOPORT\_CFG\_DRIVE\_HIGH.*

## Usage Notes

### QSPI Memory Mapped Access

After `R_QSPI_Open()` completes successfully, the QSPI flash device contents are mapped to address 0x60000000 and can be read like on-chip flash.

### Limitations

Developers should be aware of the following limitations when using the QSPI driver:

- Only P305-P310 are currently supported by the J-Link driver to flash the QSPI.
- The default J-Link downloader requires the device to be in extended SPI mode (not QPI mode).

## Examples

### Basic Example

This is a basic example of minimal use of the QSPI in an application.

```
#define QSPI_EXAMPLE_DATA_LENGTH (1024)
uint8_t g_dest[QSPI_EXAMPLE_DATA_LENGTH];
/* Place data in the .qspi_flash section to flash it during programming. */
const uint8_t g_src[QSPI_EXAMPLE_DATA_LENGTH] BSP_PLACE_IN_SECTION(".qspi_flash") =
"ABCDEFGHIJKLMNPOQRSTUVWXYZ";
/* Place code in the .code_in_qspi section to flash it during programming. */
void r_qspi_example_function(void) BSP_PLACE_IN_SECTION(".code_in_qspi")
__attribute__((noinline));
void r_qspi_example_function (void)
{
```

```
/* Add code here. */
}
void r_qspi_basic_example (void)
{
/* Open the QSPI instance. */
fsp_err_t err = R_QSPI_Open(&g_qspi0_ctrl, &g_qspi0_cfg);
assert(FSP_SUCCESS == err);
/* (Optional) Send device specific initialization commands. */
r_qspi_example_init();
/* After R_QSPI_Open() and any required device specific initialization, data can be
read directly from the QSPI flash. */
memcpy(&g_dest[0], &g_src[0], QSPI_EXAMPLE_DATA_LENGTH);
/* After R_QSPI_Open() and any required device specific initialization, functions in
the QSPI flash can be called. */
r_qspi_example_function();
}
```

## Initialization Command Structure Example

This is an example of the types of commands that can be used to initialize the QSPI.

```
#define QSPI_COMMAND_WRITE_ENABLE (0x06U)
#define QSPI_COMMAND_WRITE_STATUS_REGISTER (0x01U)
#define QSPI_COMMAND_ENTER_QPI_MODE (0x38U)
#define QSPI_EXAMPLE_STATUS_REGISTER_1 (0x40)
#define QSPI_EXAMPLE_STATUS_REGISTER_2 (0x00)
static void r_qspi_example_init (void)
{
/* Write status registers */
/* Write one byte to enable writing to the status register, then deassert QSSL. */
uint8_t data[4];
fsp_err_t err;
data[0] = QSPI_COMMAND_WRITE_ENABLE;
err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, false);
assert(FSP_SUCCESS == err);
```

```

/* Write 3 bytes, including the write status register command followed by values for
both status registers. In the
* status registers, set QE to 1 and other bits to their default setting. After all
data is written, deassert the
* QSSL line. */
data[0] = QSPI_COMMAND_WRITE_STATUS_REGISTER;
data[1] = QSPI_EXAMPLE_STATUS_REGISTER_1;
data[2] = QSPI_EXAMPLE_STATUS_REGISTER_2;
err     = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 3, false);
assert(FSP_SUCCESS == err);
/* Wait for status register to update. */
spi_flash_status_t status;
do
{
    (void) R_QSPI_StatusGet(&g_qspi0_ctrl, &status);
} while (true == status.write_in_progress);
/* Write one byte to enter QSPI mode, then deassert QSSL. After entering QPI mode on
the device, change the SPI
* protocol to QPI mode on the MCU peripheral. */
data[0] = QSPI_COMMAND_ENTER_QPI_MODE;
err     = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, false);
assert(FSP_SUCCESS == err);
(void) R_QSPI_SpiProtocolSet(&g_qspi0_ctrl, SPI_FLASH_PROTOCOL_QPI);
}

```

### Reading Status Register Example (R\_QSPI\_DirectWrite, R\_QSPI\_DirectRead)

This is an example of using R\_QSPI\_DirectWrite followed by R\_QSPI\_DirectRead to send the read status register command and read back the status register from the device.

```

#define QSPI_COMMAND_READ_STATUS_REGISTER (0x05U)
void r_qspi_direct_example (void)
{
    /* Read a status register. */
    /* Write one byte to read the status register. Do not deassert QSSL. */

```

```
uint8_t data;

fsp_err_t err;

data = QSPI_COMMAND_READ_STATUS_REGISTER;

err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data, 1, true);

assert(FSP_SUCCESS == err);

/* Read one byte. After all data is read, deassert the QSSL line. */

err = R_QSPI_DirectRead(&g_qspi0_ctrl, &data, 1);

assert(FSP_SUCCESS == err);

/* Status register contents are available in variable 'data'. */
}
```

### Querying Device Size Example (R\_QSPI\_DirectWrite, R\_QSPI\_DirectRead)

This is an example of using R\_QSPI\_DirectWrite followed by R\_QSPI\_DirectRead to query the device size.

```
#define QSPI_EXAMPLE_COMMAND_READ_ID (0x9F)
#define QSPI_EXAMPLE_COMMAND_READ_SFDP (0x5A)

void r_qspi_size_example (void)
{
    /* Many QSPI devices support more than one way to query the device size. Consult the
    datasheet for your
    * QSPI device to determine which of these methods are supported (if any). */
    uint32_t device_size_bytes;

    fsp_err_t err;

#ifdef QSPI_EXAMPLE_COMMAND_READ_ID
    /* This example shows how to get the device size by reading the manufacturer ID. */
    uint8_t data[4];

    data[0] = QSPI_EXAMPLE_COMMAND_READ_ID;

    err = R_QSPI_DirectWrite(&g_qspi0_ctrl, &data[0], 1, true);

    assert(FSP_SUCCESS == err);

    /* Read 3 bytes. The third byte often represents the size of the QSPI, where the
    size of the QSPI = 2 ^ N. */
    err = R_QSPI_DirectRead(&g_qspi0_ctrl, &data[0], 3);

    assert(FSP_SUCCESS == err);

```

```
    device_size_bytes = 1U << data[2];
    FSP_PARAMETER_NOT_USED(device_size_bytes);
#endif
#ifdef QSPI_EXAMPLE_COMMAND_READ_SFDP
    /* Read the JEDEC SFDP header to locate the JEDEC flash parameters table. Reference
    JESD216 "Serial Flash
    * Discoverable Parameters (SFDP)". */
    /* Send the standard 0x5A command followed by 3 address bytes (SFDP header is at
    address 0). */
    uint8_t buffer[16];
    memset(&buffer[0], 0, sizeof(buffer));
    buffer[0] = QSPI_EXAMPLE_COMMAND_READ_SFDP;
    err      = R_QSPI_DirectWrite(&g_qspi0_ctrl, &buffer[0], 4, true);
    assert(FSP_SUCCESS == err);
    /* Read out 16 bytes (1 dummy byte followed by 15 data bytes). */
    err = R_QSPI_DirectRead(&g_qspi0_ctrl, &buffer[0], 16);
    assert(FSP_SUCCESS == err);
    /* Read the JEDEC flash parameters to locate the memory size. */
    /* Send the standard 0x5A command followed by 3 address bytes (located in big endian
    order at offset 0xC-0xE).
    * These bytes are accessed at 0xD-0xF because the first byte read is a dummy byte.
    */
    buffer[0] = QSPI_EXAMPLE_COMMAND_READ_SFDP;
    buffer[1] = buffer[0xF];
    buffer[2] = buffer[0xE];
    buffer[3] = buffer[0xD];
    err      = R_QSPI_DirectWrite(&g_qspi0_ctrl, &buffer[0], 4, true);
    assert(FSP_SUCCESS == err);
    /* Read out 9 bytes (1 dummy byte followed by 8 data bytes). */
    err = R_QSPI_DirectRead(&g_qspi0_ctrl, &buffer[0], 9);
    assert(FSP_SUCCESS == err);
    /* Read the memory density (located in big endian order at offset 0x4-0x7). These
    bytes are accessed at 0x5-0x8
    * because the first byte read is a dummy byte. */
```

```

uint32_t memory_density = (uint32_t) ((buffer[8] << 24) | (buffer[7] << 16) |
(buffer[6] << 8) | buffer[5]);
if ((1U << 31) & memory_density)
{
/* For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines
'N' where the density is
* computed as 2^N bits (N must be >= 32). This code subtracts 3 from N to divide by
8 to get the size in
* bytes instead of bits. */
device_size_bytes = 1U << ((memory_density & ~(1U << 31)) - 3U);
}
else
{
/* For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the
size in bits. This
* code divides the memory density by 8 to get the size in bytes instead of bits. */
device_size_bytes = (memory_density / 8) + 1;
}
FSP_PARAMETER_NOT_USED(device_size_bytes);
#endif
}

```

## Data Structures

struct [qspi\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [qspi\\_qssl\\_min\\_high\\_level\\_t](#)

enum [qspi\\_qspclk\\_div\\_t](#)

## Data Structure Documentation

### ◆ [qspi\\_instance\\_ctrl\\_t](#)

struct [qspi\\_instance\\_ctrl\\_t](#)

Instance control block. DO NOT INITIALIZE. Initialization occurs when [spi\\_flash\\_api\\_t::open](#) is called

## Enumeration Type Documentation

### ◆ qspi\_qssl\_min\_high\_level\_t

enum qspi_qssl_min_high_level_t	
Enumerator	
QSPI_QSSL_MIN_HIGH_LEVEL_1_QSPCLK	QSSL deselected for at least 1 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_2_QSPCLK	QSSL deselected for at least 2 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_3_QSPCLK	QSSL deselected for at least 3 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_4_QSPCLK	QSSL deselected for at least 4 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_5_QSPCLK	QSSL deselected for at least 5 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_6_QSPCLK	QSSL deselected for at least 6 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_7_QSPCLK	QSSL deselected for at least 7 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_8_QSPCLK	QSSL deselected for at least 8 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_9_QSPCLK	QSSL deselected for at least 9 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_10_QSPCLK	QSSL deselected for at least 10 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_11_QSPCLK	QSSL deselected for at least 11 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_12_QSPCLK	QSSL deselected for at least 12 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_13_QSPCLK	QSSL deselected for at least 13 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_14_QSPCLK	QSSL deselected for at least 14 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_15_QSPCLK	QSSL deselected for at least 15 QSPCLK.
QSPI_QSSL_MIN_HIGH_LEVEL_16_QSPCLK	QSSL deselected for at least 16 QSPCLK.

◆ **qspi\_qspclk\_div\_t**

enum <code>qspi_qspclk_div_t</code>	
Enumerator	
<code>QSPI_QSPCLK_DIV_2</code>	$QSPCLK = PCLK / 2.$
<code>QSPI_QSPCLK_DIV_3</code>	$QSPCLK = PCLK / 3.$
<code>QSPI_QSPCLK_DIV_4</code>	$QSPCLK = PCLK / 4.$
<code>QSPI_QSPCLK_DIV_5</code>	$QSPCLK = PCLK / 5.$
<code>QSPI_QSPCLK_DIV_6</code>	$QSPCLK = PCLK / 6.$
<code>QSPI_QSPCLK_DIV_7</code>	$QSPCLK = PCLK / 7.$
<code>QSPI_QSPCLK_DIV_8</code>	$QSPCLK = PCLK / 8.$
<code>QSPI_QSPCLK_DIV_9</code>	$QSPCLK = PCLK / 9.$
<code>QSPI_QSPCLK_DIV_10</code>	$QSPCLK = PCLK / 10.$
<code>QSPI_QSPCLK_DIV_11</code>	$QSPCLK = PCLK / 11.$
<code>QSPI_QSPCLK_DIV_12</code>	$QSPCLK = PCLK / 12.$
<code>QSPI_QSPCLK_DIV_13</code>	$QSPCLK = PCLK / 13.$
<code>QSPI_QSPCLK_DIV_14</code>	$QSPCLK = PCLK / 14.$
<code>QSPI_QSPCLK_DIV_15</code>	$QSPCLK = PCLK / 15.$
<code>QSPI_QSPCLK_DIV_16</code>	$QSPCLK = PCLK / 16.$
<code>QSPI_QSPCLK_DIV_17</code>	$QSPCLK = PCLK / 17.$
<code>QSPI_QSPCLK_DIV_18</code>	$QSPCLK = PCLK / 18.$
<code>QSPI_QSPCLK_DIV_20</code>	$QSPCLK = PCLK / 20.$
<code>QSPI_QSPCLK_DIV_22</code>	$QSPCLK = PCLK / 22.$
<code>QSPI_QSPCLK_DIV_24</code>	$QSPCLK = PCLK / 24.$
<code>QSPI_QSPCLK_DIV_26</code>	$QSPCLK = PCLK / 26.$
<code>QSPI_QSPCLK_DIV_28</code>	

	QSPCLK = PCLK / 28.
QSPI_QSPCLK_DIV_30	QSPCLK = PCLK / 30.
QSPI_QSPCLK_DIV_32	QSPCLK = PCLK / 32.
QSPI_QSPCLK_DIV_34	QSPCLK = PCLK / 34.
QSPI_QSPCLK_DIV_36	QSPCLK = PCLK / 36.
QSPI_QSPCLK_DIV_38	QSPCLK = PCLK / 38.
QSPI_QSPCLK_DIV_40	QSPCLK = PCLK / 40.
QSPI_QSPCLK_DIV_42	QSPCLK = PCLK / 42.
QSPI_QSPCLK_DIV_44	QSPCLK = PCLK / 44.
QSPI_QSPCLK_DIV_46	QSPCLK = PCLK / 46.
QSPI_QSPCLK_DIV_48	QSPCLK = PCLK / 48.

## Function Documentation

### ◆ R\_QSPI\_Open()

```
fsp_err_t R_QSPI_Open ( spi_flash_ctrl_t * p_ctrl, spi_flash_cfg_t const *const p_cfg )
```

Open the QSPI driver module. After the driver is open, the QSPI can be accessed like internal flash memory starting at address 0x60000000.

Implements `spi_flash_api_t::open`.

#### Return values

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	The parameter <code>p_instance_ctrl</code> or <code>p_cfg</code> is NULL.
FSP_ERR_ALREADY_OPEN	Driver has already been opened with the same <code>p_instance_ctrl</code> .

◆ **R\_QSPI\_Close()**

```
fsp_err_t R_QSPI_Close ( spi_flash_ctrl_t * p_ctrl)
```

Close the QSPI driver module.

Implements `spi_flash_api_t::close`.

**Return values**

FSP_SUCCESS	Configuration was successful.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_DirectWrite()**

```
fsp_err_t R_QSPI_DirectWrite ( spi_flash_ctrl_t * p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write )
```

Writes raw data directly to the QSPI.

Implements `spi_flash_api_t::directWrite`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_DirectRead()**

```
fsp_err_t R_QSPI_DirectRead ( spi_flash_ctrl_t * p_ctrl, uint8_t *const p_dest, uint32_t const bytes )
```

Reads raw data directly from the QSPI. This API can only be called after R\_QSPI\_DirectWrite with read\_after\_write set to true.

Implements `spi_flash_api_t::directRead`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function must be called after R_QSPI_DirectWrite with read_after_write set to true.

◆ **R\_QSPI\_SpiProtocolSet()**

```
fsp_err_t R_QSPI_SpiProtocolSet ( spi_flash_ctrl_t * p_ctrl, spi_flash_protocol_t spi_protocol )
```

Sets the SPI protocol.

Implements `spi_flash_api_t::spiProtocolSet`.

**Return values**

FSP_SUCCESS	SPI protocol updated on MCU peripheral.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_ARGUMENT	Invalid SPI protocol requested.

◆ **R\_QSPI\_XipEnter()**

```
fsp_err_t R_QSPI_XipEnter ( spi_flash_ctrl_t * p_ctrl)
```

Enters XIP (execute in place) mode.

Implements `spi_flash_api_t::xipEnter`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_XipExit()**

```
fsp_err_t R_QSPI_XipExit ( spi_flash_ctrl_t * p_ctrl)
```

Exits XIP (execute in place) mode.

Implements `spi_flash_api_t::xipExit`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

◆ **R\_QSPI\_Write()**

```
fsp_err_t R_QSPI_Write ( spi_flash_ctrl_t * p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest,
uint32_t byte_count )
```

Program a page of data to the flash.

Implements `spi_flash_api_t::write`.

**Return values**

FSP_SUCCESS	The flash was programmed successfully.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> , <code>p_dest</code> or <code>p_src</code> is NULL, or <code>byte_count</code> crosses a page boundary.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_Erase()**

```
fsp_err_t R_QSPI_Erase ( spi_flash_ctrl_t * p_ctrl, uint8_t *const p_device_address, uint32_t
byte_count )
```

Erase a block or sector of flash. The `byte_count` must exactly match one of the erase sizes defined in `spi_flash_cfg_t`. For chip erase, `byte_count` must be `SPI_FLASH_ERASE_SIZE_CHIP_ERASE`.

Implements `spi_flash_api_t::erase`.

**Return values**

FSP_SUCCESS	The command to erase the flash was executed successfully.
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> or <code>p_device_address</code> is NULL, or <code>byte_count</code> doesn't match an erase size defined in <code>spi_flash_cfg_t</code> , or device is in XIP mode.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.
FSP_ERR_DEVICE_BUSY	The device is busy.

◆ **R\_QSPI\_StatusGet()**

```
fsp_err_t R_QSPI_StatusGet ( spi_flash_ctrl_t * p_ctrl, spi_flash_status_t *const p_status )
```

Gets the write or erase status of the flash.

Implements `spi_flash_api_t::statusGet`.

**Return values**

FSP_SUCCESS	The write status is in p_status.
FSP_ERR_ASSERTION	p_instance_ctrl or p_status is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.
FSP_ERR_INVALID_MODE	This function can't be called when XIP mode is enabled.

◆ **R\_QSPI\_BankSet()**

```
fsp_err_t R_QSPI_BankSet ( spi_flash_ctrl_t * p_ctrl, uint32_t bank )
```

Selects the bank to access. A bank is a 64MB sliding access window into the QSPI device flash memory space. To access chip address 0x4000000, select bank 1, then read from internal flash address 0x60000000. To access chip address 0x8001000, select bank 2, then read from internal flash address 0x60001000.

This function is not required for memory devices less than or equal to 512 Mb (64MB).

Implements `spi_flash_api_t::bankSet`.

**Return values**

FSP_SUCCESS	Bank successfully selected.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	Driver is not opened.

**4.2.42 Realtime Clock (r\_rtc)**

## Modules

**Functions**

```
fsp_err_t R_RTC_Open (rtc_ctrl_t *const p_ctrl, rtc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_RTC_Close (rtc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_RTC_CalendarTimeSet (rtc_ctrl_t *const p_ctrl, rtc_time_t *const
```

	p_time)
fsp_err_t	R_RTC_CalendarTimeGet (rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time)
fsp_err_t	R_RTC_CalendarAlarmSet (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
fsp_err_t	R_RTC_CalendarAlarmGet (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
fsp_err_t	R_RTC_PeriodicIrqRateSet (rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate)
fsp_err_t	R_RTC_ErrorAdjustmentSet (rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const *const err_adj_cfg)
fsp_err_t	R_RTC_InfoGet (rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info)
fsp_err_t	R_RTC_CallbackSet (rtc_ctrl_t *const p_ctrl, void(*p_callback)(rtc_callback_args_t *), void const *const p_context, rtc_callback_args_t *const p_callback_memory)

## Detailed Description

Driver for the RTC peripheral on RA MCUs. This module implements the [RTC Interface](#).

## Overview

The RTC HAL module configures the RTC module and controls clock, calendar and alarm functions. A callback can be used to respond to the alarm and periodic interrupt.

### Features

- RTC time and date get and set.
- RTC time and date alarm get and set.
- RTC alarm and periodic event notification.

The RTC HAL module supports three different interrupt types:

- An alarm interrupt generated on a match of any combination of year, month, day, day of the week, hour, minute or second
- A periodic interrupt generated every 2, 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, or 1/256 second(s)
- A carry interrupt is used internally when reading time from the RTC calendar to get accurate time readings.

#### Note

See section "23.3.5 Reading 64-Hz Counter and Time" of the RA6M3 manual R01UH0886EJ0100 for more details.

A user-defined callback function can be registered (in the `rtc_api_t::open` API call) and will be called from the interrupt service routine (ISR) for alarm and periodic interrupt. When called, it is passed a pointer to a structure (`rtc_callback_args_t`) that holds a user-defined context pointer and an indication of which type of interrupt was fired.

## Date and Time validation

"Parameter Checking" needs to be enabled if date and time validation is required for `calendarTimeSet` and `calendarAlarmSet` APIs. If "Parameter Checking" is enabled, the 'day of the week' field is automatically calculated and updated by the driver for the provided date. When using the `calendarAlarmSet` API, only the fields which have their corresponding match flag set are written to the registers. Other register fields are reset to default value.

## Sub-Clock error adjustment (Time Error Adjustment Function)

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. Because 32,768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low. The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software

The error adjustment is reset every time RTC is reconfigured or time is set.

### Note

*RTC driver configurations do not do error adjustment internally while initializing the driver. Application must make calls to the error adjustment api's for desired adjustment. See section 26.3.8 "Time Error Adjustment Function" of the RA6M3 manual R01UH0886EJ0100) for more details on this feature*

# Configuration

## Build Time Configurations for r\_rtc

The following build time configurations are defined in `fsp_cfg/r_rtc_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Driver > Timers > RTC Driver on r\_rtc

This module can be added to the Stacks tab via New Stack > Driver > Timers > RTC Driver on r\_rtc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rtc0	Module name.
Clock Source	<ul style="list-style-type: none"> <li>• Sub-Clock</li> </ul>	LOCO	Select the RTC clock

	• LOCO		source.
Frequency Comparison Value (LOCO)	Value must be a positive integer between 7 and 511	255	Frequency comparison value when using LOCO
Automatic Adjustment Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enable/ Disable the Error Adjustment mode
Automatic Adjustment Period	<ul style="list-style-type: none"> <li>• 10 Seconds</li> <li>• 1 Minute</li> <li>• NONE</li> </ul>	10 Seconds	Select the Error Adjustment Period for Automatic Adjustment
Adjustment Type (Plus-Minus)	<ul style="list-style-type: none"> <li>• NONE</li> <li>• Addition</li> <li>• Subtraction</li> </ul>	NONE	Select the Error Adjustment type
Error Adjustment Value	Value must be a positive integer less than equal to 63	0	Specify the Adjustment Value (the number of sub-clock cycles) from the prescaler
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Alarm Interrupt Priority	MCU Specific Options		Select the alarm interrupt priority.
Period Interrupt Priority	MCU Specific Options		Select the period interrupt priority.
Carry Interrupt Priority	MCU Specific Options		Select the carry interrupt priority.

**Note**

See 23.2.20 Frequency Register (RFRH/RFRL) of the RA6M3 manual R01UH0886EJ0100) for more details

**Interrupt Configuration**

To activate interrupts for the RTC module, the desired interrupts must be enabled, The underlying implementation will be expected to handle any interrupts it can support and notify higher layers via callback.

**Clock Configuration**

The RTC HAL module can use the following clock sources:

- LOCO (Low Speed On-Chip Oscillator) with less accuracy
- Sub-clock oscillator with increased accuracy

The LOCO is the default selection during configuration.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## System Initialization

- RTC driver does not start the sub-clock. The application is responsible for ensuring required clocks are started and stable before accessing MCU peripheral registers.

### Warning

The subclock can take seconds to stabilize. The RA startup code does not wait for subclock stabilization unless the subclock is the main clock source. When running AGT or RTC off the subclock, the application must ensure the subclock is stable before starting operation.

- Carry interrupt priority must be set to avoid incorrect time returned from `calendarTimeGet` API during roll-over.
- Even when only running in Periodic Interrupt mode `R_RTC_CalendarTimeSet` must be called successfully to start the RTC.

## Limitations

Developers should be aware of the following limitations when using the RTC:

- `R_RTC` operates in 24-hour mode.
- Binary-count mode is not supported.
- The `R_RTC_CalendarTimeGet()` cannot be used from an interrupt that has higher priority than the carry interrupt. Also, it must not be called with interrupts disabled globally, as this API internally uses carry interrupt for its processing. API may return incorrect time if this is done.

# Examples

## RTC Basic Example

This is a basic example of minimal use of the RTC in an application.

```
/* rtc_time_t is an alias for the C Standard time.h struct 'tm' */
rtc_time_t set_time =
{
    .tm_sec = 10,
    .tm_min = 11,
    .tm_hour = 12,
    .tm_mday = 6,
    .tm_wday = 3,
    .tm_mon = 11,
    .tm_year = YEARS_SINCE_1900,
```

```
};  
rtc_time_t get_time;  
void rtc_example ()  
{  
    fsp_err_t err = FSP_SUCCESS;  
    /* Initialize the RTC module */  
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    assert(FSP_SUCCESS == err);  
    /* Set the calendar time */  
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time);  
    /* Get the calendar time */  
    R_RTC_CalendarTimeGet(&g_rtc0_ctrl, &get_time);  
}
```

### RTC Periodic interrupt example

This is an example of periodic interrupt in RTC.

```
void rtc_periodic_irq_example ()  
{  
    fsp_err_t err = FSP_SUCCESS;  
    /* Initialize the RTC module*/  
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);  
    /* Handle any errors. This function should be defined by the user. */  
    assert(FSP_SUCCESS == err);  
    /* R_RTC_CalendarTimeSet must be called at least once to start the RTC */  
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time);  
    /* Set the periodic interrupt rate to 1 second */  
    R_RTC_PeriodicIrqRateSet(&g_rtc0_ctrl, RTC_PERIODIC_IRQ_SELECT_1_SECOND);  
    /* Wait for the periodic interrupt */  
    while (1)  
    {  
        /* Wait for interrupt */  
    }  
}
```

```
}
```

## RTC Alarm interrupt example

This is an example of alarm interrupt in RTC.

```
void rtc_alarm_irq_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /*Initialize the RTC module*/
    err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time1.time);
    R_RTC_CalendarAlarmSet(&g_rtc0_ctrl, &set_time1);
    /* Wait for the Alarm interrupt */
    while (1)
    {
        /* Wait for interrupt */
    }
}
```

## RTC Error Adjustment example

This is an example of modifying error adjustment in RTC.

```
void rtc_erroradj_example ()
{
    fsp_err_t err = FSP_SUCCESS;
    /*Initialize the RTC module*/
    R_RTC_Open(&g_rtc0_ctrl, &g_rtc1_cfg);
    R_RTC_CalendarTimeSet(&g_rtc0_ctrl, &set_time1.time);
    /* Modify Error Adjustment after RTC is running */
    err = R_RTC_ErrorAdjustmentSet(&g_rtc0_ctrl, &err_cfg2);
    assert(FSP_SUCCESS == err);
}
```

## Data Structures

struct [rtc\\_instance\\_ctrl\\_t](#)

### Data Structure Documentation

#### ◆ [rtc\\_instance\\_ctrl\\_t](#)

struct [rtc\\_instance\\_ctrl\\_t](#)

Channel control block. DO NOT INITIALIZE. Initialization occurs when [rtc\\_api\\_t::open](#) is called

#### Data Fields

uint32_t	<a href="#">open</a>
	Whether or not driver is open.
const <a href="#">rtc_cfg_t</a> *	<a href="#">p_cfg</a>
	Pointer to initial configurations.
volatile bool	<a href="#">carry_isr_triggered</a>
	Was the carry isr triggered.

### Function Documentation

◆ **R\_RTC\_Open()**

```
fsp_err_t R_RTC_Open ( rtc_ctrl_t *const p_ctrl, rtc_cfg_t const *const p_cfg )
```

Opens and configures the RTC driver module. Implements `rtc_api_t::open`. Configuration includes clock source, and interrupt callback function.

Example:

```
/* Initialize the RTC module */
err = R_RTC_Open(&g_rtc0_ctrl, &g_rtc0_cfg);
```

**Return values**

FSP_SUCCESS	Initialization was successful and RTC has started.
FSP_ERR_ASSERTION	Invalid p_ctrl or p_cfg pointer.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.

◆ **R\_RTC\_Close()**

```
fsp_err_t R_RTC_Close ( rtc_ctrl_t *const p_ctrl)
```

Close the RTC driver. Implements `rtc_api_t::close`

**Return values**

FSP_SUCCESS	De-Initialization was successful and RTC driver closed.
FSP_ERR_ASSERTION	Invalid p_ctrl.
FSP_ERR_NOT_OPEN	Driver not open already for close.

◆ **R\_RTC\_CalendarTimeSet()**

```
fsp_err_t R_RTC_CalendarTimeSet ( rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time )
```

Set the calendar time.

Implements `rtc_api_t::calendarTimeSet`.

**Return values**

FSP_SUCCESS	Calendar time set operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.

◆ **R\_RTC\_CalendarTimeGet()**

```
fsp_err_t R_RTC_CalendarTimeGet ( rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time )
```

Get the calendar time.

**Warning**

Do not call this function from a critical section or from an interrupt with higher priority than the carry interrupt, or the time returned may be inaccurate.

Implements `rtc_api_t::calendarTimeGet`

**Return values**

FSP_SUCCESS	Calendar time get operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_CalendarAlarmSet()**

```
fsp_err_t R_RTC_CalendarAlarmSet ( rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm )
```

Set the calendar alarm time.

Implements `rtc_api_t::calendarAlarmSet`.

**Precondition**

The calendar counter must be running before the alarm can be set.

**Return values**

FSP_SUCCESS	Calendar alarm time set operation was successful.
FSP_ERR_INVALID_ARGUMENT	Invalid time parameter field.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_CalendarAlarmGet()**

```
fsp_err_t R_RTC_CalendarAlarmGet ( rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm )
```

Get the calendar alarm time.

Implements `rtc_api_t::calendarAlarmGet`

**Return values**

FSP_SUCCESS	Calendar alarm time get operation was successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.

◆ **R\_RTC\_PeriodicIrqRateSet()**

```
fsp_err_t R_RTC_PeriodicIrqRateSet ( rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate )
```

Set the periodic interrupt rate and enable periodic interrupt.

Implements `rtc_api_t::periodicIrqRateSet`

**Note**

To start the RTC `R_RTC_CalendarTimeSet` must be called at least once.

Example:

```
/* Set the periodic interrupt rate to 1 second */
R_RTC_PeriodicIrqRateSet(&g_rtc0_ctrl, RTC_PERIODIC_IRQ_SELECT_1_SECOND);
```

**Return values**

FSP_SUCCESS	The periodic interrupt rate was successfully set.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.
FSP_ERR_IRQ_BSP_DISABLED	User IRQ parameter not valid

◆ **R\_RTC\_ErrorAdjustmentSet()**

```
fsp_err_t R_RTC_ErrorAdjustmentSet ( rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const
*const err_adj_cfg )
```

This function sets time error adjustment

Implements `rtc_api_t::errorAdjustmentSet`

**Return values**

FSP_SUCCESS	Time error adjustment successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open for operation.
FSP_ERR_UNSUPPORTED	The clock source is not sub-clock.
FSP_ERR_INVALID_ARGUMENT	Invalid error adjustment value.

◆ **R\_RTC\_InfoGet()**

```
fsp_err_t R_RTC_InfoGet ( rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info )
```

Set RTC clock source and running status information and store it in provided pointer p\_rtc\_info

Implements `rtc_api_t::infoGet`

**Return values**

FSP_SUCCESS	Get information Successful.
FSP_ERR_ASSERTION	Invalid input argument.
FSP_ERR_NOT_OPEN	Driver not open already for operation.

◆ **R\_RTC\_CallbackSet()**

```
fsp_err_t R_RTC_CallbackSet ( rtc_ctrl_t *const p_ctrl, void(*) (rtc_callback_args_t *) p_callback, void const *const p_context, rtc_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `rtc_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Baud rate was successfully changed.
FSP_ERR_ASSERTION	Pointer to RTC control block is NULL or the RTC is not configured to use the internal clock.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

**4.2.43 Secure Crypto Engine (r\_sce\_protected)**

## Modules

**Functions**

```
fsp_err_t R_SCE_Open (sce_ctrl_t *const p_ctrl, sce_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SCE_Close (sce_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SCE_SoftwareReset (void)
```

fsp_err_t	R_SCE_AES128_WrappedKeyGenerate (sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256_WrappedKeyGenerate (sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSA1024_WrappedKeyPairGenerate (sce_rsa1024_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_RSA2048_WrappedKeyPairGenerate (sce_rsa2048_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_ECC_secp192r1_WrappedKeyPairGenerate (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_ECC_secp224r1_WrappedKeyPairGenerate (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_ECC_secp256r1_WrappedKeyPairGenerate (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_ECC_secp384r1_WrappedKeyPairGenerate (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t	R_SCE_RandomNumberGenerate (uint32_t *random)
fsp_err_t	R_SCE_AES128_EncryptedKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256_EncryptedKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_SHA256HMAC_EncryptedKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSA1024_EncryptedPublicKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_public_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSA1024_EncryptedPrivateKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_private_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSA2048_EncryptedPublicKeyWrap (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa2048_public_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSA2048_EncryptedPrivateKeyWrap (uint8_t *initial_vector,

```
uint8_t *encrypted_key, sce_key_update_key_t *key_update_key,
sce_rsa2048_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_RSA3072_EncryptedPublicKeyWrap (uint8_t *initial_vector,
uint8_t *encrypted_key, sce_key_update_key_t *key_update_key,
sce_rsa3072_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_RSA4096_EncryptedPublicKeyWrap (uint8_t *initial_vector,
uint8_t *encrypted_key, sce_key_update_key_t *key_update_key,
sce_rsa4096_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp192r1_EncryptedPublicKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp224r1_EncryptedPublicKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp256r1_EncryptedPublicKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp384r1_EncryptedPublicKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp192r1_EncryptedPrivateKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp224r1_EncryptedPrivateKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp256r1_EncryptedPrivateKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECC_secp384r1_EncryptedPrivateKeyWrap (uint8_t
*initial_vector, uint8_t *encrypted_key, sce_key_update_key_t
*key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_AES128ECB_EncryptInit (sce_aes_handle_t *handle,
sce_aes_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_AES128ECB_EncryptUpdate (sce_aes_handle_t *handle,
uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
```

```
fsp_err_t R_SCE_AES128ECB_EncryptFinal (sce_aes_handle_t *handle, uint8_t
*cipher, uint32_t *cipher_length)
```

fsp_err_t	R_SCE_AES128ECB_DecryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES128ECB_DecryptUpdate (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t	R_SCE_AES128ECB_DecryptFinal (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)
fsp_err_t	R_SCE_AES256ECB_EncryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256ECB_EncryptUpdate (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t	R_SCE_AES256ECB_EncryptFinal (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)
fsp_err_t	R_SCE_AES256ECB_DecryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256ECB_DecryptUpdate (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t	R_SCE_AES256ECB_DecryptFinal (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)
fsp_err_t	R_SCE_AES128CBC_EncryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)
fsp_err_t	R_SCE_AES128CBC_EncryptUpdate (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t	R_SCE_AES128CBC_EncryptFinal (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)
fsp_err_t	R_SCE_AES128CBC_DecryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)
fsp_err_t	R_SCE_AES128CBC_DecryptUpdate (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t	R_SCE_AES128CBC_DecryptFinal (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)
fsp_err_t	R_SCE_AES256CBC_EncryptInit (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)
fsp_err_t	R_SCE_AES256CBC_EncryptUpdate (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)

fsp\_err\_t R\_SCE\_AES256CBC\_EncryptFinal (sce\_aes\_handle\_t \*handle, uint8\_t \*cipher, uint32\_t \*cipher\_length)

fsp\_err\_t R\_SCE\_AES256CBC\_DecryptInit (sce\_aes\_handle\_t \*handle, sce\_aes\_wrapped\_key\_t \*wrapped\_key, uint8\_t \*initial\_vector)

fsp\_err\_t R\_SCE\_AES256CBC\_DecryptUpdate (sce\_aes\_handle\_t \*handle, uint8\_t \*cipher, uint8\_t \*plain, uint32\_t cipher\_length)

fsp\_err\_t R\_SCE\_AES256CBC\_DecryptFinal (sce\_aes\_handle\_t \*handle, uint8\_t \*plain, uint32\_t \*plain\_length)

fsp\_err\_t R\_SCE\_AES128GCM\_EncryptInit (sce\_gcm\_handle\_t \*handle, sce\_aes\_wrapped\_key\_t \*wrapped\_key, uint8\_t \*initial\_vector, uint32\_t initial\_vector\_length)

fsp\_err\_t R\_SCE\_AES128GCM\_EncryptUpdate (sce\_gcm\_handle\_t \*handle, uint8\_t \*plain, uint8\_t \*cipher, uint32\_t plain\_data\_length, uint8\_t \*aad, uint32\_t aad\_length)

fsp\_err\_t R\_SCE\_AES128GCM\_EncryptFinal (sce\_gcm\_handle\_t \*handle, uint8\_t \*cipher, uint32\_t \*cipher\_data\_length, uint8\_t \*atag)

fsp\_err\_t R\_SCE\_AES128GCM\_DecryptInit (sce\_gcm\_handle\_t \*handle, sce\_aes\_wrapped\_key\_t \*wrapped\_key, uint8\_t \*initial\_vector, uint32\_t initial\_vector\_length)

fsp\_err\_t R\_SCE\_AES128GCM\_DecryptUpdate (sce\_gcm\_handle\_t \*handle, uint8\_t \*cipher, uint8\_t \*plain, uint32\_t cipher\_data\_length, uint8\_t \*aad, uint32\_t aad\_length)

fsp\_err\_t R\_SCE\_AES128GCM\_DecryptFinal (sce\_gcm\_handle\_t \*handle, uint8\_t \*plain, uint32\_t \*plain\_data\_length, uint8\_t \*atag, uint32\_t atag\_length)

fsp\_err\_t R\_SCE\_AES256GCM\_EncryptInit (sce\_gcm\_handle\_t \*handle, sce\_aes\_wrapped\_key\_t \*wrapped\_key, uint8\_t \*initial\_vector, uint32\_t initial\_vector\_length)

fsp\_err\_t R\_SCE\_AES256GCM\_EncryptUpdate (sce\_gcm\_handle\_t \*handle, uint8\_t \*plain, uint8\_t \*cipher, uint32\_t plain\_data\_length, uint8\_t \*aad, uint32\_t aad\_length)

fsp\_err\_t R\_SCE\_AES256GCM\_EncryptFinal (sce\_gcm\_handle\_t \*handle, uint8\_t \*cipher, uint32\_t \*cipher\_data\_length, uint8\_t \*atag)

fsp\_err\_t R\_SCE\_AES256GCM\_DecryptInit (sce\_gcm\_handle\_t \*handle, sce\_aes\_wrapped\_key\_t \*wrapped\_key, uint8\_t \*initial\_vector, uint32\_t initial\_vector\_length)

fsp_err_t	R_SCE_AES256GCM_DecryptUpdate (sce_gcm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_data_length, uint8_t *aad, uint32_t aad_length)
fsp_err_t	R_SCE_AES256GCM_DecryptFinal (sce_gcm_handle_t *handle, uint8_t *plain, uint32_t *plain_data_length, uint8_t *atag, uint32_t atag_length)
fsp_err_t	R_SCE_AES128CCM_EncryptInit (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t adata_length, uint32_t payload_length, uint32_t mac_length)
fsp_err_t	R_SCE_AES128CCM_EncryptUpdate (sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t	R_SCE_AES128CCM_EncryptFinal (sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_AES128CCM_DecryptInit (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t adata_length, uint32_t payload_length, uint32_t mac_length)
fsp_err_t	R_SCE_AES128CCM_DecryptUpdate (sce_ccm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t	R_SCE_AES128CCM_DecryptFinal (sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_AES256CCM_EncryptInit (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t adata_length, uint32_t payload_length, uint32_t mac_length)
fsp_err_t	R_SCE_AES256CCM_EncryptUpdate (sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t	R_SCE_AES256CCM_EncryptFinal (sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_AES256CCM_DecryptInit (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t adata_length, uint32_t payload_length, uint32_t mac_length)
fsp_err_t	R_SCE_AES256CCM_DecryptUpdate (sce_ccm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t	R_SCE_AES256CCM_DecryptFinal (sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)

fsp_err_t	R_SCE_AES128CMAC_GenerateInit (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES128CMAC_GenerateUpdate (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_AES128CMAC_GenerateFinal (sce_cmac_handle_t *handle, uint8_t *mac)
fsp_err_t	R_SCE_AES128CMAC_VerifyInit (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES128CMAC_VerifyUpdate (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_AES128CMAC_VerifyFinal (sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_AES256CMAC_GenerateInit (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256CMAC_GenerateUpdate (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_AES256CMAC_GenerateFinal (sce_cmac_handle_t *handle, uint8_t *mac)
fsp_err_t	R_SCE_AES256CMAC_VerifyInit (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_AES256CMAC_VerifyUpdate (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_AES256CMAC_VerifyFinal (sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_SHA256_Init (sce_sha_md5_handle_t *handle)
fsp_err_t	R_SCE_SHA256_Update (sce_sha_md5_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_SHA256_Final (sce_sha_md5_handle_t *handle, uint8_t *digest, uint32_t *digest_length)
fsp_err_t	R_SCE_SHA256HMAC_GenerateInit (sce_hmac_sha_handle_t *handle, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_SHA256HMAC_GenerateUpdate (sce_hmac_sha_handle_t *handle, uint8_t *message, uint32_t message_length)

fsp_err_t	R_SCE_SHA256HMAC_GenerateFinal (sce_hmac_sha_handle_t *handle, uint8_t *mac)
fsp_err_t	R_SCE_SHA256HMAC_VerifyInit (sce_hmac_sha_handle_t *handle, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_SHA256HMAC_VerifyUpdate (sce_hmac_sha_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t	R_SCE_SHA256HMAC_VerifyFinal (sce_hmac_sha_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t	R_SCE_RSASSA_PKCS1024_SignatureGenerate (sce_rsa_byte_data_t *message_hash, sce_rsa_byte_data_t *signature, sce_rsa1024_private_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSASSA_PKCS1024_SignatureVerify (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa1024_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSASSA_PKCS2048_SignatureGenerate (sce_rsa_byte_data_t *message_hash, sce_rsa_byte_data_t *signature, sce_rsa2048_private_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSASSA_PKCS2048_SignatureVerify (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa2048_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSASSA_PKCS3072_SignatureVerify (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa3072_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSASSA_PKCS4096_SignatureVerify (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa4096_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t	R_SCE_RSAES_PKCS1024_Encrypt (sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa1024_public_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSAES_PKCS1024_Decrypt (sce_rsa_byte_data_t *cipher, sce_rsa_byte_data_t *plain, sce_rsa1024_private_wrapped_key_t *wrapped_key)
fsp_err_t	R_SCE_RSAES_PKCS2048_Encrypt (sce_rsa_byte_data_t *plain,

sce\_rsa\_byte\_data\_t \*cipher, sce\_rsa2048\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_RSAES\_PKCS2048\_Decrypt (sce\_rsa\_byte\_data\_t \*cipher, sce\_rsa\_byte\_data\_t \*plain, sce\_rsa2048\_private\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_RSAES\_PKCS3072\_Encrypt (sce\_rsa\_byte\_data\_t \*plain, sce\_rsa\_byte\_data\_t \*cipher, sce\_rsa3072\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_RSAES\_PKCS4096\_Encrypt (sce\_rsa\_byte\_data\_t \*plain, sce\_rsa\_byte\_data\_t \*cipher, sce\_rsa4096\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp192r1\_SignatureGenerate (sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecc\_private\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp224r1\_SignatureGenerate (sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecc\_private\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp256r1\_SignatureGenerate (sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecc\_private\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp384r1\_SignatureGenerate (sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecc\_private\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp192r1\_SignatureVerify (sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecc\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp224r1\_SignatureVerify (sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecc\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp256r1\_SignatureVerify (sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecc\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDSA\_secp384r1\_SignatureVerify (sce\_ecdsa\_byte\_data\_t \*signature, sce\_ecdsa\_byte\_data\_t \*message\_hash, sce\_ecc\_public\_wrapped\_key\_t \*wrapped\_key)

fsp\_err\_t R\_SCE\_ECDH\_secp256r1\_Init (sce\_ecdh\_handle\_t \*handle, uint32\_t key\_type, uint32\_t use\_key\_id)

fsp\_err\_t R\_SCE\_ECDH\_secp256r1\_PublicKeySign (sce\_ecdh\_handle\_t \*handle,

```
sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key,
sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key, uint8_t
*public_key, sce_ecdsa_byte_data_t *signature,
sce_ecc_private_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECDH_secp256r1_PublicKeyVerify (sce_ecdh_handle_t
*handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key,
uint8_t *public_key_data, sce_ecdsa_byte_data_t *signature,
sce_ecc_public_wrapped_key_t *wrapped_key)
```

```
fsp_err_t R_SCE_ECDH_secp256r1_SharedSecretCalculate (sce_ecdh_handle_t
*handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key,
sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key,
sce_ecdh_wrapped_key_t *shared_secret_wrapped_key)
```

```
fsp_err_t R_SCE_ECDH_secp256r1_KeyDerivation (sce_ecdh_handle_t *handle,
sce_ecdh_wrapped_key_t *shared_secret_wrapped_key, uint32_t
key_type, uint32_t kdf_type, uint8_t *other_info, uint32_t
other_info_length, sce_hmac_sha_wrapped_key_t *salt_wrapped_key,
sce_aes_wrapped_key_t *wrapped_key)
```

## Detailed Description

Driver for the Secure Crypto Engine (SCE) on RA MCUs.

## Overview

This module provides SCE functions.

### HW Overview

Crypto Peripheral version	Devices
SCE9 (Protected mode)	RA4M2, RA4M3, RA6M4, RA6M5

### Features

The SCE module supports for the following features.

- Cryptography
  - Symmetric Encryption/Decryption
    - AES
      - ECB 128/256bit
      - CBC 128/256bit
      - GCM 128/256bit
      - CCM 128/256bit
  - Asymmetric Encryption/Decryption
    - RSA
      - RSAES-PKCS1-V1\_5 1024/2048bit
      - RSAES-PKCS1-V1\_5 3072/4096bit (Encryption only)
      - RSASSA-PKCS1-V1\_5 1024/2048bit
      - RSASSA-PKCS1-V1\_5 3072/4096bit (Verification only)
    - ECC

- ECDSA secp192r1/secp224r1/secp256r1/secp384r1
- ECDH secp192r1/secp224r1/secp256r1/secp384r1
- Hash Functions
  - SHA-2
    - SHA-256
- Message Authentication Code
  - HMAC-SHA256bit
  - AES-CMAC 128/256bit
- Key Support
  - AES 128/256bit
  - RSA 1024/2048bit
  - RSA 3072/4096bit (public key only)
  - ECC secp192r1/secp224r1/secp256r1/secp384r1
  - HMAC-SHA256bit
- TRNG

## Configuration

### Clock Configuration

This module does not require a specific clock configuration.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

#### Usage of R\_SCE\_ECDSA\_secp384r1\_SignatureGenerate/Verify

The SCE does not support SHA-384 in hardware, so the APIs listed below require the user to create a SHA-384 function for signature generation and verification. To use the APIs listed below, enable SCE\_USER\_SHA\_384\_ENABLED on RA Smart Configurator and prepare a function called SCE\_USER\_SHA\_384\_FUNCTION. The interface of SCE\_USER\_SHA\_384\_FUNCTION, which is called by the following APIs, is described below.

- R\_SCE\_ECDSA\_secp384r1\_SignatureGenerate()
- R\_SCE\_ECDSA\_secp384r1\_SignatureVerify()

#### SCE\_USER\_SHA\_384\_FUNCTION()

```
uint32_t SCE_USER_SHA_384_FUNCTION(uint8_t * message, uint8_t * digest, uint32_t message_length)
```

SHA-384 hash calculation is performed for an area extending the number of bytes specified by the argument message\_length from the address specified by the argument message. The calculation result should be stored at the address specified by the argument digest.

Parameters

message	[in] Start address of message
digest	[in,out] address for storing hash calculation result (48 bytes)
message_length	[in] Effective byte count of message

## Return values

0	Hash value stored successfully.
others	Storing of hash value failed.

## Examples

### AES Example

This is an example of AES-256 encryption and decryption.

```
#include <string.h>
#include "r_sce.h"
#define BLOCK 16
void r_sce_example_aes();
sce_instance_ctrl_t sce_ctrl;
sce_cfg_t sce_cfg =
{
    .lifecycle = SCE_SSD
};
static uint8_t plain[BLOCK * 2] =
{
    0x52, 0x65, 0x6e, 0x65, 0x73, 0x61, 0x73, 0x20, 0x45, 0x6c, 0x65, 0x63, 0x74,
    0x72, 0x6f, 0x6e,
    0x69, 0x63, 0x73, 0x20, 0x43, 0x6f, 0x72, 0x70, 0x6f, 0x72, 0x61, 0x74, 0x69,
    0x6f, 0x6e, 0x00
};
void r_sce_example_aes ()
{
    sce_aes_handle_t handle;
    sce_aes_wrapped_key_t wrapped_key;
    uint8_t cipher_calculated[32] = {0};
```

```
uint8_t          plain_calculated[32] = {0};
uint32_t         dummy;

/* SCE power on */
R_SCE_Open(&sce_ctrl, &sce_cfg);

/* Generate a random key */
R_SCE_AES256_WrappedKeyGenerate(&wrapped_key);

/* Encrypt a plain text */
R_SCE_AES256ECB_EncryptInit(&handle, &wrapped_key);
R_SCE_AES256ECB_EncryptUpdate(&handle, plain, cipher_calculated, BLOCK * 2);
R_SCE_AES256ECB_EncryptFinal(&handle, cipher_calculated, &dummy);

/* Decrypt a cipher text using same key as Encryption */
R_SCE_AES256ECB_DecryptInit(&handle, &wrapped_key);
R_SCE_AES256ECB_DecryptUpdate(&handle, cipher_calculated, plain_calculated, BLOCK *
2);
R_SCE_AES256ECB_DecryptFinal(&handle, plain_calculated, &dummy);

/* SCE power off */
R_SCE_Close(&sce_ctrl);

/* Compare plain and plain_calculated */
if (memcmp(plain, plain_calculated, BLOCK * 2))
{
while (1)
{
/* plain and plain_calculated are different (incorrect) */
}
}
else
{
while (1)
{
/* plain and plain_calculated are the same (correct) */
}
}
}
```

## Data Structures

```
struct sce_instance_ctrl_t
```

## Data Structure Documentation

### ◆ sce\_instance\_ctrl\_t

```
struct sce_instance_ctrl_t
```

SCE private control block. DO NOT MODIFY. Initialization occurs when [R\\_SCE\\_Open\(\)](#) is called.

## Function Documentation

### ◆ R\_SCE\_Open()

```
fsp_err_t R_SCE_Open ( sce_ctrl_t *const p_ctrl, sce_cfg_t const *const p_cfg )
```

Enables use of SCE functionality.

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	The error-detection self-test failed to terminate normally.
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTTO_SCE_RETRY	Indicates that an entropy evaluation failure occurred. Run the function again.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

#### Note

*The valid pre-run state is SCE disabled. The pre-run state is SCE Disabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_Close()

```
fsp_err_t R_SCE_Close ( sce_ctrl_t *const p_ctrl)
```

Stops supply of power to the SCE.

#### Return values

FSP_SUCCESS	Normal termination
-------------	--------------------

#### Note

*The pre-run state is any state. After the function runs the state transitions to SCE Disabled State.*

## ◆ R\_SCE\_SoftwareReset()

fsp\_err\_t R\_SCE\_SoftwareReset ( void )

Software reset to SCE.

Reverts the state to the SCE initial state.

**Return values**

FSP_SUCCESS	Normal termination
-------------	--------------------

*Note*

The pre-run state is any state. After the function runs the state transitions to SCE Disabled State.

## ◆ R\_SCE\_AES128\_WrappedKeyGenerate()

fsp\_err\_t R\_SCE\_AES128\_WrappedKeyGenerate ( sce\_aes\_wrapped\_key\_t \* wrapped\_key)

This API outputs 128-bit AES wrapped key from a random number.

This API generates a wrapped key from a random number in the SCE. Accordingly, user key input is unnecessary. By encrypting data using the wrapped key is output by this API, dead copying of data can be prevented.

**Parameters**

[in,out]	wrapped_key	128-bit AES wrapped key
----------	-------------	-------------------------

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.

*Note*

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Disabled State.

### ◆ R\_SCE\_AES256\_WrappedKeyGenerate()

`fsp_err_t R_SCE_AES256_WrappedKeyGenerate ( sce_aes_wrapped_key_t * wrapped_key)`

This API outputs 256-bit AES wrapped key from a random number.

This API generates a wrapped key from a random number in the SCE. Accordingly, user key input is unnecessary. By encrypting data using the wrapped key is output by this API, dead copying of data can be prevented.

#### Parameters

[in,out]	wrapped_key	256-bit AES wrapped key
----------	-------------	-------------------------

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Disabled State.*

## ◆ R\_SCE\_RSA1024\_WrappedKeyPairGenerate()

```
fsp_err_t R_SCE_RSA1024_WrappedKeyPairGenerate ( sce_rsa1024_wrapped_pair_key_t*
wrapped_pair_key)
```

This API outputs a wrapped key pair for a 1024-bit RSA public key and private key pair. These keys are generated from a random value produced internally by the SCE. Consequently, there is no need to input a user key. Dead copying of data can be prevented by encrypting the data using the wrapped key output by this API. A public wrapped key is generated by wrapped\_pair\_key->public, and a private wrapped key is generated by wrapped\_pair\_key->private. As the public key exponent, only 0x00010001 is generated.

**Parameters**

[in,out]	wrapped_pair_key	User key index for RSA 1024-bit public key and private key pair
----------	------------------	---

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred. Key generation failed.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSA2048\_WrappedKeyPairGenerate()

`fsp_err_t R_SCE_RSA2048_WrappedKeyPairGenerate ( sce_rsa2048_wrapped_pair_key_t * wrapped_pair_key)`

This API outputs a wrapped key pair for a 2048-bit RSA public key and private key pair. These keys are generated from a random value produced internally by the SCE. Consequently, there is no need to input a user key. Dead copying of data can be prevented by encrypting the data using the wrapped key output by this API. A public wrapped key is generated by `wrapped_pair_key->public`, and a private wrapped key is generated by `wrapped_pair_key->private`. As the public key exponent, only 0x00010001 is generated.

#### Parameters

[in,out]	<code>wrapped_pair_key</code>	User key index for RSA 2048-bit public key and private key pair
----------	-------------------------------	---

#### Return values

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred. Key generation failed.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp192r1\_WrappedKeyPairGenerate()

```
fsp_err_t R_SCE_ECC_secp192r1_WrappedKeyPairGenerate ( sce_ecc_wrapped_pair_key_t *
wrapped_pair_key)
```

This is an API for outputting a wrapped key pair for secp192r1 public key and private key pair. These keys are generated from a random number value internally within the SCE. There is therefore no need to input user keys. It is possible to prevent dead copying of data by using the wrapped key output by this API to encrypt the data. The public key index is generated in wrapped\_pair\_key->public, and the private key index is generated in wrapped\_pair\_key->private.

**Parameters**

[in,out]	wrapped_pair_key	Wrapped pair key for secp192r1 public key and private key pair
----------	------------------	--

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp224r1\_WrappedKeyPairGenerate()

`fsp_err_t R_SCE_ECC_secp224r1_WrappedKeyPairGenerate ( sce_ecc_wrapped_pair_key_t * wrapped_pair_key)`

This is an API for outputting a wrapped key pair for secp224r1 public key and private key pair. These keys are generated from a random number value internally within the SCE. There is therefore no need to input user keys. It is possible to prevent dead copying of data by using the wrapped key output by this API to encrypt the data. The public key index is generated in wrapped\_pair\_key->public, and the private key index is generated in wrapped\_pair\_key->private.

**Parameters**

[in,out]	wrapped_pair_key	Wrapped pair key for secp224r1 public key and private key pair
----------	------------------	--

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp256r1\_WrappedKeyPairGenerate()

```
fsp_err_t R_SCE_ECC_secp256r1_WrappedKeyPairGenerate ( sce_ecc_wrapped_pair_key_t *
wrapped_pair_key)
```

This is an API for outputting a wrapped key pair for secp256r1 public key and private key pair. These keys are generated from a random number value internally within the SCE. There is therefore no need to input user keys. It is possible to prevent dead copying of data by using the wrapped key output by this API to encrypt the data. The public key index is generated in wrapped\_pair\_key->public, and the private key index is generated in wrapped\_pair\_key->private.

**Parameters**

[in,out]	wrapped_pair_key	Wrapped pair key for secp256r1 public key and private key pair
----------	------------------	--

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp384r1\_WrappedKeyPairGenerate()

```
fsp_err_t R_SCE_ECC_secp384r1_WrappedKeyPairGenerate ( sce_ecc_wrapped_pair_key_t *
wrapped_pair_key)
```

This is an API for outputting a wrapped key pair for secp384r1 public key and private key pair. These keys are generated from a random number value internally within the SCE. There is therefore no need to input user keys. It is possible to prevent dead copying of data by using the wrapped key output by this API to encrypt the data. The public key index is generated in wrapped\_pair\_key->public, and the private key index is generated in wrapped\_pair\_key->private.

**Parameters**

[in,out]	wrapped_pair_key	Wrapped pair key for secp384r1 public key and private key pair
----------	------------------	--

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_RandomNumberGenerate()

```
fsp_err_t R_SCE_RandomNumberGenerate ( uint32_t * random)
```

This API can generate 4 words random number.

**Parameters**

[in,out]	random	Stores 4words (16 bytes) random data.
----------	--------	---------------------------------------

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_AES128\_EncryptedKeyWrap()**

```
fsp_err_t R_SCE_AES128_EncryptedKeyWrap ( uint8_t* initial_vector, uint8_t* encrypted_key,
sce_key_update_key_t* key_update_key, sce_aes_wrapped_key_t* wrapped_key )
```

This API wraps 128-bit AES key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	128-bit AES wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_AES256\_EncryptedKeyWrap()

```
fsp_err_t R_SCE_AES256_EncryptedKeyWrap ( uint8_t* initial_vector, uint8_t* encrypted_key,
sce_key_update_key_t* key_update_key, sce_aes_wrapped_key_t* wrapped_key )
```

This API wraps 256-bit AES key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	256-bit AES wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_SHA256HMAC\_EncryptedKeyWrap()

```
fsp_err_t R_SCE_SHA256HMAC_EncryptedKeyWrap ( uint8_t* initial_vector, uint8_t*
encrypted_key, sce_key_update_key_t* key_update_key, sce_hmac_sha_wrapped_key_t*
wrapped_key )
```

This API wraps HMAC-SHA256 key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	HMAC-SHA256 wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_RSA1024\_EncryptedPublicKeyWrap()**

```
fsp_err_t R_SCE_RSA1024_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_rsa1024_public_wrapped_key_t *
wrapped_key )
```

This API wraps 1024-bit RSA public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSA1024\_EncryptedPrivateKeyWrap()

```
fsp_err_t R_SCE_RSA1024_EncryptedPrivateKeyWrap ( uint8_t* initial_vector, uint8_t*
encrypted_key, sce_key_update_key_t* key_update_key, sce_rsa1024_private_wrapped_key_t*
wrapped_key )
```

This API wraps 1024-bit RSA private key within the user routine.

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA private wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_RSA2048\_EncryptedPublicKeyWrap()**

```
fsp_err_t R_SCE_RSA2048_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_rsa2048_public_wrapped_key_t *
wrapped_key )
```

This API wraps 2048-bit RSA public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_RSA2048\_EncryptedPrivateKeyWrap()**

```
fsp_err_t R_SCE_RSA2048_EncryptedPrivateKeyWrap ( uint8_t* initial_vector, uint8_t*
encrypted_key, sce_key_update_key_t* key_update_key, sce_rsa2048_private_wrapped_key_t*
wrapped_key )
```

This API wraps 2048-bit RSA private key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	2048-bit RSA private wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_RSA3072\_EncryptedPublicKeyWrap()**

```
fsp_err_t R_SCE_RSA3072_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_rsa3072_public_wrapped_key_t *
wrapped_key )
```

This API wraps 3072-bit RSA public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	3072-bit RSA public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSA4096\_EncryptedPublicKeyWrap()

```
fsp_err_t R_SCE_RSA4096_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_rsa4096_public_wrapped_key_t *
wrapped_key )
```

This API wraps 4096-bit RSA public key within the user routine.

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA public wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_ECC\_secp192r1\_EncryptedPublicKeyWrap()

```
fsp_err_t R_SCE_ECC_secp192r1_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_public_wrapped_key_t *
wrapped_key )
```

This API wraps secp192r1 public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp192r1 public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp224r1\_EncryptedPublicKeyWrap()

```
fsp_err_t R_SCE_ECC_secp224r1_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_public_wrapped_key_t *
wrapped_key )
```

This API wraps secp224r1 public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp224r1 public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp256r1\_EncryptedPublicKeyWrap()

```
fsp_err_t R_SCE_ECC_secp256r1_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_public_wrapped_key_t *
wrapped_key )
```

This API wraps secp256r1 public key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp256r1 public wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_ECC\_secp384r1\_EncryptedPublicKeyWrap()

```
fsp_err_t R_SCE_ECC_secp384r1_EncryptedPublicKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_public_wrapped_key_t *
wrapped_key )
```

This API wraps secp384r1 public key within the user routine.

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp384r1 public wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_ECC\_secp192r1\_EncryptedPrivateKeyWrap()

```
fsp_err_t R_SCE_ECC_secp192r1_EncryptedPrivateKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_private_wrapped_key_t *
wrapped_key )
```

This API wraps secp192r1 private key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp192r1 private wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_ECC\_secp224r1\_EncryptedPrivateKeyWrap()

```
fsp_err_t R_SCE_ECC_secp224r1_EncryptedPrivateKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_private_wrapped_key_t *
wrapped_key )
```

This API wraps secp224r1 private key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp224r1 private wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp256r1\_EncryptedPrivateKeyWrap()

```
fsp_err_t R_SCE_ECC_secp256r1_EncryptedPrivateKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_private_wrapped_key_t *
wrapped_key )
```

This API wraps secp256r1 private key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp256r1 private wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECC\_secp384r1\_EncryptedPrivateKeyWrap()

```
fsp_err_t R_SCE_ECC_secp384r1_EncryptedPrivateKeyWrap ( uint8_t * initial_vector, uint8_t *
encrypted_key, sce_key_update_key_t * key_update_key, sce_ecc_private_wrapped_key_t *
wrapped_key )
```

This API wraps secp384r1 private key within the user routine.

**Parameters**

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp384r1 private wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128ECB\_EncryptInit()

```
fsp_err_t R_SCE_AES128ECB_EncryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES128ECB_EncryptInit()` function performs preparations for the execution of an AES calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128ECB_EncryptUpdate()` function and `R_SCE_AES128ECB_EncryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128ECB\_EncryptUpdate()

```
fsp_err_t R_SCE_AES128ECB_EncryptUpdate ( sce_aes_handle_t * handle, uint8_t * plain, uint8_t *
cipher, uint32_t plain_length )
```

The `R_SCE_AES128ECB_EncryptUpdate()` function encrypts the second argument, `plain`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the encryption result to the third argument, `cipher`. After plaintext input is completed, call `R_SCE_AES128ECB_EncryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in,out]	plain_length	plaintext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128ECB\_EncryptFinal()**

```
fsp_err_t R_SCE_AES128ECB_EncryptFinal ( sce_aes_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES128ECB\\_EncryptFinal\(\)](#) function writes the calculation result to the second argument, cipher, and writes the length of the calculation result to the third argument, cipher\_length. The original intent was for a portion of the encryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to cipher, and 0 is always written to cipher\_length. The arguments cipher and cipher\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128ECB\_DecryptInit()

```
fsp_err_t R_SCE_AES128ECB_DecryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES128ECB_DecryptInit()` function performs preparations for the execution of an AES calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128ECB_DecryptUpdate()` function and `R_SCE_AES128ECB_DecryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128ECB\_DecryptUpdate()

```
fsp_err_t R_SCE_AES128ECB_DecryptUpdate ( sce_aes_handle_t * handle, uint8_t * cipher, uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES128ECB_DecryptUpdate()` function decrypts the second argument, `cipher`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the decryption result to the third argument, `plain`. After plaintext input is completed, call `R_SCE_AES128ECB_DecryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128ECB\_DecryptFinal()**

```
fsp_err_t R_SCE_AES128ECB_DecryptFinal ( sce_aes_handle_t * handle, uint8_t * plain, uint32_t * plain_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES128ECB\\_DecryptFinal\(\)](#) function writes the calculation result to the second argument, plain, and writes the length of the calculation result to the third argument, plain\_length. The original intent was for a portion of the decryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to plain, and 0 is always written to plain\_length. The arguments plain and plain\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256ECB\_EncryptInit()

```
fsp_err_t R_SCE_AES256ECB_EncryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES256ECB_EncryptInit()` function performs preparations for the execution of an AES calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES256ECB_EncryptUpdate()` function and `R_SCE_AES256ECB_EncryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256ECB\_EncryptUpdate()

```
fsp_err_t R_SCE_AES256ECB_EncryptUpdate ( sce_aes_handle_t * handle, uint8_t * plain, uint8_t *
cipher, uint32_t plain_length )
```

The `R_SCE_AES256ECB_EncryptUpdate()` function encrypts the second argument, `plain`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the encryption result to the third argument, `cipher`. After plaintext input is completed, call `R_SCE_AES256ECB_EncryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>plain</code>	plaintext data area
[in,out]	<code>cipher</code>	ciphertext data area
[in,out]	<code>plain_length</code>	plaintext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256ECB\_EncryptFinal()**

```
fsp_err_t R_SCE_AES256ECB_EncryptFinal ( sce_aes_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES256ECB\\_EncryptFinal\(\)](#) function writes the calculation result to the second argument, cipher, and writes the length of the calculation result to the third argument, cipher\_length. The original intent was for a portion of the encryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to cipher, and 0 is always written to cipher\_length. The arguments cipher and cipher\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256ECB\_DecryptInit()

```
fsp_err_t R_SCE_AES256ECB_DecryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES128ECB_DecryptInit()` function performs preparations for the execution of an AES calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128ECB_DecryptUpdate()` function and `R_SCE_AES128ECB_DecryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256ECB\_DecryptUpdate()

```
fsp_err_t R_SCE_AES256ECB_DecryptUpdate ( sce_aes_handle_t * handle, uint8_t * cipher, uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES256ECB_DecryptUpdate()` function decrypts the second argument, `cipher`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the decryption result to the third argument, `plain`. After plaintext input is completed, call `R_SCE_AES256ECB_DecryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256ECB\_DecryptFinal()**

```
fsp_err_t R_SCE_AES256ECB_DecryptFinal ( sce_aes_handle_t * handle, uint8_t * plain, uint32_t * plain_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES256ECB\\_DecryptFinal\(\)](#) function writes the calculation result to the second argument, plain, and writes the length of the calculation result to the third argument, plain\_length. The original intent was for a portion of the decryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to plain, and 0 is always written to plain\_length. The arguments plain and plain\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CBC\_EncryptInit()

```
fsp_err_t R_SCE_AES128CBC_EncryptInit ( sce_aes_handle_t* handle, sce_aes_wrapped_key_t* wrapped_key, uint8_t* initial_vector )
```

The R\_SCE\_AES128CBC\_EncryptInit() function performs preparations for the execution of an AES calculation, and writes the result to the first argument, handle. The value of handle is used as an argument in the subsequent R\_SCE\_AES128CBC\_EncryptUpdate() function and R\_SCE\_AES128CBC\_EncryptFinal() function.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initialization vector area (16byte)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128CBC\_EncryptUpdate()

```
fsp_err_t R_SCE_AES128CBC_EncryptUpdate ( sce_aes_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_length )
```

The `R_SCE_AES128CBC_EncryptUpdate()` function encrypts the second argument, `plain`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the encryption result to the third argument, `cipher`. After plaintext input is completed, call `R_SCE_AES128CBC_EncryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>plain</code>	plaintext data area
[in,out]	<code>cipher</code>	ciphertext data area
[in,out]	<code>plain_length</code>	plaintext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPT_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPT_SCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128CBC\_EncryptFinal()**

```
fsp_err_t R_SCE_AES128CBC_EncryptFinal ( sce_aes_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length )
```

Using the handle specified in the first argument, handle, the **R\_SCE\_AES128CBC\_EncryptFinal()** function writes the calculation result to the second argument, cipher, and writes the length of the calculation result to the third argument, cipher\_length. The original intent was for a portion of the encryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to cipher, and 0 is always written to cipher\_length. The arguments cipher and cipher\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CBC\_DecryptInit()

```
fsp_err_t R_SCE_AES128CBC_DecryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector )
```

The R\_SCE\_AES128CBC\_DecryptInit() function performs preparations for the execution of an AES calculation, and writes the result to the first argument, handle. The value of handle is used as an argument in the subsequent R\_SCE\_AES128CBC\_DecryptUpdate() function and R\_SCE\_AES128CBC\_DecryptFinal() function.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initialization vector area (16byte)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128CBC\_DecryptUpdate()

```
fsp_err_t R_SCE_AES128CBC_DecryptUpdate ( sce_aes_handle_t * handle, uint8_t * cipher, uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES128CBC_DecryptUpdate()` function decrypts the second argument, `cipher`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the decryption result to the third argument, `plain`. After plaintext input is completed, call `R_SCE_AES128CBC_DecryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CBC\_DecryptFinal()

```
fsp_err_t R_SCE_AES128CBC_DecryptFinal ( sce_aes_handle_t * handle, uint8_t * plain, uint32_t * plain_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES128CBC\\_DecryptFinal\(\)](#) function writes the calculation result to the second argument, plain, and writes the length of the calculation result to the third argument, plain\_length. The original intent was for a portion of the decryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to plain, and 0 is always written to plain\_length. The arguments plain and plain\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CBC\_EncryptInit()

```
fsp_err_t R_SCE_AES256CBC_EncryptInit ( sce_aes_handle_t* handle, sce_aes_wrapped_key_t* wrapped_key, uint8_t* initial_vector )
```

The R\_SCE\_AES256CBC\_EncryptInit() function performs preparations for the execution of an AES calculation, and writes the result to the first argument, handle. The value of handle is used as an argument in the subsequent R\_SCE\_AES256CBC\_EncryptUpdate() function and R\_SCE\_AES256CBC\_EncryptFinal() function.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initial vector area (16byte)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256CBC\_EncryptUpdate()

```
fsp_err_t R_SCE_AES256CBC_EncryptUpdate ( sce_aes_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_length )
```

The `R_SCE_AES256CBC_EncryptUpdate()` function encrypts the second argument, `plain`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the encryption result to the third argument, `cipher`. After plaintext input is completed, call `R_SCE_AES256CBC_EncryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	<code>handle</code>	AES handler (work area)
[in]	<code>plain</code>	plaintext data area
[in,out]	<code>cipher</code>	ciphertext data area
[in,out]	<code>plain_length</code>	plaintext data length (must be a multiple of 16)

#### Return values

<code>FSP_SUCCESS</code>	Normal termination
<code>FSP_ERR_CRYPTOSCE_PARAMETER</code>	Input data is illegal.
<code>FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION</code>	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256CBC\_EncryptFinal()**

```
fsp_err_t R_SCE_AES256CBC_EncryptFinal ( sce_aes_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length )
```

Using the handle specified in the first argument, handle, the [R\\_SCE\\_AES256CBC\\_EncryptFinal\(\)](#) function writes the calculation result to the second argument, cipher, and writes the length of the calculation result to the third argument, cipher\_length. The original intent was for a portion of the encryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to cipher, and 0 is always written to cipher\_length. The arguments cipher and cipher\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CBC\_DecryptInit()

```
fsp_err_t R_SCE_AES256CBC_DecryptInit ( sce_aes_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector )
```

The R\_SCE\_AES256CBC\_DecryptInit() function performs preparations for the execution of an AES calculation, and writes the result to the first argument, handle. The value of handle is used as an argument in the subsequent R\_SCE\_AES256CBC\_DecryptUpdate() function and R\_SCE\_AES256CBC\_DecryptFinal() function.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initialization vector area (16byte)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Input illegal wrapped key.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256CBC\_DecryptUpdate()

```
fsp_err_t R_SCE_AES256CBC_DecryptUpdate ( sce_aes_handle_t * handle, uint8_t * cipher, uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES256CBC_DecryptUpdate()` function decrypts the second argument, `cipher`, utilizing the key index stored in the handle specified in the first argument, `handle`, and writes the ongoing status to this first argument. In addition, it writes the decryption result to the third argument, `plain`. After plaintext input is completed, call `R_SCE_AES256CBC_DecryptFinal()`.

Specify areas for `plain` and `cipher` that do not overlap. For `plain` and `cipher`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256CBC\_DecryptFinal()**

```
fsp_err_t R_SCE_AES256CBC_DecryptFinal ( sce_aes_handle_t * handle, uint8_t * plain, uint32_t * plain_length )
```

Using the handle specified in the first argument, handle, the **R\_SCE\_AES256CBC\_DecryptFinal()** function writes the calculation result to the second argument, plain, and writes the length of the calculation result to the third argument, plain\_length. The original intent was for a portion of the decryption result that was not a multiple of 16 bytes to be written to the second argument. However, as a result of the restriction that only multiples of 16 can be input to the Update function, nothing is ever written to plain, and 0 is always written to plain\_length. The arguments plain and plain\_length are provided for compatibility in anticipation of the time when this restriction is lifted.

**Parameters**

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128GCM\_EncryptInit()

```
fsp_err_t R_SCE_AES128GCM_EncryptInit ( sce_gcm_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector, uint32_t initial_vector_length )
```

The `R_SCE_AES128GCM_EncryptInit()` function performs preparations for the execution of an GCM calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128GCM_EncryptUpdate()` function and `R_SCE_AES128GCM_EncryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-GCM handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key
[in]	<code>initial_vector</code>	initialization vector area ( <code>initial_vector_length</code> byte)
[in]	<code>initial_vector_length</code>	initialization vector length (1 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128GCM\_EncryptUpdate()

```
fsp_err_t R_SCE_AES128GCM_EncryptUpdate ( sce_gcm_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_data_length, uint8_t * aad, uint32_t aad_length )
```

The `R_SCE_AES128GCM_EncryptUpdate()` function encrypts the plaintext specified in the second argument, `plain`, in GCM mode using the values specified for `wrapped_key` and `initial_vector` in `R_SCE_AES128GCM_EncryptInit()`, along with the additional authentication data specified in the fifth argument, `aad`. Inside this function, the data that is input by the user is buffered until the input values of `aad` and `plain` exceed 16 bytes. After the input data from `plain` reaches 16 bytes or more, the encryption result is output to the ciphertext data area specified in the third argument, `cipher`. The lengths of the `plain` and `aad` data to input are respectively specified in the fourth argument, `plain_data_length`, and the sixth argument, `aad_length`. For these, specify not the total byte count for the `aad` and `plain` input data, but rather the data length to input when the user calls this function. If the input values `plain` and `aad` are not divisible by 16 bytes, they will be padded inside the function. First process the data that is input from `aad`, and then process the data that is input from `plain`. If `aad` data is input after starting to input `plain` data, an error will occur. If `aad` data and `plain` data are input to this function at the same time, the `aad` data will be processed, and then the function will transition to the `plain` data input state.

Specify areas for `plain` and `cipher` that do not overlap. For `plain`, `cipher`, `initial_vector`, and `aad`, specify RAM addresses that are multiples of 4

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_data_length	plaintext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	After the data from <code>plain</code> was input, an invalid handle was input from <code>aad</code> .
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128GCM\_EncryptFinal()

```
fsp_err_t R_SCE_AES128GCM_EncryptFinal ( sce_gcm_handle_t * handle, uint8_t * cipher, uint32_t * cipher_data_length, uint8_t * atag )
```

If there is 16-byte fractional data indicated by the total data length of the value of plain that was input by R\_SCE\_AES128GCM\_EncryptUpdate (), the R\_SCE\_AES128GCM\_EncryptFinal() function will output the result of encrypting that fractional data to the ciphertext data area specified in the second argument, cipher. Here, the portion that does not reach 16 bytes will be padded with zeros. The authentication tag is output to the fourth argument, atag. For cipher and atag, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area (cipher_data_length byte)
[in,out]	cipher_data_length	ciphertext data length (0 always written here)
[in,out]	atag	authentication tag area

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128GCM\_DecryptInit()

```
fsp_err_t R_SCE_AES128GCM_DecryptInit ( sce_gcm_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector, uint32_t initial_vector_length )
```

The `R_SCE_AES128GCM_DecryptInit()` function performs preparations for the execution of an GCM calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128GCM_DecryptUpdate()` function and `R_SCE_AES128GCM_DecryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-GCM handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key
[in]	<code>initial_vector</code>	initialization vector area ( <code>initial_vector_length</code> byte)
[in]	<code>initial_vector_length</code>	initialization vector length (1 or more bytes)

#### Return values

<code>FSP_SUCCESS</code>	Normal termination
<code>FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT</code>	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
<code>FSP_ERR_CRYPTOSCE_KEY_SET_FAIL</code>	Invalid wrapped key was input.
<code>FSP_ERR_CRYPTOSCE_PARAMETER</code>	Input data is illegal.
<code>FSP_ERR_CRYPTOSCE_FAIL</code>	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128GCM\_DecryptUpdate()

```
fsp_err_t R_SCE_AES128GCM_DecryptUpdate ( sce_gcm_handle_t* handle, uint8_t* cipher,
uint8_t* plain, uint32_t cipher_data_length, uint8_t* aad, uint32_t aad_length )
```

The `R_SCE_AES128GCM_DecryptUpdate()` function decrypts the ciphertext specified in the second argument, `cipher`, in GCM mode using the values specified for `wrapped_key` and `initial_vector` in `R_SCE_AES128GCM_DecryptInit()`, along with the additional authentication data specified in the fifth argument, `aad`. Inside this function, the data that is input by the user is buffered until the input values of `aad` and `plain` exceed 16 bytes. After the input data from `cipher` reaches 16 bytes or more, the decryption result is output to the plaintext data area specified in the third argument, `plain`. The lengths of the cipher and `aad` data to input are respectively specified in the fourth argument, `cipher_data_length`, and the sixth argument, `aad_length`. For these, specify not the total byte count for the `aad` and `cipher` input data, but rather the data length to input when the user calls this function. If the input values `cipher` and `aad` are not divisible by 16 bytes, they will be padded inside the function. First process the data that is input from `aad`, and then process the data that is input from `cipher`. If `aad` data is input after starting to input `cipher` data, an error will occur. If `aad` data and `cipher` data are input to this function at the same time, the `aad` data will be processed, and then the function will transition to the `cipher` data input state. Specify areas for `plain` and `cipher` that do not overlap. For `plain`, `cipher`, `stage`, `initial_vector`, and `aad`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area
[in]	plain	plaintext data area
[in]	cipher_data_length	ciphertext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	After the data from <code>plain</code> was input, an invalid handle was input from <code>aad</code> .
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128GCM\_DecryptFinal()

```
fsp_err_t R_SCE_AES128GCM_DecryptFinal ( sce_gcm_handle_t* handle, uint8_t* plain, uint32_t* plain_data_length, uint8_t* atag, uint32_t atag_length )
```

The `R_SCE_AES128GCM_DecryptFinal()` function decrypts, in GCM mode, the fractional ciphertext specified by `R_SCE_AES128GCM_DecryptUpdate()` that does not reach 16 bytes, and ends GCM decryption. The encryption data and authentication tag are respectively output to the plaintext data area specified in the second argument, `plain`, and the authentication tag area specified in the fourth argument, `atag`. The decoded data length is output to the third argument, `plain_data_length`. If authentication fails, the return value will be `TSIP_ERR_AUTHENTICATION`. For the fourth argument, `atag`, input 16 bytes or less. If it is less than 16 bytes, it will be padded with zeros inside the function. For `plain` and `atag`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	plain	plaintext data area (cipher_data_length byte)
[in,out]	plain_data_length	plaintext data length (0 always written here)
[in,out]	atag	authentication tag area (atag_length byte)
[in]	atag_length	authentication tag length (4,8,12,13,14,15,16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256GCM\_EncryptInit()

```
fsp_err_t R_SCE_AES256GCM_EncryptInit ( sce_gcm_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector, uint32_t initial_vector_length )
```

The `R_SCE_AES256GCM_EncryptInit()` function performs preparations for the execution of an GCM calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES256GCM_EncryptUpdate()` function and `R_SCE_AES256GCM_EncryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-GCM handler (work area)
[in]	<code>wrapped_key</code>	256-bit AES wrapped key
[in]	<code>initial_vector</code>	initialization vector area ( <code>initial_vector_length</code> byte)
[in]	<code>initial_vector_length</code>	initialization vector length (1 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTTO_SCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256GCM\_EncryptUpdate()

```
fsp_err_t R_SCE_AES256GCM_EncryptUpdate ( sce_gcm_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_data_length, uint8_t * aad, uint32_t aad_length )
```

The `R_SCE_AES256GCM_EncryptUpdate()` function encrypts the plaintext specified in the second argument, `plain`, in GCM mode using the values specified for `wrapped_key` and `initial_vector` in `R_SCE_AES256GCM_EncryptInit()`, along with the additional authentication data specified in the fifth argument, `aad`. Inside this function, the data that is input by the user is buffered until the input values of `aad` and `plain` exceed 16 bytes. After the input data from `plain` reaches 16 bytes or more, the encryption result is output to the ciphertext data area specified in the third argument, `cipher`. The lengths of the `plain` and `aad` data to input are respectively specified in the fourth argument, `plain_data_length`, and the sixth argument, `aad_length`. For these, specify not the total byte count for the `aad` and `plain` input data, but rather the data length to input when the user calls this function. If the input values `plain` and `aad` are not divisible by 16 bytes, they will be padded inside the function. First process the data that is input from `aad`, and then process the data that is input from `plain`. If `aad` data is input after starting to input `plain` data, an error will occur. If `aad` data and `plain` data are input to this function at the same time, the `aad` data will be processed, and then the function will transition to the `plain` data input state.

Specify areas for `plain` and `cipher` that do not overlap. For `plain`, `cipher`, `initial_vector`, and `aad`, specify RAM addresses that are multiples of 4

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_data_length	plaintext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	After the data from <code>plain</code> was input, an invalid handle was input from <code>aad</code> .
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256GCM\_EncryptFinal()

```
fsp_err_t R_SCE_AES256GCM_EncryptFinal ( sce_gcm_handle_t * handle, uint8_t * cipher, uint32_t * cipher_data_length, uint8_t * atag )
```

If there is 16-byte fractional data indicated by the total data length of the value of plain that was input by R\_SCE\_AES256GCM\_EncryptUpdate (), the R\_SCE\_AES256GCM\_EncryptFinal() function will output the result of encrypting that fractional data to the ciphertext data area specified in the second argument, cipher. Here, the portion that does not reach 16 bytes will be padded with zeros. The authentication tag is output to the fourth argument, atag. For cipher and atag, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area (cipher_data_length byte)
[in,out]	cipher_data_length	ciphertext data length (0 always written here)
[in,out]	atag	authentication tag area

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256GCM\_DecryptInit()

```
fsp_err_t R_SCE_AES256GCM_DecryptInit ( sce_gcm_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * initial_vector, uint32_t initial_vector_length )
```

The `R_SCE_AES256GCM_DecryptInit()` function performs preparations for the execution of an GCM calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES256GCM_DecryptUpdate()` function and `R_SCE_AES256GCM_DecryptFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-GCM handler (work area)
[in]	<code>wrapped_key</code>	256-bit AES wrapped key
[in]	<code>initial_vector</code>	initialization vector area ( <code>initial_vector_length</code> byte)
[in]	<code>initial_vector_length</code>	initialization vector length (1 or more bytes)

#### Return values

<code>FSP_SUCCESS</code>	Normal termination
<code>FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT</code>	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
<code>FSP_ERR_CRYPTOSCE_KEY_SET_FAIL</code>	Invalid wrapped key was input.
<code>FSP_ERR_CRYPTOSCE_PARAMETER</code>	Input data is illegal.
<code>FSP_ERR_CRYPTOSCE_FAIL</code>	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256GCM\_DecryptUpdate()

```
fsp_err_t R_SCE_AES256GCM_DecryptUpdate ( sce_gcm_handle_t* handle, uint8_t* cipher,
uint8_t* plain, uint32_t cipher_data_length, uint8_t* aad, uint32_t aad_length )
```

The `R_SCE_AES256GCM_DecryptUpdate()` function decrypts the ciphertext specified in the second argument, `cipher`, in GCM mode using the values specified for `wrapped_key` and `initial_vector` in `R_SCE_AES256GCM_DecryptInit()`, along with the additional authentication data specified in the fifth argument, `aad`. Inside this function, the data that is input by the user is buffered until the input values of `aad` and `plain` exceed 16 bytes. After the input data from `cipher` reaches 16 bytes or more, the decryption result is output to the plaintext data area specified in the third argument, `plain`. The lengths of the cipher and `aad` data to input are respectively specified in the fourth argument, `cipher_data_length`, and the sixth argument, `aad_length`. For these, specify not the total byte count for the `aad` and cipher input data, but rather the data length to input when the user calls this function. If the input values `cipher` and `aad` are not divisible by 16 bytes, they will be padded inside the function. First process the data that is input from `aad`, and then process the data that is input from `cipher`. If `aad` data is input after starting to input cipher data, an error will occur. If `aad` data and cipher data are input to this function at the same time, the `aad` data will be processed, and then the function will transition to the cipher data input state. Specify areas for `plain` and `cipher` that do not overlap. For `plain`, `cipher`, `stage`, `initial_vector`, and `aad`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	<code>handle</code>	AES-GCM handler (work area)
[in,out]	<code>cipher</code>	ciphertext data area
[in]	<code>plain</code>	plaintext data area
[in]	<code>cipher_data_length</code>	ciphertext data length (0 or more bytes)
[in]	<code>aad</code>	additional authentication data ( <code>aad_length</code> byte)
[in]	<code>aad_length</code>	additional authentication data length (0 or more bytes)

#### Return values

<code>FSP_SUCCESS</code>	Normal termination
<code>FSP_ERR_CRYPTOSCE_PARAMETER</code>	After the data from <code>plain</code> was input, an invalid handle was input from <code>aad</code> .
<code>FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION</code>	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256GCM\_DecryptFinal()

```
fsp_err_t R_SCE_AES256GCM_DecryptFinal ( sce_gcm_handle_t* handle, uint8_t* plain, uint32_t* plain_data_length, uint8_t* atag, uint32_t atag_length )
```

The `R_SCE_AES256GCM_DecryptFinal()` function decrypts, in GCM mode, the fractional ciphertext specified by `R_SCE_AES256GCM_DecryptUpdate()` that does not reach 16 bytes, and ends GCM decryption. The encryption data and authentication tag are respectively output to the plaintext data area specified in the second argument, `plain`, and the authentication tag area specified in the fourth argument, `atag`. The decoded data length is output to the third argument, `plain_data_length`. If authentication fails, the return value will be `TSIP_ERR_AUTHENTICATION`. For the fourth argument, `atag`, input 16 bytes or less. If it is less than 16 bytes, it will be padded with zeros inside the function. For `plain` and `atag`, specify RAM addresses that are multiples of 4.

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	plain	plaintext data area (cipher_data_length byte)
[in,out]	plain_data_length	plaintext data length (0 always written here)
[in,out]	atag	authentication tag area (atag_length byte)
[in]	atag_length	authentication tag length (4,8,12,13,14,15,16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CCM\_EncryptInit()

```
fsp_err_t R_SCE_AES128CCM_EncryptInit ( sce_ccm_handle_t* handle, sce_aes_wrapped_key_t* wrapped_key, uint8_t* nonce, uint32_t nonce_length, uint8_t* adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length )
```

The `R_SCE_AES128CCM_EncryptInit()` function prepares to perform CCM computation and writes the result to the first argument, `handle`. The succeeding functions `R_SCE_AES128CCM_EncryptUpdate()` and `R_SCE_AES128CCM_EncryptFinal()` use `handle` as an argument.

#### Parameters

[in,out]	<code>handle</code>	AES-CCM handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key
[in]	<code>nonce</code>	Nonce
[in]	<code>nonce_length</code>	Nonce data length (7 to 13 bytes)
[in]	<code>adata</code>	additional authentication data
[in]	<code>a_length</code>	additional authentication data length (0 to 110 bytes)
[in]	<code>payload_length</code>	Payload length (any number of bytes)
[in]	<code>mac_length</code>	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128CCM\_EncryptUpdate()

```
fsp_err_t R_SCE_AES128CCM_EncryptUpdate ( sce_ccm_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_length )
```

The `R_SCE_AES128CCM_EncryptUpdate()` function encrypts the plaintext specified in the second argument, `plain`, in CCM mode using the values specified by `wrapped_key`, `nonce`, and `adata` in `R_SCE_AES128CCM_EncryptInit()`. This function buffers internally the data input by the user until the input value of `plain` exceeds 16 bytes. Once the amount of `plain` input data is 16 bytes or greater, the encrypted result is output to `cipher`, which is specified in the third argument. Use `payload_length` in `R_SCE_AES128CCM_EncryptInit()` to specify the total data length of `plain` that will be input. Use `plain_length` in this function to specify the data length to be input when the user calls this function. If the input value of `plain` is less than 16 bytes, the function performs padding internally.

Ensure that the areas allocated to `plain` and `cipher` do not overlap. Also, specify RAM addresses that are multiples of 4 for `plain` and `cipher`.

#### Parameters

[in,out]	<code>handle</code>	AES-CCM handler (work area)
[in]	<code>plain</code>	plaintext data area
[in,out]	<code>cipher</code>	ciphertext data area
[in]	<code>plain_length</code>	plaintext data length

#### Return values

<code>FSP_SUCCESS</code>	Normal termination
<code>FSP_ERR_CRYPT_SCE_PROHIBIT_FUNCTION</code>	An invalid function was called.
<code>FSP_ERR_CRYPT_SCE_PARAMETER</code>	An invalid handle was input.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CCM\_EncryptFinal()

```
fsp_err_t R_SCE_AES128CCM_EncryptFinal ( sce_ccm_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length, uint8_t * mac, uint32_t mac_length )
```

If the data length of plain input in `R_SCE_AES128CCM_EncryptUpdate()` results in leftover data after 16 bytes, the `R_SCE_AES128CCM_EncryptFinal()` function outputs the leftover encrypted data to `cipher`, which is specified in the second argument. The MAC value is output to the fourth argument, `mac`. Set the fifth argument, `mac_length` to the same value as that specified for the argument `mac_length` in `Aes128CcmEncryptInit()`. Also, specify RAM addresses that are multiples of 4 for `cipher` and `mac`.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	cipher	ciphertext data area
[in,out]	cipher_length	ciphertext data length
[in,out]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CCM\_DecryptInit()

```
fsp_err_t R_SCE_AES128CCM_DecryptInit ( sce_ccm_handle_t * handle, sce_aes_wrapped_key_t *
wrapped_key, uint8_t * nonce, uint32_t nonce_length, uint8_t * adata, uint8_t a_length, uint32_t
payload_length, uint32_t mac_length )
```

The `R_SCE_AES128CCM_DecryptInit()` function prepares to perform CCM computation and writes the result to the first argument, `handle`. The succeeding functions `R_SCE_AES128CCM_DecryptUpdate()` and `R_SCE_AES128CCM_DecryptFinal()` use `handle` as an argument.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES128CCM\_DecryptUpdate()

```
fsp_err_t R_SCE_AES128CCM_DecryptUpdate ( sce_ccm_handle_t * handle, uint8_t * cipher,
uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES128CCM_DecryptUpdate()` function decrypts the ciphertext specified by the second argument, `cipher`, in CCM mode using the values specified by `wrapped_key`, `nonce`, and `adata` in `R_SCE_AES128CCM_DecryptInit()`. This function buffers internally the data input by the user until the input value of `cipher` exceeds 16 bytes. Once the amount of `cipher` input data is 16 bytes or greater, the decrypted result is output to `plain`, which is specified in the third argument. Use `payload_length` in `R_SCE_AES128CCM_DecryptInit()` to specify the total data length of `cipher` that will be input. Use `cipher_length` in this function to specify the data length to be input when the user calls this function. If the input value of `cipher` is less than 16 bytes, the function performs padding internally.

Ensure that the areas allocated to `cipher` and `plain` do not overlap. Also, specify RAM addresses that are multiples of 4 for `cipher` and `plain`.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in]	cipher_length	ciphertext data length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128CCM\_DecryptFinal()**

```
fsp_err_t R_SCE_AES128CCM_DecryptFinal ( sce_ccm_handle_t * handle, uint8_t * plain, uint32_t * plain_length, uint8_t * mac, uint32_t mac_length )
```

If the data length of cipher input in [R\\_SCE\\_AES128GCM\\_DecryptUpdate\(\)](#) results in leftover data after 16 bytes, the [R\\_SCE\\_AES128GCM\\_DecryptFinal\(\)](#) function outputs the leftover decrypted data to cipher, which is specified in the second argument. In addition, the function verifies the fourth argument, mac. Set the fifth argument, mac\_length, to the same value as that specified for the argument mac\_length in [Aes128CcmDecryptInit\(\)](#).

**Parameters**

[in,out]	handle	AES-CCM handler (work area)
[in,out]	plain	plaintext data area
[in,out]	plain_length	plaintext data length
[in]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	Internal error, or authentication failed.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CCM\_EncryptInit()

```
fsp_err_t R_SCE_AES256CCM_EncryptInit ( sce_ccm_handle_t* handle, sce_aes_wrapped_key_t* wrapped_key, uint8_t* nonce, uint32_t nonce_length, uint8_t* adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length )
```

The R\_SCE\_AES256CCM\_EncryptInit() function prepares to perform CCM computation and writes the result to the first argument, handle. The succeeding functions R\_SCE\_AES256CCM\_EncryptUpdate() and R\_SCE\_AES256CCM\_EncryptFinal() use handle as an argument.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256CCM\_EncryptUpdate()

```
fsp_err_t R_SCE_AES256CCM_EncryptUpdate ( sce_ccm_handle_t * handle, uint8_t * plain, uint8_t * cipher, uint32_t plain_length )
```

The `R_SCE_AES256CCM_EncryptUpdate()` function encrypts the plaintext specified in the second argument, `plain`, in CCM mode using the values specified by `wrapped_key`, `nonce`, and `adata` in `R_SCE_AES256CCM_EncryptInit()`. This function buffers internally the data input by the user until the input value of `plain` exceeds 16 bytes. Once the amount of plain input data is 16 bytes or greater, the encrypted result is output to `cipher`, which is specified in the third argument. Use `payload_length` in `R_SCE_AES256CCM_EncryptInit()` to specify the total data length of plain that will be input. Use `plain_length` in this function to specify the data length to be input when the user calls this function. If the input value of `plain` is less than 16 bytes, the function performs padding internally.

Ensure that the areas allocated to `plain` and `cipher` do not overlap. Also, specify RAM addresses that are multiples of 4 for `plain` and `cipher`.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_length	plaintext data length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPT_SCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPT_SCE_PARAMETER	An invalid handle was input.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CCM\_EncryptFinal()

```
fsp_err_t R_SCE_AES256CCM_EncryptFinal ( sce_ccm_handle_t * handle, uint8_t * cipher, uint32_t * cipher_length, uint8_t * mac, uint32_t mac_length )
```

If the data length of plain input in `R_SCE_AES256CCM_EncryptUpdate()` results in leftover data after 16 bytes, the `R_SCE_AES256CCM_EncryptFinal()` function outputs the leftover encrypted data to `cipher`, which is specified in the second argument. The MAC value is output to the fourth argument, `mac`. Set the fifth argument, `mac_length` to the same value as that specified for the argument `mac_length` in `Aes256CcmEncryptInit()`. Also, specify RAM addresses that are multiples of 4 for `cipher` and `mac`.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	cipher	ciphertext data area
[in,out]	cipher_length	ciphertext data length
[in,out]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CCM\_DecryptInit()

```
fsp_err_t R_SCE_AES256CCM_DecryptInit ( sce_ccm_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key, uint8_t * nonce, uint32_t nonce_length, uint8_t * adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length )
```

The `R_SCE_AES256CCM_DecryptInit()` function prepares to perform CCM computation and writes the result to the first argument, `handle`. The succeeding functions `R_SCE_AES256CCM_DecryptUpdate()` and `R_SCE_AES256CCM_DecryptFinal()` use `handle` as an argument.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_AES256CCM\_DecryptUpdate()

```
fsp_err_t R_SCE_AES256CCM_DecryptUpdate ( sce_ccm_handle_t * handle, uint8_t * cipher,
uint8_t * plain, uint32_t cipher_length )
```

The `R_SCE_AES256CCM_DecryptUpdate()` function decrypts the ciphertext specified by the second argument, `cipher`, in CCM mode using the values specified by `wrapped_key`, `nonce`, and `adata` in `R_SCE_AES256CCM_DecryptInit()`. This function buffers internally the data input by the user until the input value of `cipher` exceeds 16 bytes. Once the amount of `cipher` input data is 16 bytes or greater, the decrypted result is output to `plain`, which is specified in the third argument. Use `payload_length` in `R_SCE_AES256CCM_DecryptInit()` to specify the total data length of `cipher` that will be input. Use `cipher_length` in this function to specify the data length to be input when the user calls this function. If the input value of `cipher` is less than 16 bytes, the function performs padding internally.

Ensure that the areas allocated to `cipher` and `plain` do not overlap. Also, specify RAM addresses that are multiples of 4 for `cipher` and `plain`.

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in]	cipher_length	ciphertext data length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CCM\_DecryptFinal()

```
fsp_err_t R_SCE_AES256CCM_DecryptFinal ( sce_ccm_handle_t * handle, uint8_t * plain, uint32_t * plain_length, uint8_t * mac, uint32_t mac_length )
```

If the data length of cipher input in [R\\_SCE\\_AES256GCM\\_DecryptUpdate\(\)](#) results in leftover data after 16 bytes, the [R\\_SCE\\_AES256GCM\\_DecryptFinal\(\)](#) function outputs the leftover decrypted data to cipher, which is specified in the second argument. In addition, the function verifies the fourth argument, mac. Set the fifth argument, mac\_length, to the same value as that specified for the argument mac\_length in [Aes256CcmDecryptInit\(\)](#).

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	plain	plaintext data area
[in,out]	plain_length	plaintext data length
[in]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	Internal error, or authentication failed.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CMAC\_GenerateInit()

```
fsp_err_t R_SCE_AES128CMAC_GenerateInit ( sce_cmac_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES128CMAC_GenerateInit()` function performs preparations for the execution of an CMAC calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128CMAC_GenerateUpdate()` function and `R_SCE_AES128CMAC_GenerateFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-CMAC handler (work area)
[in]	<code>wrapped_key</code>	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CMAC\_GenerateUpdate()

```
fsp_err_t R_SCE_AES128CMAC_GenerateUpdate ( sce_cmact_handle_t * handle, uint8_t * message,
uint32_t message_length )
```

The `R_SCE_AES128CMAC_GenerateUpdate()` function performs MAC value generation based on the message specified in the second argument, `message`, using the value specified for `wrapped_key` in `R_SCE_AES128CMAC_GenerateInit()`. Inside this function, the data that is input by the user is buffered until the input value of `message` exceeds 16 bytes. The length of the message data to input is specified in the third argument, `message_len`. For these, input not the total byte count for message input data, but rather the message data length to input when the user calls this function. If the input value, `message`, is not a multiple of 16 bytes, it will be padded within the function. For `message`, specify a RAM address that are multiples of 4.

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128CMAC\_GenerateFinal()**

```
fsp_err_t R_SCE_AES128CMAC_GenerateFinal ( sce_cmac_handle_t* handle, uint8_t* mac )
```

The `R_SCE_AES128CMAC_GenerateFinal()` function outputs the MAC value to the MAC data area specified in the second argument, `mac`, and ends CMAC mode.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (16byte)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Not used.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES128CMAC\_VerifyInit()

```
fsp_err_t R_SCE_AES128CMAC_VerifyInit ( sce_cmac_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES128CMAC_VerifyInit()` function performs preparations for the execution of a CMAC calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES128CMAC_VerifyUpdate()` function and `R_SCE_AES128CMAC_VerifyFinal()` function.

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	128-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_AES128CMAC\_VerifyUpdate()**

```
fsp_err_t R_SCE_AES128CMAC_VerifyUpdate ( sce_cmact_handle_t * handle, uint8_t * message,
uint32_t message_length )
```

The **R\_SCE\_AES128CMAC\_VerifyUpdate()** function performs MAC value generation based on the message specified in the second argument, `message`, using the value specified for `wrapped_key` in **R\_SCE\_AES128CMAC\_VerifyInit()**. Inside this function, the data that is input by the user is buffered until the input value of `message` exceeds 16 bytes. The length of the message data to input is specified in the third argument, `message_len`. For these, input not the total byte count for message input data, but rather the message data length to input when the user calls this function. If the input value, `message`, is not a multiple of 16 bytes, it will be padded within the function. For `message`, specify a RAM address that are multiples of 4.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES128CMAC\_VerifyFinal()**

```
fsp_err_t R_SCE_AES128CMAC_VerifyFinal ( sce_cmact_handle_t* handle, uint8_t* mac, uint32_t mac_length )
```

The `R_SCE_AES128CMAC_VerifyFinal()` function inputs the MAC value in the MAC data area specified in the second argument, `mac`, and verifies the MAC value. If authentication fails, the return value will be `TSIP_ERR_AUTHENTICATION`. If the MAC value is less than 16 bytes, it will be padded with zeros inside the function.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (mac_length byte)
[in,out]	mac_length	MAC data length (2 to 16 bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CMAC\_GenerateInit()

```
fsp_err_t R_SCE_AES256CMAC_GenerateInit ( sce_cmac_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_AES256CMAC_GenerateInit()` function performs preparations for the execution of an CMAC calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_AES256CMAC_GenerateUpdate()` function and `R_SCE_AES256CMAC_GenerateFinal()` function.

#### Parameters

[in,out]	<code>handle</code>	AES-CMAC handler (work area)
[in]	<code>wrapped_key</code>	256-bit AES wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_AES256CMAC\_GenerateUpdate()

```
fsp_err_t R_SCE_AES256CMAC_GenerateUpdate ( sce_cmac_handle_t * handle, uint8_t * message,
uint32_t message_length )
```

The `R_SCE_AES256CMAC_GenerateUpdate()` function performs MAC value generation based on the message specified in the second argument, `message`, using the value specified for `wrapped_key` in `R_SCE_AES256CMAC_GenerateInit()`. Inside this function, the data that is input by the user is buffered until the input value of `message` exceeds 16 bytes. The length of the message data to input is specified in the third argument, `message_len`. For these, input not the total byte count for message input data, but rather the message data length to input when the user calls this function. If the input value, `message`, is not a multiple of 16 bytes, it will be padded within the function. For `message`, specify a RAM address that are multiples of 4.

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256CMAC\_GenerateFinal()**

```
fsp_err_t R_SCE_AES256CMAC_GenerateFinal ( sce_cmac_handle_t* handle, uint8_t* mac )
```

The `R_SCE_AES256CMAC_GenerateFinal()` function outputs the MAC value to the MAC data area specified in the second argument, `mac`, and ends CMAC mode.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (16byte)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTTO_SCE_AUTHENTICATION	Not used.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_AES256CMAC\_VerifyInit()

```
fsp_err_t R_SCE_AES256CMAC_VerifyInit ( sce_cmac_handle_t * handle, sce_aes_wrapped_key_t * wrapped_key )
```

The R\_SCE\_AES256CMAC\_VerifyInit() function performs preparations for the execution of a CMAC calculation, and writes the result to the first argument, handle. The value of handle is used as an argument in the subsequent R\_SCE\_AES256CMAC\_VerifyUpdate() function and R\_SCE\_AES256CMAC\_VerifyFinal() function.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	256-bit AES wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	Internal error occurred.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_AES256CMAC\_VerifyUpdate()

```
fsp_err_t R_SCE_AES256CMAC_VerifyUpdate ( sce_cmac_handle_t * handle, uint8_t * message,
uint32_t message_length )
```

The R\_SCE\_AES256CMAC\_VerifyUpdate() function performs MAC value generation based on the message specified in the second argument, message, using the value specified for wrapped\_key in R\_SCE\_AES256CMAC\_VerifyInit(). Inside this function, the data that is input by the user is buffered until the input value of message exceeds 16 bytes. The length of the message data to input is specified in the third argument, message\_len. For these, input not the total byte count for message input data, but rather the message data length to input when the user calls this function. If the input value, message, is not a multiple of 16 bytes, it will be padded within the function. For message, specify a RAM address that are multiples of 4.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

◆ **R\_SCE\_AES256CMAC\_VerifyFinal()**

```
fsp_err_t R_SCE_AES256CMAC_VerifyFinal ( sce_cmact_handle_t * handle, uint8_t * mac, uint32_t mac_length )
```

The `R_SCE_AES256CMAC_VerifyFinal()` function inputs the MAC value in the MAC data area specified in the second argument, `mac`, and verifies the MAC value. If authentication fails, the return value will be `TSIP_ERR_AUTHENTICATION`. If the MAC value is less than 16 bytes, it will be padded with zeros inside the function.

**Parameters**

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (mac_length byte)
[in,out]	mac_length	MAC data length (2 to 16 bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_SHA256\_Init()**

```
fsp_err_t R_SCE_SHA256_Init ( sce_sha_md5_handle_t * handle)
```

The `R_SCE_SHA256_Init()` function performs preparations for the execution of an SHA-256 hash calculation, and writes the result to the first argument, `handle`. The value of `handle` is used as an argument in the subsequent `R_SCE_SHA256_Update()` function and `R_SCE_SHA256_Final()` function.

**Parameters**

[in,out]	handle	SHA handler (work area)
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**Return values**

FSP_SUCCESS	Normal termination
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**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_SHA256\_Update()

```
fsp_err_t R_SCE_SHA256_Update ( sce_sha_md5_handle_t * handle, uint8_t * message, uint32_t message_length )
```

The `R_SCE_SHA256_Update()` function calculates a hash value based on the second argument, `message`, and the third argument, `message_length`, and writes the ongoing status to the first argument, `handle`. After message input is completed, call `R_SCE_SHA256_Final()`.

#### Parameters

[in,out]	handle	SHA handler (work area)
[in]	message	message data area
[in]	message_length	message data length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_SHA256\_Final()

```
fsp_err_t R_SCE_SHA256_Final ( sce_sha_md5_handle_t * handle, uint8_t * digest, uint32_t *
digest_length )
```

Using the handle specified in the first argument, handle, the R\_SCE\_SHA256\_Final() function writes the calculation result to the second argument, digest, and writes the length of the calculation result to the third argument, digest\_length.

**Parameters**

[in,out]	handle	SHA handler (work area)
[in,out]	digest	hash data area
[in,out]	digest_length	hash data length (32bytes)

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_SHA256HMAC\_GenerateInit()

```
fsp_err_t R_SCE_SHA256HMAC_GenerateInit ( sce_hmac_sha_handle_t* handle,
sce_hmac_sha_wrapped_key_t* wrapped_key )
```

The R\_SCE\_SHA256HMAC\_GenerateInit() function uses the second argument wrapped\_key to prepare for execution of SHA256-HMAC calculation, then writes the result to the first argument handle. The argument handle is used by the subsequent R\_SCE\_SHA256HMAC\_GenerateUpdate() function or R\_SCE\_SHA256HMAC\_GenerateFinal() function.

#### Parameters

[in,out]	handle	SHA-HMAC handler (work area)
[in]	wrapped_key	MAC wrapped key

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	An invalid MAC wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_SHA256HMAC\_GenerateUpdate()

```
fsp_err_t R_SCE_SHA256HMAC_GenerateUpdate ( sce_hmac_sha_handle_t* handle, uint8_t* message, uint32_t message_length )
```

The `R_SCE_SHA256HMAC_GenerateUpdate()` function uses the handle specified by the first argument `handle`, calculates a hash value from the second argument `message` and third argument `message_length`, then writes the intermediate result to the first argument `handle`. After message input finishes, call the `R_SCE_SHA256HMAC_GenerateFinal()` function.

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in]	message	Message area
[in]	message_length	Message length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_SHA256HMAC\_GenerateFinal()

```
fsp_err_t R_SCE_SHA256HMAC_GenerateFinal ( sce_hmac_sha_handle_t* handle, uint8_t* mac )
```

The `R_SCE_SHA256HMAC_GenerateFinal()` function uses the handle specified by the first argument `handle` and writes the calculation result to the second argument `mac`.

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in,out]	mac	HMAC area (32 bytes)

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_SHA256HMAC\_VerifyInit()

```
fsp_err_t R_SCE_SHA256HMAC_VerifyInit ( sce_hmac_sha_handle_t* handle,
sce_hmac_sha_wrapped_key_t* wrapped_key )
```

The R\_SCE\_SHA256HMAC\_VerifyInit() function uses the second argument wrapped\_key to prepare for execution of SHA256-HMAC calculation, then writes the result to the first argument handle. The argument handle is used by the subsequent R\_SCE\_SHA256HMAC\_VerifyUpdate() function or R\_SCE\_SHA256HMAC\_VerifyFinal() function.

**Parameters**

[in,out]	handle	SHA-HMAC handler (work area)
[in]	wrapped_key	MAC wrapped key

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_KEYSET_FAIL	An invalid MAC wrapped key was input.
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_SHA256HMAC\_VerifyUpdate()

```
fsp_err_t R_SCE_SHA256HMAC_VerifyUpdate ( sce_hmac_sha_handle_t * handle, uint8_t *
message, uint32_t message_length )
```

The `R_SCE_SHA256HMAC_VerifyUpdate()` function uses the handle specified by the first argument `handle`, calculates a hash value from the second argument `message` and third argument `message_length`, then writes the intermediate result to the first argument `handle`. After message input finishes, call the `R_SCE_SHA256HMAC_VerifyFinal()` function.

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in]	message	Message area
[in]	message_length	Message length

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_SHA256HMAC\_VerifyFinal()**

```
fsp_err_t R_SCE_SHA256HMAC_VerifyFinal ( sce_hmac_sha_handle_t* handle, uint8_t* mac,
uint32_t mac_length )
```

The `R_SCE_SHA256HMAC_VerifyFinal()` function uses the handle specified by the first argument handle and verifies the mac value from the second argument mac and third argument mac\_length. Input a value in bytes from 4 to 32 as mac\_length.

**Parameters**

[in,out]	handle	SHA-HMAC handle (work area)
[in]	mac	HMAC area
[in]	mac_length	HMAC length

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

◆ **R\_SCE\_RSASSA\_PKCS1024\_SignatureGenerate()**

```
fsp_err_t R_SCE_RSASSA_PKCS1024_SignatureGenerate ( sce_rsa_byte_data_t* message_hash,
sce_rsa_byte_data_t* signature, sce_rsa1024_private_wrapped_key_t* wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS1024_SignatureGenerate()` function generates, in accordance with RSASSA-PKCS1-V1\_5, a signature from the message text or hash value that is input in the first argument, message\_hash, using the private wrapped key input to the third argument, wrapped\_key, and writes the signature text to the second argument, signature. When a message is specified in the first argument, message\_hash->data\_type, a hash value is calculated for the message as specified by the fourth argument, hash\_type. When specifying a hash value in the first argument, message\_hash->data\_type, a hash value calculated with a hash algorithm as specified by the fourth argument, hash\_type, must be input to message\_hash->pdata.

**Parameters**

[in]	message_hash	Message or hash value to which to attach signature <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> </ul>
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			<ul style="list-style-type: none"> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in,out]	signature		Signature text storage destination information <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : data length</li> </ul>
[in]	wrapped_key		Inputs the 1024-bit RSA private wrapped key.
[in]	hash_type		Only HW_SCE_RSA_HASH_SHA256 is supported

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_RSASSA\_PKCS1024\_SignatureVerify()

```
fsp_err_t R_SCE_RSASSA_PKCS1024_SignatureVerify ( sce_rsa_byte_data_t * signature,
sce_rsa_byte_data_t * message_hash, sce_rsa1024_public_wrapped_key_t * wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS1024_SignatureVerify()` function verifies, in accordance with RSASSA-PKCS1-V1\_5, the signature text input to the first argument `signature`, and the message text or hash value input to the second argument, `message_hash`, using the public wrapped key input to the third argument, `wrapped_key`. When a message is specified in the second argument, `message_hash->data_type`, a hash value is calculated using the public wrapped key input to the third argument, `wrapped_key`, and as specified by the fourth argument, `hash_type`. When specifying a hash value in the second argument, `message_hash->data_type`, a hash value calculated with a hash algorithm as specified by the fourth argument, `hash_type`, must be input to `message_hash->pdata`.

**Parameters**

[in]	signature	Signature text information to verify <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : Specifies effective data length of the array</li> </ul>
[in]	message_hash	Message text or hash value to verify <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.
[in]	hash_type	Only

		HW_SCE_RSA_HASH_SHA256 is supported
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**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_RSASSA\_PKCS2048\_SignatureGenerate()**

```
fsp_err_t R_SCE_RSASSA_PKCS2048_SignatureGenerate ( sce_rsa_byte_data_t* message_hash,
sce_rsa_byte_data_t* signature, sce_rsa2048_private_wrapped_key_t* wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS2048_SignatureGenerate()` function generates, in accordance with RSASSA-PKCS1-V1\_5, a signature from the message text or hash value that is input in the first argument, `message_hash`, using the private wrapped key input to the third argument, `wrapped_key`, and writes the signature text to the second argument, `signature`. When a message is specified in the first argument, `message_hash->data_type`, a hash value is calculated for the message as specified by the fourth argument, `hash_type`. When specifying a hash value in the first argument, `message_hash->data_type`, a hash value calculated with a hash algorithm as specified by the fourth argument, `hash_type`, must be input to `message_hash->pdata`.

**Parameters**

[in]	message_hash	Message or hash value to which to attach signature <ul style="list-style-type: none"> <li>• <code>message_hash-&gt;pdata</code> : Specifies pointer to array storing the message or hash value</li> <li>• <code>message_hash-&gt;data_length</code> : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>• <code>message_hash-&gt;data_type</code> : Selects the</li> </ul>
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		data type of message_hash (Message: 0 Hash value: 1)
[in,out]	signature	Signature text storage destination information <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : data length</li> </ul>
[in]	wrapped_key	Inputs the 2048-bit RSA private wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_RSASSA\_PKCS2048\_SignatureVerify()

```
fsp_err_t R_SCE_RSASSA_PKCS2048_SignatureVerify ( sce_rsa_byte_data_t * signature,
sce_rsa_byte_data_t * message_hash, sce_rsa2048_public_wrapped_key_t * wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS2048_SignatureVerify()` function verifies, in accordance with RSASSA-PKCS1-V1\_5, the signature text input to the first argument `signature`, and the message text or hash value input to the second argument, `message_hash`, using the public wrapped key input to the third argument, `wrapped_key`. When a message is specified in the second argument, `message_hash->data_type`, a hash value is calculated using the public wrapped key input to the third argument, `wrapped_key`, and as specified by the fourth argument, `hash_type`. When specifying a hash value in the second argument, `message_hash->data_type`, a hash value calculated with a hash algorithm as specified by the fourth argument, `hash_type`, must be input to `message_hash->pdata`.

**Parameters**

[in]	signature	Signature text information to verify <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : Specifies effective data length of the array</li> </ul>
[in]	message_hash	Message text or hash value to verify <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.
[in]	hash_type	Only

HW_SCE_RSA_HASH_SHA256 is supported
-------------------------------------

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_RSASSA\_PKCS3072\_SignatureVerify()**

```
fsp_err_t R_SCE_RSASSA_PKCS3072_SignatureVerify ( sce_rsa_byte_data_t * signature,
sce_rsa_byte_data_t * message_hash, sce_rsa3072_public_wrapped_key_t * wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS3072_SignatureVerify()` function verifies, in accordance with RSASSA-PKCS1-V1\_5, the signature text input to the first argument `signature`, and the message text or hash value input to the second argument, `message_hash`, using the public wrapped key input to the third argument, `wrapped_key`. When a message is specified in the second argument, `message_hash->data_type`, a hash value is calculated using the public wrapped key input to the third argument, `wrapped_key`, and as specified by the fourth argument, `hash_type`. When specifying a hash value in the second argument, `message_hash->data_type`, a hash value calculated with a hash algorithm as specified by the fourth argument, `hash_type`, must be input to `message_hash->pdata`.

**Parameters**

[in]	signature	Signature text information to verify <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : Specifies effective data length of the array</li> </ul>
[in]	message_hash	Message text or hash value to verify <ul style="list-style-type: none"> <li>message_hash-&gt;pdata</li> </ul>

			<p>ta : Specifies pointer to array storing the message or hash value</p> <ul style="list-style-type: none"> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]		wrapped_key	Inputs the 3072-bit RSA public wrapped key.
[in]		hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSASSA\_PKCS4096\_SignatureVerify()

```
fsp_err_t R_SCE_RSASSA_PKCS4096_SignatureVerify ( sce_rsa_byte_data_t * signature,
sce_rsa_byte_data_t * message_hash, sce_rsa4096_public_wrapped_key_t * wrapped_key, uint8_t
hash_type )
```

The `R_SCE_RSASSA_PKCS4096_SignatureVerify()` function verifies, in accordance with RSASSA-PKCS1-V1\_5, the signature text input to the first argument `signature`, and the message text or hash value input to the second argument, `message_hash`, using the public wrapped key input to the third argument, `wrapped_key`. When a message is specified in the second argument, `message_hash->data_type`, a hash value is calculated using the public wrapped key input to the third argument, `wrapped_key`, and as specified by the fourth argument, `hash_type`. When specifying a hash value in the second argument, `message_hash->data_type`, a hash value calculated with a hash algorithm as specified by the fourth argument, `hash_type`, must be input to `message_hash->pdata`.

#### Parameters

[in]	signature	Signature text information to verify <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing the signature text</li> <li>signature-&gt;data_length : Specifies effective data length of the array</li> </ul>
[in]	message_hash	Message text or hash value to verify <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.
[in]	hash_type	Only

		HW_SCE_RSA_HASH_SHA256 is supported
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**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_AUTHENTICATION	Authentication failed
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_RSAES\_PKCS1024\_Encrypt()

```
fsp_err_t R_SCE_RSAES_PKCS1024_Encrypt ( sce_rsa_byte_data_t* plain, sce_rsa_byte_data_t*
cipher, sce_rsa1024_public_wrapped_key_t* wrapped_key )
```

The R\_SCE\_RSAES\_PKCS1024\_Encrypt() function RSA-encrypts the plaintext input to the first argument, plain, according to RSAES-PKCS1-V1\_5. It writes the encryption result to the second argument, cipher.

**Parameters**

[in]	plain	plaintext <ul style="list-style-type: none"> <li>plain-&gt;pdata : Specifies pointer to array containing plaintext.</li> <li>plain-&gt;data_length : Specifies valid data length of plaintext array. data size &lt;= public key n size - 11</li> </ul>
[in,out]	cipher	ciphertext <ul style="list-style-type: none"> <li>cipher-&gt;pdata : Specifies pointer to array containing ciphertext.</li> <li>cipher-&gt;data_length : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

## ◆ R\_SCE\_RSAES\_PKCS1024\_Decrypt()

```
fsp_err_t R_SCE_RSAES_PKCS1024_Decrypt ( sce_rsa_byte_data_t* cipher, sce_rsa_byte_data_t*
plain, sce_rsa1024_private_wrapped_key_t* wrapped_key )
```

The R\_SCE\_RSAES\_PKCS1024\_Decrypt() function RSA-decrypts the ciphertext input to the first argument, cipher, according to RSAES-PKCS1-V1\_5. It writes the decryption result to the second argument, plain.

**Parameters**

[in]	cipher	ciphertext <ul style="list-style-type: none"> <li>• cipher-&gt;pdata : Specifies pointer to array containing ciphertext.</li> <li>• cipher-&gt;data_length : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in,out]	plain	plaintext <ul style="list-style-type: none"> <li>• plain-&gt;pdata : Specifies pointer to array containing plaintext.</li> <li>• plain-&gt;data_length : Inputs plaintext buffer size. The following size is required. Plaintext buffer size &gt;= public key n size -11. Outputs valid data length after decryption (public key n size).</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA private wrapped key.

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.

FSP_ERR_CRYPT0_SCE_FAIL	An internal error occurred.
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**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSAES\_PKCS2048\_Encrypt()

```
fsp_err_t R_SCE_RSAES_PKCS2048_Encrypt ( sce_rsa_byte_data_t* plain, sce_rsa_byte_data_t*
cipher, sce_rsa2048_public_wrapped_key_t* wrapped_key )
```

The `R_SCE_RSAES_PKCS2048_Encrypt()` function RSA-encrypts the plaintext input to the first argument, `plain`, according to RSAES-PKCS1-V1\_5. It writes the encryption result to the second argument, `cipher`.

#### Parameters

[in]	plain	plaintext <ul style="list-style-type: none"> <li>plain-&gt;pdata : Specifies pointer to array containing plaintext.</li> <li>plain-&gt;data_length : Specifies valid data length of plaintext array. data size &lt;= public key n size - 11</li> </ul>
[in,out]	cipher	ciphertext <ul style="list-style-type: none"> <li>cipher-&gt;pdata : Specifies pointer to array containing ciphertext.</li> <li>cipher-&gt;data_length : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in]	wrapped_key	Inputs the 2048-bit RSA public wrapped key.

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_RSAES\_PKCS2048\_Decrypt()

```
fsp_err_t R_SCE_RSAES_PKCS2048_Decrypt ( sce_rsa_byte_data_t* cipher, sce_rsa_byte_data_t*
plain, sce_rsa2048_private_wrapped_key_t* wrapped_key )
```

The R\_SCE\_RSAES\_PKCS2048\_Decrypt() function RSA-decrypts the ciphertext input to the first argument, cipher, according to RSAES-PKCS1-V1\_5. It writes the decryption result to the second argument, plain.

**Parameters**

[in]	cipher	ciphertext <ul style="list-style-type: none"> <li>• cipher-&gt;pdata : Specifies pointer to array containing ciphertext.</li> <li>• cipher-&gt;data_length : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in,out]	plain	plaintext <ul style="list-style-type: none"> <li>• plain-&gt;pdata : Specifies pointer to array containing plaintext.</li> <li>• plain-&gt;data_length : Inputs plaintext buffer size. The following size is required. Plaintext buffer size &gt;= public key n size -11. Outputs valid data length after decryption (public key n size).</li> </ul>
[in]	wrapped_key	Inputs the 1024-bit RSA private wrapped key.

**Return values**

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.

FSP_ERR_CRYPTO_SCE_FAIL	An internal error occurred.
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**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSAES\_PKCS3072\_Encrypt()

```
fsp_err_t R_SCE_RSAES_PKCS3072_Encrypt ( sce_rsa_byte_data_t* plain, sce_rsa_byte_data_t*
cipher, sce_rsa3072_public_wrapped_key_t* wrapped_key )
```

The `R_SCE_RSAES_PKCS3072_Encrypt()` function RSA-encrypts the plaintext input to the first argument, `plain`, according to RSAES-PKCS1-V1\_5. It writes the encryption result to the second argument, `cipher`.

#### Parameters

[in]	<code>plain</code>	plaintext <ul style="list-style-type: none"> <li><code>plain-&gt;pdata</code> : Specifies pointer to array containing plaintext.</li> <li><code>plain-&gt;data_length</code> : Specifies valid data length of plaintext array. data size <math>\leq</math> public key n size - 11</li> </ul>
[in,out]	<code>cipher</code>	ciphertext <ul style="list-style-type: none"> <li><code>cipher-&gt;pdata</code> : Specifies pointer to array containing ciphertext.</li> <li><code>cipher-&gt;data_length</code> : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in]	<code>wrapped_key</code>	Inputs the 3072-bit RSA public wrapped key.

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_RSAES\_PKCS4096\_Encrypt()

```
fsp_err_t R_SCE_RSAES_PKCS4096_Encrypt ( sce_rsa_byte_data_t* plain, sce_rsa_byte_data_t*
cipher, sce_rsa4096_public_wrapped_key_t* wrapped_key )
```

The R\_SCE\_RSAES\_PKCS4096\_Encrypt() function RSA-encrypts the plaintext input to the first argument, plain, according to RSAES-PKCS1-V1\_5. It writes the encryption result to the second argument, cipher.

#### Parameters

[in]	plain	plaintext <ul style="list-style-type: none"> <li>plain-&gt;pdata : Specifies pointer to array containing plaintext.</li> <li>plain-&gt;data_length : Specifies valid data length of plaintext array. data size &lt;= public key n size - 11</li> </ul>
[in,out]	cipher	ciphertext <ul style="list-style-type: none"> <li>cipher-&gt;pdata : Specifies pointer to array containing ciphertext.</li> <li>cipher-&gt;data_length : Inputs ciphertext buffer size. Outputs valid data length after encryption (public key n size).</li> </ul>
[in]	wrapped_key	Inputs the 4096-bit RSA public wrapped key.

#### Return values

FSP_SUCCESS	Normal termination
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource needed by the processing routine was in use by another processing routine.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Incorrect wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is illegal.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_ECDSA\_secp192r1\_SignatureGenerate()

```
fsp_err_t R_SCE_ECDSA_secp192r1_SignatureGenerate ( sce_ecdsa_byte_data_t* message_hash,
sce_ecdsa_byte_data_t* signature, sce_ecc_private_wrapped_key_t* wrapped_key )
```

When a message is specified in the first argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the first argument, message\_hash->pdata, is calculated, and the signature text is written to the second argument, signature, in accordance with secp192r1 using the private wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the first argument, message\_hash->data\_type, the signature text for the first 24 bytes of the SHA-256 hash value input to the first argument, message\_hash->pdata, is written to the second argument, signature, in accordance with secp192r1 using the private wrapped key input as the third argument, wrapped\_key.

#### Parameters

[in]	message_hash	<p>Message or hash value to which to attach signature</p> <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in,out]	signature	<p>Signature text storage destination information</p> <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "0 padding (64 bits)    signature r (192 bits)    0 padding (64 bits)    signature s (192 bits)".</li> <li>signature-&gt;data_length : Data length (byte units)</li> </ul>

[in]	wrapped_key	Input wrapped key of secp192r1 private key.
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**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_ECDSA\_secp224r1\_SignatureGenerate()**

```
fsp_err_t R_SCE_ECDSA_secp224r1_SignatureGenerate ( sce_ecdsa_byte_data_t* message_hash,
sce_ecdsa_byte_data_t* signature, sce_ecc_private_wrapped_key_t* wrapped_key )
```

When a message is specified in the first argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the first argument, message\_hash->pdata, is calculated, and the signature text is written to the second argument, signature, in accordance with secp224r1 using the private wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the first argument, message\_hash->data\_type, the signature text for the first 28 bytes of the SHA-256 hash value input to the first argument, message\_hash->pdata, is written to the second argument, signature, in accordance with secp224r1 using the private wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	message_hash	Message or hash value to which to attach signature <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash</li> </ul>
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		(Message: 0 Hash value: 1)
[in,out]	signature	Signature text storage destination information <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "0 padding (32 bits)    signature r (224 bits)    0 padding (32 bits)    signature s (224 bits)".</li> <li>signature-&gt;data_length : Data length (byte units)</li> </ul>
[in]	wrapped_key	Input wrapped key of secp224r1 private key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTTO_SCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTTO_SCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTTO_SCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECDSA\_secp256r1\_SignatureGenerate()

```
fsp_err_t R_SCE_ECDSA_secp256r1_SignatureGenerate ( sce_ecdsa_byte_data_t * message_hash,
sce_ecdsa_byte_data_t * signature, sce_ecc_private_wrapped_key_t * wrapped_key )
```

When a message is specified in the first argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the first argument, message\_hash->pdata, is calculated, and the signature text is written to the second argument, signature, in accordance with secp256r1 using the private wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the first argument, message\_hash->data\_type, the signature text for the first 32 bytes of the SHA-256 hash value input to the first argument, message\_hash->pdata, is written to the second argument, signature, in accordance with secp256r1 using the private wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	message_hash	<p>Message or hash value to which to attach signature</p> <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in,out]	signature	<p>Signature text storage destination information</p> <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "signature r (256 bits)    signature s (256 bits)".</li> <li>signature-&gt;data_length : Data length (byte units)</li> </ul>
[in]	wrapped_key	Input wrapped key of secp256r1 private key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_ECDSA\_secp384r1\_SignatureGenerate()**

```
fsp_err_t R_SCE_ECDSA_secp384r1_SignatureGenerate ( sce_ecdsa_byte_data_t* message_hash,
sce_ecdsa_byte_data_t* signature, sce_ecc_private_wrapped_key_t* wrapped_key )
```

When a message is specified in the first argument, message\_hash->data\_type, a SHA-384 hash of the message text input as the first argument, message\_hash->pdata, is calculated, and the signature text is written to the second argument, signature, in accordance with secp384r1 using the private wrapped key input as the third argument, wrapped\_key.

To use message input, prepare a user-defined function for SHA384.

When a hash value is specified in the first argument, message\_hash->data\_type, the signature text for the first 48 bytes of the SHA-384 hash value input to the first argument, message\_hash->pdata, is written to the second argument, signature, in accordance with secp384r1 using the private wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	message_hash	<p>Message or hash value to which to attach signature</p> <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash</li> </ul>
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		value: 1)
[in,out]	signature	Signature text storage destination information <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "signature r (384 bits)    signature s (384 bits)".</li> <li>signature-&gt;data_length : Data length (byte units)</li> </ul>
[in]	wrapped_key	Input wrapped key of secp384r1 private key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_ECDSA\_secp192r1\_SignatureVerify()

```
fsp_err_t R_SCE_ECDSA_secp192r1_SignatureVerify ( sce_ecdsa_byte_data_t* signature,
sce_ecdsa_byte_data_t* message_hash, sce_ecc_public_wrapped_key_t* wrapped_key )
```

When a message is specified in the second argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the second argument, message\_hash->pdata, is calculated, and the signature text input to the first argument, signature, is validated in accordance with secp192r1 using the public wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the second argument, message\_hash->data\_type, the signature text for the first 24 bytes of the SHA-256 hash value input to the second argument, message\_hash->pdata, input to the first argument, signature, is validated in accordance with secp192r1 using the public wrapped key input as the third argument, wrapped\_key.

#### Parameters

[in]	signature	Signature text information to be verified <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "0 padding (64 bits)    signature r (192 bits)    0 padding (64 bits)    signature s (192 bits)".</li> <li>signature-&gt;data_length : Specifies the data length (byte units) (nonuse)</li> </ul>
[in,out]	message_hash	Message or hash value to be verified <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>

[in]	wrapped_key	Input wrapped key of secp192r1 public key.
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**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTO_SCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTO_SCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTO_SCE_FAIL	An internal error occurred or signature verification failed.
FSP_ERR_CRYPTO_SCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTO_SCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_ECDSA\_secp224r1\_SignatureVerify()**

```
fsp_err_t R_SCE_ECDSA_secp224r1_SignatureVerify ( sce_ecdsa_byte_data_t * signature,
sce_ecdsa_byte_data_t * message_hash, sce_ecc_public_wrapped_key_t * wrapped_key )
```

When a message is specified in the second argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the second argument, message\_hash->pdata, is calculated, and the signature text input to the first argument, signature, is validated in accordance with secp224r1 using the public wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the second argument, message\_hash->data\_type, the signature text for the first 28 bytes of the SHA-256 hash value input to the second argument, message\_hash->pdata, input to the first argument, signature, is validated in accordance with secp224r1 using the public wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	signature	Signature text information to be verified <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "0 padding (32 bits)    signature r (224 bits)    0 padding (32 bits)    signature s (224 bits)".</li> <li>signature-&gt;data_length : Specifies the data length (byte units) (nonuse)</li> </ul>
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[in,out]	message_hash	<p>Message or hash value to be verified</p> <ul style="list-style-type: none"> <li>• message_hash-&gt;data : Specifies pointer to array storing the message or hash value</li> <li>• message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>• message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Input wrapped key of secp224r1 public key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred or signature verification failed.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

## ◆ R\_SCE\_ECDSA\_secp256r1\_SignatureVerify()

```
fsp_err_t R_SCE_ECDSA_secp256r1_SignatureVerify ( sce_ecdsa_byte_data_t* signature,
sce_ecdsa_byte_data_t* message_hash, sce_ecc_public_wrapped_key_t* wrapped_key )
```

When a message is specified in the second argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the second argument, message\_hash->pdata, is calculated, and the signature text input to the first argument, signature, is validated in accordance with secp256r1 using the public wrapped key input as the third argument, wrapped\_key.

When a hash value is specified in the second argument, message\_hash->data\_type, the signature text for the first 32 bytes of the SHA-256 hash value input to the second argument, message\_hash->pdata, input to the first argument, signature, is validated in accordance with secp256r1 using the public wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	signature	Signature text information to be verified <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "signature r (256 bits)    signature s (256 bits)".</li> <li>signature-&gt;data_length : Specifies the data length (byte units) (nonuse)</li> </ul>
[in,out]	message_hash	Message or hash value to be verified <ul style="list-style-type: none"> <li>message_hash-&gt;pdata : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Input wrapped key of

secp256r1 public key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred or signature verification failed.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**◆ R\_SCE\_ECDSA\_secp384r1\_SignatureVerify()**

```
fsp_err_t R_SCE_ECDSA_secp384r1_SignatureVerify ( sce_ecdsa_byte_data_t * signature,
sce_ecdsa_byte_data_t * message_hash, sce_ecc_public_wrapped_key_t * wrapped_key )
```

When a message is specified in the second argument, message\_hash->data\_type, a SHA-256 hash of the message text input as the second argument, message\_hash->pdata, is calculated, and the signature text input to the first argument, signature, is validated in accordance with secp384r1 using the public wrapped key input as the third argument, wrapped\_key.

To use message input, prepare a user-defined function for SHA384.

When a hash value is specified in the second argument, message\_hash->data\_type, the signature text for the first 48 bytes of the SHA-256 hash value input to the second argument, message\_hash->pdata, input to the first argument, signature, is validated in accordance with secp384r1 using the public wrapped key input as the third argument, wrapped\_key.

**Parameters**

[in]	signature	Signature text information to be verified <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text The signature format is "signature r (384 bits)    signature s (384 bits)".</li> <li>signature-&gt;data_length : Specifies the data length (byte units) (nonuse)</li> </ul>
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[in,out]	message_hash	<p>Message or hash value to be verified</p> <ul style="list-style-type: none"> <li>message_hash-&gt;data : Specifies pointer to array storing the message or hash value</li> <li>message_hash-&gt;data_length : Specifies effective data length of the array (Specify only when Message is selected)</li> <li>message_hash-&gt;data_type : Selects the data type of message_hash (Message: 0 Hash value: 1)</li> </ul>
[in]	wrapped_key	Input wrapped key of secp384r1 public key.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred or signature verification failed.
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_ECDH\_secp256r1\_Init()

```
fsp_err_t R_SCE_ECDH_secp256r1_Init ( sce_ecdh_handle_t * handle, uint32_t key_type, uint32_t use_key_id )
```

The R\_SCE\_ECDH\_secp256r1\_Init() function prepares to perform ECDH key exchange computation and writes the result to the first argument, handle. The succeeding functions R\_SCE\_ECDH\_secp256r1\_PublicKeySign(), R\_SCE\_ECDH\_secp256r1\_PublicKeyVerify(), R\_SCE\_ECDH\_secp256r1\_SharedSecretCalculate(), and R\_SCE\_ECDH\_secp256r1\_KeyDerivation() use handle as an argument.

Use the second argument, key\_type, to select the type of ECDH key exchange. When ECDHE is selected, the R\_SCE\_ECDH\_secp256r1\_PublicKeySign() function uses the SCE's random number generation functionality to generate an secp256r1 key pair. When ECDH is selected, keys installed beforehand are used for key exchange.

Input 1 as the third argument, use\_key\_id, to use key\_id when key exchange is performed. key\_id is for applications conforming to the DLMS/COSEM standard for smart meters.

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	key_type	Key exchange type (0: ECDHE, 1: ECDH)
[in]	use_key_id	0: key_id not used, 1: key_id used

#### Return values

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_PARAMETER	Input data is invalid.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_ECDH\_secp256r1\_PublicKeySign()

```
fsp_err_t R_SCE_ECDH_secp256r1_PublicKeySign ( sce_ecdh_handle_t * handle,
sce_ecc_public_wrapped_key_t * ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t *
ecc_private_wrapped_key, uint8_t * public_key, sce_ecdsa_byte_data_t * signature,
sce_ecc_private_wrapped_key_t * wrapped_key )
```

The `R_SCE_ECDH_secp256r1_PublicKeySign()` function calculates a signature for a public key user wrapped key used for ECDH key exchange.

If ECDHE is specified by the `key_type` argument of the `R_SCE_ECDH_secp256r1_Init()` function, the SCE's random number generation functionality is used to generate an secp256r1 key pair. The public key is output to `public_key` and the private key is output to `wrapped_key`.

If ECDH is specified by the `key_type` argument of the `R_SCE_ECDH_secp256r1_Init()` function, the public key input as `ecc_public_wrapped_key` is output to `public_key` and nothing is output to `wrapped_key`.

The succeeding function `R_SCE_ECDH_secp256r1_SharedSecretCalculate()` uses the first argument, `handle`, as an argument. `R_SCE_ECDH_secp256r1_SharedSecretCalculate()` function uses `wrapped_key` as input to calculate Z.

#### Parameters

[in,out]	handle	ECDH handler (work area) When using <code>key_id</code> , input <code>handle-&gt;key_id</code> after running <code>R_SCE_ECDH_secp256r1_Init()</code> .
[in]	ecc_public_wrapped_key	For ECDHE, input a null pointer. For ECDH, input the wrapped key of a secp256r1 public key.
[in]	ecc_private_wrapped_key	secp256r1 private key for signature generation
[in,out]	public_key	User secp256r1 public key (512-bit) for key exchange. When using <code>key_id</code> , <code>key_id</code> (8-bit)    public key (512-bit)    0 padding (24-bit)
[in,out]	signature	Signature text storage destination information <ul style="list-style-type: none"> <li>signature-&gt;pdata : Specifies pointer to array storing signature text. The signature format is "signature r (256 bits)    signature s (256 bits)"</li> <li>signature-&gt;data_leng</li> </ul>

		th : Data length (in byte units)
[in,out]	wrapped_key	For ECDHE, a private wrapped key generated from a random number. Not output for ECDH.

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

*The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.*

### ◆ R\_SCE\_ECDH\_secp256r1\_PublicKeyVerify()

```
fsp_err_t R_SCE_ECDH_secp256r1_PublicKeyVerify ( sce_ecdh_handle_t* handle,
sce_ecc_public_wrapped_key_t* ecc_public_wrapped_key, uint8_t* public_key_data,
sce_ecdsa_byte_data_t* signature, sce_ecc_public_wrapped_key_t* wrapped_key )
```

The R\_SCE\_ECDH\_secp256r1\_PublicKeyVerify() function verifies the signature of the secp256r1 public key of the other ECDH key exchange party. If the signature is correct, it outputs the public wrapped key to the fifth argument. The first argument, handle, is used as an argument in the subsequent function R\_SCE\_ECDH\_secp256r1\_SharedSecretCalculate().

R\_SCE\_ECDH\_secp256r1\_SharedSecretCalculate() uses wrapped\_key as input to calculate Z.

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	ecc_public_wrapped_key	Public wrapped key area for signature verification
[in]	public_key_data	secp256r1 public key (512-bit). When key_id is used: key_id (8-bit)    public key (512-bit)
[in]	signature	ECDSA secp256r1 signature of ecc_public_wrapped_key
[in,out]	wrapped_key	wrapped key of ecc_public_wrapped_key

#### Return values

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred or signature verification failed.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_ECDH\_secp256r1\_SharedSecretCalculate()

```
fsp_err_t R_SCE_ECDH_secp256r1_SharedSecretCalculate ( sce_ecdh_handle_t* handle,
sce_ecc_public_wrapped_key_t* ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t*
ecc_private_wrapped_key, sce_ecdh_wrapped_key_t* shared_secret_wrapped_key )
```

The `R_SCE_ECDH_secp256r1_SharedSecretCalculate()` function uses the ECDH key exchange algorithm to output the wrapped key of the shared secret Z derived from the public key of the other key exchange party and your own private key. Input as the second argument, `ecc_public_wrapped_key`, the public wrapped key whose signature was verified by `R_SCE_ECDH_secp256r1_PublicKeyVerify()`. When `key_type` of `R_SCE_ECDH_secp256r1_Init()` is 0, input as the third argument, `ecc_private_wrapped_key`, the private wrapped key generated from a random number by `R_SCE_ECDH_secp256r1_PublicKeySign()`, and when `key_type` is other than 0, input the private wrapped key that forms a pair with the second argument of `R_SCE_ECDH_secp256r1_PublicKeySign()`. The subsequent `R_SCE_ECDH_secp256r1_KeyDerivation()` function uses `shared_secret_wrapped_key` as key material for outputting the wrapped key.

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	ecc_public_wrapped_key	Public wrapped key whose signature was verified by <code>R_SCE_ECDH_secp256r1_PublicKeyVerify()</code>
[in]	ecc_private_wrapped_key	Private wrapped key
[in,out]	shared_secret_wrapped_key	Wrapped key of shared secret Z calculated by ECDH key exchange

#### Return values

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_FAIL	An internal error occurred.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

#### Note

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

### ◆ R\_SCE\_ECDH\_secp256r1\_KeyDerivation()

```
fsp_err_t R_SCE_ECDH_secp256r1_KeyDerivation ( sce_ecdh_handle_t * handle,
sce_ecdh_wrapped_key_t * shared_secret_wrapped_key, uint32_t key_type, uint32_t kdf_type,
uint8_t * other_info, uint32_t other_info_length, sce_hmac_sha_wrapped_key_t *
salt_wrapped_key, sce_aes_wrapped_key_t * wrapped_key )
```

The `R_SCE_ECDH_secp256r1_KeyDerivation()` function uses the shared secret "Z (shared\_secret\_index)" calculated by the `R_SCE_ECDH_secp256r1_SharedSecretCalculate()` function as the key material to derive the wrapped key specified by the third argument, `key_type`. The key derivation algorithm is one-step key derivation as defined in NIST SP800-56C. Either SHA-256 or SHA-256 HMAC is specified by the fourth argument, `kdf_type`. When SHA-256 HMAC is specified, the wrapped key output by the `R_SCE_SHA256HMAC_EncryptedKeyWrap()` function is specified as the seventh argument, `salt_wrapped_key`. Enter a fixed value for deriving a key shared with the key exchange partner in the fifth argument, `other_info`. A wrapped key corresponding to `key_type` is output as the eighth argument, `wrapped_key`. The correspondences between the types of derived `wrapped_key` and the functions with which they can be used as listed below.

- AES-128: All AES-128 Init functions
- AES-256: All AES-256 Init functions
- SHA256-HMAC: `R_SCE_SHA256HMAC_GenerateInit()` function and `R_SCE_SHA256HMAC_VerifyInit()` function

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	shared_secret_wrapped_key	Z wrapped key calculated by <code>R_SCE_ECDH_secp256r1_SharedSecretCalculate</code>
[in]	key_type	Derived key type (0: AES-128, 1: AES-256, 2:SHA256-HMAC)
[in]	kdf_type	Algorithm used for key derivation calculation (0: SHA-256, 1:SHA256-HMAC)
[in]	other_info	Additional data used for key derivation calculation: AlgorithmID    PartyUInfo    PartyVInfo
[in]	other_info_length	Data length of <code>other_info</code> (up to 147 byte units)
[in]	salt_wrapped_key	Salt wrapped key (Input NULL when <code>kdf_type</code> is 0.)
[in,out]	wrapped_key	Wrapped key corresponding to <code>key_type</code> . When the value of <code>key_type</code> is 2, an SHA256-HMAC wrapped key is output. <code>wrapped_key</code> can be specified by casting the start address of the area reserved beforehand by the

		<a href="#">sce_hmac_sha_wrapped_key_t</a> type with the ( <a href="#">sce_aes_wrapped_key_t*</a> ) type.
--	--	---

**Return values**

FSP_SUCCESS	Normal end
FSP_ERR_CRYPTOSCE_RESOURCE_CONFLICT	A resource conflict occurred because a hardware resource required by the processing is in use by other processing.
FSP_ERR_CRYPTOSCE_KEY_SET_FAIL	Invalid wrapped key was input.
FSP_ERR_CRYPTOSCE_PARAMETER	An invalid handle was input.
FSP_ERR_CRYPTOSCE_PROHIBIT_FUNCTION	An invalid function was called.

**Note**

The pre-run state is SCE Enabled State. After the function runs the state transitions to SCE Enabled State.

**4.2.44 Serial Communications Interface (SCI) I2C (r\_sci\_i2c)**

## Modules

**Functions**

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_Open](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [i2c\\_master\\_cfg\\_t](#) const \*const p\_cfg)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_Close](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_Read](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [uint8\\_t](#) \*const p\_dest, [uint32\\_t](#) const bytes, [bool](#) const restart)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_Write](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [uint8\\_t](#) \*const p\_src, [uint32\\_t](#) const bytes, [bool](#) const restart)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_Abort](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_SlaveAddressSet](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [uint32\\_t](#) const slave, [i2c\\_master\\_addr\\_mode\\_t](#) const addr\_mode)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_CallbackSet](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [void\(\\*p\\_callback\)\(i2c\\_master\\_callback\\_args\\_t\\*\)](#), [void](#) const \*const p\_context, [i2c\\_master\\_callback\\_args\\_t](#) \*const p\_callback\_memory)

[fsp\\_err\\_t](#) [R\\_SCI\\_I2C\\_StatusGet](#) ([i2c\\_master\\_ctrl\\_t](#) \*const p\_api\_ctrl, [i2c\\_master\\_status\\_t](#) \*p\_status)

## Detailed Description

Driver for the SCI peripheral on RA MCUs. This module implements the [I2C Master Interface](#).

## Overview

The Simple I2C master on SCI HAL module supports transactions with an I2C Slave device. Callbacks must be provided which would be invoked when a transmission or receive has been completed. The callback arguments will contain information about the transaction status, bytes transferred and a pointer to the user defined context.

## Features

- Supports multiple transmission rates
  - Standard Mode Support with up to 100 kHz transaction rate.
  - Fast Mode Support with up to 400 kHz transaction rate.
- SDA Delay in nanoseconds can be specified as a part of the configuration.
- I2C Master Read from a slave device.
- I2C Master Write to a slave device.
- Abort any in-progress transactions.
- Set the address of the slave device.
- Non-blocking behavior is achieved by the use of callbacks.
- Additional build-time features
  - Optional (build time) DTC support for read and write respectively.
  - Optional (build time) support for 10-bit slave addressing.

## Configuration

### Build Time Configurations for r\_sci\_i2c

The following build time configurations are defined in fsp\_cfg/r\_sci\_i2c\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC on Transmission and Reception	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, DTC instances will be included in the build for both transmission and reception.
10-bit slave addressing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	If enabled, the driver will support 10-bit slave addressing mode along with the default 7-bit slave addressing mode.

### Configurations for Driver > Connectivity > I2C Master Driver on r\_sci\_i2c

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2C Master Driver on r\_sci\_i2c. Non-secure callable guard functions can be generated for this module by right

clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2c0	Module name.
Channel	Value must be an integer between 0 and 9	0	Select the SCI channel.
Slave Address	Value must be a hex value	0x00	Specify the slave address.
Address Mode	<ul style="list-style-type: none"> <li>7-Bit</li> <li>10-Bit</li> </ul>	7-Bit	Select the address mode.
Rate	<ul style="list-style-type: none"> <li>Standard</li> <li>Fast-mode</li> </ul>	Standard	Select the I2C data rate.  If the requested transfer rate cannot be achieved, the settings with the largest possible transfer rate that is less than or equal to the requested transfer rate are used. The theoretical calculated transfer rate and SDA delay are printed in a comment in the generated <a href="#">sci_i2c_extended_cfg_t</a> structure.
SDA Output Delay (nano seconds)	Must be a valid non-negative integer with maximum configurable value of 300	300	Specify the SDA output delay in nanoseconds.
Noise filter setting	<ul style="list-style-type: none"> <li>Use clock signal divided by 1 with noise filter</li> <li>Use clock signal divided by 2 with noise filter</li> <li>Use clock signal divided by 4 with noise filter</li> <li>Use clock signal divided by 8 with noise filter</li> </ul>	Use clock signal divided by 1 with noise filter	Select the sampling clock for the digital noise filter
Bit Rate Modulation	<ul style="list-style-type: none"> <li>Enable</li> <li>Disable</li> </ul>	Enable	Enabling bitrate modulation reduces the percent error of the actual bitrate with

respect to the requested baud rate. It does this by modulating the number of cycles per clock output pulse, so the clock is no longer a square wave.

Callback	Name must be a valid C symbol	sci_i2c_master_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Interrupt Priority Level	MCU Specific Options		Select the interrupt priority level. This is set for TXI, RXI (if used), TEI interrupts.
RX Interrupt Priority Level [Only used when DTC is enabled]	MCU Specific Options		Select the interrupt priority level. This is set for RXI only when DTC is enabled.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA2E1	PCLKB
RA2L1	PCLKB
RA4M1	PCLKA
RA4M2	PCLKA
RA4M3	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA
RA6M5	PCLKA
RA6T1	PCLKA

The actual I2C transfer rate will be calculated and set by the tooling depending on the selected transfer rate and the SDA delay. If the PCLK is configured in such a manner that the selected internal rate cannot be achieved, an error will be returned.

## Pin Configuration

The SCI I2C peripheral module uses pins on the MCU to communicate to external devices. I/O pins must be selected and configured as required by the external device. An I2C channel would consist of two pins - SDA and SCL for data/address and clock respectively.

# Usage Notes

## Interrupt Configuration

- Receive buffer full (RXI), transmit buffer empty (TXI) and transmit end (TEI) interrupts for the selected channel used must be enabled in the properties of the selected device.
- Set equal priority levels for all the interrupts mentioned above. Setting the interrupts to different priority levels could result in improper operation.

## SCI I2C Master Rate Calculation

- The RA Configuration editor calculates the internal baud-rate setting based on the configured transfer rate and SDA Delay. The closest possible baud-rate that can be achieved (less than or equal to the requested rate) at the current PCLK settings is calculated and used.
- If a valid clock rate could not be calculated, an error is returned by the tool.

## Enabling DTC with the SCI I2C

- DTC transfer support is configurable and is disabled from the build by default. SCI I2C driver provides two DTC instances for transmission and reception respectively.
- For further details on DTC please refer [Data Transfer Controller \(r\\_dtc\)](#)

## Multiple Devices on the Bus

- A single SCI I2C instance can be used to communicate with multiple slave devices on the same channel by using the SlaveAddressSet API.

## Restart

- SCI I2C master can hold the the bus after an I2C transaction by issuing Restart. This will mimic a stop followed by start condition.

# Examples

## Basic Example

This is a basic example of minimal use of the r\_sci\_i2c in an application. This example shows how this driver can be used for basic read and write operations.

```
void basic_example (void)
{
```

```
fsp_err_t err;

uint32_t i;

uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

/* Initialize the IIC module */

err = R_SCI_I2C_Open(&g_i2c_device_ctrl_1, &g_i2c_device_cfg_1);

/* Handle any errors. This function should be defined by the user. */

assert(FSP_SUCCESS == err);

/* Write some data to the transmit buffer */

for (i = 0; i < I2C_BUFFER_SIZE_BYTES; i++)

{

    g_i2c_tx_buffer[i] = (uint8_t) i;

}

/* Send data to I2C slave */

g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;

err = R_SCI_I2C_Write(&g_i2c_device_ctrl_1, &g_i2c_tx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);

assert(FSP_SUCCESS == err);

/* Since there is nothing else to do, block until Callback triggers*/

while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)

{

R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

    timeout_ms--;

}

if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)

{

    __BKPT(0);

}

/* Read data back from the I2C slave */

g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;

timeout_ms = I2C_TRANSACTION_BUSY_DELAY;

err = R_SCI_I2C_Read(&g_i2c_device_ctrl_1, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);

assert(FSP_SUCCESS == err);

/* Since there is nothing else to do, block until Callback triggers*/
```

```
while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
/* Verify the read data */
if (0U != memcmp(g_i2c_tx_buffer, g_i2c_rx_buffer, I2C_BUFFER_SIZE_BYTES))
{
    __BKPT(0);
}
}
```

### Multiple Slave devices on the same channel (bus)

This example demonstrates how a single SCI I2C driver can be used to communicate with different slave devices which are on the same channel.

```
void single_channel_multi_slave (void)
{
    fsp_err_t err;
    uint32_t timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
    err = R_SCI_I2C_Open(&g_i2c_device_ctrl_2, &g_i2c_device_cfg_2);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Clear the receive buffer */
    memset(g_i2c_rx_buffer, '0', I2C_BUFFER_SIZE_BYTES);
    /* Read data from I2C slave */
    g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
    err = R_SCI_I2C_Read(&g_i2c_device_ctrl_2, &g_i2c_rx_buffer[0],
I2C_BUFFER_SIZE_BYTES, false);
    assert(FSP_SUCCESS == err);
}
```

```
while ((I2C_MASTER_EVENT_RX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
/* Send data to I2C slave on the same channel */
err = R_SCI_I2C_SlaveAddressSet(&g_i2c_device_ctrl_2, I2C_SLAVE_DISPLAY_ADAPTER,
I2C_MASTER_ADDR_MODE_7BIT);
assert(FSP_SUCCESS == err);
g_i2c_tx_buffer[0] = (uint8_t) I2C_EXAMPLE_DATA_1;
g_i2c_tx_buffer[1] = (uint8_t) I2C_EXAMPLE_DATA_2;
g_i2c_callback_event = I2C_MASTER_EVENT_ABORTED;
timeout_ms = I2C_TRANSACTION_BUSY_DELAY;
err = R_SCI_I2C_Write(&g_i2c_device_ctrl_2, &g_i2c_tx_buffer[0], 2U, false);
assert(FSP_SUCCESS == err);
while ((I2C_MASTER_EVENT_TX_COMPLETE != g_i2c_callback_event) && timeout_ms)
{
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    timeout_ms--;
}
if (I2C_MASTER_EVENT_ABORTED == g_i2c_callback_event)
{
    __BKPT(0);
}
}
```

## Data Structures

struct [sci\\_i2c\\_clock\\_settings\\_t](#)

struct [sci\\_i2c\\_instance\\_ctrl\\_t](#)

struct [sci\\_i2c\\_extended\\_cfg\\_t](#)

## Data Structure Documentation

### ◆ sci\_i2c\_clock\_settings\_t

struct sci_i2c_clock_settings_t		
I2C clock settings		
Data Fields		
bool	bitrate_modulation	Bit-rate Modulation Function enable or disable.
uint8_t	brr_value	Bit rate register settings.
uint8_t	clk_divisor_value	Clock Select settings.
uint8_t	mddr_value	Modulation Duty Register settings.
uint8_t	cycles_value	SDA Delay Output Cycles Select.
uint8_t	snfr_value	Noise Filter Setting Register value.

### ◆ sci\_i2c\_instance\_ctrl\_t

struct sci_i2c_instance_ctrl_t		
I2C control structure. DO NOT INITIALIZE.		

### ◆ sci\_i2c\_extended\_cfg\_t

struct sci_i2c_extended_cfg_t		
SCI I2C extended configuration		
Data Fields		
<a href="#">sci_i2c_clock_settings_t</a>	clock_settings	I2C Clock settings.

## Function Documentation

◆ **R\_SCI\_I2C\_Open()**

```
fsp_err_t R_SCI_I2C_Open ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_cfg_t const *const p_cfg )
```

Opens the I2C device.

**Return values**

FSP_SUCCESS	Requested clock rate was set exactly.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_ASSERTION	Parameter check failure due to one or more reasons below: <ul style="list-style-type: none"> <li>1. p_api_ctrl or p_cfg is NULL.</li> <li>2. extended parameter is NULL.</li> <li>3. Callback parameter is NULL.</li> <li>4. Clock rate requested is greater than 400KHz</li> <li>5. Invalid IRQ number assigned</li> </ul>

◆ **R\_SCI\_I2C\_Close()**

```
fsp_err_t R_SCI_I2C_Close ( i2c_master_ctrl_t *const p_api_ctrl)
```

Closes the I2C device. Power down I2C peripheral.

This function will safely terminate any in-progress I2C transfer with the device. If a transfer is aborted, the user will be notified via callback with an abort event. Since the callback is optional, this function will also return a specific error code in this situation.

**Return values**

FSP_SUCCESS	Device closed without issue.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Read()**

```
fsp_err_t R_SCI_I2C_Read ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t
const bytes, bool const restart )
```

Performs a read from the I2C device. The caller will be notified when the operation has completed (successfully) by an I2C\_MASTER\_EVENT\_RX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	The parameter p_ctrl, p_dest is NULL, bytes is 0.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Write()**

```
fsp_err_t R_SCI_I2C_Write ( i2c_master_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes, bool const restart )
```

Performs a write to the I2C device.

This function will fail if there is already an in-progress I2C transfer on the associated channel. Otherwise, the I2C write operation will begin. When no callback is provided by the user, this function performs a blocking write. Otherwise, the write operation is non-blocking and the caller will be notified when the operation has finished by an I2C\_EVENT\_TX\_COMPLETE in the callback.

**Return values**

FSP_SUCCESS	Function executed without issue.
FSP_ERR_ASSERTION	p_ctrl, p_src is NULL.
FSP_ERR_INVALID_SIZE	Provided number of bytes more than uint16_t size (65535) while DTC is used for data transfer.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_Abort()**

```
fsp_err_t R_SCI_I2C_Abort ( i2c_master_ctrl_t *const p_api_ctrl)
```

Aborts any in-progress transfer and forces the I2C peripheral into a ready state.

This function will safely terminate any in-progress I2C transfer with the device. If a transfer is aborted, the user will be notified via callback with an abort event. Since the callback is optional, this function will also return a specific error code in this situation.

**Return values**

FSP_SUCCESS	Transaction was aborted without issue.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.

◆ **R\_SCI\_I2C\_SlaveAddressSet()**

```
fsp_err_t R_SCI_I2C_SlaveAddressSet ( i2c_master_ctrl_t *const p_api_ctrl, uint32_t const slave,
i2c_master_addr_mode_t const addr_mode )
```

Sets address and addressing mode of the slave device.

This function is used to set the device address and addressing mode of the slave without reconfiguring the entire bus.

**Return values**

FSP_SUCCESS	Address of the slave is set correctly.
FSP_ERR_ASSERTION	p_ctrl or address is NULL.
FSP_ERR_NOT_OPEN	Device was not even opened.
FSP_ERR_IN_USE	An I2C Transaction is in progress.

◆ **R\_SCI\_I2C\_CallbackSet()**

```
fsp_err_t R_SCI_I2C_CallbackSet ( i2c_master_ctrl_t *const p_api_ctrl,
void(*) (i2c_master_callback_args_t *) p_callback, void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2c_master_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_SCI\_I2C\_StatusGet()**

```
fsp_err_t R_SCI_I2C_StatusGet ( i2c_master_ctrl_t *const p_api_ctrl, i2c_master_status_t * p_status )
```

Provides driver status.

**Return values**

FSP_SUCCESS	Status stored in <code>p_status</code> .
FSP_ERR_ASSERTION	NULL pointer.

**4.2.45 Serial Communications Interface (SCI) SPI (r\_sci\_spi)**

## Modules

**Functions**

```
fsp_err_t R_SCI_SPI_Open (spi_ctrl_t *p_api_ctrl, spi_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SCI_SPI_Read (spi_ctrl_t *const p_api_ctrl, void *p_dest, uint32_t
const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_Write (spi_ctrl_t *const p_api_ctrl, void const *p_src,
uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_WriteRead (spi_ctrl_t *const p_api_ctrl, void const *p_src,
```

```
void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SCI_SPI_CallbackSet (spi_ctrl_t *const p_api_ctrl,
void(*p_callback)(spi_callback_args_t *), void const *const p_context,
spi_callback_args_t *const p_callback_memory)
```

```
fsp_err_t R_SCI_SPI_Close (spi_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_SCI_SPI_CalculateBitrate (uint32_t bitrate, sci_spi_div_setting_t
*sclk_div, bool use_mddr)
```

## Detailed Description

Driver for the SCI peripheral on RA MCUs. This module implements the [SPI Interface](#).

## Overview

### Features

- Standard SPI Modes
  - Master or Slave Mode
  - Clock Polarity (CPOL)
    - CPOL=0 SCLK is low when idle
    - CPOL=1 SCLK is high when idle
  - Clock Phase (CPHA)
    - CPHA=0 Select data sampling on leading edge, data change on trailing edge
    - CPHA=1 Select data change on leading edge, data sampling on trailing edge
  - MSB/LSB first
- Configurable bit rate
- DTC Support
- Callback Events
  - Transfer Complete
  - RX Overflow Error (The SCI shift register is copied to the data register before previous data was read)

## Configuration

### Build Time Configurations for r\_sci\_spi

The following build time configurations are defined in fsp\_cfg/r\_sci\_spi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC Support	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>	Enabled	If support for

- Disabled

transferring data using the DTC will be compiled in.

### Configurations for Driver > Connectivity > SPI Driver on r\_sci\_spi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > SPI Driver on r\_sci\_spi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_spi0	Module name.
Channel	Value must be a non-negative integer	0	Select the SCI channel.
Operating Mode	<ul style="list-style-type: none"> <li>• Master</li> <li>• Slave</li> </ul>	Master	Select the SPI operating mode.
Clock Phase	<ul style="list-style-type: none"> <li>• Data sampling on odd edge, data variation on even edge</li> <li>• Data sampling on even edge, data variation on odd edge</li> </ul>	Data sampling on odd edge, data variation on even edge	Select the clock edge to sample data.
Clock Polarity	<ul style="list-style-type: none"> <li>• Low when idle</li> <li>• High when idle</li> </ul>	Low when idle	Select clock level when idle.
Mode Fault Error	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Detect master/slave mode conflicts.
Bit Order	<ul style="list-style-type: none"> <li>• MSB First</li> <li>• LSB First</li> </ul>	MSB First	Select the data bit order.
Callback	Name must be a valid C symbol	sci_spi_callback	A user callback function that is called from the sci spi interrupts when a transfer is completed or an error has occurred.
Receive Interrupt Priority	MCU Specific Options		Select the receive interrupt priority.
Transmit Interrupt Priority	MCU Specific Options		Select the transmit interrupt priority.
Transmit End Interrupt Priority	MCU Specific Options		Select the transmit end interrupt priority.
Error Interrupt Priority	MCU Specific Options		Select the error interrupt priority.

Bitrate	Value must be an integer greater than 0	8000000	Enter the desired bitrate.  If the requested bitrate cannot be achieved, the settings with the largest possible value that is less than or equal to the requested bitrate is used. The theoretical bitrate is printed in a comment in the generated <a href="#">sci_spi_extended_cfg_t</a> structure.
Bitrate Modulation	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enabling bitrate modulation reduces the percent error of the actual bitrate with respect to the requested baud rate. It does this by modulating the number of cycles per clock output pulse, so the clock is no longer a square wave.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA2E1	PCLKB
RA2L1	PCLKB
RA4M1	PCLKA
RA4M2	PCLKA
RA4M3	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA
RA6M5	PCLKA

RA6T1

PCLKA

## Pin Configuration

This module uses SCIn\_MOSI, SCIn\_MISO, SCIn\_SPCK, and SCIn\_SS pins to communicate with on board devices.

### Note

*At high bit rates, it might be necessary to configure the pins with `IOPORT_CFG_DRIVE_HIGH`.*

## Usage Notes

### Transfer Complete Event

The transfer complete event is triggered when all of the data has been transferred. In slave mode if the SS pin is de-asserted then no transfer complete event is generated until the SS pin is asserted and the remaining data is transferred.

### Performance

At high bit rates, interrupts may not be able to service transfers fast enough. In master mode this means there will be a delay between each data frame. In slave mode this could result in RX Overflow errors.

In order to improve performance at high bit rates, it is recommended that the instance be configured to service transfers using the DTC.

### Transmit From RXI Interrupt

After every byte, the SCI SPI peripheral generates a transmit buffer empty interrupt and a receive buffer full interrupt. Whenever possible, the SCI\_SPI module handles both interrupts in the receive buffer full interrupt. This improves performance when the DTC is not being used.

### Slave Select Pin

- In master mode the slave select pin must be driven in software.
- In slave mode the hardware handles the slave select pin and will only transfer data when the SS pin is low.

### Bit Rate Modulation

Depending on the peripheral clock frequency, the desired bit rate may not be achievable. With bit rate modulation, the device can remove a configurable number of input clock pulses to the internal bit rate counter in order to create the desired bit rate. This has the effect of changing the period of individual bits in order to achieve the desired average bit rate. For more information see section 34.9 Bit Rate Modulation Function in the RA6M3 manual.

## Examples

### Basic Example

This is a basic example of minimal use of the SCI\_SPI in an application.

```
static volatile bool g_transfer_complete = false;
static void r_sci_spi_callback (spi_callback_args_t * p_args)
{
    if (SPI_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_transfer_complete = true;
    }
}

void sci_spi_basic_example (void)
{
    uint8_t tx_buffer[TRANSFER_SIZE];
    uint8_t rx_buffer[TRANSFER_SIZE];
    /* Configure Slave Select Line 1 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
    /* Configure Slave Select Line 2 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the SPI module. */
    err = R_SCI_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Assert Slave Select Line 1 */
    R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_LOW);
    /* Start a write/read transfer */
    g_transfer_complete = false;
    err = R_SCI_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);
    assert(FSP_SUCCESS == err);
    /* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
    while (false == g_transfer_complete)
    {
        ;
    }
    /* De-assert Slave Select Line 1 */
```

```

R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
/* Wait for minimum time required between transfers. */
R_BSP_SoftwareDelay(SSL_NEXT_ACCESS_DELAY, BSP_DELAY_UNITS_MICROSECONDS);
/* Assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_LOW);
/* Start a write/read transfer */
g_transfer_complete = false;
err = R_SCI_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);
assert(FSP_SUCCESS == err);
/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
while (false == g_transfer_complete)
{
    ;
}
/* De-assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
}

```

## Data Structures

struct [sci\\_spi\\_div\\_setting\\_t](#)

## Data Structure Documentation

### ◆ sci\_spi\_div\_setting\_t

struct sci_spi_div_setting_t		
Settings for adjusting the SPI CLK.		
Data Fields		
uint8_t	brr	
uint8_t	cks: 2	
uint8_t	mddr	Set to 0 to disable MDDR.

## Function Documentation

◆ **R\_SCI\_SPI\_Open()**

```
fsp_err_t R_SCI_SPI_Open ( spi_ctrl_t * p_api_ctrl, spi_cfg_t const *const p_cfg )
```

Initialize a channel for SPI communication mode. Implements `spi_api_t::open`.

This function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enables the clock for the SCI channel.
- Initializes the associated registers with default value and the user-configurable options.
- Provides the channel handle for use with other API functions.

**Parameters**

p_api_ctrl	Pointer to the control structure.
p_cfg	Pointer to a configuration structure.

**Return values**

FSP_SUCCESS	Channel initialized successfully.
FSP_ERR_ASSERTION	An input parameter is invalid or NULL.
FSP_ERR_ALREADY_OPEN	The instance has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel number is invalid.

## ◆ R\_SCI\_SPI\_Read()

```
fsp_err_t R_SCI_SPI_Read ( spi_ctrl_t *const p_api_ctrl, void * p_dest, uint32_t const length,
spi_bit_width_t const bit_width )
```

Receive data from an SPI device. Implements `spi_api_t::read`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable receiver.
- Enable interrupts.
- Start data transmission by writing data to the TXD register.
- Receive data from receive buffer full interrupt occurs and copy data to the buffer of destination.
- Complete data reception via receive buffer full interrupt and transmitting dummy data.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_dest</code>	Pointer to the destination buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to SPI_BIT_WIDTH_8_BITS).

### Return values

FSP_SUCCESS	Read operation successfully completed.
FSP_ERR_ASSERTION	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Bit width is not 8 bits</li> <li>• Length is equal to 0</li> <li>• Pointer to destination is NULL</li> </ul>
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_UNSUPPORTED	The given <code>bit_width</code> is not supported.
FSP_ERR_IN_USE	A transfer is already in progress.

### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reconfigure`

## ◆ R\_SCI\_SPI\_Write()

```
fsp_err_t R_SCI_SPI_Write ( spi_ctrl_t *const p_api_ctrl, void const * p_src, uint32_t const length,
spi_bit_width_t const bit_width )
```

Transmit data to a SPI device. Implements `spi_api_t::write`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable interrupts.
- Start data transmission with data via transmit buffer empty interrupt.
- Copy data from source buffer to the SPI data register for transmission.
- Complete data transmission via transmit buffer empty interrupt.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_src</code>	Pointer to the source buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to <code>SPI_BIT_WIDTH_8_BITS</code> ).

### Return values

<code>FSP_SUCCESS</code>	Write operation successfully completed.
<code>FSP_ERR_ASSERTION</code>	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Pointer to source is NULL</li> <li>• Length is equal to 0</li> <li>• Bit width is not equal to 8 bits</li> </ul>
<code>FSP_ERR_NOT_OPEN</code>	The channel has not been opened. Open the channel first.
<code>FSP_ERR_UNSUPPORTED</code>	The given <code>bit_width</code> is not supported.
<code>FSP_ERR_IN_USE</code>	A transfer is already in progress.

### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reconfigure`

### ◆ R\_SCI\_SPI\_WriteRead()

```
fsp_err_t R_SCI_SPI_WriteRead ( spi_ctrl_t *const p_api_ctrl, void const * p_src, void * p_dest,
uint32_t const length, spi_bit_width_t const bit_width )
```

Simultaneously transmit data to SPI device while receiving data from SPI device (full duplex). Implements `spi_api_t::writeRead`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Enable transmitter.
- Enable receiver.
- Enable interrupts.
- Start data transmission using transmit buffer empty interrupt (or by writing to the TDR register).
- Copy data from source buffer to the SPI data register for transmission.
- Receive data from receive buffer full interrupt and copy data to the destination buffer.
- Complete data transmission and reception via transmit end interrupt.
- Disable transmitter.
- Disable receiver.
- Disable interrupts.

#### Parameters

	<code>p_api_ctrl</code>	Pointer to the control structure.
	<code>p_src</code>	Pointer to the source buffer.
	<code>p_dest</code>	Pointer to the destination buffer.
[in]	<code>length</code>	The number of bytes to transfer.
[in]	<code>bit_width</code>	Invalid for SCI_SPI (Set to <code>SPI_BIT_WIDTH_8_BITS</code> ).

#### Return values

<code>FSP_SUCCESS</code>	Write operation successfully completed.
<code>FSP_ERR_ASSERTION</code>	One of the following invalid parameters passed: <ul style="list-style-type: none"> <li>• Pointer <code>p_api_ctrl</code> is NULL</li> <li>• Pointer to source is NULL</li> <li>• Pointer to destination is NULL</li> <li>• Length is equal to 0</li> <li>• Bit width is not equal to 8 bits</li> </ul>
<code>FSP_ERR_NOT_OPEN</code>	The channel has not been opened. Open the channel first.
<code>FSP_ERR_UNSUPPORTED</code>	The given <code>bit_width</code> is not supported.
<code>FSP_ERR_IN_USE</code>	A transfer is already in progress.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reconfigure](#)

**◆ R\_SCI\_SPI\_CallbackSet()**

```
fsp_err_t R_SCI_SPI_CallbackSet ( spi_ctrl_t *const p_api_ctrl, void(*) (spi_callback_args_t *)
p_callback, void const *const p_context, spi_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements [spi\\_api\\_t::callbackSet](#)

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

**◆ R\_SCI\_SPI\_Close()**

```
fsp_err_t R_SCI_SPI_Close ( spi_ctrl_t *const p_api_ctrl)
```

Disable the SCI channel and set the instance as not open. Implements [spi\\_api\\_t::close](#).

**Parameters**

p_api_ctrl	Pointer to an opened instance.
------------	--------------------------------

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	The parameter p_api_ctrl is NULL.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.

### ◆ R\_SCI\_SPI\_CalculateBitrate()

```
fsp_err_t R_SCI_SPI_CalculateBitrate ( uint32_t bitrate, sci_spi_div_setting_t * sclk_div, bool use_mddr )
```

Calculate the register settings required to achieve the desired bitrate.

#### Parameters

[in]	bitrate	bitrate [bps]. For example, 250,000; 500,00; 2,500,000 (max), etc.
	sclk_div	Pointer to <code>sci_spi_div_setting_t</code> used to configure baudrate settings.
[in]	use_mddr	Calculate the divider settings for use with MDDR.

#### Return values

FSP_SUCCESS	Baud rate is set successfully.
FSP_ERR_ASSERTION	Baud rate is not achievable.

#### Note

The application must pause for 1 bit time after the BRR register is loaded before transmitting/receiving to allow time for the clock to settle.

## 4.2.46 Serial Communications Interface (SCI) UART (r\_sci\_uart)

### Modules

#### Functions

```
fsp_err_t R_SCI_UART_Open (uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SCI_UART_Read (uart_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

```
fsp_err_t R_SCI_UART_Write (uart_ctrl_t *const p_api_ctrl, uint8_t const *const p_src, uint32_t const bytes)
```

```
fsp_err_t R_SCI_UART_BaudSet (uart_ctrl_t *const p_api_ctrl, void const *const p_baud_setting)
```

```
fsp_err_t R_SCI_UART_InfoGet (uart_ctrl_t *const p_api_ctrl, uart_info_t *const p_info)
```

fsp\_err\_t R\_SCI\_UART\_Close (uart\_ctrl\_t \*const p\_api\_ctrl)

fsp\_err\_t R\_SCI\_UART\_Abort (uart\_ctrl\_t \*const p\_api\_ctrl, uart\_dir\_t communication\_to\_abort)

fsp\_err\_t R\_SCI\_UART\_BaudCalculate (uint32\_t baudrate, bool bitrate\_modulation, uint32\_t baud\_rate\_error\_x\_1000, baud\_setting\_t \*const p\_baud\_setting)

fsp\_err\_t R\_SCI\_UART\_CallbackSet (uart\_ctrl\_t \*const p\_api\_ctrl, void(\*p\_callback)(uart\_callback\_args\_t \*), void const \*const p\_context, uart\_callback\_args\_t \*const p\_callback\_memory)

fsp\_err\_t R\_SCI\_UART\_ReadStop (uart\_ctrl\_t \*const p\_api\_ctrl, uint32\_t \*remaining\_bytes)

## Detailed Description

Driver for the SCI peripheral on RA MCUs. This module implements the [UART Interface](#).

## Overview

### Features

The SCI UART module supports the following features:

- Full-duplex UART communication
- Interrupt-driven data transmission and reception
- Invoking the user-callback function with an event code (RX/TX complete, TX data empty, RX char, error, etc)
- Baud-rate change at run-time
- Bit rate modulation and noise cancellation
- CTS/RTS hardware flow control (with an associated pin)
- Integration with the DTC transfer module
- Abort in-progress read/write operations
- FIFO support on supported channels

## Configuration

### Build Time Configurations for r\_sci\_uart

The following build time configurations are defined in fsp\_cfg/r\_sci\_uart\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
FIFO Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable FIFO support for the SCI_UART module.

DTC Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable DTC support for the SCI_UART module.
Flow Control Support	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable RS232 and RS485 flow control support using a user provided pin.

### Configurations for Driver > Connectivity > UART Driver on r\_sci\_uart

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > UART Driver on r\_sci\_uart. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_uart0	Module name.
General > Channel	Value must be a non-negative integer	0	Select the SCI channel.
General > Data Bits	<ul style="list-style-type: none"> <li>• 8bits</li> <li>• 7bits</li> <li>• 9bits</li> </ul>	8bits	Select the number of bits per word.
General > Parity	<ul style="list-style-type: none"> <li>• None</li> <li>• Odd</li> <li>• Even</li> </ul>	None	Select the parity mode.
General > Stop Bits	<ul style="list-style-type: none"> <li>• 1bit</li> <li>• 2bits</li> </ul>	1bit	Select the number of stop bits.
Baud > Baud Rate	Value must be an integer greater than 0	115200	Enter the desired baud rate.  If the requested baud rate cannot be achieved, the settings with the smallest percent error are used. The theoretical calculated baud rate and percent error are printed in a comment in the generated <a href="#">baud_setting_t</a> structure.
Baud > Baud Rate Modulation	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enabling baud rate modulation reduces the percent error of the actual baud rate with respect to the requested baud rate. It does this by modulating the number

Baud > Max Error (%)	Must be a valid non negative integer with a maximum configurable value of 100	5	of cycles per clock, so some bits are slightly longer than others.  Maximum percent error allowed during baud calculation. This is used by the algorithm to determine whether or not to consider using less accurate alternative register settings.
			NOTE: The baud calculation does not show an error in the tool if this percent error was not achieved. The calculated percent error is recorded in a comment in the generated <a href="#">baud_setting_t</a> structure.
Flow Control > CTS/RTS Selection	<ul style="list-style-type: none"> <li>• Hardware CTS</li> <li>• Hardware RTS</li> <li>• Hardware CTS and Software RTS</li> </ul>	Hardware RTS	Select CTS or RTS for the CTSn/RTSn pin of SCI channel n. The SCI hardware supports either the CTS or the RTS control signal on this pin but not both.
Flow Control > Software RTS Port	Refer to the RA Configuration tool for available options.	Disabled	Specify the flow control pin port for the MCU.
Flow Control > Software RTS Pin	Refer to the RA Configuration tool for available options.	Disabled	Specify the flow control pin for the MCU.
Extra > Clock Source	<ul style="list-style-type: none"> <li>• Internal Clock</li> <li>• Internal Clock With Output on SCK</li> <li>• External Clock 8x baud rate</li> <li>• External Clock 16x baud rate</li> </ul>	Internal Clock	Selection of the clock source to be used in the baud-rate clock generator. When internal clock is used the baud rate can be output on the SCK pin.
Extra > Start bit detection	<ul style="list-style-type: none"> <li>• Falling Edge</li> <li>• Low Level</li> </ul>	Falling Edge	Start bit detected as falling edge or low level.
Extra > Noise Filter	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Enable the digital noise filter on RXDn pin. The digital noise filter block

Extra > Receive FIFO Trigger Level	<ul style="list-style-type: none"> <li>• One</li> <li>• Max</li> </ul>	Max	in SCI consists of two-stage flipflop circuits.  Unused if the channel has no FIFO or if DTC is used for reception. Set to One to get a callback immediately when each byte is received. Set to Max to get a callback when FIFO is full or after 15 bit times with no data (fewer interrupts).
Interrupts > Callback	Name must be a valid C symbol	user_uart_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Interrupts > Receive Interrupt Priority	MCU Specific Options		Select the receive interrupt priority.
Interrupts > Transmit Data Empty Interrupt Priority	MCU Specific Options		Select the transmit interrupt priority.
Interrupts > Transmit End Interrupt Priority	MCU Specific Options		Select the transmit end interrupt priority.
Interrupts > Error Interrupt Priority	MCU Specific Options		Select the error interrupt priority.

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA2E1	PCLKB
RA2L1	PCLKB
RA4M1	PCLKA
RA4M2	PCLKA
RA4M3	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA

RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA
RA6M5	PCLKA
RA6T1	PCLKA

The clock source for the baud-rate clock generator can be selected from the internal clock, the external clock times 8 or the external clock times 16. The external clock is supplied to the SCK pin.

### Pin Configuration

This module uses TXD and RXD to communicate to external devices. CTS or RTS can be controlled by the hardware. If both are desired a GPIO pin can be used for RTS. When the internal clock is the source for the baud-rate generator the SCK pin can be used to output a clock with the same frequency as the bit rate.

## Usage Notes

- When configured for CTS and RTS the configured flow control pin will be used for RTS. The pin will be set high inside of the receive ISR while data is being read. It will be set low when all data is read.

### Limitations

- Transfer size must be less than or equal to 64K bytes if DTC interface is used for transfer. [uart\\_api\\_t::infoGet](#) API can be used to get the max transfer size allowed.
- Reception is still enabled after [uart\\_api\\_t::communicationAbort](#) API is called. Any characters received after abort and before the next call to read will arrive via the callback function with event `UART_EVENT_RX_CHAR`.
- When using 9-bit reception with DTC, clear the upper 7 bits of data before processing the read data. The upper 7 bits contain status flags that are part of the register used to read data in 9-bit mode.

## Examples

### SCI UART Example

```
uint8_t g_dest[TRANSFER_LENGTH];
uint8_t g_src[TRANSFER_LENGTH];
uint8_t g_out_of_band_received[TRANSFER_LENGTH];
uint32_t g_transfer_complete = 0;
uint32_t g_receive_complete = 0;
uint32_t g_out_of_band_index = 0;
void r_sci_uart_basic_example (void)
{
    /* Initialize p_src to known data */
```

```
for (uint32_t i = 0; i < TRANSFER_LENGTH; i++)
{
    g_src[i] = (uint8_t) ('A' + (i % 26));
}

/* Open the transfer instance with initial configuration. */
fsp_err_t err = R_SCI_UART_Open(&g_uart0_ctrl, &g_uart0_cfg);
assert(FSP_SUCCESS == err);
err = R_SCI_UART_Read(&g_uart0_ctrl, g_dest, TRANSFER_LENGTH);
assert(FSP_SUCCESS == err);
err = R_SCI_UART_Write(&g_uart0_ctrl, g_src, TRANSFER_LENGTH);
assert(FSP_SUCCESS == err);

while (!g_transfer_complete)
{
}

while (!g_receive_complete)
{
}
}

void example_callback (uart_callback_args_t * p_args)
{
    /* Handle the UART event */
    switch (p_args->event)
    {
        /* Received a character */
        case UART_EVENT_RX_CHAR:
            {
                /* Only put the next character in the receive buffer if there is space for it */
                if (sizeof(g_out_of_band_received) > g_out_of_band_index)
                {
                    /* Write either the next one or two bytes depending on the receive data size */
                    if (UART_DATA_BITS_8 >= g_uart0_cfg.data_bits)
                    {
                        g_out_of_band_received[g_out_of_band_index++] = (uint8_t)
p_args->data;
                    }
                }
            }
        }
    }
}
```

```
    }
else
    {
        uint16_t * p_dest = (uint16_t *)
&g_out_of_band_received[g_out_of_band_index];
        *p_dest          = (uint16_t) p_args->data;
        g_out_of_band_index += 2;
    }
}
break;
}

/* Receive complete */
case UART_EVENT_RX_COMPLETE:
    {
        g_receive_complete = 1;
break;
    }

/* Transmit complete */
case UART_EVENT_TX_COMPLETE:
    {
        g_transfer_complete = 1;
break;
    }
default:
    {
    }
}
}
```

### SCI UART Baud Set Example

```
#define SCI_UART_BAUDRATE_19200 (19200)
void r_sci_uart_baud_example (void)
{
    baud_setting_t baud_setting;
```

```

uint32_t      baud_rate          = SCI_UART_BAUDRATE_19200;
bool          enable_bitrate_modulation = false;
uint32_t      error_rate_x_1000  = 5;

fsp_err_t err = R_SCI_UART_BaudCalculate(baud_rate, enable_bitrate_modulation,
error_rate_x_1000, &baud_setting);

assert(FSP_SUCCESS == err);

err = R_SCI_UART_BaudSet(&g_uart0_ctrl, (void *) &baud_setting);

assert(FSP_SUCCESS == err);
}

```

## Data Structures

struct [sci\\_uart\\_instance\\_ctrl\\_t](#)

struct [baud\\_setting\\_t](#)

struct [sci\\_uart\\_extended\\_cfg\\_t](#)

## Enumerations

enum [sci\\_clk\\_src\\_t](#)

enum [sci\\_uart\\_flow\\_control\\_t](#)

enum [sci\\_uart\\_rx\\_fifo\\_trigger\\_t](#)

enum [sci\\_uart\\_start\\_bit\\_detect\\_t](#)

enum [sci\\_uart\\_noise\\_cancellation\\_t](#)

## Data Structure Documentation

### ◆ sci\_uart\_instance\_ctrl\_t

struct [sci\\_uart\\_instance\\_ctrl\\_t](#)

UART instance control block.

### ◆ baud\_setting\_t

struct [baud\\_setting\\_t](#)

Register settings to achieve a desired baud rate and modulation duty.

Data Fields

union <a href="#">baud_setting_t</a>	<a href="#">__unnamed__</a>	
uint8_t	cks: 2	CKS value to get divisor (CKS =

		N)
uint8_t	brr	Bit Rate Register setting.
uint8_t	mddr	Modulation Duty Register setting.

#### ◆ sci\_uart\_extended\_cfg\_t

struct sci_uart_extended_cfg_t		
UART on SCI device Configuration		
Data Fields		
sci_clk_src_t	clock	The source clock for the baud-rate generator. If internal optionally output baud rate on SCK.
sci_uart_start_bit_detect_t	rx_edge_start	Start reception on falling edge.
sci_uart_noise_cancellation_t	noise_cancel	Noise cancellation setting.
baud_setting_t *	p_baud_setting	Register settings for a desired baud rate.
sci_uart_rx_fifo_trigger_t	rx_fifo_trigger	Receive FIFO trigger level, unused if channel has no FIFO or if DTC is used.
bsp_io_port_pin_t	flow_control_pin	UART Driver Enable pin.
sci_uart_flow_control_t	flow_control	CTS/RTS function of the SSn pin.

## Enumeration Type Documentation

#### ◆ sci\_clk\_src\_t

enum sci_clk_src_t	
Enumeration for SCI clock source	
Enumerator	
SCI_UART_CLOCK_INT	Use internal clock for baud generation.
SCI_UART_CLOCK_INT_WITH_BAUDRATE_OUTPUT	Use internal clock for baud generation and output on SCK.
SCI_UART_CLOCK_EXT8X	Use external clock 8x baud rate.
SCI_UART_CLOCK_EXT16X	Use external clock 16x baud rate.

◆ **sci\_uart\_flow\_control\_t**

enum <a href="#">sci_uart_flow_control_t</a>	
UART flow control mode definition	
Enumerator	
SCI_UART_FLOW_CONTROL_RTS	Use SCI pin for RTS.
SCI_UART_FLOW_CONTROL_CTS	Use SCI pin for CTS.
SCI_UART_FLOW_CONTROL_CTSRTS	Use SCI pin for CTS, external pin for RTS.

◆ **sci\_uart\_rx\_fifo\_trigger\_t**

enum <a href="#">sci_uart_rx_fifo_trigger_t</a>	
Receive FIFO trigger configuration.	
Enumerator	
SCI_UART_RX_FIFO_TRIGGER_1	Callback after each byte is received without buffering.
SCI_UART_RX_FIFO_TRIGGER_MAX	Callback when FIFO is full or after 15 bit times with no data (fewer interrupts)

◆ **sci\_uart\_start\_bit\_detect\_t**

enum <a href="#">sci_uart_start_bit_detect_t</a>	
Asynchronous Start Bit Edge Detection configuration.	
Enumerator	
SCI_UART_START_BIT_LOW_LEVEL	Detect low level on RXDn pin as start bit.
SCI_UART_START_BIT_FALLING_EDGE	Detect falling level on RXDn pin as start bit.

◆ **sci\_uart\_noise\_cancellation\_t**

enum <code>sci_uart_noise_cancellation_t</code>	
Noise cancellation configuration.	
Enumerator	
<code>SCI_UART_NOISE_CANCELLATION_DISABLE</code>	Disable noise cancellation.
<code>SCI_UART_NOISE_CANCELLATION_ENABLE</code>	Enable noise cancellation.

**Function Documentation**◆ **R\_SCI\_UART\_Open()**

`fsp_err_t R_SCI_UART_Open ( uart_ctrl_t *const p_api_ctrl, uart_cfg_t const *const p_cfg )`

Configures the UART driver based on the input configurations. If reception is enabled at compile time, reception is enabled at the end of this function. Implements `uart_api_t::open`

**Return values**

<code>FSP_SUCCESS</code>	Channel opened successfully.
<code>FSP_ERR_ASSERTION</code>	Pointer to UART control block or configuration structure is NULL.
<code>FSP_ERR_IP_CHANNEL_NOT_PRESENT</code>	The requested channel does not exist on this MCU.
<code>FSP_ERR_INVALID_ARGUMENT</code>	Flow control is enabled but flow control pin is not defined.
<code>FSP_ERR_ALREADY_OPEN</code>	Control block has already been opened or channel is being used by another instance. Call <code>close()</code> then <code>open()</code> to reconfigure.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::open`

◆ **R\_SCI\_UART\_Read()**

```
fsp_err_t R_SCI_UART_Read ( uart_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes )
```

Receives user specified number of bytes into destination buffer pointer. Implements [uart\\_api\\_t::read](#)

**Return values**

FSP_SUCCESS	Data reception successfully ends.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL. Number of transfers outside the max or min boundary when transfer instance used
FSP_ERR_INVALID_ARGUMENT	Destination address or data size is not valid for 9-bit mode.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_IN_USE	A previous read operation is still in progress.
FSP_ERR_UNSUPPORTED	SCI_UART_CFG_RX_ENABLE is set to 0

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

**Note**

*If 9-bit data length is specified at R\_SCI\_UART\_Open call, p\_dest must be aligned 16-bit boundary.*

◆ **R\_SCI\_UART\_Write()**

```
fsp_err_t R_SCI_UART_Write ( uart_ctrl_t *const p_api_ctrl, uint8_t const *const p_src, uint32_t const bytes )
```

Transmits user specified number of bytes from the source buffer pointer. Implements [uart\\_api\\_t::write](#)

**Return values**

FSP_SUCCESS	Data transmission finished successfully.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL. Number of transfers outside the max or min boundary when transfer instance used
FSP_ERR_INVALID_ARGUMENT	Source address or data size is not valid for 9-bit mode.
FSP_ERR_NOT_OPEN	The control block has not been opened
FSP_ERR_IN_USE	A UART transmission is in progress
FSP_ERR_UNSUPPORTED	SCI_UART_CFG_TX_ENABLE is set to 0

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

**Note**

*If 9-bit data length is specified at R\_SCI\_UART\_Open call, p\_src must be aligned on a 16-bit boundary.*

◆ **R\_SCI\_UART\_BaudSet()**

```
fsp_err_t R_SCI_UART_BaudSet ( uart_ctrl_t *const p_api_ctrl, void const *const p_baud_setting )
```

Updates the baud rate using the clock selected in Open. p\_baud\_setting is a pointer to a [baud\\_setting\\_t](#) structure. Implements [uart\\_api\\_t::baudSet](#)

**Warning**

This terminates any in-progress transmission.

**Return values**

FSP_SUCCESS	Baud rate was successfully changed.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL or the UART is not configured to use the internal clock.
FSP_ERR_NOT_OPEN	The control block has not been opened

## ◆ R\_SCI\_UART\_InfoGet()

```
fsp_err_t R_SCI_UART_InfoGet ( uart_ctrl_t *const p_api_ctrl, uart_info_t *const p_info )
```

Provides the driver information, including the maximum number of bytes that can be received or transmitted at a time. Implements `uart_api_t::infoGet`

**Return values**

FSP_SUCCESS	Information stored in provided p_info.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

## ◆ R\_SCI\_UART\_Close()

```
fsp_err_t R_SCI_UART_Close ( uart_ctrl_t *const p_api_ctrl)
```

Aborts any in progress transfers. Disables interrupts, receiver, and transmitter. Closes lower level transfer drivers if used. Removes power. Implements `uart_api_t::close`

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened

### ◆ R\_SCI\_UART\_Abort()

`fsp_err_t R_SCI_UART_Abort ( uart_ctrl_t *const p_api_ctrl, uart_dir_t communication_to_abort )`

Provides API to abort ongoing transfer. Transmission is aborted after the current character is transmitted. Reception is still enabled after abort(). Any characters received after abort() and before the transfer is reset in the next call to read(), will arrive via the callback function with event UART\_EVENT\_RX\_CHAR. Implements `uart_api_t::communicationAbort`

#### Return values

FSP_SUCCESS	UART transaction aborted successfully.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_UNSUPPORTED	The requested Abort direction is unsupported.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::disable`

◆ **R\_SCI\_UART\_BaudCalculate()**

```
fsp_err_t R_SCI_UART_BaudCalculate ( uint32_t baudrate, bool bitrate_modulation, uint32_t
baud_rate_error_x_1000, baud_setting_t*const p_baud_setting )
```

Calculates baud rate register settings. Evaluates and determines the best possible settings set to the baud rate related registers.

**Parameters**

[in]	baudrate	Baud rate [bps]. For example, 19200, 57600, 115200, etc.
[in]	bitrate_modulation	Enable bitrate modulation
[in]	baud_rate_error_x_1000	<baud_rate_percent_error> x 1000 required for module to function. Absolute max baud_rate_error is 15000 (15%).
[out]	p_baud_setting	Baud setting information stored here if successful

**Return values**

FSP_SUCCESS	Baud rate is set successfully
FSP_ERR_ASSERTION	Null pointer
FSP_ERR_INVALID_ARGUMENT	Baud rate is '0', source clock frequency could not be read, or error in calculated baud rate is larger than 10%.

◆ **R\_SCI\_UART\_CallbackSet()**

```
fsp_err_t R_SCI_UART_CallbackSet ( uart_ctrl_t*const p_api_ctrl, void(*) (uart_callback_args_t*)
p_callback, void const*const p_context, uart_callback_args_t*const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `uart_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

### ◆ R\_SCI\_UART\_ReadStop()

```
fsp_err_t R_SCI_UART_ReadStop ( uart_ctrl_t *const p_api_ctrl, uint32_t * remaining_bytes )
```

Provides API to abort ongoing read. Reception is still enabled after abort(). Any characters received after abort() and before the transfer is reset in the next call to read(), will arrive via the callback function with event UART\_EVENT\_RX\_CHAR. Implements [uart\\_api\\_t::readStop](#)

#### Return values

FSP_SUCCESS	UART transaction aborted successfully.
FSP_ERR_ASSERTION	Pointer to UART control block is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_UNSUPPORTED	The requested Abort direction is unsupported.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::disable](#)

## 4.2.47 Sigma Delta Analog to Digital Converter (r\_sdadc)

### Modules

#### Functions

```
fsp_err_t R_SDADC_Open (adc_ctrl_t *p_ctrl, adc_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SDADC_ScanCfg (adc_ctrl_t *p_ctrl, void const *const p_extend)
```

```
fsp_err_t R_SDADC_InfoGet (adc_ctrl_t *p_ctrl, adc_info_t *p_adc_info)
```

```
fsp_err_t R_SDADC_ScanStart (adc_ctrl_t *p_ctrl)
```

```
fsp_err_t R_SDADC_ScanStop (adc_ctrl_t *p_ctrl)
```

```
fsp_err_t R_SDADC_StatusGet (adc_ctrl_t *p_ctrl, adc_status_t *p_status)
```

```
fsp_err_t R_SDADC_Read (adc_ctrl_t *p_ctrl, adc_channel_t const reg_id,
uint16_t *const p_data)
```

```
fsp_err_t R_SDADC_Read32 (adc_ctrl_t *p_ctrl, adc_channel_t const reg_id,
uint32_t *const p_data)
```

```
fsp_err_t R_SDADC_OffsetSet (adc_ctrl_t *const p_ctrl, adc_channel_t const
reg_id, int32_t const offset)
```

```
fsp_err_t R_SDADC_Calibrate (adc_ctrl_t *const p_ctrl, void *const p_extend)
```

```
fsp_err_t R_SDADC_Close (adc_ctrl_t *p_ctrl)
```

## Detailed Description

Driver for the SDADC24 peripheral on RA MCUs. This module implements the [ADC Interface](#).

## Overview

### Features

The SDADC module supports the following features:

- 24 bit maximum resolution
- Configure scans to include:
  - Multiple analog channels
  - Outputs of OPAMP0 (P side) and OPAMP1 (N side) of SDADC channel 4
- Configurable scan start trigger:
  - Software scan triggers
  - Hardware scan triggers (timer expiration, for example)
- Configurable scan mode:
  - Single scan mode, where each trigger starts a single scan
  - Continuous scan mode, where all channels are scanned continuously
- Supports averaging converted samples
- Optional callback when single conversion, entire scan, or calibration completes
- Supports reading converted data
- Sample and hold support

### Selecting an ADC

All RA MCUs have an [Analog to Digital Converter \(r\\_adc\)](#). Only select RA MCUs have an SDADC. When selecting between them, consider these factors. Refer to the hardware manual for details.

	ADC	SDADC
Availability	Available on all RA MCUs.	Available on select RA MCUs.
Resolution	The ADC has a maximum resolution of 12, 14, or 16 bits depending on the MCU.	The SDADC has a maximum accuracy of 24 bits.
Number of Channels	The ADC has more channels than the SDADC.	The SDADC 5 channels, one of which is tied to OPAMP0 and OPAMP1.
Frequency	The ADC sampling time is shorter (more samples per second).	The SDADC sampling time is longer (fewer samples per second).
Settling Time	The ADC does not have a settling time when switching between channels.	The SDADC requires a settling time when switching between channels.

## Configuration

### Build Time Configurations for r\_sdadc

The following build time configurations are defined in fsp\_cfg/r\_sdadc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Analog > ADC Driver on r\_sdadc

This module can be added to the Stacks tab via New Stack > Driver > Analog > ADC Driver on r\_sdadc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_adc0	Module name.
Mode	<ul style="list-style-type: none"> <li>Single Scan</li> <li>Continuous Scan</li> </ul>	Continuous Scan	In single scan mode, all channels are converted once per start trigger, and conversion stops after all enabled channels are scanned. In continuous scan mode, conversion starts after a start trigger, then continues until stopped in software.
Resolution	<ul style="list-style-type: none"> <li>16 Bit</li> <li>24 Bit</li> </ul>	24 Bit	Select 24-bit or 16-bit resolution.
Alignment	<ul style="list-style-type: none"> <li>Right</li> <li>Left</li> </ul>	Right	Select left or right alignment.
Trigger	MCU Specific Options		Select conversion start trigger. Conversion can be started in software, or conversion can be started when a hardware event occurs if the hardware event is linked to the SDADC peripheral using the ELC API.
Vref Source	<ul style="list-style-type: none"> <li>Internal</li> <li>External</li> </ul>	Internal	Vref can be source internally and output

on the SBIAS pin, or Vref can be input from VREFI.

Vref Voltage	<ul style="list-style-type: none"> <li>• 0.8 V</li> <li>• 1.0 V</li> <li>• 1.2 V</li> <li>• 1.4 V</li> <li>• 1.6 V</li> <li>• 1.8 V</li> <li>• 2.0 V</li> <li>• 2.2 V</li> <li>• 2.4 V</li> </ul>	1.0 V	Select Vref voltage. If Vref is input externally, the voltage on VREFI must match the voltage selected within 3%.
Callback	Name must be a valid C symbol	NULL	Enter the name of the callback function to be called when conversion completes or a scan ends.
Conversion End Interrupt Priority	MCU Specific Options		[Required] Select the interrupt priority for the conversion end interrupt.
Scan End Interrupt Priority	MCU Specific Options		[Optional] Select the interrupt priority for the scan end interrupt.
Calibration End Interrupt Priority	MCU Specific Options		[Optional] Select the interrupt priority for the calibration end interrupt.

### Configurations for Driver > Analog > SDADC Channel Configuration on r\_sdadc

This module can be added to the Stacks tab via New Stack > Driver > Analog > SDADC Channel Configuration on r\_sdadc.

Configuration	Options	Default	Description
Input	<ul style="list-style-type: none"> <li>• Differential</li> <li>• Single Ended</li> </ul>	Differential	Select differential or single-ended input.
Stage 1 Gain	<ul style="list-style-type: none"> <li>• 1</li> <li>• 2</li> <li>• 3</li> <li>• 4</li> <li>• 8</li> </ul>	1	Select the gain for stage 1 of the PGA. Must be 1 for single-ended input.
Stage 2 Gain	<ul style="list-style-type: none"> <li>• 1</li> <li>• 2</li> <li>• 4</li> <li>• 8</li> </ul>	1	Select the gain for stage 2 of the PGA. Must be 1 for single-ended input.
Oversampling Ratio	<ul style="list-style-type: none"> <li>• 64</li> <li>• 128</li> <li>• 256</li> </ul>	256	Select the oversampling ratio for the PGA. Must be 256

	<ul style="list-style-type: none"> <li>• 512</li> <li>• 1024</li> <li>• 2048</li> </ul>		for single-ended input.
Polarity (Valid for Single-Ended Input Only)	<ul style="list-style-type: none"> <li>• Positive</li> <li>• Negative</li> </ul>	Positive	Select positive or negative polarity for single-ended input. VBIAS (1.0 V typical) is connected on the opposite input.
Conversions to Average per Result	<ul style="list-style-type: none"> <li>• Do Not Average (Interrupt after Each Conversion)</li> <li>• Average 8</li> <li>• Average 16</li> <li>• Average 32</li> <li>• Average 64</li> </ul>	Do Not Average (Interrupt after Each Conversion)	Select the number of conversions to average for each result. The ADC_EVENT_CONVERSION_END event occurs after each average, or after each individual conversion if averaging is disabled.
Invert (Valid for Negative Single-Ended Input Only)	<ul style="list-style-type: none"> <li>• Result Not Inverted</li> <li>• Result Inverted</li> </ul>	Result Not Inverted	Select whether to invert negative single-ended input. When the result is inverted, the lowest measurable voltage gives a result of 0, and the highest measurable voltage gives a result of $2^{\text{resolution}} - 1$ .
Number of Conversions Per Scan	Refer to the RA Configuration tool for available options.	1	Number of conversions on this channel before AUTOSCAN moves to the next channel. When all conversions of all channels are complete, the ADC_EVENT_SCAN_END event occurs.

## Clock Configuration

The SDADC clock is configurable on the clocks tab.

The SDADC clock must be 4 MHz when the SDADC is used.

## Pin Configuration

The ANSDnP (n = 0-3) pins are analog input channels that can be used with the SDADC.

# Usage Notes

## Scan Procedure

In this document, the term "scan" refers to the AUTOSCAN feature of the SDADC, which works as follows:

1. Conversions are performed on enabled channels in ascending order of channel number. All conversions required for a single channel are completed before the sequencer moves to the next channel.
2. Conversions are performed at the rate (in Hz) of the SDADC oversampling clock frequency / oversampling ratio (configured per channel). The FSP uses the normal mode SDADC oversampling clock frequency.
3. If averaging is enabled for the channel, the number of conversions to average are performed before each conversion end interrupt occurs.
4. If the number of conversions for the channel is more than 1, SDADC performs the number of conversions requested. These are performed consecutively. There is a settling time associated with switching channels. Performing all of the requested conversions for each channel at a time avoids this settling time after the first conversion.

If averaging is enabled for the channel, each averaged result counts as a single conversion.

5. Continues to the next enabled channel only after completing all conversions requested.
6. After all enabled channels are scanned, a scan end interrupt occurs. The driver supports single-scan and continuous scan operation modes.
  - Single-scan mode performs one scan per trigger (hardware trigger or software start using [R\\_SDADC\\_ScanStart](#)).
  - In continuous scan mode, the scan is restarted after each scan completes. A single trigger is required to start continuous operation of the SDADC.

## When Interrupts Are Not Enabled

If interrupts are not enabled, the [R\\_SDADC\\_StatusGet\(\)](#) API can be used to poll the SDADC to determine when the scan has completed. The [R\\_SDADC\\_Read\(\)](#) API function is used to access the converted SDADC result. This applies to both normal scans and calibration scans.

## Calibration

Calibration is required to use the SDADC if any channel is configured for differential mode. Call [R\\_SDADC\\_Calibrate\(\)](#) after open, and prior to any other function, then wait for a calibration complete event before using the SDADC. [R\\_SDADC\\_Calibrate\(\)](#) should not be called if all channels are configured for single-ended mode.

# Examples

## Basic Example

This is a basic example of minimal use of the SDADC in an application.

```
void sdadc_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
}
```

```
err = R_SDADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Calibrate all differential channels. */
sdadc_calibrate_args_t calibrate_args;
calibrate_args.mode      = SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET;
calibrate_args.channel  = ADC_CHANNEL_0;
err = R_SDADC_Calibrate(&g_adc0_ctrl, &calibrate_args);
assert(FSP_SUCCESS == err);
/* Wait for calibration to complete. */
adc_status_t status;
status.state = ADC_STATE_SCAN_IN_PROGRESS;
while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
{
R_SDADC_StatusGet(&g_adc0_ctrl, &status);
}
/* In software trigger mode, start a scan by calling R_SDADC_ScanStart(). In other
modes, enable external
* triggers by calling R_SDADC_ScanStart(). */
(void) R_SDADC_ScanStart(&g_adc0_ctrl);
/* Wait for conversion to complete. */
status.state = ADC_STATE_SCAN_IN_PROGRESS;
while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
{
R_SDADC_StatusGet(&g_adc0_ctrl, &status);
}
/* Read converted data. */
uint32_t channel1_conversion_result;
R_SDADC_Read32(&g_adc0_ctrl, ADC_CHANNEL_1, &channel1_conversion_result);
}
```

## Using DTC or DMAC with the SDADC

If desired, the DTC or DMAC can be used to store each conversion result in a circular buffer. An example configuration is below.

```
/* Example DTC transfer settings to used with SDADC. */
/* The transfer length should match the total number of conversions per scan. This
example assumes the SDADC is
 * configured to scan channel 1 three times, then channel 2 and channel 4 once, for a
total of 5 conversions. */
#define SDADC_EXAMPLE_TRANSFER_LENGTH (5)
uint32_t g_sdadc_example_buffer[SDADC_EXAMPLE_TRANSFER_LENGTH];
transfer_info_t g_sdadc_transfer_info =
{
    .dest_addr_mode = TRANSFER_ADDR_MODE_INCREMENTED,
    .repeat_area    = TRANSFER_REPEAT_AREA_DESTINATION,
    .irq            = TRANSFER_IRQ_END,
    .chain_mode     = TRANSFER_CHAIN_MODE_DISABLED,
    .src_addr_mode  = TRANSFER_ADDR_MODE_FIXED,
    .mode           = TRANSFER_MODE_REPEAT,
    /* NOTE: The data transferred will contain a 24-bit converted value in bits 23:0.
Bit 24 contains a status flag
 * indicating if the result overflowed or not. Bits 27:25 contain the channel number
+ 1. The settings for
 * resolution and alignment and ignored when DTC or DMAC is used. */
    .size           = TRANSFER_SIZE_4_BYTE,
    /* NOTE: It is strongly recommended to enable averaging on all channels or no
channels when using DTC with SDADC
 * because the result register is different when averaging is used. If averaging is
enabled on all channels,
 * set transfer_info_t::p_src to &R_SDADC->ADAR. */
    .p_src          = (void const *) &R_SDADC0->ADCR,
    .p_dest         = &g_sdadc_example_buffer[0],
    .length         = SDADC_EXAMPLE_TRANSFER_LENGTH,
};
void sdadc_dtc_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
```

```
err = R_SDADC_Open(&g_adc0_ctrl, &g_adc0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Calibrate all differential channels. */
sdadc_calibrate_args_t calibrate_args;
calibrate_args.mode      = SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET;
calibrate_args.channel = ADC_CHANNEL_0;
err = R_SDADC_Calibrate(&g_adc0_ctrl, &calibrate_args);
assert(FSP_SUCCESS == err);
/* Wait for calibration to complete. */
adc_status_t status;
status.state = ADC_STATE_SCAN_IN_PROGRESS;
while (ADC_STATE_SCAN_IN_PROGRESS == status.state)
{
R_SDADC_StatusGet(&g_adc0_ctrl, &status);
}
/* In software trigger mode, start a scan by calling R_SDADC_ScanStart(). In other
modes, enable external
* triggers by calling R_SDADC_ScanStart(). */
(void) R_SDADC_ScanStart(&g_adc0_ctrl);
/* After each conversion, the converted data is transferred to the next index in
g_sdadc_example_buffer. After
* the entire scan completes, the index in g_sdadc_example_buffer resets. The data
in g_sdadc_example_buffer
* is:
* - g_sdadc_example_buffer[0] = SDADC channel 1 conversion 0
* - g_sdadc_example_buffer[1] = SDADC channel 1 conversion 1
* - g_sdadc_example_buffer[2] = SDADC channel 1 conversion 2
* - g_sdadc_example_buffer[3] = SDADC channel 2 conversion 0
* - g_sdadc_example_buffer[4] = SDADC channel 4 conversion 0
*/* At any point in the application after the first scan completes, the most
recent data for channel 2 can be read
* from the buffer like this. Shifting removes the unrelated bits in the result
register and propagates the sign
```

```
* bit so the value can be interpreted as a signed result. This assumes channel 2 is
configured in differential
* mode. */
int32_t channel_2_data = (int32_t) (g_sdadc_example_buffer[3] << 8) >> 8;
FSP_PARAMETER_NOT_USED(channel_2_data);
}
```

## Data Structures

struct [sdadc\\_calibrate\\_args\\_t](#)

struct [sdadc\\_channel\\_cfg\\_t](#)

struct [sdadc\\_scan\\_cfg\\_t](#)

struct [sdadc\\_extended\\_cfg\\_t](#)

struct [sdadc\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [sdadc\\_vref\\_src\\_t](#)

enum [sdadc\\_vref\\_voltage\\_t](#)

enum [sdadc\\_channel\\_input\\_t](#)

enum [sdadc\\_channel\\_stage\\_1\\_gain\\_t](#)

enum [sdadc\\_channel\\_stage\\_2\\_gain\\_t](#)

enum [sdadc\\_channel\\_oversampling\\_t](#)

enum [sdadc\\_channel\\_polarity\\_t](#)

enum [sdadc\\_channel\\_average\\_t](#)

enum [sdadc\\_channel\\_inversion\\_t](#)

enum [sdadc\\_channel\\_count\\_formula\\_t](#)

enum [sdadc\\_calibration\\_t](#)

## Data Structure Documentation

### ◆ [sdadc\\_calibrate\\_args\\_t](#)

struct sdadc_calibrate_args_t		
Structure to pass to the <a href="#">adc_api_t::calibrate</a> p_extend argument.		
Data Fields		
<a href="#">adc_channel_t</a>	channel	Which channel to calibrate.
<a href="#">sdadc_calibration_t</a>	mode	Calibration mode.

◆ **sdadc\_channel\_cfg\_t**

struct sdadc_channel_cfg_t		
SDADC per channel configuration.		

◆ **sdadc\_scan\_cfg\_t**

struct sdadc_scan_cfg_t		
SDADC active channel configuration		
Data Fields		
uint32_t	scan_mask	Channels/bits: bit 0 is ch0; bit 15 is ch15.

◆ **sdadc\_extended\_cfg\_t**

struct sdadc_extended_cfg_t		
SDADC configuration extension. This extension is required and must be provided in <a href="#">adc_cfg_t::p_extend</a> .		
Data Fields		
uint8_t	conv_end_ipl	Conversion end interrupt priority.
IRQn_Type	conv_end_irq	
<a href="#">sdadc_vref_src_t</a>	vref_src	Source of Vref (internal or external)
<a href="#">sdadc_vref_voltage_t</a>	vref_voltage	Voltage of Vref, required for both internal and external Vref. If Vref is from an external source, the voltage must match the specified voltage within 3%.
<a href="#">sdadc_channel_cfg_t</a> const *	p_channel_cfgs[SDADC_MAX_N UM_CHANNELS]	Configuration for each channel, set to NULL if unused.

◆ **sdadc\_instance\_ctrl\_t**

struct sdadc_instance_ctrl_t		
ADC instance control block. DO NOT INITIALIZE. Initialized in <a href="#">adc_api_t::open()</a> .		

## Enumeration Type Documentation

### ◆ sdadc\_vref\_src\_t

enum sdadc_vref_src_t	
Source of Vref.	
Enumerator	
SDADC_VREF_SRC_INTERNAL	Vref is internally sourced, can be output as SBIAS.
SDADC_VREF_SRC_EXTERNAL	Vref is externally sourced from the VREFI pin.

### ◆ sdadc\_vref\_voltage\_t

enum sdadc_vref_voltage_t	
Voltage of Vref.	
Enumerator	
SDADC_VREF_VOLTAGE_800_MV	Vref is 0.8 V.
SDADC_VREF_VOLTAGE_1000_MV	Vref is 1.0 V.
SDADC_VREF_VOLTAGE_1200_MV	Vref is 1.2 V.
SDADC_VREF_VOLTAGE_1400_MV	Vref is 1.4 V.
SDADC_VREF_VOLTAGE_1600_MV	Vref is 1.6 V.
SDADC_VREF_VOLTAGE_1800_MV	Vref is 1.8 V.
SDADC_VREF_VOLTAGE_2000_MV	Vref is 2.0 V.
SDADC_VREF_VOLTAGE_2200_MV	Vref is 2.2 V.
SDADC_VREF_VOLTAGE_2400_MV	Vref is 2.4 V (only valid for external Vref)

◆ **sdadc\_channel\_input\_t**

enum <code>sdadc_channel_input_t</code>	
Per channel input mode.	
Enumerator	
<code>SDADC_CHANNEL_INPUT_DIFFERENTIAL</code>	Differential input.
<code>SDADC_CHANNEL_INPUT_SINGLE_ENDED</code>	Single-ended input.

◆ **sdadc\_channel\_stage\_1\_gain\_t**

enum <code>sdadc_channel_stage_1_gain_t</code>	
Per channel stage 1 gain options.	
Enumerator	
<code>SDADC_CHANNEL_STAGE_1_GAIN_1</code>	Gain of 1.
<code>SDADC_CHANNEL_STAGE_1_GAIN_2</code>	Gain of 2.
<code>SDADC_CHANNEL_STAGE_1_GAIN_3</code>	Gain of 3 (only valid for stage 1)
<code>SDADC_CHANNEL_STAGE_1_GAIN_4</code>	Gain of 4.
<code>SDADC_CHANNEL_STAGE_1_GAIN_8</code>	Gain of 8.

◆ **sdadc\_channel\_stage\_2\_gain\_t**

enum <code>sdadc_channel_stage_2_gain_t</code>	
Per channel stage 2 gain options.	
Enumerator	
<code>SDADC_CHANNEL_STAGE_2_GAIN_1</code>	Gain of 1.
<code>SDADC_CHANNEL_STAGE_2_GAIN_2</code>	Gain of 2.
<code>SDADC_CHANNEL_STAGE_2_GAIN_4</code>	Gain of 4.
<code>SDADC_CHANNEL_STAGE_2_GAIN_8</code>	Gain of 8.

◆ **sdadc\_channel\_oversampling\_t**

enum <code>sdadc_channel_oversampling_t</code>	
Per channel oversampling ratio.	
Enumerator	
<code>SDADC_CHANNEL_OVERSAMPLING_64</code>	Oversampling ratio of 64.
<code>SDADC_CHANNEL_OVERSAMPLING_128</code>	Oversampling ratio of 128.
<code>SDADC_CHANNEL_OVERSAMPLING_256</code>	Oversampling ratio of 256.
<code>SDADC_CHANNEL_OVERSAMPLING_512</code>	Oversampling ratio of 512.
<code>SDADC_CHANNEL_OVERSAMPLING_1024</code>	Oversampling ratio of 1024.
<code>SDADC_CHANNEL_OVERSAMPLING_2048</code>	Oversampling ratio of 2048.

◆ **sdadc\_channel\_polarity\_t**

enum <code>sdadc_channel_polarity_t</code>	
Per channel polarity, valid for single-ended input only.	
Enumerator	
<code>SDADC_CHANNEL_POLARITY_POSITIVE</code>	Positive-side single-ended input.
<code>SDADC_CHANNEL_POLARITY_NEGATIVE</code>	Negative-side single-ended input.

◆ **sdadc\_channel\_average\_t**

enum <code>sdadc_channel_average_t</code>	
Per channel number of conversions to average before conversion end callback.	
Enumerator	
<code>SDADC_CHANNEL_AVERAGE_NONE</code>	Do not average (callback for each conversion)
<code>SDADC_CHANNEL_AVERAGE_8</code>	Average 8 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_16</code>	Average 16 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_32</code>	Average 32 samples for each conversion end callback.
<code>SDADC_CHANNEL_AVERAGE_64</code>	Average 64 samples for each conversion end callback.

◆ **sdadc\_channel\_inversion\_t**

enum <code>sdadc_channel_inversion_t</code>	
Per channel polarity, valid for negative-side single-ended input only.	
Enumerator	
<code>SDADC_CHANNEL_INVERSION_OFF</code>	Do not invert conversion result.
<code>SDADC_CHANNEL_INVERSION_ON</code>	Invert conversion result.

◆ **sdadc\_channel\_count\_formula\_t**

enum <code>sdadc_channel_count_formula_t</code>	
Select a formula to specify the number of conversions. The following symbols are used in the formulas:	
<ul style="list-style-type: none"> <li>• N: Number of conversions</li> <li>• n: <code>sdadc_channel_cfg_t::coefficient_n</code>, do not set to 0 if m is 0</li> <li>• m: <code>sdadc_channel_cfg_t::coefficient_m</code>, do not set to 0 if n is 0</li> </ul> Either m or n must be non-zero.	
Enumerator	
<code>SDADC_CHANNEL_COUNT_FORMULA_EXPONENTIAL</code>	$N = 32 * (2 ^ n - 1) + m * 2 ^ n.$
<code>SDADC_CHANNEL_COUNT_FORMULA_LINEAR</code>	$N = (32 * n) + m.$

◆ **sdadc\_calibration\_t**

enum <code>sdadc_calibration_t</code>	
Calibration mode.	
Enumerator	
<code>SDADC_CALIBRATION_INTERNAL_GAIN_OFFSET</code>	Use internal reference to calibrate offset and gain.
<code>SDADC_CALIBRATION_EXTERNAL_OFFSET</code>	Use external reference to calibrate offset.
<code>SDADC_CALIBRATION_EXTERNAL_GAIN</code>	Use external reference to calibrate gain.

**Function Documentation**

◆ **R\_SDADC\_Open()**

```
fsp_err_t R_SDADC_Open ( adc_ctrl_t * p_ctrl, adc_cfg_t const *const p_cfg )
```

Applies power to the SDADC and initializes the hardware based on the user configuration. As part of this initialization, the SDADC clock is configured and enabled. If an interrupt priority is non-zero, enables an interrupt which will call a callback to notify the user when a conversion, scan, or calibration is complete. [R\\_SDADC\\_Calibrate\(\)](#) must be called after this function before using the SDADC if any channels are used in differential mode. Implements [adc\\_api\\_t::open\(\)](#).

**Note**

*This function delays at least 2 ms as required by the SDADC power on procedure.*

**Return values**

FSP_SUCCESS	Configuration successful.
FSP_ERR_ASSERTION	An input pointer is NULL or an input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Control block is already open.
FSP_ERR_IRQ_BSP_DISABLED	A required interrupt is disabled

◆ **R\_SDADC\_ScanCfg()**

```
fsp_err_t R_SDADC_ScanCfg ( adc_ctrl_t * p_ctrl, void const *const p_extend )
```

Configures the enabled channels of the ADC. Pass a pointer to [sdadc\\_scan\\_cfg\\_t](#) to p\_extend. Implements [adc\\_api\\_t::scanCfg\(\)](#).

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input pointer is NULL or an input parameter is invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_InfoGet()**

```
fsp_err_t R_SDADC_InfoGet ( adc_ctrl_t* p_ctrl, adc_info_t* p_adc_info )
```

Returns the address of the lowest number configured channel, the total number of results to be read in order to read the results of all configured channels, the size of each result, and the ELC event enumerations. Implements `adc_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Information stored in p_adc_info.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_ScanStart()**

```
fsp_err_t R_SDADC_ScanStart ( adc_ctrl_t* p_ctrl)
```

If the SDADC is configured for hardware triggers, enables hardware triggers. Otherwise, starts a scan. Implements `adc_api_t::scanStart()`.

**Return values**

FSP_SUCCESS	Scan started or hardware triggers enabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.
FSP_ERR_IN_USE	A conversion or calibration is in progress.

◆ **R\_SDADC\_ScanStop()**

```
fsp_err_t R_SDADC_ScanStop ( adc_ctrl_t* p_ctrl)
```

If the SDADC is configured for hardware triggers, disables hardware triggers. Otherwise, stops any in-progress scan started by software. Implements `adc_api_t::scanStop()`.

**Return values**

FSP_SUCCESS	Scan stopped or hardware triggers disabled successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_StatusGet()**

```
fsp_err_t R_SDADC_StatusGet ( adc_ctrl_t * p_ctrl, adc_status_t * p_status )
```

Returns the status of a scan started by software, including calibration scans. It is not possible to determine the status of a scan started by a hardware trigger. Implements [adc\\_api\\_t::scanStatusGet\(\)](#).

**Return values**

FSP_SUCCESS	No software scan or calibration is in progress.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_Read()**

```
fsp_err_t R_SDADC_Read ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint16_t *const p_data )
```

Reads the most recent conversion result from a channel. Truncates 24-bit results to the upper 16 bits. Implements [adc\\_api\\_t::read\(\)](#).

**Note**

*The result stored in p\_data is signed when the SDADC channel is configured in differential mode. Do not use this API if the conversion end interrupt (SDADC0\_ADI) is used to trigger the DTC unless the interrupt mode is set to TRANSFER\_IRQ\_EACH.*

**Return values**

FSP_SUCCESS	Conversion result in p_data.
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

◆ **R\_SDADC\_Read32()**

```
fsp_err_t R_SDADC_Read32 ( adc_ctrl_t * p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data )
```

Reads the most recent conversion result from a channel. Implements `adc_api_t::read32()`.

**Note**

*The result stored in `p_data` is signed when the SDADC channel is configured in differential mode. When the SDADC is configured for 24-bit resolution and right alignment, the sign bit is bit 23, and the upper 8 bits are 0. When the SDADC is configured for 16-bit resolution and right alignment, the sign bit is bit 15, and the upper 16 bits are 0.*

*Do not use this API if the conversion end interrupt (`SDADC0_ADI`) is used to trigger the DTC unless the interrupt mode is set to `TRANSFER_IRQ_EACH`.*

**Return values**

FSP_SUCCESS	Conversion result in <code>p_data</code> .
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_SDADC\_OffsetSet()

```
fsp_err_t R_SDADC_OffsetSet ( adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t const offset )
```

Sets the offset. Offset is applied after stage 1 of the input channel. Offset can only be applied when the channel is configured for differential input. Implements `adc_api_t::offsetSet()`.

Note: The offset is cleared if `adc_api_t::calibrate()` is called. The offset can be re-applied if necessary after the the callback with event `ADC_EVENT_CALIBRATION_COMPLETE` is called.

#### Parameters

[in]	p_ctrl	See p_instance_ctrl in <code>adc_api_t::offsetSet()</code> .
[in]	reg_id	See reg_id in <code>adc_api_t::offsetSet()</code> .
[in]	offset	Must be between -15 and 15, offset (mV) = 10.9376 mV * offset_steps / stage 1 gain.

#### Return values

FSP_SUCCESS	Offset updated successfully.
FSP_ERR_ASSERTION	An input pointer was NULL or an input parameter was invalid.
FSP_ERR_IN_USE	A conversion or calibration is in progress.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_SDADC\_Calibrate()

`fsp_err_t R_SDADC_Calibrate ( adc_ctrl_t *const p_ctrl, void *const p_extend )`

Requires `sdadc_calibrate_args_t` passed to `p_extend`. Calibrates the specified channel. Calibration is not required or supported for single-ended mode. Calibration must be completed for differential mode before using the SDADC. A callback with the event `ADC_EVENT_CALIBRATION_COMPLETE` is called when calibration completes. Implements `adc_api_t::calibrate()`.

During external offset calibration, apply a differential voltage of 0 to `ANSDnP - ANSDnN`, where `n` is the input channel and `ANSDnP` is `OPAMP0` for channel 4 and `ANSDnN` is `OPAMP1` for channel 4. Complete external offset calibration before external gain calibration.

During external gain calibration apply a voltage between `0.4 V / total_gain` and `0.8 V / total_gain`. The differential voltage applied during calibration is corrected to a conversion result of `0x7FFFFFFF`, which is the maximum possible positive differential measurement.

This function clears the offset value. If offset is required after calibration, it must be reapplied after calibration is complete using `adc_api_t::offsetSet`.

#### Return values

FSP_SUCCESS	Calibration began successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_IN_USE	A conversion or calibration is in progress.
FSP_ERR_NOT_OPEN	Instance control block is not open.

### ◆ R\_SDADC\_Close()

`fsp_err_t R_SDADC_Close ( adc_ctrl_t * p_ctrl)`

Stops any scan in progress, disables interrupts, and powers down the SDADC peripheral. Implements `adc_api_t::close()`.

#### Note

*This function delays at least 3 us as required by the SDADC24 stop procedure.*

#### Return values

FSP_SUCCESS	Instance control block closed successfully.
FSP_ERR_ASSERTION	An input pointer was NULL.
FSP_ERR_NOT_OPEN	Instance control block is not open.

## 4.2.48 SD/MMC Host Interface (r\_sdhi)

## Modules

### Functions

fsp_err_t	R_SDHI_Open (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_cfg_t const *const p_cfg)
fsp_err_t	R_SDHI_MediaInit (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_device_t *const p_device)
fsp_err_t	R_SDHI_Read (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t	R_SDHI_Write (sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t	R_SDHI_Readlo (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address)
fsp_err_t	R_SDHI_Writelo (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
fsp_err_t	R_SDHI_ReadloExt (sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
fsp_err_t	R_SDHI_WriteloExt (sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)
fsp_err_t	R_SDHI_IoIntEnable (sdmmc_ctrl_t *const p_api_ctrl, bool enable)
fsp_err_t	R_SDHI_StatusGet (sdmmc_ctrl_t *const p_api_ctrl, sdmmc_status_t *const p_status)
fsp_err_t	R_SDHI_Erase (sdmmc_ctrl_t *const p_api_ctrl, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t	R_SDHI_CallbackSet (sdmmc_ctrl_t *const p_api_ctrl, void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t *const p_callback_memory)
fsp_err_t	R_SDHI_Close (sdmmc_ctrl_t *const p_api_ctrl)

### Detailed Description

Driver for the SD/MMC Host Interface (SDHI) peripheral on RA MCUs. This module implements the

## SD/MMC Interface.

## Overview

### Features

- Supports the following memory devices: SDSC (SD Standard Capacity), SDHC (SD High Capacity), SDXC (SD Extended Capacity) and eMMC (embedded Multi Media Card)
  - Supports reading, writing and erasing SD memory devices
  - Supports 1, 4 or 8-bit data bus (8-bit bus is supported for eMMC only)
  - Supports detection of device write protection (SD cards only)
  - Supports high speed mode
- Automatically configures the clock to the maximum clock rate supported by both host (MCU) and device
- Supports hardware acceleration using DMAC or DTC
- Supports callback notification when an operation completes or an error occurs

## Configuration

### Build Time Configurations for r\_sdhi

The following build time configurations are defined in fsp\_cfg/r\_sdhi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Unaligned Access Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	If enabled, code for supporting buffers that are not aligned on a 4-byte boundary is included in the build. Only disable this if all buffers passed to the driver are 4-byte aligned.
SD Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	If selected code for SD card support is included in the build.
eMMC Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	If selected code for eMMC device support is included in the build.

### Configurations for Driver > Storage > SD/MMC Driver on r\_sdhi

This module can be added to the Stacks tab via New Stack > Driver > Storage > SD/MMC Driver on r\_sdhi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

Name	Name must be a valid C symbol	g_sdmmc0	Module name.
Channel	Value must be a non-negative integer	0	Select the channel.
Bus Width	MCU Specific Options		Select the bus width.
Block Size	Value must be an integer between 1 and 512	512	Select the media block size. Must be 512 for SD cards or eMMC devices. Must be 1-512 for SDIO.
Card Detection	<ul style="list-style-type: none"> <li>• Not Used</li> <li>• CD Pin</li> </ul>	CD Pin	Select the card detection method.
Write Protection	<ul style="list-style-type: none"> <li>• Not Used</li> <li>• WP Pin</li> </ul>	WP Pin	Select whether or not to use the write protect pin. Select Not Used if the MCU or device does not have a write protect pin.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
Access Interrupt Priority	MCU Specific Options		Select the access interrupt priority.
Card Interrupt Priority	MCU Specific Options		Select the card interrupt priority.
DTC Interrupt Priority	MCU Specific Options		Select the DTC interrupt priority.

### Interrupt Configurations:

The following interrupts are required to use the r\_sdhi module:

Using SD/MMC with DTC:

- Access Interrupt
- DTC Interrupt

Using SD/MMC with DMAC:

- Access Interrupt
- DMAC Interrupt (in DMAC instance)

The Card interrupt is optional and only available on MCU packages that have the SDnCD pin (n = channel number).

## Clock Configuration

The SDMMC MCU peripheral (SDHI) uses the PCLKA for its clock source. The SDMMC driver selects the optimal built-in divider based on the PCLKA frequency and the maximum clock rate allowed by the device obtained at media initialization.

## Pin Configuration

The SDMMC driver supports the following pins (n = channel number):

- SDnCLK
- SDnCMD
- SDnDAT0
- SDnDAT1
- SDnDAT2
- SDnDAT3
- SDnDAT4 (not available on all MCUs)
- SDnDAT5 (not available on all MCUs)
- SDnDAT6 (not available on all MCUs)
- SDnDAT7 (not available on all MCUs)
- SDnCD (not available on all MCUs)
- SDnWP

The drive capacity for each pin should be set to "Medium" or "High" for most hardware designs. This can be configured in the **Pins** tab of the RA Configuration editor by selecting the pin under Pin Selection -> Ports.

## Usage Notes

### Card Detection

When Card Detection is configured to "CD Pin" in the RA Configuration editor, interrupt flags are cleared and card detection is enabled during `R_SDHI_Open()`.

`R_SDHI_StatusGet()` can be called to retrieve the current status of the card (including whether a card is present). If the Card Interrupt Priority is enabled, a callback is called when a card is inserted or removed.

If a card is removed and reinserted, `R_SDHI_MediaInit()` must be called before reading from the card or writing to the card.

*Note*

*`R_SDHI_StatusGet()` should be used to initially determine the card state after opening the interface.*

### DMA Request Interrupt Priority

When data transfers are not 4-byte aligned or not a multiple of 4 bytes, a software copy of the block size (up to 512 bytes) is done in the DMA Request interrupt. This blocks all other interrupts that are a lower or equal priority to the access interrupt until the software copy is complete.

### Timing Notes for `R_SDHI_MediaInit`

The `R_SDHI_MediaInit()` API completes the entire device identification and configuration process. This involves several command-response cycles at a bus width of 1 bit and a bus speed of 400 kHz or

less.

## Limitations

Developers should be aware of the following limitations when using the SDHI:

## Blocking Calls

The following functions block execution until the response is received for at least one command:

- [R\\_SDHI\\_MediaInit](#)
- [R\\_SDHI\\_Erase](#)

Once the function returns the status of the operation can be determined via [R\\_SDHI\\_StatusGet](#) or through receipt of a callback.

### Note

*Due to the variability in clocking configurations it is recommended to determine blocking delays experimentally on the target system.*

## Data Alignment and Size

Data transfers should be 4-byte aligned and a multiple of 4 bytes in size whenever possible. This recommendation applies to the `read()`, `write()`, `readloExt()`, and `writeloxExt()` APIs. When data transfers are 4-byte aligned and a multiple of 4-bytes, the `r_sdhi` driver is zero copy and takes full advantage of hardware acceleration by the DMAC or DTC. When data transfers are not 4-byte aligned or not a multiple of 4 bytes an extra CPU interrupt is required for each block transferred and a software copy is used to move data to the destination buffer.

## Examples

### Basic Example

This is a basic example of minimal use of the `r_sdhi` in an application.

```
uint8_t g_dest[SDHI_MAX_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t g_src[SDHI_MAX_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint32_t g_transfer_complete = 0;
void r_sdhi_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < SDHI_MAX_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the SDHI driver. */
    fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);
```

```
    assert(FSP_SUCCESS == err);

    /* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1

    * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */

    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);

    /* Initialize the SD card. This should not be done until the card is plugged in for
SD devices. */

    err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);

    assert(FSP_SUCCESS == err);

    err = R_SDHI_Write(&g_sdmmc0_ctrl, g_src, 3, 1);

    assert(FSP_SUCCESS == err);

while (!g_transfer_complete)
    {
    /* Wait for transfer. */

    }

    err = R_SDHI_Read(&g_sdmmc0_ctrl, g_dest, 3, 1);

    assert(FSP_SUCCESS == err);

while (!g_transfer_complete)
    {
    /* Wait for transfer. */

    }
}

/* The callback is called when a transfer completes. */
void r_sdhi_example_callback (sdmmc_callback_args_t * p_args)
{
    if (SDMMC_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_transfer_complete = 1;
    }
}
```

## Card Detection Example

This is an example of using SDHI when the card may not be plugged in. The card detection interrupt

must be enabled to use this example.

```
bool g_card_inserted = false;
void r_sdhi_card_detect_example (void)
{
    /* Open the SDHI driver. This enables the card detection interrupt. */
    fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Check if card is inserted. */
    sdmmc_status_t status;
    err = R_SDHI_StatusGet(&g_sdmmc0_ctrl, &status);
    assert(FSP_SUCCESS == err);
    if (!status.card_inserted)
    {
        while (!g_card_inserted)
        {
            /* Wait for a card insertion interrupt. */
        }
    }
    /* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1
    * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    /* Initialize the SD card after card insertion is detected. */
    err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);
    assert(FSP_SUCCESS == err);
}
/* The callback is called when a card detection event occurs if the card detection
interrupt is enabled. */
void r_sdhi_card_detect_example_callback (sdmmc_callback_args_t * p_args)
{
    if (SDMMC_EVENT_CARD_INSERTED == p_args->event)
    {
```

```

    g_card_inserted = true;
}
if (SDMMC_EVENT_CARD_REMOVED == p_args->event)
{
    g_card_inserted = false;
}
}

```

## Function Documentation

### ◆ R\_SDHI\_Open()

```
fsp_err_t R_SDHI_Open ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_cfg_t const *const p_cfg )
```

Opens the driver. Resets SDHI, and enables card detection interrupts if card detection is enabled. [R\\_SDHI\\_MediaInit](#) must be called after this function before any other functions can be used.

Implements [sdmmc\\_api\\_t::open\(\)](#).

Example:

```

/* Open the SDHI driver. */
fsp_err_t err = R_SDHI_Open(&g_sdmmc0_ctrl, &g_sdmmc0_cfg);

```

### Return values

FSP_SUCCESS	Module is now open.
FSP_ERR_ASSERTION	Null Pointer or block size is not in the valid range of 1-512. Block size must be 512 bytes for SD cards and eMMC devices. It is configurable for SDIO only.
FSP_ERR_ALREADY_OPEN	Driver has already been opened with this instance of the control structure.
FSP_ERR_IRQ_BSP_DISABLED	Access interrupt is not enabled.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Requested channel does not exist on this MCU.

◆ **R\_SDHI\_MediaInit()**

```
fsp_err_t R_SDHI_MediaInit ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_device_t *const p_device )
```

Initializes the SDHI hardware and completes identification and configuration for the SD or eMMC device. This procedure requires several sequential commands. This function blocks until all identification and configuration commands are complete.

Implements `sdmmc_api_t::mediaInit()`.

Example:

```
/* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1
 * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
/* Initialize the SD card. This should not be done until the card is plugged in for
SD devices. */
err = R_SDHI_MediaInit(&g_sdmmc0_ctrl, NULL);
```

**Return values**

FSP_SUCCESS	Module is now ready for read/write access.
FSP_ERR_ASSERTION	Null Pointer or block size is not in the valid range of 1-512. Block size must be 512 bytes for SD cards and eMMC devices. It is configurable for SDIO only.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_INIT_FAILED	Device was not identified as an SD card, eMMC device, or SDIO card.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_Read()**

```
fsp_err_t R_SDHI_Read ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const
start_sector, uint32_t const sector_count )
```

Reads data from an SD or eMMC device. Up to 0x10000 sectors can be read at a time. Implements `sdmmc_api_t::read()`.

A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the read data is available.

Example:

```
err = R_SDHI_Read(&g_sdmmc0_ctrl, g_dest, 3, 1);
```

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.

◆ **R\_SDHI\_Write()**

```
fsp_err_t R_SDHI_Write ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source, uint32_t
const start_sector, uint32_t const sector_count )
```

Writes data to an SD or eMMC device. Up to 0x10000 sectors can be written at a time. Implements `sdmmc_api_t::write()`.

A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the all data has been written and the device is no longer holding `DAT0` low to indicate it is busy.

Example:

```
err = R_SDHI_Write(&g_sdmmc0_ctrl, g_src, 3, 1);
```

**Return values**

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	Handle or Source address is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_CARD_WRITE_PROTECTED	SD card is Write Protected.
FSP_ERR_WRITE_FAILED	Write operation failed.

◆ **R\_SDHI\_Readlo()**

```
fsp_err_t R_SDHI_Readlo ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address )
```

The Read function reads a one byte register from an SDIO card. Implements `sdmmc_api_t::readlo()`.

This function blocks until the command is sent and the response is received. `p_data` contains the register value read when this function returns.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_UNSUPPORTED	SDIO support disabled in SDHI_CFG_SDIO_SUPPORT_ENABLE.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_Writelo()**

```
fsp_err_t R_SDHI_Writelo ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write )
```

Writes a one byte register to an SDIO card. Implements `sdmmc_api_t::writelo()`.

This function blocks until the command is sent and the response is received. The register has been written when this function returns. If `read_after_write` is true, `p_data` contains the register value read when this function returns.

**Return values**

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	Handle or Source address is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_UNSUPPORTED	SDIO support disabled in SDHI_CFG_SDIO_SUPPORT_ENABLE.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

## ◆ R\_SDHI\_ReadloExt()

```
fsp_err_t R_SDHI_ReadloExt ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const
function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode )
```

Reads data from an SDIO card function. Implements `sdmmc_api_t::readloExt()`.

This function blocks until the command is sent and the response is received. A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the read data is available.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	NULL pointer, or count is not in the valid range of 1-512 for byte mode or 1-511 for block mode.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_WritelExt()**

```
fsp_err_t R_SDHI_WritelExt ( sdmmc_ctrl_t *const p_api_ctrl, uint8_t const *const p_source,
uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode )
```

Writes data to an SDIO card function. Implements `sdmmc_api_t::writelExt()`.

This function blocks until the command is sent and the response is received. A callback with the event `SDMMC_EVENT_TRANSFER_COMPLETE` is called when the all data has been written.

**Return values**

FSP_SUCCESS	Card write finished successfully.
FSP_ERR_ASSERTION	NULL pointer, or count is not in the valid range of 1-512 for byte mode or 1-511 for block mode.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_WRITE_FAILED	Write operation failed.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_IoIntEnable()**

```
fsp_err_t R_SDHI_IoIntEnable ( sdmmc_ctrl_t *const p_api_ctrl, bool enable )
```

Enables or disables the SDIO Interrupt. Implements `sdmmc_api_t::IoIntEnable()`.

**Return values**

FSP_SUCCESS	Card enabled or disabled SDIO interrupts successfully.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_DEVICE_BUSY	Driver is busy with a previous operation.
FSP_ERR_UNSUPPORTED	SDIO support disabled in <code>SDHI_CFG_SDIO_SUPPORT_ENABLE</code> .

◆ **R\_SDHI\_StatusGet()**

```
fsp_err_t R_SDHI_StatusGet ( sdmmc_ctrl_t *const p_api_ctrl, sdmmc_status_t *const p_status )
```

Provides driver status. Implements `sdmmc_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Driver has not been initialized.

◆ **R\_SDHI\_Erase()**

```
fsp_err_t R_SDHI_Erase ( sdmmc_ctrl_t *const p_api_ctrl, uint32_t const start_sector, uint32_t const sector_count )
```

Erases sectors of an SD card or eMMC device. Implements `sdmmc_api_t::erase()`.

This function blocks until the erase command is sent. Poll the status to determine when erase is complete.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	A required pointer is NULL or an argument is invalid.
FSP_ERR_NOT_OPEN	Driver has not been initialized.
FSP_ERR_CARD_NOT_INITIALIZED	Card was unplugged.
FSP_ERR_CARD_WRITE_PROTECTED	SD card is Write Protected.
FSP_ERR_RESPONSE	Device did not respond or responded with an error.
FSP_ERR_DEVICE_BUSY	Device is holding DAT0 low (device is busy) or another operation is ongoing.

◆ **R\_SDHI\_CallbackSet()**

```
fsp_err_t R_SDHI_CallbackSet ( sdmmc_ctrl_t *const p_api_ctrl, void(*) (sdmmc_callback_args_t *)
p_callback, void const *const p_context, sdmmc_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `sdmmc_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **R\_SDHI\_Close()**

```
fsp_err_t R_SDHI_Close ( sdmmc_ctrl_t *const p_api_ctrl)
```

Closes an open SD/MMC device. Implements `sdmmc_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	The parameter <code>p_ctrl</code> is NULL.
FSP_ERR_NOT_OPEN	Driver has not been initialized.

**4.2.49 Segment LCD Controller (r\_slcdc)**

## Modules

**Functions**

```
fsp_err_t R_SLCDC_Open (slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const
p_cfg)
```

```
fsp_err_t R_SLCDC_Write (slcdc_ctrl_t *const p_ctrl, uint8_t const
start_segment, uint8_t const *p_data, uint8_t const segment_count)
```

```
fsp_err_t R_SLCDC_Modify (slcdc_ctrl_t *const p_ctrl, uint8_t const
segment_number, uint8_t const data_mask, uint8_t const data)
```

```
fsp_err_t R_SLCDC_Start (slcdc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SLCDC_Stop (slcdc_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SLCDC_SetContrast (slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t
const contrast)
```

```
fsp_err_t R_SLCDC_SetDisplayArea (slcdc_ctrl_t *const p_ctrl,
slcdc_display_area_t const display_area)
```

```
fsp_err_t R_SLCDC_Close (slcdc_ctrl_t *const p_ctrl)
```

## Detailed Description

Driver for the SLCDC peripheral on RA MCUs. This module implements the [SLCDC Interface](#).

## Overview

The segment LCD controller (SLCDC) utilizes two to four reference voltages to provide AC signals for driving traditional segment LCD panels. Depending on the LCD and MCU package, up to 272 segments can be driven. A built-in link to the RTC allows for up to 152 segments to switch between two patterns at regular intervals. An on-chip boost driver can be used to provide configurable reference voltages up to 5.25V allowing for simple contrast adjustment.

## Features

The SLCDC module can perform the following functions:

- Initialize, start and stop the SLCDC
- Set and modify the output pattern
- Blink between two patterns based on a periodic RTC interrupt signal
- Adjust display contrast (only when using internal voltage boosting)

## Configuration

### Build Time Configurations for r\_slcdc

The following build time configurations are defined in fsp\_cfg/r\_slcdc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Driver > Graphics > Segment LCD Driver on r\_slcdc

This module can be added to the Stacks tab via New Stack > Driver > Graphics > Segment LCD Driver on r\_slcdc.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_slcdc0	Module Name
Clock > Source	<ul style="list-style-type: none"> <li>• LOCO</li> <li>• SOSC</li> <li>• MOSC</li> <li>• HOCO</li> </ul>	HOCO	Select the clock source.
Clock > Divisor	Refer to the RA Configuration tool for available options.	(HOCO/MOSC) 16384	Select the clock divisor.
Output > Bias method	<ul style="list-style-type: none"> <li>• 1/2 bias</li> <li>• 1/3 bias</li> <li>• 1/4 bias</li> </ul>	1/2 bias	Select the bias method. This determines the number of voltage levels used to create the waveforms.
Output > Timeslice	<ul style="list-style-type: none"> <li>• Static</li> <li>• 2-slice</li> <li>• 3-slice</li> <li>• 4-slice</li> <li>• 8-slice</li> </ul>	Static	Select the LCD time slice. The number of slices should match the number of common (COM) pins for your LCD panel.
Output > Waveform	<ul style="list-style-type: none"> <li>• Waveform A</li> <li>• Waveform B</li> </ul>	Waveform A	Select the LCD waveform.
Output > Drive method	<ul style="list-style-type: none"> <li>• External resistance division</li> <li>• Internal voltage boosting</li> <li>• Capacitor split</li> </ul>	External resistance division	Select the LCD drive method.
Output > Default contrast	Refer to the RA Configuration tool for available options.	0	Select the default contrast level.

### Valid Configurations

Though there are many setting combinations only a limited subset are supported by the SLCDC peripheral hardware:

Waveform	Slices	Bias	External Resistance	Internal Boost	Capacitor Split
A	8	1/4	Available	Available	—
A	4	1/3	Available	Available	Available
A	3	1/3	Available	Available	Available
A	3	1/2	Available	—	—
A	2	1/2	Available	—	—
A	Static	—	Available	—	—

B	8	1/4	Available	Available	Available
B	4	1/3	Available	Available	—

## Clock Configuration

The SLCDC clock can be sourced from the main clock (MOSC), sub-clock (SOSC), HOCO or LOCO. Dividers of 4 to 1024 are available for SOSC/LOCO and 256 to 524288 for MOSC/HOCO. It is recommended to adjust the divisor such that the resulting clock provides a frame frequency of 32-128 Hz.

### Note

*Make sure your desired source clock is enabled and running before starting SLCDC output.  
Do not set the segment LCD clock over 512 Hz when using internal boost or capacitor split modes.*

## Pin Configuration

This module controls a variety of pins necessary for segment LCD voltage generation and signal output:

Pin Name	Function	Notes
SEGN	Segment data output	Connect these signals to the segment pins of the LCD.
COMn	Common signal output	Connect these signals to the common pins of the LCD.
VLn	Voltage reference	These pins should be connected to passive components based on the selected drive method (see section 45.7 "Supplying LCD Drive Voltages VL1, VL2, VL3, and VL4" in the RA4M1 User's Manual (R01UH0887EJ0100)).
CAPH, CAPL	Drive voltage generator capacitor	Connect a nonpolar 0.47uF capacitor across these pins when using internal boost or capacitor split modes. This pin is not needed when using resistance division.

## Interrupt Configuration

The SLCDC provides no interrupt signals.

### Note

*Blinking output timing is driven directly from the RTC periodic interrupt. Once the interrupt is enabled setting the display to SLCDC\_DISP\_BLINK will swap between A- and B-pattern each time it occurs. The ELC is not required for this functionality.*

# Usage Notes

## Limitations

Developers should be aware of the following limitations when using the SLCDC:

- Different packages provide different numbers of segment pins. Check the User's Manual for your device to confirm availability and mapping of segment signals.
- When using internal boost mode a delay of 5ms is required between calling R\_SLCDC\_Open and R\_SLCDC\_Start to allow the boost circuit to charge.
- When using the internal boost or capacitor split method do not set the segment LCD clock higher than 512 Hz.

## Examples

### Basic Example

Below is a basic example of minimal use of the SLCDC in an application. The SLCDC driver is initialized, output is started and a pattern is written to the segment registers.

```
void slcdc_init (void)
{
    fsp_err_t err;

    /* Open SLCDC driver */
    err = R_SLCDC_Open(&g_slcdc_ctrl, &g_slcdc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* When using internal boost mode this delay is required to allow the boost circuit
to charge. See RA4M1 User's
    * Manual (R01UH0887EJ0100) 8.2.18 "Segment LCD Source Clock Control Register
(SLDCSCKCR)" for details. */
    R_BSP_SoftwareDelay(5, BSP_DELAY_UNITS_MILLISECONDS);

    /* Start SLCDC output */
    err = R_SLCDC_Start(&g_slcdc_ctrl);
    assert(FSP_SUCCESS == err);

    /* Write pattern to display */
    err = R_SLCDC_Write(&g_slcdc_ctrl, 0, segment_data, NUM_SEGMENTS);
    assert(FSP_SUCCESS == err);
}
```

#### Note

*While the SLCDC is running, pattern data is constantly being output. No latching or buffering is required when writing or reading segment data.*

### Blinking Output

This example demonstrates how to set up blinking output using the RTC periodic interrupt. In this example it is assumed that the SLCDC has already been started.

```
void slcdc_blink (void)
{
    fsp_err_t err;

    /* Open RTC and set time/date */
    err = R_RTC_Open(&r_rtc_ctrl, &r_rtc_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    err = R_RTC_CalendarTimeSet(&r_rtc_ctrl, &g_rtc_time);
    assert(FSP_SUCCESS == err);

    /* Set RTC periodic interrupt to 2 Hz (display blink cycle will be 1 Hz) */
    err = R_RTC_PeriodicIrqRateSet(&r_rtc_ctrl,
    RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_2_SECOND);
    assert(FSP_SUCCESS == err);

    /* Set display to blink */
    err = R_SLCDC_SetDisplayArea(&g_slcdc_ctrl, SLCDC_DISP_BLINK);
    assert(FSP_SUCCESS == err);

    /* Display will now continuously blink */
}
```

## Data Structures

struct [slcdc\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [slcdc\\_instance\\_ctrl\\_t](#)

struct [slcdc\\_instance\\_ctrl\\_t](#)

SLCDC control block. DO NOT INITIALIZE. Initialization occurs when [slcdc\\_api\\_t::open](#) is called

## Function Documentation

◆ **R\_SLCDC\_Open()**

```
fsp_err_t R_SLCDC_Open ( slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg )
```

Opens the SLCDC driver. Implements `slcdc_api_t::open`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block or the configuration structure is NULL.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_UNSUPPORTED	Invalid display mode.

◆ **R\_SLCDC\_Write()**

```
fsp_err_t R_SLCDC_Write ( slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count )
```

Writes a sequence of display data to the segment data registers. Implements `slcdc_api_t::write`.

**Return values**

FSP_SUCCESS	Data was written successfully.
FSP_ERR_ASSERTION	Pointer to the control block or data is NULL.
FSP_ERR_INVALID_ARGUMENT	Segment index is (or will be) out of range.
FSP_ERR_NOT_OPEN	Device is not opened or initialized.

◆ **R\_SLCDC\_Modify()**

```
fsp_err_t R_SLCDC_Modify ( slcdc_ctrl_t *const p_ctrl, uint8_t const segment, uint8_t const data, uint8_t const data_mask )
```

Modifies a single segment register based on a mask and the desired data. Implements `slcdc_api_t::modify`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_INVALID_ARGUMENT	Invalid parameter in the argument.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_Start()**

```
fsp_err_t R_SLCDC_Start ( slcdc_ctrl_t *const p_ctrl)
```

Starts output of LCD signals. Implements `slcdc_api_t::start`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_Stop()**

```
fsp_err_t R_SLCDC_Stop ( slcdc_ctrl_t *const p_ctrl)
```

Stops output of LCD signals. Implements `slcdc_api_t::stop`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

◆ **R\_SLCDC\_SetContrast()**

```
fsp_err_t R_SLCDC_SetContrast ( slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast )
```

Sets contrast to the specified level. Implements `slcdc_api_t::setContrast`.

**Note**

*Contrast can be adjusted when the SLCDC is operating in internal boost mode only. The range of values is 0-5 when 1/4 bias setting is used and 0-15 otherwise. See RA4M1 User's Manual (R01UH0887EJ0100) section 45.2.4 "LCD Boost Level Control Register (VLCD)" for voltage levels at each setting.*

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized
FSP_ERR_UNSUPPORTED	Unsupported operation

◆ **R\_SLCDC\_SetDisplayArea()**

```
fsp_err_t R_SLCDC_SetDisplayArea ( slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area )
```

Sets output to Waveform A, Waveform B or blinking output. Implements `slcdc_api_t::setDisplayArea`.

**Return values**

FSP_SUCCESS	Device was opened successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_UNSUPPORTED	Pattern selection has no effect in 8-time-slice mode.
FSP_ERR_NOT_OPEN	Device is not opened or initialized.

◆ **R\_SLCDC\_Close()**

```
fsp_err_t R_SLCDC_Close ( slcdc_ctrl_t *const p_ctrl)
```

Closes the SLCDC driver. Implements `slcdc_api_t::close`.

**Return values**

FSP_SUCCESS	Device was closed successfully.
FSP_ERR_ASSERTION	Pointer to the control block structure is NULL.
FSP_ERR_NOT_OPEN	Device is not opened or initialized

**4.2.50 Serial Peripheral Interface (r\_spi)**

## Modules

**Functions**

```
fsp_err_t R_SPI_Open (spi_ctrl_t *p_api_ctrl, spi_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SPI_Read (spi_ctrl_t *const p_api_ctrl, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_Write (spi_ctrl_t *const p_api_ctrl, void const *p_src, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_WriteRead (spi_ctrl_t *const p_api_ctrl, void const *p_src, void
*p_dest, uint32_t const length, spi_bit_width_t const bit_width)
```

```
fsp_err_t R_SPI_Close (spi_ctrl_t *const p_api_ctrl)
```

```
fsp_err_t R_SPI_CalculateBitrate (uint32_t bitrate, rspck_div_setting_t
*spck_div)
```

```
fsp_err_t R_SPI_CallbackSet (spi_ctrl_t *const p_api_ctrl,
void(*p_callback)(spi_callback_args_t*), void const *const p_context,
spi_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the SPI peripheral on RA MCUs. This module implements the [SPI Interface](#).

## Overview

### Features

- Standard SPI Modes
  - Master or Slave Mode
  - Clock Polarity (CPOL)
    - CPOL=0 SCLK is low when idle
    - CPOL=1 SCLK is high when idle
  - Clock Phase (CPHA)
    - CPHA=0 Data Sampled on the even edge of SCLK (Master Mode Only)
    - CPHA=1 Data Sampled on the odd edge of SCLK
  - MSB/LSB first
  - 8-Bit, 9-bit, 10-bit, 11-bit, 12-bit, 13-bit, 14-bit, 15-bit, 16-Bit, 20-bit, 24-bit, and 32-Bit data frames
    - Hardware endian swap in 16-Bit and 32-Bit mode
  - 3-Wire (clock synchronous) or 4-Wire (SPI) Mode
- Configurable bitrate
- Supports Full Duplex or Transmit Only Mode
- DTC Support
- Callback Events
  - Transfer Complete
  - RX Overflow Error (The SPI shift register is copied to the data register before previous data was read)
  - TX Underrun Error (No data to load into shift register for transmitting)
  - Parity Error (When parity is enabled and a parity error is detected)

## Configuration

### Build Time Configurations for r\_spi

The following build time configurations are defined in fsp\_cfg/r\_spi\_cfg.h:

--	--	--	--

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Enable Support for using DTC	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	If enabled, DTC instances will be included in the build for both transmission and reception.
Enable Transmitting from RXI Interrupt	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If enabled, all operations will be handled from the RX (receive) interrupt. This setting only provides a performance boost when DTC is not used. In addition, Transmit Only mode is not supported when this configuration is enabled.

### Configurations for Driver > Connectivity > SPI Driver on r\_spi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > SPI Driver on r\_spi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_spi0	Module name.
Channel	Value must be a non-negative integer	0	Select the SPI channel.
Receive Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Transmit Buffer Empty Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Transfer Complete Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Error Interrupt Priority	MCU Specific Options		Select the interrupt priority for all SPI interrupts.
Operating Mode	<ul style="list-style-type: none"> <li>Master</li> <li>Slave</li> </ul>	Master	Select the SPI operating mode.
Clock Phase	<ul style="list-style-type: none"> <li>Data sampling</li> </ul>	Data sampling on odd	Select the clock edge

	<ul style="list-style-type: none"> <li>on odd edge, data variation on even edge</li> <li>• Data sampling on even edge, data variation on odd edge</li> </ul>	edge, data variation on even edge	to sample data.
Clock Polarity	<ul style="list-style-type: none"> <li>• Low when idle</li> <li>• High when idle</li> </ul>	Low when idle	Select clock level when idle.
Mode Fault Error	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	Detect master/slave mode conflicts.
Bit Order	<ul style="list-style-type: none"> <li>• MSB First</li> <li>• LSB First</li> </ul>	MSB First	Select the data bit order.
Callback	Name must be a valid C symbol	spi_callback	A user callback function can be provided. If this callback function is provided, it will be called from the interrupt service routine (ISR).
SPI Mode	<ul style="list-style-type: none"> <li>• SPI Operation</li> <li>• Clock Synchronous Operation</li> </ul>	Clock Synchronous Operation	Select the clock sync mode.
Full or Transmit Only Mode	<ul style="list-style-type: none"> <li>• Full Duplex</li> <li>• Transmit Only</li> </ul>	Full Duplex	Select Full Duplex or Transmit Only Mode.
Slave Select Polarity	<ul style="list-style-type: none"> <li>• Active Low</li> <li>• Active High</li> </ul>	Active Low	Select the slave select active level.
Select SSL(Slave Select)	<ul style="list-style-type: none"> <li>• SSL0</li> <li>• SSL1</li> <li>• SSL2</li> <li>• SSL3</li> </ul>	SSL0	Select which slave to use.
MOSI Idle State	<ul style="list-style-type: none"> <li>• MOSI Idle Value Fixing Disable</li> <li>• MOSI Idle Value Fixing Low</li> <li>• MOSI Idle Value Fixing High</li> </ul>	MOSI Idle Value Fixing Disable	Select the MOSI idle level if MOSI idle is enabled.
Parity Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Odd</li> <li>• Even</li> </ul>	Disabled	Select the parity mode if parity is enabled.
Byte Swapping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Select the byte swap mode for 16/32-Bit Data Frames.
Bitrate	Value must be an integer greater than 0	16000000	Enter the desired bitrate, change the

bitrate to a value supported by MCU. If the requested bitrate cannot be achieved, the settings with the largest possible value that is less than or equal to the requested bitrate is used. The theoretical bitrate is printed in a comment in the generated [spi\\_extended\\_cfg\\_t](#) structure.

## Clock Delay

- SPI\_DELAY\_COU SPI\_DELAY\_COUNT\_1 NT\_1
- SPI\_DELAY\_COU NT\_2
- SPI\_DELAY\_COU NT\_3
- SPI\_DELAY\_COU NT\_4
- SPI\_DELAY\_COU NT\_5
- SPI\_DELAY\_COU NT\_6
- SPI\_DELAY\_COU NT\_7
- SPI\_DELAY\_COU NT\_8

Configure the number of SPI clock cycles before each data frame.

## SSL Negation Delay

- SPI\_DELAY\_COU SPI\_DELAY\_COUNT\_1 NT\_1
- SPI\_DELAY\_COU NT\_2
- SPI\_DELAY\_COU NT\_3
- SPI\_DELAY\_COU NT\_4
- SPI\_DELAY\_COU NT\_5
- SPI\_DELAY\_COU NT\_6
- SPI\_DELAY\_COU NT\_7
- SPI\_DELAY\_COU NT\_8

Configure the number of SPI clock cycles after each data frame.

## Next Access Delay

- SPI\_DELAY\_COU SPI\_DELAY\_COUNT\_1 NT\_1
- SPI\_DELAY\_COU NT\_2
- SPI\_DELAY\_COU NT\_3
- SPI\_DELAY\_COU

Configure the number of SPI clock cycles between each data frame.

- NT\_4
- SPI\_DELAY\_COU
- NT\_5
- SPI\_DELAY\_COU
- NT\_6
- SPI\_DELAY\_COU
- NT\_7
- SPI\_DELAY\_COU
- NT\_8

## Clock Configuration

The clock for this module is derived from the following peripheral clock for each MCU group:

MCU Group	Peripheral Clock
RA2A1	PCLKB
RA2E1	PCLKB
RA2L1	PCLKB
RA4M1	PCLKA
RA4M2	PCLKA
RA4M3	PCLKA
RA4W1	PCLKA
RA6M1	PCLKA
RA6M2	PCLKA
RA6M3	PCLKA
RA6M4	PCLKA
RA6M5	PCLKA
RA6T1	PCLKA

## Pin Configuration

This module uses MOSI, MISO, RSPCK, and SSL pins to communicate with on board devices.

### Note

*At high bitrates, it might be necessary to configure the pins with `IOPORT_CFG_DRIVE_HIGH`.*

## Usage Notes

### Performance

At high bitrates, interrupts may not be able to service transfers fast enough. In master mode this means there will be a delay between each data frame. In slave mode this could result in TX Underrun and RX Overflow errors.

In order to improve performance at high bitrates, it is recommended that the instance be configured

to service transfers using the DTC.

Another way to improve performance is to transfer the data in 16/32 bit wide data frames when possible. A typical use-case where this is possible is when reading/writing to a block device.

### Transmit From RXI Interrupt

After every data frame the SPI peripheral generates a transmit buffer empty interrupt and a receive buffer full interrupt. It is possible to configure the driver to handle transmit buffer empty interrupts in the receive buffer full isr. This only improves performance when the DTC is not being used.

#### Note

*Configuring the module to use RX DTC instance without also providing a TX DTC instance results in an invalid configuration when RXI transmit is enabled.*

*Transmit Only mode is not supported when Transmit from RXI is enabled.*

### Clock Auto-Stopping

In master mode, if the Receive Buffer Full Interrupts are not handled fast enough, instead of generating a RX Overflow error, the last clock cycle will be stretched until the receive buffer is read.

### Parity Mode

When parity mode is configured, the LSB of each data frame is used as a parity bit. When odd parity is selected, the LSB is set such that there are an odd number of ones in the data frame. When even parity is selected, the LSB is set such that there are an even number of ones in the data frame.

### Limitations

Developers should be aware of the following limitations when using the SPI:

- In master mode, the driver will only configure 4-Wire mode if the device supports SSL Level Keeping (SSLKP bit in SPCMD0) and will return FSP\_ERR\_UNSUPPORTED if configured for 4-Wire mode on devices without SSL Level Keeping. Without SSL Level Keeping, the SSL pin is toggled after every data frame. In most cases this is not desirable behavior so it is recommended that the SSL pin be driven in software if SSL Level Keeping is not present on the device.
- In order to use CPHA=0 setting in slave mode, the master must toggle the SSL pin after every data frame (Even if the device supports SSL Level Keeping). Because of this hardware limitation, the module will return FSP\_ERR\_UNSUPPORTED when it is configured to use CPHA=0 setting in slave mode.
- The module does not support communicating with multiple slaves using different SSL pins. In order to achieve this, the module must either be closed and re-opened to change the SSL pin or drive SSL in software. It is recommended that SSL be driven in software when controlling multiple slave devices.
- The SPI peripheral has a minimum 3 SPI CLK delay between each data frame.
- The behavior for Byte Swap operation is not guaranteed for data frames other than 8-bit, 16-bit and 32bit.

## Examples

### Basic Example

This is a basic example of minimal use of the SPI in an application.

```
static volatile bool g_transfer_complete = false;
void spi_basic_example (void)
{
    uint8_t tx_buffer[TRANSFER_SIZE];
    uint8_t rx_buffer[TRANSFER_SIZE];
    fsp_err_t err = FSP_SUCCESS;
    /* Initialize the SPI module. */
    err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Start a write/read transfer */
    err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer, TRANSFER_SIZE,
SPI_BIT_WIDTH_8_BITS);
    assert(FSP_SUCCESS == err);
    /* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
    while (false == g_transfer_complete)
    {
        ;
    }
}
static void r_spi_callback (spi_callback_args_t * p_args)
{
    if (SPI_EVENT_TRANSFER_COMPLETE == p_args->event)
    {
        g_transfer_complete = true;
    }
}
```

## Driving Software Slave Select Line

This is an example of communicating with multiple slave devices by asserting SSL in software.

```
void spi_software_ssl_example (void)
{
    uint8_t tx_buffer[TRANSFER_SIZE];
```

```
uint8_t rx_buffer[TRANSFER_SIZE];
/* Configure Slave Select Line 1 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
/* Configure Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
fsp_err_t err = FSP_SUCCESS;
/* Initialize the SPI module. */
err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Assert Slave Select Line 1 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_LOW);
/* Start a write/read transfer */
g_transfer_complete = false;
err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer,
TRANSFER_SIZE, SPI_BIT_WIDTH_8_BITS);
assert(FSP_SUCCESS == err);
/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
while (false == g_transfer_complete)
{
    ;
}
/* De-assert Slave Select Line 1 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_1, BSP_IO_LEVEL_HIGH);
/* Wait for minimum time required between transfers. */
R_BSP_SoftwareDelay(SSL_NEXT_ACCESS_DELAY, BSP_DELAY_UNITS_MICROSECONDS);
/* Assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_LOW);
/* Start a write/read transfer */
g_transfer_complete = false;
err = R_SPI_WriteRead(&g_spi_ctrl, tx_buffer, rx_buffer,
TRANSFER_SIZE, SPI_BIT_WIDTH_8_BITS);
assert(FSP_SUCCESS == err);
/* Wait for SPI_EVENT_TRANSFER_COMPLETE callback event. */
```

```
while (false == g_transfer_complete)
{
    ;
}

/* De-assert Slave Select Line 2 */
R_BSP_PinWrite(SLAVE_SELECT_LINE_2, BSP_IO_LEVEL_HIGH);
}
```

## Configuring the SPI Clock Divider Registers

This example demonstrates how to set the SPI clock divisors at runtime.

```
void spi_bitrate_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    g_spi_cfg.p_extend = &g_spi_extended_cfg;
    /* Configure SPI Clock divider to achieve largest bitrate less than or equal to the
desired bitrate. */
    err = R_SPI_CalculateBitrate(BITRATE, &(g_spi_extended_cfg.spck_div));
    assert(FSP_SUCCESS == err);
    /* Initialize the SPI module. */
    err = R_SPI_Open(&g_spi_ctrl, &g_spi_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
}
```

## Data Structures

struct [rspck\\_div\\_setting\\_t](#)

struct [spi\\_extended\\_cfg\\_t](#)

struct [spi\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [spi\\_ssl\\_mode\\_t](#)

enum [spi\\_communication\\_t](#)

enum [spi\\_ssl\\_polarity\\_t](#)

enum [spi\\_ssl\\_select\\_t](#)enum [spi\\_mosi\\_idle\\_value\\_fixing\\_t](#)enum [spi\\_parity\\_t](#)enum [spi\\_byte\\_swap\\_t](#)enum [spi\\_delay\\_count\\_t](#)

## Data Structure Documentation

### ◆ [rspck\\_div\\_setting\\_t](#)

struct <a href="#">rspck_div_setting_t</a>		
SPI Clock Divider settings.		
Data Fields		
<a href="#">uint8_t</a>	spbr	SPBR register setting.
<a href="#">uint8_t</a>	brdv: 2	BRDV setting in SPCMD0.

### ◆ [spi\\_extended\\_cfg\\_t](#)

struct <a href="#">spi_extended_cfg_t</a>		
Extended SPI interface configuration		
Data Fields		
<a href="#">spi_ssl_mode_t</a>	spi_clksyn	Select spi or clock syn mode operation.
<a href="#">spi_communication_t</a>	spi_comm	Select full-duplex or transmit-only communication.
<a href="#">spi_ssl_polarity_t</a>	ssl_polarity	Select SSLn signal polarity.
<a href="#">spi_ssl_select_t</a>	ssl_select	Select which slave to use: 0-SSL0, 1-SSL1, 2-SSL2, 3-SSL3.
<a href="#">spi_mosi_idle_value_fixing_t</a>	mosi_idle	Select MOSI idle fixed value and selection.
<a href="#">spi_parity_t</a>	parity	Select parity and enable/disable parity.
<a href="#">spi_byte_swap_t</a>	byte_swap	Select byte swap mode.
<a href="#">rspck_div_setting_t</a>	spck_div	Register values for configuring the SPI Clock Divider.
<a href="#">spi_delay_count_t</a>	spck_delay	SPI Clock Delay Register Setting.
<a href="#">spi_delay_count_t</a>	ssl_negation_delay	SPI Slave Select Negation Delay Register Setting.

<code>spi_delay_count_t</code>	<code>next_access_delay</code>	SPI Next-Access Delay Register Setting.
--------------------------------	--------------------------------	---

◆ `spi_instance_ctrl_t`

struct <code>spi_instance_ctrl_t</code>	
Channel control block. DO NOT INITIALIZE. Initialization occurs when <code>spi_api_t::open</code> is called.	
<b>Data Fields</b>	
<code>uint32_t</code>	<code>open</code>
	Indicates whether the <code>open()</code> API has been successfully called.
<code>spi_cfg_t const *</code>	<code>p_cfg</code>
	Pointer to instance configuration.
<code>R_SPI0_Type *</code>	<code>p_regs</code>
	Base register for this channel.
<code>void const *</code>	<code>p_tx_data</code>
	Buffer to transmit.
<code>void *</code>	<code>p_rx_data</code>
	Buffer to receive.
<code>uint32_t</code>	<code>tx_count</code>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)
<code>uint32_t</code>	<code>rx_count</code>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)
<code>uint32_t</code>	<code>count</code>
	Number of Data Frames to transfer (8-bit, 16-bit, 32-bit)

<code>spi_bit_width_t</code>	<code>bit_width</code>
	Bits per Data frame (8-bit, 16-bit, 32-bit)

## Enumeration Type Documentation

### ◆ `spi_ssl_mode_t`

enum <code>spi_ssl_mode_t</code>	
3-Wire or 4-Wire mode.	
Enumerator	
<code>SPI_SSL_MODE_SPI</code>	SPI operation (4-wire method)
<code>SPI_SSL_MODE_CLK_SYN</code>	Clock Synchronous operation (3-wire method)

### ◆ `spi_communication_t`

enum <code>spi_communication_t</code>	
Transmit Only (Half Duplex), or Full Duplex.	
Enumerator	
<code>SPI_COMMUNICATION_FULL_DUPLEX</code>	Full-Duplex synchronous serial communication.
<code>SPI_COMMUNICATION_TRANSMIT_ONLY</code>	Transit only serial communication.

### ◆ `spi_ssl_polarity_t`

enum <code>spi_ssl_polarity_t</code>	
Slave Select Polarity.	
Enumerator	
<code>SPI_SSPL_LOW</code>	SSLP signal polarity active low.
<code>SPI_SSPL_HIGH</code>	SSLP signal polarity active high.

## ◆ spi\_ssl\_select\_t

enum spi_ssl_select_t	
The Slave Select Line	
Enumerator	
SPI_SSL_SELECT_SSL0	Select SSL0.
SPI_SSL_SELECT_SSL1	Select SSL1.
SPI_SSL_SELECT_SSL2	Select SSL2.
SPI_SSL_SELECT_SSL3	Select SSL3.

## ◆ spi\_mosi\_idle\_value\_fixing\_t

enum spi_mosi_idle_value_fixing_t	
MOSI Idle Behavior.	
Enumerator	
SPI_MOSI_IDLE_VALUE_FIXING_DISABLE	MOSI output value=value set in MOIFV bit.
SPI_MOSI_IDLE_VALUE_FIXING_LOW	MOSIn level low during MOSI idling.
SPI_MOSI_IDLE_VALUE_FIXING_HIGH	MOSIn level high during MOSI idling.

## ◆ spi\_parity\_t

enum spi_parity_t	
Parity Mode	
Enumerator	
SPI_PARITY_MODE_DISABLE	Disable parity.
SPI_PARITY_MODE_ODD	Select even parity.
SPI_PARITY_MODE_EVEN	Select odd parity.

## ◆ spi\_byte\_swap\_t

enum spi_byte_swap_t	
Byte Swapping Enable/Disable.	
Enumerator	
SPI_BYTE_SWAP_DISABLE	Disable Byte swapping for 16/32-Bit transfers.
SPI_BYTE_SWAP_ENABLE	Enable Byte swapping for 16/32-Bit transfers.

## ◆ spi\_delay\_count\_t

enum spi_delay_count_t	
Delay count for SPI delay settings.	
Enumerator	
SPI_DELAY_COUNT_1	Set RSPCK delay count to 1 RSPCK.
SPI_DELAY_COUNT_2	Set RSPCK delay count to 2 RSPCK.
SPI_DELAY_COUNT_3	Set RSPCK delay count to 3 RSPCK.
SPI_DELAY_COUNT_4	Set RSPCK delay count to 4 RSPCK.
SPI_DELAY_COUNT_5	Set RSPCK delay count to 5 RSPCK.
SPI_DELAY_COUNT_6	Set RSPCK delay count to 6 RSPCK.
SPI_DELAY_COUNT_7	Set RSPCK delay count to 7 RSPCK.
SPI_DELAY_COUNT_8	Set RSPCK delay count to 8 RSPCK.

## Function Documentation

◆ **R\_SPI\_Open()**

```
fsp_err_t R_SPI_Open ( spi_ctrl_t * p_api_ctrl, spi_cfg_t const *const p_cfg )
```

This function initializes a channel for SPI communication mode. Implements [spi\\_api\\_t::open](#).

This function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Configures the peripheral registers according to the configuration.
- Initialize the control structure for use in other [SPI Interface](#) functions.

**Return values**

FSP_SUCCESS	Channel initialized successfully.
FSP_ERR_ALREADY_OPEN	Instance was already initialized.
FSP_ERR_ASSERTION	An invalid argument was given in the configuration structure.
FSP_ERR_UNSUPPORTED	A requested setting is not possible on this device with the current build configuration.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	The channel number is invalid.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls: [transfer\\_api\\_t::open](#)

*Note*

*This function is reentrant.*

◆ **R\_SPI\_Read()**

```
fsp_err_t R_SPI_Read ( spi_ctrl_t *const p_api_ctrl, void * p_dest, uint32_t const length, spi_bit_width_t const bit_width )
```

This function receives data from a SPI device. Implements [spi\\_api\\_t::read](#).

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI read operation.

**Return values**

FSP_SUCCESS	Read operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control or destination parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open channel first.
FSP_ERR_IN_USE	A transfer is already in progress.

◆ **R\_SPI\_Write()**

```
fsp_err_t R_SPI_Write ( spi_ctrl_t *const p_api_ctrl, void const * p_src, uint32_t const length,
spi_bit_width_t const bit_width )
```

This function transmits data to a SPI device using the TX Only Communications Operation Mode. Implements `spi_api_t::write`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI write operation.

**Return values**

FSP_SUCCESS	Write operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control or source parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_IN_USE	A transfer is already in progress.

◆ **R\_SPI\_WriteRead()**

```
fsp_err_t R_SPI_WriteRead ( spi_ctrl_t *const p_api_ctrl, void const * p_src, void * p_dest, uint32_t
const length, spi_bit_width_t const bit_width )
```

This function simultaneously transmits and receive data. Implements `spi_api_t::writeRead`.

The function performs the following tasks:

- Performs parameter checking and processes error conditions.
- Sets up the instance to complete a SPI writeRead operation.

**Return values**

FSP_SUCCESS	Write operation successfully completed.
FSP_ERR_ASSERTION	NULL pointer to control, source or destination parameters or transfer length is zero.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.
FSP_ERR_IN_USE	A transfer is already in progress.

◆ **R\_SPI\_Close()**

```
fsp_err_t R_SPI_Close ( spi_ctrl_t *const p_api_ctrl)
```

This function manages the closing of a channel by the following task. Implements `spi_api_t::close`.

Disables SPI operations by disabling the SPI bus.

- Disables the SPI peripheral.
- Disables all the associated interrupts.
- Update control structure so it will not work with [SPI Interface](#) functions.

**Return values**

FSP_SUCCESS	Channel successfully closed.
FSP_ERR_ASSERTION	A required pointer argument is NULL.
FSP_ERR_NOT_OPEN	The channel has not been opened. Open the channel first.

◆ **R\_SPI\_CalculateBitrate()**

```
fsp_err_t R_SPI_CalculateBitrate ( uint32_t bitrate, rspck_div_setting_t * spck_div )
```

Calculates the SPBR register value and the BRDV bits for a desired bitrate. If the desired bitrate is faster than the maximum bitrate, than the bitrate is set to the maximum bitrate. If the desired bitrate is slower than the minimum bitrate, than an error is returned.

**Parameters**

[in]	bitrate	Desired bitrate
[out]	spck_div	Memory location to store bitrate register settings.

**Return values**

FSP_SUCCESS	Valid spbr and brdv values were calculated
FSP_ERR_UNSUPPORTED	Bitrate is not achievable

◆ **R\_SPI\_CallbackSet()**

```
fsp_err_t R_SPI_CallbackSet ( spi_ctrl_t *const p_api_ctrl, void(*) (spi_callback_args_t *) p_callback,
void const *const p_context, spi_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `spi_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.51 Serial Sound Interface (r\_ssi)**

## Modules

**Functions**

```
fsp_err_t R_SSI_Open (i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg)
```

```
fsp_err_t R_SSI_Stop (i2s_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SSI_StatusGet (i2s_ctrl_t *const p_ctrl, i2s_status_t *const
p_status)
```

```
fsp_err_t R_SSI_Write (i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t
const bytes)
```

```
fsp_err_t R_SSI_Read (i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t
const bytes)
```

```
fsp_err_t R_SSI_WriteRead (i2s_ctrl_t *const p_ctrl, void const *const p_src,
void *const p_dest, uint32_t const bytes)
```

```
fsp_err_t R_SSI_Mute (i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable)
```

```
fsp_err_t R_SSI_Close (i2s_ctrl_t *const p_ctrl)
```

```
fsp_err_t R_SSI_CallbackSet (i2s_ctrl_t *const p_api_ctrl,
```

```
void(*p_callback)(i2s_callback_args_t*), void const *const p_context,
i2s_callback_args_t *const p_callback_memory)
```

## Detailed Description

Driver for the SSIE peripheral on RA MCUs. This module implements the [I2S Interface](#).

## Overview

### Features

The SSI module supports the following features:

- Transmission and reception of uncompressed audio data using the standard I2S protocol in master mode
- Full-duplex I2S communication (channel 0 only)
- Integration with the DTC transfer module
- Internal connection to GPT timer output to generate the audio clock
- Callback function notification when all data is loaded into the SSI FIFO

## Configuration

### Build Time Configurations for r\_ssi

The following build time configurations are defined in fsp\_cfg/r\_ssi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DTC Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	If code for DTC transfer support is included in the build.

### Configurations for Driver > Connectivity > I2S Driver on r\_ssi

This module can be added to the Stacks tab via New Stack > Driver > Connectivity > I2S Driver on r\_ssi. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_i2s0	Module name.
Channel	Value must be an integer between 0 and 1	0	Specify the I2S channel.
Bit Depth	<ul style="list-style-type: none"> <li>• 8 Bits</li> </ul>	16 Bits	Select the bit depth of

	<ul style="list-style-type: none"> <li>• 16 Bits</li> <li>• 18 Bits</li> <li>• 20 Bits</li> <li>• 22 Bits</li> <li>• 24 Bits</li> <li>• 32 Bits</li> </ul>		one sample of audio data.
Word Length	<ul style="list-style-type: none"> <li>• 8 Bits</li> <li>• 16 Bits</li> <li>• 24 Bits</li> <li>• 32 Bits</li> <li>• 48 Bits</li> <li>• 64 Bits</li> <li>• 128 Bits</li> <li>• 256 Bits</li> </ul>	16 Bits	Select the word length of audio data. Must be at least as large as Data bits.
WS Continue Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable WS continue mode to output the word select (WS) pin even when transmission is idle.
Bit Clock Source	<ul style="list-style-type: none"> <li>• External AUDIO_CLK</li> <li>• Internal AUDIO_CLK</li> </ul>	External AUDIO_CLK	Select External AUDIO_CLK for external signal to AUDIO_CLK input pin or Internal AUDIO_CLK for internal connection to MCU specific GPT channel. Please refer to the hardware manual for which GPT channel is connected to the internal signal
Bit Clock Divider	Refer to the RA Configuration tool for available options.	Audio Clock / 1	Select divider used to generate bit clock from audio clock.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called from all three interrupt service routines (ISR).
Transmit Interrupt Priority	MCU Specific Options		Select the transmit interrupt priority.
Receive Interrupt Priority	MCU Specific Options		Select the receive interrupt priority.
Idle/Error Interrupt Priority	MCU Specific Options		Select the Idle/Error interrupt priority.

## Clock Configuration

The SSI peripheral runs on PCLKB. The PCLKB frequency can be configured on the **Clocks** tab of the RA Configuration editor. The SSI audio clock can optionally be supplied from an external source through the AUDIO\_CLK pin in master mode.

## Pin Configuration

The SSI uses the following pins:

- AUDIO\_CLK (optional, master mode only): The AUDIO\_CLK pin is used to supply the audio clock from an external source.
- SSIBCKn: Bit clock pin for channel n
- SSILRCKn/SSIFSn: Channel selection pin for channel n
- SSIRXD0: Reception pin for channel 0
- SSITXD0: Transmission pin for channel 0
- SSIDATA1: Transmission or reception pin for channel 1

## Usage Notes

### SSI Frames

An SSI frame is 2 samples worth of data. The frame boundary (end of previous frame, start of next frame) is on the falling edge of the SSILRCKn signal.

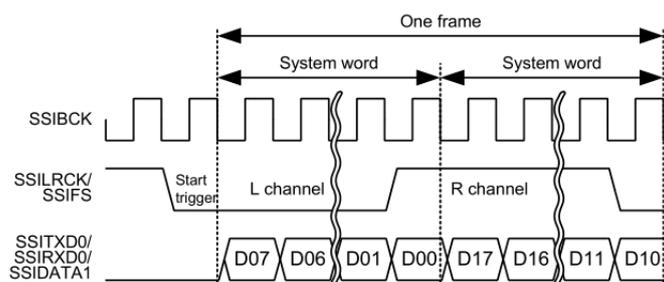


Figure 167: SSI Frame Diagram (8-bit word, 8-bit samples)

### Note

*If the word length is longer than the sample bit depth, padding bits (0) will be added after the sample.*

### Audio Data

Only uncompressed PCM data is supported.

Data arrays have the following size, alignment, and length based on the "Bit Depth" setting:

Bit Depth	Array Data Type	Required Alignment	Required Length (bytes)
8 Bits	8-bit integer	1 byte alignment	Multiple of 2
16 Bits	16-bit integer	2 byte alignment	Multiple of 4
18 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8

20 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
22 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
24 Bits	32-bit integer, right justified	4 byte alignment	Multiple of 8
32 Bits	32-bit integer	4 byte alignment	Multiple of 8

*Note*

*The length of the array must be a multiple of 2 when the data type is the recommended data type. The 2 represents the frame size (left and right channel) of I2S communication. The SSIE peripheral does not support odd read/write lengths in I2S mode.*

**Audio Clock**

The audio clock is only required for master mode.

**Audio Clock Frequency**

The bit clock frequency is the product of the sampling frequency and channels and bits per system word:

$$\text{bit\_clock (Hz)} = \text{sampling\_frequency (Hz)} * \text{channels} * \text{system\_word\_bits}$$

I2S data always has 2 channels.

For example, the bit clock for transmitting 2 channels of 16-bit data (using a 16-bit system word) at 44100 Hz would be:

$$44100 * 2 * 16 = 1,411,200 \text{ Hz}$$

The audio clock frequency is used to generate the bit clock frequency. It must be a multiple of the bit clock frequency. Refer to the Bit Clock Divider configuration for divider options. The input audio clock frequency must be:

$$\text{audio\_clock (Hz)} = \text{desired\_bit\_clock (Hz)} * \text{bit\_clock\_divider}$$

To get a bit clock of 1.4 MHz from an audio clock of 2.8 MHz, select the divider Audio Clock / 2.

**Audio Clock Source**

The audio clock source can come from:

- An external source input to the AUDIO\_CLK pin
- An internal connection to the GPT timer output

*Note*

*When using the internal GPT timer output, Pin Output Support must be Enabled, and GTIOCA Output Enabled must be True.*

*See the SSIE section in the MCU hardware manual for information about which GPT channel may be used.*

**Limitations**

Developers should be aware of the following limitations when using the SSI:

- When using channel 1, full duplex communication is not possible. Only transmission or reception is possible.
- SSI must go idle before changing the communication mode (between read only, write only, and full duplex)

## Examples

### Basic Example

This is a basic example of minimal use of the SSI in an application.

```
#define SSI_EXAMPLE_SAMPLES_TO_TRANSFER (1024)
#define SSI_EXAMPLE_TONE_FREQUENCY_HZ (800)
int16_t g_src[SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
int16_t g_dest[SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
void ssi_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Create a stereo sine wave. Using formula sample = sin(2 * pi * tone_frequency * t
    / sampling_frequency) */

    uint32_t freq = SSI_EXAMPLE_TONE_FREQUENCY_HZ;
    for (uint32_t t = 0; t < SSI_EXAMPLE_SAMPLES_TO_TRANSFER / 2; t += 1)
    {
        float input = (((float) (freq * t)) * (M_TWOPI)) /
        SSI_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ;

        g_src[2 * t] = (int16_t) ((INT16_MAX * sinf(input)));
        g_src[2 * t + 1] = (int16_t) ((INT16_MAX * sinf(input)));
    }

    /* Initialize the module. */
    err = R_SSI_Open(&g_i2s_ctrl, &g_i2s_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Transfer data. */
    (void) R_SSI_WriteRead(&g_i2s_ctrl,
                          (uint8_t *) &g_src[0],
                          (uint8_t *) &g_dest[0],
                          SSI_EXAMPLE_SAMPLES_TO_TRANSFER * sizeof(int16_t));
}
```

```
}
```

## Streaming Example

This is an example of using SSI to stream audio data. This application uses a double buffer to store PCM sine wave data. It starts transmitting in the main loop, then loads the next buffer if it is ready in the callback. If the next buffer is not ready, a flag is set in the callback so the application knows to restart transmission in the main loop.

This example also checks the return code of `R_SSI_Write()` because `R_SSI_Write()` can return an error if a transmit overflow occurs before the FIFO is reloaded. If a transmit overflow occurs before the FIFO is reloaded, the SSI will be stopped in the error interrupt, and it cannot be restarted until the `I2S_EVENT_IDLE` callback is received.

```
#define SSI_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ (22050)
#define SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK (1024)
#define SSI_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ (800)
int16_t      g_stream_src[2][SSI_EXAMPLE_SAMPLES_TO_TRANSFER];
uint32_t     g_buffer_index      = 0;
volatile bool g_send_data_in_main_loop = true;
volatile bool g_data_ready = false;
/* Example callback called when SSI is ready for more data. */
void ssi_example_callback (i2s_callback_args_t * p_args)
{
    /* Reload the FIFO if we hit the transmit watermark or restart transmission if the
    SSI is idle because it was
    * stopped after a transmit FIFO overflow. */
    if ((I2S_EVENT_TX_EMPTY == p_args->event) || (I2S_EVENT_IDLE == p_args->event))
    {
        if (g_data_ready)
        {
            /* Reload FIFO and handle errors. */
            ssi_example_write();
        }
        else
        {
            /* Data was not ready yet, send it in the main loop. */
            g_send_data_in_main_loop = true;
        }
    }
}
```

```
    }
}

/* Load the transmit FIFO and check for error conditions. */
void ssi_example_write (void)
{
    /* Transfer data. This call is non-blocking. */
    fsp_err_t err = R_SSI_Write(&g_i2s_ctrl,
                               (uint8_t *) &g_stream_src[g_buffer_index][0],
                               SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK * sizeof
(int16_t));
    if (FSP_SUCCESS == err)
    {
        /* Switch the buffer after data is sent. */
        g_buffer_index = !g_buffer_index;
        /* Allow loop to calculate next buffer only if transmission was successful. */
        g_data_ready = false;
    }
    else
    {
        /* Getting here most likely means a transmit overflow occurred before the FIFO could
be reloaded. The
        * application must wait until the SSI is idle, then restart transmission. In this
example, the idle
        * callback transmits data or resets the flag g_send_data_in_main_loop. */
    }
}

/* Calculate samples. This example is just a sine wave. For this type of data, it
would be better to calculate
* one period and loop it. This example should be updated for the audio data used by
the application. */
void ssi_example_calculate_samples (uint32_t buffer_index)
{
    static uint32_t t = 0U;
```

```
/* Create a stereo sine wave. Using formula sample = sin(2 * pi * tone_frequency * t
/ sampling_frequency) */
uint32_t freq = SSI_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ;
for (uint32_t i = 0; i < SSI_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK / 2; i += 1)
{
float input = (((float) (freq * t)) * M_TWOPI) /
SSI_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ;

t++;

/* Store sample twice, once for left channel and once for right channel. */
int16_t sample = (int16_t) ((INT16_MAX * sinf(input)));
g_stream_src[buffer_index][2 * i] = sample;
g_stream_src[buffer_index][2 * i + 1] = sample;
}

/* Data is ready to be sent in the interrupt. */
g_data_ready = true;
}

void ssi_streaming_example (void)
{
fsp_err_t err = FSP_SUCCESS;
/* Initialize the module. */
err = R_SSI_Open(&g_i2s_ctrl, &g_i2s_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
while (true)
{
/* Prepare data in a buffer that is not currently used for transmission. */
ssi_example_calculate_samples(g_buffer_index);
/* Send data in main loop the first time, and if it was not ready in the interrupt.
*/
if (g_send_data_in_main_loop)
{
/* Clear flag. */
g_send_data_in_main_loop = false;
/* Reload FIFO and handle errors. */
```

```

        ssi_example_write();
    }

    /* If the next buffer is ready, wait for the data to be sent in the interrupt. */
    while (g_data_ready)
    {
        /* Do nothing. */
    }
}

```

## Data Structures

struct [ssi\\_instance\\_ctrl\\_t](#)

struct [ssi\\_extended\\_cfg\\_t](#)

## Enumerations

enum [ssi\\_audio\\_clock\\_t](#)

enum [ssi\\_clock\\_div\\_t](#)

## Data Structure Documentation

### ◆ [ssi\\_instance\\_ctrl\\_t](#)

struct [ssi\\_instance\\_ctrl\\_t](#)

Channel instance control block. DO NOT INITIALIZE. Initialization occurs when [i2s\\_api\\_t::open](#) is called.

### ◆ [ssi\\_extended\\_cfg\\_t](#)

struct [ssi\\_extended\\_cfg\\_t](#)

SSI configuration extension. This extension is optional.

#### Data Fields

<a href="#">ssi_audio_clock_t</a>	<a href="#">audio_clock</a>	Audio clock source, default is <a href="#">SSI_AUDIO_CLOCK_EXTERNAL</a> .
<a href="#">ssi_clock_div_t</a>	<a href="#">bit_clock_div</a>	Select bit clock division ratio.

## Enumeration Type Documentation

◆ **ssi\_audio\_clock\_t**

enum <code>ssi_audio_clock_t</code>	
Audio clock source.	
Enumerator	
<code>SSI_AUDIO_CLOCK_EXTERNAL</code>	Audio clock source is the AUDIO_CLK input pin.
<code>SSI_AUDIO_CLOCK_INTERNAL</code>	Audio clock source is internal connection to a MCU specific GPT channel output.

◆ **ssi\_clock\_div\_t**

enum <code>ssi_clock_div_t</code>	
Bit clock division ratio. Bit clock frequency = audio clock frequency / bit clock division ratio.	
Enumerator	
<code>SSI_CLOCK_DIV_1</code>	Clock divisor 1.
<code>SSI_CLOCK_DIV_2</code>	Clock divisor 2.
<code>SSI_CLOCK_DIV_4</code>	Clock divisor 4.
<code>SSI_CLOCK_DIV_6</code>	Clock divisor 6.
<code>SSI_CLOCK_DIV_8</code>	Clock divisor 8.
<code>SSI_CLOCK_DIV_12</code>	Clock divisor 12.
<code>SSI_CLOCK_DIV_16</code>	Clock divisor 16.
<code>SSI_CLOCK_DIV_24</code>	Clock divisor 24.
<code>SSI_CLOCK_DIV_32</code>	Clock divisor 32.
<code>SSI_CLOCK_DIV_48</code>	Clock divisor 48.
<code>SSI_CLOCK_DIV_64</code>	Clock divisor 64.
<code>SSI_CLOCK_DIV_96</code>	Clock divisor 96.
<code>SSI_CLOCK_DIV_128</code>	Clock divisor 128.

**Function Documentation**

◆ **R\_SSI\_Open()**

```
fsp_err_t R_SSI_Open ( i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg )
```

Opens the SSI. Implements [i2s\\_api\\_t::open](#).

This function sets this clock divisor and the configurations specified in [i2s\\_cfg\\_t](#). It also opens the timer and transfer instances if they are provided.

**Return values**

FSP_SUCCESS	Ready for I2S communication.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_cfg is null.
FSP_ERR_ALREADY_OPEN	The control block has already been opened.
FSP_ERR_IP_CHANNEL_NOT_PRESENT	Channel number is not available on this MCU.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::open](#)

◆ **R\_SSI\_Stop()**

```
fsp_err_t R_SSI_Stop ( i2s_ctrl_t *const p_ctrl)
```

Stops SSI. Implements [i2s\\_api\\_t::stop](#).

This function disables both transmission and reception, and disables any transfer instances used.

The SSI will stop on the next frame boundary. Do not restart SSI until it is idle.

**Return values**

FSP_SUCCESS	I2S communication stop request issued.
FSP_ERR_ASSERTION	The pointer to p_ctrl was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

**Returns**

See [Common Error Codes](#) or lower level drivers for other possible return codes.

◆ **R\_SSI\_StatusGet()**

```
fsp_err_t R_SSI_StatusGet ( i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status )
```

Gets SSI status and stores it in provided pointer p\_status. Implements `i2s_api_t::statusGet`.

**Return values**

FSP_SUCCESS	Information stored successfully.
FSP_ERR_ASSERTION	The p_instance_ctrl or p_status parameter was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_Write()**

```
fsp_err_t R_SSI_Write ( i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes )
```

Writes data buffer to SSI. Implements `i2s_api_t::write`.

This function resets the transfer if the transfer interface is used, or writes the length of data that fits in the FIFO then stores the remaining write buffer in the control block to be written in the ISR.

Write() cannot be called if another write(), read() or writeRead() operation is in progress. Write can be called when the SSI is idle, or after the I2S\_EVENT\_TX\_EMPTY event.

**Return values**

FSP_SUCCESS	Write initiated successfully.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_src was null, or bytes requested was 0.
FSP_ERR_IN_USE	Another transfer is in progress, data was not written.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_UNDERFLOW	A transmit underflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `transfer_api_t::reset`

◆ **R\_SSI\_Read()**

```
fsp_err_t R_SSI_Read ( i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes )
```

Reads data into provided buffer. Implements `i2s_api_t::read`.

This function resets the transfer if the transfer interface is used, or reads the length of data available in the FIFO then stores the remaining read buffer in the control block to be filled in the ISR.

Read() cannot be called if another write(), read() or writeRead() operation is in progress. Read can be called when the SSI is idle, or after the I2S\_EVENT\_RX\_FULL event.

**Return values**

FSP_SUCCESS	Read initiated successfully.
FSP_ERR_IN_USE	Peripheral is in the wrong mode or not idle.
FSP_ERR_ASSERTION	The pointer to p_ctrl or p_dest was null, or bytes requested was 0.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_OVERFLOW	A receive overflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

◆ **R\_SSI\_WriteRead()**

```
fsp_err_t R_SSI_WriteRead ( i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest,
uint32_t const bytes )
```

Writes from source buffer and reads data into destination buffer. Implements [i2s\\_api\\_t::writeRead](#).

This function calls [R\\_SSI\\_Write](#) and [R\\_SSI\\_Read](#).

[writeRead\(\)](#) cannot be called if another [write\(\)](#), [read\(\)](#) or [writeRead\(\)](#) operation is in progress. [writeRead\(\)](#) can be called when the SSI is idle, or after the [I2S\\_EVENT\\_RX\\_FULL](#) event.

**Return values**

FSP_SUCCESS	Write and read initiated successfully.
FSP_ERR_IN_USE	Peripheral is in the wrong mode or not idle.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	The channel is not opened.
FSP_ERR_UNDERFLOW	A transmit underflow error is pending. Wait for the SSI to go idle before resuming communication.
FSP_ERR_OVERFLOW	A receive overflow error is pending. Wait for the SSI to go idle before resuming communication.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [transfer\\_api\\_t::reset](#)

◆ **R\_SSI\_Mute()**

```
fsp_err_t R_SSI_Mute ( i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable )
```

Mutes SSI on the next frame boundary. Implements [i2s\\_api\\_t::mute](#).

Data is still written while mute is enabled, but the transmit line outputs zeros.

**Return values**

FSP_SUCCESS	Transmission is muted.
FSP_ERR_ASSERTION	The pointer to <a href="#">p_ctrl</a> was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_Close()**

```
fsp_err_t R_SSI_Close ( i2s_ctrl_t *const p_ctrl)
```

Closes SSI. Implements `i2s_api_t::close`.

This function powers down the SSI and closes the lower level timer and transfer drivers if they are used.

**Return values**

FSP_SUCCESS	Device closed successfully.
FSP_ERR_ASSERTION	The pointer to <code>p_ctrl</code> was null.
FSP_ERR_NOT_OPEN	The channel is not opened.

◆ **R\_SSI\_CallbackSet()**

```
fsp_err_t R_SSI_CallbackSet ( i2s_ctrl_t *const p_api_ctrl, void(*) (i2s_callback_args_t *) p_callback, void const *const p_context, i2s_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `i2s_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.52 USB (r\_usb\_basic)**

## Modules

**Functions**

```
fsp_err_t R_USB_Open (usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg)
```

Applies power to the USB module specified in the argument (`p_ctrl`).  
[More...](#)

`fsp_err_t R_USB_Close (usb_ctrl_t *const p_api_ctrl)`  
Terminates power to the USB module specified in argument (`p_ctrl`). USB0 module stops when `USB_IP0` is specified to the member (module), USB1 module stops when `USB_IP1` is specified to the member (module). [More...](#)

`fsp_err_t R_USB_Read (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t destination)`  
Bulk/interrupt data transfer and control data transfer. [More...](#)

`fsp_err_t R_USB_Write (usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size, uint8_t destination)`  
Bulk/Interrupt data transfer and control data transfer. [More...](#)

`fsp_err_t R_USB_Stop (usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination)`  
Requests a data read/write transfer be terminated when a data read/write transfer is being performed. [More...](#)

`fsp_err_t R_USB_Suspend (usb_ctrl_t *const p_api_ctrl)`  
Sends a SUSPEND signal from the USB module assigned to the member (module) of the `usb_ctrl_t` structure. [More...](#)

`fsp_err_t R_USB_Resume (usb_ctrl_t *const p_api_ctrl)`  
Sends a RESUME signal from the USB module assigned to the member (module) of the `usb_ctrl_t` structure. [More...](#)

`fsp_err_t R_USB_VbusSet (usb_ctrl_t *const p_api_ctrl, uint16_t state)`  
Specifies starting or stopping the VBUS supply. [More...](#)

`fsp_err_t R_USB_InfoGet (usb_ctrl_t *const p_api_ctrl, usb_info_t *p_info, uint8_t destination)`  
Obtains completed USB-related events. [More...](#)

`fsp_err_t R_USB_PipeRead (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)`  
Requests a data read (bulk/interrupt transfer) via the pipe specified in the argument. [More...](#)

`fsp_err_t` [R\\_USB\\_PipeWrite](#) (`usb_ctrl_t *const p_api_ctrl`, `uint8_t *p_buf`, `uint32_t size`, `uint8_t pipe_number`)

Requests a data write (bulk/interrupt transfer). [More...](#)

`fsp_err_t` [R\\_USB\\_PipeStop](#) (`usb_ctrl_t *const p_api_ctrl`, `uint8_t pipe_number`)

Terminates a data read/write operation. [More...](#)

`fsp_err_t` [R\\_USB\\_UsedPipesGet](#) (`usb_ctrl_t *const p_api_ctrl`, `uint16_t *p_pipe`, `uint8_t destination`)

Gets the selected pipe number (number of the pipe that has completed initialization) via bit map information. [More...](#)

`fsp_err_t` [R\\_USB\\_PipeInfoGet](#) (`usb_ctrl_t *const p_api_ctrl`, `usb_pipe_t *p_info`, `uint8_t pipe_number`)

Gets the following pipe information regarding the pipe specified in the argument (`p_ctrl`) member (`pipe`): endpoint number, transfer type, transfer direction and maximum packet size. [More...](#)

`fsp_err_t` [R\\_USB\\_PullUp](#) (`usb_ctrl_t *const p_api_ctrl`, `uint8_t state`)

This API enables or disables pull-up of D+/D- line. [More...](#)

`fsp_err_t` [R\\_USB\\_EventGet](#) (`usb_ctrl_t *const p_api_ctrl`, `usb_status_t *event`)

Obtains completed USB related events. (OS-less Only) [More...](#)

`fsp_err_t` [R\\_USB\\_Callback](#) (`usb_callback_t *p_callback`)

Register a callback function to be called upon completion of a USB related event. (RTOS only) [More...](#)

`fsp_err_t` [R\\_USB\\_HostControlTransfer](#) (`usb_ctrl_t *const p_api_ctrl`, `usb_setup_t *p_setup`, `uint8_t *p_buf`, `uint8_t device_address`)

Performs settings and transmission processing when transmitting a setup packet. [More...](#)

`fsp_err_t` [R\\_USB\\_PeriControlDataGet](#) (`usb_ctrl_t *const p_api_ctrl`, `uint8_t *p_buf`, `uint32_t size`)

Receives data sent by control transfer. [More...](#)

`fsp_err_t R_USB_PeriControlDataSet (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)`

Performs transfer processing for control transfer. [More...](#)

`fsp_err_t R_USB_PeriControlStatusSet (usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status)`

Set the response to the setup packet. [More...](#)

`fsp_err_t R_USB_RemoteWakeup (usb_ctrl_t *const p_api_ctrl)`

Sends a remote wake-up signal to the connected Host. [More...](#)

`fsp_err_t R_USB_ModuleNumberGet (usb_ctrl_t *const p_api_ctrl, uint8_t *module_number)`

This API gets the module number. [More...](#)

`fsp_err_t R_USB_ClassTypeGet (usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type)`

This API gets the class type. [More...](#)

`fsp_err_t R_USB_DeviceAddressGet (usb_ctrl_t *const p_api_ctrl, uint8_t *device_address)`

This API gets the device address. [More...](#)

`fsp_err_t R_USB_PipeNumberGet (usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number)`

This API gets the pipe number. [More...](#)

`fsp_err_t R_USB_DeviceStateGet (usb_ctrl_t *const p_api_ctrl, uint16_t *state)`

This API gets the state of the device. [More...](#)

`fsp_err_t R_USB_DataSizeGet (usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)`

This API gets the data size. [More...](#)

`fsp_err_t R_USB_SetupGet (usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)`

This API gets the setup type. [More...](#)

## Detailed Description

Driver for the USB peripheral on RA MCUs. This module implements the [USB Interface](#).

## Overview

The USB module operates in combination with the device class drivers provided by Renesas to form a complete USB stack.

### Features

The USB module has the following key features:

- USB Host mode
  - Enumerates Low/Full/High-speed devices (see note below)
  - Automatic transfer error determination and retry
- USB Peripheral mode
  - Supports USB1.1/2.0/3.0 hosts
- Automatic processing of device connect/disconnect, suspend/resume, and USB bus reset
- Up to 10 pipes
  - Control transfers supported on pipe 0
  - Data transfer on pipes 1 to 9 (Bulk or Interrupt)
- Functions with or without an RTOS

#### Note

*Supported speeds are dependent on the MCU.*

## Configuration

### Build Time Configurations for r\_usb\_basic

The following build time configurations are defined in fsp\_cfg/r\_usb\_basic\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
PLL Frequency	<ul style="list-style-type: none"> <li>• 24MHz</li> <li>• 20MHz</li> <li>• 12MHz</li> <li>• Other</li> </ul>	24MHz	Specify the PLL frequency supplied to the USB module. This setting only applies to USB1 (not USB0).
CPU Bus Access Wait Cycles	Refer to the RA Configuration tool for available options.	9 cycles	This setting controls the delay for consecutive USB peripheral register access. Set this value to a number of CPU cycles that is equivalent to 40.8ns or more.

Battery Charging	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Specify whether or not to include battery charging functionality.
Power IC Shutdown Polarity	<ul style="list-style-type: none"> <li>• Active High</li> <li>• Active Low</li> </ul>	Active High	Select the polarity of the Shutdown signal on the power supply IC (if provided).
Dedicated Charging Port (DCP) Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, USB communication is disabled and the port is used for charging only.
Notifications for SET_INTERFACE/SET_FEATURE/CLEAR_FEATURE	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	When enabled, the application will receive notifications for SET_INTERFACE, SET_FEATURE and CLEAR_FEATURE messages.
Double Buffering	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	When enabled, the FIFOs for Pipes 1-5 are double-buffered.
Continuous Transfer Mode	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	Enable or disable continuous transfer mode.
LDO Regulator	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable LDO regulator.
DMA Support	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Enable or disable DMA support for the USB module.
DMA Source Address	<ul style="list-style-type: none"> <li>• DMA Disabled</li> <li>• FS Address</li> <li>• HS Address</li> </ul>	DMA Disabled	Set this to match the speed mode when DMA is enabled. Otherwise, set to 'DMA Disabled'.
DMA Destination Address	<ul style="list-style-type: none"> <li>• DMA Disabled</li> <li>• FS Address</li> <li>• HS Address</li> </ul>	DMA Disabled	Set this to match the speed mode when DMA is enabled. Otherwise, set to 'DMA Disabled'.

### Configurations for Middleware > USB > USB Driver on r\_usb\_basic

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_basic0	Module name.
USB Mode	<ul style="list-style-type: none"> <li>• Host mode</li> <li>• Peri mode</li> </ul>	Host mode	Select the usb mode.
USB Speed	<ul style="list-style-type: none"> <li>• Full Speed</li> <li>• Hi Speed</li> <li>• Low Speed</li> </ul>	Full Speed	Select the USB speed.

USB Module Number	<ul style="list-style-type: none"> <li>• USB_IP0 Port</li> <li>• USB_IP1 Port</li> </ul>	USB_IP0 Port	Specify the USB module number to be used.
USB Device Class	<ul style="list-style-type: none"> <li>• Peripheral Communications Device Class</li> <li>• Peripheral Human Interface Device Class</li> <li>• Peripheral Mass Storage Class</li> <li>• Peripheral Vendor Class</li> <li>• Host Communications Device Class</li> <li>• Host Human Interface Device Class</li> <li>• Host Mass Storage Class</li> <li>• Host Vendor Class</li> </ul>	Peripheral Communications Device Class	Select the USB device class.
USB Descriptor	USB Descriptor must be a valid C symbol.	g_usb_descriptor	Enter the name of the descriptor to be used. For how to create a descriptor structure, refer to the Descriptor definition chapter in the usb_basic manual. Specify NULL when using the Host class.
USB Compliance Callback	Compliance Callback must be a valid C symbol.	NULL	Set the callback for compliance tests here.
USBFS Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the main USBFS ISR.
USBFS Resume Priority	MCU Specific Options		Select the interrupt priority used by the USBFS Resume ISR.
USBFS D0FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBFS D0FIFO.
USBFS D1FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBFS D1FIFO.
USBHS Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the

main USBHS ISR.

USBHS D0FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBHS D0FIFO ISR.
USBHS D1FIFO Interrupt Priority	MCU Specific Options		Select the interrupt priority used by the USBHS D1FIFO ISR.
USB RTOS Callback	Enter the address of the function.	NULL	If an FreeRTOS is used, set the callback function here.
USB Callback Context	Enter the address of the context.	NULL	Set the callback context here.

## Clock Configuration

The USB module uses PLL as the clock source. The PLL frequency can be set in the **Clocks** tab of the configuration editor or by using the CGC Interface at run-time.

### Note

When using HOCO as the PLL source on Cortex M33 parts the FLL function must be enabled for correct USB operation. Refer to the MCU Family -> Clocks group of the BSP properties in the RA configuration tool to adjust FLL settings.

## Pin Configuration

In peripheral mode the USB\_VBUS and/or USBHS\_VBUS pins are used to detect the USB connection status (connected or disconnected) and should be connected to the USB VBUS signal.

### Note

USB\_VBUS and USBHS\_VBUS are 5V-tolerant pins.

In host mode the USBHS\_VBUSEN, USBHS\_OVRCURA and USBHS\_OVRCURB pins should be connected to the relevant pins of an external power supply IC, if available. These pins will be used to manage the USB VBUS supply.

## DMA Configuration

When using DMA with USB the following properties must be configured for each DMAC module:

Config Name	Select Name	Description
Transfer Size	2 Bytes 4 Bytes	In FS mode, select "2 Bytes" In HS mode, select "4 Bytes"
Activation source	USBFS FIFO 0 USBFS FIFO 1 USBHS FIFO 0 USBHS FIFO 1	USB FS Reception USB FS Transmission USB HS Reception USB HS Transmission

## Descriptor definition

In Peripheral mode, the usb\_descriptor\_t structure stores descriptor information including the device

and configuration descriptors. The values set in this structure are sent to the USB host as part of enumeration.

```
typedef struct usb_descriptor
{
    uint8_t *p_device; /* Pointer to device descriptor */
    uint8_t *p_config_f; /* Pointer to full-speed configuration descriptor */
    uint8_t *p_config_h; /* Pointer to high-speed configuration descriptor (HS only)
*/
    uint8_t *p_qualifier; /* Pointer to device qualifier descriptor (HS only) */
    uint8_t **pp_string; /* Pointer to string descriptor table */
    uint8_t num_string; /* Number of strings in table */
} usb_descriptor_t;
```

#### Note

*Even in high-speed mode the full-speed configuration must be made available:*

```
/* Example USB FS descriptor struct */
usb_descriptor_t g_usb_descriptor =
{
    smp_device,
    smp_config_f,
    NULL,
    NULL,
    smp_str_table,
    3,
};

/* Example USB HS descriptor struct */
usb_descriptor_t g_usb_descriptor =
{
    smp_device,
    smp_config_f,
    smp_config_h,
    smp_qualifier,
    smp_str_table,
    3,
};
```

```
};
```

## String Descriptor

This USB driver requires string descriptors to be registered in the string descriptor table. Use the following format to define the elements:

```
/* String descriptor 0 is reserved for language ID information */
uint8_t str_descriptor_0[]
{
    0x04,      /* Length */
    0x03,      /* Descriptor type */
    0x09, 0x04 /* Language ID */
};

uint8_t str_descriptor_manufacturer[] =
{
    0x10,      /* Length */
    0x03,      /* Descriptor type */
    'R', 0x00,
    'E', 0x00,
    'N', 0x00,
    'E', 0x00,
    'S', 0x00,
    'A', 0x00,
    'S', 0x00
};

uint8_t str_descriptor_product[] =
{
    0x12,      /* Length */
    0x03,      /* Descriptor type */
    'C', 0x00,
    'D', 0x00,
    'C', 0x00,
    '_', 0x00,
    'D', 0x00,
```

```
'E', 0x00,  
'M', 0x00,  
'O', 0x00  
};  
/* String descriptor table */  
uint8_t * smp_str_table[] =  
{  
    str_descriptor_0,          /* Index: 0 */  
    str_descriptor_manufacturer, /* Index: 1 */  
    str_descriptor_product,    /* Index: 2 */  
};
```

#### Note

Set the string index values in the device/configuration descriptors (*iManufacturer*, *iConfiguration* etc.) to the index of the desired string in the string descriptor table. For example, in the table below, the manufacturer is described in *str\_descriptor\_manufacturer* and the value of *iManufacturer* in the device descriptor is **1**.

## Other Descriptors

Refer to the Universal Serial Bus Revision 2.0 specification (<http://www.usb.org/developers/docs/>) for details on how to construct the device, configuration and qualifier descriptors.

## Usage Notes

### Program Structure

USB applications (whether using an RTOS or not) should be written as an event-handling loop. Either a callback function (RTOS only) or `R_USB_EventGet` should be used to provide event data to the application loop where a switch statement handles the event.

#### Note

1. The `USB_STATUS_CONFIGURED` event should be confirmed before calling `R_USB_Read` or `R_USB_Write`.
2. When attaching to USB Host, Suspend event is notified to the application program in USB peripheral mode. Notification of this event to the application program does not affect the operation.

## Limitations

Developers should be aware of the following limitations when using the USB driver:

- The current USB driver does not support hub.
- In USB host mode, the module does not support suspend during data transfers. Execute suspend only after confirming that all transfers are complete.
- Multiconfigurations are not supported.
- This driver does not support CPU transfers using the D0FIFO/D1FIFO register.
- Only one device-class driver may be used at a time.

- The USB Hi-Speed module only supports Hi-Speed operation.
- In USB host mode, this USB driver does not support the composite device.
- The user can not specify DMA transfer to USB IP0 and IP1 modules at the same time when using USB multi-port feature. USB multi-port function: Simultaneous operation feature of USB Host and Peripheral.

## TrustZone

The USB driver for FreeRTOS cannot be allocated in Secure region.

## UCLK setting

Enable UCLK in "Clocks" tab on e2 studio when using the following MCU.

1. RA6M4

# Examples

## USB Basic Example

This is a basic example of minimal use of the USB in an application.

```
void usb_basic_example (void)
{
    usb_event_info_t event_info;
    usb_status_t     event;

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
        g_usb_on_usb.eventGet(&event_info, &event);
        switch (event)
        {
            case USB_STATUS_CONFIGURED:
            case USB_STATUS_WRITE_COMPLETE:
                g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
                break;
            case USB_STATUS_READ_COMPLETE:
                g_usb_on_usb.write(&g_basic0_ctrl, g_buf, event_info.data_size,
                USB_CLASS_PCDC);
                break;
            case USB_STATUS_REQUEST: /* Receive Class Request */
```

```
if (USB_PCDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
{
    g_usb_on_usb.periControlDataGet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
}
else if (USB_PCDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
{
    g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
}
else
{
    g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
}

break;
case USB_STATUS_SUSPEND:
case USB_STATUS_DETACH:
break;
default:
break;
}
}
} /* End of function usb_main() */
```

## Typedefs

```
typedef usb_event_info_t  usb_instance_ctrl_t
```

## Typedef Documentation

### ◆ usb\_instance\_ctrl\_t

```
typedef usb_event_info_t  usb_instance_ctrl_t
```

ICU private control block. DO NOT MODIFY. Initialization occurs when R\_ICU\_ExternallrqOpen is called.

## Function Documentation

◆ **R\_USB\_Open()**

```
fsp_err_t R_USB_Open ( usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg )
```

Applies power to the USB module specified in the argument (p\_ctrl).

**Return values**

FSP_SUCCESS	Success in open.
FSP_ERR_USB_BUSY	Specified USB module now in use.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_Close()**

```
fsp_err_t R_USB_Close ( usb_ctrl_t *const p_api_ctrl)
```

Terminates power to the USB module specified in argument (p\_ctrl). USB0 module stops when USB\_IP0 is specified to the member (module), USB1 module stops when USB\_IP1 is specified to the member (module).

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_NOT_OPEN	USB module is not open.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_Read()**

```
fsp_err_t R_USB_Read ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t destination )
```

Bulk/interrupt data transfer and control data transfer.

## 1. Bulk/interrupt data transfer

Requests USB data read (bulk/interrupt transfer). The read data is stored in the area specified by argument (p\_buf). After data read is completed, confirm the operation by checking the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function. The received data size is set in member (size) of the usb\_ctrl\_t structure. To figure out the size of the data when a read is complete, check the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function, and then refer to the member (size) of the usb\_ctrl\_t structure.

## 2. Control data transfer

The R\_USB\_Read function is used to receive data in the data stage and the R\_USB\_Write function is used to send data to the USB host.

**Return values**

FSP_SUCCESS	Successfully completed (Data read request completed).
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Data receive request already in process for USB device with same device address.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

## ◆ R\_USB\_Write()

```
fsp_err_t R_USB_Write ( usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size,
uint8_t destination )
```

Bulk/Interrupt data transfer and control data transfer.

### 1. Bulk/Interrupt data transfer

Requests USB data write (bulk/interrupt transfer). Stores write data in area specified by argument (p\_buf). Set the device class type in usb\_ctrl\_t structure member (type). Confirm after data write is completed by checking the return value (USB\_STATUS\_WRITE\_COMPLETE) of the R\_USB\_GetEvent function. For sending a zero-length packet, please refer the following Note.

### 2. Control data transfer

The R\_USB\_Read function is used to receive data in the data stage and the R\_USB\_Write function is used to send data to the USB host.

## Return values

FSP_SUCCESS	Successfully completed. (Data write request completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Data write request already in process for USB device with same device address.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

## Note

1. The user needs to send the zero-length packet (ZLP) since this USB driver does not send the ZLP automatically. When sending a ZLP, the user sets USB\_NULL in the third argument (size) of R\_USB\_Write function as follow. e.g)

```
R_USB_Write (&g_basic0_ctrl, &g_buf, USB_NULL);
```

2. Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_Stop()**

```
fsp_err_t R_USB_Stop ( usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination )
```

Requests a data read/write transfer be terminated when a data read/write transfer is being performed.

To stop a data read, set USB\_TRANSFER\_READ as the argument (type); to stop a data write, specify USB\_WRITE as the argument (type).

**Return values**

FSP_SUCCESS	Successfully completed. (stop completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Stop processing is called multiple times.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_Suspend()**

```
fsp_err_t R_USB_Suspend ( usb_ctrl_t *const p_api_ctrl)
```

Sends a SUSPEND signal from the USB module assigned to the member (module) of the usb\_ctrl\_t structure.

After the suspend request is completed, confirm the operation with the return value (USB\_STATUS\_SUSPEND) of the R\_USB\_EventGet function.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	During a suspend request to the specified USB module, or when the USB module is already in the suspended state.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_Resume()**

```
fsp_err_t R_USB_Resume ( usb_ctrl_t *const p_api_ctrl)
```

Sends a RESUME signal from the USB module assigned to the member (module) of the usb\_ctrl\_t structure.

After the resume request is completed, confirm the operation with the return value (USB\_STATUS\_RESUME) of the R\_USB\_EventGet function

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_BUSY	Resume already requested for same device address. (USB host mode only)
FSP_ERR_USB_NOT_SUSPEND	USB device is not in the SUSPEND state.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_VbusSet()**

```
fsp_err_t R_USB_VbusSet ( usb_ctrl_t *const p_api_ctrl, uint16_t state )
```

Specifies starting or stopping the VBUS supply.

**Return values**

FSP_SUCCESS	Successful completion. (VBUS supply start/stop completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_InfoGet()**

```
fsp_err_t R_USB_InfoGet ( usb_ctrl_t *const p_api_ctrl, usb_info_t * p_info, uint8_t destination )
```

Obtains completed USB-related events.

**Return values**

FSP_SUCCESS	Successful completion. (VBUS supply start/stop completed)
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_PipeRead()**

```
fsp_err_t R_USB_PipeRead ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t pipe_number )
```

Requests a data read (bulk/interrupt transfer) via the pipe specified in the argument.

The read data is stored in the area specified in the argument (p\_buf). After the data read is completed, confirm the operation with the R\_USB\_GetEvent function return value(USB\_STATUS\_READ\_COMPLETE). To figure out the size of the data when a read is complete, check the return value (USB\_STATUS\_READ\_COMPLETE) of the R\_USB\_GetEvent function, and then refer to the member (size) of the usb\_ctrl\_t structure.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

- Do not call this API in the following function.
- (1). Interrupt function.
  - (2). Callback function ( for RTOS ).

◆ **R\_USB\_PipeWrite()**

```
fsp_err_t R_USB_PipeWrite ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size, uint8_t pipe_number )
```

Requests a data write (bulk/interrupt transfer).

The write data is stored in the area specified in the argument (p\_buf). After data write is completed, confirm the operation with the return value (USB\_STATUS\_WRITE\_COMPLETE) of the EventGet function. For sending a zero-length packet, please refer the following Note.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

1. The user needs to send the zero-length packet(ZLP) since this USB driver does not send the ZLP automatically. When sending a ZLP, the user sets USB\_NULL in the third argument (size) of R\_USB\_PipeWrite function as follow.

e.g)

```
R_USB_PipeWrite (&g_basic0_ctrl, &g_buf, USB_NULL, pipe_number);
```

2. Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PipeStop()**

```
fsp_err_t R_USB_PipeStop ( usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number )
```

Terminates a data read/write operation.

**Return values**

FSP_SUCCESS	Successfully completed. (Stop request completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_UsedPipesGet()**

```
fsp_err_t R_USB_UsedPipesGet ( usb_ctrl_t *const p_api_ctrl, uint16_t * p_pipe, uint8_t destination )
```

Gets the selected pipe number (number of the pipe that has completed initialization) via bit map information.

The bit map information is stored in the area specified in argument (p\_pipe). Based on the information (module member and address member) assigned to the usb\_ctrl\_t structure, obtains the PIPE information of that USB device.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_PipeInfoGet()**

```
fsp_err_t R_USB_PipeInfoGet ( usb_ctrl_t *const p_api_ctrl, usb_pipe_t * p_info, uint8_t pipe_number )
```

Gets the following pipe information regarding the pipe specified in the argument (p\_ctrl) member (pipe): endpoint number, transfer type, transfer direction and maximum packet size.

The obtained pipe information is stored in the area specified in the argument (p\_info).

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_PullUp()**

```
fsp_err_t R_USB_PullUp ( usb_ctrl_t *const p_api_ctrl, uint8_t state )
```

This API enables or disables pull-up of D+/D- line.

**Return values**

FSP_SUCCESS	Successful completion. (Pull-up enable/disable setting completed)
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

- (1). Interrupt function.
- (2). Callback function ( for RTOS ).

◆ **R\_USB\_EventGet()**

```
fsp_err_t R_USB_EventGet ( usb_ctrl_t *const p_api_ctrl, usb_status_t * event )
```

Obtains completed USB related events. (OS-less Only)

In USB host mode, the device address value of the USB device that completed an event is specified in the `usb_ctrl_t` structure member (address) specified by the event's argument. In USB peripheral mode, `USB_NULL` is specified in member (address). If this function is called in the RTOS execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Event Get Success.
FSP_ERR_USB_FAILED	If called in the RTOS environment, an error is returned.

**Note**

*Do not use the same variable as the first argument of `R_USB_Open` for the first argument.  
Do not call this API in the interrupt function.*

◆ **R\_USB\_Callback()**

```
fsp_err_t R_USB_Callback ( usb_callback_t * p_callback)
```

Register a callback function to be called upon completion of a USB related event. (RTOS only)

This function registers a callback function to be called when a USB-related event has completed. If this function is called in the OS-less execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Successfully completed.
FSP_ERR_USB_FAILED	If this function is called in the OS-less execution environment, a failure is returned.
FSP_ERR_ASSERTION	Parameter is NULL error.

**Note**

*Do not call this API in the interrupt function.*

◆ **R\_USB\_HostControlTransfer()**

```
fsp_err_t R_USB_HostControlTransfer ( usb_ctrl_t *const p_api_ctrl, usb_setup_t * p_setup, uint8_t * p_buf, uint8_t device_address )
```

Performs settings and transmission processing when transmitting a setup packet.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PeriControlDataGet()**

```
fsp_err_t R_USB_PeriControlDataGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size )
```

Receives data sent by control transfer.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PericontrolDataSet()**

```
fsp_err_t R_USB_PericontrolDataSet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_buf, uint32_t size )
```

Performs transfer processing for control transfer.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_BUSY	Specified pipe now handling data receive/send request.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_PericontrolStatusSet()**

```
fsp_err_t R_USB_PericontrolStatusSet ( usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status )
```

Set the response to the setup packet.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_PARAMETER	Parameter error.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_RemoteWakeup()**

```
fsp_err_t R_USB_RemoteWakeup ( usb_ctrl_t *const p_api_ctrl)
```

Sends a remote wake-up signal to the connected Host.

**Return values**

FSP_SUCCESS	Successful completion.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter is NULL error.
FSP_ERR_USB_NOT_SUSPEND	Device is not suspended.
FSP_ERR_USB_BUSY	The device is in resume operation.

**Note**

Do not call this API in the following function.

(1). Interrupt function.

(2). Callback function ( for RTOS ).

◆ **R\_USB\_ModuleNumberGet()**

```
fsp_err_t R_USB_ModuleNumberGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * module_number )
```

This API gets the module number.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_ClassTypeGet()**

```
fsp_err_t R_USB_ClassTypeGet ( usb_ctrl_t *const p_api_ctrl, usb_class_t * class_type )
```

This API gets the class type.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DeviceAddressGet()**

```
fsp_err_t R_USB_DeviceAddressGet ( usb_ctrl_t*const p_api_ctrl, uint8_t* device_address )
```

This API gets the device address.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_PipeNumberGet()**

```
fsp_err_t R_USB_PipeNumberGet ( usb_ctrl_t*const p_api_ctrl, uint8_t* pipe_number )
```

This API gets the pipe number.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DeviceStateGet()**

```
fsp_err_t R_USB_DeviceStateGet ( usb_ctrl_t*const p_api_ctrl, uint16_t* state )
```

This API gets the state of the device.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

◆ **R\_USB\_DataSizeGet()**

```
fsp_err_t R_USB_DataSizeGet ( usb_ctrl_t*const p_api_ctrl, uint32_t* data_size )
```

This API gets the data size.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

**◆ R\_USB\_SetupGet()**

```
fsp_err_t R_USB_SetupGet ( usb_ctrl_t *const p_api_ctrl, usb_setup_t * setup )
```

This API gets the setup type.

**Return values**

FSP_SUCCESS	Successful completion.
-------------	------------------------

**4.2.53 USB Composite Class (r\_usb\_composite)****Modules****Functions**

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

**Overview**

USB composite device works as a USB Peripheral by combining two peripheral device classes and r\_usb\_basic module.

This USB driver supports the following composite devices:

1. PCDC + PMSC
2. PCDC + PHID
3. PHID + PMSC
4. PCDC + PCDC

**How to Configuration**

The following shows FSP configuration procedure for USB composite device.

- Select [New Stack]->[USB]->[USB Composite]

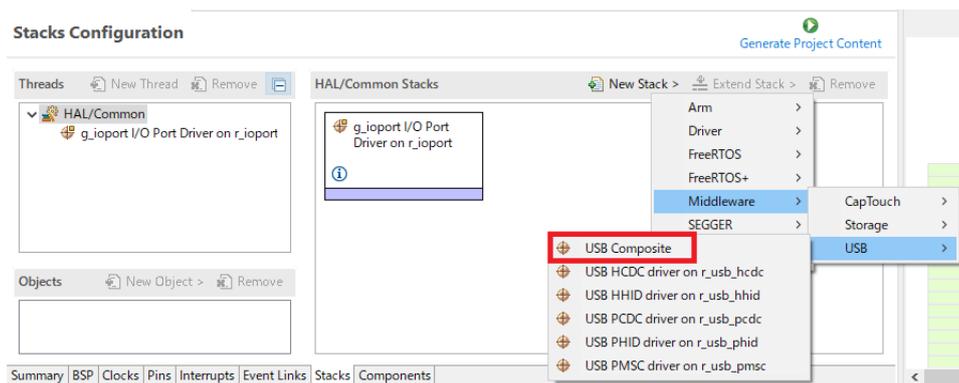


Figure 168: Select USB Composite

- The following is displayed when selecting [USB Composite].

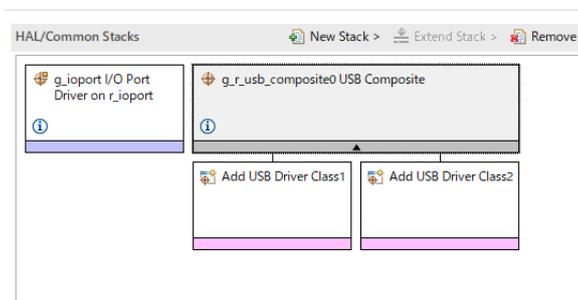


Figure 169: USB Composite Stack

- Select the supported 2 device classes as follows.

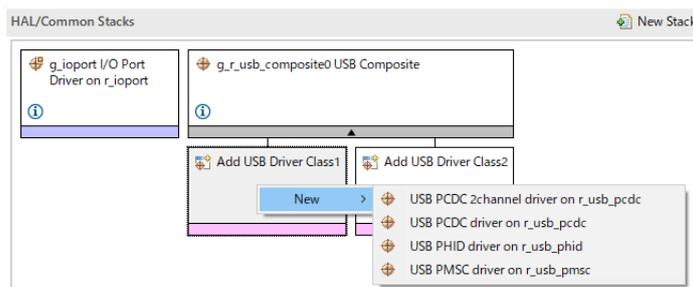


Figure 170: Select Device Classes

*Note*

1. Be sure to select "USB PCDC driver on r\_usb\_pcdc" and "USB PCDC 2channel driver on r\_usb\_pcdc" when configuring for "PCDC + PCDC".

- Select the supported 2 device classes as follows. The following is displayed when selecting 2 device classes.

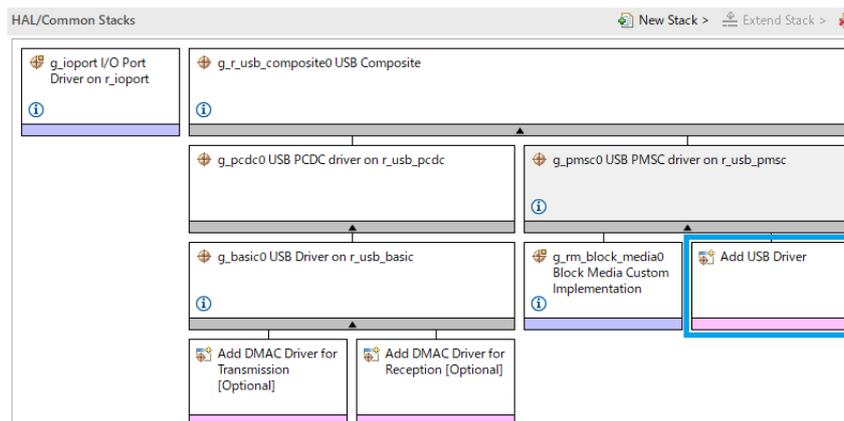


Figure 171: Delete USB Basic Instance

**Note**

1. Delete the "g\_basic1" instance manually since this instance is not used in composite device. (Refer to the blue frame in the above figure.)
2. The error is output when selecting the following device classes.
  - a. PMSC + PMSC
  - b. PHID + PHID

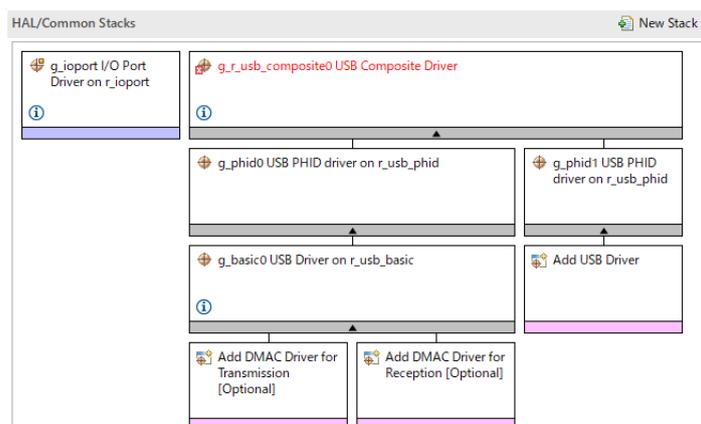


Figure 172: Device Class Selection Error

**Limitations**

1. The following composite device is not supported when using RA2A1(MCU).

1. PMSC + PCDC
2. PCDC + PCDC

2. If you use PMSC, make sure to use usb\_basic module with PMSC. There is a risk that the information on the PMSC storage media cannot be registered normally in the "USB Callback Context".

**Notes**

Please determine by the member "pipe" in "usb\_event\_info" structure when getting PCDC channel number which the write event is completed in PCDC + PCDC.  
Don't refer to the member "type" in "usb\_event\_info" structure.

## Descriptor

Templates for composite device descriptors can be found in ra/fsp/src/r\_usb\_composite folder. Also, please be sure to use your vendor ID.

1. r\_usb\_pcdc\_pmsc\_descriptor.c.template (for PCDC + PMSC)
2. r\_usb\_pcdc\_phid\_descriptor.c.template (for PCDC + PHID)
3. r\_usb\_phid\_pmsc\_descriptor.c.template (for PHID + PMSC)
4. r\_usb\_pcdc\_pcdc\_descriptor.c.template (for PCDC + PCDC)

## Examples

### USB COMPOSITE Example

- PCDC + PHID

```
void main_task (void)
{
    #if (BSP_CFG_RTOS == 2)
        usb_event_info_t * p_mess;
    #endif

    usb_event_info_t usb_event;
    usb_status_t      event;
    uint8_t           * p_idle_value;
    uint8_t           sw_data;
    usb_info_t        info;
    fsp_err_t         ret_code = FSP_SUCCESS;
    uint8_t           send_data[16] BSP_ALIGN_VARIABLE(4);
    uint8_t           req_comp_flag = 0;
    uint8_t           count         = 0;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    set_key_data(g_buf_phid);
    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
        #if (BSP_CFG_RTOS == 2)
            USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
```

```
        usb_event = *p_mess;
event    = usb_event.event;
    #else /* (BSP_CFG_RTOS == 2) */
R_USB_EventGet(&usb_event, &event);
    #endif /* (BSP_CFG_RTOS == 2) */
switch (event)
    {
case USB_STATUS_CONFIGURED:
    {
        g_status = NO_WRITING;
        g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
break;
    }
case USB_STATUS_WRITE_COMPLETE:
    {
if (usb_event.type == USB_CLASS_PCDC)
    {
        g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
    }
else if (usb_event.type == USB_CLASS_PHID)
    {
if (DATA_WRITING == g_status)
    {
        g_status = ZERO_WRITING;
        g_usb_on_usb.write(&g_basic0_ctrl, (uint8_t *) g_zero_data,
DATA_LEN_PHID, USB_CLASS_PHID); /* Sending the zero data (8 bytes) */
    }
else if (g_status == ZERO_WRITING)
    {
        g_status = NO_WRITING;
    }
    }
break;
    }
    }
```

```
case USB_STATUS_READ_COMPLETE:
{
if (usb_event.type == USB_CLASS_PCDC)
{
g_usb_on_usb.write(&g_basic0_ctrl, g_buf, usb_event.data_size,
USB_CLASS_PCDC);
if (req_comp_flag == 1)
{
if (g_status == NO_WRITING)
{
count++;
g_status = DATA_WRITING;
g_usb_on_usb.write(&g_basic0_ctrl, g_buf_phid,
DATA_LEN_PHID, USB_CLASS_PHID);
}
}
}
break;
}
case USB_STATUS_REQUEST: /* Receive Class Request */
{
if (USB_PCDC_SET_LINE_CODING == (usb_event.setup.request_type & USB_BREQUEST))
{
R_USB_PericontrolDataGet(&g_basic0_ctrl, (uint8_t *) &g_line_coding,
LINE_CODING_LENGTH);
}
else if (USB_PCDC_GET_LINE_CODING == (usb_event.setup.request_type & USB_BREQUEST))
{
R_USB_PericontrolDataSet(&g_basic0_ctrl, (uint8_t *) &g_line_coding,
LINE_CODING_LENGTH);
}
else if (USB_SET_REPORT == (usb_event.setup.request_type & USB_BREQUEST))
{
g_usb_on_usb.read(&g_basic0_ctrl, (uint8_t *) &g_numlock, 2,
```

```
USB_CLASS_PHID); /* Get the NumLock data (NumLock data is not used) */
    }

else if (USB_GET_DESCRIPTOR == (usb_event.setup.request_type & USB_BREQUEST))
    {
    if (USB_GET_REPORT_DESCRIPTOR == usb_event.setup.request_value)
        {
            g_usb_on_usb.periControlDataSet(&g_basic0_ctrl,
                                           (uint8_t *) g_apl_report,
                                           USB_RECEIVE_REPORT_DESCRIPTOR);
        }

else if (USB_GET_HID_DESCRIPTOR == usb_event.setup.request_value)
    {
    for (uint8_t i = 0; i < USB_RECEIVE_HID_DESCRIPTOR; i++)
        {
            send_data[i] = g_apl_configuration[84 + i];
        }

/* Configuration Descriptor address set. */
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, send_data,
        USB_RECEIVE_HID_DESCRIPTOR);
    }

else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
        USB_SETUP_STATUS_STALL);
    }
    }

else if (USB_SET_IDLE == (usb_event.setup.request_type & USB_BREQUEST))
    {
    /* Get SetIdle value */
        p_idle_value = (uint8_t *) &usb_event.setup.request_value;
        g_idle        = p_idle_value[1];
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
        USB_SETUP_STATUS_ACK);
    }
```

```
    }
else if (USB_GET_IDLE == (usb_event.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, &g_idle, 1);
    }
else if (USB_SET_PROTOCOL == (usb_event.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
else if (USB_GET_PROTOCOL == (usb_event.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
break;
}
case USB_STATUS_REQUEST_COMPLETE: /* Complete Class Request */
    {
        if (USB_SET_IDLE == (usb_event.setup.request_type & USB_BREQUEST))
            {
                p_idle_value = (uint8_t *) &usb_event.setup.request_value;
                g_idle = p_idle_value[1];
            }
        else if (USB_SET_PROTOCOL == (usb_event.setup.request_type & USB_BREQUEST))
            {
                /* None */
                /* g_protocol = event_info.setup.value; */
            }
    }
```

```
else
    {
        req_comp_flag = 1;
    }
break;
}
case USB_STATUS_SUSPEND:
case USB_STATUS_DETACH:
    {
break;
    }
default:
    {
break;
    }
}
} /* End of function usb_main() */
void set_key_data (uint8_t * p_buf)
{
    static uint8_t key_data;
    key_data = KBD_CODE_A;
    *(p_buf + 2) = key_data;
}
#if (BSP_CFG_RTOS == 2)
/*****
* Function Name : usb_apl_rec_msg
* Description : Receive a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t** mess : Message pointer
* : usb_tm_t tm : Timeout Value
* Return : uint16_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_rec_msg (uint8_t id, usb_msg_t ** mess, usb_tm_t tm)
```

```

{
    BaseType_t    err;
    QueueHandle_t handle;
    usb_er_t      result;
    (void) tm;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    *mess = NULL;
    err = xQueueReceive(handle, (void *) mess, (portMAX_DELAY));
    if ((pdTRUE == err) && (NULL != (*mess)))
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }
    return result;
}
/*****
* End of function usb_apl_rec_msg
*****/
/*****
* Function Name : usb_apl_snd_msg
* Description : Send a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t* mess : Message pointer
* Return : usb_er_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_snd_msg (uint8_t id, usb_msg_t * mess)
{

```

```
    BaseType_t    err;
    QueueHandle_t handle;
    usb_er_t      result;

    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }

    handle = (*(g_apl_mbx_table[id]));
    err = xQueueSend(handle, (const void *) &mess, (TickType_t) (0));

    if (pdTRUE == err)
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }

    return result;
}

/*****
 * End of function usb_apl_snd_msg
 *****/

#endif /* #if (BSP_CFG_RTOS == 2) */
```

## 4.2.54 USB Host Communications Device Class Driver (r\_usb\_hcdc)

### Modules

This module provides a USB Host Communications Device Class (HCDC) driver. It implements the [USB HCDC Interface](#).

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

### Detailed Description

## Overview

The `r_usb_hcdc` module, when used in combination with the `r_usb_basic` module, operates as a USB Host Communications Device Class (HCDC) driver. The HCDC conforms to the PSTN device subclass abstract control model of the USB Communications Device Class (CDC) specification and enables communication with a CDC peripheral device.

### Features

The `r_usb_hcdc` module has the following key features:

- Checks for connected devices
- Implementation of communication line settings
- Acquisition of the communication line state
- Data transfer to and from a CDC peripheral device

## Configuration

### Build Time Configurations for `r_usb_hcdc`

The following build time configurations are defined in `fsp_cfg/r_usb_hcdc_cfg.h`:

Configuration	Options	Default	Description
Target Peripheral Device Class ID	<ul style="list-style-type: none"> <li>• CDC class supported device</li> <li>• Vendor class device</li> </ul>	CDC class supported device	Specify the device class ID of the CDC device to be connected.
Bulk Input Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Output Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the USB pipe to use for interrupts.

### Configurations for Middleware > USB > USB HCDC driver on `r_usb_hcdc`

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB HCDC driver on `r_usb_hcdc`.

Configuration	Options	Default	Description
Name	Name must be a valid	<code>g_hcdc0</code>	Module name.

## C symbol

### Note

Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Communications Device Class (CDC), PSTN and ACM

This software conforms to the Abstract Control Model (ACM) subclass of the Communications Device Class specification as defined in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2. The Abstract Control Model subclass is a technology that bridges the gap between USB devices and earlier modems (employing RS-232C connections) enabling use of application programs designed for older modems.

### Basic Functions

The main functions of HCDC are the following:

- Verify connected devices
- Make communication line settings
- Acquire the communication line state
- Transfer data to and from the CDC peripheral device

### Abstract Control Model Class Requests - Host to Device

This driver supports the following class requests:

Request	Code	Description
SendEncapsulatedCommand	0x00	Transmits an AT command as defined by the protocol used by the device (normally 0 for USB).
GetEncapsulatedResponse	0x01	Requests a response to a command transmitted by SendEncapsulatedCommand.
SetCommFeature	0x02	Enables or disables features such as device-specific 2-byte code and country setting.
GetCommFeature	0x03	Acquires the enabled/disabled state of features such as device-specific 2-byte code and country setting.
ClearCommFeature	0x04	Restores the default

			enabled/disabled settings of features such as device-specific 2-byte code and country setting.
SetLineCoding	0x20		Makes communication line settings (communication speed, data length, parity bit, and stop bit length).
GetLineCoding	0x21		Acquires the communication line setting state.
SetControlLineState	0x22		Makes communication line control signal (RTS, DTR) settings.
SendBreak	0x23		Transmits a break signal.

*Note*

For more information about Abstract Control Model requests, refer to Table 11 "Requests - Abstract Control Model" in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2.

The expected data format for each command is shown below followed by dependent structures.

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x21	SEND_ENCAPSULATED_COMMAND (0x00)	0x0000	0x0000	Data length	<a href="#">usb_hcdc_encapsulated_t</a>
0x21	GET_ENCAPSULATED_RESPONSE (0x01)	0x0000	0x0000	Data length	<a href="#">usb_hcdc_encapsulated_t</a>
0x21	SET_COMM_FEATURE (0x02)	<a href="#">usb_hcdc_feature_selector_t</a>	0x0000	Data length	<a href="#">usb_hcdc_comfeature_t</a>
0x21	GET_COMM_FEATURE (0x03)	<a href="#">usb_hcdc_feature_selector_t</a>	0x0000	Data length	<a href="#">usb_hcdc_comfeature_t</a>
0x21	CLEAR_COMM_FEATURE (0x04)	<a href="#">usb_hcdc_feature_selector_t</a>	0x0000	Data length	None
0x21	SET_LINE_CODING (0x20)	0x0000	0x0000	0x0000	<a href="#">usb_hcdc_linecoding_t</a>
0xA1	GET_LINE_CODING (0x21)	0x0000	0x0000	0x0007	<a href="#">usb_hcdc_linecoding_t</a>
0x21	SET_CONTROL_LINE_STATE (0x22)	<a href="#">usb_hcdc_control_line_state_t</a>	0x0000	0x0000	None
0x21	SEND_BREAK (0x23)	<a href="#">usb_hcdc_break_duration_t</a>	0x0000	0x0000	None

## ACM Notifications from Device to Host

The following class notifications are supported:

Notification	Code	Description
RESPONSE_AVAILABLE	0x01	Response to GET_ENCAPSULATED_RESPONSE
SERIAL_STATE	0x20	Notification of serial line state

The data types returned are as follows:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0xA1	RESPONSE_AVAILABLE (0x01)	0x0000	0x0000	0x0000	None
0xA1	SERIAL_STATE (0x20)	0x0000	0x0000	0x0002	<a href="#">usb_hcdc_serialstate_t</a>

*Note*

*The host is notified with SERIAL\_STATE whenever a change in the UART port state is detected.*

## Limitations

This driver is subject to the following limitations:

- Suspend is not supported when a data transfer is in progress. Confirm that data transfer has completed before executing suspend.
- Use of compound USB devices with CDC class support is not supported.
- This module must be incorporated into a project using r\_usb\_basic and does not provide any public APIs.
- This driver does not support Low-speed.
- This driver does not support simultaneous operation with the other device class.

## Examples

### USB H CDC Loopback Example

The main functions of the H CDC loopback example are as follows:

1. Virtual UART control settings are configured by transmitting the class request SET\_LINE\_CODING to the CDC device.
2. Sends receive (Bulk In transfer) requests to a CDC peripheral device and receives data.
3. Loops received data back to the peripheral by means of Bulk Out transfers.

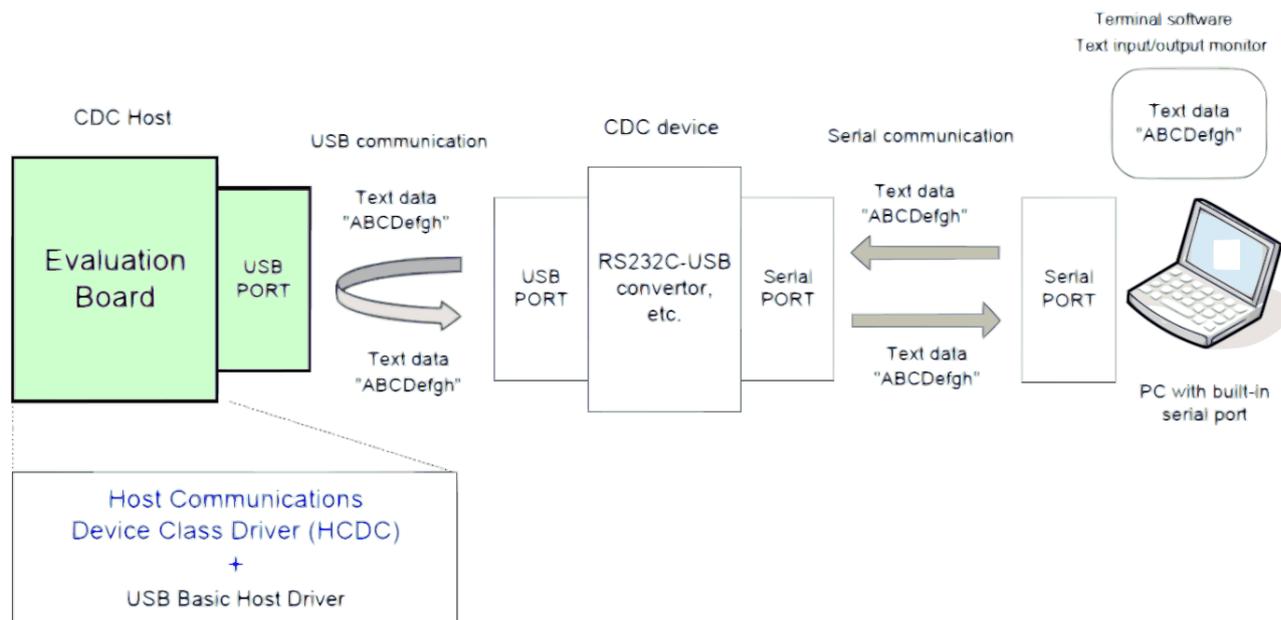


Figure 173: Data Transfer (Loopback)

The main loop performs loopback processing in which data received from a CDC peripheral device is transmitted unaltered back to the peripheral.

```
#define SET_LINE_CODING (USB_CDC_SET_LINE_CODING | USB_HOST_TO_DEV | USB_CLASS |
USB_INTERFACE)
#define GET_LINE_CODING (USB_CDC_GET_LINE_CODING | USB_DEV_TO_HOST | USB_CLASS |
USB_INTERFACE)
#define SET_CONTROL_LINE_STATE (USB_CDC_SET_CONTROL_LINE_STATE | USB_HOST_TO_DEV |
USB_CLASS | USB_INTERFACE)
#define COM_SPEED (9600U)
#define COM_DATA_BIT (8U)
#define COM_STOP_BIT (0)
#define COM_PARITY_BIT (0)
#define LINE_CODING_LENGTH (7)
void usb_basic_example (void)
{
    usb_status_t    event;
    usb_event_info_t event_info;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
```

```
/* Get USB event data */
    g_usb_on_usb.eventGet(&event_info, &event);
/* Handle the received event (if any) */
switch (event)
{
case USB_STATUS_CONFIGURED:
/* Configure virtual UART settings */
    set_line_coding(&g_basic0_ctrl, event_info.device_address); /* CDC
Class request "SetLineCoding" */
    break;
case USB_STATUS_READ_COMPLETE:
if (USB_CLASS_HCDC == event_info.type)
{
if (event_info.data_size > 0)
{
/* Send the received data back to the connected peripheral */
    g_usb_on_usb.write(&g_basic0_ctrl, g_snd_buf,
event_info.data_size, USB_DEVICE_ADDRESS_1);
}
else
{
/* Send the data reception request when the zero-length packet is received. */
    g_usb_on_usb.read(&g_basic0_ctrl, g_rcv_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);
}
}
else /* USB_HCDCC */
{
/* Control Class notification "SerialState" receive start */
    g_usb_on_usb.read(&g_basic0_ctrl,
                    (uint8_t *) &g_serial_state,
                    USB_HCDC_SERIAL_STATE_MSG_LEN,
                    USB_DEVICE_ADDRESS_1);
}
}
```

```
break;

case USB_STATUS_WRITE_COMPLETE:

/* Start receive operation */
    g_usb_on_usb.read(&g_basic0_ctrl, g_rcv_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);

break;

case USB_STATUS_REQUEST_COMPLETE:

if (USB_CDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {

/* Set virtual RTS/DTR signal state */
        set_control_line_state(&g_basic0_ctrl, event_info.device_address);
/* CDC Class request "SetControlLineState" */
    }

/* Check Complete request "SetControlLineState" */
else if (USB_CDC_SET_CONTROL_LINE_STATE == (event_info.setup.request_type &
USB_BREQUEST))
    {

/* Read back virtual UART settings */
        get_line_coding(&g_basic0_ctrl, event_info.device_address); /* CDC
Class request "SetLineCoding" */
    }

else if (USB_CDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {

/* Now that setup is complete, start loopback operation */
        g_usb_on_usb.read(&g_basic0_ctrl, g_snd_buf, CDC_DATA_LEN,
USB_DEVICE_ADDRESS_1);
    }

else
    {

/* Unsupported request */
    }

break;

default:

/* Other event */
```

```
break;
    }
}

void set_control_line_state (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;
    setup.request_type = SET_CONTROL_LINE_STATE; /*
bRequestCode:SET_CONTROL_LINE_STATE, bmRequestType */
    setup.request_value = 0x0000; /* wValue:Zero */
    setup.request_index = 0x0000; /* wIndex:Interface */
    setup.request_length = 0x0000; /* wLength:Zero */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_usb_dummy,
device_address);
}

void set_line_coding (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;
    g_com_parm.dwdte_rate = (usb_hcdc_line_speed_t) COM_SPEED;
    g_com_parm.bchar_format = (usb_hcdc_stop_bit_t) COM_STOP_BIT;
    g_com_parm.bparity_type = (usb_hcdc_parity_bit_t) COM_PARITY_BIT;
    g_com_parm.bdata_bits = (usb_hcdc_data_bit_t) COM_DATA_BIT;
    setup.request_type = SET_LINE_CODING; /* bRequestCode:SET_LINE_CODING,
bmRequestType */
    setup.request_value = 0x0000; /* wValue:Zero */
    setup.request_index = 0x0000; /* wIndex:Interface */
    setup.request_length = LINE_CODING_LENGTH; /* Data:Line Coding Structure */
    /* Request Control transfer */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_com_parm,
device_address);
}

void get_line_coding (usb_instance_ctrl_t * p_ctrl, uint8_t device_address)
{
    usb_setup_t setup;
```

```

    setup.request_type    = GET_LINE_CODING;      /* bRequestCode:GET_LINE_CODING,
bmRequestType */

    setup.request_value  = 0x0000;                /* wValue:Zero */

    setup.request_index  = 0x0000;                /* wIndex:Interface */

    setup.request_length = LINE_CODING_LENGTH; /* Data:Line Coding Structure */
/* Request Control transfer */

    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_com_parm,
device_address);
}

```

## 4.2.55 USB Host Human Interface Device Class Driver (r\_usb\_hhid)

### Modules

#### Functions

`fsp_err_t` [R\\_USB\\_HHID\\_TypeGet](#) (`usb_ctrl_t` \*const p\_api\_ctrl, `uint8_t` \*p\_type, `uint8_t` device\_address)

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.) [More...](#)

`fsp_err_t` [R\\_USB\\_HHID\\_MaxPacketSizeGet](#) (`usb_ctrl_t` \*const p\_api\_ctrl, `uint16_t` \*p\_size, `uint8_t` direction, `uint8_t` device\_address)

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT). [More...](#)

#### Detailed Description

This module provides a USB Host Human Interface Device Class Driver (HHID). It implements the [USB HHID Interface](#).

## Overview

The `r_usb_hhid` module combines with the `r_usb_basic` module to provide a USB Host Human Interface Device Class (HHID) driver. The HHID driver conforms to the USB Human Interface Device class specifications and implements communication with a HID device.

#### Features

The `r_usb_hhid` module has the following key features:

- Data communication with a connected HID device (USB mouse, keyboard etc.)
- Issuing of HID class requests to a connected HID device
- Supports Interrupt OUT transfer

## Configuration

### Build Time Configurations for r\_usb\_hhid

The following build time configurations are defined in fsp\_cfg/r\_usb\_hhid\_cfg.h:

Configuration	Options	Default	Description
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the pipe number to use for input interrupt events.
Interrupt Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE9	Select the pipe number to use for output interrupt events.

### Configurations for Middleware > USB > USB HHID driver on r\_usb\_hhid

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB HHID driver on r\_usb\_hhid. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_hhid0	Module name.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Note

*This driver is not guaranteed to provide USB HID operation in all scenarios. The developer must verify correct operation when connected to the targeted USB peripherals.*

### Class Requests

The class requests supported by this driver are shown below:

Request	Code	Description
USB_GET_REPORT	0x01	Receives a report from the HID device.

USB_SET_REPORT	0x09	Sends a report to the HID device.
USB_GET_IDLE	0x02	Receives a duration (time) from the HID device.
USB_SET_IDLE	0x0A	Sends a duration (time) to the HID device.
USB_GET_PROTOCOL	0x03	Reads a protocol from the HID device.
USB_SET_PROTOCOL	0x0B	Sends a protocol to the HID device.
USB_GET_REPORT_DESCRIPTOR	0x06	Requests a report descriptor.
USB_GET_HID_DESCRIPTOR	0x06	Requests a HID descriptor.

### Data Format

The boot protocol data format of data received from the keyboard or mouse through interrupt-IN transfers is shown below:

offset	Keyboard (8 Bytes)	Mouse (3 Bytes)
0 (Top Byte)	Modifier keys	b0 : Button 1 b1 : Button 2 b2 : Button 3 b3-b7 : Reserved
+1	Reserved	X displacement
+2	Keycode 1	Y displacement
+3	Keycode 2	-
+4	Keycode 3	-
+5	Keycode 4	-
+6	Keycode 5	-
+7	Keycode 6	-

### Limitations

- The HID driver does not analyze the report descriptor. This driver determines the report format from the interface protocol.
- This driver does not support DMA transfers.
- This driver does not support High-speed.
- The transfer rates of Full-speed and Low-speed are the same when the max packet sizes of Full-speed and Low-speed are the same.
- This driver does not support simultaneous operation with the other device class.

## Examples

### USB HHID Example

The main functions of the application are as follows:

1. Performs enumeration and initialization of HID devices.
2. Transfers data to and from a connected HID device (mouse or keyboard). Data received from the device is read and discarded.
3. When an RTOS is used, the USB driver calls the callback (`usb_apl_callback`) in order to pass events to the main loop through a queue.

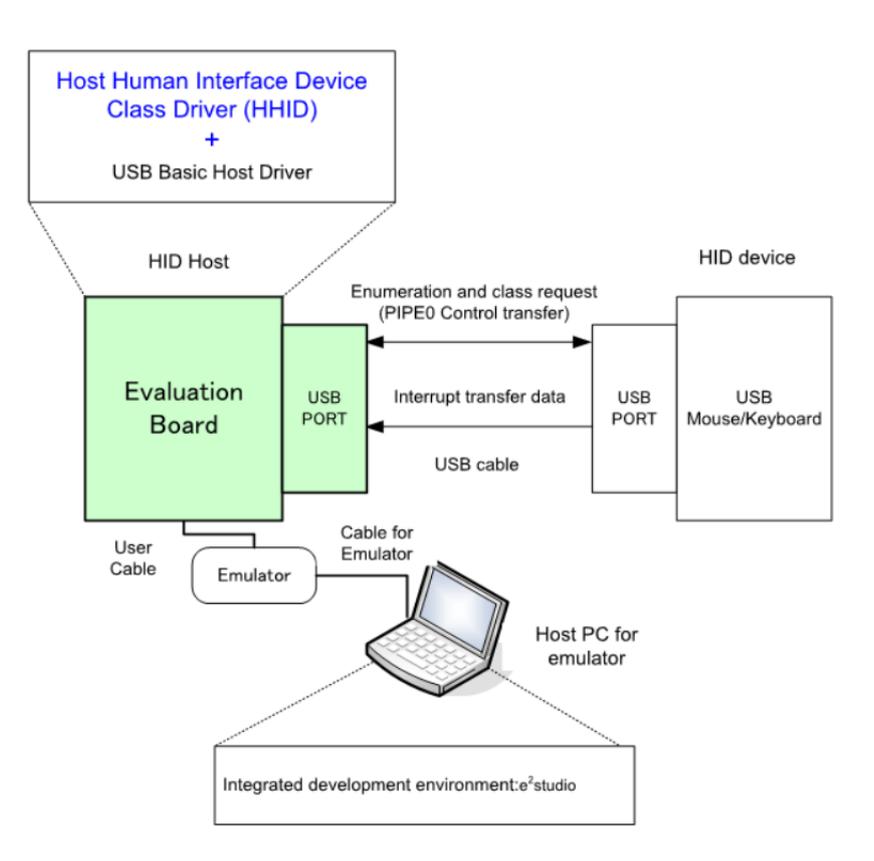


Figure 174: Example Operating Environment

### Application Processing (for RTOS)

The main loop performs processing to receive data from the HID device as part of the main routine. An overview of the processing performed by the loop is shown below.

1. When a USB-related event has completed, the USB driver calls the callback function (`usb_apl_callback`). In the callback function (`usb_apl_callback`), the application task (APL) is notified of the USB completion event using the real-time OS functionality.
2. In APL, information regarding the USB completion event was notified from the callback function is retrieved using the real-time OS functionality.
3. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STATUS_CONFIGURED`, APL sends the class request (`SET_PROTOCOL`) to the HID device.
4. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STATUS_REQUEST_COMPLETE`, APL performs a data reception request to receive data transmitted from the HID device by calling the `R_USB_Read` function.
5. The above processing is repeated.

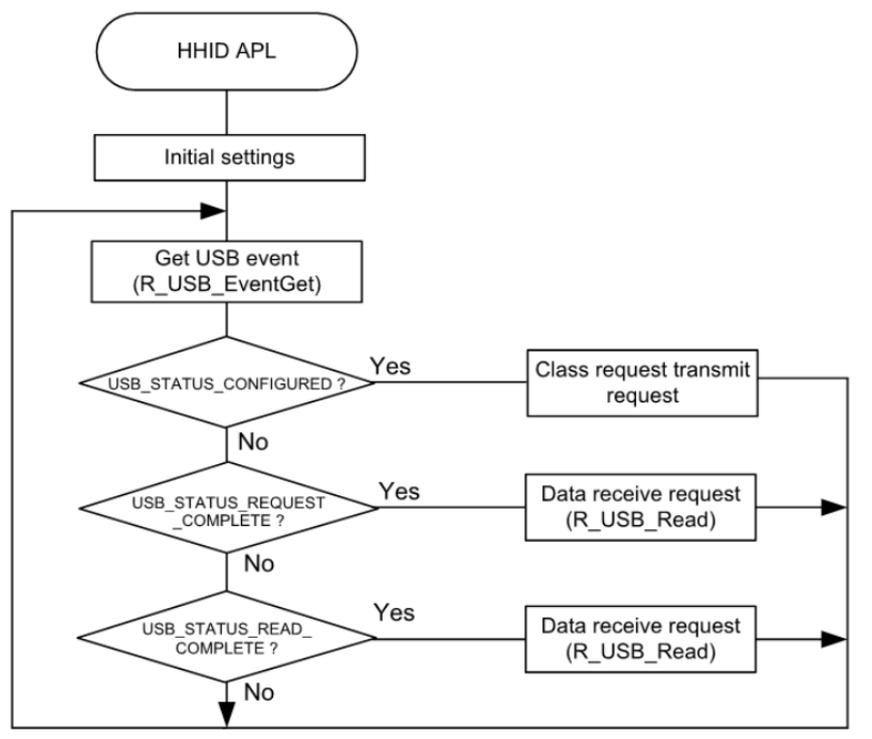


Figure 175: Main Loop (Normal mode)

### Application Processing (for Non-OS)

The main loop performs processing to receive data from the HID device as part of the main routine. An overview of the processing of the main loop is presented below.

1. When the R\_USB\_GetEvent function is called after an HID device attaches to the USB host and enumeration completes, USB\_STATUS\_CONFIGURED is set as the return value. When the APL confirms USB\_STATUS\_CONFIGURED, it calls the R\_USB\_Write function to request transmission of data to the HID device.
2. When the R\_USB\_GetEvent function is called after sending of class request SET\_PROTOCOL to the HID device has completed, USB\_STATUS\_REQUEST\_COMPLETE is set as the return value. When the APL confirms USB\_STATUS\_REQUEST\_COMPLETE, it calls the R\_USB\_Read function to make a data receive request for data sent by the HID device.
3. When the R\_USB\_GetEvent function is called after reception of data from the HID device has completed, USB\_STATUS\_READ\_COMPLETE is set as the return value. When the APL confirms USB\_STATUS\_READ\_COMPLETE, it calls the R\_USB\_Read function to make a data receive request for data sent by the HID device.
4. The processing in step 3, above, is repeated.

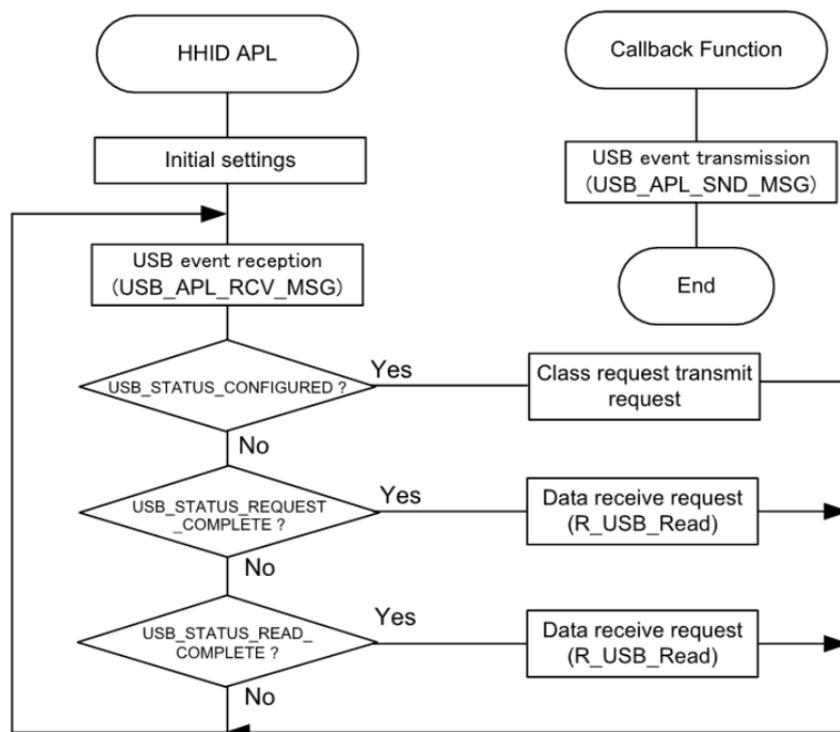


Figure 176: Main Loop (Normal mode)

```

/*****
 * Macro definitions
 *****/
#define SET_PROTOCOL (USB_HID_SET_PROTOCOL | USB_HOST_TO_DEV | USB_CLASS |
USB_INTERFACE)
#define BOOT_PROTOCOL (0)
#define USB_FS_DEVICE_ADDRESS_1 (1)
/*****
 * Private global variables and functions
 *****/
static const usb_hhid_api_t g_hhid_on_usb =
{
    .typeGet          = R_USB_HHID_TypeGet,
    .maxPacketSizeGet = R_USB_HHID_MaxPacketSizeGet,
};
/*****
 * Function Name : r_usb_hhid_example
 * Description : Host HID application main process
 *****/

```

```
* Arguments : none
* Return value : none
*****/
static void r_usb_hhid_example (void)
{
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
#endif /* (BSP_CFG_RTOS == 2) */
    usb_status_t      event;
    usb_event_info_t event_info;
    uint16_t          offset = 0;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
#if (BSP_CFG_RTOS == 2)
        USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
        event_info = *p_mess;
        event      = event_info.event;
#else /* (BSP_CFG_RTOS == 2) */
        g_usb_on_usb.eventGet(&event_info, &event); /* Get event code */
#endif /* (BSP_CFG_RTOS == 2) */
        switch (event)
        {
        case USB_STATUS_CONFIGURED:
            {
                g_hhid_on_usb.typeGet(&g_basic0_ctrl, &g_hid_type,
USB_FS_DEVICE_ADDRESS_1);
                g_hhid_on_usb.maxPacketSizeGet(&g_basic0_ctrl, &g_mxps, USB_HID_IN,
USB_FS_DEVICE_ADDRESS_1);
                /* Send the HID request (SetProtocol) to HID device */
                set_protocol(&g_basic0_ctrl, BOOT_PROTOCOL, USB_FS_DEVICE_ADDRESS_1);
                break;
            }
        case USB_STATUS_READ_COMPLETE:
```

```

        {
            offset = hid_memcpy(g_store_buf, g_buf, offset, g_mxps);
            g_usb_on_usb.read(&g_basic0_ctrl, g_buf, (uint32_t) g_mxps,
USB_FS_DEVICE_ADDRESS_1);
        }
        break;
    }
    case USB_STATUS_REQUEST_COMPLETE:
        {
            if (USB_HID_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
                {
                    g_usb_on_usb.read(&g_basic0_ctrl, g_buf, (uint32_t) g_mxps,
USB_FS_DEVICE_ADDRESS_1);
                }
            break;
        }
    default:
        {
            break;
        }
    }
}
} /* End of function usb_main */
/*****
* Function Name : set_protocol
* Description : Sending SetProtocol request to HID device
* Arguments : usb_ctrl_t *p_ctrl : Pointer to usb_instance_ctrl_t structure.
* : uint8_t ptorocol: Protocol Type
* : uint8_t device_address: Device address that sends this request
* Return value : none
*****/
static void set_protocol (usb_instance_ctrl_t * p_ctrl, uint8_t protocol, uint8_t
device_address)
{
    usb_setup_t setup;

```

```

    setup.request_type    =
SET_PROTOCOL; /*
bRequestCode:SET_PROTOCOL, bmRequestType */
    setup.request_value =
protocol; /* wValue: Protocol
Type */
    setup.request_index =
0x0000; /* wIndex:Interface */
    setup.request_length =
0x0000; /* wLength:Zero */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, (uint8_t *) &g_setup_data,
device_address); /* Request Control transfer */
} /* End of function set_protocol */
/*****
* Function Name : hid_memcpy
* Description : Copy received hhid data to the application buffer
* Arguments : uint8_t *p_dest : Pointer to application buffer
* : uint8_t *p_src : Pointer to received buffer
* : uint16_t offset : Application buffer offset
* : uint16_t size : Size of received hhid data
* Return value : uint16_t offset + i: Offset
*****/
static uint16_t hid_memcpy (uint8_t * p_dest, uint8_t * p_src, uint16_t offset,
uint16_t size)
{
    uint16_t i;
    for (i = 0; i < size; i++)
    {
        if ((offset + i) == BUFSIZE)
        {
            offset = 0;
        }
        *(p_dest + offset + i) = *(p_src + i);
    }
}

```

```
return (uint16_t) (offset + i);
} /* End of function hid_memcpy */
```

## Function Documentation

### ◆ R\_USB\_HHID\_TypeGet()

```
fsp_err_t R_USB_HHID_TypeGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_type, uint8_t device_address )
```

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.)

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

### ◆ R\_USB\_HHID\_MaxPacketSizeGet()

```
fsp_err_t R_USB_HHID_MaxPacketSizeGet ( usb_ctrl_t *const p_api_ctrl, uint16_t * p_size, uint8_t direction, uint8_t device_address )
```

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT).

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

## 4.2.56 USB Host Mass Storage Class Driver (r\_usb\_hmsc)

### Modules

#### Functions

```
fsp_err_t R_USB_HMSC_StorageCommand (usb_ctrl_t *const p_api_ctrl, uint8_t
```

\*buf, uint8\_t command, uint8\_t destination)

Processing for MassStorage(ATAPI) command. [More...](#)

fsp\_err\_t R\_USB\_HMSC\_DriveNumberGet (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_drive, uint8\_t destination)

Get number of Storage drive. [More...](#)

fsp\_err\_t R\_USB\_HMSC\_SemaphoreGet (void)

Get a semaphore. (RTOS only) [More...](#)

fsp\_err\_t R\_USB\_HMSC\_SemaphoreRelease (void)

Release a semaphore. (RTOS only) [More...](#)

fsp\_err\_t R\_USB\_HMSC\_StorageReadSector (uint16\_t drive\_number, uint8\_t \*const buff, uint32\_t sector\_number, uint16\_t sector\_count)

Read sector information. [More...](#)

fsp\_err\_t R\_USB\_HMSC\_StorageWriteSector (uint16\_t drive\_number, uint8\_t const \*const buff, uint32\_t sector\_number, uint16\_t sector\_count)

Write sector information. [More...](#)

## Detailed Description

This module provides a USB Host Mass Storage Class (HMSC) driver. It implements the [USB HMSC Interface](#).

## Overview

The r\_usb\_hmsc module, when used in combination with the r\_usb\_basic module, operates as a USB Host Mass Storage Class (HMSC) driver. It is built on the USB Mass Storage Class Bulk-Only Transport (BOT) protocol. It is possible to communicate with BOT-compatible USB storage devices by combining this module with a file system and storage device driver.

### Note

*This module should be used in combination with the FreeRTOS+FAT File System.*

## Features

The r\_usb\_hmsc module has the following key features:

- Checking of connected USB storage devices to determine whether or not operation is supported

- Storage command communication using the BOT protocol
- Support for SFF-8070i (ATAPI) USB mass storage subclass
- Sharing of a single pipe for IN/OUT directions or multiple devices
- Supports up to 4 connected USB storage devices

## Class Requests

The class requests supported by this driver are shown below.

Request	Description
GetMaxLun	Gets the maximum number of units that are supported.
MassStorageReset	Cancels a protocol error.

## Storage Commands

This driver supports the following storage commands:

- TEST\_UNIT\_READY
- MODE\_SELECT10
- MODE\_SENSE10
- PREVENT\_ALLOW
- READ\_FORMAT\_CAPACITY
- READ10
- WRITE10

## Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Warning

Due to the wide variety of USB mass storage device implementations, this driver is not guaranteed to work with all devices. When implementing the driver it is important to verify correct operation with the mass storage devices that the end user is expected to use.

### Multi Port

This driver supports simultaneous operation with Peripheral Communication Device Class(PCDC). If the user are using MCU that supports 2 USB modules, such as RA6M3, the user can run HMSC on one USB module and PCDC on the other. This driver does not support simultaneous operation using device classes other than PCDC.

## For Bare Metal

1. To use FreeRTOS+FAT without FreeRTOS, copy FreeRTOSConfigMinimal.h to one of your project's include paths and rename it FreeRTOSConfig.h.
2. In RA configurator, enter the appropriate values in the Main stack size and Heap size fields. The figure below is an example of the RA6M3-EK board.

RA Common	
Main stack size (bytes)	0x800
Heap size (bytes)	0x800
MCU Vcc (mV)	3300
Parameter checking	Disabled
Assert Failures	Return FSP_ERR_ASSERTION
Error Log	No Error Log
Soft Reset	Disabled
Main Oscillator Populated	Populated
PFS Protect	Enabled
C Runtime Initialization	Enabled
Main Oscillator Clock Source	Crystal or Resonator
Subclock Populated	Populated
Subclock Drive (Drive capac	Standard/Normal mode
Subclock Stabilization Time	1000

Figure 177: BSP Setting

1. In the Bare Metal version, specify "NULL" in the Callback item.

The image shows a screenshot of the RA configurator interface. On the left, there is a tree view of modules. The 'FreeRTOS+FAT Port for RA' module is selected. On the right, the 'API Info' panel is open, showing the configuration for this module. The 'Callback' field is highlighted with a red box and contains the value 'NULL'.

API Info	
Common	Default (BSP)
Parameter Checking	Default (BSP)
Module FreeRTOS+FAT Port for RA	
Name	g_rm_freertos_plus_fat0
Total Number of Sectors	31293440
Sector Size (bytes)	512
Cache Size (bytes)	1024
Partition Number	0
Callback	NULL

Figure 178: For Bare Metal Setting

## Limitations

1. Some MSC devices may be unable to connect because they are not recognized as storage devices.
2. MSC devices that return values of 1 or higher in response to the GetMaxLun command (mass storage class command) are not supported.
3. A maximum of 4 USB storage devices can be connected.
4. Only USB storage devices with a sector size of 512 bytes can be connected.
5. A device that does not respond to the READ\_CAPACITY command operates as a device with a sector size of 512 bytes.
6. The continuous transfer mode cannot be used when using DMA.
7. This module must be incorporated into a project using r\_usb\_basic and does not provide any public APIs.
8. This driver does not support Low-speed.

## Examples

### USB HMSC Example

#### Example Operating Environment

The following shows an example operating environment for the HMSC.



functionality.

4. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STS_CONFIGURED` then, based on the USB completion event, the MSC device is mounted and the file is written to the MSC device.
5. If the USB completion event (the event member of the `usb_ctrl_t` structure) retrieved in step 2 above is `USB_STS_DETACH`, the application initializes the variables for state management.

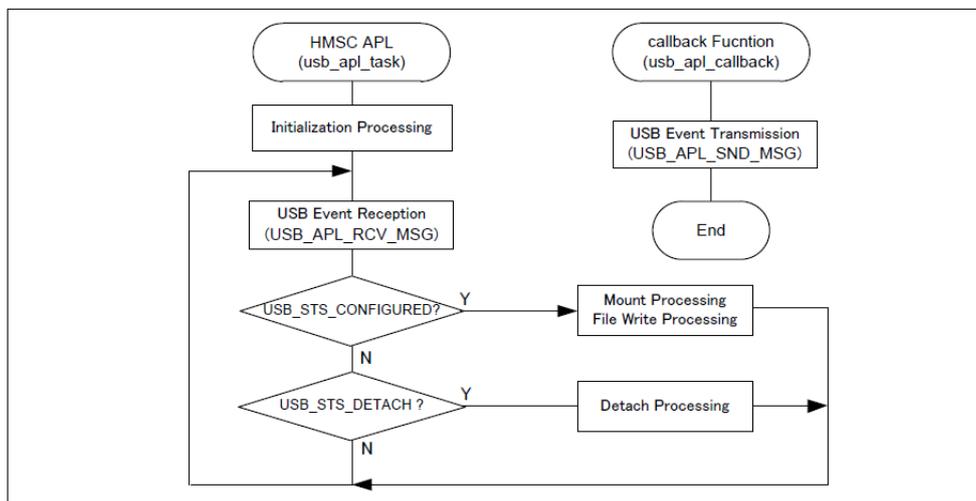


Figure 180: `usb_apl_task`

## file\_read\_task

Of the application tasks `usb_apl_task` and `file_read_task`, `file_read_task` is processed while `usb_apl_task` is in the wait state. This task performs file read processing on the file that was written to the MSC device.

## Example Code

```

#define RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME "TEST_FILE.txt"
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES (10240)
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER (0)
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_SUPPORT_USB

typedef enum
{
    STATE_ATTACH, STATE_DATA_READY, STATE_DATA_WRITE, STATE_FILE_READ, STATE_DETACH,
    STATE_ERROR,
} state_t;

extern rm_freertos_plus_fat_instance_ctrl_t g_rm_freertos_plus_fat0_ctrl;
extern const rm_freertos_plus_fat_cfg_t g_rm_freertos_plus_fat0_cfg;
// @extern const rm_freertos_plus_fat_disk_cfg_t g_rm_freertos_plus_fat0_disk_cfg;
uint8_t g_file_data[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
  
```

```
uint8_t g_read_buffer[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
static uint16_t g_state = STATE_DETACH;
void usb_hmsc_baremetal_example (void)
{
    uint16_t i;
    uint16_t k;
    fsp_err_t err;
    FF_FILE * pxSourceFile;
    FF_Disk_t disk;
    rm_freertos_plus_fat_device_t device;
    usb_status_t event;
    usb_event_info_t event_info;
    FF_Error_t ff_err;
    size_t size_return;
    int close_err;
    rm_block_media_usb_instance_ctrl_t * p_instance_ctrl;
    for (i = 0; i < RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES; i++)
    {
        g_file_data[i] = (uint8_t) i;
    }
    /* Open media driver.*/
    RM_FREERTOS_PLUS_FAT_Open(&g_rm_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat0_cfg);
    /* When using USB media, enable RM_FREERTOS_PLUS_FAT_EXAMPLE_SUPPORT_USB macro. */
    #ifdef RM_FREERTOS_PLUS_FAT_EXAMPLE_SUPPORT_USB
    while (1)
    {
        g_usb_on_usb.eventGet(&event_info, &event);
        switch (event)
        {
        case USB_STATUS_CONFIGURED:
            {
                /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
```

```
* RM_FREERTOS_PLUS_FAT_MediaInit. */
    p_instance_ctrl          = event_info.p_context;
    p_instance_ctrl->device_address = event_info.device_address;
    RM_FREERTOS_PLUS_FAT_MediaInit(&g_rm_freertos_plus_fat0_ctrl, &device);
/* Initialize one disk for each partition used in the application. */
    RM_FREERTOS_PLUS_FAT_DiskInit(&g_rm_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat0_disk_cfg, &disk);
/* Mount each disk. This assumes the disk is already partitioned and formatted. */
    FF_Mount(&disk, RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);
/* Add the disk to the file system. */
    FF_FS_Add("/", &disk);
/* Open a source file for writing. */
    pxSourceFile = ff_fopen((const char *)
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "w");
/* Write file data. */
    ff_fwrite(g_file_data, sizeof(g_file_data), 1, pxSourceFile);
/* Close the file. */
    ff_fclose(pxSourceFile);
    g_state = STATE_FILE_READ;

break;
    }
case USB_STATUS_DETACH:
    {
        g_state = STATE_DETACH;
        RM_FREERTOS_PLUS_FAT_DiskDeinit(&g_rm_freertos_plus_fat0_ctrl, &disk);
break;
    }
default:
    {
break;
    }
    }

if (STATE_FILE_READ == g_state)
    {
```

```

        pxSourceFile = ff_fopen((const char *)
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "r");
    for (k = 0; k < RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES; k++)
        {
            g_read_buffer[k] = (uint8_t) 0;
        }
    /* Read file data. */
    size_return = ff_fread(g_read_buffer, sizeof(g_file_data), 1,
pxSourceFile);
    /* Close the file. */
    close_err = ff_fclose(pxSourceFile);
    }
}
#endif
}

```

## Function Documentation

### ◆ R\_USB\_HMSC\_StorageCommand()

`fsp_err_t R_USB_HMSC_StorageCommand ( usb_ctrl_t *const p_api_ctrl, uint8_t * buf, uint8_t command, uint8_t destination )`

Processing for MassStorage(ATAPI) command.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_HMSSC\_DriveNumberGet()**

```
fsp_err_t R_USB_HMSSC_DriveNumberGet ( usb_ctrl_t *const p_api_ctrl, uint8_t * p_drive, uint8_t destination )
```

Get number of Storage drive.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

◆ **R\_USB\_HMSSC\_SemaphoreGet()**

```
fsp_err_t R_USB_HMSSC_SemaphoreGet ( void )
```

Get a semaphore. (RTOS only)

If this function is called in the OS less execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.

◆ **R\_USB\_HMSSC\_SemaphoreRelease()**

```
fsp_err_t R_USB_HMSSC_SemaphoreRelease ( void )
```

Release a semaphore. (RTOS only)

If this function is called in the OS less execution environment, a failure is returned.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.

### ◆ R\_USB\_HMSC\_StorageReadSector()

```
fsp_err_t R_USB_HMSC_StorageReadSector ( uint16_t drive_number, uint8_t *const buff, uint32_t
sector_number, uint16_t sector_count )
```

Read sector information.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

#### Note

The address specified in the argument *buff* must be 4-byte aligned.

### ◆ R\_USB\_HMSC\_StorageWriteSector()

```
fsp_err_t R_USB_HMSC_StorageWriteSector ( uint16_t drive_number, uint8_t const *const buff,
uint32_t sector_number, uint16_t sector_count )
```

Write sector information.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_USB_FAILED	The function could not be completed successfully.
FSP_ERR_ASSERTION	Parameter Null pointer error.
FSP_ERR_USB_PARAMETER	Parameter error.

#### Note

The address specified in the argument *buff* must be 4-byte aligned.

## 4.2.57 USB Host Vendor Class (r\_usb\_hvnd)

### Modules

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

## Overview

USB Host Vendor class works by combining r\_usb\_basic module.

## How to Configuration

The following shows FSP configuration procedure for USB Host Vendor class.

- Select [New Stack]->[Middleware]->[USB]->[USB Host Vendor class driver on r\_usb\_hvnd].

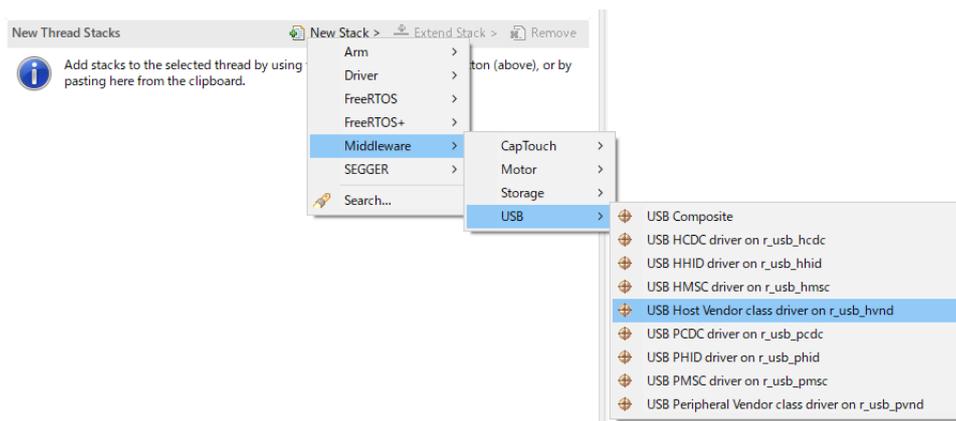


Figure 181: Select USB Host Vendor Class

- The following is displayed when selecting [USB Host Vendor class driver on r\_usb\_hvnd]. The user does not specify USB pipe number in Vendor class.

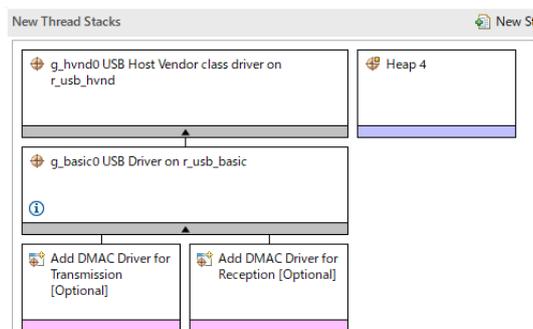


Figure 182: USB Host Vendor Class Stack

## API

Use the following APIs in Host Vendor class application program.

- For Data Transfer  
Use the following APIs for data transfer for Bulk transfer or Interrupt transfer.

1. R\_USB\_PipeRead()
2. R\_USB\_PipeWrite()

### 3. R\_USB\_PipeStop()

- For Control Transfer  
Use the following API for the class request processing.

#### 1. R\_USB\_HostControlTransfer()

- For USB Pipe Information  
The USB driver allocates USB PIPE by analyzing the descriptor of USB device in Vendor class. Use the following APIs to get the allocated USB pipe information.

1. R\_USB\_UsedPipesGet()
2. R\_USB\_PipeInfoGet()

## USB PIPE Allocation

The USB driver allocates USB PIPE by analyzing the descriptor of USB device in Vendor class. The USB PIPE related to the Endpoint Descriptor are allocated in order from USB PIPE1 according to the description order of the Endpoint Descriptor.

## Examples

This application program processes the following after the enumeration completes with USB device.

1. Getting USB Pipe Information
2. Vendor Class Request Processing
3. Loopback processing of bulk transfer and interrupt transfer.

```

/*****
**
* Macro definitions
*****
**/

/* for Vendor Class Request */
#define USB_SET_VENDOR_NO_DATA (0x0000U)
#define USB_SET_VENDOR (0x0100U)
#define USB_GET_VENDOR (0x0200U)
#define SET_VENDOR_NO_DATA (USB_SET_VENDOR_NO_DATA | USB_HOST_TO_DEV |
USB_VENDOR | USB_INTERFACE)
#define SET_VENDOR (USB_SET_VENDOR | USB_HOST_TO_DEV | USB_VENDOR |
USB_INTERFACE)
#define GET_VENDOR (USB_GET_VENDOR | USB_DEV_TO_HOST | USB_VENDOR |
USB_INTERFACE)

/*****
**

```

```

* Function Name : usb_main
* Description : main routine or task for host vendor class application.
* Arguments : none:
* Return value : none
*****
**/
void main_task (void)
{
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
#endif

    usb_status_t    event;

    usb_event_info_t event_info;

    uint8_t         bulk_out_pipe = 0; /* Bulk Out Pipe      */
    uint8_t         bulk_in_pipe  = 0; /* Bulk In Pipe       */
    uint8_t         int_out_pipe  = 0; /* Interrupt Out Pipe */
    uint8_t         int_in_pipe   = 0; /* Interrupt In Pipe  */

    uint16_t        buf_type = 0;

    uint8_t         pipe          = 0;

    uint8_t         is_zlp[2] = {0, 0};

    uint16_t        used_pipe = 0;

    usb_pipe_t      pipe_info;

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);

    while (1)
    {
#if (BSP_CFG_RTOS == 2)
        USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);

        event_info = *p_mess;

        event      = event_info.event;
#else /* (BSP_CFG_RTOS == 2) */
        g_usb_on_usb.eventGet(&event_info, &event);
#endif /* (BSP_CFG_RTOS == 2) */

        switch (event)
        {

```

```
case USB_STATUS_CONFIGURED:
{
    buffer_init();
    is_zlp[0] = 0;
    is_zlp[1] = 0;
    /* Get USB Pipe Information */
    g_usb_on_usb.usedPipesGet(&g_basic0_ctrl, &used_pipe,
ADDRESS1);
    for (pipe = START_PIPE; pipe < END_PIPE; pipe++)
    {
        if ((used_pipe & (1 << pipe)) != 0)
        {
            g_usb_on_usb.pipeInfoGet(&g_basic0_ctrl, &pipe_info,
pipe);
            if (USB_EP_DIR_IN != (pipe_info.endpoint & USB_EP_DIR_IN))
            {
                /* Out Transfer */
                if (USB_TRANSFER_TYPE_BULK == pipe_info.transfer_type)
                {
                    buf_type      = BUF_BULK;
                    bulk_out_pipe = pipe;
                }
            }
            else
            {
                buf_type      = BUF_INT;
                int_out_pipe = pipe;
            }
        }
    }
    else
    {
        /* In Transfer */
        if (USB_TRANSFER_TYPE_BULK == pipe_info.transfer_type)
        {
            buf_type      = BUF_BULK;
```

```
                bulk_in_pipe = pipe;
            }
else
    {
                buf_type      = BUF_INT;
                int_in_pipe = pipe;
            }
    }
}

/* Send Vendor Class Request */
    class_request_set_vendor_no_data(&g_basic0_ctrl,
event_info.device_address);
break;
    }

case USB_STATUS_READ_COMPLETE:
    {
if (FSP_ERR_USB_FAILED != event_info.status)
    {
if (bulk_in_pipe == event_info.pipe)
    {
                buf_type = BUF_BULK;
                pipe      = bulk_out_pipe;
            }
else if (int_in_pipe == event_info.pipe)
    {
                buf_type = BUF_INT;
                pipe      = int_out_pipe;
            }
else
    {
while (1)
    {
                ;

```

```
        }
    }
    buffer_check(buf_type, event_info.data_size);
    g_usb_on_usb.pipeWrite(&g_basic0_ctrl,
&g_buf[buf_type][0], event_info.data_size, pipe);
    }
break;
    }
case USB_STATUS_WRITE_COMPLETE:
    {
if (bulk_out_pipe == event_info.pipe)
    {
        buf_type = BUF_BULK;
if (1 == is_zlp[buf_type])
    {
        pipe = bulk_in_pipe;
    }
    }
else if (int_out_pipe == event_info.pipe)
    {
        buf_type = BUF_INT;
if (1 == is_zlp[buf_type])
    {
        pipe = int_in_pipe;
    }
    }
else
    {
/* Nothing */
    }
if (1 == is_zlp[buf_type])
    {
        is_zlp[buf_type] = 0;
        buffer_clear(buf_type);
    }
    }
    }
```

```
        g_usb_on_usb.pipeRead(&g_basic0_ctrl, &g_buf[buf_type][0],
BUF_SIZE, pipe);
    }
else
    {
        is_zlp[buf_type] = 1;
        g_usb_on_usb.pipeWrite(&g_basic0_ctrl, 0, 0,
event_info.pipe); /* Send ZLP */
    }
break;
}
case USB_STATUS_REQUEST_COMPLETE:
    {
        if (USB_SET_VENDOR_NO_DATA == (event_info.setup.request_type & USB_BREQUEST
))
        {
            class_request_set_vendor(&g_basic0_ctrl,
event_info.device_address);
        }
        else if (USB_SET_VENDOR == (event_info.setup.request_type & USB_BREQUEST))
        {
            class_request_get_vendor(&g_basic0_ctrl,
event_info.device_address);
        }
        else if (USB_GET_VENDOR == (event_info.setup.request_type & USB_BREQUEST))
        {
            buffer_init();
            /* Bulk Out Transfer */
            g_usb_on_usb.pipeWrite(&g_basic0_ctrl,
&g_buf[BUF_BULK][0], (BUF_SIZE - USB_APL_MXPS),
bulk_out_pipe);
            /* Interrupt Out Transfer */
            g_usb_on_usb.pipeWrite(&g_basic0_ctrl, &g_buf[BUF_INT][0],
(BUF_SIZE - USB_APL_MXPS), int_out_pipe);
```

```
        }

else
    {
        /* Unsupported request */
        }

break;
    }

case USB_STATUS_DETACH:
    {
break;
        }

default:
    {
break;
        }
    }
} /* End of function usb_main */

static void class_request_set_vendor (usb_instance_ctrl_t * p_ctrl, uint8_t
device_address)
{
    usb_setup_t setup;
    uint16_t i;
    for (i = 0; i < REQ_SIZE; i++)
    {
        g_request_buf[i] = (uint8_t) i;
    }

    setup.request_type = SET_VENDOR; /* bRequestCode:SET_VENDOR,
bmRequestType */

    setup.request_value = 0x0000; /* wValue:Zero */
    setup.request_index = 0x0000; /* wIndex:Interface */
    setup.request_length = REQ_SIZE; /* wLength: Data Length */
    /* Request Control transfer */

    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, &g_request_buf[0],
```

```
device_address);
}
static void class_request_set_vendor_no_data (usb_instance_ctrl_t * p_ctrl,
uint8_t device_address)
{
    usb_setup_t setup;
    uint16_t i;
    for (i = 0; i < REQ_SIZE; i++)
    {
        g_request_buf[i] = (uint8_t) i;
    }
    setup.request_type = SET_VENDOR_NO_DATA; /*
bRequestCode:SET_VENDOR_NO_DATA, bmRequestType */
    setup.request_value = 0x0000; /* wValue:Zero */
    setup.request_index = 0x0000; /* wIndex:Interface */
    setup.request_length = 0x0000; /* wLength: Data Length */
    /* Request Control transfer */
    g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, &g_request_buf[0],
device_address);
}
/*****
**
* Function Name : class_request_get_vendor
* Description : Send Vendor Class Request (GET_VENDOR) to USB device.
* Arguments : none
* Return value : none
*****/
static void class_request_get_vendor (usb_instance_ctrl_t * p_ctrl, uint8_t
device_address)
{
    usb_setup_t setup;
    uint16_t i;
    for (i = 0; i < REQ_SIZE; i++)
```

```
{
    g_request_buf[i] = 0;
}

setup.request_type    = GET_VENDOR; /* bRequestCode:GET_VENDOR,
bmRequestType */

setup.request_value   = 0x0000;    /* wValue:Zero */
setup.request_index   = 0x0000;    /* wIndex:Interface */
setup.request_length  = REQ_SIZE;   /* wLength: Data Length */
/* Request Control transfer */

g_usb_on_usb.hostControlTransfer(p_ctrl, &setup, &g_request_buf[0],
device_address);
}

/*****
**
* Function Name : buffer_init
* Description : buffer initialization
* Arguments : none
* Return value : none
*****/
**/

static void buffer_init (void)
{
    uint16_t i;
    uint16_t j;
    for (j = 0; j < 2; j++)
    {
        for (i = 0; i < BUF_SIZE; i++)
        {
            g_buf[j][i] = (uint8_t) i;
        }
    }
}

/*****
**
```

```
* Function Name : buffer_check
* Description : buffer check
* Arguments : buf_type : buffer number
* Return value : none
*****
**/
static void buffer_check (uint16_t buf_type, uint32_t size)
{
    uint16_t i;
    for (i = 0; i < (uint16_t) size; i++)
    {
        if ((uint8_t) (i & USB_VALUE_FF) != g_buf[buf_type][i])
        {
            while (1)
            {
                ;
            }
        }
    }
}
/*****
**
* Function Name : buffer_clear
* Description : buffer clear
* Arguments : buf_type : buffer number
* Return value : none
*****
**/
static void buffer_clear (uint16_t buf_type)
{
    uint16_t i;
    for (i = 0; i < BUF_SIZE; i++)
    {
        g_buf[buf_type][i] = 0;
    }
}
```

```
    }
}
/*****
**
* End of function usb_mcu_init
*****/
**/
#if (BSP_CFG_RTOS == 2)
/*****
**
* Function Name : usb_apl_rec_msg
* Description : Receive a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t** mess : Message pointer
* : usb_tm_t tm : Timeout Value
* Return : uint16_t : USB_OK / USB_ERROR
*****/
**/
usb_er_t usb_apl_rec_msg (uint8_t id, usb_msg_t ** mess, usb_tm_t tm)
{
    BaseType_t err;
    QueueHandle_t handle;
    usb_er_t result;
    (void) tm;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    *mess = NULL;
    err = xQueueReceive(handle, (void *) mess, (portMAX_DELAY));
    if ((pdTRUE == err) && (NULL != (*mess)))
    {
        result = USB_APL_OK;
    }
}
```

```
    }
else
    {
        result = USB_APL_ERROR;
    }
return result;
}

/*****
**
* End of function usb_apl_rec_msg
*****/

**/

/*****
**
* Function Name : usb_apl_snd_msg
* Description : Send a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t* mess : Message pointer
* Return : usb_er_t : USB_OK / USB_ERROR
*****/

**/
usb_er_t usb_apl_snd_msg (uint8_t id, usb_msg_t * mess)
{
    BaseType_t err;
    QueueHandle_t handle;
    usb_er_t result;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    err = xQueueSend(handle, (const void *) &mess, (TickType_t) (0));
    if (pdTRUE == err)
    {

```

```
        result = USB_APL_OK;
    }
else
    {
        result = USB_APL_ERROR;
    }
return result;
}
/*****
**
* End of function usb_apl_snd_msg
*****/
**/
#endif /* #if (BSP_CFG_RTOS == 2) */
```

## 4.2.58 USB Peripheral Communications Device Class (r\_usb\_pcdc)

### Modules

This module provides a USB Peripheral Communications Device Class Driver (PCDC). It implements the [USB PCDC Interface](#).

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

### Detailed Description

## Overview

The r\_usb\_pcdc module combines with the r\_usb\_basic module to provide a USB Peripheral Communications Device Class (PCDC) driver. The PCDC driver conforms to Abstract Control Model of the USB Communications Device Class (CDC) specification and enables communication with a CDC host device.

### Features

The r\_usb\_pcdc module has the following key features:

- Data transfer to and from a USB host
- Response to CDC class requests
- Supports CDC notifications

## Configuration

### Build Time Configurations for r\_usb\_pcdc

The following build time configurations are defined in fsp\_cfg/r\_usb\_pcdc\_cfg.h:

Configuration	Options	Default	Description
Bulk In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Interrupt Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the USB pipe to use for interrupts.

### Configurations for Middleware > USB > USB PCDC driver on r\_usb\_pcdc

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PCDC driver on r\_usb\_pcdc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_pcdc0	Module name.

*Note*

*Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.*

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Abstract Control Model Overview

The Abstract Control Model subclass of CDC is a technology that bridges the gap between USB devices and earlier modems (employing RS-232C connections), enabling use of application programs designed for older modems.

### Class Requests (Host to Peripheral)

This driver notifies the application when receiving the following class requests:

Request	Code	Description
SetLineCoding	0x20	Sets communication line settings (bitrate, data length, parity, and stop bit length)
GetLineCoding	0x21	Acquires the communication line setting state
SetControlLineState	0x22	Set communication line control signals (RTS, DTR)

#### Note

For details concerning the Abstract Control Model requests, refer to Table 11 "Requests - Abstract Control Model" in the "USB Communications Class Subclass Specification for PSTN Devices", Revision 1.2.

### Data Format of Class Requests

The data format of supported class requests is described below:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x21	SET_LINE_CODING (0x20)	0x0000	0x0000	0x0007	<a href="#">usb_pcdc_linecoding_t</a>
0xA1	GET_LINE_CODING (0x21)	0x0000	0x0000	0x0007	<a href="#">usb_pcdc_linecoding_t</a>
0x21	SET_CONTROL_LINE_STATE (0x22)	<a href="#">usb_pcdc_ctrllinestate_t</a>	0x0000	0x0000	None

### Class Notifications (Peripheral to Host)

The following class notifications are supported:

Notification	Code	Description
SERIAL_STATE	0x20	Notification of serial line state

The data types returned are as follows:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0xA1	SERIAL_STATE (0x20)	0x0000	0x0000	0x0002	<a href="#">usb_serial_state_bitmap_t</a>

*Note*

*The host is notified with SERIAL\_STATE whenever a change in the UART port state is detected. This driver will automatically detect overrun, parity and framing errors. A state notification is performed when a transition from normal to error state is detected.*

## Virtual COM-port Usage

When connected to a PC the CDC device can be used as a virtual COM port. After enumeration, the CDC class requests GetLineCoding and SetControlLineState are executed by the target, and the CDC device is registered in Windows Device Manager as a virtual COM device.

Registering the CDC device as a virtual COM-port in Windows Device Manager enables data communication with the CDC device via a terminal app such as PuTTY. When changing settings of the serial port in the terminal application, the UART setting is propagated to the firmware via the class request SetLineCoding.

Data input (or file transmission) from the terminal app window is transmitted to the board using endpoint 2 (EP2); data from the board side is transmitted to the PC using EP1.

When the last packet of data received is the maximum packet size, and the terminal determines that there is continuous data, the received data may not be displayed in the terminal. If the received data is smaller than the maximum packet size, the data received up to that point is displayed in the terminal.

## Multi Port

This driver supports simultaneous operation with Host Mass Storage Class(HMSC). If the user are using MCU that supports 2 USB modules, such as RA6M3, the user can run PCDC on one USB module and HMSC on the other. This driver does not support simultaneous operation using device classes other than HMSC.

## Limitations

- This module must be incorporated into a project using r\_usb\_basic and does not provide any public APIs.
- This driver does not support Low-speed.

# Examples

## USB PCDC Loopback Example

The main functions of the PCDC loopback example are as follows:

1. Receives virtual UART configuration data from the host terminal
2. Loops all other received data back to the host terminal

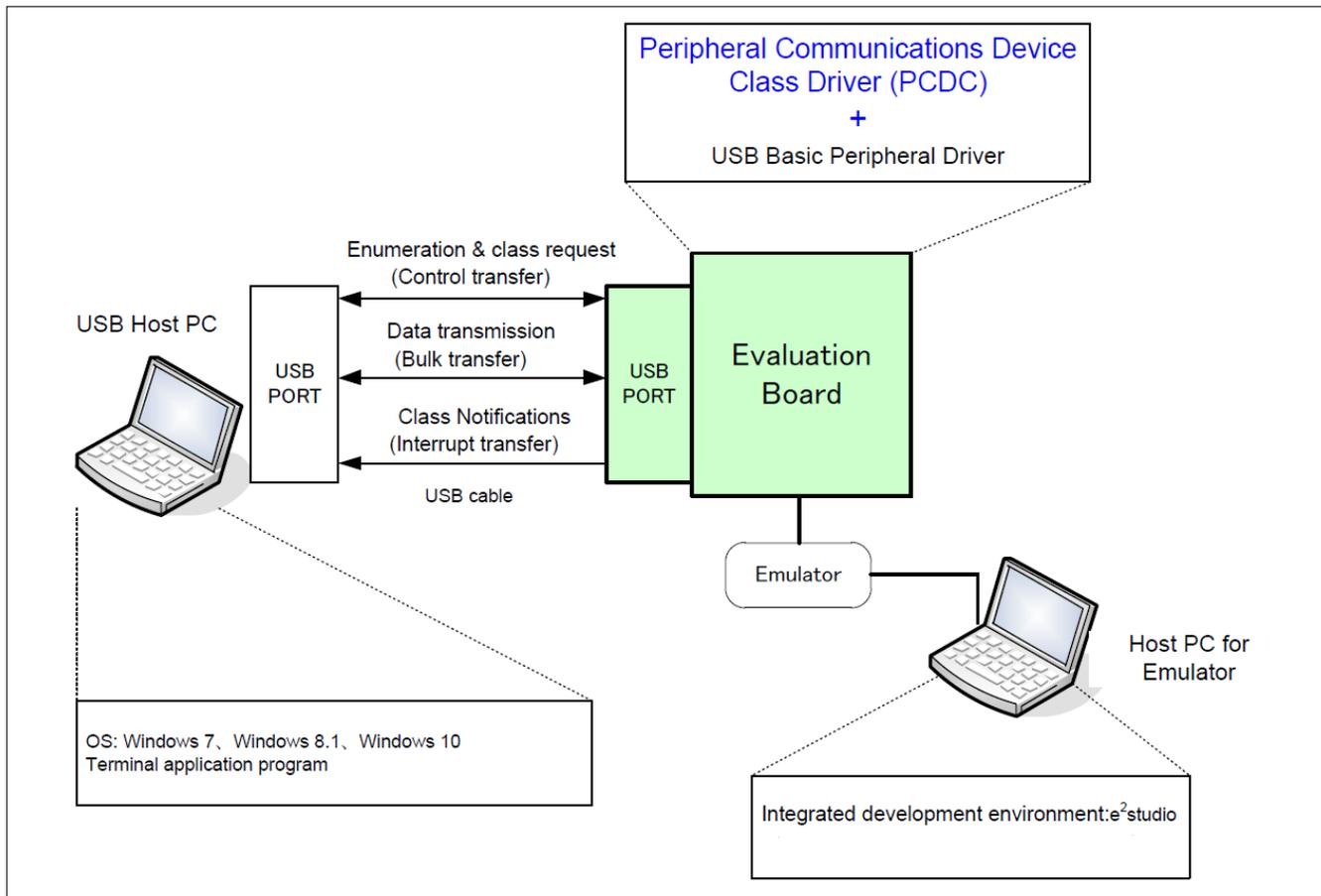


Figure 183: Example Operating Environment

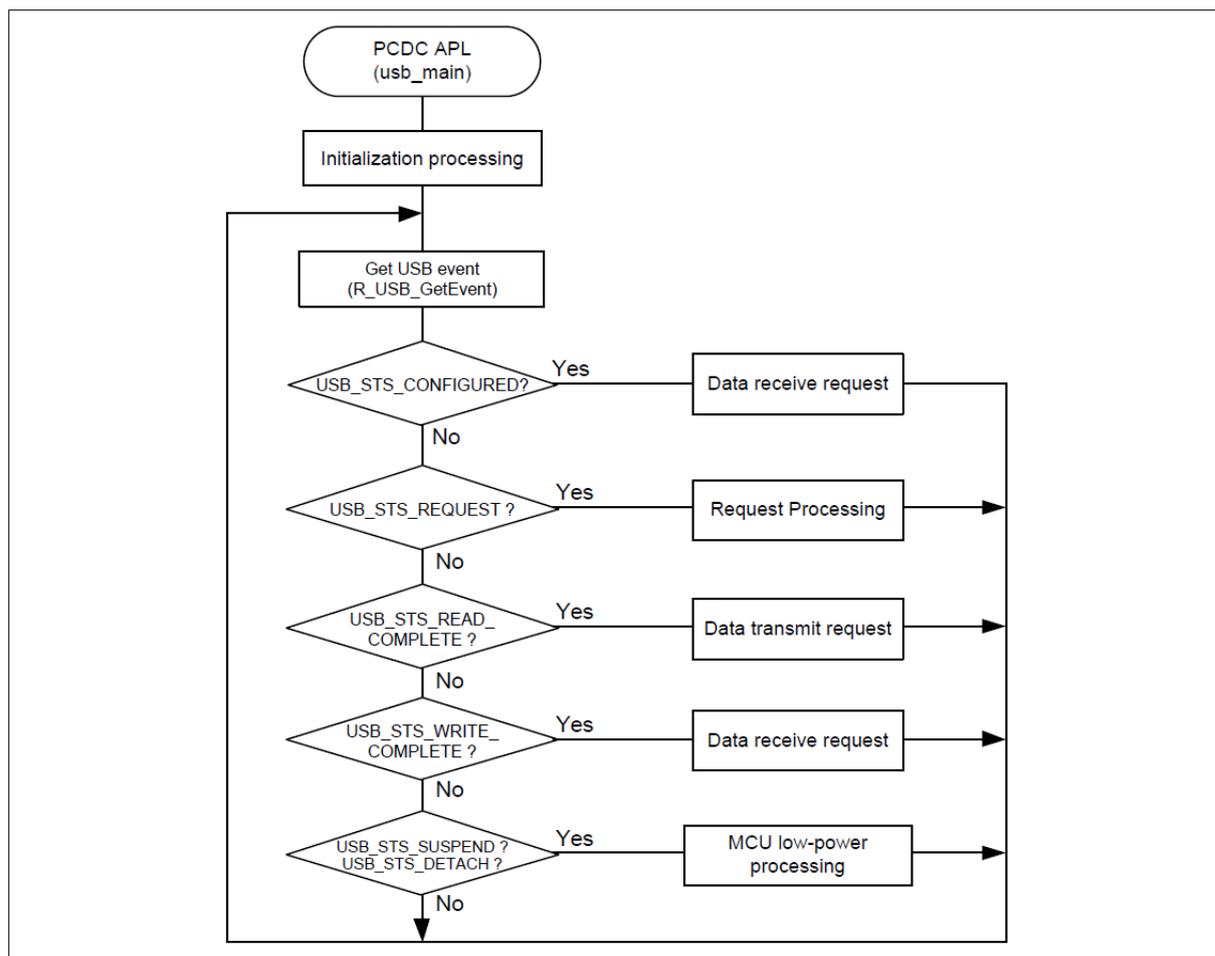


Figure 184: Main Loop processing (Echo mode)

```

void usb_basic_example (void)
{
    usb_event_info_t event_info;
    usb_status_t event;
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
        /* Get USB event data */
        g_usb_on_usb.eventGet(&event_info, &event);
        /* Handle the received event (if any) */
        switch (event)
        {
            case USB_STATUS_CONFIGURED:

```

```
case USB_STATUS_WRITE_COMPLETE:
/* Initialization complete; get data from host */
    g_usb_on_usb.read(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PCDC);
break;
case USB_STATUS_READ_COMPLETE:
/* Loop back received data to host */
    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, event_info.data_size,
USB_CLASS_PCDC);
break;
case USB_STATUS_REQUEST: /* Receive Class Request */
if (USB_PCDC_SET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Configure virtual UART settings */
    g_usb_on_usb.periControlDataGet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
    }
else if (USB_PCDC_GET_LINE_CODING == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Send virtual UART settings back to host */
    g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, (uint8_t *)
&g_line_coding, LINE_CODING_LENGTH);
    }
else
    {
/* ACK all other status requests */
    g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
break;
case USB_STATUS_SUSPEND:
case USB_STATUS_DETACH:
break;
default:
break;
```



## Descriptor

A template for PCDC descriptors can be found in `ra/fsp/src/r_usb_pcdc/r_usb_pcdc_descriptor.c.template`. Also, please be sure to use your vendor ID.

### 4.2.59 USB Peripheral Human Interface Device Class (r\_usb\_phid)

#### Modules

This module is USB Peripheral Human Interface Device Class Driver (PHID). It implements the [USB PHID Interface](#).

#### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (`r_usb_basic`) to be called from the application.

#### Detailed Description

## Overview

The `r_usb_phid` module combines with the `r_usb_basic` module to provide a USB Peripheral Human Interface Device Class (PHID) driver. The PHID driver conforms to the USB Human Interface Device class specifications and implements communication with a HID host.

#### Features

The `r_usb_phid` module has the following functions:

- Data transfer to and from a USB host
- Response to HID class requests
- Response to function references from the HID host

#### Note

*This driver is not guaranteed to provide USB HID operation in all scenarios. The developer must verify correct operation when connected to the targeted USB hosts.*

## Configuration

### Build Time Configurations for r\_usb\_phid

The following build time configurations are defined in fsp\_cfg/r\_usb\_phid\_cfg.h:

Configuration	Options	Default	Description
Interrupt In Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE6	Select the pipe number for input interrupt events.
Interrupt Out Pipe	<ul style="list-style-type: none"> <li>• USB PIPE6</li> <li>• USB PIPE7</li> <li>• USB PIPE8</li> <li>• USB PIPE9</li> </ul>	USB PIPE7	Select the pipe number for output interrupt events.

### Configurations for Middleware > USB > USB PHID driver on r\_usb\_phid

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PHID driver on r\_usb\_phid.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_phid0	Module name.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Class Requests (Host to Peripheral)

This driver notifies the application when receiving the following class requests:

Request	Code	Description
Get_Report	0x01	Receives a report from the HID host
Set_Report	0x09	Sends a report to the HID host
Get_Idle	0x02	Receives a duration (time) from the HID host
Set_Idle	0x0A	Sends a duration (time) to the HID host
Get_Protocol	0x03	Reads a protocol from the HID host
Set_Protocol	0x0B	Sends a protocol to the HID host



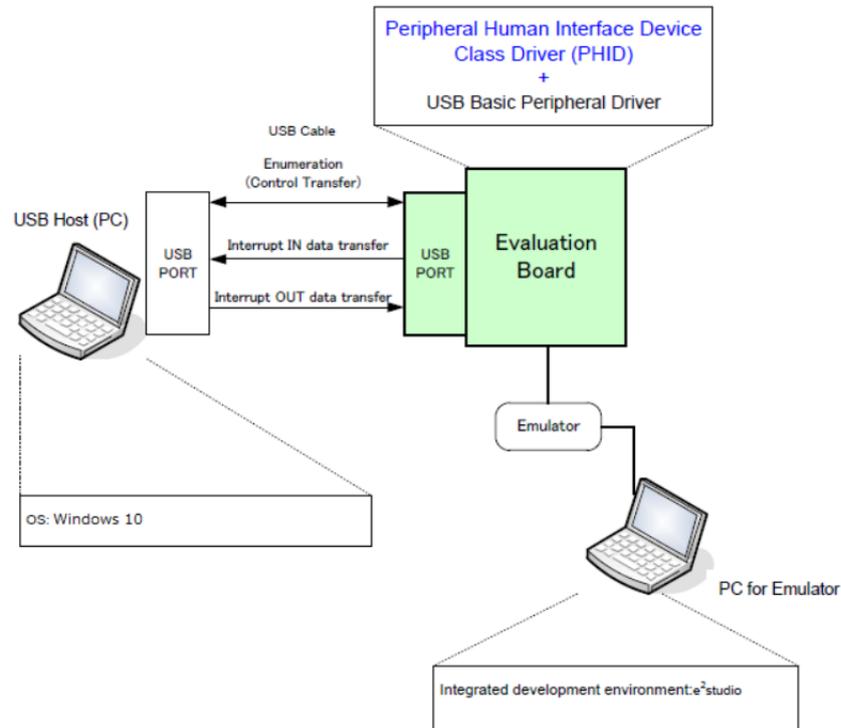


Figure 185: Example Operating Environment

### USB PHID Example (no RTOS)

This is a minimal example for implementing PHID in a non-RTOS application.

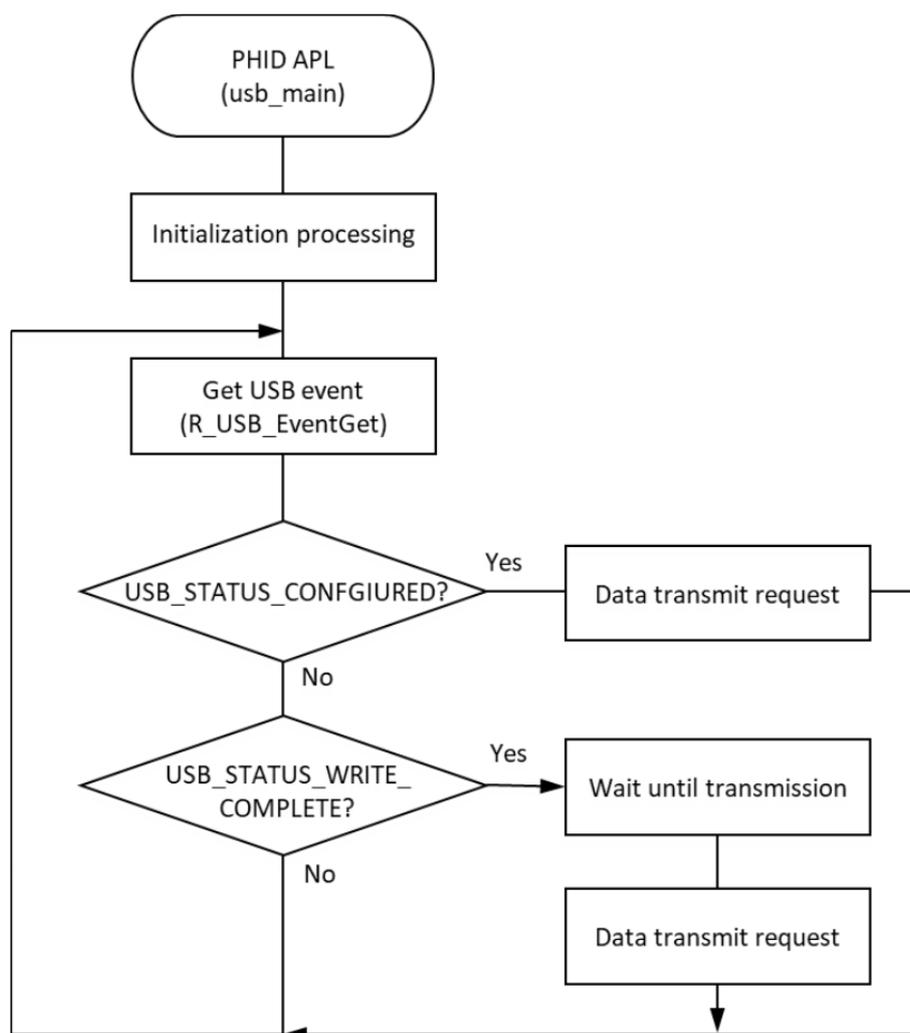


Figure 186: Main Loop processing for non-RTOS example

```

#define USB_RECEIVE_REPORT_DESCRIPTOR (76)
#define USB_RECEIVE_HID_DESCRIPTOR (9)
#define USB_WAIT_1000MS (1000)
#define SW_ACTIVE 0
#define SW_R_PFS->PORT[0].PIN[8].PmnPFS_b.PIDR
#define SW_PDR R_PFS->PORT[0].PIN[8].PmnPFS_b.PDR
#define SW_PMR R_PFS->PORT[0].PIN[8].PmnPFS_b.PMR
static uint8_t g_buf[] = {0, 0, 0, 0, 0, 0, 0, 0}; /* HID data */
static const uint8_t g_zero_data[] = {0, 0, 0, 0, 0, 0, 0, 0}; /* zero data */
static uint16_t g_numlock = 0;
static uint8_t g_idle = 0;
uint8_t          g_remote_wakeup_enable = USB_OFF;
uint8_t          g_status                = NO_WRITING;
  
```

```
/*
 * Function Name : usb_cpu_getkeyno
 * Description : input key port
 * Arguments : none
 * Return value : uint16_t : key_no
 */
uint8_t usb_cpu_getkeyno (void)
{
    uint8_t key_buf = 0;
    if (SW_ACTIVE == SW)
    {
        if (sw_on_count[0] < SW_ON_THRESHOLD)
        {
            sw_on_count[0]++;
        }
    }
    else
    {
        if (sw_on_count[0] >= SW_ON_THRESHOLD)
        {
            key_buf |= SW_PUSH;
        }
        sw_on_count[0] = 0;
    }
    return key_buf;
}

void set_key_data (uint8_t * p_buf)
{
    static uint8_t key_data;
    key_data = KBD_CODE_A;
    *(p_buf + 2) = key_data;
}

void usb_basic_example (void)
{
```

```
usb_event_info_t event_info;

usb_status_t     event;

uint8_t         * p_idle_value;

uint8_t         sw_data;

usb_info_t      info;

fsp_err_t       ret_code = FSP_SUCCESS;

uint8_t         send_data[16] BSP_ALIGN_VARIABLE(4);

g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);

set_key_data(g_buf);

while (1)
{
    g_usb_on_usb.eventGet(&event_info, &event);

switch (event)
{
case USB_STATUS_CONFIGURED:
break;

case USB_STATUS_WRITE_COMPLETE:
if (DATA_WRITING == g_status)
{
    g_status = ZERO_WRITING;
    g_usb_on_usb.write(&g_basic0_ctrl, (uint8_t *) g_zero_data,
DATA_LEN, USB_CLASS_PHID); /* Sending the zero data (8 bytes) */
}

else
{
    g_status = DATA_WRITING;
    usb_cpu_delay_xms(USB_WAIT_1000MS);
    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
}

break;

case USB_STATUS_REQUEST:
/* Receive Class Request */

if (USB_SET_REPORT == (event_info.setup.request_type & USB_BREQUEST))
```

```
{
    g_usb_on_usb.read(&g_basic0_ctrl, (uint8_t *) &g_numlock, 2,
USB_CLASS_PHID); /* Get the NumLock data (NumLock data is not used) */
}
else if (USB_GET_DESCRIPTOR == (event_info.setup.request_type & USB_BREQUEST))
{
    if (USB_GET_REPORT_DESCRIPTOR == event_info.setup.request_value)
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl,
                                        (uint8_t *) g_apl_report,
USB_RECEIVE_REPORT_DESCRIPTOR);
    }
    else if (USB_GET_HID_DESCRIPTOR == event_info.setup.request_value)
    {
        for (uint8_t i = 0; i < USB_RECEIVE_HID_DESCRIPTOR; i++)
        {
            send_data[i] = g_apl_configuration[18 + i];
        }
        /* Configuration Descriptor address set. */
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, send_data,
USB_RECEIVE_HID_DESCRIPTOR);
    }
    else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
}
else if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
{
    /* Get SetIdle value */
    p_idle_value = (uint8_t *) &event_info.setup.request_value;
    g_idle = p_idle_value[1];
}
```

```
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
    else if (USB_GET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, &g_idle, 1);
    }
    else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);

        g_status = DATA_WRITING;

        g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
    }
    else if (USB_GET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    break;
case USB_STATUS_REQUEST_COMPLETE: /* Complete Class Request */
if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];
    }
    else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
```

```
/* None */
    }
else
    {
        g_status = DATA_WRITING;
        g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
    }
break;
case USB_STATUS_SUSPEND:
break;
case USB_STATUS_DETACH:
    g_remote_wakeup_enable = USB_OFF;
break;
default:
break;
    }
    ret_code = g_usb_on_usb.infoGet(&g_basic0_ctrl, &info, NULL);
if (FSP_SUCCESS == ret_code)
    {
        sw_data = usb_cpu_getkeyno();
if (USB_STATUS_SUSPEND == info.device_status)
    {
if (0 != (sw_data & SW_PUSH))
    {
        g_usb_on_usb.remoteWakeup(&g_basic0_ctrl);
    }
    }
    }
}
} /* End of function usb_basic_example() */
```

## USB PHID Example (RTOS)

This is a minimal example for implementing PHID in an RTOS application.

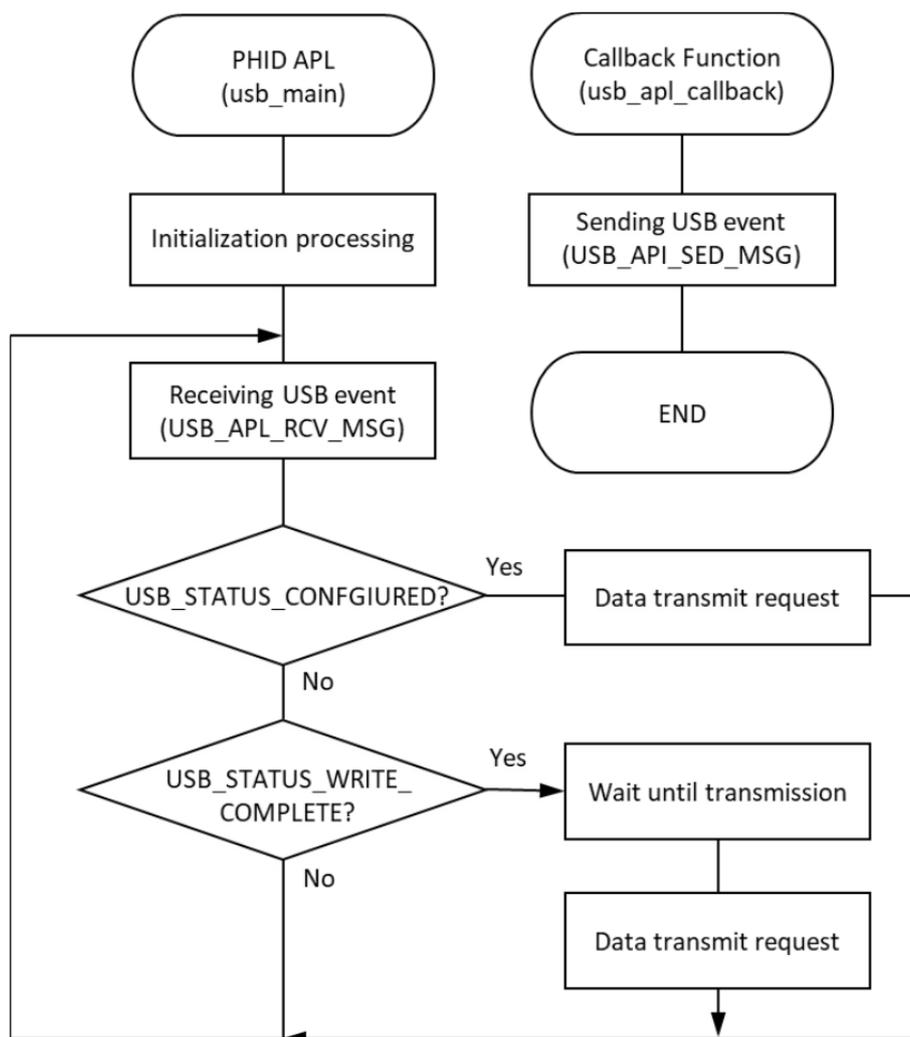


Figure 187: Main Loop processing for RTOS example

```

#define USB_APL_MBX (0)

void usb_apl_callback (usb_event_info_t * p_api_event, usb_hdl_t cur_task,
usb_onoff_t usb_state)
{
    (void) usb_state;
    (void) cur_task;
    USB_APL_SND_MSG(USB_APL_MBX, (usb_msg_t *) p_api_event);
} /* End of function usb_apl_callback */

/*****
* Function Name : usb_apl_rec_msg
* Description : Receive a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t** mess : Message pointer
  
```

```

* : usb_tm_t tm : Timeout Value
* Return : uint16_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_rec_msg (uint8_t id, usb_msg_t ** mess, usb_tm_t tm)
{
    BaseType_t    err;
    QueueHandle_t handle;
    usb_er_t      result;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    *mess = NULL;
    err = xQueueReceive(handle, (void *) mess, (tm));
    if ((pdTRUE == err) && (NULL != (*mess)))
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }
    return result;
}
/*****
* Function Name : usb_apl_snd_msg
* Description : Send a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t* mess : Message pointer
* Return : usb_er_t : USB_OK / USB_ERROR
*****/
usb_er_t usb_apl_snd_msg (uint8_t id, usb_msg_t * mess)
{

```

```
BaseType_t    err;
QueueHandle_t handle;
usb_er_t      result;

if (NULL == mess)
{
return USB_APL_ERROR;
}

handle = (*(g_apl_mbx_table[id]));
err = xQueueSend(handle, (const void *) &mess, (TickType_t) (0));

if (pdTRUE == err)
{
    result = USB_APL_OK;
}
else
{
    result = USB_APL_ERROR;
}

return result;
}

/* RTOS-enabled HID example */
void usb_basic_example_rtos (void)
{
    usb_event_info_t * p_mess;
    usb_event_info_t  event_info;
    uint8_t           * p_idle_value;
    uint8_t           sw_data;
    usb_info_t        info;
    fsp_err_t         ret_code = FSP_SUCCESS;
    uint8_t           send_data[16] BSP_ALIGN_VARIABLE(4);
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    set_key_data(g_buf);

    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
```

```
    USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);

    event_info = *p_mess;

    switch (event_info.event)
    {
    case USB_STATUS_CONFIGURED:
        break;

    case USB_STATUS_WRITE_COMPLETE:
        if (DATA_WRITING == g_status)
        {
            g_status = ZERO_WRITING;
            g_usb_on_usb.write(&g_basic0_ctrl, (uint8_t *) g_zero_data,
DATA_LEN, USB_CLASS_PHID); /* Sending the zero data (8 bytes) */
        }
        else
        {
            g_status = DATA_WRITING;
            usb_cpu_delay_xms(USB_WAIT_1000MS);
            g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);
        }
        break;

    case USB_STATUS_REQUEST:
        /* Receive Class Request */
        if (USB_SET_REPORT == (event_info.setup.request_type & USB_BREQUEST))
        {
            g_usb_on_usb.read(&g_basic0_ctrl, (uint8_t *) &g_numlock, 2,
USB_CLASS_PHID); /* Get the NumLock data (NumLock data is not used) */
        }
        else if (USB_GET_DESCRIPTOR == (event_info.setup.request_type & USB_BREQUEST))
        {
            if (USB_GET_REPORT_DESCRIPTOR == event_info.setup.request_value)
            {
                g_usb_on_usb.periControlDataSet(&g_basic0_ctrl,
                                                (uint8_t *) g_apl_report,
```

```
USB_RECEIVE_REPORT_DESCRIPTOR);
    }
else if (USB_GET_HID_DESCRIPTOR == event_info.setup.request_value)
    {
for (uint8_t i = 0; i < USB_RECEIVE_HID_DESCRIPTOR; i++)
    {
        send_data[i] = g_apl_configuration[18 + i];
    }
/* Configuration Descriptor address set. */
    g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, send_data,
USB_RECEIVE_HID_DESCRIPTOR);
    }
else
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);
    }
    }
else if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
/* Get SetIdle value */
        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_ACK);
    }
else if (USB_GET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl, &g_idle, 1);
    }
else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
```

```
USB_SETUP_STATUS_ACK);

    g_status = DATA_WRITING;

    g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);

    }

else if (USB_GET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {

        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);

    }

else
    {

        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
USB_SETUP_STATUS_STALL);

    }

break;

case USB_STATUS_REQUEST_COMPLETE: /* Complete Class Request */
if (USB_SET_IDLE == (event_info.setup.request_type & USB_BREQUEST))
    {

        p_idle_value = (uint8_t *) &event_info.setup.request_value;
        g_idle = p_idle_value[1];

    }

else if (USB_SET_PROTOCOL == (event_info.setup.request_type & USB_BREQUEST))
    {

/* None */

    }

else
    {

        g_status = DATA_WRITING;

        g_usb_on_usb.write(&g_basic0_ctrl, g_buf, DATA_LEN, USB_CLASS_PHID
);

    }

break;

case USB_STATUS_SUSPEND:
```

```
break;

case USB_STATUS_DETACH:

    g_remote_wakeup_enable = USB_OFF;

break;

default:

break;

    }

    ret_code = g_usb_on_usb.infoGet(&g_basic0_ctrl, &info, NULL);

if (FSP_SUCCESS == ret_code)

    {

        sw_data = usb_cpu_getkeyno();

if (USB_STATUS_SUSPEND == info.device_status)

    {

if (0 != (sw_data & SW_PUSH))

    {

        g_usb_on_usb.remoteWakeup(&g_basic0_ctrl);

    }

    }

    }

}

} /* End of function usb_basic_example_rtos() */
```

## 4.2.60 USB Peripheral Mass Storage Class (r\_usb\_pmsc)

### Modules

This module provides a USB Peripheral Mass Storage Class (PMSC) driver. It implements the [USB PMSC Interface](#).

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

### Detailed Description

## Overview

The r\_usb\_pmsc module combines with the r\_usb\_basic module to provide USB Peripheral It operates as a Mass Storage class driver (hereinafter referred to as PMSC).

The USB peripheral mass storage class driver (PMSC) comprises a USB mass storage class bulk-only transport (BOT) protocol.

When combined with a USB peripheral control driver and media driver, it enables communication with a USB host as a BOT-compatible storage device.

## Features

The r\_usb\_pmsc module has the following key features:

- Storage command control using the BOT protocol
- Supports SFF-8070i (ATAPI)
- Response to mass storage device class requests from a USB host

## Configuration

### Build Time Configurations for r\_usb\_pmsc

The following build time configurations are defined in fsp\_cfg/r\_usb\_pmsc\_cfg.h:

Configuration	Options	Default	Description
Bulk Input Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE1	Select the USB pipe to use for bulk input transfers.
Bulk Output Transfer Pipe	<ul style="list-style-type: none"> <li>• USB PIPE1</li> <li>• USB PIPE2</li> <li>• USB PIPE3</li> <li>• USB PIPE4</li> <li>• USB PIPE5</li> </ul>	USB PIPE2	Select the USB pipe to use for bulk output transfers.
Vendor Information	Vendor Information must be 8 bytes long; pad with spaces if shorter.	Vendor	Specify the vendor information field (part of the Inquiry command response).
Product Information	Product Information must be 16 bytes long; pad with spaces if shorter.	Mass Storage	Specify the product information field (part of the Inquiry command response).
Product Revision Level	Product Revision Level must be 4 bytes long; pad with spaces if shorter.	1.00	Specify the product revision level field (part of the Inquiry command response).
Number of Transfer Sectors	Please enter a number between 1 and 255.	8	Specify the maximum sector size to request with one data transfer.

### Configurations for Middleware > USB > USB PMSC driver on r\_usb\_pmsc

This module can be added to the Stacks tab via New Stack > Middleware > USB > USB PMSC driver on r\_usb\_pmsc.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_pmsc0	Module name.

Refer to the [USB \(r\\_usb\\_basic\)](#) module for hardware configuration options.

### Clock Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

### Pin Configuration

Refer to the [USB \(r\\_usb\\_basic\)](#) module.

## Usage Notes

### Class Requests

The class requests supported by this driver are shown below.

Request	Code	Description
Bulk-Only Mass Storage Reset	0xFF	Resets the connection interface to the mass storage device.
Get Max Logical Unit Number	0xFE	Reports the logical numbers supported by the device.

### Storage Commands

This driver supports the following storage commands.

Command	Code	Description
TEST_UNIT_READY	0x00	Checks the state of the peripheral device.
REQUEST_SENSE	0x03	Gets the error information of the previous storage command execution result.
INQUIRY	0x12	Gets the parameter information of the logical unit.
READ_FORMAT_CAPACITY	0x23	Gets the formattable capacity.
READ_CAPACITY	0x25	Gets the capacity information of the logical unit.
READ10	0x28	Reads data.
WRITE10	0x1A	Writes data.

MODE\_SENSE10

0x5A

Gets the parameters of the logical unit.

*Note*

A *STALL* or *FAIL* error is sent to the host upon receipt of any command not listed in the above table.

**BOT Protocol Overview**

BOT (USB MSC Bulk-Only Transport) is a transfer protocol that encapsulates command, data, and status (results of commands) using only two endpoints (one bulk in and one bulk out). The ATAPI storage commands and the response status are embedded in a Command Block Wrapper (CBW) and a Command Status Wrapper (CSW). The below image shows an overview of how the BOT protocol progresses with command and status data flowing between USB host and peripheral.

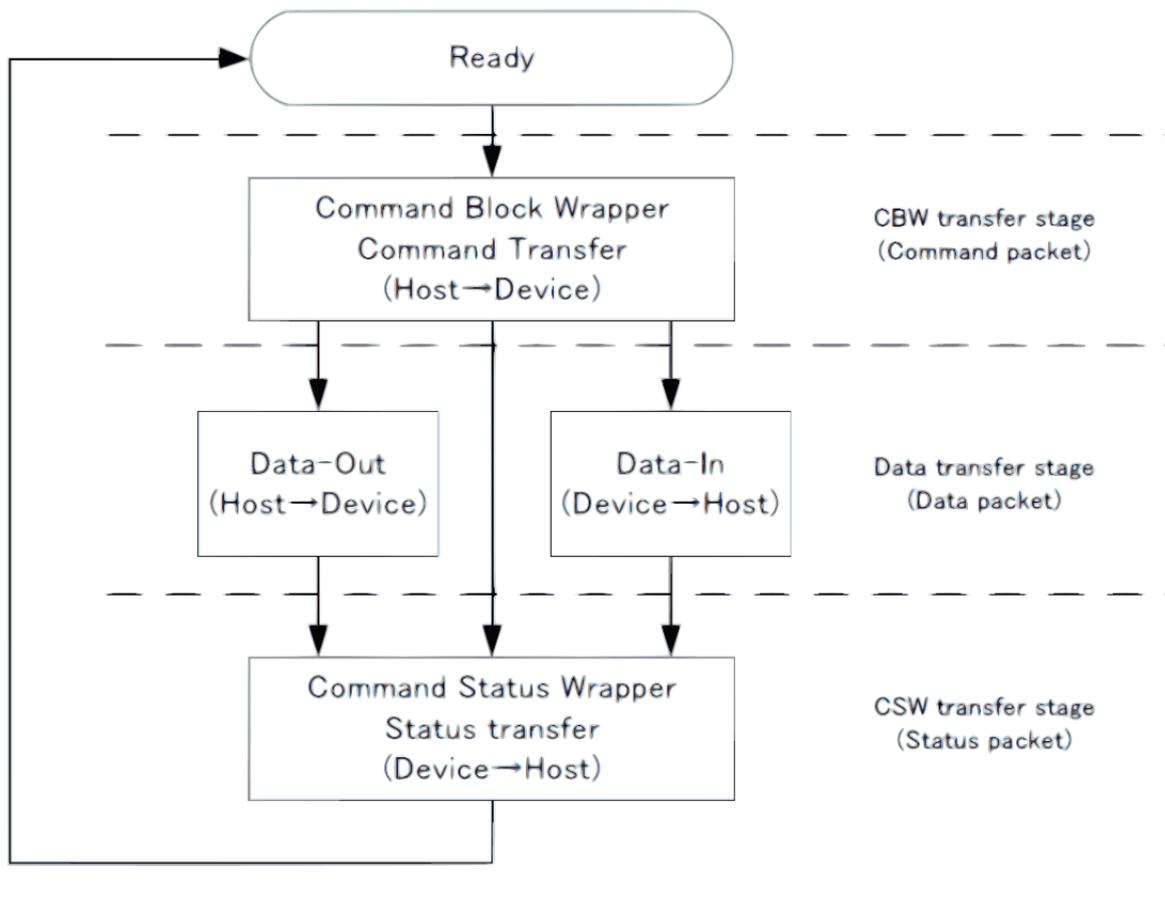


Figure 188: BOT protocol Overview

**Block Media Interface**

PMSC implements a block media interface to enable access to higher-level modules. If the block media interface supports multiple media, users can select any media to access.

*Note*

When the user develops the storage media driver, be sure to define the instance named "g\_rm\_block\_media0".

**Limitations**

1. The driver always returns 0 in response to the GetMaxLun command.
2. The driver supports a sector size of 512 bytes only.
3. The only media currently supported by the block media interface is an SD card. The card must be inserted before initializing the driver.
4. When using DMA for Hi-Speed transfers continuous transfer mode must not be used in the USB Basic driver.
5. The storage area must be formatted before use.
6. When using the SD/MMC Block Media Implementation (rm\_block\_media\_sdmmc), "Card Detection" must be set to "Not Used" in the SD/MMC Host Interface (r\_sdhi) settings.
7. The driver does not support Low-speed.
8. This driver does not support simultaneous operation with USB Host device class.

## Examples

### USB PMSC Example

In this example, when the evaluation board is connected to the host PC it is recognized as a removable disk and reading/writing files is possible. The FAT type is either FAT12, FAT16, or FAT32 depending on the size of the media used.

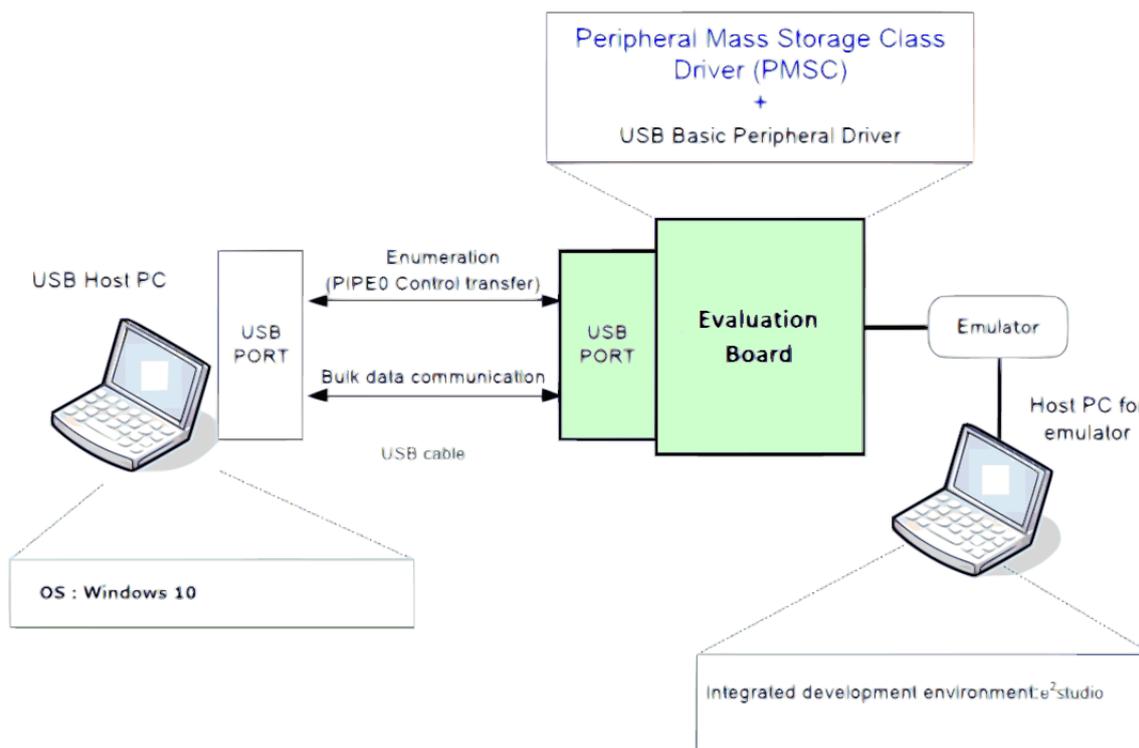


Figure 189: Example Operating Environment

```
void usb_pmsc_example (void)
{
    usb_event_info_t usb_event;
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
```

```
#else
    usb_status_t event;
#endif

    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    /* Loop back between PC(TerminalSoft) and USB MCU */
    while (1)
    {
#if (BSP_CFG_RTOS == 2)
        USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
        usb_event = *p_mess;

        /* Analyzing the received message */
        switch (usb_event.event)
#else /* (BSP_CFG_RTOS == 2) */
        g_usb_on_usb.eventGet(&usb_event, &event);

        switch (event)
#endif /* (BSP_CFG_RTOS == 2) */
        {
            case USB_STATUS_CONFIGURED:
                {
                    break;
                }

            case USB_STATUS_SUSPEND:
            case USB_STATUS_DETACH:
                {

#if USB_SUPPORT_LPW == USB_APL_ENABLE
                // @@ low_power_mcu();
#endif /* USB_SUPPORT_LPW == USB_APL_ENABLE */

                    break;
                }

            default:
                {
                    break;
                }
        }
    }
}
```

```
}  
  
} /* End of function usb_main() */
```

## Descriptor

A template for PMSC descriptors can be found in `ra/fsp/src/r_usb_pmsc/r_usb_pmsc_descriptor.c.template`. Also, please be sure to use your vendor ID.

### 4.2.61 USB Peripheral Vendor Class (r\_usb\_pvnd)

#### Modules

#### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (`r_usb_basic`) to be called from the application.

## Overview

USB Peripheral Vendor class works by combining `r_usb_basic` module.

## How to Configuration

The following shows FSP configuration procedure for USB Peripheral Vendor class.

- Select [New Stack]->[Middleware]->[USB]->[USB Peripheral Vendor class driver on `r_usb_pvnd`].

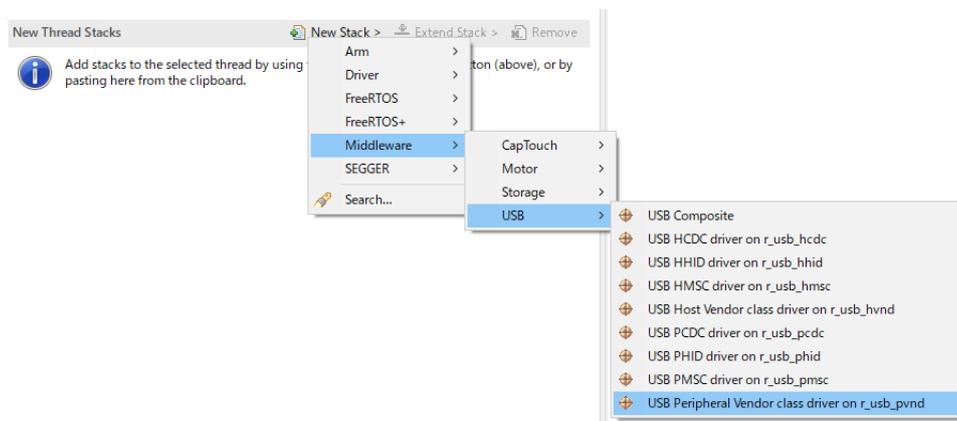


Figure 190: Select USB Peripheral Vendor Class

- The following is displayed when selecting [USB Peripheral Vendor class driver on r\_usb\_pvnd]. The user does not specify USB pipe number in Vendor class.

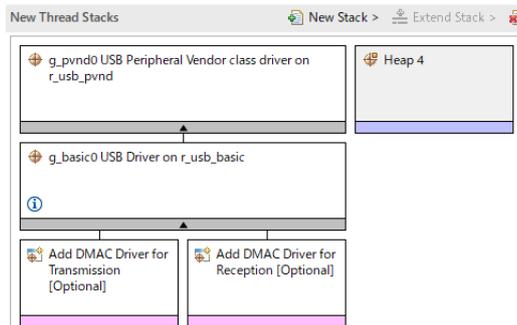


Figure 191: USB Peripheral Vendor Class Stack

## API

Use the following APIs in Peripheral Vendor class application program.

- For Data Transfer  
Use the following APIs for data transfer for Bulk transfer or Interrupt transfer.
  1. R\_USB\_PipeRead()
  2. R\_USB\_PipeWrite()
  3. R\_USB\_PipeStop()
- For Control Transfer  
Use the following API for the class request processing.
  1. R\_USB\_PeriControlDataGet()
  2. R\_USB\_PeriControlDataSet()
  3. R\_USB\_PeriControlStatusSet()
- For USB Pipe Information  
The USB driver allocates USB PIPE by analyzing the descriptor of USB device in Vendor class. Use the following APIs to get the allocated USB pipe information.
  1. R\_USB\_UsedPipesGet()
  2. R\_USB\_PipeInfoGet()

## USB PIPE Allocation

The USB driver allocates USB PIPE by analyzing the descriptor of USB device in Vendor class. The USB PIPE related to the Endpoint Descriptor are allocated in order from USB PIPE1 according to the description order of the Endpoint Descriptor.

## Limitations

This Peripheral Vendor class can not be included in composite device.

## Descriptor

Template for Vendor class descriptor can be found in ra/fsp/src/r\_usb\_pvnd folder. Also, please be sure to use your vendor ID.

## Examples

This application program processes the following after the enumeration completes with USB device.

1. Getting USB Pipe Information
2. Vendor Class Request Processing
3. Loopback processing of bulk transfer and interrupt transfer.

```
/*
 *
 * Macro definitions
 *
 */
/* for Vendor Class Request */
#define USB_SET_VENDOR_NO_DATA (0x0000U)
#define USB_SET_VENDOR (0x0100U)
#define USB_GET_VENDOR (0x0200U)
/*
 *
 * Function Name : usb_main
 * Description : main routine or task for peripheral vendor class
application.
 * Arguments : none:
 * Return value : none
 *
 */
void main_task (void)
{
#if (BSP_CFG_RTOS == 2)
    usb_event_info_t * p_mess;
#endif
    usb_status_t event;
    usb_event_info_t event_info;
    uint8_t bulk_out_pipe = 0; /* Bulk Out Pipe */
}
```

```
uint8_t      bulk_in_pipe = 0; /* Bulk In Pipe      */
uint8_t      int_out_pipe = 0; /* Interrupt Out Pipe */
uint8_t      int_in_pipe  = 0; /* Interrupt In Pipe  */

uint16_t     buf_type      = 0;
uint8_t      pipe          = 0;
uint8_t      is_zlp[2]    = {0, 0};
uint32_t     request_length = 0;
uint16_t     used_pipe     = 0;
usb_pipe_t   pipe_info;

g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);

while (1)
{
#if (BSP_CFG_RTOS == 2)
    USB_APL_RCV_MSG(USB_APL_MBX, (usb_msg_t **) &p_mess);
    event_info = *p_mess;

    event      = event_info.event;
#else /* (BSP_CFG_RTOS == 2) */
    g_usb_on_usb.eventGet(&event_info, &event);
#endif /* (BSP_CFG_RTOS == 2) */

    switch (event)
    {
case USB_STATUS_CONFIGURED:
        {
            buffer_init();

            is_zlp[0] = 0;
            is_zlp[1] = 0;

            g_usb_on_usb.usedPipesGet(&g_basic0_ctrl, &used_pipe,
USB_CLASS_PVND);

            for (pipe = START_PIPE; pipe < END_PIPE; pipe++)
            {
                if ((used_pipe & (1 << pipe)) != 0)
                {
                    g_usb_on_usb.pipeInfoGet(&g_basic0_ctrl, &pipe_info,
pipe);
```

```
if (USB_EP_DIR_IN != (pipe_info.endpoint & USB_EP_DIR_IN))
    {
/* Out Transfer */
if (USB_TRANSFER_TYPE_BULK == pipe_info.transfer_type)
    {
        buf_type      = BUF_BULK;
        bulk_out_pipe = pipe;
    }
else
    {
        buf_type      = BUF_INT;
        int_out_pipe = pipe;
    }
}

else
    {
/* In Transfer */
if (USB_TRANSFER_TYPE_BULK == pipe_info.transfer_type)
    {
        buf_type      = BUF_BULK;
        bulk_in_pipe = pipe;
    }
else
    {
        buf_type      = BUF_INT;
        int_in_pipe = pipe;
    }
}
}

break;
}

case USB_STATUS_READ_COMPLETE:
    {
```

```
if (FSP_ERR_USB_FAILED != event_info.status)
{
if (bulk_out_pipe == event_info.pipe)
{
buf_type = BUF_BULK;
pipe = bulk_in_pipe;
}
else if (int_out_pipe == event_info.pipe)
{
buf_type = BUF_INT;
pipe = int_in_pipe;
}
else
{
while (1)
{
;
}
}
buffer_check(buf_type, event_info.data_size);
g_usb_on_usb.pipeWrite(&g_basic0_ctrl,
&g_buf[buf_type][0], event_info.data_size, pipe);
}
break;
}
case USB_STATUS_WRITE_COMPLETE:
{
if (bulk_in_pipe == event_info.pipe)
{
buf_type = BUF_BULK;
if (1 == is_zlp[buf_type])
{
pipe = bulk_out_pipe;
}
}
}
```

```
    }
else if (int_in_pipe == event_info.pipe)
    {
        buf_type = BUF_INT;
if (1 == is_zlp[buf_type])
    {
        pipe = int_out_pipe;
    }
    }
else
    {
/* Nothing */
    }
if (1 == is_zlp[buf_type])
    {
        is_zlp[buf_type] = 0;
        buffer_clear(buf_type);
        g_usb_on_usb.pipeRead(&g_basic0_ctrl, &g_buf[buf_type][0],
BUF_SIZE, pipe);
    }
else
    {
        is_zlp[buf_type] = 1;
        g_usb_on_usb.pipeWrite(&g_basic0_ctrl, 0, 0,
event_info.pipe); /* Send ZLP */
    }
break;
    }
case USB_STATUS_REQUEST:
    {
if (USB_SET_VENDOR_NO_DATA == (event_info.setup.request_type & USB_BREQUEST
))
    {
        g_usb_on_usb.periControlStatusSet(&g_basic0_ctrl,
```

```
USB_SETUP_STATUS_ACK);
    }

    else if (USB_SET_VENDOR == (event_info.setup.request_type & USB_BREQUEST))
    {
        request_length = event_info.setup.request_length;
        g_usb_on_usb.periControlDataGet(&g_basic0_ctrl,
&g_request_buf[0], request_length);
    }

    else if (USB_GET_VENDOR == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.periControlDataSet(&g_basic0_ctrl,
&g_request_buf[0], request_length);
    }

    else
    {
        /* Nothing */
    }

    break;
}

case USB_STATUS_REQUEST_COMPLETE:
{
    if (USB_GET_VENDOR == (event_info.setup.request_type & USB_BREQUEST))
    {
        g_usb_on_usb.pipeRead(&g_basic0_ctrl, &g_buf[BUF_BULK][0],
BUF_SIZE, bulk_out_pipe);
        g_usb_on_usb.pipeRead(&g_basic0_ctrl, &g_buf[BUF_INT][0],
BUF_SIZE, int_out_pipe);
    }

    break;
}

case USB_STATUS_DETACH:
{
    break;
}
```

```
default:
    {
break;
    }
}

}

/* End of function usb_main */

/*****
**
* Function Name : buffer_init
* Description : buffer initialization
* Arguments : none
* Return value : none
*****/

**/

static void buffer_init (void)
{
    uint16_t i;
    uint16_t j;
    for (j = 0; j < 2; j++)
    {
    for (i = 0; i < BUF_SIZE; i++)
        {
            g_buf[j][i] = (uint8_t) i;
        }
    }
}

/*****
**
* Function Name : buffer_check
* Description : buffer check
* Arguments : buf_type : buffer number
* Return value : none
*****/
```

```
*/
static void buffer_check (uint16_t buf_type, uint32_t size)
{
    uint16_t i;
    for (i = 0; i < (uint16_t) size; i++)
    {
        if ((uint8_t) (i & USB_VALUE_FF) != g_buf[buf_type][i])
        {
            while (1)
            {
                ;
            }
        }
    }
}

/*****
**
* Function Name : buffer_clear
* Description : buffer clear
* Arguments : buf_type : buffer number
* Return value : none
*****/
*/
static void buffer_clear (uint16_t buf_type)
{
    uint16_t i;
    for (i = 0; i < BUF_SIZE; i++)
    {
        g_buf[buf_type][i] = 0;
    }
}

/*****
**
* End of function usb_mcu_init
*****/
```

```
*****
**/
#if (BSP_CFG_RTOS == 2)
/*****
**
* Function Name : usb_apl_rec_msg
* Description : Receive a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t** mess : Message pointer
* : usb_tm_t tm : Timeout Value
* Return : uint16_t : USB_OK / USB_ERROR
*****
**/
usb_er_t usb_apl_rec_msg (uint8_t id, usb_msg_t ** mess, usb_tm_t tm)
{
    BaseType_t err;
    QueueHandle_t handle;
    usb_er_t result;
    (void) tm;
    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }
    handle = (*(g_apl_mbx_table[id]));
    *mess = NULL;
    err = xQueueReceive(handle, (void *) mess, (portMAX_DELAY));
    if ((pdTRUE == err) && (NULL != (*mess)))
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }
}
```

```

return result;
}
/*****
**
* End of function usb_apl_rec_msg
*****/
**/
/*****
**
* Function Name : usb_apl_snd_msg
* Description : Send a message to the specified id (mailbox).
* Argument : uint8_t id : ID number (mailbox).
* : usb_msg_t* mess : Message pointer
* Return : usb_er_t : USB_OK / USB_ERROR
*****/
**/
usb_er_t usb_apl_snd_msg (uint8_t id, usb_msg_t * mess)
{
    BaseType_t err;
    QueueHandle_t handle;
    usb_er_t result;

    if (NULL == mess)
    {
        return USB_APL_ERROR;
    }

    handle = (*(g_apl_mbx_table[id]));
    err = xQueueSend(handle, (const void *) &mess, (TickType_t) (0));
    if (pdTRUE == err)
    {
        result = USB_APL_OK;
    }
    else
    {
        result = USB_APL_ERROR;
    }
}

```

```

    }

    return result;
}

/*****
**
** End of function usb_apl_snd_msg
*****/

**/
#endif /* #if (BSP_CFG_RTOS == 2) */

```

## 4.2.62 Watchdog Timer (r\_wdt)

### Modules

#### Functions

`fsp_err_t` `R_WDT_Refresh` (`wdt_ctrl_t *const p_ctrl`)

`fsp_err_t` `R_WDT_Open` (`wdt_ctrl_t *const p_ctrl`, `wdt_cfg_t const *const p_cfg`)

`fsp_err_t` `R_WDT_StatusClear` (`wdt_ctrl_t *const p_ctrl`, `const wdt_status_t status`)

`fsp_err_t` `R_WDT_StatusGet` (`wdt_ctrl_t *const p_ctrl`, `wdt_status_t *const p_status`)

`fsp_err_t` `R_WDT_CounterGet` (`wdt_ctrl_t *const p_ctrl`, `uint32_t *const p_count`)

`fsp_err_t` `R_WDT_TimeoutGet` (`wdt_ctrl_t *const p_ctrl`, `wdt_timeout_values_t *const p_timeout`)

`fsp_err_t` `R_WDT_CallbackSet` (`wdt_ctrl_t *const p_ctrl`, `void(*p_callback)(wdt_callback_args_t *)`, `void const *const p_context`, `wdt_callback_args_t *const p_callback_memory`)

### Detailed Description

Driver for the WDT peripheral on RA MCUs. This module implements the [WDT Interface](#).

## Overview

The watchdog timer is used to recover from unexpected errors in an application. The watchdog timer must be refreshed periodically in the permitted count window by the application. If the count is allowed to underflow or refresh occurs outside of the valid refresh period, the WDT resets the device or generates an NMI.

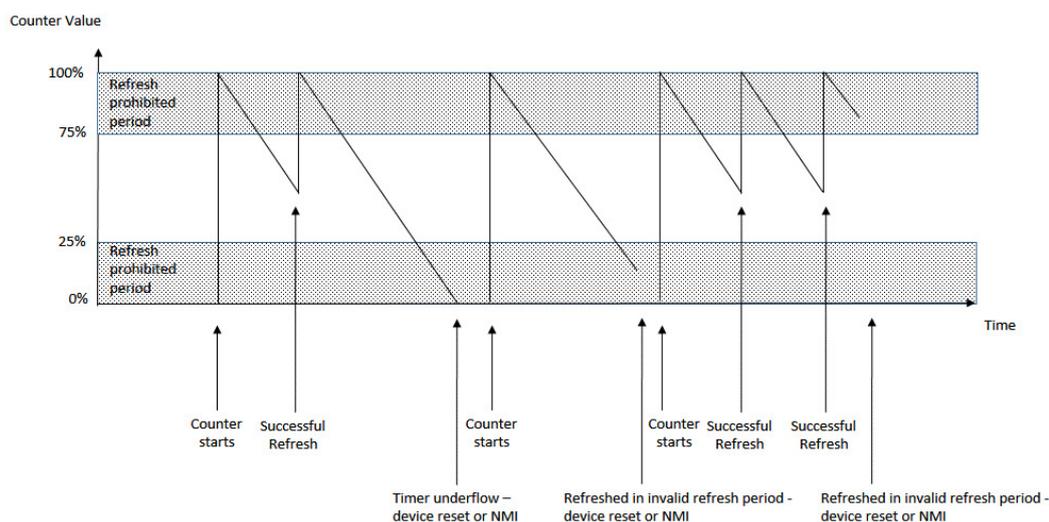


Figure 192: Watchdog Timer Operation Example

## Features

The WDT HAL module has the following key features:

- When the WDT underflows or is refreshed outside of the permitted refresh window, one of the following events can occur:
  - Resetting of the device
  - Generation of an NMI
- The WDT has two supported modes:
  - In auto start mode, the WDT begins counting at reset.
  - In register start mode, the WDT can be started from the application.

## Selecting a Watchdog

RA MCUs have two watchdog peripherals: the watchdog timer (WDT) and the independent watchdog timer (IWDT). When selecting between them, consider these factors:

	WDT	IWDT
Start Mode	The WDT can be started from the application (register start mode) or configured by hardware to start automatically	The IWDT can only be configured by hardware to start automatically.

(auto start mode).

Clock Source

The WDT runs off a peripheral clock.

The IWDT has its own clock source which improves safety.

## Configuration

When using register start mode, configure the watchdog timer on the Stacks tab.

### Note

When using auto start mode, configurations on the **Stacks** tab are ignored. Configure the watchdog using the **OFS** settings on the **BSP** tab.

### Build Time Configurations for r\_wdt

The following build time configurations are defined in fsp\_cfg/r\_wdt\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Register Start NMI Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	If enabled, code for NMI support in register start mode is included in the build.

### Configurations for Driver > Monitoring > Watchdog Driver on r\_wdt

This module can be added to the Stacks tab via New Stack > Driver > Monitoring > Watchdog Driver on r\_wdt. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_wdt0	Module name.
Timeout	<ul style="list-style-type: none"> <li>1,024 Cycles</li> <li>4,096 Cycles</li> <li>8,192 Cycles</li> <li>16,384 Cycles</li> </ul>	16,384 Cycles	Select the watchdog timeout in cycles.
Clock Division Ratio	<ul style="list-style-type: none"> <li>PCLK/4</li> <li>PCLK/64</li> <li>PCLK/128</li> <li>PCLK/512</li> <li>PCLK/2048</li> <li>PCLK/8192</li> </ul>	PCLK/8192	Select the watchdog clock divisor.
Window Start Position	<ul style="list-style-type: none"> <li>100% (Window Position Not Specified)</li> <li>75%</li> </ul>	100% (Window Position Not Specified)	Select the allowed watchdog refresh start point.

	<ul style="list-style-type: none"> <li>• 50%</li> <li>• 25</li> </ul>		
Window End Position	<ul style="list-style-type: none"> <li>• 0% (Window Position Not Specified)</li> <li>• 25%</li> <li>• 50%</li> <li>• 75%</li> </ul>	0% (Window Position Not Specified)	Select the allowed watchdog refresh end point.
Reset Control	<ul style="list-style-type: none"> <li>• Reset Output</li> <li>• NMI Generated</li> </ul>	Reset Output	Select what happens when the watchdog timer expires.
Stop Control	<ul style="list-style-type: none"> <li>• WDT Count Enabled in Low Power Mode</li> <li>• WDT Count Disabled in Low Power Mode</li> </ul>	WDT Count Disabled in Low Power Mode	Select the watchdog state in low power mode.
NMI Callback	Name must be a valid C symbol	NULL	A user callback function must be provided if the WDT is configured to generate an NMI when the timer underflows or a refresh error occurs. If this callback function is provided, it will be called from the NMI handler each time the watchdog triggers.

## Clock Configuration

The WDT clock is based on the PCLKB frequency. You can set the PCLKB frequency using the **Clocks** tab of the RA Configuration editor or by using the CGC Interface at run-time. The maximum timeout period with PCLKB running at 60 MHz is approximately 2.2 seconds.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### NMI Interrupt

The watchdog timer uses the NMI, which is enabled by default. No special configuration is required. When the NMI is triggered, the callback function registered during open is called.

#### Note

*When using the WDT in software start mode with NMI and the timer underflows, the WDT status must be reset by calling [R\\_WDT\\_StatusClear](#) before restarting the timer via [R\\_WDT\\_Refresh](#).*

### Period Calculation

The WDT operates from PCLKB. With a PCLKB of 60 MHz, the maximum time from the last refresh to device reset or NMI generation will be just over 2.2 seconds as detailed below.

PLCKB = 60 MHz

Clock division ratio = PCLKB / 8192

Timeout period = 16384 cycles

WDT clock frequency = 60 MHz / 8192 = 7.324 kHz

Cycle time = 1 / 7.324 kHz = 136.53 us

Timeout = 136.53 us x 16384 cycles = 2.23 seconds

## Limitations

Developers should be aware of the following limitations when using the WDT:

- When using a J-Link debugger the WDT counter does not count and therefore will not reset the device or generate an NMI. To enable the watchdog to count and generate a reset or NMI while debugging, add this line of code in the application:

```
/* (Optional) Enable the WDT to count and generate NMI or reset when the
 * debugger is connected. */
R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;
```

- If the WDT is configured to stop the counter in low power mode, then your application must restart the watchdog by calling [R\\_WDT\\_Refresh\(\)](#) after the MCU wakes from low power mode.

## Examples

### WDT Basic Example

This is a basic example of minimal use of the WDT in an application.

```
void wdt_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* In auto start mode, the WDT starts counting immediately when the MCU is powered
    on. */

    /* Initializes the module. */
    err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* In register start mode, start the watchdog by calling R_WDT_Refresh. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    assert(FSP_SUCCESS == err);
}
```

```
while (true)
{
/* Application work here. */
/* Refresh before the counter underflows to prevent reset or NMI. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
assert(FSP_SUCCESS == err);
}
}
```

### WDT Advanced Example

This example demonstrates using a start window and gives an example callback to handle an NMI generated by an underflow or refresh error.

```
#define WDT_TIMEOUT_COUNTS (16384U)
#define WDT_MAX_COUNTER (WDT_TIMEOUT_COUNTS - 1U)
#define WDT_START_WINDOW_75 ((WDT_MAX_COUNTER * 3) / 4)
/* Example callback called when a watchdog NMI occurs. */
void wdt_callback (wdt_callback_args_t * p_args)
{
FSP_PARAMETER_NOT_USED(p_args);
fsp_err_t err = FSP_SUCCESS;
/* (Optional) Determine the source of the NMI. */
wdt_status_t status = WDT_STATUS_NO_ERROR;
err = R_WDT_StatusGet(&g_wdt0_ctrl, &status);
assert(FSP_SUCCESS == err);
/* (Optional) Log source of NMI and any other debug information. */
/* (Optional) Clear the error flags. */
err = R_WDT_StatusClear(&g_wdt0_ctrl, status);
assert(FSP_SUCCESS == err);
/* (Register start mode) In register start mode, call R_WDT_Refresh() to
* continue using the watchdog after an error. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
assert(FSP_SUCCESS == err);
/* (Optional) Issue a software reset to reset the MCU. */
```

```
    __NVIC_SystemReset();
}

void wdt_advanced_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* (Optional) Enable the WDT to count and generate NMI or reset when the
     * debugger is connected. */
    R_DEBUG->DBGSTOPCR_b.DBGSTOP_WDT = 0;

    /* (Optional) Check if the WDTRF flag is set to know if the system is
     * recovering from a WDT reset. */
    if (R_SYSTEM->RSTSR1_b.WDTRF)
    {
        /* Clear the flag. */
        R_SYSTEM->RSTSR1 = 0U;
    }

    /* Open the module. */
    err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize other application code. */
    /* (Register start mode) Call R_WDT_Refresh() to start the WDT in register
     * start mode. Do not call R_WDT_Refresh() in auto start mode unless the
     * counter is in the acceptable refresh window. */
    err = R_WDT_Refresh(&g_wdt0_ctrl);
    assert(FSP_SUCCESS == err);

    while (true)
    {
        /* Application work here. */
        /* (Optional) If there is a chance the application takes less time than
         * the start window, verify the WDT counter is past the start window
         * before refreshing the WDT. */
        uint32_t wdt_counter = 0U;
    }
}
```

```
/* Read the current WDT counter value. */
    err = R_WDT_CounterGet(&g_wdt0_ctrl, &wdt_counter);
    assert(FSP_SUCCESS == err);
} while (wdt_counter >= WDT_START_WINDOW_75);
/* Refresh before the counter underflows to prevent reset or NMI. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
assert(FSP_SUCCESS == err);
}
}
```

## Data Structures

struct [wdt\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [wdt\\_instance\\_ctrl\\_t](#)

struct [wdt\\_instance\\_ctrl\\_t](#)

WDT private control block. DO NOT MODIFY. Initialization occurs when [R\\_WDT\\_Open\(\)](#) is called.

## Function Documentation

◆ **R\_WDT\_Refresh()**

```
fsp_err_t R_WDT_Refresh ( wdt_ctrl_t *const p_ctrl)
```

Refresh the watchdog timer. Implements `wdt_api_t::refresh`.

In addition to refreshing the watchdog counter this function can be used to start the counter in register start mode.

Example:

```
/* Refresh before the counter underflows to prevent reset or NMI. */
err = R_WDT_Refresh(&g_wdt0_ctrl);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	WDT successfully refreshed.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

**Note**

*This function only returns FSP\_SUCCESS. If the refresh fails due to being performed outside of the permitted refresh period the device will either reset or trigger an NMI ISR to run.*

◆ **R\_WDT\_Open()**

```
fsp_err_t R_WDT_Open ( wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg )
```

Configure the WDT in register start mode. In auto-start\_mode the NMI callback can be registered. Implements `wdt_api_t::open`.

This function should only be called once as WDT configuration registers can only be written to once so subsequent calls will have no effect.

Example:

```
/* Initializes the module. */
err = R_WDT_Open(&g_wdt0_ctrl, &g_wdt0_cfg);
```

**Return values**

FSP_SUCCESS	WDT successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_STATE	The security state of the NMI and the module do not match.

**Note**

*In auto start mode the only valid configuration option is for registering the callback for the NMI ISR if NMI output has been selected.*

◆ **R\_WDT\_StatusClear()**

```
fsp_err_t R_WDT_StatusClear ( wdt_ctrl_t *const p_ctrl, const wdt_status_t status )
```

Clear the WDT status and error flags. Implements `wdt_api_t::statusClear`.

Example:

```
/* (Optional) Clear the error flags. */
err = R_WDT_StatusClear(&g_wdt0_ctrl, status);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	WDT flag(s) successfully cleared.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.
FSP_ERR_UNSUPPORTED	This function is only valid if the watchdog generates an NMI when an error occurs.

**Note**

*When the WDT is configured to output a reset on underflow or refresh error reading the status and error flags serves no purpose as they will always indicate that no underflow has occurred and there is no refresh error. Reading the status and error flags is only valid when interrupt request output is enabled.*

◆ **R\_WDT\_StatusGet()**

```
fsp_err_t R_WDT_StatusGet ( wdt_ctrl_t*const p_ctrl, wdt_status_t*const p_status )
```

Read the WDT status flags. Implements `wdt_api_t::statusGet`.

Indicates both status and error conditions.

Example:

```
/* (Optional) Determine the source of the NMI. */
wdt_status_t status = WDT_STATUS_NO_ERROR;
err = R_WDT_StatusGet(&g_wdt0_ctrl, &status);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	WDT status successfully read.
FSP_ERR_ASSERTION	Null pointer as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.
FSP_ERR_UNSUPPORTED	This function is only valid if the watchdog generates an NMI when an error occurs.

**Note**

*When the WDT is configured to output a reset on underflow or refresh error reading the status and error flags serves no purpose as they will always indicate that no underflow has occurred and there is no refresh error. Reading the status and error flags is only valid when interrupt request output is enabled.*

◆ **R\_WDT\_CounterGet()**

```
fsp_err_t R_WDT_CounterGet ( wdt_ctrl_t*const p_ctrl, uint32_t*const p_count )
```

Read the current count value of the WDT. Implements `wdt_api_t::counterGet`.

Example:

```
/* Read the current WDT counter value. */
err = R_WDT_CounterGet(&g_wdt0_ctrl, &wdt_counter);
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	WDT current count successfully read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

◆ **R\_WDT\_TimeoutGet()**

```
fsp_err_t R_WDT_TimeoutGet ( wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout )
```

Read timeout information for the watchdog timer. Implements `wdt_api_t::timeoutGet`.

**Return values**

FSP_SUCCESS	WDT timeout information retrieved successfully.
FSP_ERR_ASSERTION	Null Pointer.
FSP_ERR_NOT_OPEN	Instance control block is not initialized.

◆ **R\_WDT\_CallbackSet()**

```
fsp_err_t R_WDT_CallbackSet ( wdt_ctrl_t *const p_ctrl, void(*)(wdt_callback_args_t *) p_callback, void const *const p_context, wdt_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `wdt_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

**4.2.63 ADPCM Decoder (rm\_adpcm\_decoder)**

## Modules

**Functions**

```
fsp_err_t RM_ADPCM_DECODER_Open (adpcm_decoder_ctrl_t *p_ctrl, adpcm_decoder_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_ADPCM_DECODER_Decode (adpcm_decoder_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t src_len_bytes)
```

```
fsp_err_t RM_ADPCM_DECODER_Reset (adpcm_decoder_ctrl_t *p_ctrl)
```

```
fsp_err_t RM_ADPCM_DECODER_Close (adpcm_decoder_ctrl_t *p_ctrl)
```

## Detailed Description

Middleware to implement the ADPCM Audio Decoder. This module implements the [ADPCM Decoder Interface](#).

## Overview

### Features

The ADPCM Audio Decoder has the following key features:

- Decodes 4-bit ADPCM input to 16-bit PCM output

## Configuration

### Build Time Configurations for rm\_adpcm\_decoder

The following build time configurations are defined in fsp\_cfg/rm\_adpcm\_decoder\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Audio > ADPCM Decoder on rm\_adpcm\_decoder

This module can be added to the Stacks tab via New Stack > Middleware > Audio > ADPCM Decoder on rm\_adpcm\_decoder.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_adpcm_decoder0	Module name.

### Clock Configuration

This module has no required clock configurations.

### Pin Configuration

This module does not use I/O pins.

## Examples

### Basic Example

This is a basic example of minimal use of the ADPCM Audio Decoder implementation in an application.

```

void rm_adpcm_decoder_example ()
{
    /* Open the ADPCM audio decoder instance. */
    fsp_err_t err = RM_ADPCM_DECODER_Open(&g_adpcmdec_ctrl, &g_adpcmdec_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Decode the data */
    err = RM_ADPCM_DECODER_Decode(&g_adpcmdec_ctrl, g_adpcm_stream1, g_pcm_stream,
ADPCM_BUFFER_SIZE_BYTES);
    assert(FSP_SUCCESS == err);
    /* Reset the ADPCM audio decoder instance before decoding a new stream. */
    err = RM_ADPCM_DECODER_Reset(&g_adpcmdec_ctrl);
    assert(FSP_SUCCESS == err);
    /* Decode the first chunk of ADPCM data */
    err = RM_ADPCM_DECODER_Decode(&g_adpcmdec_ctrl, g_adpcm_stream2, g_pcm_stream,
(ADPCM_BUFFER_SIZE_BYTES/2));
    assert(FSP_SUCCESS == err);
    /* Decode the second chunk of ADPCM data */
    err = RM_ADPCM_DECODER_Decode(&g_adpcmdec_ctrl,
&g_adpcm_stream2[ADPCM_BUFFER_SIZE_BYTES/2],
                                g_pcm_stream, (ADPCM_BUFFER_SIZE_BYTES/2));
    assert(FSP_SUCCESS == err);
}

```

## Data Structures

```
struct adpcm_decoder_instance_ctrl_t
```

## Data Structure Documentation

### ◆ adpcm\_decoder\_instance\_ctrl\_t

```
struct adpcm_decoder_instance_ctrl_t
```

RM\_ADPCM\_DECODER instance control block. DO NOT INITIALIZE. Initialized in [adpcm\\_decoder\\_api\\_t::open\(\)](#).

## Function Documentation

◆ **RM\_ADPCM\_DECODER\_Open()**

```
fsp_err_t RM_ADPCM_DECODER_Open ( adpcm_decoder_ctrl_t * p_ctrl, adpcm_decoder_cfg_t const *const p_cfg )
```

Initializes ADPCM audio decoder device.

Implements `adpcm_decoder_api_t::open()`.

**Return values**

FSP_SUCCESS	Module is ready for use.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_ALREADY_OPEN	The instance control structure has already been opened.

◆ **RM\_ADPCM\_DECODER\_Decode()**

```
fsp_err_t RM_ADPCM_DECODER_Decode ( adpcm_decoder_ctrl_t *const p_ctrl, void const * p_src, void * p_dest, uint32_t src_len_bytes )
```

Decodes 4bit ADPCM data to 16bit PCM data. It reads ADPCM data from area pointed by inputAddr pointer, decodes the number of samples specified and stores the decoded data in buffer pointed with outputAddr pointer.

Implements `adpcm_decoder_api_t::decode()`.

**Return values**

FSP_SUCCESS	Decode operation successfully completed.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

◆ **RM\_ADPCM\_DECODER\_Reset()**

```
fsp_err_t RM_ADPCM_DECODER_Reset ( adpcm_decoder_ctrl_t * p_ctrl)
```

This function resets the ADPCM decoder device.

Implements `adpcm_decoder_api_t::reset()`.

**Return values**

FSP_SUCCESS	Module closed.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

### ◆ RM\_ADPCM\_DECODER\_Close()

`fsp_err_t RM_ADPCM_DECODER_Close ( adpcm_decoder_ctrl_t * p_ctrl)`

This function closes the ADPCM decoder device.

Implements `adpcm_decoder_api_t::close()`.

#### Return values

FSP_SUCCESS	Module closed.
FSP_ERR_ASSERTION	An input argument is invalid.
FSP_ERR_NOT_OPEN	Unit is not open.

## 4.2.64 Audio Playback with PWM (rm\_audio\_playback\_pwm)

### Modules

#### Functions

`fsp_err_t RM_AUDIO_PLAYBACK_PWM_Open (audio_playback_ctrl_t *const p_api_ctrl, audio_playback_cfg_t const *const p_cfg)`

`fsp_err_t RM_AUDIO_PLAYBACK_PWM_Start (audio_playback_ctrl_t *const p_api_ctrl)`

`fsp_err_t RM_AUDIO_PLAYBACK_PWM_Stop (audio_playback_ctrl_t *const p_api_ctrl)`

`fsp_err_t RM_AUDIO_PLAYBACK_PWM_Play (audio_playback_ctrl_t *const p_api_ctrl, void const *const p_buffer, uint32_t length)`

`fsp_err_t RM_AUDIO_PLAYBACK_PWM_Close (audio_playback_ctrl_t *const p_api_ctrl)`

#### Detailed Description

Driver for the Audio Playback middleware on RA MCUs. This module implements the [AUDIO PLAYBACK Interface](#).

## Overview

### Features

The Audio Playback with PWM middleware is used to play audio streams at user selected playback rate using Pulse Width Modulation hardware on GPT or AGT timers. This module can play the 16 bit

uncompressed, unsigned PCM audio stream when AGT is selected as PWM interface and can play 32 bit uncompressed, unsigned PCM audio stream when GPT is used as PWM interface. The application code is expected to convert the signed PCM data to unsigned PCM data and scale it with the playback rate before starting the playback.

## Configuration

### Build Time Configurations for rm\_audio\_playback\_pwm

The following build time configurations are defined in fsp\_cfg/rm\_audio\_playback\_pwm\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
DMAC Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Select if DMAC will be used.

### Configurations for Middleware > Audio > Audio Playback PWM driver on rm\_audio\_playback\_pwm

This module can be added to the Stacks tab via New Stack > Middleware > Audio > Audio Playback PWM driver on rm\_audio\_playback\_pwm.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_rm_audio_playback0	Module name.
General > Playback Speed (Hz)	Manual Entry	44100	Enter playback sample rate in Hz.
Interrupts > Callback	Name must be a valid C symbol	g_rm_audio_playback0_callback	A user callback function. If this callback function is provided, it is called from the interrupt service routine (ISR) each time the playback completes.
PWM Output Pin	<ul style="list-style-type: none"> <li>Pin A</li> <li>Pin B</li> </ul>	Pin A	Select which timer output pin should be used for audio output.

### Clock Configuration

The Audio Playback with PWM module does not require a specific clock configuration.

### Pin Configuration

Configure the PWM output pins for selected PWM HAL layer peripheral (AGT/GPT). One of the

following pins needs to be selected and enabled as PWM output for selected channel n,

If GPT is used as PWM interface,

- GTIOCA<sub>n</sub>
- GTIOCB<sub>n</sub>

If AGT is used as PWM interface,

- AGTOA<sub>n</sub>
- AGTOB<sub>n</sub>

## Usage Notes

### DMAC/DTC Integration

DMAC/DTC is used as a lower level transfer instance with this module and is operated in Normal mode to transfer 16 bit or 32 bit data from the audio stream buffer to the PWM peripheral AGT or GPT respectively. Destination address for transfer instance needs to be the Duty Cycle setting register GTCCR for GPT as PWM driver or AGTMA/AGTCMB in case of AGT as PWM driver. Select 'Transfer Size' as 2 Bytes when AGT is used for PWM generation otherwise select 'Transfer Size' as 4 Bytes if GPT is used for PWM generation.

## Examples

### Basic Example

This is a basic example of minimal use of the RM\_AUDIO\_PLAYBACK\_PWM in an application. This example shows how this driver can be used for playing a 16 bit uncompressed PCM audio from a single input buffer.

```
int16_t play_buffer[AUDIO_EXAMPLE_LENGTH];
uint32_t g_audio_callback_counter = 0;
void g_audio_example_counter_callback (audio_playback_callback_args_t * p_args)
{
    if (AUDIO_PLAYBACK_EVENT_PLAYBACK_COMPLETE == (p_args->event))
    {
        g_audio_callback_counter++;
    }
}
void basic_example (void)
{
    fsp_err_t err;

    /* Initialize the Audio Playback module for playing an audio stream. */
    err = RM_AUDIO_PLAYBACK_PWM_Open(&g_audio_playback_pwm_ctrl,
```

```
&g_audio_playback_pwm_cfg);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Set the 16 Bit PCM audio stream to play next */
err = RM_AUDIO_PLAYBACK_PWM_Play(&g_audio_playback_pwm_ctrl, play_buffer,
AUDIO_EXAMPLE_LENGTH);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Start to the play the selected audio stream*/
err = RM_AUDIO_PLAYBACK_PWM_Start(&g_audio_playback_pwm_ctrl);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Wait till the playback is completed */
while (g_audio_callback_counter == 0)
{
    ;
}

/* Stop playing. */
err = RM_AUDIO_PLAYBACK_PWM_Stop(&g_audio_playback_pwm_ctrl);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
}
```

## Streaming Example

This is an example of using Audio Playback module to play audio stream. This application uses a double buffer to store PCM sine wave data. It starts playing in the main loop, then loads the next buffer if it is ready in the callback. If the next buffer is not ready, a flag is set in the callback so the application knows to restart playing in the main loop. This example also demonstrates conversion of signed PCM format data to unsigned PWM format data along with scaling the data samples for optimum PWM wave generation.

```
#define AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ (22050U)
#define AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_PERIOD_VALUE_AT_22050HZ (0x11B7U)
#define AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK (1024U)
#define AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ (800U)
#define AUDIO_PLAYBACK_PWM_EXAMPLE_SAMPLES_TO_TRANSFER (1024U)
```

```
#define AUDIO_PLAYBACK_PWM_EXAMPLE_CONVERT_TO_PWM_SAMPLES (32768U)
#define AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_DATA_BIT_SIZE (16U)
int16_t      g_stream_src[2][AUDIO_PLAYBACK_PWM_EXAMPLE_SAMPLES_TO_TRANSFER];
q15_t       g_pwm_sample[2][AUDIO_PLAYBACK_PWM_EXAMPLE_SAMPLES_TO_TRANSFER];
q15_t       g_pwm_scaled_sample[2][AUDIO_PLAYBACK_PWM_EXAMPLE_SAMPLES_TO_TRANSFER];
uint32_t     g_buffer_index          = 0;
volatile bool g_send_data_in_main_loop = true;
volatile bool g_data_ready = false;
/* Example callback called when Audio Playback is ready for more data. */
void rm_audio_playback_example_callback (audio_playback_callback_args_t * p_args)
{
    /* Start playing next stream if data is ready. */
    if (AUDIO_PLAYBACK_EVENT_PLAYBACK_COMPLETE == (p_args->event))
    {
        if (g_data_ready)
        {
            /* Reload data and handle errors. */
            rm_audio_playback_example_play();
        }
        else
        {
            /* Data was not ready yet, send it in the main loop. */
            g_send_data_in_main_loop = true;
        }
    }
}
/* Load the next stream and check for error condition. */
void rm_audio_playback_example_play (void)
{
    /* Set the playback stream */
    fsp_err_t err;
    err =
    RM_AUDIO_PLAYBACK_PWM_Play(&g_audio_playback_pwm_ctrl, (int16_t *)
&g_pwm_scaled_sample[g_buffer_index][0],
```

```
(AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK * sizeof(int16_t));
if (FSP_SUCCESS == err)
{
/* Switch the buffer after data is sent. */
g_buffer_index = !g_buffer_index;
/* Allow loop to calculate next buffer. */
g_data_ready = false;
}
else
{
/* The
* application must wait until the audio playback is completed. In this example, the
* callback sets data or resets the flag g_send_data_in_main_loop. */
}
}
/* Calculate samples. This example is just a sine wave. For this type of data, it
would be better to calculate
* one period and loop it. This example should be updated for the audio data used by
the application. */
void rm_audio_playback_example_calculate_samples (uint32_t buffer_index)
{
static uint32_t t = 0U;
/* Create a sine wave. Using formula sample = sin(2 * pi * tone_frequency * t /
sampling_frequency) */
uint32_t freq = AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_TONE_FREQUENCY_HZ;
for (uint32_t i = 0; i < AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK; i
+= 1)
{
float input = (((float) (freq * t)) * M_TWOPi) /

AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_AUDIO_SAMPLING_FREQUENCY_HZ;

t++;
/* Store sample. */
```

```
    int16_t sample = (int16_t) ((INT16_MAX * sinf(input)));
    g_stream_src[buffer_index][i] = sample;
}

/* Convert signed PCM data to unsigned PCM data as PWM needs unsigned input. */
arm_offset_q15(&g_stream_src[buffer_index][0],
              (q15_t) (INT16_MAX + 1),
              &g_pwm_sample[buffer_index][0],
              AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK);

/* Scale the data by the selected period for the timer (calculated for equivalent
playback rate) */
arm_scale_q15(&g_pwm_sample[buffer_index][0],
              AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_PERIOD_VALUE_AT_22050HZ,
              AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_DATA_BIT_SIZE,
              &g_pwm_scaled_sample[buffer_index][0],
              AUDIO_PLAYBACK_PWM_STREAMING_EXAMPLE_SAMPLES_PER_CHUNK);

/* Data is ready to be sent in the interrupt. */
g_data_ready = true;
}

void rm_audio_playback_streaming_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initialize the module.
    * Configure the following pins in the pin configurator for PWM output:
    * - If the GPT timer is used for generation of PWM waves configure GTIOCAn or
    GTIOCBn pin and enable the output
    * to these pins through the GPT module properties for desired channel n.
    * - Otherwise, if AGT is used for generation of PWM waves configure AGTOAn or
    AGTOBn pin and enable the output to
    * to these pins through the AGT module properties for desired channel n.
    * Configure the DMAC/DTC destination address as following:
    * - If the GPT timer is used for generation of PWM waves, configure DMAC/DTC
    destination address to the address of
    * GTCCRC register (&R_GPTn->GTCCR[2]) if PWM output pin is GTIOCA otherwise
    configure to the address of GTCCRD
```

```
* register (&R_GPTn->GTCCR[3]) if PWM output pin is GTIOCB for desired GPT channel
n.
* - If the AGT timer is used for generation of PWM waves, configure DMAC/DTC
destination address as the address of
* AGTCMA register (&R_AGTn->AGTCMA) if PWM output pin is AGTOA otherwise the
address of AGTCMB register
* (&R_AGTn->AGTCMB) if the PWM output pin is AGTOB for desired AGT channel n.
* Configure the DMAC/DTC transfer size as 4 Bytes if PWM interface is GPT timer
otherwise configure transfer size as 2 Bytes if
* PWM interface is AGT timer. */
err = RM_AUDIO_PLAYBACK_PWM_Open(&g_audio_playback_pwm_ctrl,
&g_audio_playback_pwm_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Start timer and transfer modules. */
err = RM_AUDIO_PLAYBACK_PWM_Start(&g_audio_playback_pwm_ctrl);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
while (true)
{
/* Prepare data in a buffer that is not currently used for transmission. */
rm_audio_playback_example_calculate_samples(g_buffer_index);
/* Send data in main loop the first time, and if it was not ready in the interrupt.
*/
if (g_send_data_in_main_loop)
{
/* Clear flag. */
g_send_data_in_main_loop = false;
/* Reload data and handle errors. */
rm_audio_playback_example_play();
}
/* If the next buffer is ready, wait for the data to be sent in the interrupt. */
while (g_data_ready)
{
```

```

/* Do nothing. */
}
}
}

```

## Data Structures

struct [audio\\_playback\\_pwm\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ audio\_playback\_pwm\_instance\_ctrl\_t

struct [audio\\_playback\\_pwm\\_instance\\_ctrl\\_t](#)

AUDIO\_PLAYBACK\_PWM instance control block. DO NOT MODIFY. Initialization occurs when [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Open\(\)](#) is called.

#### Data Fields

void(*)	<a href="#">p_callback</a> )(audio_playback_callback_args_t *p_args)
void *	<a href="#">p_context</a>
<a href="#">audio_playback_cfg_t</a> const *	<a href="#">p_cfg</a>
	Pointer to the configuration structure.
uint32_t	<a href="#">open</a>
	Used by driver to check if the control structure is valid.
<a href="#">timer_instance_t</a> const *	<a href="#">p_lower_lvl_timer</a>
	Timer API used to generate sampling frequency and GPT/AGT API used to access PWM hardware.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_lower_lvl_transfer</a>
	Transfer API used to transfer data each sampling frequency.

## Field Documentation

**◆ p\_callback**

```
void(* audio_playback_pwm_instance_ctrl_t::p_callback) (audio_playback_callback_args_t *p_args)
```

Callback called when play is complete.

**◆ p\_context**

```
void* audio_playback_pwm_instance_ctrl_t::p_context
```

Placeholder for user data. Passed to the user callback in [audio\\_playback\\_callback\\_args\\_t](#).

**Function Documentation****◆ RM\_AUDIO\_PLAYBACK\_PWM\_Open()**

```
fsp_err_t RM_AUDIO_PLAYBACK_PWM_Open ( audio_playback_ctrl_t *const p_api_ctrl,
audio_playback_cfg_t const *const p_cfg )
```

Opens and configures the Audio Playback with PWM driver. Sets playback speed and transfer rate to read the audio buffer.

Example:

```
/* Initialize the Audio Playback module for playing an audio stream. */
err = RM_AUDIO_PLAYBACK_PWM_Open(&g_audio_playback_pwm_ctrl,
&g_audio_playback_pwm_cfg);
```

**Return values**

FSP_SUCCESS	Audio Playback module successfully configured.
FSP_ERR_ALREADY_OPEN	Module already open.
FSP_ERR_ASSERTION	One or more pointers point to NULL or callback is NULL.

◆ **RM\_AUDIO\_PLAYBACK\_PWM\_Start()**

```
fsp_err_t RM_AUDIO_PLAYBACK_PWM_Start ( audio_playback_ctrl_t *const p_api_ctrl)
```

Start the PWM HAL driver (AGT or GPT) and timer HAL (AGT or GPT) drivers.

## • Example:

```
/* Start to the play the selected audio stream*/
err = RM_AUDIO_PLAYBACK_PWM_Start(&g_audio_playback_pwm_ctrl);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Audio playback hardware started successfully.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver not open. This function calls <ul style="list-style-type: none"> <li>• <a href="#">timer_api_t::start</a></li> </ul>

◆ **RM\_AUDIO\_PLAYBACK\_PWM\_Stop()**

```
fsp_err_t RM_AUDIO_PLAYBACK_PWM_Stop ( audio_playback_ctrl_t *const p_api_ctrl)
```

Stop the PWM HAL driver (AGT or GPT) and timer HAL driver (AGT or GPT).

## • Example:

```
/* Stop playing. */
err = RM_AUDIO_PLAYBACK_PWM_Stop(&g_audio_playback_pwm_ctrl);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
```

**Return values**

FSP_SUCCESS	Audio playback hardware stopped successfully.
FSP_ERR_ASSERTION	The parameter p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver not open. This function calls <ul style="list-style-type: none"> <li>• <a href="#">timer_api_t::stop</a></li> </ul>

### ◆ RM\_AUDIO\_PLAYBACK\_PWM\_Play()

```
fsp_err_t RM_AUDIO_PLAYBACK_PWM_Play ( audio_playback_ctrl_t *const p_api_ctrl, void const *const p_buffer, uint32_t length )
```

Play a single audio buffer by input samples to the PWM HAL (AGT or GPT) at the sampling frequency configured by the timer.

- Example:

```
/* Set the 16 Bit PCM audio stream to play next */
err = RM_AUDIO_PLAYBACK_PWM_Play(&g_audio_playback_pwm_ctrl, play_buffer,
AUDIO_EXAMPLE_LENGTH);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
```

#### Return values

FSP_SUCCESS	Buffer playback began successfully.
FSP_ERR_ASSERTION	The parameter p_ctrl or p_buffer is NULL or buffer length is greater than 0x10000.
FSP_ERR_NOT_OPEN	Driver not open.. This function calls <ul style="list-style-type: none"> <li>• <a href="#">transfer_api_t::reset</a></li> </ul>

### ◆ RM\_AUDIO\_PLAYBACK\_PWM\_Close()

```
fsp_err_t RM_AUDIO_PLAYBACK_PWM_Close ( audio_playback_ctrl_t *const p_api_ctrl)
```

Closes the module driver. Enables module stop mode.

#### Return values

FSP_SUCCESS	Module successfully closed.
FSP_ERR_NOT_OPEN	Driver not open.
FSP_ERR_ASSERTION	Pointer pointing to NULL.

#### Note

*This function will close all the lower level HAL drivers as well.*

## 4.2.65 AWS PKCS11 PAL (rm\_aws\_pkcs11\_pal)

### Modules

PKCS#11 PAL layer implementation for use by FreeRTOS TLS.

## Overview

*Note*

*The PKCS#11 PAL Interface does not provide any interfaces to the user. Consult the AWS documentation for more info: <https://docs.aws.amazon.com/freertos/latest/portingguide/afr-porting-pkcs.html>.*

## Configuration

There is no user configuration for this module

### Data Flash Usage

The current implementation utilizes 16K of Data flash of which 8K is used for storage and the other 8K is used for backup.

## Usage Notes

### Limitations

- Interrupts are disabled while write or erase operations are being performed.
- Credentials are stored on data flash with no tamper protection other than SHA256 for integrity.
- Credential access is not limited in any way. The credential access and tamper issues can be resolved by updating the implementation to use code flash instead of data flash and using the Secure MPU to control access to it.

### 4.2.66 AWS PKCS11 PAL LITTLEFS (rm\_aws\_pkcs11\_pal\_littlefs)

[Modules](#)

PKCS#11 PAL LittleFS layer implementation for use by FreeRTOS TLS.

## Overview

*Note*

*The PKCS#11 PAL LittleFS Interface does not provide any interfaces to the user. Consult the AWS documentation for more info: <https://docs.aws.amazon.com/freertos/latest/portingguide/afr-porting-pkcs.html>.*

## Configuration

There is no user configuration for this module

## Usage Notes

The current implementation utilizes [LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#) for storage.

### Limitations

- Credential access is not limited in any way.

## 4.2.67 Bluetooth Low Energy Abstraction (rm\_ble\_abs)

### Modules

#### Functions

`fsp_err_t` [RM\\_BLE\\_ABS\\_Open](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_cfg\\_t](#) const \*const p\_cfg)

`fsp_err_t` [RM\\_BLE\\_ABS\\_Close](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl)  
Close the BLE channel. Implements [ble\\_abs\\_api\\_t::close](#). [More...](#)

`fsp_err_t` [RM\\_BLE\\_ABS\\_Reset](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_event\\_cb\\_t](#) init\_callback)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartLegacyAdvertising](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_legacy\\_advertising\\_parameter\\_t](#) const \*const p\_advertising\_parameter)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartExtendedAdvertising](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_extend\\_advertising\\_parameter\\_t](#) const \*const p\_advertising\_parameter)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartNonConnectableAdvertising](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_non\\_connectable\\_advertising\\_parameter\\_t](#) const \*const p\_advertising\_parameter)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartPeriodicAdvertising](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_periodic\\_advertising\\_parameter\\_t](#) const \*const p\_advertising\_parameter)

`fsp_err_t` [RM\\_BLE\\_ABS\\_StartScanning](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl, [ble\\_abs\\_scan\\_parameter\\_t](#) const \*const p\_scan\_parameter)

`fsp_err_t` [RM\\_BLE\\_ABS\\_CreateConnection](#) ([ble\\_abs\\_ctrl\\_t](#) \*const p\_ctrl,

```
ble_abs_connection_parameter_t const *const
p_connection_parameter)
```

```
fsp_err_t RM_BLE_ABS_SetLocalPrivacy (ble_abs_ctrl_t *const p_ctrl, uint8_t
const *const p_lc_irk, uint8_t privacy_mode)
```

```
fsp_err_t RM_BLE_ABS_StartAuthentication (ble_abs_ctrl_t *const p_ctrl,
uint16_t connection_handle)
```

```
fsp_err_t RM_BLE_ABS_DeleteBondInformation (ble_abs_ctrl_t *const p_ctrl,
ble_abs_bond_information_parameter_t const *const
p_bond_information_parameter)
```

## Detailed Description

Middleware for the Bluetooth peripheral on RA MCUs. This module implements the [BLE ABS Interface](#).

## Overview

This module provides BLE GAP functionality that complies with the Bluetooth Core Specification version 5.0 specified by the Bluetooth SIG. This module is configured via the [QE for BLE](#). QE for BLE provides standard services defined by standardization organization and custom services defined by user. [Bluetooth LE Profile API Document User's Manual](#) describes the APIs for standard services.

## Features

The Bluetooth Low Energy Abstraction module supports the following features:

- following GAP Role support
  - Central: The device that sends a connection request to the Peripheral device.
  - Peripheral: The device that accepts a connection request from Central and establishes a connection.
  - Observer : The device that scans for advertising.
  - Broadcaster : The device that sends advertising.
- LE 2M PHY
  - BLE communication is supported on the 2 Msym/s PHY.
- LE Coded PHY -Supports BLE communication on the Coded PHY. This enables communication over longer distances than 1M PHY and 2M PHY.
- LE Advertising Extensions
  - Up to four independent adverts can be executed simultaneously.
  - The size of Advertising Data/Scan Response Data has been expanded to a maximum of 1650 bytes.
  - Periodic Advertising is available.
- LE Channel Selection Algorithm #2
  - With the hopping channel selection algorithm added in Version 5.0, the machine that selects the channel It is possible.
- High Duty Cycle Non-Connectable Advertising
  - The ability to support non-connectable advertising with a minimum interval of up to 20 msec.
- LE Secure Connections
  - Elliptic curve Diffie-Hellman key sharing (ECDH) for pairing with passive

eavesdropping support.

- Link Layer privacy
  - This feature avoids being tracked by other BLE devices by periodically changing the Bluetooth device address.
- Link Layer Extended Scanner Filter policies
  - Scan Filter support for Resolvable private addresses.
- LE Data Packet Length Extension
  - This function expands the packet size of BLE data communications. It is possible to scale up to 251 bytes.
- LE L2CAP Connection Oriented Channel Support
  - The ability to support communication using the L2CAP credit based flow control channel.
- Low Duty Cycle Directed Advertising
  - The ability to support the advertising of the Low Duty Cycle for reconnecting to a known device.
- LE Link Layer Topology
  - It supports both Master and Slave roles and can operate as Master when connected to one remote device and as Slave when connected to another remote device.
- LE Ping
  - This function checks whether the link is maintained or not by requesting the transmission of packets containing MIC after link encryption.

## BLE Library Configuration

There are three types of BLE Protocol Stacks, and the functions provided are different depending on the type of BLE Protocol Stack you select.

BLE library feature	Extended	Balance	Compact
GAP Role	Central Peripheral Observer Broadcaster	Central Peripheral Observer Broadcaster	Peripheral Broadcaster
LE 2M PHY	Yes	Yes	No
LE Coded PHY	Yes	Yes	No
LE Advertising Extensions	Yes	No	No
LE Channel Selection Algorithm #2	Yes	Yes	No
High Duty Cycle Non-Connectable Advertising	Yes	Yes	Yes
LE Secure Connections	Yes	Yes	Yes
Link Layer privacy	Yes	Yes	Yes
Link Layer Extended Scanner Filter policies	Yes	Yes	No
LE Data Packet Length Extension	Yes	Yes	Yes
LE L2CAP Connection Oriented Channel	Yes	No	No

## Support

Low Duty Cycle Directed Advertising	Yes	Yes	Yes
LE Link Layer Topology	Yes	Yes	No
LE Ping	Yes	Yes	Yes
32-bit UUID Support in LE	Yes	Yes	Yes

## Target Devices

The Bluetooth Low Energy Abstraction module supports the following devices.

- RA4W1

## Configuration

### Build Time Configurations for rm\_ble\_abs

The following build time configurations are defined in fsp\_cfg/rm\_ble\_abs\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enable</li> <li>• Disable</li> </ul>	Default (BSP)	Specify whether to include code for API parameter checking. Valid settings include.
Debug Public Address	Must be a valid device address	FF:FF:FF:50:90:74	Public Address of firmware initial value.
Debug Random Address	Must be a valid device address	FF:FF:FF:FF:FF:FF	Random Address of firmware initial value.
Maximum number of connections	Value must be an integer between 1 and 7	7	Maximum number of connections.
Maximum connection data length	Value must be an integer between 27 and 251	251	Maximum connection data length.
Maximum advertising data length	Value must be an integer between 31 and 1650	1650	Maximum advertising data length.
Maximum advertising set number	Value must be an integer between 1 and 4	4	Maximum advertising set number.
Maximum periodic sync set number.	Value must be an integer between 1 and 2	2	Maximum periodic sync set number.
Store Security Data	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Store Security Data in DataFlash.

Data Flash Block for Security Data	Value must be an integer between 0 and 7	0	Data Flash Block for Security Data Management.
Remote Device Bonding Number	Value must be an integer between 1 and 7	7	Number of remote device bonding information.
Connection Event Start Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Connection event start notify enable/disable.
Connection Event Close Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Connection event close notify enable/disable.
Advertising Event Start Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Advertising event start notify enable/disable.
Advertising Event Close Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Advertising event close notify enable/disable.
Scanning Event Start Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Scanning event start notify enable/disable.
Scanning Event Close Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Scanning event close notify enable/disable.
Initiating Event Start Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Initiating event start notify enable/disable.
Initiating Event Close Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set Initiating event close notify enable/disable.
RF Deep Sleep Start Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set RF_DEEP_SLEEP start notify enable/disable.
RF Deep Sleep Wakeup Notify	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set RF_DEEP_SLEEP wakeup notify enable/disable.
Bluetooth dedicated clock	Value must be an integer between 0 and 15	6	Load capacitance adjustment.
DC-DC converter	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Set DC-DC converter for RF part.
Slow Clock Source	<ul style="list-style-type: none"> <li>• Use RF_LOCO</li> <li>• Use External 32.768kHz</li> </ul>	Use RF_LOCO	Set slow clock source for RF part.
MCU CLKOUT Port	<ul style="list-style-type: none"> <li>• P109</li> </ul>	P109	When BLE_ABS_CFG_RF

	<ul style="list-style-type: none"> <li>• P205</li> </ul>		_EXTERNAL_32K_ENAB LE = 1, Set port of MCU CLKOUT.
MCU CLKOUT Frequency Output	<ul style="list-style-type: none"> <li>• MCU CLKOUT frequency 32.768kHz</li> <li>• MCU CLKOUT frequency 16.384kHz</li> </ul>	MCU CLKOUT frequency 32.768kHz	When BLE_ABS_CFG_RF _EXTERNAL_32K_ENAB LE = 1, set frequency output from CLKOUT of MCU part.
Sleep Clock Accuracy(SCA)	Value must be an integer between 0 and 500	250	When BLE_ABS_CFG_RF _EXTERNAL_32K_ENAB LE = 1, set Sleep Clock Accuracy(SCA) for RF slow clock.
Transmission Power Maximum Value	<ul style="list-style-type: none"> <li>• max +0dBm</li> <li>• max +4dBm</li> </ul>	max +4dBm	Set transmission power maximum value.
Transmission Power Default Value	<ul style="list-style-type: none"> <li>• High 0dBm(Tran smission Power Maximum Value = +0dBm) / +4 dBm(Transmissi on Power Maximum Value = +4dBm)</li> <li>• Mid 0dBm(Tran smission Power Maximum Value = +0dBm) / 0d Bm(Transmissio n Power Maximum Value = +4dBm)</li> <li>• Low -18dBm(Tr ansmission Power Maximum Value = +0dBm) / -20 dBm(Transmissi on Power Maximum Value = +4dBm)</li> </ul>	High 0dBm(Transmission Power Maximum Value = +0dBm) / +4dBm(Transmission Power Maximum Value = +4dBm)	Set default transmit power. Default transmit power is dependent on the configuration of Maximum transmission power(BLE_ABS_CFG_R F_DEF_TX_POW).
CLKOUT_RF Output	<ul style="list-style-type: none"> <li>• No output</li> <li>• 4MHz output</li> <li>• 2MHz output</li> <li>• 1MHz output</li> </ul>	No output	Set CLKOUT_RF output setting.
RF_DEEP_SLEEP Transition	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Set RF_DEEP_SLEEP transition.
MCU Main Clock Frequency	Value must be an integer between 1000 and 20000	8000	Set MCU Main Clock Frequency (kHz). Set clock source according

to your board environment. HOCO: don't care. / Main Clock: 1000 to 20000 kHz / PLL Circuit: 4000 to 12500 kHz

Code Flash(ROM) Device Data Block	Value must be an integer between -1 and 255	255	Device specific data block on Code Flash (ROM).
Device Specific Data Flash Block	Value must be an integer between -1 and 7	-1	Device specific data block on E2 Data Flash.
MTU Size Configured	Value must be an integer between 23 and 247	247	MTU Size configured by GATT MTU exchange procedure.
Timer Slot Maximum Number	Value must be an integer between 1 and 10	10	The maximum number of timer slot.

### Configurations for Middleware > BLE > BLE Abstraction Driver on rm\_ble\_abs

This module can be added to the Stacks tab via New Stack > Middleware > BLE > BLE Abstraction Driver on rm\_ble\_abs.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_ble_abs0	Module name.
General > Gap callback	Name must be a valid C symbol	gap_cb	A user callback function must be provided if the BLE_ABS is configured to generate a GAP. If QE is used, set to NULL.
General > Vendor specific callback	Name must be a valid C symbol	vs_cb	A user callback function must be provided if the BLE_ABS is configured to generate a Vendor Specific. If QE is used, set to NULL.
General > GATT server callback parameter	Name must be a valid C symbol	gs_abs_gatts_cb_param	Set GATT server callback parameter. If QE is used, set to NULL.
General > GATT server callback number	Must be a valid number	2	The number of GATT Server callback functions.

General > GATT client callback parameter	Name must be a valid C symbol	gs_abs_gattc_cb_param	Set GATT client callback parameter. If QE is used, set to NULL.
General > GATT client callback number	Must be a valid number	2	The number of GATT Server callback functions.
Security > Pairing parameters	Name must be a valid C symbol	gs_abs_pairing_param	Set pairing parameters.
Security > IO capabilities of local device.	<ul style="list-style-type: none"> <li>• BLE_GAP_IOCAP_DISPLAY_ONLY</li> <li>• BLE_GAP_IOCAP_DISPLAY_YESNO</li> <li>• BLE_GAP_IOCAP_KEYBOARD_ONLY</li> <li>• BLE_GAP_IOCAP_NOINPUT_NOOUTPUT</li> <li>• BLE_GAP_IOCAP_KEYBOARD_DISPLAY</li> </ul>	BLE_GAP_IOCAP_NOINPUT_NOOUTPUT	Select IO capabilities of local device.
Security > MITM protection policy.	<ul style="list-style-type: none"> <li>• BLE_GAP_SEC_MITM_BEST_EFFORT</li> <li>• BLE_GAP_SEC_MITM_STRICT</li> </ul>	BLE_GAP_SEC_MITM_BEST_EFFORT	Select MITM protection policy.
Security > Determine whether to accept only Secure Connections or not.	<ul style="list-style-type: none"> <li>• BLE_GAP_SC_BEST_EFFORT</li> <li>• BLE_GAP_SC_STRICT</li> </ul>	BLE_GAP_SC_BEST_EFFORT	Select determine whether to accept only Secure Connections or not.
Security > Type of keys to be distributed from local device.	<ul style="list-style-type: none"> <li>• BLE_GAP_KEY_DIST_ENCKEY</li> <li>• BLE_GAP_KEY_DIST_IDKEY</li> <li>• BLE_GAP_KEY_DIST_SIGNKEY</li> </ul>		Select type of keys to be distributed from local device.
Security > Type of keys which local device requests a remote device to distribute.	<ul style="list-style-type: none"> <li>• BLE_GAP_KEY_DIST_ENCKEY</li> <li>• BLE_GAP_KEY_DIST_IDKEY</li> <li>• BLE_GAP_KEY_DIST_SIGNKEY</li> </ul>		Set type of keys which local device requests a remote device to distribute.
Security > Maximum LTK size.	Valid range is 7 - 16	16	Set Maximum LTK size.
Interrupts > Callback provided when an ISR occurs	Name must be a valid C symbol	NULL	Callback provided when BLE ABS ISR occurs

## Clock Configuration

### Note

*System clock (ICLK): 8 MHz or more*

*Peripheral module clock A (PCLKA): 8MHz or more*

*The BLE Protocol Stack is optimized for ICLK and PCLKA frequencies of 32 MHz.*

*It is recommended that the clock be set so that the ICLK and PCLKA frequencies are 32MHz in order to get the best performance from the BLE.*

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the BLE\_ABS:

## Examples

### BLE\_ABS Basic Example

This is a basic example of minimal use of the BLE\_ABS in an application.

```
#define BLE_ABS_EVENT_FLAG_STACK_ON (0x01 << 0)
#define BLE_ABS_EVENT_FLAG_CONN_IND (0x01 << 1)
#define BLE_ABS_EVENT_FLAG_ADV_ON (0x01 << 2)
#define BLE_ABS_EVENT_FLAG_ADV_OFF (0x01 << 3)
#define BLE_ABS_EVENT_FLAG_DISCONN_IND (0x01 << 4)
#define BLE_ABS_EVENT_FLAG_RSLV_LIST_CONF_COMP (0x01 << 5)
#define BLE_ABS_EXAMPLE_SHORTENED_LOCAL_NAME 'E', 'x', 'a', 'm', 'p', 'l', 'e'
#define BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME 'T', 'E', 'S', 'T', '_', 'E', 'x', 'a', 'm', 'p', 'l', 'e'
#define BLE_ABS_EXAMPLE_SLOW_ADVERTISING_INTERVAL (0x00000640)
void ble_abs_peripheral_example (void)
{
    fsp_err_t      err      = FSP_SUCCESS;
    volatile uint32_t timeout = UINT16_MAX * UINT8_MAX * 8;
    uint8_t * p_lc_irk      = NULL;
    uint8_t  privacy_mode   = BLE_GAP_NET_PRIV_MODE;
    uint8_t  advertising_data[] =
    {
```

```
/* Flags */
    0x02,
    0x01,
    (0x1a),
/* Shortened Local Name */
    0x08,
    0x08,
    BLE_ABS_EXAMPLE_SHORTENED_LOCAL_NAME,
};
/* Scan Response Data */
uint8_t scan_response_data[] =
{
/* Complete Local Name */
    0x0D,
    0x09,
    BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME,
};
ble_abs_legacy_advertising_parameter_t legacy_advertising_parameter =
{
    .p_peer_address          =
NULL,
    .slow_advertising_interval =
BLE_ABS_EXAMPLE_SLOW_ADVERTISING_INTERVAL,
    .slow_advertising_period  =
0x0000,
    .p_advertising_data      =
advertising_data,
    .advertising_data_length  = sizeof
(advertising_data),
    .p_scan_response_data    =
scan_response_data,
    .scan_response_data_length = sizeof
(scan_response_data),
    .advertising_filter_policy = BLE_ABS_ADVERTISING_FILTER_ALLOW_ANY
```

```
,
    .advertising_channel_map    = (BLE_GAP_ADV_CH_37 | BLE_GAP_ADV_CH_38 |
BLE_GAP_ADV_CH_39),
    .own_bluetooth_address_type = BLE_GAP_ADDR_PUBLIC
},
    .own_bluetooth_address      = {0},
};

g_ble_event_flag = 0;
/* Open the module. */
err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Wait BLE_GAP_EVENT_STACK_ON event is notified. */
while (!(BLE_ABS_EVENT_FLAG_STACK_ON & g_ble_event_flag) && (--timeout > 0U))
{
R_BLE_Execute();
}
/* Set local privacy. */
err = RM_BLE_ABS_SetLocalPrivacy(&g_ble_abs0_ctrl, p_lc_irk, privacy_mode);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Wait BLE_GAP_EVENT_RSLV_LIST_CONF_COMP event is notified. */
while (!(BLE_ABS_EVENT_FLAG_RSLV_LIST_CONF_COMP & g_ble_event_flag) && (--timeout >
0U))
{
R_BLE_Execute();
}
time_out_handle_error(timeout);
g_ble_event_flag = 0;
timeout = UINT16_MAX * UINT8_MAX * 8;
/* Start advertising. */
err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
&legacy_advertising_parameter);
/* Handle any errors. This function should be defined by the user. */
```

```
    assert(FSP_SUCCESS == err);

    while (!(BLE_ABS_EVENT_FLAG_CONN_IND & g_ble_event_flag) && (--timeout > 0U))
    {
        if (BLE_ABS_EVENT_FLAG_ADV_OFF & g_ble_event_flag)
        {
            /* Restart advertise, when stop advertising. */
            err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
&legacy_advertising_parameter);
            if (FSP_SUCCESS == err)
            {
                g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_ADV_OFF;
            }
        }
        else if (FSP_ERR_INVALID_STATE == err)
        {
            /* BLE driver state is busy. */
            ;
        }
        else
        {
            /* Handle any errors. This function should be defined by the user. */
            assert(FSP_SUCCESS == err);
        }
    }
    else if ((timeout % BLE_ABS_RETRY_INTERVAL) == 0U)
    {
        /* Stop advertising after a certain amount of time */
        R_BLE_GAP_StopAdv(g_advertising_handle);
    }
    else
    {
        ;
    }

    R_BLE_Execute();
}
```

```
    time_out_handle_error(timeout);
/* Clean up & Close BLE driver */
    g_ble_event_flag = 0;
/* Close BLE driver */
    err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
}
```

```
#define BLE_ABS_EVENT_FLAG_STACK_ON (0x01 << 0)
#define BLE_ABS_EVENT_FLAG_CONN_IND (0x01 << 1)
#define BLE_ABS_EVENT_FLAG_ADV_REPT_IND (0x01 << 2)
#define BLE_ABS_EVENT_FLAG_ADV_OFF (0x01 << 3)
#define BLE_ABS_EVENT_FLAG_PAIRING_COMP (0x01 << 4)
#define BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT (0x01 << 5)
#define BLE_ABS_EVENT_FLAG_DELETE_BOND_COMP (0x01 << 6)
#define BLE_ABS_EXAMPLE_FAST_SCAN_INTERVAL (0x0060)
#define BLE_ABS_EXAMPLE_FAST_SCAN_WINDOW (0x0030)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_INTERVAL (0x0800)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_WINDOW (0x0012)
#define BLE_ABS_EXAMPLE_FAST_SCAN_PERIOD (0x0BB8)
#define BLE_ABS_EXAMPLE_SLOW_SCAN_PERIOD (0x0000)
#define BLE_ABS_EXAMPLE_CONNECTION_INTERVAL (0x0028)
#define BLE_ABS_EXAMPLE_SUPERVISION_TIMEOUT (0x0200)
#define BLE_ABS_SCAN_FILTER_DATA_LENGTH (12)
/* Scan filter data (data type: Complete Local Name) */
static uint8_t g_filter_data[] =
{
    BLE_ABS_EXAMPLE_COMPLETE_LOCAL_NAME
};
/* Connection phy parameters */
ble_abs_connection_phy_parameter_t g_connection_phy_parameter =
{
    .connection_interval = BLE_ABS_EXAMPLE_CONNECTION_INTERVAL, /* 50.0(ms) */

```

```
.supervision_timeout      = BLE_ABS_EXAMPLE_SUPERVISION_TIMEOUT, /* 5,120(ms) */
.connection_slave_latency = 0x0000,
};
/* Connection device address */
ble_device_address_t g_connection_device_address;
/* Connection parameters */
ble_abs_connection_parameter_t g_connection_parameter =
{
    .p_connection_phy_parameter_lm = &g_connection_phy_parameter,
    .p_device_address              = &g_connection_device_address,
    .filter_parameter              = BLE_GAP_INIT_FILT_USE_ADDR,
    .connection_timeout            = 0x05, /* 5(s) */
};
ble_abs_bond_information_parameter_t g_bond_information_parameter =
{
    .local_bond_information        = BLE_ABS_LOCAL_BOND_INFORMATION_ALL,
    .remote_bond_information       = BLE_ABS_REMOTE_BOND_INFORMATION_ALL,
    .delete_non_volatile_area      = BLE_ABS_DELETE_NON_VOLATILE_AREA_ENABLE,
    .p_address                    = NULL,
    .abs_delete_bond_callback      = delete_bond_cb,
};
void ble_abs_central_example (void)
{
    fsp_err_t      err      = FSP_SUCCESS;
    volatile uint32_t timeout = UINT16_MAX * UINT8_MAX * 8;
    g_connection_handle = BLE_GAP_INVALID_CONN_HDL;
    static ble_abs_scan_phy_parameter_t scan_phy_parameter =
    {
        .fast_scan_interval = BLE_ABS_EXAMPLE_FAST_SCAN_INTERVAL, /* 60.0(ms) */
        .fast_scan_window   = BLE_ABS_EXAMPLE_FAST_SCAN_WINDOW,   /* 30.0(ms) */
        .slow_scan_interval = BLE_ABS_EXAMPLE_SLOW_SCAN_INTERVAL, /* 1,280.0(ms) */
        .slow_scan_window   = BLE_ABS_EXAMPLE_SLOW_SCAN_WINDOW,   /* 11.25(ms) */
        .scan_type           = BLE_GAP_SCAN_ACTIVE
    };
};
```

```
/* Scan parameters */
ble_abs_scan_parameter_t scan_parameter =
{
    .p_phy_parameter_1M      = &scan_phy_parameter,
    .fast_scan_period        = BLE_ABS_EXAMPLE_FAST_SCAN_PERIOD, /* 30,000(ms)
*/
    .slow_scan_period        = BLE_ABS_EXAMPLE_SLOW_SCAN_PERIOD,
    .p_filter_data           = g_filter_data,
    .filter_data_length      = (uint16_t) BLE_ABS_SCAN_FILTER_DATA_LENGTH,
    .filter_ad_type          = 0x09, /* Data type:
Complete Local Name */
    .device_scan_filter_policy = BLE_GAP_SCAN_ALLOW_ADV_ALL,
    .filter_duplicate        = BLE_GAP_SCAN_FILT_DUPLIC_ENABLE,
};
g_ble_event_flag = 0;
/* Open the module. */
err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Connection parameters */
while (!(BLE_ABS_EVENT_FLAG_STACK_ON & g_ble_event_flag) && (--timeout > 0U))
{
    R_BLE_Execute();
}
/* Start scanning. */
err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
while ((BLE_ABS_EVENT_FLAG_ADV_REPT_IND & g_ble_event_flag) && (--timeout > 0U))
{
    if ((BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT & g_ble_event_flag) || (BLE_GAP_EVENT_SCAN_OFF
& g_ble_event_flag))
    {
        g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_ADV_OFF;
```

```
        g_ble_event_flag &= (uint16_t) ~BLE_ABS_EVENT_FLAG_SCAN_TIMEOUT;
/* Start scanning. */
    err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
}
else if ((timeout % BLE_ABS_RETRY_INTERVAL) == 0U)
{
/* Stop scanning after a certain amount of time */
R_BLE_GAP_StopScan();
}
else
{
    ;
}
R_BLE_Execute();
}
g_ble_event_flag = 0;
time_out_handle_error(timeout);
timeout = UINT16_MAX * UINT8_MAX * 8;
/* Create connection with remote device. */
err = RM_BLE_ABS_CreateConnection(&g_ble_abs0_ctrl, &g_connection_parameter);
/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);
/* Wait BLE_GAP_EVENT_CONN_IND event is notified. */
while (!(BLE_ABS_EVENT_FLAG_CONN_IND & g_ble_event_flag) && (--timeout > 0U))
{
R_BLE_Execute();
}
time_out_handle_error(timeout);
g_ble_event_flag = 0;
timeout = UINT16_MAX * UINT8_MAX * 8;
/* Start authentication with remote device. */
err = RM_BLE_ABS_StartAuthentication(&g_ble_abs0_ctrl, g_connection_handle);
```

```
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

/* Wait BLE_GAP_EVENT_PAIRING_COMP event is notified. */
while (!(BLE_ABS_EVENT_FLAG_PAIRING_COMP & g_ble_event_flag) && (--timeout > 0U))
    {
    R_BLE_Execute();
    }
    time_out_handle_error(timeout);
    g_ble_event_flag = 0;
    timeout = UINT16_MAX * UINT8_MAX * 8;
/* Delete bonding information. */
    err = RM_BLE_ABS_DeleteBondInformation(&g_ble_abs0_ctrl,
&g_bond_information_parameter);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

/* Wait delete_bond_cb application callback function is called. */
while (!(BLE_ABS_EVENT_FLAG_DELETE_BOND_COMP & g_ble_event_flag) && (--timeout >
0U))
    {
    R_BLE_Execute();
    }
    time_out_handle_error(timeout);
/* Clean up & Close BLE driver */
    g_ble_event_flag = 0;
    err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
}

void delete_bond_cb (st_ble_dev_addr_t * p_addr) {
    (void) p_addr;
    g_ble_event_flag = g_ble_event_flag | BLE_ABS_EVENT_FLAG_DELETE_BOND_COMP;
}
}
```

## Data Structures

```
struct abs_advertising_parameter_t
```

```
struct abs_scan_parameter_t
```

```
struct ble_abs_instance_ctrl_t
```

```
struct st_ble_rf_notify_t
```

This structure is RF event notify management. [More...](#)

## Typedefs

```
typedef void(* ble_abs_timer_cb_t) (uint32_t timer_hdl)
```

```
typedef void(* ble_mcu_clock_change_cb_t) (void)
```

`ble_mcu_clock_change_cb_t` is the callback function type to use `CLKOUT_RF` as the MCU main clock source. [More...](#)

```
typedef void(* ble_rf_notify_cb_t) (uint32_t)
```

`ble_rf_notify_cb_t` is the RF event notify callback function type. [More...](#)

## Enumerations

```
enum e_ble_timer_type_t
```

## Data Structure Documentation

### ◆ abs\_advertising\_parameter\_t

struct abs_advertising_parameter_t		
advertising set parameters structure		
Data Fields		
union <a href="#">abs_advertising_parameter_t</a>	advertising_parameter	Advertising parameters.
uint32_t	advertising_status	Advertising status.
<a href="#">ble_device_address_t</a>	remote_device_address	Remote device address for direct advertising.

### ◆ abs\_scan\_parameter\_t

struct abs_scan_parameter_t		
scan parameters structure		
Data Fields		
<a href="#">ble_abs_scan_parameter_t</a>	scan_parameter	Scan parameters.

<a href="#">ble_abs_scan_phy_parameter_t</a>	scan_phy_parameter_1M	1M phy parameters for scan.
<a href="#">ble_abs_scan_phy_parameter_t</a>	scan_phy_parameter_coded	Coded phy parameters for scan. */.
uint32_t	scan_status	

#### ◆ ble\_abs\_instance\_ctrl\_t

struct ble_abs_instance_ctrl_t		
BLE ABS private control block. DO NOT MODIFY. Initialization occurs when <a href="#">RM_BLE_ABS_Open()</a> is called.		
Data Fields		
uint32_t	open	Indicates whether the <a href="#">open()</a> API has been successfully called.
void const *	p_context	Placeholder for user data. Passed to the user callback in <a href="#">ble_abs_callback_args_t</a> .
<a href="#">ble_gap_application_callback_t</a>	abs_gap_callback	GAP callback function.
<a href="#">ble_vendor_specific_application_callback_t</a>	abs_vendor_specific_callback	Vendor specific callback function.
<a href="#">ble_abs_delete_bond_application_callback_t</a>	abs_delete_bond_callback	Delete bond information callback function.
uint32_t	connection_timer_handle	Cancel a request for connection timer.
uint32_t	advertising_timer_handle	Advertising timer for legacy advertising.
uint32_t	scan_timer_handle	Scan interval timer.
<a href="#">abs_advertising_parameter_t</a>	advertising_sets[ <a href="#">BLE_MAX_NO_OF_ADV_SETS_SUPPORTED</a> ]	Advertising set information.
<a href="#">abs_scan_parameter_t</a>	abs_scan	Scan information.
<a href="#">st_ble_dev_addr_t</a>	loc_bd_addr	Local device address.
uint8_t	privacy_mode	Privacy mode.
uint32_t	set_privacy_status	Local privacy status.
<a href="#">ble_abs_timer_t</a>	timer[ <a href="#">BLE_ABS_CFG_TIMER_NUMBER_OF_SLOT</a> ]	
uint32_t	current_timeout_ms	Current timeout.
uint32_t	elapsed_timeout_ms	Elapsed timeout.
<a href="#">ble_abs_cfg_t</a> const *	p_cfg	Pointer to the BLE ABS configuration block.

◆ **st\_ble\_rf\_notify\_t**

struct st_ble_rf_notify_t		
This structure is RF event notify management.		
Data Fields		
uint32_t	enable	Set enable/disable of each RF event notification.  Bit0 Notify Connection event start(0:Disable/1:Enable) Bit1 Notify Advertising event start(0:Disable/1:Enable) Bit2 Notify Scanning event start(0:Disable/1:Enable) Bit3 Notify Initiating event start(0:Disable/1:Enable) Bit4 Notify Connection event close(0:Disable/1:Enable) Bit5 Notify Advertising event close(0:Disable/1:Enable) Bit6 Notify Scanning event close(0:Disable/1:Enable) Bit7 Notify Initiating event close(0:Disable/1:Enable) Bit8 Notify RF_DEEP_SLEEP event start(0:Disable/1:Enable) Bit9 Notify RF_DEEP_SLEEP event close(0:Disable/1:Enable) Other Bit: Reserved for future use.
ble_rf_notify_cb_t	start_cb	Set callback function pointer for RF event start.
ble_rf_notify_cb_t	close_cb	Set callback function pointer for RF event close.
ble_rf_notify_cb_t	dsleep_cb	Set callback function pointer for RF_DEEP_SLEEP.

**Typedef Documentation**◆ **ble\_abs\_timer\_cb\_t**

typedef void(* ble_abs_timer_cb_t) (uint32_t timer_hdl)
The timer callback invoked when the timer expired.

## ◆ ble\_mcu\_clock\_change\_cb\_t

ble\_mcu\_clock\_change\_cb\_t

ble\_mcu\_clock\_change\_cb\_t is the callback function type to use CLKOUT\_RF as the MCU main clock source.

**Parameters**

none	
------	--

**Returns**

none

## ◆ ble\_rf\_notify\_cb\_t

ble\_rf\_notify\_cb\_t

ble\_rf\_notify\_cb\_t is the RF event notify callback function type.

**Parameters**

[in]	uint32_t	The information of RF event notification.
------	----------	---

**Returns**

none

**Enumeration Type Documentation**

## ◆ e\_ble\_timer\_type\_t

enum e\_ble\_timer\_type\_t

The timer type.

Enumerator	
BLE_TIMER_ONE_SHOT	One shot timer type
BLE_TIMER_PERIODIC	Periodic timer type

**Function Documentation**

### ◆ RM\_BLE\_ABS\_Open()

```
fsp_err_t RM_BLE_ABS_Open ( ble_abs_ctrl_t *const p_ctrl, ble_abs_cfg_t const *const p_cfg )
```

Host stack is initialized with this function. Before using All the R\_BLE APIs, it's necessary to call this function. A callback functions are registered with this function. In order to receive the GAP, GATT, Vendor specific event, it's necessary to register a callback function. The result of this API call is notified in BLE\_GAP\_EVENT\_STACK\_ON event. Implements `ble_abs_api_t::open`.

Example:

```
/* Open the module. */
err = RM_BLE_ABS_Open(&g_ble_abs0_ctrl, &g_ble_abs0_cfg);
```

#### Return values

FSP_SUCCESS	Channel opened successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_INVALID_CHANNEL	The channel number is invalid.
FSP_ERR_ALREADY_OPEN	Requested channel is already open in a different configuration.
FSP_ERR_INVALID_ARGUMENT	Invalid input parameter.

### ◆ RM\_BLE\_ABS\_Close()

```
fsp_err_t RM_BLE_ABS_Close ( ble_abs_ctrl_t *const p_ctrl)
```

Close the BLE channel. Implements `ble_abs_api_t::close`.

Example:

```
/* Close BLE driver */
err = RM_BLE_ABS_Close(&g_ble_abs0_ctrl);
```

#### Return values

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_NOT_OPEN	Control block not open.

◆ **RM\_BLE\_ABS\_Reset()**

```
fsp_err_t RM_BLE_ABS_Reset ( ble_abs_ctrl_t *const p_ctrl, ble_event_cb_t init_callback )
```

BLE is reset with this function. The process is carried out in the following order. [R\\_BLE\\_Close\(\)](#) -> [R\\_BLE\\_GAP\\_Terminate\(\)](#) -> [R\\_BLE\\_Open\(\)](#) -> [R\\_BLE\\_SetEvent\(\)](#). The `init_cb` callback initializes the others (Host Stack, timer, etc...). Implements [ble\\_abs\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Channel closed successfully.
FSP_ERR_ASSERTION	Null pointer presented.
FSP_ERR_NOT_OPEN	Control block not open.

◆ **RM\_BLE\_ABS\_StartLegacyAdvertising()**

```
fsp_err_t RM_BLE_ABS_StartLegacyAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_legacy_advertising_parameter_t const *const p_advertising_parameter )
```

Start Legacy Advertising after setting advertising parameters, advertising data and scan response data. The legacy advertising uses the advertising set whose advertising handle is 0. The advertising type is connectable and scannable(ADV\_IND). The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Implements [ble\\_abs\\_api\\_t::startLegacyAdvertising](#)

Example:

```
/* Start advertising. */
err = RM_BLE_ABS_StartLegacyAdvertising(&g_ble_abs0_ctrl,
&legacy_advertising_parameter);
```

**Return values**

FSP_SUCCESS	Operation succeeded
FSP_ERR_ASSERTION	<code>p_instance_ctrl</code> is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_POINTER	<code>p_advertising_parameter</code> is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.

### ◆ RM\_BLE\_ABS\_StartExtendedAdvertising()

```
fsp_err_t RM_BLE_ABS_StartExtendedAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_extend_advertising_parameter_t const *const p_advertising_parameter )
```

Start Extended Advertising after setting advertising parameters, advertising data. The extended advertising uses the advertising set whose advertising handle is 1. The advertising type is connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Implements [ble\\_abs\\_api\\_t::startExtendedAdvertising](#)

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.
FSP_ERR_UNSUPPORTED	Subordinate modules do not support this feature.

### ◆ RM\_BLE\_ABS\_StartNonConnectableAdvertising()

```
fsp_err_t RM_BLE_ABS_StartNonConnectableAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_non_connectable_advertising_parameter_t const *const p_advertising_parameter )
```

Start Non-Connectable Advertising after setting advertising parameters, advertising data. The non-connectable advertising uses the advertising set whose advertising handle is 2. The advertising type is non-connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Secondary Advertising Max Skip is 0. Implements [ble\\_abs\\_api\\_t::startNonConnectableAdvertising](#).

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_STATE	Host stack hasn't been initialized.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.

### ◆ RM\_BLE\_ABS\_StartPeriodicAdvertising()

```
fsp_err_t RM_BLE_ABS_StartPeriodicAdvertising ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_periodic_advertising_parameter_t const *const p_advertising_parameter )
```

Start Periodic Advertising after setting advertising parameters, periodic advertising parameters, advertising data and periodic advertising data. The periodic advertising uses the advertising set whose advertising handle is 3. The advertising type is non-connectable and non-scannable. The address type of local device is Public Identity Address or RPA(If the resolving list contains no matching entry, use the public address.). Scan request event(BLE\_GAP\_EVENT\_SCAN\_REQ\_RECV) is not notified. Secondary Advertising Max Skip is 0. Implements [ble\\_abs\\_api\\_t::startPeriodicAdvertising](#)

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_advertising_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The advertising parameter is out of range.
FSP_ERR_UNSUPPORTED	This feature is not supported in this configuration.

### ◆ RM\_BLE\_ABS\_StartScanning()

```
fsp_err_t RM_BLE_ABS_StartScanning ( ble_abs_ctrl_t *const p_ctrl, ble_abs_scan_parameter_t
const *const p_scan_parameter )
```

Start scanning after setting scan parameters. The scanner address type is Public Identity Address. Fast scan is followed by slow scan. The end of fast scan or slow scan is notified with BLE\_GAP\_EVENT\_SCAN\_TO event. If fast\_period is 0, only slow scan is carried out. If scan\_period is 0, slow scan continues. Implements `ble_abs_api_t::startScanning`.

Example:

```
/* Start scanning. */
err = RM_BLE_ABS_StartScanning(&g_ble_abs0_ctrl, &scan_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_scan_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The scan parameter is out of range.
FSP_ERR_IN_USE	This API is called in scanning.
FSP_ERR_BLE_ABS_NOT_FOUND	Usable timer slot not found.
FSP_ERR_UNSUPPORTED	This feature is not supported in this configuration.

### ◆ RM\_BLE\_ABS\_CreateConnection()

```
fsp_err_t RM_BLE_ABS_CreateConnection ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_connection_parameter_t const *const p_connection_parameter )
```

Request create connection. The initiator address type is Public Identity Address. The scan interval is 60ms and the scan window is 30ms in case of 1M PHY or 2M PHY. The scan interval is 180ms and the scan window is 90ms in case of coded PHY. The Minimum CE Length and the Maximum CE Length are 0xFFFF. When the request for a connection has been received by the Controller, BLE\_GAP\_EVENT\_CREATE\_CONN\_COMP event is notified. When a link has been established, BLE\_GAP\_EVENT\_CONN\_IND event is notified. Implements [ble\\_abs\\_api\\_t::createConnection](#).

Example:

```
/* Create connection with remote device. */
err = RM_BLE_ABS_CreateConnection(&g_ble_abs0_ctrl, &g_connection_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_POINTER	p_connection_parameter is specified as NULL.
FSP_ERR_INVALID_ARGUMENT	The create connection parameter is out of range.
FSP_ERR_IN_USE	This API is called while creating a link by previous API call.
FSP_ERR_BLE_ABS_NOT_FOUND	Couldn't find a valid timer.
FSP_ERR_UNSUPPORTED	This feature is not supported in this configuration.

### ◆ RM\_BLE\_ABS\_SetLocalPrivacy()

```
fsp_err_t RM_BLE_ABS_SetLocalPrivacy ( ble_abs_ctrl_t *const p_ctrl, uint8_t const *const p_lc_irk,
uint8_t privacy_mode )
```

Generate a IRK, add it to the resolving list, set privacy mode and enable RPA function. Register vendor specific callback function, if IRK is generated by this function. After configuring local device privacy, BLE\_GAP\_ADDR\_RPA\_ID\_PUBLIC is specified as own device address in the advertising/scan/create connection API. Implements [ble\\_abs\\_api\\_t::setLocalPrivacy](#)

Example:

```
/* Set local privacy. */
err = RM_BLE_ABS_SetLocalPrivacy(&g_ble_abs0_ctrl, p_lc_irk, privacy_mode);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl is specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_ARGUMENT	The privacy_mode parameter is out of range.
FSP_ERR_BLE_ABS_INVALID_OPERATION	Host stack hasn't been initialized. configuring the resolving list or privacy mode.

### ◆ RM\_BLE\_ABS\_StartAuthentication()

```
fsp_err_t RM_BLE_ABS_StartAuthentication ( ble_abs_ctrl_t *const p_ctrl, uint16_t
connection_handle )
```

Start pairing or encryption. If pairing has been done, start encryption. The pairing parameters are configured by [RM\\_BLE\\_ABS\\_Open\(\)](#) or [R\\_BLE\\_GAP\\_SetPairingParams\(\)](#). If the pairing parameters are configure by [RM\\_BLE\\_ABS\\_Open\(\)](#),

- bonding policy is that bonding information is stored.
- Key press notification is not supported. Implements [ble\\_abs\\_api\\_t::startAuthentication](#).

Example:

```
/* Start authentication with remote device. */
err = RM_BLE_ABS_StartAuthentication(&g_ble_abs0_ctrl, g_connection_handle);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	p_instance_ctrl or connection_handle are specified as NULL.
FSP_ERR_NOT_OPEN	Control block not open.
FSP_ERR_INVALID_ARGUMENT	The connection handle parameter is out of range.

### ◆ RM\_BLE\_ABS\_DeleteBondInformation()

```
fsp_err_t RM_BLE_ABS_DeleteBondInformation ( ble_abs_ctrl_t *const p_ctrl,
ble_abs_bond_information_parameter_t const *const p_bond_information_parameter )
```

Delete bonding information from BLE stack and storage. Implements [ble\\_abs\\_api\\_t::deleteBondInformation](#).

Example:

```
/* Delete bonding information. */
err = RM_BLE_ABS_DeleteBondInformation(&g_ble_abs0_ctrl,
&g_bond_information_parameter);
```

#### Return values

FSP_SUCCESS	Operation succeeded.
FSP_ERR_ASSERTION	The parameter p_instance_ctrl is NULL.
FSP_ERR_INVALID_POINTER	The parameter p_bond_information_parameter is NULL.
FSP_ERR_NOT_OPEN	Control block not open.

## 4.2.68 SD/MMC Block Media Implementation (rm\_block\_media\_sdmmc)

### Modules

#### Functions

fsp_err_t	RM_BLOCK_MEDIA_SDMMC_Open (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_cfg_t const *const p_cfg)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_MediaInit (rm_block_media_ctrl_t *const p_ctrl)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_Read (rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address, uint32_t const num_blocks)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_Write (rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const p_src_address, uint32_t const block_address, uint32_t const num_blocks)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_Erase (rm_block_media_ctrl_t *const p_ctrl, uint32_t const block_address, uint32_t const num_blocks)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_CallbackSet (rm_block_media_ctrl_t *const p_ctrl, void(*p_callback)(rm_block_media_callback_args_t *), void const *const p_context, rm_block_media_callback_args_t *const p_callback_memory)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_StatusGet (rm_block_media_ctrl_t *const p_api_ctrl, rm_block_media_status_t *const p_status)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_InfoGet (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_info_t *const p_info)
fsp_err_t	RM_BLOCK_MEDIA_SDMMC_Close (rm_block_media_ctrl_t *const p_ctrl)

#### Detailed Description

Middleware to implement the block media interface on SD cards. This module implements the [Block Media Interface](#).

## Overview

### Features

The SD/MMC implementation of the block media interface has the following key features:

- Reading, writing, and erasing data from an SD card
- Callback called when card insertion or removal is detected
- Provides media information such as sector size and total number of sectors.

## Configuration

### Build Time Configurations for rm\_block\_media\_sdmmc

The following build time configurations are defined in driver/rm\_block\_media\_sdmmc\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Storage > Block Media Implementation on rm\_block\_media\_sdmmc

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Block Media Implementation on rm\_block\_media\_sdmmc. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_block_media0	Module name.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called when a card is inserted or removed.

### Clock Configuration

This module has no required clock configurations.

### Pin Configuration

This module does not use I/O pins.

## Examples

### Basic Example

This is a basic example of minimal use of the SD/MMC block media implementation in an application.

```
#define RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE (512)
uint8_t g_dest[RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
```

```
uint8_t g_src[RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint32_t g_transfer_complete = 0;
void rm_block_media_sdmmc_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_SDMMC_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the RM_BLOCK_MEDIA_SDMMC driver. */
    fsp_err_t err = RM_BLOCK_MEDIA_SDMMC_Open(&g_rm_block_media0_ctrl,
&g_rm_block_media0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* A device shall be ready to accept the first command within 1ms from detecting VDD
min. Reference section 6.4.1.1
    * "Power Up Time of Card" in the SD Physical Layer Simplified Specification Version
6.00. */
    R_BSP_SoftwareDelay(1U, BSP_DELAY_UNITS_MILLISECONDS);
    /* Initialize the SD card. This should not be done until the card is plugged in for
SD devices. */
    err = RM_BLOCK_MEDIA_SDMMC_MediaInit(&g_rm_block_media0_ctrl);
    assert(FSP_SUCCESS == err);
    /* Write a block of data to sector 3 of an SD card. */
    err = RM_BLOCK_MEDIA_SDMMC_Write(&g_rm_block_media0_ctrl, g_src, 3, 1);
    assert(FSP_SUCCESS == err);
    /* Read a block of data from sector 3 of an SD card. */
    err = RM_BLOCK_MEDIA_SDMMC_Read(&g_rm_block_media0_ctrl, g_dest, 3, 1);
    assert(FSP_SUCCESS == err);
}
```

## Function Documentation

---

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Open()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Open ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg )
```

Opens the module.

Implements `rm_block_media_api_t::open()`.

**Return values**

FSP_SUCCESS	Module is available and is now open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Module has already been opened with this instance of the control structure.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `sdmmc_api_t::open`

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_MediaInit()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_MediaInit ( rm_block_media_ctrl_t *const p_ctrl)
```

Initializes the SD or eMMC device. This procedure requires several sequential commands. This function blocks until all identification and configuration commands are complete.

Implements `rm_block_media_api_t::mediaInit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `sdmmc_api_t::mediaInit`

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Read()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Read ( rm_block_media_ctrl_t *const p_ctrl, uint8_t *const
p_dest_address, uint32_t const block_address, uint32_t const num_blocks )
```

Reads data from an SD or eMMC device. Up to 0x10000 sectors can be read at a time. Implements [rm\\_block\\_media\\_api\\_t::read\(\)](#).

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [sdmmc\\_api\\_t::read](#)

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Write()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Write ( rm_block_media_ctrl_t *const p_ctrl, uint8_t const
*const p_src_address, uint32_t const block_address, uint32_t const num_blocks )
```

Writes data to an SD or eMMC device. Up to 0x10000 sectors can be written at a time. Implements [rm\\_block\\_media\\_api\\_t::write\(\)](#).

**Return values**

FSP_SUCCESS	Write finished successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [sdmmc\\_api\\_t::write](#)

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Erase()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Erase ( rm_block_media_ctrl_t *const p_ctrl, uint32_t const
block_address, uint32_t const num_blocks )
```

Erases sectors of an SD card or eMMC device. Implements [rm\\_block\\_media\\_api\\_t::erase\(\)](#).

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [sdmmc\\_api\\_t::erase](#)
- [sdmmc\\_api\\_t::statusGet](#)

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_CallbackSet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_CallbackSet ( rm_block_media_ctrl_t *const p_ctrl,
void(*) (rm_block_media_callback_args_t *) p_callback, void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements [rm\\_block\\_media\\_api\\_t::callbackSet](#).

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	p_callback is non-secure and p_callback_memory is either secure or NULL.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_StatusGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_StatusGet ( rm_block_media_ctrl_t *const p_api_ctrl,
rm_block_media_status_t *const p_status )
```

Provides driver status. Implements `rm_block_media_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_InfoGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_InfoGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info )
```

Retrieves module information. Implements `rm_block_media_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

◆ **RM\_BLOCK\_MEDIA\_SDMMC\_Close()**

```
fsp_err_t RM_BLOCK_MEDIA_SDMMC_Close ( rm_block_media_ctrl_t *const p_ctrl)
```

Closes an open SD/MMC device. Implements `rm_block_media_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

**4.2.69 SPI Block Media Implementation (rm\_block\_media\_spi)**

## Modules

## Functions

fsp_err_t	RM_BLOCK_MEDIA_SPI_Open (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_cfg_t const *const p_cfg)
fsp_err_t	RM_BLOCK_MEDIA_SPI_InfoGet (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_info_t *const p_info)
fsp_err_t	RM_BLOCK_MEDIA_SPI_MediaInit (rm_block_media_ctrl_t *const p_ctrl)
fsp_err_t	RM_BLOCK_MEDIA_SPI_Read (rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const start_block, uint32_t const num_blocks)
fsp_err_t	RM_BLOCK_MEDIA_SPI_StatusGet (rm_block_media_ctrl_t *const p_ctrl, rm_block_media_status_t *const p_status)
fsp_err_t	RM_BLOCK_MEDIA_SPI_Write (rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const p_src, uint32_t const start_block, uint32_t const num_blocks)
fsp_err_t	RM_BLOCK_MEDIA_SPI_CallbackSet (rm_block_media_ctrl_t *const p_ctrl, void(*p_callback)(rm_block_media_callback_args_t *), void const *const p_context, rm_block_media_callback_args_t *const p_callback_memory)
fsp_err_t	RM_BLOCK_MEDIA_SPI_Close (rm_block_media_ctrl_t *const p_ctrl)
fsp_err_t	RM_BLOCK_MEDIA_SPI_Erase (rm_block_media_ctrl_t *const p_ctrl, uint32_t const start_block, uint32_t const num_blocks)

## Detailed Description

Middleware to implement the block media interface on SPI flash memory. This module implements the [Block Media Interface](#).

## Overview

### Features

The SPI implementation of the block media interface has the following key features:

- Reading, writing, and erasing data from SPI flash memory
- Provides media information such as sector size and total number of sectors.

*Note*

*By default, Block Media SPI Read, Write, and Erase are blocking operations. Non-blocking operation may be achieved by yielding control within the optional callback function.*

## Configuration

### Build Time Configurations for rm\_block\_media\_spi

The following build time configurations are defined in driver/rm\_block\_media\_spi\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected, code for parameter checking is included in the build

### Configurations for Middleware > Storage > Block Media Implementation on rm\_block\_media\_spi

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Block Media Implementation on rm\_block\_media\_spi.

Configuration	Options	Default	Description
Module Instance Name	Name must be a valid C symbol	g_rm_block_media0	Module name
Block size (bytes)	Manual Entry	4096	Specify the size of a block in bytes.
Block count	Minimum block count is 1, maximum is defined by hardware and software design.	8192	Number of blocks available for use by this driver instance.
Base Address	Manual Entry	0	Base address offset (bytes) for instance memory region.
Callback Function	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback is provided, it will be called after the completion of Read, Write, and Erase operations, or anytime these functions are waiting on hardware.
[DEPRECATED] Callback Context	Name must be a valid C symbol	NULL	A user specified context that will be provided back to the user when a callback occurs.

### Clock Configuration

This module has no required clock configurations.

### Pin Configuration

This module does not use I/O pins.

## Limitations

Developers should be aware of the following limitations when using RM\_BLOCK\_MEDIA\_SPI:

- Getting and setting Block Protection or Advanced Sector Protection modes is not supported.
- Addressing QSPI memory address ranges greater than 64 MB (one bank) is not supported.

## Examples

### Basic Example

This is a basic example of minimal use of the SPI block media implementation in an application.

```
#define RM_BLOCK_MEDIA_SPI_BLOCK_SIZE (256U)
uint8_t g_dest[RM_BLOCK_MEDIA_SPI_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t g_src[RM_BLOCK_MEDIA_SPI_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
void rm_block_media_spi_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_SPI_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the RM_BLOCK_MEDIA_SPI driver. */
    fsp_err_t err = RM_BLOCK_MEDIA_SPI_Open(&g_rm_block_media0_ctrl,
&g_rm_block_media0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize the SPI flash memory. */
    err = RM_BLOCK_MEDIA_SPI_MediaInit(&g_rm_block_media0_ctrl);
    assert(FSP_SUCCESS == err);

    /* Write a block of data to block 3 of the SPI flash memory. */
    err = RM_BLOCK_MEDIA_SPI_Write(&g_rm_block_media0_ctrl, g_src, 3, 1);
    assert(FSP_SUCCESS == err);

    /* Read a block of data from block 3 of the SPI flash memory. */
    err = RM_BLOCK_MEDIA_SPI_Read(&g_rm_block_media0_ctrl, g_dest, 3, 1);
    assert(FSP_SUCCESS == err);
}
```

```
}
```

## Non-Blocking Example

This is a basic example of using the optional SPI callback to impliment non-blocking operation.

```
#define RM_BLOCK_MEDIA_EXAMPLE_DEVICE_BLOCK_COUNT 0x1000
void rm_block_media_spi_non_blocking_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_SPI_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }

    /* Open the RM_BLOCK_MEDIA_SPI driver. This enables the card detection interrupt. */
    fsp_err_t err = RM_BLOCK_MEDIA_SPI_Open(&g_rm_block_media0_ctrl,
    &g_rm_block_media0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize the Block Media SPI driver. */
    err = RM_BLOCK_MEDIA_SPI_MediaInit(&g_rm_block_media0_ctrl);
    assert(FSP_SUCCESS == err);

    /* Erase a large quantity of data from SPI Flash Memory */
    err = RM_BLOCK_MEDIA_SPI_Erase(&g_rm_block_media0_ctrl, 0,
    RM_BLOCK_MEDIA_EXAMPLE_DEVICE_BLOCK_COUNT);
    assert(FSP_SUCCESS == err);
}

/* The optional callback is invoked for Read, Write, and Erase operations, whenever
the operation completes or has
* been blocked by the lower level SPI driver busy indication.
*/
void rm_block_media_spi_example_callback (rm_block_media_callback_args_t * p_args)
{
    if (RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE == p_args->event)
    {
```

```
/* TODO: Process operation complete. */
}
else if (RM_BLOCK_MEDIA_EVENT_POLL_STATUS == p_args->event)
{
    rm_block_media_status_t status;
    rm_block_media_ctrl_t * p_ctrl = (rm_block_media_ctrl_t *) p_args->p_context;
    fsp_err_t err = RM_BLOCK_MEDIA_SPI_StatusGet(p_ctrl, &status);
    assert(FSP_SUCCESS == err);
    if (true == status.busy)
    {
        /* Run waiting tasks */
        vTaskSuspend(xTaskGetCurrentTaskHandle());
    }
}
else
{
    assert(RM_BLOCK_MEDIA_EVENT_ERROR == p_args->event);
    /* TODO: Process Read, Write, or Erase error. */
}
}
```

## Function Documentation

---

◆ **RM\_BLOCK\_MEDIA\_SPI\_Open()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_Open ( rm_block_media_ctrl_t *const p_ctrl, rm_block_media_cfg_t
const *const p_cfg )
```

Parameter checking and Acquires mutex, then handles driver initialization at the HAL SPI layer and marking the open flag in control block.

Implements `rm_block_media_api_t::open`.

**Return values**

FSP_SUCCESS	Block media for SPI framework is successfully opened.
FSP_ERR_ASSERTION	One of the input parameters or their data references may be null.
FSP_ERR_ALREADY_OPEN	The channel specified has already been opened. See HAL driver for other possible causes.

**Returns**

See [Common Error Codes](#) or HAL driver for other possible return codes or causes. This function calls

- `spi_flash_api_t::open`

◆ **RM\_BLOCK\_MEDIA\_SPI\_InfoGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_InfoGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info )
```

Retrieves module information.

Implements `rm_block_media_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

◆ **RM\_BLOCK\_MEDIA\_SPI\_MediaInit()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_MediaInit ( rm_block_media_ctrl_t *const p_ctrl)
```

Initializes the Block Media SPI Flash device.

Implements `rm_block_media_api_t::mediaInit`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_BLOCK\_MEDIA\_SPI\_Read()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_Read ( rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest,
uint32_t const start_block, uint32_t const num_blocks )
```

Reads a number of blocks from spi flash memory. By default, this is a function is blocking. Non-blocking operation may be achieved by yielding control within the optional callback function.

Implements `rm_block_media_api_t::read`.

**Return values**

FSP_SUCCESS	SPI data read successfully
FSP_ERR_ASSERTION	p_ctrl or p_dest is NULL, or num_blocks is zero
FSP_ERR_NOT_OPEN	Block Media SPI module is not yet open
FSP_ERR_INVALID_ADDRESS	Invalid address range for read operation
FSP_ERR_NOT_INITIALIZED	Block Media SPI module is not yet initialized

◆ **RM\_BLOCK\_MEDIA\_SPI\_StatusGet()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_StatusGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_status_t *const p_status )
```

Provides driver status.

Implements `rm_block_media_api_t::statusGet`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Module is not open.

**Returns**

See [Common Error Codes](#) or HAL driver for other possible return codes or causes. This function calls

- `spi_flash_api_t::statusGet`

◆ **RM\_BLOCK\_MEDIA\_SPI\_Write()**

```
fsp_err_t RM_BLOCK_MEDIA_SPI_Write ( rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const
p_src, uint32_t const start_block, uint32_t const num_blocks )
```

Writes provided data to a number of blocks of spi flash memory. By default, this is a function is blocking. Non-blocking operation may be achieved by yielding control within the optional callback function.

Implements `rm_block_media_api_t::write`.

**Return values**

FSP_SUCCESS	Flash write finished successfully.
FSP_ERR_ASSERTION	p_ctrl or p_src is NULL. Or num_blocks is zero.
FSP_ERR_NOT_OPEN	Block media SPI Framework module is not yet initialized.
FSP_ERR_INVALID_ADDRESS	Invalid address range
FSP_ERR_NOT_INITIALIZED	Block Media SPI module is not yet initialized

**Returns**

See [Common Error Codes](#) or HAL driver for other possible return codes or causes. This function calls

- `spi_flash_api_t::write`

### ◆ RM\_BLOCK\_MEDIA\_SPI\_CallbackSet()

```
fsp_err_t RM_BLOCK_MEDIA_SPI_CallbackSet ( rm_block_media_ctrl_t *const p_ctrl,
void(*) (rm_block_media_callback_args_t *) p_callback, void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. API not supported.

Implements `rm_block_media_api_t::callbackSet`.

#### Return values

FSP_ERR_UNSUPPORTED	API not supported by RM_BLOCK_MEDIA_SPI.
---------------------	--

### ◆ RM\_BLOCK\_MEDIA\_SPI\_Close()

```
fsp_err_t RM_BLOCK_MEDIA_SPI_Close ( rm_block_media_ctrl_t *const p_ctrl)
```

Closes the Block Media SPI device. Implements `rm_block_media_api_t::close`.

#### Return values

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	One of the following parameters may be null: <code>p_ctrl</code> .
FSP_ERR_NOT_OPEN	Block media SPI Framework module is not yet initialized.

#### Returns

See [Common Error Codes](#) or HAL driver for other possible return codes or causes. This function calls

- `spi_flash_api_t::close`

### ◆ RM\_BLOCK\_MEDIA\_SPI\_Erase()

```
fsp_err_t RM_BLOCK_MEDIA_SPI_Erase ( rm_block_media_ctrl_t *const p_ctrl, uint32_t const
start_block, uint32_t const num_blocks )
```

This function erases blocks of the SPI device. By default, this is a function is blocking. Non-blocking operation may be achieved by yielding control within the optional callback function.

Implements `rm_block_media_api_t::erase`.

#### Return values

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.
FSP_ERR_INVALID_ADDRESS	Invalid address range

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `spi_flash_api_t::erase`
- `spi_flash_api_t::statusGet`

## 4.2.70 USB HMSC Block Media Implementation (rm\_block\_media\_usb)

### Modules

#### Functions

```
fsp_err_t RM_BLOCK_MEDIA_USB_Open (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_MediaInit (rm_block_media_ctrl_t *const
p_ctrl)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Read (rm_block_media_ctrl_t *const p_ctrl,
uint8_t *const p_dest_address, uint32_t const block_address,
uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Write (rm_block_media_ctrl_t *const p_ctrl,
uint8_t const *const p_src_address, uint32_t const block_address,
uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Erase (rm_block_media_ctrl_t *const p_ctrl,
uint32_t const block_address, uint32_t const num_blocks)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_CallbackSet (rm_block_media_ctrl_t *const
```

```
p_ctrl, void(*p_callback)(rm_block_media_callback_args_t*), void
const *const p_context, rm_block_media_callback_args_t *const
p_callback_memory)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_StatusGet (rm_block_media_ctrl_t *const
p_api_ctrl, rm_block_media_status_t *const p_status)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_InfoGet (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info)
```

```
fsp_err_t RM_BLOCK_MEDIA_USB_Close (rm_block_media_ctrl_t *const p_ctrl)
```

## Detailed Description

Middleware to implement the block media interface on USB mass storage devices. This module implements the [Block Media Interface](#).

## Overview

### Features

The USB implementation of the block media interface has the following key features:

- Reading, writing, and erasing data from a USB mass storage device
- Callback called when device insertion or removal is detected
- Provides media information such as sector size and total number of sectors.

## Configuration

### Build Time Configurations for rm\_block\_media\_usb

The following build time configurations are defined in driver/rm\_block\_media\_usb\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Storage > Block Media Implementation on rm\_block\_media\_usb

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Block Media Implementation on rm\_block\_media\_usb.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_block_media0	Module name.
Callback	Name must be a valid C symbol	NULL	A user callback function can be

provided. If this callback function is provided, it will be called when a device is attached or removed.

A user context can be provided. If this context is provided, it will be passed to callback function when a device is attached or removed.

Pointer to user context    Name must be a valid C symbol    NULL

#### Note

*RM\_BLOCK\_MEDIA\_USB\_MediaInit function must be called after receiving the insert event notification.*

## Clock Configuration

This module has no required clock configurations.

## Pin Configuration

This module does not use I/O pins.

## Examples

### Basic Example

This is a basic example of minimal use of the USB mass storage block media implementation in an application.

```
#define RM_BLOCK_MEDIA_USB_BLOCK_SIZE (512)
volatile bool g_usb_inserted = false;
uint8_t      g_dest[RM_BLOCK_MEDIA_USB_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
uint8_t      g_src[RM_BLOCK_MEDIA_USB_BLOCK_SIZE] BSP_ALIGN_VARIABLE(4);
void rm_block_media_usb_basic_example (void)
{
    /* Initialize g_src to known data */
    for (uint32_t i = 0; i < RM_BLOCK_MEDIA_USB_BLOCK_SIZE; i++)
    {
        g_src[i] = (uint8_t) ('A' + (i % 26));
    }
    /* Open the RM_BLOCK_MEDIA_USB driver. */
    fsp_err_t err = RM_BLOCK_MEDIA_USB_Open(&g_rm_block_media0_ctrl,
&g_rm_block_media0_cfg);
```

```
/* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
while (!g_usb_inserted)
    {
/* Wait for a card insertion interrupt. */
    }

/* Initialize the mass storage device. This should not be done until the device is
plugged in and initialized. */
    err = RM_BLOCK_MEDIA_USB_MediaInit(&g_rm_block_media0_ctrl);
    assert(FSP_SUCCESS == err);

/* Write a block of data to sector 3 of an USB mass storage device. */
    err = RM_BLOCK_MEDIA_USB_Write(&g_rm_block_media0_ctrl, g_src, 3, 1);
    assert(FSP_SUCCESS == err);

/* Read a block of data from sector 3 of an USB mass storage device. */
    err = RM_BLOCK_MEDIA_USB_Read(&g_rm_block_media0_ctrl, g_dest, 3, 1);
    assert(FSP_SUCCESS == err);
}
```

## Device Insertion

This is an example of using a callback to determine when a mass storage device is plugged in and enumerated.

```
/* The callback is called when a media insertion event occurs. */
void rm_block_media_usb_media_insertion_example_callback
(rm_block_media_callback_args_t * p_args)
{
    if (RM_BLOCK_MEDIA_EVENT_MEDIA_INSERTED == p_args->event)
    {
        g_usb_inserted = true;
    }

    if (RM_BLOCK_MEDIA_EVENT_MEDIA_REMOVED == p_args->event)
    {
        g_usb_inserted = false;
    }
}
```

}

## Function Documentation

### ◆ RM\_BLOCK\_MEDIA\_USB\_Open()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Open ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_cfg_t const *const p_cfg )
```

Opens the module.

Implements `rm_block_media_api_t::open()`.

#### Return values

FSP_SUCCESS	Module is available and is now open.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_ALREADY_OPEN	Module has already been opened with this instance of the control structure.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_MediaInit()

```
fsp_err_t RM_BLOCK_MEDIA_USB_MediaInit ( rm_block_media_ctrl_t *const p_ctrl)
```

Initializes the USB device.

Implements `rm_block_media_api_t::mediaInit()`.

#### Return values

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_BLOCK\_MEDIA\_USB\_Read()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_Read ( rm_block_media_ctrl_t *const p_ctrl, uint8_t *const
p_dest_address, uint32_t const block_address, uint32_t const num_blocks )
```

Reads data from an USB device. Implements `rm_block_media_api_t::read()`.

This function blocks until the data is read into the destination buffer.

**Return values**

FSP_SUCCESS	Data read successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.
FSP_ERR_USB_FAILED	The message could not received completed successfully.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

◆ **RM\_BLOCK\_MEDIA\_USB\_Write()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_Write ( rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const
p_src_address, uint32_t const block_address, uint32_t const num_blocks )
```

Writes data to an USB device. Implements `rm_block_media_api_t::write()`.

This function blocks until the write operation completes.

**Return values**

FSP_SUCCESS	Write finished successfully.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.
FSP_ERR_USB_FAILED	The message could not received completed successfully.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_Erase()

```
fsp_err_t RM_BLOCK_MEDIA_USB_Erase ( rm_block_media_ctrl_t *const p_ctrl, uint32_t const
block_address, uint32_t const num_blocks )
```

Erases sectors of an USB device. Implements `rm_block_media_api_t::erase()`.

This function blocks until erase is complete.

#### Return values

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes.

### ◆ RM\_BLOCK\_MEDIA\_USB\_CallbackSet()

```
fsp_err_t RM_BLOCK_MEDIA_USB_CallbackSet ( rm_block_media_ctrl_t *const p_ctrl,
void(*) (rm_block_media_callback_args_t *) p_callback, void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure. Implements `rm_block_media_api_t::callbackSet`.

#### Note

*This function is currently unsupported for Block Media over USB.*

#### Return values

FSP_ERR_UNSUPPORTED	CallbackSet is not currently supported for Block Media over USB.
---------------------	--

◆ **RM\_BLOCK\_MEDIA\_USB\_StatusGet()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_StatusGet ( rm_block_media_ctrl_t *const p_api_ctrl,
rm_block_media_status_t *const p_status )
```

Provides driver status. Implements `rm_block_media_api_t::statusGet()`.

**Return values**

FSP_SUCCESS	Status stored in p_status.
FSP_ERR_ASSERTION	NULL pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

◆ **RM\_BLOCK\_MEDIA\_USB\_InfoGet()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_InfoGet ( rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info )
```

Retrieves module information. Implements `rm_block_media_api_t::infoGet()`.

**Return values**

FSP_SUCCESS	Erase operation requested.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_NOT_INITIALIZED	Module has not been initialized.

◆ **RM\_BLOCK\_MEDIA\_USB\_Close()**

```
fsp_err_t RM_BLOCK_MEDIA_USB_Close ( rm_block_media_ctrl_t *const p_ctrl)
```

Closes an open USB device. Implements `rm_block_media_api_t::close()`.

**Return values**

FSP_SUCCESS	Successful close.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

## 4.2.71 User Block Media Implementation (rm\_block\_media\_user)

### Modules

Middleware that implements a block media interface on the media of your choice. This module implements the [Block Media Interface](#).

## Overview

### Features

This module is for using Block media with user-selected media.

## Configuration

Block Media User has no output config settings.

The user is required to create the config settings etc. in the application.

The figure below is an example of the config definition when the user media in USB PMSC is RAM.

```
const rm_block_media_api_t g_rm_block_media_on_user_media =
{
    .open      = RM_BLOCK_MEDIA_RAM_Open,
    .mediaInit = RM_BLOCK_MEDIA_RAM_MediaInit,
    .read      = RM_BLOCK_MEDIA_RAM_Read,
    .write     = RM_BLOCK_MEDIA_RAM_Write,
    .erase     = RM_BLOCK_MEDIA_RAM_Erase,
    .infoGet   = RM_BLOCK_MEDIA_RAM_InfoGet,
    .statusGet = RM_BLOCK_MEDIA_RAM_StatusGet,
    .close     = RM_BLOCK_MEDIA_RAM_Close,
};

extern void r_usb_pmsc_block_media_event_callback(rm_block_media_callback_args_t *
p_args);

const rm_block_media_cfg_t g_rm_block_media0_cfg =
{.p_extend = NULL, .p_callback = r_usb_pmsc_block_media_event_callback, .p_context =
NULL, };

rm_block_media_instance_t g_rm_block_media0 =
{.p_api = &g_rm_block_media_on_user_media, .p_ctrl = NULL, .p_cfg =
&g_rm_block_media0_cfg, };
```

**Note**

If you use `block_media_user`, you need to create a function that matches the media you are using. In the above example, this is the function with `RM_BLOCK_MEDIA_`. Register the created function in `rm_block_media_api_t`. The registered `rm_block_media_api_t` is registered in `p_api`, which is a member of `rm_block_media_instance_t`.

**Clock Configuration**

This module has no required clock configurations.

**Pin Configuration**

This module does not use I/O pins.

**Examples****Basic Example**

Please refer to [USB Peripheral Mass Storage Class \(r\\_usb\\_pmesc\)](#) for the PMSC application given as an example.

**4.2.72 I2C Communicatons Middleware (rm\_comms\_i2c)****Modules****Functions**

`fsp_err_t` [RM\\_COMMS\\_I2C\\_Open](#) (`rm_comms_ctrl_t *const p_api_ctrl, rm_comms_cfg_t const *const p_cfg`)

Opens and configures the Communications Middle module. Implements `rm_comms_api_t::open`. [More...](#)

`fsp_err_t` [RM\\_COMMS\\_I2C\\_Close](#) (`rm_comms_ctrl_t *const p_api_ctrl`)

Disables specified Communications Middle module. Implements `rm_comms_api_t::close`. [More...](#)

`fsp_err_t` [RM\\_COMMS\\_I2C\\_Read](#) (`rm_comms_ctrl_t *const p_api_ctrl, uint8_t *const p_dest, uint32_t const bytes`)

Performs a read from the I2C device. Implements `rm_comms_api_t::read`. [More...](#)

`fsp_err_t` [RM\\_COMMS\\_I2C\\_Write](#) (`rm_comms_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t const bytes`)

Performs a write from the I2C device. Implements [rm\\_comms\\_api\\_t::write](#). [More...](#)

`fsp_err_t` [RM\\_COMMS\\_I2C\\_WriteRead](#) (`rm_comms_ctrl_t *const p_api_ctrl, rm_comms_write_read_params_t const write_read_params`)

Performs a write to, then a read from the I2C device. Implements [rm\\_comms\\_api\\_t::writeRead](#). [More...](#)

`void` [rm\\_comms\\_i2c\\_callback](#) (`i2c_master_callback_args_t *p_args`)

Common callback function called in the I2C driver callback function.

## Detailed Description

Middleware to implement the I2C communications interface. This module implements the [Communications Middleware Interface](#).

## Overview

### Features

The implementation of the I2C communications interface has the following key features:

- Reading data from, writing data to I2C bus
- Writes to I2C bus, then reads with restart
- A single I2C bus used by multiple I2C devices

## Configuration

### Build Time Configurations for `rm_comms_i2c`

The following build time configurations are defined in `fsp_cfg/rm_comms_i2c_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Communications > I2C Shared Bus on `rm_comms_i2c`

This module can be added to the Stacks tab via New Stack > Middleware > Communications > I2C Shared Bus on `rm_comms_i2c`.

Configuration	Options	Default	Description
Name	Manual Entry	<code>g_comms_i2c_bus0</code>	Module name.
Bus Timeout	Value must be a non-	<code>0xFFFFFFFF</code>	Set timeout for locking

	negative integer		bus in using RTOS.
Semaphore for Blocking	<ul style="list-style-type: none"> <li>• Unuse</li> <li>• Use</li> </ul>	Unuse	Set Semaphore for blocking in using RTOS.
Recursive Mutex for Bus	<ul style="list-style-type: none"> <li>• Unuse</li> <li>• Use</li> </ul>	Unuse	Set Mutex for locking bus in using RTOS.

## Configurations for Middleware > Communications > I2C Communication Device on rm\_comms\_i2c

This module can be added to the Stacks tab via New Stack > Middleware > Communications > I2C Communication Device on rm\_comms\_i2c.

Configuration	Options	Default	Description
Name	Manual Entry	g_comms_i2c_device0	Module name.
Semaphore Timeout	Value must be a non-negative integer	0xFFFFFFFF	Set timeout for blocking in using RTOS.
Slave Address	Value must be non-negative	0x00	Specify the slave address.
Address Mode	<ul style="list-style-type: none"> <li>• 7-Bit</li> <li>• 10-Bit</li> </ul>	7-Bit	Select the I2C address mode.
Callback	Name must be a valid C symbol	comms_i2c_callback	A user callback function can be provided.

## Pin Configuration

This module uses SDA and SCL pins of I2C Master and SCI I2C.

## Usage Notes

### Bus Initialization

The I2C communications interface expects a bus instance to be opened before opening any specific I2C comms device. The communications interface will handle switching between devices on the bus but will not open or close the bus instance. The user should open the bus with the appropriate [I2C Master Interface](#) open call.

## Examples

### Basic Example

This is a basic example of minimal use of I2C communications implementation in an application.

```
void rm_comms_i2c_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Open the I2C bus if it is not already open. */
}
```

```

    rm_comms_i2c_bus_extended_cfg_t * p_extend          =
(rm_comms_i2c_bus_extended_cfg_t *) g_comms_i2c_cfg.p_extend;
    i2c_master_instance_t          * p_driver_instance = (i2c_master_instance_t *)
p_extend->p_driver_instance;

    p_driver_instance->p_api->open(p_driver_instance->p_ctrl,
p_driver_instance->p_cfg);

    err = RM_COMMS_I2C_Open(&g_comms_i2c_ctrl, &g_comms_i2c_cfg);
/* Handle any errors. This function should be defined by the user. */
    handle_error(err);
while (true)
    {
        g_flag = 0;
/* Send data to an I2C device. */
RM_COMMS_I2C_Write(&g_comms_i2c_ctrl, &write_data, 1);
while (0 == g_flag)
    {
/* Wait callback */
    }
        g_flag = 0;
/* Receive data from an I2C device. */
RM_COMMS_I2C_Read(&g_comms_i2c_ctrl, &read_data, 1);
while (0 == g_flag)
    {
/* Wait callback */
    }
    }
}

```

## Data Structures

```
struct  rm_comms_i2c_instance_ctrl_t
```

## Data Structure Documentation

### ◆ rm\_comms\_i2c\_instance\_ctrl\_t

```
struct rm_comms_i2c_instance_ctrl_t
```

Communications middleware control structure.

Data Fields	
<code>rm_comms_cfg_t const *</code>	<code>p_cfg</code>
	middleware configuration.
<code>rm_comms_i2c_bus_extended_cfg_t *</code>	<code>p_bus</code>
	Bus using this device;.
<code>void *</code>	<code>p_lower_level_cfg</code>
	Used to reconfigure I2C driver.
<code>uint32_t</code>	<code>open</code>
	Open flag.
<code>uint32_t</code>	<code>transfer_data_bytes</code>
	Size of transfer data.
<code>uint8_t *</code>	<code>p_transfer_data</code>
	Pointer to transfer data buffer.
<code>void const *</code>	<code>p_context</code>
	Pointer to the user-provided context.

## Function Documentation

◆ **RM\_COMMS\_I2C\_Open()**

```
fsp_err_t RM_COMMS_I2C_Open ( rm_comms_ctrl_t *const p_api_ctrl, rm_comms_cfg_t const
*const p_cfg )
```

Opens and configures the Communications Middle module. Implements `rm_comms_api_t::open`.

Example:

```
err = RM_COMMS_I2C_Open(&g_comms_i2c_ctrl, &g_comms_i2c_cfg);
```

**Return values**

FSP_SUCCESS	Communications Middle module successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_COMMS_BUS_NOT_OPEN	I2C driver is not open.

◆ **RM\_COMMS\_I2C\_Close()**

```
fsp_err_t RM_COMMS_I2C_Close ( rm_comms_ctrl_t *const p_api_ctrl)
```

Disables specified Communications Middle module. Implements `rm_comms_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_COMMS\_I2C\_Read()**

```
fsp_err_t RM_COMMS_I2C_Read ( rm_comms_ctrl_t *const p_api_ctrl, uint8_t *const p_dest,
uint32_t const bytes )
```

Performs a read from the I2C device. Implements `rm_comms_api_t::read`.

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_COMMS\_I2C\_Write()

```
fsp_err_t RM_COMMS_I2C_Write ( rm_comms_ctrl_t *const p_api_ctrl, uint8_t *const p_src, uint32_t
const bytes )
```

Performs a write from the I2C device. Implements `rm_comms_api_t::write`.

#### Return values

FSP_SUCCESS	Successfully writing data .
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_COMMS\_I2C\_WriteRead()

```
fsp_err_t RM_COMMS_I2C_WriteRead ( rm_comms_ctrl_t *const p_api_ctrl,
rm_comms_write_read_params_t const write_read_params )
```

Performs a write to, then a read from the I2C device. Implements `rm_comms_api_t::writeRead`.

#### Return values

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

## 4.2.73 SEGGER emWin Port (rm\_emwin\_port)

### Modules

SEGGER emWin port for RA MCUs.

## Overview

The SEGGER emWin RA Port module provides the configuration and hardware acceleration support necessary for use of emWin on RA products. The port provides full integration with the graphics peripherals (GLCDC, DRW and JPEG) as well as FreeRTOS.

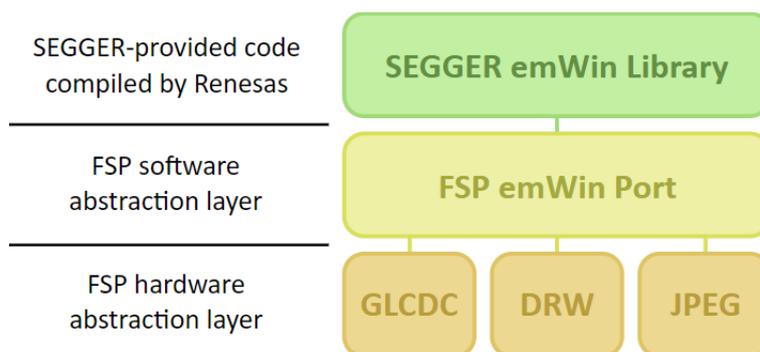


Figure 193: SEGGER emWin FSP Port Block Diagram

**Note**

*This port layer primarily enables hardware acceleration and background handling of many display operations and does not contain code intended to be directly called by the user. Please consult the SEGGER emWin User Guide (UM03001) for details on how to use emWin in your project.*

**Hardware Acceleration**

The following functions are currently performed with hardware acceleration:

- DRW Engine (r\_drw)
  - Drawing bitmaps (ARGB8888 and RGB565)
  - 4bpp font rendering
  - Rectangle fill
  - Line and shape drawing
  - Anti-aliased operations
    - Circle stroke and fill
    - Polygon stroke and fill
    - Lines and arcs
- JPEG Codec (r\_jpeg)
  - JPEG decoding
- Graphics LCD Controller (r\_glcdc)
  - Brightness, contrast and gamma correction
  - Pixel format conversion (framebuffer to LCD)

**Configuration****Build Time Configurations for rm\_emwin\_port**

The following build time configurations are defined in fsp\_cfg/rm\_emwin\_port\_cfg.h:

Configuration	Options	Default	Description
Memory Allocation > GUI Heap Size	Value must be a non-negative integer	32768	Set the size of the heap to be allocated for use exclusively by emWin.
Memory Allocation > Section for GUI Heap	Manual Entry	.noinit	Specify the section in which to allocate the GUI heap. When Arm Compiler 6 is used to

place this memory in on-chip SRAM, the section name must be .bss or start with .bss. to avoid consuming unnecessary ROM space.

Set the maximum number of available display layers in emWin.

This setting is not related to GLCDC Layer 1 or 2.

Set the size of the conversion buffer for anti-aliased font glyphs. This should be set to the size (in bytes) of the largest AA character to be rendered.

Enable or disable multithreading support.

If multithreading support is enabled this configuration specifies the number of different tasks that can call emWin functions.

Enable or disable touch panel support.

Enable or disable support for mouse input.

Enable or disable support for memory devices, which allow the user to allocate their own memory in the GUI heap.

Enable or disable support for displaying rotated text.

Enable or disable the emWin Window Manager (WM).

Enable or disable

Memory Allocation > Maximum Layers	Value must be a non-negative integer	16
Memory Allocation > AA Font Conversion Buffer Size	Value must be a non-negative integer	400
Configuration > Multi-thread Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
Configuration > Number of emWin-supported threads	Manual Entry	5
Configuration > Touch Panel Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
Configuration > Mouse Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled
Configuration > Memory Devices	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
Configuration > Text Rotation	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
Configuration > Window Manager	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled
Configuration >	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>	Disabled

Bidirectional Text	<ul style="list-style-type: none"> <li>• Disabled</li> </ul>		support for bidirectional text (such as Arabic or Hebrew).
Configuration > Debug Logging Level	<ul style="list-style-type: none"> <li>• None (0)</li> <li>• Parameter checking only (1)</li> <li>• All checks enabled (2)</li> <li>• Log errors (3)</li> <li>• Log warnings (4)</li> <li>• Log all messages (5)</li> </ul>	All checks enabled (2)	Set the debug logging level.
LCD Settings > Wait for Vertical Sync	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	<p>When enabled emWin will wait for a vertical sync event each time the display is updated. If an RTOS is used the thread will yield; otherwise each frame will block until Vsync.</p> <p>WARNING: Disabling vertical sync will result in tearing. It is recommended to always leave this setting Enabled if an RTOS is used.</p>
JPEG Decoding > General > Input Alignment	<ul style="list-style-type: none"> <li>• 8-byte aligned (faster)</li> <li>• Unaligned (slower)</li> </ul>	Unaligned (slower)	<p>Setting this option to 8-bit alignment can allow the hardware JPEG Codec to directly read JPEG data. This speeds up JPEG decoding operations and reduces RAM overhead, but all JPEG images must reside on an 8-byte boundary.</p> <p>When this option is enabled the input buffer is not allocated.</p>
JPEG Decoding > General > Double-Buffer Output	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable this option to configure JPEG decoding operations to use a double-buffered output pipeline. This allows the JPEG to be rendered to the display

at the same time as decoding at the cost of additional RAM usage.

Enabling this option automatically allocates double the output buffer size.

Set the timeout for JPEG decoding operations (in RTOS ticks) in the event of a decode error.

Set the size of the JPEG decode input buffer (in bytes). This buffer is used to ensure 8-byte alignment of input data. Specifying a size smaller than the size of the JPEG to decode will use additional interrupts to stream data in during the decoding process.

Set the size of the JPEG decode output buffer (in bytes). An output buffer smaller than the size of a decoded image will use additional interrupts to stream the data into a framebuffer.

Unless you are sure of the subsampling used in and the size of the input JPEG images it is recommended to allocate at least 16 framebuffer lines of memory.

Specify the section in which to allocate the JPEG work buffers. When Arm Compiler 6 is used to place this memory in on-chip SRAM, the section name must be `.bss` or start with `.bss.` to avoid

JPEG Decoding >  
General > Error  
Timeout

Value must be a non-negative integer

50

JPEG Decoding >  
Buffers > Input Buffer  
Size

Value must be a non-negative integer

0x1000

JPEG Decoding >  
Buffers > Output Buffer  
Size

Value must be a non-negative integer

0x3C00

JPEG Decoding >  
Buffers > Section for  
Buffers

Manual Entry

.noinit

consuming unnecessary ROM space.

## Hardware Configuration

No clocks or pins are directly required by this module. Please consult the submodules' documentation for their requirements.

---

# Usage Notes

## Getting Started

To get started with emWin in an RA project the following must be performed:

1. Open the RA Configuration editor for your project
2. Add emWin to your project in the Stacks view by clicking **New Stack -> SEGGER -> SEGGER emWin**
3. Ensure the configuration options for emWin are set as necessary for your application
4. Set the properties for the GLCDC module to match the timing and memory requirements of your display panel
5. Set the JPEG decode color depth to the desired value (if applicable)
6. Ensure interrupts on all modules are enabled:
  - GLCDC Vertical Position (Vpos) Interrupt
  - DRW Interrupt (if applicable)
  - JPEG Encode/Decode and Data Transfer Interrupts (if applicable)
7. Click Generate Project Content to save and commit configuration changes
8. (Non-RTOS projects only) Before calling GUI\_Init, call g\_hal\_init to initialize the framebuffer address.

At this point the project is now ready to build with emWin. Please refer to the SEGGER emWin User Guide (UM03001) as well as demo and sample code for details on how to create a GUI application.

## Using Hardware Acceleration

In most cases there is no need to perform additional configuration to ensure the DRW Engine is used. However, there are some guidelines that should be followed depending on the item in question:

- Bitmaps:
  - ARGB8888, RGB888 and RGB565 bitmaps require no additional settings.
- Anti-aliased shapes:
  - Anti-aliased lines, circles, polygons, polygon outlines and arcs are rendered with the DRW Engine.
- Anti-aliased (4bpp) fonts:
  - Set the text mode to GUI\_TM\_TRANS or create the relevant widget with WM\_CF\_HASTRANS set.
  - Ensure the "AA Font Conversion Buffer Size" configuration option is set to a size equal to or greater than the size (in bytes) of the largest glyph.
- 8bpp palletized images:
  - When creating these images ensure transparency is not enabled as the SEGGER method for this is not compatible with the DRW Engine.
- RLE-encoded images:
  - Hardware acceleration is not available for SEGGER's RLE format.

## Multi-thread Support

When the "Multi-thread Support" configuration is enabled, emWin can be called from multiple threads. This comes with advantages and disadvantages:

Advantages:

- High flexibility in development of applications
- Threads can pend and post on emWin events

Disadvantages:

- Slightly higher RAM/ROM use
- Large GUI projects can become difficult to debug

*Note*

*Multi-thread support is independent of RTOS support. RTOS support is managed internally and cannot be manually configured.*

## Limitations

Developers should be aware of the following limitations when using SEGGER emWin with FSP:

- Hardware acceleration is not available when using color modes lower than 16 bits.
- Support for rotated screen modes is in development.
- Hardware acceleration is not available for SEGGER's RLE image format.

## Examples

### Basic Example

This is a basic example demonstrating a very simple emWin application. The screen is cleared to white and "Hello World!" is printed in the center.

*Note*

*emWin manages the GLCDC, DRW and JPEG Codec submodules internally; they do not need to be opened directly.*

```
#include "DIALOG.h"

#define COLOR_WHITE 0x00FFFFFFU
#define COLOR_BLACK 0x00000000U
#define GUI_DRAW_DELAY 100

static void _cbMain (WM_MESSAGE * pMsg)
{
    GUI_RECT Rect;

    switch (pMsg->MsgId)
    {
        case WM_CREATE:
            {
```

```
break;
    }
case WM_PAINT:
    {
/* Clear background to white */
        GUI_SetBkColor(COLOR_WHITE);
        GUI_Clear();
/* Draw "Hello World!" in black in the center */
        WM_GetClientRect(&Rect);
        GUI_SetColor(COLOR_BLACK);
        GUI_DispStringInRect("Hello World!", &Rect, GUI_TA_VCENTER |
GUI_TA_HCENTER);
break;
    }
default:
    {
        WM_DefaultProc(pMsg);
break;
    }
}
void emWinTask (void)
{
    int32_t xSize;
    int32_t ySize;
/* Initialize emWin */
    GUI_Init();
/* Get screen dimensions */
    xSize = LCD_GetXSize();
    ySize = LCD_GetYSize();
/* Create main window */
    WM_CreateWindowAsChild(0, 0, xSize, ySize, WM_HBKWIN, WM_CF_SHOW, _cbMain, 0);
/* Enter main drawing loop */
while (1)
```

```

{
    GUI_Delay(GUI_DRAW_DELAY);
}
}

```

**Note**

For further example code please consult SEGGER emWin documentation, which can be downloaded [here](#), as well as the Quick Start Guide and example project(s) provided with your Evaluation Kit (if applicable).

## 4.2.74 Azure RTOS FileX Block Media I/O Driver (rm\_filex\_block\_media)

### Modules

#### Functions

`fsp_err_t` [RM\\_FILEX\\_BLOCK\\_MEDIA\\_Open](#) (`rm_filex_block_media_ctrl_t *const p_ctrl, rm_filex_block_media_cfg_t const *const p_cfg`)

`fsp_err_t` [RM\\_FILEX\\_BLOCK\\_MEDIA\\_Close](#) (`rm_filex_block_media_ctrl_t *const p_ctrl`)

`void` [RM\\_FILEX\\_BLOCK\\_MEDIA\\_BlockDriver](#) (`FX_MEDIA *p_fx_media`)

Access Block Media device functions open, close, read, write and control. [More...](#)

#### Detailed Description

Middleware for the Azure RTOS FileX File System control using Block Media on RA MCUs.

## Overview

This module provides the hardware port layer for FileX file system. After initializing this module, refer to the FileX API reference to use the file system: <https://docs.microsoft.com/en-us/azure/rtos/filex/>

#### Features

The FileX Block Media module supports the following features:

- Callbacks for insertion and removal for removable devices.
- ThreadX is typically required for FileX. To use FileX without ThreadX `FX_STANDALONE_ENABLE` must be defined.
- Unless `FX_SINGLE_THREAD` or `FX_STANDALONE_ENABLE` are defined, all FileX operations are thread safe.

## Configuration

### Build Time Configurations for rm\_filex\_block\_media

The following build time configurations are defined in fsp\_cfg/middleware/rm\_filex\_block\_media\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	Selects if code for parameter checking is to be included in the build.

### Configurations for Middleware > Storage > FileX I/O Driver on rm\_filex\_block\_media

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_filex_block_media_0	Module name.
Callback	Name must be a valid C symbol	g_rm_filex_block_media_0_callback	A user callback function can be provided. If this callback function is provided, it will be called when media is inserted or removed. It will also be called during operations by the lower level block media as a way for the user to provide their desired waiting functionality.
Partition Number	<ul style="list-style-type: none"> <li>0</li> <li>1</li> <li>2</li> <li>3</li> </ul>	0	The partition to use for partitioned media. This partition will only be used if a Master Boot Record with partition table exists at block 0 of the media, otherwise the FileX FAT boot record should exist or be formatted to block 0.

### Build Time Configurations for fx

The following build time configurations are defined in fsp\_cfg/azure/fx/fx\_user.h:

Configuration	Options	Default	Description
Common > Max Long Name Len	Value must be greater than or equal to 13 and		Specifies the maximum file name size for FileX.

	less than or equal to 256, or empty		If left blank the default value is 256. Legal values range between 13 and 256.
Common > Max Last Name Len	Value must be greater than or equal to 13 and less than or equal to 256, or empty		This value defines the maximum file name length, which includes full path name. If left blank the default value is 256. Legal values range between 13 and 256.
Common > Max Sector Cache	Value must be greater than 0 or empty		Specifies the maximum number of logical sectors that can be cached by FileX. The actual number of sectors that can be cached is lesser of this constant and how many sectors can fit in the amount of memory supplied at <code>fx_media_open</code> . The default value if left blank is 256. All values must be a power of 2.
Common > Fat Map Size	Value must be greater than 0 or empty		Specifies the number of sectors that can be represented in the FAT update map. The default value if left blank is 256. Larger values help reduce unneeded updates of secondary FAT sectors.
Common > Max Fat Cache	Value must be greater than 0 or empty		Specifies the number of entries in the internal FAT cache. The default value if left blank is 16. All values must be a power of 2.
Threading > Update Rate (Seconds)	Value must be greater than 0 or empty		Specifies rate at which system time in FileX is adjusted. Default value if left blank is 10, specifying that the FileX system time is updated every 10 seconds.
Threading > No Timer	<ul style="list-style-type: none"> <li>• Enabled</li> </ul>	Disabled (default)	Eliminates the ThreadX

	<ul style="list-style-type: none"> <li>• Disabled (default)</li> </ul>		timer setup to update the FileX system time and date. Doing so causes default time and date to be placed on all file operations.
Threading > Single Thread	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Eliminates ThreadX protection logic from the FileX source. It should be used if FileX is being used only from one thread.
Threading > Standalone	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Enables FileX to be used in standalone mode (without Azure RTOS).
Extra Features > Don't Update Open Files	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, FileX does not update already opened files.
Extra Features > Media Search Cache	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, the file search cache optimization is disabled.
Extra Features > Direct Data Read Cache Fill	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, the direct read sector update of cache is disabled.
Extra Features > Media Statistics	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, gathering of media statistics is disabled.
Extra Features > Single Open Legacy	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, legacy single open logic for the same file is enabled.
Extra Features > Rename Path Inherit	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, renaming inherits path information.
Extra Features > No Local Path	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, removes local path logic from FileX, resulting in smaller code size.
Extra Features > 64-bit LBA	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, 64-bit sector addresses are used in I/O driver.
Extra Features > Cache	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables the cache, default is enabled.

Extra Features > File Close	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables file close, default is enabled.
Extra Features > Fast Close	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables fast open, default is enabled.
Extra Features > Force Memory Operation	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables force memory operation, default is enabled.
Extra Features > Build Options	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables build options, default is enabled.
Extra Features > One Line Function	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables one line function, default is enabled.
Extra Features > FAT Entry Refresh	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables FAT entry refresh, default is enabled.
Extra Features > Consecutive Detect	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables consecutive detect, default is enabled.
Extra Features > Enable exFAT	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Enables exFAT support in FileX.
Fault Tolerant > Fault Tolerant Service	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, enables the FileX Fault Tolerant Module. Enabling Fault Tolerant automatically defines the symbol <code>FX_FAULT_TOLERANT</code> and <code>FX_FAULT_TOLERANT_DATA</code> .
Fault Tolerant > Fault Tolerant Data	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, FileX immediately passes all file data write requests to the media's driver. This potentially decreases performance, but helps limit lost file data. Note that enabling this feature does not automatically enable FileX Fault Tolerant Module, which should be enabled separately.
Fault Tolerant > Fault Tolerant	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled (default)	When enabled, FileX immediately passes

(default)

write requests of all system sectors (boot, FAT, and directory sectors) to the media's driver. This potentially decreases performance, but helps limit corruption to lost clusters. Note that enabling this feature does not automatically enable FileX Fault Tolerant Module, which should be enabled separately.

Defines byte offset in the boot sector where the cluster for the fault tolerant log is. By default if left blank this value is 116. This field takes 4 bytes. Bytes 116 through 119 are chosen because they are marked as reserved by FAT 12/16/32/exFAT specification.

Fault Tolerant > Fault Tolerant Boot Index

Value must be greater than or equal to 116 and less than or equal to 119

Error Checking

- Enabled (default)
- Disabled

Enabled (default)

### Configurations for Azure RTOS > FileX > FileX on Block Media

This module can be added to the Stacks tab via New Stack > Azure RTOS > FileX > FileX on Block Media.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_fx_media0	Symbol used for media_ptr parameter in FileX APIs
Volume Name	Name must be a valid C symbol	Volume 1	Volume name string, which is a maximum of 11 characters.
Number of FATs	Number of FATs must be an integer greater than 0	1	Number of FATs in the media. The minimal value is 1 for the primary FAT. Values greater than 1 result in additional FAT copies being maintained at run-time.

Directory Entries	Number of Directory Entries must be an integer greater than 0	256	Number of directory entries in the root directory.
Hidden Sectors	Number of Hidden Sectors must be an integer	0	Number of sectors hidden before this media's boot sector. If using media formatted with multiple partitions this number should correspond to the starting block number for the desired partition.
Total Sectors	Total Sectors must be an integer greater than 0	3751936	Total number of sectors in the media. When using a Renesas provided block media implementation, total sectors can be fetched by the infoGet from the block media API. Any removable media must be inserted and initialized first to retrieve this info.
Bytes per Sector	Bytes per Sector must be multiple of 32	512	Number of bytes per sector, which is typically 512. FileX requires this to be a multiple of 32. When using a Renesas provided block media implementation, bytes per sector can be fetched by the infoGet from the block media API. Any removable media must be inserted and initialized first to retrieve this info.
Sectors per Cluster	Sectors per Cluster must be an integer greater than 0	1	Number of sectors in each cluster. The cluster is the minimum allocation unit in a FAT file system.
Volume Serial Number (exFAT only)	Volume Serial Number must be an integer greater than 0	12345	Serial number to be used for this volume. exFAT only.
Boundary Unit (exFAT only)	Boundary unit must be an integer greater than 0	128	Physical data area alignment size, in number of sectors.

exFAT only.

Working media  
memory size

Memory size must be 512  
an integer greater than  
or equal to the size of  
one sector

Memory allocated for  
file system. Memory  
size must be an integer  
greater than or equal  
to the size of one  
sector.

## Usage Notes

### Pending during Read/Write

The FileX Block Media driver provides a number of events in the user callback to handle waiting or pending while it is doing blocking operations. The events received in the callback will differ depending on the lower level block media driver in use.

If the lower level block media driver is `rm_block_media_spi` (SPI blocks on read/write operations):

- The user will receive `RM_BLOCK_MEDIA_EVENT_POLL_STATUS` in the user callback while the lower level driver is polling for the read/write operation to be complete. The user can choose to do a thread sleep or software delay upon receiving this event in the callback.
- Once the operation is complete no other callbacks will be received.

If the lower level block media driver is `rm_block_media_sdmmc` (SDMMC is interrupt based, the FileX Block Media driver will still block while waiting for interrupts from SDMMC):

- The user will receive `RM_BLOCK_MEDIA_EVENT_WAIT` in the user callback when the FileX Block Media driver begins waiting for an interrupt event from SDMMC. This is sent from a thread context. The user can choose to pend on a semaphore, sleep the thread, or do a software delay upon receiving this event in the callback. The FileX Block Media driver thread will block until an interrupt is received.
- Once an SDMMC interrupt is received the user will receive `RM_BLOCK_MEDIA_EVENT_WAIT_END` in the user callback. This is sent from an interrupt context. The user can choose to give a semaphore on this event or do nothing.
- If SDMMC is busy on a long erase after receiving the interrupt the FileX Block Media driver will send `RM_BLOCK_MEDIA_EVENT_POLL_STATUS` to the user callback and proceed to do a blocking poll on SDMMC status. The user can choose to do a thread sleep or software delay upon receiving this event in the callback. This event will not be received by the user on typical operations by FileX.

### Partitioned Media

When using `fx_format` to format a partition the number of hidden sectors should match the starting block number of the partition and the total number of sectors should be equal to the number of sectors in the partition.

### Unused User Callback Events

Certain events are defined in `rm_block_media_event_t` but not returned by the FileX Block Media user callback:

- `RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE`: This event is handled internally and operation success is indicated by FileX API calls returning `FX_SUCCESS`.
- `RM_BLOCK_MEDIA_EVENT_ERROR`: This event is handled internally and operation failure will

be indicated by an error return code from FileX API calls.

## Examples

### Basic Example

This is a basic example of FileX Block Media in an application.

```
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_FILE_NAME "TEST_FILE.txt"
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_BUFFER_SIZE_BYTES (10240)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_PARTITION_NUMBER (0)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_BLOCK_SIZE (512)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_DIRECTORY_ENTRIES (128)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_FATS (1)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_HIDDEN_SECTORS (0)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_TOTAL_SECTORS (1073741824)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTOR_SIZE (512)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_CLUSTER (1)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_HEADS (1)
#define RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_TRACK (1)
extern rm_filex_block_media_instance_t g_filex_block_media0;
extern rm_filex_block_media_instance_ctrl_t g_filex_block_media0_ctrl;
extern rm_filex_block_media_cfg_t g_filex_block_media0_cfg;
extern FX_MEDIA g_fx_media0;
extern uint8_t g_fx_media0_memory[RM_FILEX_BLOCK_MEDIA_EXAMPLE_BLOCK_SIZE];
extern uint8_t g_file_data[RM_FILEX_BLOCK_MEDIA_EXAMPLE_BUFFER_SIZE_BYTES];
extern uint8_t g_read_buffer[RM_FILEX_BLOCK_MEDIA_EXAMPLE_BUFFER_SIZE_BYTES];
void rm_filex_block_media_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FILEX_BLOCK_MEDIA_Open(&g_filex_block_media0_ctrl,
&g_filex_block_media0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize FileX */
    fx_system_initialize();

    /* Open the media. If the media is removable, it must be inserted before calling
```

```
 * fx_media_open. This assumes the disk is already partitioned and formatted. */
  UINT fx_err = fx_media_open(&g_fx_media0,
  "filex_example_media",
  RM_FILEX_BLOCK_MEDIA_BlockDriver,
                                &g_filex_block_media0,
                                g_fx_media0_memory,
  sizeof(g_fx_media0_memory));
  handle_fx_error(fx_err);
  /* Create a file */
  fx_err = fx_file_create(&g_fx_media0, RM_FILEX_BLOCK_MEDIA_EXAMPLE_FILE_NAME);
  handle_fx_error(fx_err);
  /* Open source file for writing. */
  FX_FILE sourceFile;
  fx_err = fx_file_open(&g_fx_media0, &sourceFile,
  RM_FILEX_BLOCK_MEDIA_EXAMPLE_FILE_NAME, FX_OPEN_FOR_WRITE);
  handle_fx_error(fx_err);
  /* Write file data. */
  fx_err = fx_file_write(&sourceFile, g_file_data, sizeof(g_file_data));
  handle_fx_error(fx_err);
  /* Close the file. */
  fx_err = fx_file_close(&sourceFile);
  handle_fx_error(fx_err);
  /* Open the source file in read mode. */
  fx_err = fx_file_open(&g_fx_media0, &sourceFile,
  RM_FILEX_BLOCK_MEDIA_EXAMPLE_FILE_NAME, FX_OPEN_FOR_READ);
  handle_fx_error(fx_err);
  /* Read file data. */
  ULONG actual_size_read;
  fx_err = fx_file_read(&sourceFile, g_read_buffer, sizeof(g_file_data),
  &actual_size_read);
  handle_fx_error(fx_err);
  assert(sizeof(g_file_data) == actual_size_read);
  /* Close the file. */
  fx_err = fx_file_close(&sourceFile);
```

```
    handle_fx_error(fx_err);

    /* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));

    /* Close the Media */
    fx_err = fx_media_close(&g_fx_media0);
    handle_fx_error(fx_err);
}
```

## Format Example

This shows how to partition and format a disk if it is not already partitioned and formatted.

```
void rm_filex_block_media_format_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FILEX_BLOCK_MEDIA_Open(&g_filex_block_media0_ctrl,
    &g_filex_block_media0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Format the media */
    UINT fx_err =
    fx_media_format(&g_fx_media0, // Pointer to
    FileX media control block.
    RM_FILEX_BLOCK_MEDIA_BlockDriver, // Driver entry
    &g_filex_block_media0, // Pointer to Block Media
    Driver
    g_fx_media0_memory, // Media buffer pointer
    sizeof(g_fx_media0_memory), // Media buffer size
    "EXAMPLE_VOLUME", // Volume Name
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_FATS,
    // Number of FATs
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_DIRECTORY_ENTRIES,
    // Directory Entries
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_HIDDEN_SECTORS,
    // Hidden sectors
}
```

```

RM_FILEX_BLOCK_MEDIA_EXAMPLE_TOTAL_SECTORS,          // Total sectors
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTOR_SIZE,
// Sector size

RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_CLUSTER,    // Sectors per cluster
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_HEADS,
// Heads
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_TRACK);
// Sectors per track
    handle_fx_error(fx_err);
}

```

### Callback Pend Example

This shows how to use the I/O driver callback with ThreadX in order to wait/pend for operations to complete.

```

TX_SEMAPHORE g_operation_wait_semaphore;
/* Callback called by FileX block media I/O driver needs to pend on operation. */
void rm_filex_block_media_test_callback_pend (rm_filex_block_media_callback_args_t *
p_args)
{
    if (p_args->event & RM_BLOCK_MEDIA_EVENT_WAIT)
    {
        /* Interrupt has not happened for operation, get semaphore to wait for it. This will
be called from the FileX I/O driver thread. */
        tx_semaphore_get(&g_operation_wait_semaphore, TX_WAIT_FOREVER);
    }
    if (p_args->event & RM_BLOCK_MEDIA_EVENT_WAIT_END)
    {
        /* Interrupt has occurred for operation, post semaphore so that wait will end. This
will be called from an interrupt context. */
        tx_semaphore_put(&g_operation_wait_semaphore);
    }
}

```

```
if (p_args->event & RM_BLOCK_MEDIA_EVENT_POLL_STATUS)
{
    /* Interrupt has been received from block media device but operation is still
ongoing. The FileX I/O driver will wait on the driver busy status.
    * This event can be used to put the thread to sleep while waiting. This will be
called from the FileX I/O driver thread. */
    tx_thread_sleep(1);
}
}

void rm_filex_block_media_callback_pend_example (void)
{
    /* Create semaphore for driver use */
    tx_semaphore_create(&g_operation_wait_semaphore, "operation_wait_semaphore", 0);
    /* Open media driver.*/
    fsp_err_t err = RM_FILEX_BLOCK_MEDIA_Open(&g_filex_block_media0_ctrl,
&g_filex_block_media0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Format the media */
    UINT fx_err =
fx_media_format(&g_fx_media0, // Pointer to
FileX media control block.
    RM_FILEX_BLOCK_MEDIA_BlockDriver, // Driver entry
    &g_filex_block_media0, // Pointer to Block Media
Driver
    g_fx_media0_memory, // Media buffer pointer
    sizeof(g_fx_media0_memory), // Media buffer size
    "EXAMPLE_VOLUME", // Volume Name
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_FATS,
// Number of FATs
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_DIRECTORY_ENTRIES,
// Directory Entries
    RM_FILEX_BLOCK_MEDIA_EXAMPLE_HIDDEN_SECTORS,
// Hidden sectors
```

```
RM_FILEX_BLOCK_MEDIA_EXAMPLE_TOTAL_SECTORS,          // Total sectors
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTOR_SIZE,
// Sector size

RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_CLUSTER,    // Sectors per cluster
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_NUM_HEADS,
// Heads
                RM_FILEX_BLOCK_MEDIA_EXAMPLE_SECTORS_PER_TRACK);
// Sectors per track
    handle_fx_error(fx_err);
}
```

## Media Insertion Example

This shows how to use the callback to wait for media insertion.

```
volatile uint32_t g_rm_filex_block_media_insertion_events = 0;
volatile uint32_t g_rm_filex_block_media_removal_events = 0;
/* Callback called by media driver when a removable device is inserted or removed. */
void rm_filex_block_media_test_callback (rm_filex_block_media_callback_args_t *
p_args)
{
    if (p_args->event & RM_BLOCK_MEDIA_EVENT_MEDIA_INSERTED)
    {
        g_rm_filex_block_media_insertion_events++;
    }
    if (p_args->event & RM_BLOCK_MEDIA_EVENT_MEDIA_REMOVED)
    {
        g_rm_filex_block_media_removal_events++;
    }
}
void rm_filex_block_media_media_insertion_example (void)
{
    /* Open media driver.*/
```

```

fsp_err_t err = RM_FILEX_BLOCK_MEDIA_Open(&g_filex_block_media0_ctrl,
&g_filex_block_media0_cfg);

/* Handle any errors. This function should be defined by the user. */
assert(FSP_SUCCESS == err);

/* Wait for media insertion. */
while (0U == g_rm_filex_block_media_insertion_events)
{
/* Wait for media insertion. */
}

/* Open the media. If the media is removable, it must be inserted before calling
* fx_media_open. This assumes the disk is already partitioned and formatted. */
UINT fx_err = fx_media_open(&g_fx_media0,
"filex_example_media",
RM_FILEX_BLOCK_MEDIA_BlockDriver,
&g_filex_block_media0,
g_fx_media0_memory,
sizeof(g_fx_media0_memory));
handle_fx_error(fx_err);
}

```

## Using FileX with Custom Block Media Implementations

When using a Custom Block Media implementation with `rm_filex_block_media` the custom implementation must call `rm_filex_block_media_memory_callback` upon the completion of a read/write operation. This callback should be called with an event of `RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE` and `p_context` of `rm_filex_block_media_instance_ctrl_t` \*. The following example shows how this should be done in the context of a demo RAM block media read function.

```

#define EXAMPLE_BLOCK_MEDIA_RAM_START_ADDR (0x20004AFE)
#define EXAMPLE_BLOCK_MEDIA_RAM_BLOCK_SIZE_BYTES (512)

/* Example implementation of rm_block_media_api_t::read(), user should define custom
block media RAM implementation. */
fsp_err_t RM_BLOCK_MEDIA_CUSTOM_RAM_Read (rm_block_media_ctrl_t * const p_ctrl,
uint8_t * const
p_dest_address,
uint32_t const

```

```

block_address,
                                uint32_t const          num_blocks)
{
    FSP_PARAMETER_NOT_USED(p_ctrl);
    memcpy(p_dest_address,
           (void *) (EXAMPLE_BLOCK_MEDIA_RAM_START_ADDR + (block_address *
EXAMPLE_BLOCK_MEDIA_RAM_BLOCK_SIZE_BYTES)),
           (EXAMPLE_BLOCK_MEDIA_RAM_BLOCK_SIZE_BYTES * num_blocks));
    /* Notify FileX port of operation complete through calling the callback, this is
required for custom block media/FileX port integration */
    rm_block_media_callback_args_t args;
    args.event      = RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE;
    args.p_context = (void *) &g_filex_block_media0_ctrl;
    rm_filex_block_media_memory_callback(&args);
    return FSP_SUCCESS;
}

```

## Data Structures

```
struct rm_filex_block_media_instance_ctrl_t
```

## Data Structure Documentation

### ◆ rm\_filex\_block\_media\_instance\_ctrl\_t

```
struct rm_filex_block_media_instance_ctrl_t
```

Common macro for FSP header files. There is also a corresponding FSP\_FOOTER macro at the end of this file. FileX block media private control block. DO NOT MODIFY. Initialization occurs when RM\_FILEX\_BLOCK\_MEDIA\_Open is called.

## Function Documentation

◆ **RM\_FILEX\_BLOCK\_MEDIA\_Open()**

```
fsp_err_t RM_FILEX_BLOCK_MEDIA_Open ( rm_filex_block_media_ctrl_t *const p_ctrl,
rm_filex_block_media_cfg_t const *const p_cfg )
```

The file system relies on the media to be formatted prior to creating directories and files. The sector size and sector count will change depending on the media type and size.

The File Allocation Table (FAT) starts after the reserved sectors in the media. The FAT area is basically an array of 12-bit, 16-bit, or 32-bit entries that determine if that cluster is allocated or part of a chain of clusters comprising a subdirectory or a file. The size of each FAT entry is determined by the number of clusters that need to be represented. If the number of clusters (derived from the total sectors divided by the sectors per cluster) is less than 4,086, 12-bit FAT entries are used. If the total number of clusters is greater than 4,086 and less than or equal to 65,525, 16-bit FAT entries are used. Otherwise, if the total number of clusters is greater than 65,525, 32-bit FAT entries are used. Initializes callback and configuration for FileX Block Media interface. Call this before calling any FileX functions.

Implements `rm_filex_block_media_api_t::open()`.

**Return values**

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

◆ **RM\_FILEX\_BLOCK\_MEDIA\_Close()**

```
fsp_err_t RM_FILEX_BLOCK_MEDIA_Close ( rm_filex_block_media_ctrl_t *const p_ctrl)
```

Closes media device.

Implements `rm_filex_block_media_api_t::close()`.

**Return values**

FSP_SUCCESS	Media device closed.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes.

**◆ RM\_FILEX\_BLOCK\_MEDIA\_BlockDriver()**

```
void RM_FILEX_BLOCK_MEDIA_BlockDriver ( FX_MEDIA * p_fx_media)
```

Access Block Media device functions open, close, read, write and control.

The RM\_FILEX\_BLOCK\_MEDIA\_BlockDriver function is called from the FileX file system driver and issues requests to a Block Media device through the FSP Block Media Interface. Uses block media driver for accesses.

**Parameters**

[in,out]	p_fx_media	FileX media control block. All information about each open media device are maintained in the FX_MEDIA data type. The I/O driver communicates the success or failure of the request through the fx_media_driver_status member of FX_MEDIA (p_fx_media->fx_media_driver_status). Possible values are documented in the FileX User Guide.
----------	------------	---

**Return values**

None	
------	--

**Returns**

Nothing, but updates FileX media control block.

**4.2.75 Azure RTOS FileX LevelX I/O Driver (rm\_filex\_levelx\_nor)****Modules****Functions**

```
void RM_FILEX_LEVELX_NOR_DeviceDriver (FX_MEDIA *p_fx_media)
```

Access LevelX NOR device functions open, close, read, write and control. [More...](#)

**Detailed Description**

Middleware for the Azure RTOS FileX File System control using LevelX NOR on RA MCUs.

**Overview**

This module provides the hardware port layer for FileX file system. After initializing this module, refer to the FileX API reference to use the file system: <https://docs.microsoft.com/en-us/azure/rtos/filex/>

## Features

The FileX LevelX NOR module supports the following features:

- ThreadX is typically required for FileX. To use FileX without ThreadX `FX_STANDALONE_ENABLE` must be defined.
- Unless `FX_SINGLE_THREAD` or `FX_STANDALONE_ENABLE` are defined, all FileX operations are thread safe.

## Configuration

### Build Time Configurations for `rm_filex_levelx_nor`

The following build time configurations are defined in `fsp_cfg/middleware/rm_filex_levelx_nor_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	Selects if code for parameter checking is to be included in the build.

### Configurations for Middleware > Storage > FileX I/O Driver on `rm_filex_levelx_nor`

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	<code>g_rm_filex_levelx_nor0</code>	Module name.
Callback	Name must be a valid C symbol	<code>g_rm_filex_levelx_nor_0_callback</code>	A user callback function can be provided. If this callback function is provided, it will be called when media is inserted or removed. It will also be called during operations by the lower level block media as a way for the user to provide their desired waiting functionality.
LevelX NOR Name (String)	Manual Entry	<code>g_rm_filex_levelx_nor_0</code>	String name to be input into LevelX API.

### Build Time Configurations for `fx`

The following build time configurations are defined in `fsp_cfg/azure/fx/fx_user.h`:

Configuration	Options	Default	Description
---------------	---------	---------	-------------

---

Common > Max Long Name Len	Value must be greater than or equal to 13 and less than or equal to 256, or empty	Specifies the maximum file name size for FileX. If left blank the default value is 256. Legal values range between 13 and 256.
Common > Max Last Name Len	Value must be greater than or equal to 13 and less than or equal to 256, or empty	This value defines the maximum file name length, which includes full path name. If left blank the default value is 256. Legal values range between 13 and 256.
Common > Max Sector Cache	Value must be greater than 0 or empty	Specifies the maximum number of logical sectors that can be cached by FileX. The actual number of sectors that can be cached is lesser of this constant and how many sectors can fit in the amount of memory supplied at <code>fx_media_open</code> . The default value if left blank is 256. All values must be a power of 2.
Common > Fat Map Size	Value must be greater than 0 or empty	Specifies the number of sectors that can be represented in the FAT update map. The default value if left blank is 256. Larger values help reduce unneeded updates of secondary FAT sectors.
Common > Max Fat Cache	Value must be greater than 0 or empty	Specifies the number of entries in the internal FAT cache. The default value if left blank is 16. All values must be a power of 2.
Threading > Update Rate (Seconds)	Value must be greater than 0 or empty	Specifies rate at which system time in FileX is adjusted. Default value if left blank is 10, specifying that the FileX system time is updated every 10 seconds.

Threading > No Timer	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Eliminates the ThreadX timer setup to update the FileX system time and date. Doing so causes default time and date to be placed on all file operations.
Threading > Single Thread	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Eliminates ThreadX protection logic from the FileX source. It should be used if FileX is being used only from one thread.
Threading > Standalone	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Enables FileX to be used in standalone mode (without Azure RTOS).
Extra Features > Don't Update Open Files	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, FileX does not update already opened files.
Extra Features > Media Search Cache	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, the file search cache optimization is disabled.
Extra Features > Direct Data Read Cache Fill	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, the direct read sector update of cache is disabled.
Extra Features > Media Statistics	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	When disabled, gathering of media statistics is disabled.
Extra Features > Single Open Legacy	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, legacy single open logic for the same file is enabled.
Extra Features > Rename Path Inherit	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, renaming inherits path information.
Extra Features > No Local Path	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, removes local path logic from FileX, resulting in smaller code size.
Extra Features > 64-bit LBA	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, 64-bits sector addresses are used in I/O driver.
Extra Features > Cache	<ul style="list-style-type: none"> <li>• Enabled (default)</li> </ul>	Enabled (default)	Enables or disables the cache, default is

	<ul style="list-style-type: none"> <li>• Disabled</li> </ul>		enabled.
Extra Features > File Close	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables file close, default is enabled.
Extra Features > Fast Close	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables fast open, default is enabled.
Extra Features > Force Memory Operation	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables force memory operation, default is enabled.
Extra Features > Build Options	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables build options, default is enabled.
Extra Features > One Line Function	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables one line function, default is enabled.
Extra Features > FAT Entry Refresh	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables FAT entry refresh, default is enabled.
Extra Features > Consecutive Detect	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	Enables or disables consecutive detect, default is enabled.
Extra Features > Enable exFAT	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	Enables exFAT support in FileX.
Fault Tolerant > Fault Tolerant Service	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, enables the FileX Fault Tolerant Module. Enabling Fault Tolerant automatically defines the symbol <code>FX_FAULT_TOLERANT</code> and <code>FX_FAULT_TOLERA NT_DATA</code> .
Fault Tolerant > Fault Tolerant Data	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, FileX immediately passes all file data write requests to the media's driver. This potentially decreases performance, but helps limit lost file data. Note that enabling this feature does not automatically enable FileX Fault Tolerant Module, which should be enabled separately.

Fault Tolerant > Fault Tolerant	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, FileX immediately passes write requests of all system sectors (boot, FAT, and directory sectors) to the media's driver. This potentially decreases performance, but helps limit corruption to lost clusters. Note that enabling this feature does not automatically enable FileX Fault Tolerant Module, which should be enabled separately.
Fault Tolerant > Fault Tolerant Boot Index	Value must be greater than or equal to 116 and less than or equal to 119		Defines byte offset in the boot sector where the cluster for the fault tolerant log is. By default if left blank this value is 116. This field takes 4 bytes. Bytes 116 through 119 are chosen because they are marked as reserved by FAT 12/16/32/exFAT specification.
Error Checking	<ul style="list-style-type: none"> <li>• Enabled (default)</li> <li>• Disabled</li> </ul>	Enabled (default)	

### Configurations for Azure RTOS > FileX > FileX on LevelX NOR

This module can be added to the Stacks tab via New Stack > Azure RTOS > FileX > FileX on LevelX NOR.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_fx_media0	Symbol used for media_ptr parameter in FileX APIs
Volume Name	Name must be a valid C symbol	Volume 1	Volume name string, which is a maximum of 11 characters.
Number of FATs	Number of FATs must be an integer greater than 0	1	Number of FATs in the media. The minimal value is 1 for the primary FAT. Values greater than 1 result in additional FAT copies

being maintained at run-time.

Directory Entries	Number of Directory Entries must be an integer greater than 0	256	Number of directory entries in the root directory.
Hidden Sectors	Number of Hidden Sectors must be an integer	0	Number of sectors hidden before this media's boot sector. If using media formatted with multiple partitions this number should correspond to the starting block number for the desired partition.
Total Sectors	Total Sectors must be an integer greater than 0	3751936	Total number of sectors in the media. When using a Renesas provided block media implementation, total sectors can be fetched by the infoGet from the block media API. Any removable media must be inserted and initialized first to retrieve this info.
Sectors per Cluster	Sectors per Cluster must be an integer greater than 0	1	Number of sectors in each cluster. The cluster is the minimum allocation unit in a FAT file system.
Volume Serial Number (exFAT only)	Volume Serial Number must be an integer greater than 0	12345	Serial number to be used for this volume. exFAT only.
Boundary Unit (exFAT only)	Boundary unit must be an integer greater than 0	128	Physical data area alignment size, in number of sectors. exFAT only.
Working media memory size	Memory size must be an integer greater than or equal to the size of one sector	512	Memory allocated for file system. Memory size must be an integer greater than or equal to the size of one sector.

## Usage Notes

### Pending during Write/Erase

If the underlying LevelX NOR driver performs a blocking operation that requires waiting to complete (such as a long write/erase on NOR SPI), a callback can be provided to provide a way to wait with an OS-specific thread wait. This callback will also pass up block erase events.

## Partitioned Media

Partitioned media is not supported directly by the FileX LevelX NOR port.

# Examples

## Basic Example

This is a basic example of FileX Block Media in an application.

```
#define RM_FILEX_LEVELX_NOR_EXAMPLE_FILE_NAME "TEST_FILE.txt"
#define RM_FILEX_LEVELX_NOR_EXAMPLE_BUFFER_SIZE_BYTES (10240)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_PARTITION_NUMBER (0)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_BLOCK_SIZE (512)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_DIRECTORY_ENTRIES (128)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_FATS (1)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_HIDDEN_SECTORS (0)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_TOTAL_SECTORS (512)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_SECTOR_SIZE (512)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_CLUSTER (1)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_HEADS (1)
#define RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_TRACK (1)
extern rm_filex_levelx_nor_instance_t g_filex_levelx_nor0;
extern rm_filex_levelx_nor_instance_ctrl_t g_filex_levelx_nor0_ctrl;
extern rm_filex_levelx_nor_cfg_t g_filex_levelx_nor0_cfg;
extern FX_MEDIA g_fx_media0;
extern uint8_t g_fx_media0_memory[RM_FILEX_LEVELX_NOR_EXAMPLE_BLOCK_SIZE];
extern uint8_t g_file_data[RM_FILEX_LEVELX_NOR_EXAMPLE_BUFFER_SIZE_BYTES];
extern uint8_t g_read_buffer[RM_FILEX_LEVELX_NOR_EXAMPLE_BUFFER_SIZE_BYTES];
void rm_filex_levelx_nor_example (void)
{
    /* Initialize FileX */
    fx_system_initialize();
    /* Initialize LevelX */
    lx_nor_flash_initialize();
}
```

```
/* Open the media. This assumes the flash is already formatted. */
UINT fx_err = fx_media_open(&g_fx_media0,
"filex_example_media",
RM_FILEX_LEVELX_NOR_DeviceDriver,
&g_filex_levelx_nor0,
g_fx_media0_memory,
sizeof(g_fx_media0_memory));
handle_fx_error(fx_err);
/* Create a file */
fx_err = fx_file_create(&g_fx_media0, RM_FILEX_LEVELX_NOR_EXAMPLE_FILE_NAME);
handle_fx_error(fx_err);
/* Open source file for writing. */
FX_FILE sourceFile;
fx_err = fx_file_open(&g_fx_media0, &sourceFile,
RM_FILEX_LEVELX_NOR_EXAMPLE_FILE_NAME, FX_OPEN_FOR_WRITE);
handle_fx_error(fx_err);
/* Write file data. */
fx_err = fx_file_write(&sourceFile, g_file_data, sizeof(g_file_data));
handle_fx_error(fx_err);
/* Close the file. */
fx_err = fx_file_close(&sourceFile);
handle_fx_error(fx_err);
/* Open the source file in read mode. */
fx_err = fx_file_open(&g_fx_media0, &sourceFile,
RM_FILEX_LEVELX_NOR_EXAMPLE_FILE_NAME, FX_OPEN_FOR_READ);
handle_fx_error(fx_err);
/* Read file data. */
ULONG actual_size_read;
fx_err = fx_file_read(&sourceFile, g_read_buffer, sizeof(g_file_data),
&actual_size_read);
handle_fx_error(fx_err);
assert(sizeof(g_file_data) == actual_size_read);
/* Close the file. */
fx_err = fx_file_close(&sourceFile);
```

```
    handle_fx_error(fx_err);

    /* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));

    /* Close the Media */
    fx_err = fx_media_close(&g_fx_media0);
    handle_fx_error(fx_err);
}
```

## Format Example

This shows how to partition and format a disk if it is not already partitioned and formatted.

```
extern rm_levelx_nor_spi_cfg_t g_levelx_nor_spi0_cfg;
#define RM_FILEX_LEVELX_NOR_EXAMPLE_SPI_SECTOR_SIZE (4096)
void rm_filex_levelx_nor_format_example (void)
{
    spi_flash_instance_t * p_spi_flash_instance = (spi_flash_instance_t *)
g_levelx_nor_spi0_cfg.p_lower_lvl;
    spi_flash_status_t    status;
    /* Erase flash prior to usage */
    fsp_err_t err = p_spi_flash_instance->p_api->open(p_spi_flash_instance->p_ctrl,
p_spi_flash_instance->p_cfg);
    assert(FSP_SUCCESS == err);
    for (uint32_t i = g_levelx_nor_spi0_cfg.address_offset;
        i < g_levelx_nor_spi0_cfg.size;
        i += RM_FILEX_LEVELX_NOR_EXAMPLE_SPI_SECTOR_SIZE)
    {
        err = p_spi_flash_instance->p_api->erase(p_spi_flash_instance->p_ctrl,
                                                (uint8_t *)
g_levelx_nor_spi0_cfg.base_address + i,
RM_FILEX_LEVELX_NOR_EXAMPLE_SPI_SECTOR_SIZE);
        assert(FSP_SUCCESS == err);
        status.write_in_progress = true;
        while (status.write_in_progress)
```

```

    {
        err =
p_spi_flash_instance->p_api->statusGet(p_spi_flash_instance->p_ctrl, &status);
        assert(FSP_SUCCESS == err);
    }
}

err = p_spi_flash_instance->p_api->close(p_spi_flash_instance->p_ctrl);
assert(FSP_SUCCESS == err);

/* Format the media */
UINT fx_err = fx_media_format(&g_fx_media0,
// Pointer to FileX media control block.
RM_FILEX_LEVELX_NOR_DeviceDriver, // Driver entry
&g_filex_levelx_nor0, // Pointer to Block Media
Driver
g_fx_media0_memory, // Media buffer pointer
sizeof(g_fx_media0_memory), // Media buffer size
"EXAMPLE_VOLUME", // Volume Name
RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_FATS,
// Number of FATs
RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_DIRECTORY_ENTRIES,
// Directory Entries
RM_FILEX_LEVELX_NOR_EXAMPLE_HIDDEN_SECTORS,
// Hidden sectors
RM_FILEX_LEVELX_NOR_EXAMPLE_TOTAL_SECTORS, // Total sectors
RM_FILEX_LEVELX_NOR_EXAMPLE_SECTOR_SIZE,
// Sector size
RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_CLUSTER, // Sectors per cluster
RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_HEADS,
// Heads
RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_TRACK);
// Sectors per track
handle_fx_error(fx_err);

```

```
}
```

## Callback Wait Example

This shows how to use the I/O driver callback with ThreadX in order to wait for operations to complete.

```
/* Callback called by FileX block media I/O driver needs to wait on operation. */
void rm_filex_levelx_nor_test_callback_wait (rm_filex_levelx_nor_callback_args_t *
p_args)
{
    if (p_args->event & RM_FILEX_LEVELX_NOR_EVENT_BUSY)
    {
        /* Put the thread to sleep while waiting for operation to complete. */
        tx_thread_sleep(1);
    }
}

void rm_filex_levelx_nor_callback_wait_example (void)
{
    /* Format the media */
    UINT fx_err = fx_media_format(&g_fx_media0,
// Pointer to FileX media control block.
    RM_FILEX_LEVELX_NOR_DeviceDriver,           // Driver entry
                                                &g_filex_levelx_nor0, // Pointer to Block Media
Driver
                                                g_fx_media0_memory, // Media buffer pointer
    sizeof(g_fx_media0_memory),                // Media buffer size
    "EXAMPLE_VOLUME",                          // Volume Name
                                                RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_FATS,
// Number of FATs
                                                RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_DIRECTORY_ENTRIES,
// Directory Entries
                                                RM_FILEX_LEVELX_NOR_EXAMPLE_HIDDEN_SECTORS,
// Hidden sectors
```

```

RM_FILEX_LEVELX_NOR_EXAMPLE_TOTAL_SECTORS,          // Total sectors

                RM_FILEX_LEVELX_NOR_EXAMPLE_SECTOR_SIZE,

// Sector size

RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_CLUSTER,    // Sectors per cluster

                RM_FILEX_LEVELX_NOR_EXAMPLE_NUM_HEADS,

// Heads

                RM_FILEX_LEVELX_NOR_EXAMPLE_SECTORS_PER_TRACK);

// Sectors per track

    handle_fx_error(fx_err);
}

```

## Data Structures

struct [rm\\_filex\\_levelx\\_nor\\_callback\\_args\\_t](#)

struct [rm\\_filex\\_levelx\\_nor\\_cfg\\_t](#)

struct [rm\\_filex\\_levelx\\_nor\\_instance\\_ctrl\\_t](#)

struct [rm\\_filex\\_levelx\\_nor\\_instance\\_t](#)

## Enumerations

enum [rm\\_filex\\_levelx\\_nor\\_event\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_filex\\_levelx\\_nor\\_callback\\_args\\_t](#)

struct <a href="#">rm_filex_levelx_nor_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">rm_filex_levelx_nor_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

### ◆ [rm\\_filex\\_levelx\\_nor\\_cfg\\_t](#)

struct <a href="#">rm_filex_levelx_nor_cfg_t</a>	
FileX LevelX configuration	
Data Fields	

UINT(*)	<a href="#">nor_driver_initialize</a> (LX_NOR_FLASH *)
	Pointer to the initialization function.
LX_NOR_FLASH *	<a href="#">p_nor_flash</a>
	NOR Flash instance.
CHAR *	<a href="#">p_nor_flash_name</a>
	NOR Flash instance name.
<a href="#">fsp_err_t</a> (*)	<a href="#">close</a> ()
	Pointer to underlying driver close.
void(*)	<a href="#">p_callback</a> (rm_filex_levelx_nor_callback_args_t *p_args)
	Pointer to callback function.
void const *	<a href="#">p_context</a>
	Placeholder for user data.

#### ◆ [rm\\_filex\\_levelx\\_nor\\_instance\\_ctrl\\_t](#)

struct <a href="#">rm_filex_levelx_nor_instance_ctrl_t</a>		
FileX block media private control block. DO NOT MODIFY. Initialization occurs when <a href="#">RM_FILEX_LEVELX_NOR_Open</a> is called.		
Data Fields		
<a href="#">rm_filex_levelx_nor_cfg_t</a> const *	<a href="#">p_cfg</a>	Pointer to instance configuration.

#### ◆ [rm\\_filex\\_levelx\\_nor\\_instance\\_t](#)

struct <a href="#">rm_filex_levelx_nor_instance_t</a>		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<a href="#">rm_filex_levelx_nor_instance_ctrl_t</a> *	<a href="#">p_ctrl</a>	Pointer to the control structure for this instance.

<a href="#">rm_filex_levelx_nor_cfg_t</a> const *const	p_cfg	Pointer to the configuration structure for this instance.
---	-------	---

## Enumeration Type Documentation

### ◆ rm\_filex\_levelx\_nor\_event\_t

enum <a href="#">rm_filex_levelx_nor_event_t</a>	
Common macro for FSP header files. There is also a corresponding FSP_FOOTER macro at the end of this file. Options for the callback events.	
Enumerator	
RM_FILEX_LEVELX_NOR_EVENT_BUSY	Pending operation, user can define their own wait functionality.

## Function Documentation

### ◆ RM\_FILEX\_LEVELX\_NOR\_DeviceDriver()

void <a href="#">RM_FILEX_LEVELX_NOR_DeviceDriver</a> ( FX_MEDIA * <i>p_fx_media</i> )		
Access LevelX NOR device functions open, close, read, write and control.		
The <a href="#">RM_FILEX_LEVELX_NOR_DeviceDriver</a> function is called from the FileX file system driver and issues requests to a LevelX NOR device through the LevelX API.		
<b>Parameters</b>		
[in,out]	p_fx_media	FileX media control block. All information about each open media device are maintained in the FX_MEDIA data type. The I/O driver communicates the success or failure of the request through the fx_media_driver_status member of FX_MEDIA (p_fx_media->fx_media_driver_status). Possible values are documented in the FileX User Guide.
<b>Return values</b>		
None		
<b>Returns</b>		
Nothing, but updates FileX media control block.		

## 4.2.76 FreeRTOS+FAT Port (rm\_freertos\_plus\_fat)

### Modules

#### Functions

fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_Open</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_cfg_t const *const p_cfg)
fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_MediaInit</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_device_t *const p_device)
fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_DiskInit</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl, rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk)
fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_DiskDeinit</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk)
fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_InfoGet</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t *const p_disk, rm_freertos_plus_fat_info_t *const p_info)
fsp_err_t	<a href="#">RM_FREERTOS_PLUS_FAT_Close</a> (rm_freertos_plus_fat_ctrl_t *const p_ctrl)

#### Detailed Description

Middleware for the FAT File System control on RA MCUs.

## Overview

This module provides the hardware port layer for FreeRTOS+FAT file system. After initializing this module, refer to the FreeRTOS+FAT API reference to use the file system:  
[https://www.freertos.org/FreeRTOS-Plus/FreeRTOS\\_Plus\\_FAT/index.html](https://www.freertos.org/FreeRTOS-Plus/FreeRTOS_Plus_FAT/index.html)

#### Features

The FreeRTOS+FAT port module supports the following features:

- Callbacks for insertion and removal for removable devices.
- Helper function to initialize FF\_Disk\_t
- Blocking read and write port functions that use FreeRTOS task notification to pend if FreeRTOS is used
- FreeRTOS is optional

## Configuration

### Build Time Configurations for rm\_freertos\_plus\_fat

The following build time configurations are defined in fsp\_cfg/middleware/rm\_freertos\_plus\_fat\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for FreeRTOS+ > FreeRTOS+FAT Port for RA

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_freertos_plus_fat_0	Module name.
Total Number of Sectors	Must be a non-negative integer	31293440	Enter the total number of sectors on the device. If this is not known, update <code>rm_freertos_plus_fat_disk_cfg_t::num_blocks</code> after calling <a href="#">RM_FREERTOS_PLUS_FAT_MediaInit()</a> .
Sector Size (bytes)	Must be a power of 2 multiple of 512	512	Select the sector size. Must match the underlying media sector size and at least 512. If this is not known, update <code>rm_freertos_plus_fat_disk_cfg_t::num_blocks</code> after calling <a href="#">RM_FREERTOS_PLUS_FAT_MediaInit()</a> .
Cache Size (bytes)	Must be a power of 2 multiple of 512	1024	Select the cache size. Must be a multiple of the sector size and at least 2 times the sector size.
Partition Number	Must be a non-negative integer	0	Select the partition number for this disk.
Callback	Name must be a valid C symbol	NULL	A user callback function can be provided. If this callback function is provided, it will be called when a card is inserted or removed.

## Usage Notes

### Pending during Read/Write

If the underlying driver supports non-blocking operations, the FreeRTOS+FAT port pends the active

FreeRTOS task during read and write operations so other tasks can run in the background.

If FreeRTOS is not used, the FreeRTOS+FAT port spins in a while loop waiting for read and write operations to complete.

### FreeRTOS+FAT without FreeRTOS

To use FreeRTOS+FAT without FreeRTOS, copy FreeRTOSConfigMinimal.h to one of your project's include paths and rename it FreeRTOSConfig.h.

Also, update the Malloc function to malloc and the Free function to free in the Common configurations.

## Examples

### Basic Example

This is a basic example of FreeRTOS+FAT in an application.

```
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME "TEST_FILE.txt"
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES (10240)
#define RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER (0)
extern rm_freertos_plus_fat_instance_ctrl_t g_freertos_plus_fat0_ctrl;
extern const rm_freertos_plus_fat_cfg_t g_freertos_plus_fat0_cfg;
extern rm_freertos_plus_fat_disk_cfg_t g_rm_freertos_plus_fat_disk_cfg;
extern uint8_t g_file_data[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
extern uint8_t g_read_buffer[RM_FREERTOS_PLUS_FAT_EXAMPLE_BUFFER_SIZE_BYTES];
void rm_freertos_plus_fat_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
    * RM_FREERTOS_PLUS_FAT_MediaInit. */
    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg.device);

    assert(FSP_SUCCESS == err);

    /* Initialize one disk for each partition used in the application. */
```

```
    FF_Disk_t disk;

    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);

    assert(FSP_SUCCESS == err);

    /* Mount each disk. This assumes the disk is already partitioned and formatted. */
    FF_Error_t ff_err = FF_Mount(&disk,
RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);

    handle_ff_error(ff_err);

    /* Add the disk to the file system. */
    FF_FS_Add("/", &disk);

    /* Open a source file for writing. */
    FF_FILE * pxSourceFile = ff_fopen((const char *)
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "w");

    assert(NULL != pxSourceFile);

    /* Write file data. */
    size_t size_return = ff_fwrite(g_file_data, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    int close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);

    /* Open the source file in read mode. */
    pxSourceFile = ff_fopen((const char *) RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME,
"r");

    assert(NULL != pxSourceFile);

    /* Read file data. */
    size_return = ff_fread(g_read_buffer, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);

    /* Close the file. */
    close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);

    /* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));
}
```

## Format Example

This shows how to partition and format a disk if it is not already partitioned and formatted.

```
void rm_freertos_plus_fat_format_example (void)
{
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
    &g_freertos_plus_fat0_cfg);

    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);

    /* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
    * RM_FREERTOS_PLUS_FAT_MediaInit. */
    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl,
    &g_rm_freertos_plus_fat_disk_cfg.device);
    assert(FSP_SUCCESS == err);

    /* Initialize one disk for each partition used in the application. */
    FF_Disk_t disk;
    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
    &g_rm_freertos_plus_fat_disk_cfg, &disk);
    assert(FSP_SUCCESS == err);

    /* Try to mount the disk. If the disk is not formatted, mount will fail. */
    FF_Error_t ff_err = FF_Mount(&disk,
    RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);
    if (FF_isERR((uint32_t) ff_err))
    {
        /* The disk is likely not formatted. Partition and format the disk, then mount
again. */
        FF_PartitionParameters_t partition_params;
        partition_params.ulSectorCount =
g_rm_freertos_plus_fat_disk_cfg.device.sector_count;
        partition_params.ulHiddenSectors = 1;
        partition_params.ulInterSpace = 0;
        memset(partition_params.xSizes, 0, sizeof(partition_params.xSizes));
        partition_params.xSizes[RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER] =
```

```
        (BaseType_t) partition_params.ulSectorCount - 1;
    partition_params.xPrimaryCount = 1;
    partition_params.eSizeType     = eSizeIsSectors;
    ff_err = FF_Partition(&disk, &partition_params);
    handle_ff_error(ff_err);
    ff_err = FF_Format(&disk, RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER,
pdFALSE, pdFALSE);
    handle_ff_error(ff_err);
    ff_err = FF_Mount(&disk, RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);
    handle_ff_error(ff_err);
}
}
```

## Media Insertion Example

This shows how to use the callback to wait for media insertion.

```
#if 2 == BSP_CFG_RTOS
static EventGroupHandle_t xUSBEventGroupHandle = NULL;
#else
volatile uint32_t g_rm_freertos_plus_fat_insertion_events = 0;
volatile uint32_t g_rm_freertos_plus_fat_removal_events = 0;
#endif

/* Callback called by media driver when a removable device is inserted or removed. */
void rm_freertos_plus_fat_test_callback (rm_freertos_plus_fat_callback_args_t *
p_args)
{
#if 2 == BSP_CFG_RTOS
    /* Post an event if FreeRTOS is available. */
    BaseType_t xHigherPriorityTaskWoken = pdFALSE;
    xEventGroupSetBitsFromISR(xUSBEventGroupHandle, p_args->event,
&xHigherPriorityTaskWoken);
    portYIELD_FROM_ISR(xHigherPriorityTaskWoken);
#else
    /* If FreeRTOS is not used, set a global flag. */

```

```
if (p_args->event & RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED)
{
    g_rm_freertos_plus_fat_insertion_events++;
}
if (p_args->event & RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_REMOVED)
{
    g_rm_freertos_plus_fat_removal_events++;
}
#endif
}
void rm_freertos_plus_fat_media_insertion_example (void)
{
#if 2 == BSP_CFG_RTOS
    /* Create event flags if FreeRTOS is used. */
    xUSBEventGroupHandle = xEventGroupCreate();
    TEST_ASSERT_NOT_EQUAL(NULL, xUSBEventGroupHandle);
#endif
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Wait for media insertion. */
#if 2 == BSP_CFG_RTOS
        EventBits_t xEventGroupValue = xEventGroupWaitBits(xUSBEventGroupHandle,
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED,
                                                                pdTRUE,
                                                                pdFALSE,
                                                                portMAX_DELAY);
        assert(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED ==
            (RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED & xEventGroupValue));
#else
    while (0U == g_rm_freertos_plus_fat_insertion_events)
    {
```

```
/* Wait for media insertion. */
    }
#endif

/* Initialize the media and the disk. If the media is removable, it must be inserted
before calling
* RM_FREERTOS_PLUS_FAT_MediaInit. */
    err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg.device);
    assert(FSP_SUCCESS == err);
/* Initialize one disk for each partition used in the application. */
    FF_Disk_t disk;
    err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,
&g_rm_freertos_plus_fat_disk_cfg, &disk);
    assert(FSP_SUCCESS == err);
}
```

## Media Insertion Example for USB

This shows how to use the callback to read and write to USB media.

```
void rm_freertos_plus_fat_usb_example (void)
{
#if 2 == BSP_CFG_RTOS
    /* Create event flags if FreeRTOS is used. */
    xUSBEventGroupHandle = xEventGroupCreate();
#endif
    /* Open media driver.*/
    fsp_err_t err = RM_FREERTOS_PLUS_FAT_Open(&g_freertos_plus_fat0_ctrl,
&g_freertos_plus_fat0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Wait for the USB media to be attached. */
#if 2 == BSP_CFG_RTOS
    EventBits_t xEventGroupValue = xEventGroupWaitBits(xUSBEventGroupHandle,
RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED,
```

```
pdTRUE,  
pdFALSE,  
portMAX_DELAY);  
  
assert(RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED ==  
       (RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED & xEventGroupValue));  
#else  
while (0U == g_rm_freertos_plus_fat_insertion_events)  
{  
    /* Wait for the USB media to be attached. */  
}  
#endif  
  
/* Initialize the media and the disk. If the media is removable, it must be inserted  
before calling  
* RM_FREERTOS_PLUS_FAT_MediaInit. */  
err = RM_FREERTOS_PLUS_FAT_MediaInit(&g_freertos_plus_fat0_ctrl,  
&g_rm_freertos_plus_fat_disk_cfg.device);  
assert(FSP_SUCCESS == err);  
  
/* Initialize one disk for each partition used in the application. */  
FF_Disk_t disk;  
err = RM_FREERTOS_PLUS_FAT_DiskInit(&g_freertos_plus_fat0_ctrl,  
&g_rm_freertos_plus_fat_disk_cfg, &disk);  
assert(FSP_SUCCESS == err);  
  
/* Mount each disk. This assumes the disk is already partitioned and formatted. */  
FF_Error_t ff_err = FF_Mount(&disk,  
RM_FREERTOS_PLUS_FAT_EXAMPLE_PARTITION_NUMBER);  
handle_ff_error(ff_err);  
  
/* Add the disk to the file system. */  
FF_FS_Add("/", &disk);  
  
/* Open a source file for writing. */  
FF_FILE * pxSourceFile = ff_fopen((const char *)  
RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME, "w");  
assert(NULL != pxSourceFile);  
  
/* Write file data. */  
size_t size_return = ff_fwrite(g_file_data, sizeof(g_file_data), 1, pxSourceFile);
```

```
    assert(1 == size_return);
/* Close the file. */
int close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);
/* Open the source file in read mode. */
    pxSourceFile = ff_fopen((const char *) RM_FREERTOS_PLUS_FAT_EXAMPLE_FILE_NAME,
"r");
    assert(NULL != pxSourceFile);
/* Read file data. */
    size_return = ff_fread(g_read_buffer, sizeof(g_file_data), 1, pxSourceFile);
    assert(1 == size_return);
/* Close the file. */
    close_err = ff_fclose(pxSourceFile);
    assert(0 == close_err);
/* Verify the file data read matches the file written. */
    assert(0U == memcmp(g_file_data, g_read_buffer, sizeof(g_file_data)));
}
```

## Data Structures

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_ctrl\\_t](#)

FreeRTOS plus FAT private control block. DO NOT MODIFY. Initialization occurs when `RM_FREERTOS_PLUS_FAT_Open` is called.

## Function Documentation

### ◆ RM\_FREERTOS\_PLUS\_FAT\_Open()

```
fsp_err_t RM_FREERTOS_PLUS_FAT_Open ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_cfg_t const *const p_cfg )
```

Initializes lower layer media device.

Implements `rm_freertos_plus_fat_api_t::open()`.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_OUT_OF_MEMORY	Not enough memory to create semaphore.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `rm_block_media_api_t::open`

### ◆ RM\_FREERTOS\_PLUS\_FAT\_MediaInit()

```
fsp_err_t RM_FREERTOS_PLUS_FAT_MediaInit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_device_t *const p_device )
```

Initializes the media device. This function blocks until all identification and configuration commands are complete.

Implements `rm_freertos_plus_fat_api_t::mediaInit()`.

#### Return values

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `rm_block_media_api_t::mediaInit`
- `rm_block_media_api_t::infoGet`

◆ **RM\_FREERTOS\_PLUS\_FAT\_DiskInit()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_DiskInit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk )
```

Initializes a FreeRTOS+FAT disk structure. This function calls FF\_CreateIOManger.

Implements `rm_freertos_plus_fat_api_t::diskInit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.
FSP_ERR_INTERNAL	Call to FF_CreateIOManger failed.

◆ **RM\_FREERTOS\_PLUS\_FAT\_DiskDeinit()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_DiskDeinit ( rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk )
```

Deinitializes a FreeRTOS+FAT disk structure. This function calls FF\_DeleteIOManger.

Implements `rm_freertos_plus_fat_api_t::diskDeinit()`.

**Return values**

FSP_SUCCESS	Module is initialized and ready to access the memory device.
FSP_ERR_ASSERTION	An input parameter is invalid.
FSP_ERR_NOT_OPEN	Module has not been initialized.

**◆ RM\_FREERTOS\_PLUS\_FAT\_InfoGet()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_InfoGet ( rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk, rm_freertos_plus_fat_info_t *const p_info )
```

Get partition information. This function can only be called after [rm\\_freertos\\_plus\\_fat\\_api\\_t::diskInit\(\)](#).

Implements [rm\\_freertos\\_plus\\_fat\\_api\\_t::infoGet\(\)](#).

**Return values**

FSP_SUCCESS	Information stored in p_info.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

**◆ RM\_FREERTOS\_PLUS\_FAT\_Close()**

```
fsp_err_t RM_FREERTOS_PLUS_FAT_Close ( rm_freertos_plus_fat_ctrl_t *const p_ctrl)
```

Closes media device.

Implements [rm\\_freertos\\_plus\\_fat\\_api\\_t::close\(\)](#).

**Return values**

FSP_SUCCESS	Media device closed.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- [rm\\_block\\_media\\_api\\_t::close](#)

**4.2.77 FreeRTOS Plus TCP (rm\_freertos\_plus\_tcp)****Modules**

Middleware for using TCP on RA MCUs.

**Overview**

FreeRTOS Plus TCP is a TCP stack created for use with FreeRTOS.

This module provides the NetworkInterface required to use FreeRTOS Plus TCP with the [Ethernet \(r\\_ether\)](#) driver.

Please refer to the [FreeRTOS Plus TCP documentation](#) for further details.

## Configuration

### Build Time Configurations for FreeRTOS\_Plus\_TCP

The following build time configurations are defined in aws/FreeRTOSIPConfig.h:

Configuration	Options	Default	Description
Print debug messages	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Disable	If ipconfigHAS_DEBUG_PRINTF is set to 1 then FreeRTOS_debug_printf should be defined to the function used to print out the debugging messages.
Print info messages	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Disable	Set to 1 to print out non debugging messages, for example the output of the FreeRTOS_netstat() command, and ping replies. If ipconfigHAS_PRINTF is set to 1 then FreeRTOS_printf should be set to the function used to print out the messages.
Byte order of the target MCU	pdFREERTOS_LITTLE_ENDIAN	pdFREERTOS_LITTLE_ENDIAN	Define the byte order of the target MCU
IP/TCP/UDP checksums	<ul style="list-style-type: none"> <li>Disable</li> <li>Enable</li> </ul>	Enable	If the network card/driver includes checksum offloading (IP/TCP/UDP checksums) then set ipconfigDRIVER_INCLUDED_RX_IP_CHECKSUM to 1 to prevent the software stack repeating the checksum calculations.
Receive Block Time	Value must be a non-negative integer	10000	Amount of time FreeRTOS_recv() will block for. The timeouts can be set per socket,

Send Block Time	Value must be a non-negative integer	10000	using setsockopt(). Amount of time FreeRTOS_send() will block for. The timeouts can be set per socket, using setsockopt().
DNS caching	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	DNS caching
DNS Request Attempts	Value must be an integer	2	When a cache is present, ipconfigDNS_REQUEST_ATTEMPTS can be kept low and also DNS may use small timeouts.
IP stack task priority	Manual Entry	configMAX_PRIORITIES - 2	Set the priority of the task that executes the IP stack.
Stack size in words (not bytes)	Manual Entry	configMINIMAL_STACK_SIZE * 5	The size, in words (not bytes), of the stack allocated to the FreeRTOS+TCP stack.
Network Events call vApplicationIPNetworkEventHook	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	vApplicationIPNetworkEventHook is called when the network connects or disconnects.
Max UDP send block time	Manual Entry	15000 / portTICK_PERIOD_MS	Max UDP send block time
Use DHCP	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	If ipconfigUSE_DHCP is 1 then FreeRTOS+TCP will attempt to retrieve an IP address, netmask, DNS server address and gateway address from a DHCP server.
DHCP Register Hostname	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Register hostname when using DHCP
DHCP Uses Unicast	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	DHCP uses unicast.
DHCP Send Discover After Auto IP	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	DHCP Send Discover After Auto IP
DHCP callback function	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Provide an implementation of the DHCP callback function (xApplicationDHCPHook)

Interval between transmissions	Manual Entry	120000 / portTICK_PERIOD_MS	When ipconfigUSE_DHCP is set to 1, DHCP requests will be sent out at increasing time intervals until either a reply is received from a DHCP server and accepted, or the interval between transmissions reaches ipconfigMAXIMUM_DISCOVER_TX_PERIOD.
ARP Cache Entries	Value must be an integer	6	The maximum number of entries that can exist in the ARP table at any one time
ARP Request Retransmissions	Value must be an integer	5	ARP requests that do not result in an ARP response will be re-transmitted a maximum of ipconfigMAX_ARP_RETRANSMISSIONS times before the ARP request is aborted.
Maximum time before ARP table entry becomes stale	Value must be an integer	150	The maximum time between an entry in the ARP table being created or refreshed and the entry being removed because it is stale
Use string for IP Address	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Take an IP in decimal dot format (for example, "192.168.0.1") as its parameter FreeRTOS_inet_addr_quick() takes an IP address as four separate numerical octets (for example, 192, 168, 0, 1) as its parameters
Total number of available network buffers	Value must be an integer	10	Define the total number of network buffer that are available to the IP stack
Set the maximum number of events	Please enter a valid function name without spaces or funny	ipconfigNUM_NETWORK_BUFFER_DESCRIPTORS + 5	Set the maximum number of events that can be queued for

	characters		
Enable FreeRTOS_sendto() without calling Bind	<ul style="list-style-type: none"> <li>• Enable</li> <li>• Disable</li> </ul>	Disable	processing at any one time. The event queue must be a minimum of 5 greater than the total number of network buffers  Set to 1 then calling FreeRTOS_sendto() on a socket that has not yet been bound will result in the IP stack automatically binding the socket to a port number from the range socketAUTO_PORT_ALL OCATION_START_NUMB ER to 0xffff. If ipconfigA LLOW_SOCKET_SEND_ WITHOUT_BIND is set to 0 then calling FreeRTOS_sendto() on a socket that has not yet been bound will result in the send operation being aborted.
TTL values for UDP packets	Value must be an integer	128	Define the Time To Live (TTL) values used in outgoing UDP packets
TTL values for TCP packets	Value must be an integer	128	Defines the Time To Live (TTL) values used in outgoing TCP packets
Use TCP and all its features	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Use TCP and all its features
Let TCP use windowing mechanism	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Let TCP use windowing mechanism
Maximum number of bytes the payload of a network frame can contain	Value must be an integer	1500	Maximum number of bytes the payload of a network frame can contain
Basic DNS client or resolver	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Set ipconfigUSE_DNS to 1 to include a basic DNS client/resolver. DNS is used through the FreeRTOS_gethostbyname() API function.
Reply to incoming ICMP echo (ping) requests	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	If ipconfigREPLY_TO_INCOMING_PINGS is set to 1 then the IP stack

			will generate replies to incoming ICMP echo (ping) requests.
FreeRTOS_SendPingRequest() is available	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigSUPPORT_OUTGOING_PINGS is set to 1 then the FreeRTOS_SendPingRequest() API function is available.
FreeRTOS_select() (and associated) API function is available	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigSUPPORT_SELECT_FUNCTION is set to 1 then the FreeRTOS_select() (and associated) API function is available
Filter out non Ethernet II frames.	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	If ipconfigFILTER_OUT_NON_ETHERNET_II_FRAMES is set to 1 then Ethernet frames that are not in Ethernet II format will be dropped. This option is included for potential future IP stack developments
Responsibility of the Ethernet interface to filter out packets	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	If ipconfigETHERNET_DRIVER_FILTERS_FRAME_TYPES is set to 1 then it is the responsibility of the Ethernet interface to filter out packets that are of no interest.
Send RST packets, when receive unknown packets.	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	TCP will not send RST packets in reply to TCP unknown or out-of-order packets
Block time to simulate MAC interrupts	Please enter a valid function name without spaces or funny characters	20 / portTICK_PERIOD_MS	The windows simulator cannot really simulate MAC interrupts, and needs to block occasionally to allow other tasks to run
Access 32-bit fields in the IP packets	Value must be an integer	2	To access 32-bit fields in the IP packets with 32-bit memory instructions, all packets will be stored 32-bit-aligned, plus 16-bits. This has to do with the contents of the IP-packets: all 32-bit fields are 32-bit-aligned, plus 16-bit

Size of the pool of TCP window descriptors	Value must be an integer	240	Define the size of the pool of TCP window descriptors
Size of Rx buffer for TCP sockets	Value must be an integer	3000	Define the size of Rx buffer for TCP sockets
Size of Tx buffer for TCP sockets	Value must be an integer	3000	Define the size of Tx buffer for TCP sockets
TCP keep-alive	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	TCP keep-alive is available or not
TCP keep-alive interval	Value must be an integer	120	TCP keep-alive interval in second
The socket semaphore to unblock the MQTT task (USER_SEMAPHORE)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (WAKE_CALLBACK)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (USE_CALLBACKS)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (TX_DRIVER)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
The socket semaphore to unblock the MQTT task (RX_DRIVER)	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	The socket semaphore is used to unblock the MQTT task
Possible optimisation for expert users	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	Possible optimisation for expert users - requires network driver support. It is useful when there is high network traffic. If non-zero value then instead of passing received packets into the IP task one at a time the network interface can chain received packets together and pass them into the IP task in one go. If set to 0 then only one buffer will be sent at a time.

## Usage Notes

In order to use the NetworkInterface implementation provided by Renesas for RA devices:

- Configure an `r_ether` instance and provide a pointer to the instance of the NetworkInterface as follows:

```
/* Reference used by the NetworkInterface to access the ethernet instance. */
extern ether_instance_t const * gp_freertos_ether;

...

/* Make it reference the configured ether instance. */
ether_instance_t const * gp_freertos_ether = &g_ether_instance;
```

- Follow the TCP stack initialization procedure as described here: [FreeRTOS+TCP Networking Tutorial: Initializing the TCP/IP Stack](#)

#### Note

*The MAC address passed to `FreeRTOS_IPInit` must match the MAC address configured in the `r_ether` instance. `g_ether_instance` must have `vEtherISRcallback` configured as the callback. The `xApplicationGetRandomNumber` and `ulApplicationGetNextSequenceNumber` functions should be implemented in systems using FreeRTOS Plus TCP without Secure Sockets. To connect to a server using an IP address the macro `ipconfigINCLUDE_FULL_INET_ADDR` must be set to 1.*

#### Limitations

- Zero-copy is not currently supported by the NetworkInterface.

## 4.2.78 FreeRTOS Port (rm\_freertos\_port)

### Modules

FreeRTOS port for RA MCUs.

## Overview

#### Note

*The FreeRTOS Port does not provide any interfaces to the user. Consult the FreeRTOS documentation at <https://www.freertos.org/Documentation> for further information.*

### Features

The RA FreeRTOS port supports the following features:

- Standard FreeRTOS configurations
- Hardware stack monitor

# Configuration

## Build Time Configurations for all

The following build time configurations are defined in aws/FreeRTOSConfig.h:

Configuration	Options	Default	Description
General > Custom FreeRTOSConfig.h	Manual Entry		Add a path to your custom FreeRTOSConfig.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
General > Use Preemption	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Set to Enabled to use the preemptive RTOS scheduler, or Disabled to use the cooperative RTOS scheduler.
General > Use Port Optimised Task Selection	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Some FreeRTOS ports have two methods of selecting the next task to execute - a generic method, and a method that is specific to that port.</p> <p>The Generic method: Is used when Use Port Optimized Task Selection is set to 0, or when a port specific method is not implemented. Can be used with all FreeRTOS ports. Is completely written in C, making it less efficient than a port specific method. Does not impose a limit on the maximum number of available priorities.</p> <p>A port specific method: Is not available for all ports. Is used when Use Port Optimized Task</p>

Selection is Enabled. Relies on one or more architecture specific assembly instructions (typically a Count Leading Zeros [CLZ] or equivalent instruction) so can only be used with the architecture for which it was specifically written. Is more efficient than the generic method. Typically imposes a limit of 32 on the maximum number of available priorities.

Set Use Tickless Idle to Enabled to use the low power tickless mode, or Disabled to keep the tick interrupt running at all times. Low power tickless implementations are not provided for all FreeRTOS ports.

Enter the frequency in Hz at which the internal clock that drives the peripheral used to generate the tick interrupt will be executing - this is normally the same clock that drives the internal CPU clock. This value is required in order to correctly configure timer peripherals.

The frequency of the RTOS tick interrupt. The tick interrupt is used to measure time. Therefore a higher tick frequency means time can be measured to a higher resolution. However, a high tick frequency also means that the RTOS kernel will use more CPU time

General > Use Tickless Idle

- Enabled
- Disabled

Disabled

General > Cpu Clock Hz

Manual Entry

SystemCoreClock

General > Tick Rate Hz

Must be an integer and greater than 0 1000

so be less efficient. The RTOS demo applications all use a tick rate of 1000Hz. This is used to test the RTOS kernel and is higher than would normally be required.

More than one task can share the same priority. The RTOS scheduler will share processor time between tasks of the same priority by switching between the tasks during each RTOS tick. A high tick rate frequency will therefore also have the effect of reducing the 'time slice' given to each task.

The number of priorities available to the application tasks. Any number of tasks can share the same priority. Each available priority consumes RAM within the RTOS kernel so this value should not be set any higher than actually required by your application.

The size of the stack used by the idle task. Generally this should not be reduced from the value set in the FreeRTOSConfig.h file provided with the demo application for the port you are using. Like the stack size parameter to the xTaskCreate() and xTaskCreateStatic() functions, the stack size is specified in words, not bytes. If each item placed on

General > Max  
Priorities

Must be an integer and  
greater than 0 5

General > Minimal  
Stack Size

Must be an integer and  
greater than 0 128

General > Max Task Name Len	Must be an integer and greater than 0	16	the stack is 32-bits, then a stack size of 100 means 400 bytes (each 32-bit stack item consuming 4 bytes).
General > Use 16-bit Ticks	Disabled	Disabled	<p>The maximum permissible length of the descriptive name given to a task when the task is created. The length is specified in the number of characters including the NULL termination byte.</p> <p>Time is measured in 'ticks' - which is the number of times the tick interrupt has executed since the RTOS kernel was started. The tick count is held in a variable of type TickType_t. Defining configUSE_16_BIT_TICKS as 1 causes TickType_t to be defined (typedef'ed) as an unsigned 16bit type. Defining configUSE_16_BIT_TICKS as 0 causes TickType_t to be defined (typedef'ed) as an unsigned 32bit type.</p> <p>Using a 16-bit type will greatly improve performance on 8- and 16-bit architectures, but limits the maximum specifiable time period to 65535 'ticks'. Therefore, assuming a tick frequency of 250Hz, the maximum time a task can delay or block when a 16bit counter is used is 262 seconds, compared to 17179869 seconds when using a 32-bit counter.</p>

General > Idle Should Yield

- Enabled
- Disabled

Enabled

This parameter controls the behaviour of tasks at the idle priority. It only has an effect if:

- The preemptive scheduler is being used.
- The application creates tasks that run at the idle priority.
- If Use Time Slicing is Enabled then tasks that share the same priority will time slice. If none of the tasks get preempted then it might be assumed that each task at a given priority will be allocated an equal amount of processing time - and if the priority is above the idle priority then this is indeed the case.
- When tasks share the idle priority the behaviour can be slightly different. If Idle Should Yield is Enabled then the idle task will yield immediately if any other task at the idle priority is ready to run. This ensures the minimum amount of time is spent in the idle task when application tasks are available for scheduling. This behaviour can however have undesirable effects (depending on the needs of your application) as depicted below:

The diagram above shows the execution pattern of four tasks that are all running at the idle priority. Tasks A, B and C are

application tasks. Task I is the idle task. A context switch occurs with regular period at times T0, T1, ..., T6. When the idle task yields task A starts to execute - but the idle task has already consumed some of the current time slice. This results in task I and task A effectively sharing the same time slice. The application tasks B and C therefore get more processing time than the application task A.

This situation can be avoided by:

If appropriate, using an idle hook in place of separate tasks at the idle priority.

Creating all application tasks at a priority greater than the idle priority.

Setting Idle Should Yield to Disabled.

Setting Idle Should Yield to Disabled prevents the idle task from yielding processing time until the end of its time slice. This ensure all tasks at the idle priority are allocated an equal amount of processing time (if none of the tasks get pre-empted) - but at the cost of a greater proportion of the total processing time being allocated to the idle task.

Setting Use Task Notifications to Enabled will include direct to

General > Use Task Notifications

- Enabled                      Enabled
- Disabled

task notification functionality and its associated API in the build.  
Setting Use Task Notifications to Disabled will exclude direct to task notification functionality and its associated API from the build.

Each task consumes 8 additional bytes of RAM when direct to task notifications are included in the build.

Set to Enabled to include mutex functionality in the build, or Disabled to omit mutex functionality from the build. Readers should familiarise themselves with the differences between mutexes and binary semaphores in relation to the FreeRTOS functionality.

Set to Enabled to include recursive mutex functionality in the build, or Disabled to omit recursive mutex functionality from the build.

Set to Enabled to include counting semaphore functionality in the build, or Disabled to omit counting semaphore functionality from the build.

The queue registry has two purposes, both of which are associated with RTOS kernel aware debugging:

General > Use Mutexes      • Enabled      Disabled  
   • Disabled

General > Use Recursive Mutexes      • Enabled      Disabled  
   • Disabled

General > Use Counting Semaphores      • Enabled      Enabled  
   • Disabled

General > Queue Registry Size      Must be an integer and greater than 0      10

It allows a textual name to be associated with a queue for easy queue identification within a debugging GUI.

It contains the information required by a debugger to locate each registered queue and semaphore.

The queue registry has no purpose unless you are using a RTOS kernel aware debugger. Registry Size defines the maximum number of queues and semaphores that can be registered. Only those queues and semaphores that you want to view using a RTOS kernel aware debugger need be registered. See the API reference documentation for `vQueueAddToRegistry()` and `vQueueUnregisterQueue()` for more information.

Set to Enabled to include queue set functionality (the ability to block, or pend, on multiple queues and semaphores), or Disabled to omit queue set functionality.

If Use Time Slicing is Enabled, FreeRTOS uses prioritised preemptive scheduling with time slicing. That means the RTOS scheduler will always run the highest priority task that is in the Ready state, and will switch between tasks of equal priority on

General > Use Queue Sets

- Enabled
- Disabled

Disabled

General > Use Time Slicing

- Enabled
- Disabled

Disabled

every RTOS tick interrupt. If Use Time Slicing is Disabled then the RTOS scheduler will still run the highest priority task that is in the Ready state, but will not switch between tasks of equal priority just because a tick interrupt has occurred.

If Use Newlib Reentrant is Enabled then a newlib reent structure will be allocated for each created task. Note Newlib support has been included by popular demand, but is not used by the FreeRTOS maintainers themselves. FreeRTOS is not responsible for resulting newlib operation. User must be familiar with newlib and must provide system-wide implementations of the necessary stubs. Be warned that (at the time of writing) the current newlib design implements a system-wide malloc() that must be provided with locks.

The FreeRTOS.h header file includes a set of #define macros that map the names of data types used in versions of FreeRTOS prior to version 8.0.0 to the names used in FreeRTOS version 8.0.0. The macros allow application code to update the version of FreeRTOS they are built against from a pre 8.0.0 version to a post 8.0.0 version without modification. Setting Enable Backward

General > Use Newlib  
Reentrant

- Enabled
- Disabled

Disabled

General > Enable  
Backward Compatibility

- Enabled
- Disabled

Disabled

General > Num Thread Local Storage Pointers	Must be an integer and greater than 0	5	Compatibility to Disabled in FreeRTOSConfig.h excludes the macros from the build, and in so doing allowing validation that no pre version 8.0.0 names are being used.
General > Stack Depth Type	Manual Entry	uint32_t	Sets the number of indexes in each task's thread local storage array.  Sets the type used to specify the stack depth in calls to xTaskCreate(), and various other places stack sizes are used (for example, when returning the stack high water mark). Older versions of FreeRTOS specified stack sizes using variables of type UBaseType_t, but that was found to be too restrictive on 8-bit microcontrollers. Stack Depth Type removes that restriction by enabling application developers to specify the type to use.
General > Message Buffer Length Type	Manual Entry	size_t	FreeRTOS Message buffers use variables of type Message Buffer Length Type to store the length of each message. If Message Buffer Length Type is not defined then it will default to size_t. If the messages stored in a message buffer will never be larger than 255 bytes then defining Message Buffer Length Type to uint8_t will save 3 bytes per message on a 32-bit microcontroller.

Likewise if the messages stored in a message buffer will never be larger than 65535 bytes then defining Message Buffer Length Type to uint16\_t will save 2 bytes per message on a 32-bit microcontroller.

The highest interrupt priority that can be used by any interrupt service routine that makes calls to interrupt safe FreeRTOS API functions. DO NOT CALL INTERRUPT SAFE FREERTOS API FUNCTIONS FROM ANY INTERRUPT THAT HAS A HIGHER PRIORITY THAN THIS! (higher priorities are lower numeric values)

Below is explanation for macros that are set based on this value from FreeRTOS website.

In the RA port, configKERNEL\_INTERRUPT\_PRIORITY is not used and the kernel runs at the lowest priority.

Note in the following discussion that only API functions that end in "FromISR" can be called from within an interrupt service routine.

configMAX\_SYSCALL\_INTERRUPT\_PRIORITY sets the highest interrupt priority from which interrupt safe FreeRTOS API functions can be called.

General > Library Max  
Syscall Interrupt  
Priority

MCU Specific Options

A full interrupt nesting model is achieved by setting `configMAX_SYSCALL_INTERRUPT_PRIORITY` above (that is, at a higher priority level) than `configKERNEL_INTERRUPT_PRIORITY`. This means the FreeRTOS kernel does not completely disable interrupts, even inside critical sections. Further, this is achieved without the disadvantages of a segmented kernel architecture.

Interrupts that do not call API functions can execute at priorities above `configMAX_SYSCALL_INTERRUPT_PRIORITY` and therefore never be delayed by the RTOS kernel execution.

A special note for ARM Cortex-M users: Please read the page dedicated to interrupt priority settings on ARM Cortex-M devices. As a minimum, remember that ARM Cortex-M cores use numerically low priority numbers to represent HIGH priority interrupts, which can seem counter-intuitive and is easy to forget! If you wish to assign an interrupt a low priority do NOT assign it a priority of 0 (or other low numeric value) as this can result in the interrupt actually having the highest priority in the system - and therefore potentially make your

system crash if this priority is above configMAX\_SYSCALL\_INTERRUPT\_PRIORITY.

The lowest priority on a ARM Cortex-M core is in fact 255 - however different ARM Cortex-M vendors implement a different number of priority bits and supply library functions that expect priorities to be specified in different ways. For example, on the RA6M3 the lowest priority you can specify is 15 - and the highest priority you can specify is 0.

The semantics of the configASSERT() macro are the same as the standard C assert() macro. An assertion is triggered if the parameter passed into configASSERT() is zero. configASSERT() is called throughout the FreeRTOS source files to check how the application is using FreeRTOS. It is highly recommended to develop FreeRTOS applications with configASSERT() defined.

The example definition (shown at the top of the file and replicated below) calls vAssertCalled(), passing in the file name and line number of the triggering configASSERT() call (`__FILE__` and `__LINE__` are standard macros provided by most compilers). This is just

General > Assert

Manual Entry

assert(x)

for demonstration as `vAssertCalled()` is not a FreeRTOS function, `configASSERT()` can be defined to take whatever action the application writer deems appropriate.

It is normal to define `configASSERT()` in such a way that it will prevent the application from executing any further. This is for two reasons; stopping the application at the point of the assertion allows the cause of the assertion to be debugged, and executing past a triggered assertion will probably result in a crash anyway.

Note defining `configASSERT()` will increase both the application code size and execution time. When the application is stable the additional overhead can be removed by simply commenting out the `configASSERT()` definition in `FreeRTOSConfig.h`.

```
/* Define
configASSERT() to call
vAssertCalled() if the
assertion fails. The
assertion
has failed if the value
of the parameter
passed into
configASSERT() equals
zero. */
#define configASSERT(
( x ) ) if( ( x ) == 0 )
vAssertCalled( __FILE__,
__LINE__ )
If running FreeRTOS
```

under the control of a debugger, then `configASSERT()` can be defined to just disable interrupts and sit in a loop, as demonstrated below. That will have the effect of stopping the code on the line that failed the assert test - pausing the debugger will then immediately take you to the offending line so you can see why it failed.

```
/* Define
configASSERT() to
disable interrupts and
sit in a loop. */
#define configASSERT(
(x)) if( (x) == 0 ) { t
askDISABLE_INTERRUPTS(); for( ;; ); }
```

Include Application Defined Privileged Functions is only used by FreeRTOS MPU. If Include Application Defined Privileged Functions is Enabled then the application writer must provide a header file called "application\_defined\_privileged\_functions.h", in which functions the application writer needs to execute in privileged mode can be implemented. Note that, despite having a .h extension, the header file should contain the implementation of the C functions, not just the functions' prototypes.

Functions implemented in "application\_defined\_privileged\_functions.h

General > Include  
Application Defined  
Privileged Functions

- Enabled
  - Disabled
- Disabled

" must save and restore the processor's privilege state using the prvRaisePrivilege() function and portRESET\_PRIVILEGE() macro respectively. For example, if a library provided print function accesses RAM that is outside of the control of the application writer, and therefore cannot be allocated to a memory protected user mode task, then the print function can be encapsulated in a privileged function using the following code:

```
void MPU_debug_printf(
const char *pcMessage
)
{
/* State the privilege
level of the processor
when the function was
called. */
BaseType_t
xRunningPrivileged =
prvRaisePrivilege();

/* Call the library
function, which now
has access to all RAM.
*/
debug_printf(
pcMessage );

/* Reset the processor
privilege level to its
original value. */
portRESET_PRIVILEGE(
xRunningPrivileged );
}
```

This technique should only be use during development, and not deployment, as it circumvents the memory protection.

Set to Enabled if you

Hooks > Use Idle Hook

• Enabled

Enabled

	<ul style="list-style-type: none"> <li>• Disabled</li> </ul>		wish to use an idle hook, or Disabled to omit an idle hook.
Hooks > Use Malloc Failed Hook	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>The kernel uses a call to pvPortMalloc() to allocate memory from the heap each time a task, queue or semaphore is created. The official FreeRTOS download includes four sample memory allocation schemes for this purpose. The schemes are implemented in the heap_1.c, heap_2.c, heap_3.c, heap_4.c and heap_5.c source files respectively. Use Malloc Failed Hook is only relevant when one of these three sample schemes is being used. The malloc() failed hook function is a hook (or callback) function that, if defined and configured, will be called if pvPortMalloc() ever returns NULL. NULL will be returned only if there is insufficient FreeRTOS heap memory remaining for the requested allocation to succeed.</p> <p>If Use Malloc Failed Hook is Enabled then the application must define a malloc() failed hook function. If Use Malloc Failed Hook is set to Disabled then the malloc() failed hook function will not be called, even if one is defined. Malloc() failed hook functions must have the name and prototype shown below.</p>

Hooks > Use Daemon Task Startup Hook	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<pre>void vApplicationMallocFailedHook( void );</pre> <p>If Use Timers and Use Daemon Task Startup Hook are both Enabled then the application must define a hook function that has the exact name and prototype as shown below. The hook function will be called exactly once when the RTOS daemon task (also known as the timer service task) executes for the first time. Any application initialisation code that needs the RTOS to be running can be placed in the hook function.</p> <pre>void void vApplicationDaemonTaskStartupHook( void );</pre>
Hooks > Use Tick Hook	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Set to Enabled if you wish to use an tick hook, or Disabled to omit an tick hook.</p>
Hooks > Check For Stack Overflow	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>The stack overflow detection page describes the use of this parameter. This is not recommended for RA MCUs with hardware stack monitor support. RA MCU designs should enable the RA hardware stack monitor instead.</p>
Stats > Use Trace Facility	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Set to Enabled if you wish to include additional structure members and functions to assist with execution visualisation and tracing.</p>
Stats > Use Stats Formatting Functions	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Set Use Trace Facility and Use Stats Formatting Functions to Enabled to include</p>

Stats > Generate Run  
Time Stats

- Enabled
- Disabled

Disabled

Memory Allocation >  
Support Static  
Allocation

- Enabled
- Disabled

Enabled

the vTaskList() and vTaskGetRunTimeStats() functions in the build. Setting either to Disabled will omit vTaskList() and vTaskGetRunTimeStats() from the build.

The Run Time Stats page describes the use of this parameter.

If Support Static Allocation is Enabled then RTOS objects can be created using RAM provided by the application writer. If Support Static Allocation is Disabled then RTOS objects can only be created using RAM allocated from the FreeRTOS heap.

If Support Static Allocation is left undefined it will default to 0.

If Support Static Allocation is Enabled then the application writer must also provide two callback functions: vApplicationGetIdleTaskMemory() to provide the memory for use by the RTOS Idle task, and (if Use Timers is Enabled) vApplicationGetTimerTaskMemory() to provide memory for use by the RTOS Daemon/Timer Service task. Examples are provided below.

/\* Support Static Allocation is Enabled, so the application must provide an implementation of vApplicationGetIdleTaskMe

```
mory() to provide the
memory that is
used by the Idle task. */
void vApplicationGetIdleTaskMemory(
    StaticTask_t **ppxIdleTaskTCBBuffer, <br>
    StackType_t **ppxIdleTaskStackBuffer, <br>
    uint32_t
    *pulIdleTaskStackSize )
{
    /* If the buffers to be
    provided to the Idle
    task are declared
    inside this
    function then they
    must be declared static
    - otherwise they will be
    allocated on
    the stack and so not
    exists after this
    function exits. */
    static StaticTask_t
    xIdleTaskTCB;
    static StackType_t
    uxIdleTaskStack[ configMINIMAL_STACK_SIZE ];

    /* Pass out a pointer to
    the StaticTask_t
    structure in which the
    Idle task's
    state will be stored. */
    *ppxIdleTaskTCBBuffer
    =

    /* Pass out the array
    that will be used as the
    Idle task's stack. */
    *ppxIdleTaskStackBuffer
    = uxIdleTaskStack;

    /* Pass out the size of
    the array pointed to by
    *ppxIdleTaskStackBuffer.
    Note that, as the array
    is necessarily of type
    StackType_t,
    configMINIMAL_STACK_SIZE
    is specified in
    words, not bytes. */
    *pulIdleTaskStackSize
    = configMINIMAL_STACK
```

```
K_SIZE;  
}  
/*-----  
-----*/
```

```
/* Support Static  
Allocation and Use  
Timers are both  
Enabled, so the  
application must  
provide an  
implementation of vAp  
plicationGetTimerTask  
Memory()  
to provide the memory  
that is used by the  
Timer service task. */  
void vApplicationGetTi  
merTaskMemory(  
StaticTask_t **ppxTime  
rTaskTCBBuffer,<br>  
StackType_t **ppxTime  
rTaskStackBuffer,<br>  
uint32_t  
*pulTimerTaskStackSiz  
e )  
{  
/* If the buffers to be  
provided to the Timer  
task are declared  
inside this  
function then they  
must be declared static  
- otherwise they will be  
allocated on  
the stack and so not  
exists after this  
function exits. */  
static StaticTask_t  
xTimerTaskTCB;  
static StackType_t  
uxTimerTaskStack[ con  
figTIMER_TASK_STACK_  
DEPTH ];
```

```
/* Pass out a pointer to  
the StaticTask_t  
structure in which the  
Timer  
task's state will be  
stored. */  
*ppxTimerTaskTCBBuff  
er =
```

```
/* Pass out the array
```

```

that will be used as the
Timer task's stack. */
*ppxTimerTaskStackBu
ffer =
uxTimerTaskStack;

```

```

/* Pass out the size of
the array pointed to by
*ppxTimerTaskStackBu
ffer.

```

```

Note that, as the array
is necessarily of type
StackType_t,
configTIMER_TASK_STA
CK_DEPTH is specified
in words, not bytes. */
*puTimerTaskStackSiz
e = configTIMER_TASK_
STACK_DEPTH;
}

```

Examples of the callback functions that must be provided by the application to supply the RAM used by the Idle and Timer Service tasks if Support Static Allocation is Enabled.

See the Static Vs Dynamic Memory Allocation page for more information.

If Support Dynamic Allocation is Enabled then RTOS objects can be created using RAM that is automatically allocated from the FreeRTOS heap. If Support Dynamic Allocation is set to 0 then RTOS objects can only be created using RAM provided by the application writer.

See the Static Vs Dynamic Memory Allocation page for more information.

The total amount of

Memory Allocation >  
Support Dynamic  
Allocation

- Enabled
- Disabled

Disabled

Memory Allocation >

Must be an integer and 1024

Total Heap Size	greater than 0			RAM available in the FreeRTOS heap. This value will only be used if Support Dynamic Allocation is Enabled and the application makes use of one of the sample memory allocation schemes provided in the FreeRTOS source code download. See the memory configuration section for further details.
Memory Allocation > Application Allocated Heap	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled		<p>By default the FreeRTOS heap is declared by FreeRTOS and placed in memory by the linker. Setting Application Allocated Heap to Enabled allows the heap to instead be declared by the application writer, which allows the application writer to place the heap wherever they like in memory.</p> <p>If heap_1.c, heap_2.c or heap_4.c is used, and Application Allocated Heap is Enabled, then the application writer must provide a <code>uint8_t</code> array with the exact name and dimension as shown below. The array will be used as the FreeRTOS heap. How the array is placed at a specific memory location is dependent on the compiler being used - refer to your compiler's documentation.</p> <pre>uint8_t ucHeap[ configTOTAL_HEAP_SIZE ];</pre>
Timers > Use Timers	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled		Set to Enabled to include software timer

Timers > Timer Task Priority	Must be an integer and greater than 0	3	functionality, or Disabled to omit software timer functionality. See the FreeRTOS software timers page for a full description.
Timers > Timer Queue Length	Must be an integer and greater than 0	10	Sets the priority of the software timer service/daemon task. See the FreeRTOS software timers page for a full description.
Timers > Timer Task Stack Depth	Must be an integer and greater than 0	128	Sets the length of the software timer command queue. See the FreeRTOS software timers page for a full description.
Optional Functions > vTaskPrioritySet() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Sets the stack depth allocated to the software timer service/daemon task. See the FreeRTOS software timers page for a full description.
Optional Functions > uxTaskPriorityGet() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include vTaskPrioritySet() function in build
Optional Functions > vTaskDelete() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include uxTaskPriorityGet() function in build
Optional Functions > vTaskSuspend() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include vTaskDelete() function in build
Optional Functions > xResumeFromISR() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include vTaskSuspend() function in build
Optional Functions > vTaskDelayUntil() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include xResumeFromISR() function in build
Optional Functions > vTaskDelay() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include vTaskDelayUntil() function in build
Optional Functions > xTaskGetSchedulerState() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include vTaskDelay() function in build

Optional Functions > xTaskGetCurrentTaskHandle() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include xTaskGetCurrentTaskHandle() function in build
Optional Functions > uxTaskGetStackHighWaterMark() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include uxTaskGetStackHighWaterMark() function in build
Optional Functions > xTaskGetIdleTaskHandle() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include xTaskGetIdleTaskHandle() function in build
Optional Functions > eTaskGetState() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include eTaskGetState() function in build
Optional Functions > xEventGroupSetBitFromISR() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include xEventGroupSetBitFromISR() function in build
Optional Functions > xTimerPendFunctionCall() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include xTimerPendFunctionCall() function in build
Optional Functions > xTaskAbortDelay() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include xTaskAbortDelay() function in build
Optional Functions > xTaskGetHandle() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include xTaskGetHandle() function in build
Optional Functions > xTaskResumeFromISR() Function	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Include xTaskResumeFromISR() function in build
RA > Hardware Stack Monitor	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Include RA stack monitor
Logging > Print String Function	Manual Entry	printf(x)	
Logging > Logging Max Message Length	Manual Entry	192	
Logging > Logging Include Time and Task Name	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Disabled	

## Clock Configuration

The FreeRTOS port uses the SysTick timer as the system clock. The timer rate is configured in the FreeRTOS component under General > Tick Rate Hz.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

## Hardware Stack Monitor (PSPLIM)

A UsageFault is generated if PSP goes out of the memory area for the stack allocated for the current task. If UsageFault is not enabled, it is escalated to HardFault.

## Hardware Stack Monitor (SPMON)

The hardware stack monitor generates an NMI if the PSP goes out of the memory area for the stack allocated for the current task. A callback can be registered using `R_BSP_GroupIrqWrite()` to be called whenever a stack overflow or underflow of the PSP for a particular thread is detected.

## Stack Monitor Underflow Detection

By default the hardware stack monitor only checks for overflow of the process stack. To check for underflow define `configRECORD_STACK_HIGH_ADDRESS` as 1 on the command line.

## Low Power Modes

When FreeRTOS is configured to use tickless idle, the idle task executes `WFI()` when no task is ready to run. If the MCU is configured to enter software standby mode or deep software standby mode when the idle task executes `WFI()`, the RA FreeRTOS port changes the low power mode to sleep mode so the idle task can wake from `SysTick`. The low power mode settings are restored when the MCU wakes from sleep mode.

## TrustZone Integration

When using an RTOS in a TrustZone project, ARM recommends keeping the RTOS in the non-secure project. Tasks may call non-secure callable functions if the task has allocated a secure context (using `portALLOCATE_SECURE_CONTEXT`).

The secure context can be freed by deleting the thread or using the `portCLEAN_UP_TCB(pxTCB)` macro.

# Examples

## Stack Monitor Example

This is an example of using the stack monitor in an application.

```
#if BSP_FEATURE_BSP_HAS_SP_MON
void stack_monitor_callback (bsp_grp_irq_t irq)
{
    FSP_PARAMETER_NOT_USED(irq);

    if (1U == R_MPU_SPMON->SP[0].CTL_b.ERROR)
    {
        /* Handle main stack monitor error here. */
    }

    if (1U == R_MPU_SPMON->SP[1].CTL_b.ERROR)
```

```
{
/* Handle process stack monitor error here. */
}
}
void rm_freertos_port_stack_monitor_example (void)
{
/* Register a callback to be called when the stack goes outside the allocated stack
area. */
R_BSP_GroupIrqWrite(BSP_GRP_IRQ_MPU_STACK, stack_monitor_callback);
}
#else
/* Allocate stack space to return from UsageFault. */
uint32_t g_stack_overflow_exception_stack[8] BSP_ALIGN_VARIABLE(BSP_STACK_ALIGNMENT)
BSP_PLACE_IN_SECTION(
    BSP_SECTION_STACK);
/* MCUs that do not have an SPMON stack monitor use PSPLIM to detect stack overflows.
When a stack overflow error
* occurs, the UsageFault_Handler fires if it has been enabled. */
void UsageFault_Handler (void)
{
register uint32_t cfsr = SCB->CFSR;
if (cfsr & SCB_CFSR_STKOF_Msk)
{
/* Update PSP and PSPLIM to point to an exception stack frame allocated for stack
overflows. */
register uint32_t * p_exception_stack_frame = (uint32_t *)
(&g_stack_overflow_exception_stack);
__set_PSP((uint32_t) p_exception_stack_frame);
__set_PSPLIM((uint32_t) p_exception_stack_frame);
/* Clear XPSR, only set T-bit. */
p_exception_stack_frame[7] = 1U << 24;
/* Set PC to stack overflow error while loop. When execution returns from the
UsageFault, it will go to the
* stack_overflow_error_occurred function. It cannot return to the location where
```

```
the fault occurred because
 * the MCU does not save the exception stack frame to the stack when a stack
overflow error occurs. */
    p_exception_stack_frame[6] = (uint32_t) stack_overflow_error_occurred;
}
/* Clear flags. */
SCB->CFSR = cfsr;
}
/* This function is called from UsageFault_Handler after a stack overflow occurs. */
void stack_overflow_error_occurred (void)
{
    /* When recovering from a stack overflow, move the task to a while(1) loop. */
    while (1)
    {
        /* Do nothing. */
    }
}
void rm_freertos_port_stack_monitor_example (void)
{
    /* Enable usage fault. */
    SCB->SHCSR |= SCB_SHCSR_USGFAULTENA_Msk;
}
#endif
```

## TrustZone Example

This is an example of calling portALLOCATE\_SECURE\_CONTEXT before calling any non-secure callable functions in a task.

```
void rm_freertos_port_trustzone_task_example (void)
{
    /* When FreeRTOS is used in a non-secure TrustZone application,
portALLOCATE_SECURE_CONTEXT must be called prior
 * to calling any non-secure callable function in a task. The parameter is unused in
the FSP implementation. */
```

```
portALLOCATE_SECURE_CONTEXT(0);
rm_freertos_port_nsc_function();
}
```

## 4.2.79 RTOS Context Management (rm\_tz\_context)

### Modules

RTOS Context Management for RA MCUs.

## Overview

Add this module to a secure TrustZone project to allow the associated non-secure project to use an RTOS. It is used by an RTOS port for RA MCUs (for example, the [FreeRTOS Port \(rm\\_freertos\\_port\)](#), which is automatically added to RA projects when FreeRTOS is selected during project creation).

### Note

*The RTOS Context Management module does not provide any interfaces to the user. To use this module to port an RTOS, consult the Arm documentation at [https://arm-software.github.io/CMSIS\\_5/Core/html/group\\_\\_context\\_\\_trustzone\\_\\_functions.html](https://arm-software.github.io/CMSIS_5/Core/html/group__context__trustzone__functions.html) for further information.*

## Configuration

### Build Time Configurations for rm\_tz\_context

The following build time configurations are defined in fsp\_cfg/rm\_tz\_context\_cfg.h:

Configuration	Options	Default	Description
Process Stack Slots	Value must be a non-negative integer greater than 0	8	The maximum number of threads that can allocate a secure context. For applications using FreeRTOS, the Idle task requires 1 context as well.
Process Stack Size	Value must be a non-negative multiple of 8	256	The maximum stack size of all non-secure callable functions.

### Clock Configuration

This module does not use peripheral clocks.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### TrustZone Integration

When using an RTOS in a TrustZone project, ARM recommends keeping the RTOS in the non-secure project. Tasks may call non-secure callable functions if the task has allocated a secure context. To allocate a secure context, reference the documentation for the RTOS port used. For example, reference [TrustZone Integration](#) when FreeRTOS is used.

### Sealing the Process Stack

This module seals each process stack by placing the value 0xFE5EDA5 above the stack top. For more information, refer to section 3.5 "Sealing a Stack" in "Secure software guidelines for ARMv8-M": <https://developer.arm.com/documentation/100720/0300>.

## 4.2.80 Azure RTOS GUIX Port (rm\_guix\_port)

### Modules

#### Functions

UINT [rm\\_guix\\_port\\_hw\\_initialize](#) (GX\_DISPLAY \*p\_display)

### Detailed Description

## Overview

The Azure RTOS GUIX Port module provides the configuration and hardware acceleration support necessary for use of GUIX on RA products. The port provides full integration with the graphics peripherals (GLCDC, DRW and JPEG).

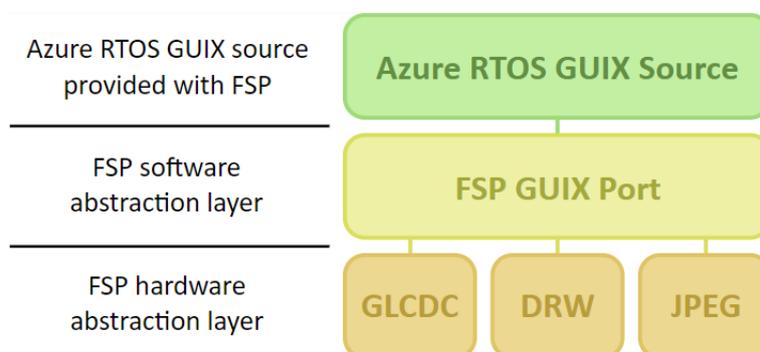


Figure 194: Azure RTOS GUIX Port Block Diagram

*Note*

*This port layer primarily enables hardware acceleration and background handling of many display operations and does not contain code intended to be directly called by the user. For information about how to use GUIX and GUIX Studio (including example code) please consult the [Azure RTOS GUIX documentation](#).*

## Hardware Acceleration

The following functions are currently performed with hardware acceleration:

- DRW Engine ([D/AVE 2D Port Interface \(r\\_drw\)](#))
  - Drawing bitmaps
  - 8, 4 and 1bpp uncompressed and compressed (RLE) font rendering
  - Line and shape drawing
  - Anti-aliased operations
    - Circle stroke and fill
    - Polygon stroke and fill
    - Lines and arcs
- [JPEG Codec \(r\\_jpeg\)](#)
  - JPEG decoding
- [Graphics LCD Controller \(r\\_glcdc\)](#)
  - Brightness, contrast and gamma correction
  - Pixel format conversion (framebuffer to LCD)

## Configuration

### Build Time Configurations for gx

The following build time configurations are defined in fsp\_cfg/azure/gx/gx\_user.h:

Configuration	Options	Default	Description
Hardware Acceleration > JPEG Codec Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Select whether or not to use the JPEG Codec for hardware acceleration.
Hardware Acceleration > DRW Engine Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Select whether or not to use the DRW Engine for hardware acceleration.
Hardware Acceleration > Max DRW Operations	Value must be a positive integer	85	Specifies the maximum number of DRW operations before flushing the display list. Reducing this value may reduce the peak heap used by the application but may reduce performance.
Internal Thread > Stack Size	Value must be greater than zero	4096	GUIX internal thread stack size in bytes. Must be greater than zero.
Internal Thread >	Value must be between	30	Priority of the GUIX

Priority	0 to 31		Internal Thread. The value must be between 0 to 31.
Internal Thread > Time Slice	Value must be a non-negative integer	10	Time Slice value of the GUIX Internal Thread. The value must be between 0 (TX_NO_TIME_SLICE) to 0xFFFFFFFF.
System Timer (ms)	Value must be greater than or equal to 10	20	GUIX system timer period (GX_SYSTEM_TIMER_MS). This value will be internally converted to RTOS ticks and will be rounded down to the next smallest multiple of the RTOS tick period (1000 / TX_TIMER_TICKS_PER_SECOND).
Multithread Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Must be enabled if GUIX functions are called from multiple threads. Set to Disabled when calling GUIX from only one thread to reduce system overhead.
UTF8 Support	<ul style="list-style-type: none"> <li>• Disabled</li> <li>• Enabled</li> </ul>	Enabled	Select whether to enable or disable support for UTF8 characters.
Event Queue Size	Value must be greater than zero	48	Maximum number of events in the GUIX event queue.
Enable GX_WIDGET User Data	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Set to Enabled to use the gx_widget_user_data member in the GX_WIDGET structure.

### Build Time Configurations for rm\_guix\_port

The following build time configurations are defined in fsp\_cfg/middleware/rm\_guix\_port\_cfg.h:

Configuration	Options	Default	Description
DRW Buffer Cache	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enabling this option significantly improves DRW Engine performance. Set to

Disabled only if Display underflow events are triggered under high graphics load.

## Configurations for Azure RTOS > GUIX Port on rm\_guix\_port

This module can be added to the Stacks tab via New Stack > Azure RTOS > GUIX Port on rm\_guix\_port.

Configuration	Options	Default	Description
Display Rotation > Screen Orientation	<ul style="list-style-type: none"> <li>None</li> <li>CW (90 degrees)</li> <li>FLIP (180 degrees)</li> <li>CCW (270 degrees)</li> </ul>	None	Select the display orientation specified in the GUIX Studio project. The Canvas Buffer must be enabled when rotating 180 degrees (FLIP).
Display Rotation > Use Canvas Buffer	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	When screen rotation is set to a value other than 0 a canvas buffer must be used. The canvas buffer size will be the same as a frame buffer for the display module.
Display Rotation > Canvas Buffer Memory Section	This property must be a valid section name	bss	Specify the memory section where the GUIX Canvas Buffer will be allocated.
JPEG Decoding > Work Buffer Size	Must be a valid integer	0xC800	Specify the JPEG work buffer size in bytes. A larger buffer can reduce JPEG decode/draw times. The buffer will not be allocated if JPEG Codec support is disabled.  Unless you are sure of the subsampling used in and the size of the input JPEG images it is recommended to allocate at least 16 framebuffer lines of memory.
JPEG Decoding > Buffer Memory Section	This property must be a valid section name	bss	Specify the memory section where the JPEG Work Buffer will be allocated.

Name	Name must be a valid C symbol	g_rm_guix_port0	Module name.
Target Display Layer	<ul style="list-style-type: none"> <li>Graphics Layer 1</li> <li>Graphics Layer 2</li> </ul>	Graphics Layer 1	Specify which graphics screen to inherit the buffer and display dimensions from.
Callback Function	Must be a valid C symbol	NULL	If a callback function is provided it will be called when Display events occur.

## Hardware Configuration

No clocks or pins are directly required by this module. Please consult the submodules' documentation for their requirements.

## Usage Notes

### Getting Started

To get started with GUIX in an RA project the following must be performed:

1. In e2 studio, open the RA Configuration editor for your GUIX project
2. Select or create a thread
3. Add GUIX to your project in the Stacks view by clicking **New Stack -> Azure RTOS -> GUIX**
4. Ensure the configuration options for GUIX and the port layer are set as necessary for your application
5. Set the properties for the GLCDC module to match the timing and memory requirements of your display panel
6. Set the input color format in the GLCDC module (Input -> Graphics Layer \* -> General -> Color format) and the output color format in the JPEG Codec module if applicable (Decode -> Output color format) per your project specification
7. Click the BSP tab in the configuration editor and confirm the heap size in the Properties pane is sufficient (see Note below)
8. Click Generate Project Content to save and commit configuration changes
9. Drop the Quick Setup entry in Developer Assistance into the desired thread entry C file and update the items marked with TODO as necessary
10. Call the Quick Setup function from the thread entry function (or where desired)

At this point the project is now ready to build and run your GUIX Studio project. Please refer to the documentation for Azure RTOS GUIX and GUIX Studio for details on how to create and edit a GUI application.

#### Note

*It is recommended to start with 8K-32K of heap to begin development. Actual heap use is typically far lower than this but must be characterized by the developer.*

## Using Hardware Acceleration

In most cases there is no need to perform additional configuration to ensure the DRW Engine is used. However, there are some guidelines that should be followed:

- Avoid transparent pixelmaps in 8-bit display mode as they are rendered in software. In particular, ensure PNGs to be used in 8bpp GUIX Studio projects are saved without transparency data if no transparency is needed.
- The following items may require a large heap to draw successfully:
  - Polygons (more sides = more heap)
  - Filled arcs and ellipses (more framebuffer lines occupied = more heap)
  - `gx_canvas_pixelmap_tile` (more tiles = more heap)
- When using hardware acceleration, images used for tile fill of shapes must have dimensions that are a power of 2. This limitation does not apply to `gx_canvas_pixelmap_tile` as well as certain arc/ellipse fill functions as GUIX manually draws pixelmaps to fill these shapes (at the expense of heap space).

## Examples

### Basic Example

This is a basic example demonstrating how to get GUIX up and running given an existing GUIX Studio project. A template for this code is available in Developer Assistance for the GUIX Port module.

*Note*

*GUIX manages the GLCDC, DRW and JPEG Codec submodules internally; they do not need to be opened directly.*

```
GX_WINDOW_ROOT * p_window_root;
void guix_user_start (void)
{
    /* Initialize GUIX */
    gx_system_initialize();

    /* Configure GUIX Studio project main display and get a pointer to the root window
    */
    gx_studio_display_configure(MAIN_DISPLAY,
    rm_guix_port_hw_initialize,
                                MAIN_DISPLAY_LANGUAGE_ENGLISH,
                                MAIN_DISPLAY_THEME,
                                &p_window_root);

    /* Set pointer to the first buffer generated by the configuration
    (rm_guix_port_canvas) */
    gx_canvas_memory_define(p_window_root->gx_window_root_canvas,
                            rm_guix_port_canvas,
                            p_window_root->gx_window_root_canvas->gx_canvas_memory_size);

    /* Create and show the root window in the GUIX Studio project */
```

```

    gx_studio_named_widget_create("root_widget_name", (GX_WIDGET *) p_window_root,
GX_NULL);

    gx_widget_show(p_window_root);

/* Start GUIX */

    gx_system_start();

/* GUIX will continue to run in its own thread */
}

```

## Data Structures

struct [rm\\_guix\\_port\\_callback\\_args\\_t](#)

## Enumerations

enum [rm\\_guix\\_port\\_device\\_t](#)

enum [rm\\_guix\\_port\\_event\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_guix\\_port\\_callback\\_args\\_t](#)

Data Fields		
<a href="#">rm_guix_port_device_t</a>	device	Device code.
<a href="#">rm_guix_port_event_t</a>	event	Event code of the low level hardware.
uint32_t	error	Error code if RM_GUIX_PORT_EVENT_ERROR.

## Enumeration Type Documentation

◆ **rm\_guix\_port\_device\_t**

enum <code>rm_guix_port_device_t</code>	
Low level device code for the GUIX	
Enumerator	
<code>RM_GUIX_PORT_DEVICE_NONE</code>	Non hardware.
<code>RM_GUIX_PORT_DEVICE_DISPLAY</code>	Display device.
<code>RM_GUIX_PORT_DEVICE_DRW</code>	2D Graphics Engine
<code>RM_GUIX_PORT_DEVICE_JPEG</code>	JPEG Codec.

◆ **rm\_guix\_port\_event\_t**

enum <code>rm_guix_port_event_t</code>	
Display event codes	
Enumerator	
<code>RM_GUIX_PORT_EVENT_ERROR</code>	Low level driver error occurs.
<code>RM_GUIX_PORT_EVENT_DISPLAY_VSYNC</code>	Display interface VSYNC.
<code>RM_GUIX_PORT_EVENT_UNDERFLOW</code>	Display interface underflow.

**Function Documentation**

### ◆ rm\_guix\_port\_hw\_initialize()

UINT rm\_guix\_port\_hw\_initialize ( GX\_DISPLAY \* p\_display)

Callback function to be passed to gx\_studio\_display\_configure in order to start hardware modules.

Example:

```
/* Configure GUIX Studio project main display and get a pointer to the root window
*/
gx_studio_display_configure(MAIN_DISPLAY,
rm_guix_port_hw_initialize,
MAIN_DISPLAY_LANGUAGE_ENGLISH,
MAIN_DISPLAY_THEME,
&p_window_root);
```

#### Note

*This function should only be called by GUIX.*

#### Return values

GX_SUCCESS	Device driver setup is successfully done.
GX_FAILURE	Device driver setup failed.

## 4.2.81 HS300X Sensor Middleware (rm\_hs300x)

### Modules

### Functions

**fsp\_err\_t** RM\_HS300X\_Open (rm\_hs300x\_ctrl\_t \*const p\_api\_ctrl, rm\_hs300x\_cfg\_t const \*const p\_cfg)  
Opens and configures the HS300X Middle module. Implements rm\_hs300x\_api\_t::open. [More...](#)

**fsp\_err\_t** RM\_HS300X\_Close (rm\_hs300x\_ctrl\_t \*const p\_api\_ctrl)  
Disables specified HS300X control block. Implements rm\_hs300x\_api\_t::close. [More...](#)

**fsp\_err\_t** RM\_HS300X\_MeasurementStart (rm\_hs300x\_ctrl\_t \*const p\_api\_ctrl)  
This function should be called when start a measurement and when measurement data is stale data. Sends the slave address to the hs300x and start a measurement. Implements rm\_hs300x\_api\_t::measurementStart. [More...](#)

fsp_err_t	<p><a href="#">RM_HS300X_Read</a> (<a href="#">rm_hs300x_ctrl_t</a> *const p_api_ctrl, <a href="#">rm_hs300x_raw_data_t</a> *const p_raw_data)</p> <p>Reads ADC data from HS300X. Implements <a href="#">rm_hs300x_api_t::read</a>. <a href="#">More...</a></p>
fsp_err_t	<p><a href="#">RM_HS300X_DataCalculate</a> (<a href="#">rm_hs300x_ctrl_t</a> *const p_api_ctrl, <a href="#">rm_hs300x_raw_data_t</a> *const p_raw_data, <a href="#">rm_hs300x_data_t</a> *const p_hs300x_data)</p> <p>Calculates humidity [RH] and temperature [Celsius] from ADC data. Implements <a href="#">rm_hs300x_api_t::dataCalculate</a>. <a href="#">More...</a></p>
void	<p><a href="#">rm_hs300x_callback</a> (<a href="#">rm_comms_callback_args_t</a> *p_args)</p> <p>HS300X callback function called in the I2C Communications Middleware callback function. <a href="#">More...</a></p>

## Detailed Description

Middleware to implement the HS300X sensor interface. This module implements the [HS300X Middleware Interface](#).

## Overview

### Features

The HS300X sensor interface implementation has the following key features:

- Starting a measurement at any time
- Getting ADC data from the sensor
- Calculating humidity and temperature value from getting ADC data

## Configuration

### Build Time Configurations for rm\_hs300x

The following build time configurations are defined in `fsp_cfg/rm_hs300x_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Data type	<ul style="list-style-type: none"> <li>• Both humidity and temperature</li> <li>• Humidity only</li> </ul>	Both humidity and temperature	Select Getting humidity only and both humidity and temperature.

## Configurations for Middleware > Sensor > HS300X on rm\_hs300x

This module can be added to the Stacks tab via New Stack > Middleware > Sensor > HS300X on rm\_hs300x.

Configuration	Options	Default	Description
Name	Manual Entry	g_hs300x_sensor0	Module name.
Callback	Name must be a valid C symbol	hs300x_callback	A user callback function can be provided.

### Pin Configuration

This module use SDA and SCL pins of I2C Master and SCI I2C.

## Usage Notes

[HS300x datasheet is here.](#)

If ADC data is valid and calculating humidity and temperature is finished, it is needed to start a measurement again. If ADC data is invalid, it is needed to read ADC data from HS300x again.

## Examples

### Basic Example

This is a basic example of minimal use of HS300X sensor implementation in an application.

```
void rm_hs300x_basic_example (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    rm_hs300x_raw_data_t hs300x_raw_data;
    rm_hs300x_data_t   hs300x_data;
    uint8_t            calcualted_flag = 0;
    /* Open the I2C bus if it is not already open. */
    rm_comms_i2c_bus_extended_cfg_t * p_extend =
        (rm_comms_i2c_bus_extended_cfg_t *) g_hs300x_cfg.p_instance->p_cfg->p_extend;
    i2c_master_instance_t * p_driver_instance = (i2c_master_instance_t *)
p_extend->p_driver_instance;
    p_driver_instance->p_api->open(p_driver_instance->p_ctrl,
p_driver_instance->p_cfg);
    err = RM_HS300X_Open(&g_hs300x_ctrl, &g_hs300x_cfg);
    /* Handle any errors. This function should be defined by the user. */
}
```

```
    handle_error(err);
while (true)
{
    g_flag = 0;
    /* Start Measurement */
    RM_HS300X_MeasurementStart(&g_hs300x_ctrl);
    while (0 == g_flag)
    {
        /* Wait callback */
    }
    /* Wait 4 seconds. See table 4 on the page 6 of the datasheet. */
    R_BSP_SoftwareDelay(4, BSP_DELAY_UNITS_SECONDS);
do
{
    g_flag = 0;
    /* Read ADC Data from HS300X */
    RM_HS300X_Read(&g_hs300x_ctrl, &hs300x_raw_data);
    while (0 == g_flag)
    {
        /* Wait callback */
    }
    /* Calculate Humidity and Temperature values from ADC data */
    err = RM_HS300X_DataCalculate(&g_hs300x_ctrl, &hs300x_raw_data,
&hs300x_data);
    if (FSP_SUCCESS == err)
    {
        calculated_flag = 1;
    }
    else if (FSP_ERR_SENSOR_INVALID_DATA == err)
    {
        calculated_flag = 0;
    }
    else
    {
```

```

    handle_error(err);
    }
    } while (0 == calculated_flag);
}
}

```

## Data Structures

struct [rm\\_hs300x\\_instance\\_ctrl\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_hs300x\\_instance\\_ctrl\\_t](#)

struct <a href="#">rm_hs300x_instance_ctrl_t</a>	
HS300x Control Block	
<b>Data Fields</b>	
<a href="#">uint32_t</a>	<a href="#">open</a>
	Open flag.
<a href="#">rm_hs300x_cfg_t</a> const *	<a href="#">p_cfg</a>
	Pointer to HS300X Configuration.
<a href="#">rm_comms_instance_t</a> const *	<a href="#">p_comms_i2c_instance</a>
	Pointer of I2C Communications Middleware instance structure.
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.

## Function Documentation

◆ **RM\_HS300X\_Open()**

```
fsp_err_t RM_HS300X_Open ( rm_hs300x_ctrl_t *const p_api_ctrl, rm_hs300x_cfg_t const *const p_cfg )
```

Opens and configures the HS300X Middle module. Implements `rm_hs300x_api_t::open`.

Example:

```
err = RM_HS300X_Open(&g_hs300x_ctrl, &g_hs300x_cfg);
```

**Return values**

FSP_SUCCESS	HS300X successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.

◆ **RM\_HS300X\_Close()**

```
fsp_err_t RM_HS300X_Close ( rm_hs300x_ctrl_t *const p_api_ctrl)
```

Disables specified HS300X control block. Implements `rm_hs300x_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_HS300X\_MeasurementStart()**

```
fsp_err_t RM_HS300X_MeasurementStart ( rm_hs300x_ctrl_t *const p_api_ctrl)
```

This function should be called when start a measurement and when measurement data is stale data. Sends the slave address to the hs300x and start a measurement. Implements `rm_hs300x_api_t::measurementStart`.

**Return values**

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_HS300X\_Read()**

```
fsp_err_t RM_HS300X_Read ( rm_hs300x_ctrl_t *const p_api_ctrl, rm_hs300x_raw_data_t *const p_raw_data )
```

Reads ADC data from HS300X. Implements `rm_hs300x_api_t::read`.

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_HS300X\_DataCalculate()**

```
fsp_err_t RM_HS300X_DataCalculate ( rm_hs300x_ctrl_t *const p_api_ctrl, rm_hs300x_raw_data_t *const p_raw_data, rm_hs300x_data_t *const p_hs300x_data )
```

Calculates humidity [RH] and temperature [Celsius] from ADC data. Implements `rm_hs300x_api_t::dataCalculate`.

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_SENSOR_INVALID_DATA	Data is invalid.

◆ **rm\_hs300x\_callback()**

```
void rm_hs300x_callback ( rm_comms_callback_args_t * p_args)
```

HS300X callback function called in the I2C Communications Middleware callback function.

(end addtogroup HS300X)

**4.2.82 Azure RTOS LevelX NOR SPI Driver (rm\_levelx\_nor\_spi)**

## Modules

**Functions**

`fsp_err_t RM_LEVELX_NOR_SPI_Open (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, rm_levelx_nor_spi_cfg_t const *const p_cfg)`

Initializes LevelX NOR SPI port read/write and control. [More...](#)

`fsp_err_t RM_LEVELX_NOR_SPI_Read (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG *const p_flash_addr, ULONG *const p_dest, ULONG word_count)`

LevelX NOR driver "read sector" service. [More...](#)

`fsp_err_t RM_LEVELX_NOR_SPI_Write (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG *const p_flash_addr, ULONG *const p_src, ULONG word_count)`

LevelX NOR driver "write sector" service. [More...](#)

`fsp_err_t RM_LEVELX_NOR_SPI_BlockErase (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG block, ULONG erase_count)`

LevelX NOR driver "block erase" service. [More...](#)

`fsp_err_t RM_LEVELX_NOR_SPI_BlockErasedVerify (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG block)`

LevelX NOR driver "block erased verify" service. [More...](#)

`fsp_err_t RM_LEVELX_NOR_SPI_Close (rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl)`

LevelX NOR driver close service. [More...](#)

## Detailed Description

Middleware for using Azure RTOS LevelX on NOR SPI memory.

## Overview

This module provides the hardware port layer for LevelX on NOR SPI flash memory. Setup for this module is done solely through calling LevelX APIs. Please refer to the LevelX API reference: <https://docs.microsoft.com/en-us/azure/rtos/levelx/>

## Configuration

### Build Time Configurations for `rm_levelx_nor_spi`

The following build time configurations are defined in `fsp_cfg/middleware/rm_levelx_nor_spi_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	Selects if code for parameter checking is to be included in the build.
Write Verify	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	When enabled reads back data written to SPI memory in order to verify it.
Page Buffer Size (bytes)	Size should be greater than zero	256	When direct read is enabled in LevelX a situation can occur where the driver has to write to SPI memory with the source location also being within the SPI memory address range. In this situation the driver needs a buffer that is at least the same size as a page in order to temporarily store data to write out.

### Configurations for Middleware > Storage > LevelX NOR Port on rm\_levelx\_nor\_spi

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_levelx_nor_spi0	Module name.
Memory Start Address Offset (bytes)	Offset should be greater than or equal to zero	0	Enter the starting offset to use in the SPI memory. The starting address for LevelX memory will be the SPI memory base address plus this offset.
Memory Size (bytes)	Size should be greater than zero	33554432	Enter the size that the LevelX Memory should be. This can be smaller than the SPI memory size in order to use a subset of SPI memory.
Poll Status Count	Poll Status Count should be greater than or equal to zero	0xFFFFFFFF	Number of times to poll for operation complete status for blocking memory operations.

### Build Time Configurations for lx

The following build time configurations are defined in fsp\_cfg/azure/lx/lx\_user.h:

Configuration	Options	Default	Description
NOR > Direct Read	<ul style="list-style-type: none"> <li>Enabled (default)</li> <li>Disabled</li> </ul>	Enabled (default)	When enabled, this option bypasses the NOR flash driver read routine in favor of reading the NOR memory directly, resulting in a significant performance increase.
NOR > Free Sector Data Verify	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled (default)</li> </ul>	Disabled (default)	When enabled, this causes the LevelX NOR instance open logic to verify free NOR sectors are all ones.
NOR > Extended Cache	<ul style="list-style-type: none"> <li>Enabled (default)</li> <li>Disabled</li> </ul>	Enabled (default)	Enables the extended NOR cache.
NOR > Extended Cache Size	Manual Entry		If not set this value defaults to 8, which represents a maximum of 8 sectors that can be cached in a NOR instance.
NOR > Sector Mapping Cache Size	Value must be greater than or equal to 8 and a power of 2, or empty		If not set this value defaults to 16 and defines the logical sector mapping cache size. Large values improve performance, but cost memory. The minimum size is 8 and all values must be a power of 2.
NAND > Sector Mapping Cache Size	Value must be greater than or equal to 8 and a power of 2, or empty		If not set this value defaults to 128 and defines the logical sector mapping cache size. Large values improve performance, but cost memory. The minimum size is 8 and all values must be a power of 2.
NAND > Flash Direct Mapping Cache	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled (default)</li> </ul>	Disabled (default)	When enabled, this creates a direct mapping cache, such that there are no cache

misses. It also required that LX\_NAND\_SECTOR\_MAPPING\_CACHE\_SIZE represents the exact number of total pages in your flash device.

Thread Safe	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, this makes LevelX thread-safe by using a ThreadX mutex object throughout the API.
Standalone Mode	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled (default)</li> </ul>	Disabled (default)	When enabled, allows LevelX to be used in standalone mode (without Azure RTOS).

## Usage Notes

### Pending during Erase/Write

The LevelX NOR SPI driver is blocking on all SPI operations and will poll device status for operation completion on Writes and Erases. A callback can be provided by the user to wait with an OS-specific thread wait in these instances.

### Closing the driver

When lx\_nor\_flash\_close is called to close the LevelX instance it does not call any services within the LevelX NOR SPI driver to close out the driver instance. The user should call the generated close function (i.e. g\_rm\_levelx\_nor\_spi0\_close) in order to close out the driver instance.

### Erasing Flash Memory Prior to Usage

The area of the flash memory being used for the LevelX instance should be erased using the lower level flash API prior to usage. Otherwise, LevelX API may fail on lx\_nor\_flash\_open due to any areas in flash memory that have been written/set.

## Examples

### Basic Example

This is a basic example of using the LevelX NOR SPI driver with the LevelX API in an application.

```
#define RM_LEVELX_NOR_SPI_EXAMPLE_SECTOR_SIZE (512)
#define RM_LEVELX_NOR_SPI_EXAMPLE_BUFFER_FILL_VALUE (0xA5)
#define RM_LEVELX_NOR_SPI_EXAMPLE_SPI_SECTOR_SIZE (4096)
extern rm_levelx_nor_spi_instance_ctrl_t g_levelx_nor_spi0_ctrl;
extern rm_levelx_nor_spi_cfg_t g_levelx_nor_spi0_cfg;
extern LX_NOR_FLASH g_lx_nor_flash0;
```

```
void rm_levelx_nor_spi_example (void)
{
    uint8_t          read_buffer[RM_LEVELX_NOR_SPI_EXAMPLE_SECTOR_SIZE];
    uint8_t          write_buffer[RM_LEVELX_NOR_SPI_EXAMPLE_SECTOR_SIZE];
    spi_flash_instance_t * p_spi_flash_instance = (spi_flash_instance_t *)
g_levelx_nor_spi0_cfg.p_lower_lvl;
    spi_flash_status_t status;

    memset(write_buffer, RM_LEVELX_NOR_SPI_EXAMPLE_BUFFER_FILL_VALUE, sizeof
(write_buffer));

    /* Erase flash prior to usage */
    fsp_err_t err = p_spi_flash_instance->p_api->open(p_spi_flash_instance->p_ctrl,
p_spi_flash_instance->p_cfg);
    assert(FSP_SUCCESS == err);
    for (uint32_t i = g_levelx_nor_spi0_cfg.address_offset;
        i < g_levelx_nor_spi0_cfg.size;
        i += RM_LEVELX_NOR_SPI_EXAMPLE_SPI_SECTOR_SIZE)
    {
        err = p_spi_flash_instance->p_api->erase(p_spi_flash_instance->p_ctrl,
                                                (uint8_t *)
g_levelx_nor_spi0_cfg.base_address + i,
RM_LEVELX_NOR_SPI_EXAMPLE_SPI_SECTOR_SIZE);
        assert(FSP_SUCCESS == err);
        status.write_in_progress = true;
        while (status.write_in_progress)
        {
            err =
p_spi_flash_instance->p_api->statusGet(p_spi_flash_instance->p_ctrl, &status);
            assert(FSP_SUCCESS == err);
        }
    }
    err = p_spi_flash_instance->p_api->close(p_spi_flash_instance->p_ctrl);
    assert(FSP_SUCCESS == err);
    /* Initialize LevelX */
}
```

```

lx_nor_flash_initialize();

UINT lx_err = lx_nor_flash_open(&g_lx_nor_flash0, "LX_NOR_SPI_EXAMPLE",
g_levelx_nor_spi0_initialize);

handle_lx_error(lx_err);

/* Write test value to sector 0 then read back to verify */
lx_err = lx_nor_flash_sector_write(&g_lx_nor_flash0, 0, write_buffer);
handle_lx_error(lx_err);

lx_err = lx_nor_flash_sector_read(&g_lx_nor_flash0, 0, read_buffer);
handle_lx_error(lx_err);

assert(0 == memcmp(read_buffer, write_buffer, sizeof(read_buffer)));
}

```

## Callback Wait Example

This shows how to use the LevelX NOR SPI driver callback with ThreadX in order to wait for operations to complete.

```

/* Callback called by LevelX NOR SPI driver needs to wait on operation. */
void rm_levelx_nor_spi_callback_wait_example (rm_levelx_nor_spi_callback_args_t *
p_args)
{
    if (p_args->event & RM_LEVELX_NOR_SPI_EVENT_BUSY)
    {
        /* Put the thread to sleep while waiting for operation to complete. */
        tx_thread_sleep(1);
    }
}

```

## Data Structures

struct [rm\\_levelx\\_nor\\_spi\\_callback\\_args\\_t](#)

struct [rm\\_levelx\\_nor\\_spi\\_cfg\\_t](#)

struct [rm\\_levelx\\_nor\\_spi\\_instance\\_ctrl\\_t](#)

## Enumerations

enum [rm\\_levelx\\_nor\\_spi\\_event\\_t](#)

## Data Structure Documentation

### ◆ rm\_levelx\_nor\_spi\_callback\_args\_t

struct rm_levelx_nor_spi_callback_args_t		
RM_LEVELX_NOR_SPI callback arguments definitions		
Data Fields		
rm_levelx_nor_spi_event_t	event	LevelX NOR driver callback event.
void const *	p_context	Placeholder for user data.

### ◆ rm\_levelx\_nor\_spi\_cfg\_t

struct rm_levelx_nor_spi_cfg_t	
SF_EL_LX_NOR Config Block Type	
<b>Data Fields</b>	
spi_flash_instance_t const *	p_lower_lvl
	Lower level memory pointer.
LX_NOR_FLASH *	p_lx_nor_flash
	Pointer to the LevelX nor flash instance.
uint32_t	base_address
	Base address of memory mapped region.
uint32_t	address_offset
	Offset to use subset of available flash size if desired.
uint32_t	size
	Size of the partitioned region.
uint32_t	poll_status_count
	Number of times to poll for operation complete status before returning an error.

void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to the user callback.
void(*	<a href="#">p_callback</a> )(rm_levelx_nor_spi_callback_args_t *p_args)
	Callback function.

#### ◆ [rm\\_levelx\\_nor\\_spi\\_instance\\_ctrl\\_t](#)

struct <a href="#">rm_levelx_nor_spi_instance_ctrl_t</a>		
SF_EL_LX_NOR Control Block Type		
Data Fields		
<a href="#">rm_levelx_nor_spi_cfg_t</a> const *	<a href="#">p_cfg</a>	Pointer to instance configuration.
uint32_t	<a href="#">start_address</a>	Start address of partition to use within memory mapped region.
uint32_t	<a href="#">minimum_erase_size</a>	Minimum erase size of SPI memory.
uint8_t	<a href="#">page_buffer</a> [RM_LEVELX_NOR_S PI_CFG_BUFFER_SIZE]	Page buffer for situations when writing to SPI memory from a source within SPI memory.
uint32_t	<a href="#">open</a>	Used to determine if module is initialized.

### Enumeration Type Documentation

#### ◆ [rm\\_levelx\\_nor\\_spi\\_event\\_t](#)

enum <a href="#">rm_levelx_nor_spi_event_t</a>	
Common macro for FSP header files. There is also a corresponding FSP_FOOTER macro at the end of this file. Options for the callback events.	
Enumerator	
RM_LEVELX_NOR_SPI_EVENT_BUSY	Pending operation, user can define their own wait functionality.

### Function Documentation

◆ **RM\_LEVELX\_NOR\_SPI\_Open()**

```
fsp_err_t RM_LEVELX_NOR_SPI_Open ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl,
rm_levelx_nor_spi_cfg_t const *const p_cfg )
```

Initializes LevelX NOR SPI port read/write and control.

Calls lower level SPI memory functions.

**Parameters**

[in,out]	p_ctrl	Control block for the LevelX NOR SPI instance.
[in,out]	p_cfg	Configuration for LevelX NOR SPI port.

**Return values**

FSP_SUCCESS	LevelX NOR driver is successfully opened.
FSP_ERR_ASSERTION	p_ctrl or p_cfg is NULL.
FSP_ERR_ALREADY_OPEN	Driver is already in OPEN state.

**Returns**

See Common\_Error\_Codes or lower level drivers for other possible return codes. This function calls

- spi\_flash\_api\_t:open

◆ **RM\_LEVELX\_NOR\_SPI\_Read()**

```
fsp_err_t RM_LEVELX_NOR_SPI_Read ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG
*const p_flash_addr, ULONG *const p_dest, ULONG word_count )
```

LevelX NOR driver "read sector" service.

This is responsible for reading a specific sector in a specific block of the NOR flash. All error checking and correcting logic is the responsibility of this service.

**Parameters**

[in]	p_ctrl	Control block for the LevelX NOR SPI instance.
[in]	p_flash_addr	Specifies the address of a logical sector within a NOR flash block of memory.
[in,out]	p_dest	Specifies where to place the sector contents.
[in]	word_count	Specifies how many 32-bit words to read.

**Return values**

FSP_SUCCESS	LevelX NOR flash sector read successful.
FSP_ERR_ASSERTION	p_ctrl, p_flash_addr or p_dest is NULL.
FSP_ERR_NOT_OPEN	Driver not in OPEN state for reading.

**Returns**

See `Common_Error_Codes` or lower level drivers for other possible return codes.

### ◆ RM\_LEVELX\_NOR\_SPI\_Write()

```
fsp_err_t RM_LEVELX_NOR_SPI_Write ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl, ULONG
*const p_flash_addr, ULONG *const p_src, ULONG word_count )
```

LevelX NOR driver "write sector" service.

This is responsible for writing a specific sector into a block of the NOR flash. All error checking is the responsibility of the this service.

#### Parameters

[in]	p_ctrl	Control block for the LevelX NOR SPI instance.
[in,out]	p_flash_addr	Specifies the address of a logical sector within a NOR flash block of memory.
[in]	p_src	Specifies the source of the write.
[in]	word_count	Specifies how many 32-bit words to write.

#### Return values

FSP_SUCCESS	LevelX NOR flash sector write successful.
FSP_ERR_ASSERTION	p_ctrl, p_flash_addr or p_src is NULL.
FSP_ERR_NOT_OPEN	Driver not in OPEN state for writing.
FSP_ERR_TIMEOUT	Timeout occurred while waiting for operation to complete.
FSP_ERR_WRITE_FAILED	Verification of Write operation failed.
FSP_ERR_INVALID_ADDRESS	Write address or size falls outside of flash memory range.

#### Returns

See Common\_Error\_Codes or lower level drivers for other possible return codes. This function calls

- [spi\\_flash\\_api\\_t:write](#)

### ◆ RM\_LEVELX\_NOR\_SPI\_BlockErase()

```
fsp_err_t RM_LEVELX_NOR_SPI_BlockErase ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl,
ULONG block, ULONG erase_count )
```

LevelX NOR driver "block erase" service.

This is responsible for erasing the specified block of the NOR flash.

#### Parameters

[in]	p_ctrl	Control block for the LevelX NOR SPI instance.
[in]	block	Specifies which NOR block to erase.
[in]	erase_count	Provided for diagnostic purposes(currently unused).

#### Return values

FSP_SUCCESS	LevelX NOR flash block erase successful.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver not in OPEN state for erasing.
FSP_ERR_TIMEOUT	Timeout occurred while waiting for operation to complete.

#### Returns

See Common\_Error\_Codes or lower level drivers for other possible return codes. This function calls

- spi\_flash\_api\_t:erase

◆ **RM\_LEVELX\_NOR\_SPI\_BlockErasedVerify()**

```
fsp_err_t RM_LEVELX_NOR_SPI_BlockErasedVerify ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl,
ULONG block )
```

LevelX NOR driver "block erased verify" service.

This is responsible for verifying the specified block of the NOR flash is erased.

**Parameters**

[in]	p_ctrl	Control block for the LevelX NOR SPI instance.
[in]	block	Specifies which block to verify that it is erased.

**Return values**

FSP_SUCCESS	LevelX flash block erase verification successful.
FSP_ERR_ASSERTION	p_ctrl or lower level driver is NULL.
FSP_ERR_NOT_OPEN	Driver not in OPEN state for verifying.
FSP_ERR_NOT_ERASED	The block is not erased properly.

**Returns**

See `Common_Error_Codes` or lower level drivers for other possible return codes.

◆ **RM\_LEVELX\_NOR\_SPI\_Close()**

```
fsp_err_t RM_LEVELX_NOR_SPI_Close ( rm_levelx_nor_spi_instance_ctrl_t *const p_ctrl)
```

LevelX NOR driver close service.

This is responsible for closing the driver properly.

**Parameters**

[in]	p_ctrl	Control block for the LevelX NOR SPI instance.
------	--------	--

**Return values**

FSP_SUCCESS	LevelX flash is available and is now open for read, write, and control access.
FSP_ERR_ASSERTION	p_ctrl is NULL.
FSP_ERR_NOT_OPEN	Driver not in OPEN state for closing.

**Returns**

See `Common_Error_Codes` or lower level drivers for other possible return codes. This function calls

- `spi_flash_api_t:close`

## 4.2.83 LittleFS Flash Port (rm\_littlefs\_flash)

### Modules

#### Functions

```
fsp_err_t RM_LITTLEFS_FLASH_Open (rm_littlefs_ctrl_t *const p_ctrl,
    rm_littlefs_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_LITTLEFS_FLASH_Close (rm_littlefs_ctrl_t *const p_ctrl)
```

#### Detailed Description

Middleware for the LittleFS File System control on RA MCUs.

## Overview

This module provides the hardware port layer for the LittleFS file system. After initializing this module, refer to the LittleFS documentation to use the file system:

<https://github.com/ARMmbed/littlefs>

## Configuration

### Build Time Configurations for rm\_littlefs\_flash

The following build time configurations are defined in fsp\_cfg/rm\_littlefs\_flash\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > LittleFS on Flash

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_rm_littlefs0	Module name.
Read Size	Must be a non-negative integer	1	Minimum size of a block read. All read operations will be a multiple of this value.
Program Size	Must be a non-negative integer	4	Minimum size of a block program. All program operations will be a multiple of this value.

Block Size (bytes)	Must be a multiple of 64	128	Size of an erasable block. This does not impact RAM consumption and may be larger than the physical erase size. However, non-inlined files take up at minimum one block. Must be a multiple of the read and program sizes.
Block Count	Manual Entry	(BSP_DATA_FLASH_SIZE_BYTES/128)	Number of erasable blocks on the device.
Block Cycles	Must be an integer	1024	Number of erase cycles before LittleFS evicts metadata logs and moves the metadata to another block. Suggested values are in the range 100-1000, with large values having better performance at the cost of less consistent wear distribution. Set to -1 to disable block-level wear-leveling.
Cache Size	Must be a non-negative integer	64	Size of block caches. Each cache buffers a portion of a block in RAM. The LittleFS needs a read cache, a program cache, and one additional cache per file. Larger caches can improve performance by storing more data and reducing the number of disk accesses. Must be a multiple of the read and program sizes, and a factor of the block size.
Lookahead Size	Must be a non-negative multiple of 8	16	Size of the lookahead buffer in bytes. A larger lookahead buffer increases the number of blocks found during an allocation pass. The lookahead buffer is

stored as a compact bitmap, so each byte of RAM can track 8 blocks. Must be a multiple of 8.

## Common LittleFS Configuration

### Build Time Configurations for LittleFS

The following build time configurations are defined in arm/littlefs/lfs\_util.h:

Configuration	Options	Default	Description
Custom lfs_util.h	Manual Entry		Add a path to your custom lfs_util.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
Thread Safe	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enables thread safety in LittleFS.
Use Malloc	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures the use of malloc by LittleFS.
Use Assert	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures the use of assert by LittleFS.
Debug Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configures debug messages.
Warning Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configures warning messages.
Error Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configures error messages.
Trace Messages	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Configures trace messages.
Intrinsics	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Configures intrinsic functions such as <code>__builtin_clz</code> .
Instance Name for STDIO wrapper	Name must be a valid C symbol	g_rm_littlefs0	The rm_littlefs instance name to use with the STDIO wrapper.

## Usage Notes

### Blocking Read/Write/Erase

The LittleFS port blocks on Read/Write/Erase calls until the operation has completed.

## Memory Constraints

The block size defined in the LittleFS configuration must be a multiple of the data flash erase size of the MCU. It must be greater than 104bytes which is the minimum block size of a LittleFS block. For information about data flash erase sizes refer to the "Specifications of the code flash memory and data flash memory" table of the "Flash Memory" chapter's "Overview" section.

## Limitations

This module is not thread safe.

## Examples

### Basic Example

This is a basic example of LittleFS on Flash in an application.

```
extern const rm_littlefs_cfg_t g_rm_littlefs_flash0_cfg;
#ifdef LFS_NO_MALLOC
static uint8_t g_file_buffer[LFS_CACHE_SIZE];
static struct lfs_file_config g_file_cfg =
{
    .buffer = g_file_buffer
};
#endif
void rm_littlefs_example (void)
{
    uint8_t    buffer[30];
    lfs_file_t file;
    /* Open LittleFS Flash port.*/
    fsp_err_t err = RM_LITTLEFS_FLASH_Open(&g_rm_littlefs_flash0_ctrl,
&g_rm_littlefs_flash0_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    /* Format the filesystem. */
    int lfs_err = lfs_format(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
    handle_lfs_error(lfs_err);
    /* Mount the filesystem. */
    lfs_err = lfs_mount(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
    handle_lfs_error(lfs_err);
}
```

```
/* Create a breakfast directory. */
    lfs_err = lfs_mkdir(&g_rm_littlefs_flash0_lfs, "breakfast");
    handle_lfs_error(lfs_err);

/* Create a file toast in the breakfast directory. */
const char * path = "breakfast/toast";
#ifdef LFS_NO_MALLOC
/*****
*****
* By default LittleFS uses malloc to allocate buffers. This can be disabled in the
RA Configuration editor.
* Buffers will be generated from the configuration for the read, program and
lookahead buffers.
* When opening a file a unique buffer must be passed in for use as a file buffer.
* The buffer size must be equal to the cache size.
*****
*****/
    lfs_err = lfs_file_opencfg(&g_rm_littlefs_flash0_lfs,
                              &file,
                              path,
                              LFS_O_WRONLY | LFS_O_CREAT | LFS_O_APPEND,
                              &g_file_cfg);

    handle_lfs_error(lfs_err);
#else
    lfs_err = lfs_file_open(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_WRONLY |
LFS_O_CREAT | LFS_O_APPEND);
    handle_lfs_error(lfs_err);
#endif
const char * contents = "butter";
    lfs_size_t len = strlen(contents);
/* Apply butter to toast 10 times. */
for (uint32_t i = 0; i < 10; i++)
{
    lfs_err = lfs_file_write(&g_rm_littlefs_flash0_lfs, &file, contents, len);
    if (lfs_err < 0)
```

```
    {
        handle_lfs_error(lfs_err);
    }
}

/* Close the file. */
lfs_err = lfs_file_close(&g_rm_littlefs_flash0_lfs, &file);
handle_lfs_error(lfs_err);

/* Unmount the filesystem. */
lfs_err = lfs_unmount(&g_rm_littlefs_flash0_lfs);
handle_lfs_error(lfs_err);

/* Remount the filesystem. */
lfs_err = lfs_mount(&g_rm_littlefs_flash0_lfs, &g_rm_littlefs_flash0_lfs_cfg);
handle_lfs_error(lfs_err);

/* Open breakfast/toast. */
#ifdef LFS_NO_MALLOC
    lfs_err = lfs_file_opencfg(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_RDONLY,
&g_file_cfg);
    handle_lfs_error(lfs_err);
#else
    lfs_err = lfs_file_open(&g_rm_littlefs_flash0_lfs, &file, path, LFS_O_RDONLY);
    handle_lfs_error(lfs_err);
#endif
    handle_lfs_error(lfs_err);

/* Verify the toast is buttered the correct amount. */
for (uint32_t i = 0; i < 10; i++)
    {
        lfs_err = lfs_file_read(&g_rm_littlefs_flash0_lfs, &file, buffer, len);
        if (lfs_err < 0)
            {
                handle_lfs_error(lfs_err);
            }
        assert(0 == memcmp(buffer, contents, len));
    }

/* Close the file. */
```

```

lfs_err = lfs_file_close(&g_rm_littlefs_flash0_lfs, &file);

handle_lfs_error(lfs_err);

}

```

## Function Documentation

### ◆ RM\_LITTLEFS\_FLASH\_Open()

`fsp_err_t RM_LITTLEFS_FLASH_Open ( rm_littlefs_ctrl_t *const p_ctrl, rm_littlefs_cfg_t const *const p_cfg )`

Opens the driver and initializes lower layer driver.

Implements `rm_littlefs_api_t::open()`.

#### Return values

FSP_SUCCESS	Success.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_INVALID_SIZE	The provided block size is invalid.
FSP_ERR_INVALID_ARGUMENT	Flash BGO mode must be disabled.
FSP_ERR_INTERNAL	Failed to create the semaphore.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `flash_api_t::open`

### ◆ RM\_LITTLEFS\_FLASH\_Close()

`fsp_err_t RM_LITTLEFS_FLASH_Close ( rm_littlefs_ctrl_t *const p_ctrl)`

Closes the lower level driver.

Implements `rm_littlefs_api_t::close()`.

#### Return values

FSP_SUCCESS	Media device closed.
FSP_ERR_ASSERTION	An input parameter was invalid.
FSP_ERR_NOT_OPEN	Module not open.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- `flash_api_t::close`

## 4.2.84 MCUboot Port (rm\_mcuboot\_port)

### Modules

MCUboot Port for RA MCUs.

## Overview

### Note

*The MCUboot Port does not provide any interfaces to the user. Consult the MCUboot documentation at <https://mcu-tools.github.io/mcuboot/> for further information.*

## Configuration

### Build Time Configurations for MCUboot

The following build time configurations are defined in mcu-tools/include/mcuboot\_config/mcuboot\_config.h:

Configuration	Options	Default	Description
General > Custom mcuboot_config.h	Manual Entry		Add a path to your custom mcuboot_config.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
General > Upgrade Mode	<ul style="list-style-type: none"> <li>Swap</li> <li>Overwrite Only</li> <li>Overwrite Only Fast</li> </ul>	Overwrite Only	Swap supports A/B image swapping with rollback. Other modes with simpler code path, which only supports overwriting the existing image with the update image or running the newest image directly from its flash partition, are also available.
General > Validate Primary Image	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Enabled	Always check the signature of the image in the primary slot before booting, even if no upgrade was performed. This is recommended if the

General > Downgrade Prevention (Overwrite Only)	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	boot time penalty is acceptable.
General > Number of Images Per Application	<ul style="list-style-type: none"> <li>• 1</li> <li>• 2 (TrustZone)</li> </ul>	1	Prevent downgrades by enforcing incrementing version numbers. When this option is set, any upgrade must have greater major version or greater minor version with equal major version. This mechanism only protects against some attacks against version downgrades (for example, a JTAG could be used to write an older version).
General > Watchdog Feed	Manual Entry		Number of separately updateable images.
General > Measured Boot	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	This function might be implemented if the OS / HW watchdog is enabled while doing a swap upgrade and the time it takes for a swapping is long enough to cause an unwanted reset. If implementing this, the OS main.c must also enable the watchdog (if required)!
General > Data Sharing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Copies the boot data into the secure RAM, intended to be used by the secure App.
General > Data Sharing	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Copies the user data into the secure RAM, intended to be used by the secure App.
Signing Options > TrustZone > Boot Record (Image 2)	String length must be 12 characters or less.		Create CBOR encoded boot record TLV for Image 2. Represents the role of the software component (e.g. CoFM for coprocessor firmware). [max. 12 characters]
Signing Options > TrustZone > Custom	Manual Entry	--confirm	Add any custom options to pass to

(Image 2)

imgtool.py here. --pad places a trailer on the image that indicates that the image should be considered an upgrade. Writing this image in the secondary slot will then cause the bootloader to upgrade to it. --confirm marks the image as confirmed, which causes the upgrade to be permanent.

Signing Options >  
Signature Type

- None
- ECDSA P-256
- RSA 2048
- RSA 3072

ECDSA P-256

Configure the signature type.

Signing Options > Boot  
Record

String length must be 12 characters or less.

Create CBOR encoded boot record TLV. Represents the role of the software component (e.g. CoFM for coprocessor firmware). [max. 12 characters]

Signing Options >  
Custom

Manual Entry

--confirm

Add any custom options to pass to imgtool.py here. --pad places a trailer on the image that indicates that the image should be considered an upgrade. Writing this image in the secondary slot will then cause the bootloader to upgrade to it. --confirm marks the image as confirmed, which causes the upgrade to be permanent.

Debugging > Log Level

- Off
- Error
- Warning
- Info
- Debug

Off

Configure log level.

Flash Layout >  
TrustZone > Non-Secure Callable Region Size (Bytes)

Value must be an integer multiple of the 1024.

0x0

Size of the Non-Secure Callable region of the Secure image.

Flash Layout > TrustZone > Non-Secure Flash Area Size (Bytes) (TrustZone Non-Secure)	Value must be an integer multiple of the largest erase size on the mcu.	0x0	Size of the Non-Secure region. This must be non-zero for all TrustZone projects to ensure memory is partitioned correctly, even if the Secure and Non-Secure regions are treated as a single image. If the Non-Secure region can be updated separately, this size must account for the header and trailer.
Flash Layout > TrustZone > Non-Secure Callable RAM Region Size (Bytes)	Value must be an integer multiple of the 1024.	0x0	Size of the Non-Secure Callable RAM region of the Secure image.
Flash Layout > TrustZone > Non-Secure RAM Region Size (Bytes) (TrustZone Non-Secure)	Value must be an integer multiple of the 8192.	0x0	Size of the Non-Secure RAM region. This must be non-zero for all TrustZone projects to ensure memory is partitioned correctly, even if the Secure and Non-Secure regions are treated as a single image.
Flash Layout > TrustZone > Image 2 Header Size (Bytes)	Value must be an integer multiple of 0x80 (alignment required by VTOR).	0x80	Size of the flash reserved for the application image header for Image 2.
Flash Layout > Bootloader Flash Area Size (Bytes)	Value must be an integer multiple of the largest erase size on the mcu.	0x20000	Size of the flash reserved for the bootloader.
Flash Layout > Image 1 Header Size (Bytes)	Value must be an integer multiple of 0x80 (alignment required by VTOR).	0x80	Size of the flash reserved for the application image header.
Flash Layout > Image 1 Flash Area Size (Bytes)	Value must be an integer multiple of the largest erase size on the mcu.	0x20000	Size of the application image 1, including the header and trailer. For TrustZone projects, enter the combined size of the Secure and Non-Secure Callable regions if the Non-Secure image can be updated separately, or

enter the size of the entire image slot if Secure, Non-Secure Callable, and Non-Secure regions are updated as a single image.

Size of the scratch area. Only required for swap update method.

Maximum size of the boot record.

Size of the shared RAM area. Required for Measured Boot.

Shared RAM start address. Required for Measured Boot.

Flash Layout > Scratch Flash Area Size (Bytes)	Value must be an integer multiple of the largest erase size on the mcu.	0x0
Data Sharing > Maximum Measured Boot Record Size (Bytes)	Value must be an integer.	0x64
Data Sharing > Shared Data Size (Bytes)	Value must be an integer.	0x380
Data Sharing > Shared Data Address	Value must be an integer	0x20000000

## Clock Configuration

This module does not use peripheral clocks.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Getting Started: Creating an MCUboot Project

Start by creating a new project in e2 studio or RA SC. If the MCU supports TrustZone, select a Flat project. The bootloader resides entirely in Secure memory, but it is considered a flat project because it does not provide any Non-Secure Callable functions. On the Stacks tab, add New > Bootloader > MCUboot. Resolve any constraint errors and edit configurations as desired. Add either the example keys or generate your own key. The MCUboot key generation tool is provided at ra/mcu-tools/MCUboot/scripts/imgtool.py and documented at <https://github.com/mcu-tools/mcuboot/blob/master/docs/imgtool.md>. Install the following required python packages to use imgtool.py: <https://github.com/mcu-tools/mcuboot/blob/master/scripts/requirements.txt>.

In src/hal\_entry.c, drag in Developer Assistance > HAL/Common > MCUboot > Quick Setup > Call Quick Setup. Add a call to mcuboot\_quick\_setup() in the application and make any desired updates.

*Note*

*MCUboot will contain either the verification public key or its hash. During production it is necessary to permanently lock the flash region where MCUboot is programmed to prevent the keys or the code from being modified.*

## Getting Started: Signing Tool Prerequisite

To use the MCUboot signing tool, ensure you have Python 3.x installed on your system. Then install the Python packages required for the signing tool with the following command:

```
pip3 install --user -r ra/mcu-tools/MCUboot/scripts/requirements.txt
```

### Getting Started: Converting a Project to an MCUboot Image

MCUboot application images must execute from the image slot defined by the MCUboot project. They are also limited to a single downloadable flash region. All of this is handled by specifying a `BootloaderDataFile` in the FSP Configuration tool.

Any existing project can be converted to an MCUboot image.

1. If the project was created with a version prior to FSP v3.0.0, update the linker script to the v3.0.0 version before using it as an MCUboot application image.
2. Right click the project to convert in e2 studio or RA SC and select Properties.
3. Open C/C++ Build and select Build Variables.
4. Click Add...
5. For Variable Name, enter `BootloaderDataFile`. For Type, select File. Browse to the \*.bld file created alongside the \*.elf file for the associated MCUboot project.
6. Click OK, then Apply and Close.

To convert a TrustZone image, follow the steps above for both the Secure project and the Non-Secure project.

MCUboot application images must also be signed to work with MCUboot. At a minimum, this involves adding a SHA and MCUboot specific constant data called boot magic in the image trailer.

A template to get started with signing based on the properties specified in the MCUboot stack is output in a comment at the top of `ra_cfg/mcu-tools/include/mcuboot_config/mcuboot_config.h`.

Signing can be done on the command line after building or as a post-build step in e2 studio. To sign the image as a post-build step:

1. Update the paths as documented in the signing comment in `ra_cfg/mcu-tools/include/mcuboot_config/mcuboot_config.h`.
2. Join the two commands (`arm-none-eabi-objcopy` and `python`) with `' & '` on Windows or `' ; '` on Linux.
3. Copy the single line command to Project > Properties, C/C++ Build > Settings, Build Steps (tab), Post-build steps, Command(s).
4. The signed image is output next to the application `<project>.elf` file with a default name of `<project>_signed.bin`.

### Getting Started: Download and Debug

For projects that do not use TrustZone, debug the MCUboot project using the default configuration. Before running, load the signed image to the address specified in the signing comment in `ra_cfg/mcu-tools/include/mcuboot_config/mcuboot_config.h`. This can be done with the Load Ancillary File button when debugging in e2 studio. Upgrade images can be loaded to the upgrade image slots using the same method.

For TrustZone projects, debug using the Secure project to ensure the IDAU is partitioned correctly when debugging in e2 studio. Make the following modifications before debugging in e2 studio:

1. In the Debug Configurations for your project, on the Startup tab, click Add... to add the

- MCUboot project \*.elf file (Image and Symbols), and optionally the Non-Secure project \*.elf file.
2. For the Secure and Non-Secure project \*.elf file, load Symbols Only.
  3. After starting to debug, load the signed Secure image and the signed Non-Secure image into the addresses specified in the signing comment in ra\_cfg/mcu-tools/include/mcuboot\_config/mcuboot\_config.h. This can be done with the Load Ancillary File button when debugging in e2 studio. Upgrade images can be loaded to the upgrade image slots using the same method.

## Confirming Upgrade in Swap Mode

In Swap Mode operation, if the upgrade image is signed with the `-pad` option, MCUboot will install that image as a temporary update where if nothing else is done, a reboot will cause MCUboot to revert to the image version that was swapped out during the upgrade. In order for the updated image to prevent this reversion and make the update permanent, the `boot_set_confirmed()` must be called from the application.

To avail this capability in the application image, from the Stacks tab, add New > Bootloader > MCUboot Image Utilities (Swap Mode). Resolve any constraint errors and edit configurations as desired.

In `src/hal_entry.c`, drag in Developer Assistance > HAL/Common > MCUboot Image Utilities > Quick Setup > Confirm Primary Image. Add a call to `boot_set_confirmed()` in the application and confirm the image in the primary slot.

## MCUboot Memory Map

For single image projects, the default memory map looks like:

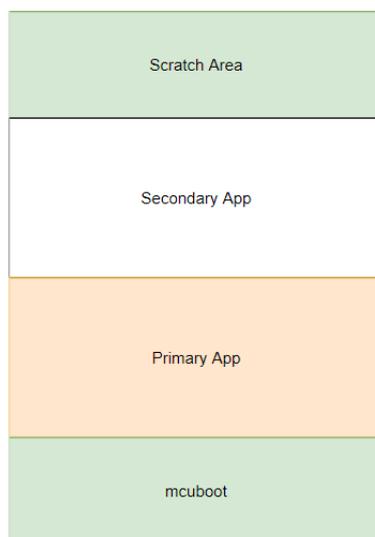


Figure 195: MCUboot Memory Map

For projects with 2 separately updateable images (used for TrustZone applications where the Secure and Non-Secure images can be updated separately), the default memory map looks like:

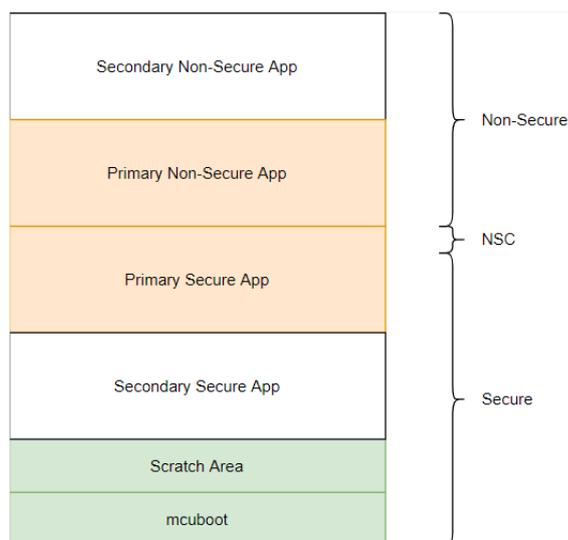


Figure 196: MCUboot Memory Map (TrustZone)

## MCUboot Crypto Stack Options

The following crypto stacks can be used with MCUboot in FSP:

1. MbedTLS, which is hardware accelerated on all RA devices. On the RA2 which has an AES engine only, ECC/RSA/SHA operations are in software.
2. TinyCrypt (S/W Only) can be used with all devices.
3. TinyCrypt (H/W Accelerated) has AES operations accelerated for the RA2 family only. When using MCUboot without encryption there is no difference between using this or the S/W only version.
4. SCE9 Protected Mode on devices that have the SCE9 (eg: RA6M4, RA4M3, RA4M2)

MbedTLS provides the best performance for MCUBoot signature verification on the RA6 and RA4 devices but has a much larger code footprint compared to TinyCrypt. For RA2 devices TinyCrypt is the best option.

## Using SCE9 Protected Mode Crypto Stack

Using this crypto stack with MCUBoot provides additional security by ensuring that any keys that are used were securely provisioned for the specific device. The Application Note R11AN0496 provides detailed steps on how to go about installing these keys. Since the section "Preparing Keys for Installation and Update Using RFP" document currently only provides information on how to install an AES key, this section will provide information on how to install an ECC public key.

### Note

*When using the SCE9 Protected Mode Stack with MCUboot it is required that the public keys in the format described in the "MCUboot Example Keys" module in the stack is also provided in the project.*

1. Generate an ECC key pair. There are various ways to do this but you can use openssl to do so: "openssl ecparam -name secp256k1 -genkey -noout -out my\_ecc\_secp256k1\_key.pem".
2. Once the key is generated, in order to install the public key using RFP (Renesas Flash Programmer) the user needs to have their own UFPK (User Factory Programming Key) and W-UFPK (Wrapped User Factory Programming Key). Refer to R11AN0496 on how to obtain these keys.

3. Once the UFPK and W-UFPK are available, we need to extract the public key from the pem file. The public key can be viewed by using "openssl ec -noout -text -in my\_ecc\_secp256k1\_key.pem". Note that when the ECC public key is printed out this way, it will contain a 0x04 ASN.1 demarcator at the start which should be discarded.
4. Use the rfp-util.exe utility from the RFP installation folder to wrap the public key using the UFPK and W-UFPK into a format that can be installed by RFP and the factory bootloader on the MCU.
5. Use RFP as described in R11AN0496 to install the key to the location of mcuboot\_sce9\_key section.

These are examples that install the default keys provided with MCUboot in ra/mcu-tools/MCUboot/. The examples assume that UFPK and W-UFPK are already available.

```
//Print out the EC-P256 Public Key using openSSL
C:\ openssl ec -noout -text -in root-ec-p256.pem
read EC key
Private-Key: (256 bit)
priv:
    d7:98:d5:2f:83:01:24:3b:d3:54:2b:7e:55:ed:4c:
    74:61:19:00:b0:f9:50:5a:82:4f:e1:e8:ec:06:3b:
    cf:f1
pub:
    04:2a:cb:40:3c:e8:fe:ed:5b:a4:49:95:a1:a9:1d:
    ae:e8:db:be:19:37:cd:14:fb:2f:24:57:37:e5:95:
    39:88:d9:94:b9:d6:5a:eb:d7:cd:d5:30:8a:d6:fe:
    48:b2:4a:6a:81:0e:e5:f0:7d:8b:68:34:cc:3a:6a:
    fc:53:8e:fa:c1
ASN1 OID: prime256v1
NIST CURVE: P-256
//Use the public key (ignore the 0x04 ASN.1 demarcator) in the RFP command line to
convert the public key into an installable format
C:\ "C:\Program Files (x86)\Renesas Electronics\Programming Tools\Renesas Flash
Programmer V3.08\rfp-util.exe" /genkey /ufpk "C:\ufpk.key" /wufpk
"C:\ufpk.key_enc.key" /key "2acb403ce8feed5ba44995a1a91daee8dbbe1937cd14fb2f245737e59
53988d994b9d65aebd7cdd5308ad6fe48b24a6a810ee5f07d8b6834cc3a6afc538efac1" /userkey
"16" /output "C:\ECC_pub_install.rkey"
// From the bootloader map file determine the address of mcuboot_sce9_key section
Use RFP to install "ECC_pub_install.rkey" as described in R11AN0496 to the address
where the mcuboot_sce9_key section is located.
```

## Limitations

MCUboot tooling updates to adjust available flash in application images are currently only supported for the GCC compiler. IAR and AC6 support will be added in a future release.

## Examples

### Basic Example

This is an example of using MCUboot in an application.

```
void rm_mcuboot_port_example (void)
{
#ifdef MCUBOOT_USE_MBED_TLS
    /* Initialize mbedtls. */
    mbedtls_platform_context ctx = {0};
    assert(0 == mbedtls_platform_setup(&ctx));
#elif defined(MCUBOOT_USE_TINYCRYPT)
    /* Initialize TinyCrypt port. */
    assert(FSP_SUCCESS == RM_TINYCRYPT_PORT_Init());
#else
    /* Initialize SCE9 Protected Mode driver. */
    sce_instance_ctrl_t sce_ctrl;
    const sce_cfg_t sce_cfg =
        {.lifecycle = SCE_SSD};
    assert(FSP_SUCCESS == R_SCE_Open(&sce_ctrl, &sce_cfg));
#endif

    /* (Optional) To check for updates, call boot_set_pending. */
    bool update = 0;
    if (update)
    {
        boot_set_pending(0);
    }

    /* Verify the boot image and get its location. */
    struct boot_rsp rsp;
    assert(0 == boot_go(&rsp));
}
```

```

/* Enter the application. */
RM_MCUBOOT_PORT_BootApp(&rsp);
}

```

## 4.2.85 Motor Current (rm\_motor\_current)

### Modules

#### Functions

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_Open](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_cfg_t const *const p_cfg`)

Opens and configures the Motor Current Module. Implements [motor\\_current\\_api\\_t::open](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_Close](#) (`motor_current_ctrl_t *const p_ctrl`)

Disables specified Motor Current Module. Implements [motor\\_current\\_api\\_t::close](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_Reset](#) (`motor_current_ctrl_t *const p_ctrl`)

Reset variables of Motor Current Module. Implements [motor\\_current\\_api\\_t::reset](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_Run](#) (`motor_current_ctrl_t *const p_ctrl`)

Run(Start) the Current Control. Implements [motor\\_current\\_api\\_t::run](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_ParameterSet](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_input_t const *const p_st_input`)

Set (Input) Parameter Data. Implements [motor\\_current\\_api\\_t::parameterSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_CurrentReferenceSet](#) (`motor_current_ctrl_t *const p_ctrl`, `float const id_reference`, `float const iq_reference`)

Set Current Reference Data. Implements [motor\\_current\\_api\\_t::currentReferenceSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_SpeedPhaseSet](#) (`motor_current_ctrl_t *const p_ctrl`, `float const speed`, `float const phase`)

Set Current Speed & rotor phase Data. Implements [motor\\_current\\_api\\_t::speedPhaseSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_CurrentSet](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_input_current_t const *const p_st_current`, `motor_current_input_voltage_t const *const p_st_voltage`)

Set d/q-axis Current & Voltage Data. Implements [motor\\_current\\_api\\_t::currentSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_ParameterGet](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_output_t *const p_st_output`)

Get Output Parameters. Implements [motor\\_current\\_api\\_t::parameterGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_CurrentGet](#) (`motor_current_ctrl_t *const p_ctrl`, `float *const p_id`, `float *const p_iq`)

Get d/q-axis Current. Implements [motor\\_current\\_api\\_t::currentGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_PhaseVoltageGet](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_get_voltage_t *const p_voltage`)

Gets the set phase voltage. Implements [motor\\_current\\_api\\_t::phaseVoltageGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_CURRENT\\_ParameterUpdate](#) (`motor_current_ctrl_t *const p_ctrl`, `motor_current_cfg_t const *const p_cfg`)

Update the parameters of Current Control. Implements [motor\\_current\\_api\\_t::parameterUpdate](#). [More...](#)

`void` [rm\\_motor\\_current\\_encoder\\_cyclic](#) (`motor_current_instance_t const *p_ctrl`)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor current Interface](#).

## Overview

The motor current is used to control the electric current of motor rotation in an application. This module should be called cyclically after the A/D conversion of electric current of each phase in an application. This module calculates each phase voltage with input current reference, electric current

and rotor angle.

## Features

The Motor Current Module has below features.

- Calculate each phase(U/V/W) voltage.
- Decoupling Control.
- Voltage Error Compensation.

## Configuration

### Build Time Configurations for rm\_motor\_current

The following build time configurations are defined in fsp\_cfg/rm\_motor\_current\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Current Controller on rm\_motor\_current

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Current Controller on rm\_motor\_current.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_current0	Module name.
General > Sensor type	<ul style="list-style-type: none"> <li>• Sensorless</li> <li>• Encoder</li> </ul>	Sensorless	Select sensor type
General > Current control decimation	Manual Entry	0	Decimation of current control.
General > PWM carrier frequency (kHz)	Manual Entry	20.0F	PWM carrier frequency.
General > Input voltage	Manual Entry	24.0F	Input voltage for limitation of current PI control.
General > Sample delay compensation	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable sample delay compensation.
General > Voltage error compensation	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Select enable/disable voltage error compensation.
General > Voltage error compensation table of voltage 1	Manual Entry	0.672F	Voltage error compensation table of voltage.
General > Voltage	Manual Entry	0.945F	Voltage error

error compensation table of voltage 2			compensation table of voltage.
General > Voltage error compensation table of voltage 3	Manual Entry	1.054F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 4	Manual Entry	1.109F	Voltage error compensation table of voltage.
General > Voltage error compensation table of voltage 5	Manual Entry	1.192F	Voltage error compensation table of voltage.
General > Voltage error compensation table of current 1	Manual Entry	0.013F	Voltage error compensation table of current.
General > Voltage error compensation table of current 2	Manual Entry	0.049F	Voltage error compensation table of current.
General > Voltage error compensation table of current 3	Manual Entry	0.080F	Voltage error compensation table of current.
General > Voltage error compensation table of current 4	Manual Entry	0.184F	Voltage error compensation table of current.
General > Voltage error compensation table of current 5	Manual Entry	0.751F	Voltage error compensation table of current.
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at A/D conversion finish interrupt.
Design Parameter > Current PI loop omega	Manual Entry	300.0F	Current PI loop omega
Design Parameter > Current PI loop zeta	Manual Entry	1.0F	Current PI loop zeta
Motor Parameter > Pole pairs	Manual Entry	2	Pole pairs
Motor Parameter > Resistance (ohm)	Manual Entry	8.5F	Resistance
Motor Parameter > Inductance of d-axis (H)	Manual Entry	0.0045F	Inductance of d-axis
Motor Parameter > Inductance of q-axis	Manual Entry	0.0045F	Inductance of q-axis

(H)

Motor Parameter > Permanent magnetic flux (Wb)	Manual Entry	0.02159F	Permanent magnetic flux
Motor Parameter > Rotor inertia (kgm <sup>2</sup> )	Manual Entry	0.0000028F	Rotor inertia

## Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

- Set the Period of Current Control with none-negative value.
- Set the Reference Voltage with none-negative value.

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Current in an application.

```
void motor_current_basic_example (void)
{
    motor_current_input_current_t temp_input_current;
    motor_current_input_voltage_t temp_input_voltage;
    motor_current_get_voltage_t temp_get_voltage;
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_CURRENT_Open(g_test_motor_current.p_ctrl,
g_test_motor_current.p_cfg);
    assert(FSP_SUCCESS == err);
    /* Basically run this module at A/D conversion finish interrupt.
    * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */
    }
}
```

```
/* Set current reference before get phase voltage */
    (void) RM_MOTOR_CURRENT_CurrentReferenceSet(g_test_motor_current.p_ctrl, 1.0F,
1.0F);
/* Set speed and phase data before get phase voltage */
    (void) RM_MOTOR_CURRENT_SpeedPhaseSet(g_test_motor_current.p_ctrl, 104.72F,
1.0F);

    temp_input_current.iu    = 1.0F;
    temp_input_current.iv    = 1.0F;
    temp_input_current.iw    = 1.0F;
    temp_input_voltage.vdc   = 24.0F;
    temp_input_voltage.va_max = 24.0F;

/* Set electric current and voltage before get phase voltage */
    (void) RM_MOTOR_CURRENT_CurrentSet(g_test_motor_current.p_ctrl,
temp_input_current, temp_input_voltage);
/* Activate the process. */
    (void) RM_MOTOR_CURRENT_Run(g_test_motor_current.p_ctrl);
/* Get d/q-axis current*/
    (void) RM_MOTOR_CURRENT_CurrentGet(g_test_motor_current.p_ctrl, &f_get_id,
&f_get_iq);
/* Get the flag of PI control */
    (void) RM_MOTOR_CURRENT_PhaseVolageGet(g_test_motor_current.p_ctrl,
&temp_get_voltage);
/* Get Output Parameter */
    (void) RM_MOTOR_CURRENT_ParameterGet(g_test_motor_current.p_ctrl,
&test_output);
    (void) RM_MOTOR_CURRENT_ParameterUpdate(g_test_motor_current.p_ctrl,
g_test_motor_current.p_cfg);
}
/* Reset the process. */
    (void) RM_MOTOR_CURRENT_Reset(g_test_motor_current.p_ctrl);
/* Close the module. */
    (void) RM_MOTOR_CURRENT_Close(g_test_motor_current.p_ctrl);
}
```

## Function Documentation

### ◆ RM\_MOTOR\_CURRENT\_Open()

```
fsp_err_t RM_MOTOR_CURRENT_Open ( motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t
const *const p_cfg )
```

Opens and configures the Motor Current Module. Implements `motor_current_api_t::open`.

#### Return values

FSP_SUCCESS	Motor Current successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

### ◆ RM\_MOTOR\_CURRENT\_Close()

```
fsp_err_t RM_MOTOR_CURRENT_Close ( motor_current_ctrl_t *const p_ctrl)
```

Disables specified Motor Current Module. Implements `motor_current_api_t::close`.

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_MOTOR\_CURRENT\_Reset()

```
fsp_err_t RM_MOTOR_CURRENT_Reset ( motor_current_ctrl_t *const p_ctrl)
```

Reset variables of Motor Current Module. Implements `motor_current_api_t::reset`.

#### Return values

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_Run()**

```
fsp_err_t RM_MOTOR_CURRENT_Run ( motor_current_ctrl_t *const p_ctrl)
```

Run(Start) the Current Control. Implements `motor_current_api_t::run`.

**Return values**

FSP_SUCCESS	Successfully run.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_ParameterSet()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterSet ( motor_current_ctrl_t *const p_ctrl,
motor_current_input_t const *const p_st_input )
```

Set (Input) Parameter Data. Implements `motor_current_api_t::parameterSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input argument error.

◆ **RM\_MOTOR\_CURRENT\_CurrentReferenceSet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentReferenceSet ( motor_current_ctrl_t *const p_ctrl, float
const id_reference, float const iq_reference )
```

Set Current Reference Data. Implements `motor_current_api_t::currentReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_SpeedPhaseSet()**

```
fsp_err_t RM_MOTOR_CURRENT_SpeedPhaseSet ( motor_current_ctrl_t *const p_ctrl, float const speed, float const phase )
```

Set Current Speed & rotor phase Data. Implements `motor_current_api_t::speedPhaseSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_CURRENT\_CurrentSet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentSet ( motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage )
```

Set d/q-axis Current & Voltage Data. Implements `motor_current_api_t::currentSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_ParameterGet()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterGet ( motor_current_ctrl_t *const p_ctrl, motor_current_output_t *const p_st_output )
```

Get Output Parameters. Implements `motor_current_api_t::parameterGet`.

**Return values**

FSP_SUCCESS	Successful data get.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_CurrentGet()**

```
fsp_err_t RM_MOTOR_CURRENT_CurrentGet ( motor_current_ctrl_t *const p_ctrl, float *const p_id,
float *const p_iq )
```

Get d/q-axis Current. Implements `motor_current_api_t::currentGet`.

**Return values**

FSP_SUCCESS	Successful data get.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_PhaseVoltageGet()**

```
fsp_err_t RM_MOTOR_CURRENT_PhaseVoltageGet ( motor_current_ctrl_t *const p_ctrl,
motor_current_get_voltage_t *const p_voltage )
```

Gets the set phase voltage. Implements `motor_current_api_t::phaseVoltageGet`.

**Return values**

FSP_SUCCESS	Successful data calculation.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_CURRENT\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_CURRENT_ParameterUpdate ( motor_current_ctrl_t *const p_ctrl,
motor_current_cfg_t const *const p_cfg )
```

Update the parameters of Current Control. Implements `motor_current_api_t::parameterUpdate`.

**Return values**

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **rm\_motor\_current\_encoder\_cyclic()**

```
void rm_motor_current_encoder_cyclic ( motor_current_instance_t const * p_ctrl)
```

```
(end addtogroup MOTOR_CURRENT)
```

**4.2.86 Motor Driver (rm\_motor\_driver)**

## Modules

**Functions**

`fsp_err_t` `RM_MOTOR_DRIVER_Open` (`motor_driver_ctrl_t *const p_ctrl`,  
`motor_driver_cfg_t const *const p_cfg`)

Opens and configures the Motor Driver module. Implements `motor_driver_api_t::open`. [More...](#)

`fsp_err_t` `RM_MOTOR_DRIVER_Close` (`motor_driver_ctrl_t *const p_ctrl`)

Disables specified Motor Driver Module. Implements `motor_driver_api_t::close`. [More...](#)

`fsp_err_t` `RM_MOTOR_DRIVER_Reset` (`motor_driver_ctrl_t *const p_ctrl`)

Reset variables of Motor Driver Module. Implements `motor_driver_api_t::reset`. [More...](#)

`fsp_err_t` `RM_MOTOR_DRIVER_PhaseVoltageSet` (`motor_driver_ctrl_t *const p_ctrl`, `float const u_voltage`, `float const v_voltage`, `float const w_voltage`)

Set Phase Voltage Data to calculate PWM duty. Implements `motor_driver_api_t::phaseVoltageSet`. [More...](#)

`fsp_err_t` `RM_MOTOR_DRIVER_CurrentGet` (`motor_driver_ctrl_t *const p_ctrl`,  
`motor_driver_current_get_t *const p_current_get`)

Get calculated phase Current, Vdc & Va\_max data. Implements `motor_driver_api_t::currentGet`. [More...](#)

`fsp_err_t` `RM_MOTOR_DRIVER_FlagCurrentOffsetGet` (`motor_driver_ctrl_t *const p_ctrl`,  
`uint8_t *const p_flag_offset`)

Get the flag of finish current offset detection. Implements `motor_driver_api_t::flagCurrentOffsetGet`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_CurrentOffsetRestart (motor_driver_ctrl_t *const p_ctrl)`

Restart the current offset detection. Implements `motor_driver_api_t::currentOffsetRestart`. [More...](#)

`fsp_err_t RM_MOTOR_DRIVER_ParameterUpdate (motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)`

Update the parameters of Driver Module. Implements `motor_driver_api_t::parameterUpdate`. [More...](#)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor driver Interface](#).

## Overview

The motor driver module is used to translate phase voltage to PWM duty and output PWM, and detect phase current and main line voltage. This module should be called cyclically at included A/D Conversion finish interrupt.

## Features

The Motor Driver Module has below features.

- Calculate each phase(U/V/W) PWM duty according to reference and output PWM.
- Detect each phase current and main line voltage.
- Detect and correct A/D offset at phase current channel

## Configuration

### Build Time Configurations for rm\_motor\_driver

The following build time configurations are defined in `fsp_cfg/rm_motor_driver_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > ADC and PWM Modulation Driver on rm\_motor\_driver

This module can be added to the Stacks tab via New Stack > Middleware > Motor > ADC and PWM Modulation Driver on `rm_motor_driver`.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

General > Name	Name must be a valid C symbol	g_motor_driver0	Module name.
General > PWM Timer Frequency[MHz]	Manual Entry	120	GPT PWM Timer Frequency
General > PWM Carrier Period[Microseconds]	Manual Entry	50	GPT PWM Carrier Period
General > Dead Time[Raw Counts]	Manual Entry	240	GPT PWM Dead Time
General > Current Range[A]	Manual Entry	27.5F	Current Range to measure(Maximum input current)
General > Voltage Range[V]	Manual Entry	111.0F	Voltage Range to measure(Maximum input Main Line Voltage)
General > Counts for current offset measurement	Manual Entry	500	How many times to measure current offset
General > A/D conversion channel for U Phase current	Manual Entry	0	Specify the A/D channel for U Phase current
General > A/D conversion channel for W Phase current	Manual Entry	2	Specify the A/D channel for W Phase current
General > A/D conversion channel for Main Line Voltage	Manual Entry	5	Specify the A/D channel for Main Line Voltage
General > Input Voltage	Manual Entry	24.0F	Input Voltage
General > Resolution of A/D conversion	Manual Entry	0xFFF	Resolution of A/D conversion
General > Offset of A/D conversion for current	Manual Entry	0x745	Offset of A/D conversion for current
General > Conversion level of A/D conversion for voltage	Manual Entry	0.6F	Conversion level of A/D conversion for voltage
General > GTIOCA Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level High	Select the behavior of the output pin when the timer is stopped.
General > GTIOCB Stop Level	<ul style="list-style-type: none"> <li>• Pin Level Low</li> <li>• Pin Level High</li> </ul>	Pin Level High	Select the behavior of the output pin when the timer is stopped.
Modulation > Maximum Duty	Manual Entry	0.9375F	Maximum Duty of PWM

Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at A/D conversion finish interrupt.
-----------------------	-------------------------------	------	---

## Clock Configuration

Set used clock with included GPT timer.

## Pin Configuration

Depend on included GPT Three Phase Module and ADC Module.

# Usage Notes

## Limitations

Basically no limitation exists.

# Examples

## Basic Example

This is a basic example of minimal use of the Motor Driver in an application.

```
void motor_driver_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_DRIVER_Open(&g_motor_driver0.p_ctrl, &g_motor_driver0.p_cfg);
    assert(FSP_SUCCESS == err);
    /* Basically run this module at cyclic interrupt (e.g. included GPT PWM Carrier
    interrupt).
    * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */
        /* Get electric current, main line voltage and maximum voltage component */
        (void) RM_MOTOR_DRIVER_CurrentGet(&g_motor_driver0.p_ctrl, &f_get_iu,
        &f_get_iw, &f_get_vdc, &f_get_va_max);
        /* Get the flag of A/D converted current offset */
        (void) RM_MOTOR_DRIVER_FlagCurrentOffsetGet(&g_motor_driver0.p_ctrl,
```

```

&ul_get_flg_offset);

// Perform current control process here
/* Set phase voltage */
    (void) RM_MOTOR_DRIVER_PhaseVoltageSet(&g_motor_driver0.p_ctrl, 1.0F, 1.0F,
1.0F);
    (void) RM_MOTOR_DRIVER_ParameterUpdate(&g_motor_driver0.p_ctrl,
&g_motor_driver0.p_cfg);
}
(void) RM_MOTOR_DRIVER_Reset(&g_motor_driver0.p_ctrl);
//

(void) RM_MOTOR_DRIVER_Close(&g_motor_driver0.p_ctrl);
}

```

## Function Documentation

### ◆ RM\_MOTOR\_DRIVER\_Open()

`fsp_err_t RM_MOTOR_DRIVER_Open ( motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg )`

Opens and configures the Motor Driver module. Implements `motor_driver_api_t::open`.

#### Return values

FSP_SUCCESS	Motor Driver successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.

◆ **RM\_MOTOR\_DRIVER\_Close()**

```
fsp_err_t RM_MOTOR_DRIVER_Close ( motor_driver_ctrl_t *const p_ctrl)
```

Disables specified Motor Driver Module. Implements `motor_driver_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_Reset()**

```
fsp_err_t RM_MOTOR_DRIVER_Reset ( motor_driver_ctrl_t *const p_ctrl)
```

Reset variables of Motor Driver Module. Implements `motor_driver_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_PhaseVoltageSet()**

```
fsp_err_t RM_MOTOR_DRIVER_PhaseVoltageSet ( motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage )
```

Set Phase Voltage Data to calculate PWM duty. Implements `motor_driver_api_t::phaseVoltageSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_DRIVER\_CurrentGet()**

```
fsp_err_t RM_MOTOR_DRIVER_CurrentGet ( motor_driver_ctrl_t *const p_ctrl,
motor_driver_current_get_t *const p_current_get )
```

Get calculated phase Current, Vdc & Va\_max data. Implements `motor_driver_api_t::currentGet`.

**Return values**

FSP_SUCCESS	Successful data get.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_DRIVER\_FlagCurrentOffsetGet()**

```
fsp_err_t RM_MOTOR_DRIVER_FlagCurrentOffsetGet ( motor_driver_ctrl_t *const p_ctrl, uint8_t
*const p_flag_offset )
```

Get the flag of finish current offset detection. Implements `motor_driver_api_t::flagCurrentOffsetGet`.

**Return values**

FSP_SUCCESS	Successful data get.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input parameter error.

◆ **RM\_MOTOR\_DRIVER\_CurrentOffsetRestart()**

```
fsp_err_t RM_MOTOR_DRIVER_CurrentOffsetRestart ( motor_driver_ctrl_t *const p_ctrl)
```

Restart the current offset detection. Implements `motor_driver_api_t::currentOffsetRestart`.

**Return values**

FSP_SUCCESS	Successfully restarted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_MOTOR\_DRIVER\_ParameterUpdate()

```
fsp_err_t RM_MOTOR_DRIVER_ParameterUpdate ( motor_driver_ctrl_t *const p_ctrl,
motor_driver_cfg_t const *const p_cfg )
```

Update the parameters of Driver Module. Implements [motor\\_driver\\_api\\_t::parameterUpdate](#).

#### Return values

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

## 4.2.87 Motor encoder vector control (rm\_motor\_encoder)

### Modules

#### Functions

```
fsp_err_t RM_MOTOR_ENCODER_Open (motor_ctrl_t *const p_ctrl, motor_cfg_t
const *const p_cfg)
```

```
fsp_err_t RM_MOTOR_ENCODER_Close (motor_ctrl_t *const p_ctrl)
```

Disables specified Motor Encoder Control block. Implements [motor\\_api\\_t::close](#). [More...](#)

```
fsp_err_t RM_MOTOR_ENCODER_Run (motor_ctrl_t *const p_ctrl)
```

Run Motor (Start motor rotation). Implements [motor\\_api\\_t::run](#). [More...](#)

```
fsp_err_t RM_MOTOR_ENCODER_Stop (motor_ctrl_t *const p_ctrl)
```

Stop Motor (Stop motor rotation). Implements [motor\\_api\\_t::stop](#). [More...](#)

```
fsp_err_t RM_MOTOR_ENCODER_Reset (motor_ctrl_t *const p_ctrl)
```

Reset Motor Encoder Control block. Implements [motor\\_api\\_t::reset](#). [More...](#)

```
fsp_err_t RM_MOTOR_ENCODER_ErrorSet (motor_ctrl_t *const p_ctrl,
motor_error_t const error)
```

Set error information. Implements [motor\\_api\\_t::errorSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_SpeedSet](#) (`motor_ctrl_t *const p_ctrl`, `float const speed_rpm`)

Set speed reference[rpm]. Implements [motor\\_api\\_t::speedSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_PositionSet](#) (`motor_ctrl_t *const p_ctrl`, `motor_speed_position_data_t const *const p_position`)

Set position reference[degree]. Implements [motor\\_api\\_t::positionSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_StatusGet](#) (`motor_ctrl_t *const p_ctrl`, `uint8_t *const p_status`)

Get current control status. Implements [motor\\_api\\_t::statusGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_AngleGet](#) (`motor_ctrl_t *const p_ctrl`, `float *const p_angle_rad`)

Get current rotor angle. Implements [motor\\_api\\_t::angleGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_SpeedGet](#) (`motor_ctrl_t *const p_ctrl`, `float *const p_speed_rpm`)

Get rotational speed. Implements [motor\\_api\\_t::speedGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_ENCODER\\_ErrorCheck](#) (`motor_ctrl_t *const p_ctrl`, `uint16_t *const p_error`)

Check the occurrence of Error. Implements [motor\\_api\\_t::errorCheck](#). [More...](#)

## Detailed Description

Control a SPM motor on RA MCUs. This module implements the [Motor encoder vector control \(rm\\_motor\\_encoder\)](#).

## Overview

The motor encoder vector control is used to control motor rotation in an application. This module is meant to be used with Surface Permanent Magnet (SPM) motors and allows applications to start or stop motor rotation easily.

## Features

The motor encoder module has below features.

- Start/stop motor rotation
- Error detection (over current, over speed, over voltage, low voltage)

## Configuration

### Build Time Configurations for rm\_motor\_encoder

The following build time configurations are defined in fsp\_cfg/rm\_motor\_encoder\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor encoder vector control

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor encoder vector control.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_encoder0	Module name.
General > Limit of over current (A)	Must be a valid non-negative value.	2.0F	Limit of over current.(Detection threshold)
General > Limit of over voltage (V)	Must be a valid non-negative value.	28.0F	Limit of over voltage.(Detection threshold)
General > Limit of over speed (rpm)	Must be a valid non-negative value.	2100.0F	Limit of over speed.(Detection threshold)
General > Limit of low voltage (V)	Must be a valid non-negative value.	18.0F	Limit of low voltage.(Detection threshold)
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at speed control cyclic interrupt.

### Clock Configuration

This module doesn't depend on clock setting, because this module is a simple status transition process.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

## Examples

### Basic Example

This is a basic example of minimal use of the motor encoder module in an application.

```
void motor_encoder_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_ENCODER_Open(g_motor_encoder0.p_ctrl, g_motor_encoder0.p_cfg);
    handle_error(err);
    /* Set speed reference before motor run */
    (void) RM_MOTOR_ENCODER_SpeedSet(g_motor_encoder0.p_ctrl,
RM_MOTOR_ENCODER_TEST_OVER_SPEED_LIMIT);
    /* Set position reference before motor run */
    (void) RM_MOTOR_ENCODER_PositionSet(g_motor_encoder0.p_ctrl, &g_posref_sample1);
    /* Start motor rotation */
    (void) RM_MOTOR_ENCODER_Run(g_motor_encoder0.p_ctrl);
    /* Get current status */
    (void) RM_MOTOR_ENCODER_StatusGet(g_motor_encoder0.p_ctrl, &smpl_status);
    /* Get current rotor angle */
    (void) RM_MOTOR_ENCODER_AngleGet(g_motor_encoder0.p_ctrl, &smpl_angle);
    /* Get current motor speed */
    (void) RM_MOTOR_ENCODER_SpeedGet(g_motor_encoder0.p_ctrl, &smpl_speed);
    /* Check error */
    (void) RM_MOTOR_ENCODER_ErrorCheck(g_motor_encoder0.p_ctrl, &smpl_error);
    /* Stop motor rotation */
    (void) RM_MOTOR_ENCODER_Stop(g_motor_encoder0.p_ctrl);
    /* Stop motor rotation */
    (void) RM_MOTOR_ENCODER_ErrorSet(g_motor_encoder0.p_ctrl,
MOTOR_ERROR_OVER_CURRENT_HW);
}
```

```

/* Reset Speed Control */
(void) RM_MOTOR_ENCODER_Reset(g_motor_encoder0.p_ctrl);
/* Close Speed Control */
(void) RM_MOTOR_ENCODER_Close(g_motor_encoder0.p_ctrl);
}

```

## Data Structures

struct [motor\\_encoder\\_callback\\_args\\_t](#)

## Enumerations

enum [motor\\_encoder\\_ctrl\\_t](#)

enum [motor\\_encoder\\_ctrl\\_event\\_t](#)

enum [motor\\_encoder\\_callback\\_event\\_t](#)

## Data Structure Documentation

### ◆ motor\_encoder\_callback\_args\_t

struct <a href="#">motor_encoder_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data.
<a href="#">motor_encoder_callback_event_t</a>	event	

## Enumeration Type Documentation

### ◆ motor\_encoder\_ctrl\_t

enum <a href="#">motor_encoder_ctrl_t</a>	
Enumerator	
MOTOR_ENCODER_CTRL_STOP	Stop mode.
MOTOR_ENCODER_CTRL_RUN	Run mode.
MOTOR_ENCODER_CTRL_ERROR	Error mode.

## ◆ motor\_encoder\_ctrl\_event\_t

enum motor_encoder_ctrl_event_t	
Enumerator	
MOTOR_ENCODER_CTRL_EVENT_STOP	Stop event.
MOTOR_ENCODER_CTRL_EVENT_RUN	Run event.
MOTOR_ENCODER_CTRL_EVENT_ERROR	Error event.
MOTOR_ENCODER_CTRL_EVENT_RESET	Reset event.

## ◆ motor\_encoder\_callback\_event\_t

enum motor_encoder_callback_event_t	
Events that can trigger a callback function	
Enumerator	
MOTOR_ENCODER_CALLBACK_EVENT_SPEED_FORWARD	Event forward speed control.
MOTOR_ENCODER_CALLBACK_EVENT_SPEED_BACKWARD	Event backward speed control.
MOTOR_ENCODER_CALLBACK_EVENT_CURRENT_FORWARD	Event forward current control.
MOTOR_ENCODER_CALLBACK_EVENT_CURRENT_BACKWARD	Event backward current control.

## Function Documentation

---

◆ **RM\_MOTOR\_ENCODER\_Open()**

```
fsp_err_t RM_MOTOR_ENCODER_Open ( motor_ctrl_t *const p_ctrl, motor_cfg_t const *const p_cfg )
```

Configure the MOTOR in register start mode. Implements `motor_api_t::open`.

This function should only be called once as MOTOR configuration registers can only be written to once so subsequent calls will have no effect.

Example:

```
/* Initializes the module. */
err = RM_MOTOR_ENCODER_Open(g_motor_encoder0.p_ctrl, g_motor_encoder0.p_cfg);
```

**Return values**

FSP_SUCCESS	MOTOR successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

*Note*

◆ **RM\_MOTOR\_ENCODER\_Close()**

```
fsp_err_t RM_MOTOR_ENCODER_Close ( motor_ctrl_t *const p_ctrl)
```

Disables specified Motor Encoder Control block. Implements `motor_api_t::close`.

Example:

```
/* Close Speed Control */
(void) RM_MOTOR_ENCODER_Close(g_motor_encoder0.p_ctrl);
```

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_ENCODER\_Run()**

```
fsp_err_t RM_MOTOR_ENCODER_Run ( motor_ctrl_t *const p_ctrl)
```

Run Motor (Start motor rotation). Implements `motor_api_t::run`.

Example:

```
/* Start motor rotation */
(void) RM_MOTOR_ENCODER_Run(g_motor_encoder0.p_ctrl);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_ENCODER\_Stop()**

```
fsp_err_t RM_MOTOR_ENCODER_Stop ( motor_ctrl_t *const p_ctrl)
```

Stop Motor (Stop motor rotation). Implements `motor_api_t::stop`.

Example:

```
/* Stop motor rotation */
(void) RM_MOTOR_ENCODER_Stop(g_motor_encoder0.p_ctrl);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_ENCODER\_Reset()

```
fsp_err_t RM_MOTOR_ENCODER_Reset ( motor_ctrl_t *const p_ctrl)
```

Reset Motor Encoder Control block. Implements `motor_api_t::reset`.

Example:

```
/* Reset Speed Control */
(void) RM_MOTOR_ENCODER_Reset(g_motor_encoder0.p_ctrl);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_ENCODER\_ErrorSet()

```
fsp_err_t RM_MOTOR_ENCODER_ErrorSet ( motor_ctrl_t *const p_ctrl, motor_error_t const error )
```

Set error information. Implements `motor_api_t::errorSet`.

Example:

```
/* Stop motor rotation */
(void) RM_MOTOR_ENCODER_ErrorSet(g_motor_encoder0.p_ctrl,
MOTOR_ERROR_OVER_CURRENT_HW);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_ENCODER\_SpeedSet()**

```
fsp_err_t RM_MOTOR_ENCODER_SpeedSet ( motor_ctrl_t *const p_ctrl, float const speed_rpm )
```

Set speed reference[rpm]. Implements `motor_api_t::speedSet`.

Example:

```
/* Set speed reference before motor run */
(void) RM_MOTOR_ENCODER_SpeedSet(g_motor_encoder0.p_ctrl,
RM_MOTOR_ENCODER_TEST_OVER_SPEED_LIMIT);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_ENCODER\_PositionSet()**

```
fsp_err_t RM_MOTOR_ENCODER_PositionSet ( motor_ctrl_t *const p_ctrl,
motor_speed_position_data_t const *const p_position )
```

Set position reference[degree]. Implements `motor_api_t::positionSet`.

Example:

```
/* Set position reference before motor run */
(void) RM_MOTOR_ENCODER_PositionSet(g_motor_encoder0.p_ctrl, &g_posref_sample1);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data set pointer is invalid..

*Note*

◆ **RM\_MOTOR\_ENCODER\_StatusGet()**

```
fsp_err_t RM_MOTOR_ENCODER_StatusGet ( motor_ctrl_t *const p_ctrl, uint8_t *const p_status )
```

Get current control status. Implements `motor_api_t::statusGet`.

Example:

```
/* Get current status */
(void) RM_MOTOR_ENCODER_StatusGet(g_motor_encoder0.p_ctrl, &smpl_status);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

◆ **RM\_MOTOR\_ENCODER\_AngleGet()**

```
fsp_err_t RM_MOTOR_ENCODER_AngleGet ( motor_ctrl_t *const p_ctrl, float *const p_angle_rad )
```

Get current rotor angle. Implements `motor_api_t::angleGet`.

Example:

```
/* Get current rotor angle */
(void) RM_MOTOR_ENCODER_AngleGet(g_motor_encoder0.p_ctrl, &smpl_angle);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

◆ **RM\_MOTOR\_ENCODER\_SpeedGet()**

```
fsp_err_t RM_MOTOR_ENCODER_SpeedGet ( motor_ctrl_t *const p_ctrl, float *const p_speed_rpm )
```

Get rotational speed. Implements `motor_api_t::speedGet`.

Example:

```
/* Get current motor speed */
(void) RM_MOTOR_ENCODER_SpeedGet(g_motor_encoder0.p_ctrl, &smpl_speed);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

◆ **RM\_MOTOR\_ENCODER\_ErrorCheck()**

```
fsp_err_t RM_MOTOR_ENCODER_ErrorCheck ( motor_ctrl_t *const p_ctrl, uint16_t *const p_error )
```

Check the occurrence of Error. Implements `motor_api_t::errorCheck`.

Example:

```
/* Check error */
(void) RM_MOTOR_ENCODER_ErrorCheck(g_motor_encoder0.p_ctrl, &smpl_error);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

**4.2.88 Motor Angle and Speed Estimation (rm\_motor\_estimate)**

Modules

**Functions**

`fsp_err_t` `RM_MOTOR_ESTIMATE_Open` (`motor_angle_ctrl_t *const p_ctrl`,  
`motor_angle_cfg_t const *const p_cfg`)  
Opens and configures the Angle Estimation module. Implements `motor_angle_api_t::open`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_Close` (`motor_angle_ctrl_t *const p_ctrl`)  
Disables specified Angle Estimation module. Implements `motor_angle_api_t::close`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_Reset` (`motor_angle_ctrl_t *const p_ctrl`)  
Reset variables of Angle Estimation module. Implements `motor_angle_api_t::reset`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_CurrentSet` (`motor_angle_ctrl_t *const p_ctrl`,  
`motor_angle_current_t *const p_st_current`,  
`motor_angle_voltage_reference_t *const p_st_voltage`)  
Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_SpeedSet` (`motor_angle_ctrl_t *const p_ctrl`,  
`float const speed_ctrl`, `float const damp_speed`)  
Set Speed Information. Implements `motor_angle_api_t::speedSet`.  
[More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_FlagPiCtrlSet` (`motor_angle_ctrl_t *const p_ctrl`,  
`uint32_t const flag_pi`)  
Set the flag of PI Control runs. Implements `motor_angle_api_t::flagPiCtrlSet`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_AngleSpeedGet` (`motor_angle_ctrl_t *const p_ctrl`,  
`float *const p_angle`, `float *const p_speed`, `float *const p_phase_err`)  
Gets the current rotor's angle and rotation speed. Implements `motor_angle_api_t::angleSpeedGet`. [More...](#)

`fsp_err_t` `RM_MOTOR_ESTIMATE_EstimatedComponentGet` (`motor_angle_ctrl_t *const p_ctrl`,  
`float *const p_ed`, `float *const p_eq`)  
Gets estimated d/q-axis component. Implements `motor_angle_api_t::estimatedComponentGet`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_ParameterUpdate (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)`

Update the parameters of Angle&Speed Estimation. Implements `motor_angle_api_t::parameterUpdate`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_InternalCalculate (motor_angle_ctrl_t *const p_ctrl)`

Calculate internal parameters. Implements `motor_angle_api_t::internalCalculate`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_AngleAdjust (motor_angle_ctrl_t *const p_ctrl)`

Angle Adjustment Process. Implements `motor_angle_api_t::angleAdjust`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_EncoderCyclic (motor_angle_ctrl_t *const p_ctrl)`

Encoder Cyclic Process (Call in cyclic timer). Implements `motor_angle_api_t::encoderCyclic`. [More...](#)

`fsp_err_t RM_MOTOR_ESTIMATE_InfoGet (motor_angle_ctrl_t *const p_ctrl, motor_angle_encoder_info_t *const p_info)`

Gets information of Encoder Angle Module. Implements `motor_angle_api_t::infoGet`. [More...](#)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor angle Interface](#).

## Overview

The motor angle and speed estimation module is used to calculate rotor angle and rotational speed in an application. This module should be called cyclically after the A/D conversion of electric current of each phase in an application.

### Features

The Motor Angle and Speed Estimation Module has below features.

- Calculate rotor angle [radian].
- Calculate rotational speed [radian/second].

## Configuration

## Build Time Configurations for rm\_motor\_estimate

The following build time configurations are defined in fsp\_cfg/rm\_motor\_estimate\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## Configurations for Middleware > Motor > Motor Angle Driver on rm\_motor\_estimate

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Angle Driver on rm\_motor\_estimate.

Configuration	Options	Default	Description
Motor Parameter > Pole pairs	Manual Entry	2	Pole pairs
Motor Parameter > Resistance[ohm]	Manual Entry	8.5F	Resistance
Motor Parameter > Inductance of d-axis[H]	Manual Entry	0.0045F	Inductance of d-axis
Motor Parameter > Inductance of q-axis[H]	Manual Entry	0.0045F	Inductance of q-axis
Motor Parameter > Permanent magnetic flux[Wb]	Manual Entry	0.02159F	Permanent magnetic flux
Motor Parameter > Rotor inertia[kgm <sup>2</sup> ]	Manual Entry	0.0000028F	Rotor inertia
Name	Name must be a valid C symbol	g_motor_angle0	Module name.
Openloop damping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Enable	Openloop damping functionally enable or disable
Natural frequency of BEMF observer	Manual Entry	1000.0F	Natural frequency of BEMF observer
Damping ratio of BEMF observer	Manual Entry	1.0F	Damping ratio of BEMF observer
Natural frequency of PLL Speed estimate loop	Manual Entry	20.0F	Natural frequency of PLL Speed estimate loop
Damping ratio of PLL Speed estimate loop	Manual Entry	1.0F	Damping ratio of PLL Speed estimate loop
Control period	Manual Entry	0.00005F	Control period

## Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

Developers should be aware of the following limitations when using the Motor Angle and Speed Estimation:

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Angle and Speed Estimation in an application.

```
void motor_estimate_basic_example (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    motor_angle_current_t  smpl_current;
    motor_angle_voltage_reference_t  smpl_voltage;
    /* Initializes the module. */
    err = RM_MOTOR_ESTIMATE_Open(&g_mtr_angle0_ctrl, &g_mtr_angle_set0_cfg);
    assert(FSP_SUCCESS == err);
    /* Basically run this module at A/D conversion finish interrupt.
     * This implementation is an example. */
    while (true)
    {
        /* Application work here. */
        /* Set PI Control Flag before get Angle/Speed and Estimated Component */
        (void) RM_MOTOR_ESTIMATE_FlagPiCtrlSet(&g_mtr_angle0_ctrl, 1U);
        smpl_current.id = 1.0F;
        smpl_current.iq = 1.0F;
        smpl_voltage.vd = 10.0F;
        smpl_voltage.vq = 10.0F;
        /* Set Current and Speed data before get Angle/Speed and Estimated Component */
        (void) RM_MOTOR_ESTIMATE_CurrentSet(&g_mtr_angle0_ctrl, smpl_current,
smpl_voltage);
    }
}
```

```

/* Set Internal Speed Reference & damping speed data before get Angle/Speed and
Estimated Component */
    (void) RM_MOTOR_ESTIMATE_SpeedSet(&g_mtr_angle0_ctrl, 104.27F, 10.0F);
/* Get Angle/Speed data */
    (void) RM_MOTOR_ESTIMATE_AngleSpeedGet(&g_mtr_angle0_ctrl, &f_get_angle,
&f_get_speed, &f_get_phase_err);
/* Get Estimated Component */
    (void) RM_MOTOR_ESTIMATE_EstimatedComponentGet(&g_mtr_angle0_ctrl, &f_get_ed,
&f_get_eq);
}
}

```

## Function Documentation

### ◆ RM\_MOTOR\_ESTIMATE\_Open()

```
fsp_err_t RM_MOTOR_ESTIMATE_Open ( motor_angle_ctrl_t*const p_ctrl, motor_angle_cfg_t const
*const p_cfg )
```

Opens and configures the Angle Estimation module. Implements [motor\\_angle\\_api\\_t::open](#).

#### Return values

FSP_SUCCESS	MTR_ANGL_EST successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

### ◆ RM\_MOTOR\_ESTIMATE\_Close()

```
fsp_err_t RM_MOTOR_ESTIMATE_Close ( motor_angle_ctrl_t*const p_ctrl)
```

Disables specified Angle Estimation module. Implements [motor\\_angle\\_api\\_t::close](#).

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_Reset()**

```
fsp_err_t RM_MOTOR_ESTIMATE_Reset ( motor_angle_ctrl_t *const p_ctrl)
```

Reset variables of Angle Estimation module. Implements `motor_angle_api_t::reset`.

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_CurrentSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_CurrentSet ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage )
```

Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`.

**Return values**

FSP_SUCCESS	Successfully set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_SpeedSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_SpeedSet ( motor_angle_ctrl_t *const p_ctrl, float const
speed_ctrl, float const damp_speed )
```

Set Speed Information. Implements `motor_angle_api_t::speedSet`.

**Return values**

FSP_SUCCESS	Successfully set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_FlagPiCtrlSet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_FlagPiCtrlSet ( motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi )
```

Set the flag of PI Control runs. Implements `motor_angle_api_t::flagPiCtrlSet`.

**Return values**

FSP_SUCCESS	Successfully set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_AngleSpeedGet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_AngleSpeedGet ( motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err )
```

Gets the current rotor's angle and rotation speed. Implements `motor_angle_api_t::angleSpeedGet`.

**Return values**

FSP_SUCCESS	Successful data get.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_EstimatedComponentGet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_EstimatedComponentGet ( motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq )
```

Gets estimated d/q-axis component. Implements `motor_angle_api_t::estimatedComponentGet`.

**Return values**

FSP_SUCCESS	Successfully data gotten.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_ESTIMATE_ParameterUpdate ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_cfg_t const *const p_cfg )
```

Update the parameters of Angle&Speed Estimation. Implements `motor_angle_api_t::parameterUpdate`.

**Return values**

FSP_SUCCESS	Successfully data is update.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_InternalCalculate()**

```
fsp_err_t RM_MOTOR_ESTIMATE_InternalCalculate ( motor_angle_ctrl_t *const p_ctrl)
```

Calculate internal parameters. Implements `motor_angle_api_t::internalCalculate`.

**Return values**

FSP_ERR_UNSUPPORTED	Unsupported.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_AngleAdjust()**

```
fsp_err_t RM_MOTOR_ESTIMATE_AngleAdjust ( motor_angle_ctrl_t *const p_ctrl)
```

Angle Adjustment Process. Implements `motor_angle_api_t::angleAdjust`.

**Return values**

FSP_ERR_UNSUPPORTED	Unsupported.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_EncoderCyclic()**

```
fsp_err_t RM_MOTOR_ESTIMATE_EncoderCyclic ( motor_angle_ctrl_t *const p_ctrl)
```

Encoder Cyclic Process (Call in cyclic timer). Implements [motor\\_angle\\_api\\_t::encoderCyclic](#).

**Return values**

FSP_ERR_UNSUPPORTED	Unsupported.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_ESTIMATE\_InfoGet()**

```
fsp_err_t RM_MOTOR_ESTIMATE_InfoGet ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_encoder_info_t *const p_info )
```

Gets information of Encoder Angle Module. Implements [motor\\_angle\\_api\\_t::infoGet](#).

**Return values**

FSP_ERR_UNSUPPORTED	Unsupported.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

**4.2.89 Motor Position (rm\_motor\_position)**

## Modules

**Functions**

```
fsp_err_t RM_MOTOR_POSITION_Open (motor_position_ctrl_t *const p_ctrl,
motor_position_cfg_t const *const p_cfg)
```

Opens and configures the Motor Position Module. Implements [motor\\_position\\_api\\_t::open](#). [More...](#)

```
fsp_err_t RM_MOTOR_POSITION_Close (motor_position_ctrl_t *const p_ctrl)
```

Disables specified Motor Position Module. Implements [motor\\_position\\_api\\_t::close](#). [More...](#)

```
fsp_err_t RM_MOTOR_POSITION_Reset (motor_position_ctrl_t *const p_ctrl)
```

Reset the variables of Motor Position Module. Implements [motor\\_position\\_api\\_t::reset](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_PositionGet](#) (`motor_position_ctrl_t *const p_ctrl, int16_t *const p_position`)

Get Rotor Position Data [degree]. Implements [motor\\_position\\_api\\_t::positionGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_PositionSet](#) (`motor_position_ctrl_t *const p_ctrl, float const position_rad`)

Set Position Data from Encoder [radian]. Implements [motor\\_position\\_api\\_t::positionSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_PositionReferenceSet](#) (`motor_position_ctrl_t *const p_ctrl, int16_t const position_reference_deg`)

Set Position Reference Data [degree]. Implements [motor\\_position\\_api\\_t::positionReferenceSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_ControlModeSet](#) (`motor_position_ctrl_t *const p_ctrl, motor_position_ctrl_mode_t const mode`)

Set Position Control Mode. Implements [motor\\_position\\_api\\_t::controlModeSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_PositionControl](#) (`motor_position_ctrl_t *const p_ctrl`)

Calculates internal position reference.(Main process of Position Control) Implements [motor\\_position\\_api\\_t::positionControl](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_IpdSpeedPControl](#) (`motor_position_ctrl_t *const p_ctrl, float const ref_speed_rad, float const speed_rad, float *const p_iq_ref`)

Calculates the q-axis current reference by P control. Implements [motor\\_position\\_api\\_t::ipdSpeedPControl](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_SpeedReferencePControlGet](#) (`motor_position_ctrl_t *const p_ctrl, float *const p_speed_ref`)

Get Speed Reference by P Control. Implements [motor\\_position\\_api\\_t::speedReferencePControlGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_POSITION\\_SpeedReferenceIpdControlGet](#)

(motor\_position\_ctrl\_t \*const p\_ctrl, float const max\_speed\_rad, float \*const p\_speed\_ref)

Get Speed Reference by IPD Control. Implements [motor\\_position\\_api\\_t::speedReferenceIpdControlGet](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_POSITION\_SpeedReferenceFeedforwardGet (motor\_position\_ctrl\_t \*const p\_ctrl, float \*const p\_speed\_ref)

Get Speed Reference by Feedforward. Implements [motor\\_position\\_api\\_t::speedReferenceFeedforwardGet](#). [More...](#)

fsp\_err\_t RM\_MOTOR\_POSITION\_ParameterUpdate (motor\_position\_ctrl\_t \*const p\_ctrl, motor\_position\_cfg\_t const \*const p\_cfg)

Update the parameters of Position Control Calculation. Implements [motor\\_position\\_api\\_t::parameterUpdate](#). [More...](#)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor position Interface](#).

## Overview

The motor position is used to control the position of motor rotor in an application. This module should be called cyclically in an application (e.g. in cyclic timer interrupt). This module calculates speed reference with inputted position reference and current rotational speed.

### Features

The Motor Position Module has below features.

- Calculate speed reference.

## Configuration

### Build Time Configurations for rm\_motor\_position

The following build time configurations are defined in fsp\_cfg/rm\_motor\_position\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Position Controller on rm\_motor\_position

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Position

Controller on rm\_motor\_position.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_position0	Module name.
General > Position Dead Band	Manual Entry	1U	Ignored Area of Position Control.
General > Position Band Limit	Manual Entry	3U	Ignored Area of Position Control.
General > Speed Feedforward Ratio	Manual Entry	0.8F	Speed Feedforward Ratio.
General > Encoder Counts per one rotation	Manual Entry	1200.0F	Encoder Counts per one rotation.
General > Position Omega	Manual Entry	10.0F	Position Control Omega.
General > Period of Speed Control[sec]	Manual Entry	0.0005F	Period of Speed Control.
IPD > IPD LPF	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>	Disable	IPD LPF process enable or disable
IPD > Position Kp ratio	Manual Entry	0.3F	Position Kp ratio.
IPD > Position Feedforward ratio	Manual Entry	0.0F	Position Feedforward ratio.
IPD > Speed K ratio	Manual Entry	2.0F	Speed K ratio
IPD > Error Limit #1	Manual Entry	10.0F	Error Limitation #1
IPD > Error Limit #2	Manual Entry	0.2F	Error Limitation #2
IPD > LPF Omega	Manual Entry	500.0F	LPF Omega.
IPD > LPF Zeta	Manual Entry	1.0F	LPF Zeta.
Position Profiling > Interval Time	Manual Entry	400U	Interval Time.
Position Profiling > Accel Time	Manual Entry	0.3F	Accel Time.
Position Profiling > Maximum Accel Time	Manual Entry	8117.96F	Maximum Acceleration Time [sec]
Position Profiling > Acceleration Maximum Speed	Manual Entry	2000.0F	Acceleration Maximum Speed.
Position Profiling > Update Step of Timer	Manual Entry	0.0005F	Update Step of Timer.
Motor Parameter > Pole Pair	Manual Entry	7	Pole Pair
Motor Parameter >	Manual Entry	0.453F	Resistance

Resistance[ohm]

Motor Parameter > Inductance of d-axis[H]	Manual Entry	0.0009447F	Inductance of d-axis
--	--------------	------------	----------------------

Motor Parameter > Inductance of q-axis[H]	Manual Entry	0.0009447F	Inductance of q-axis
--	--------------	------------	----------------------

Motor Parameter > Inertia[kgm^2]	Manual Entry	0.006198F	Inertia
-------------------------------------	--------------	-----------	---------

Motor Parameter > Motor Inertia[kgm^2]	Manual Entry	0.00000962F	Motor Inertia
---	--------------	-------------	---------------

## Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Limitations

- Set the period of speed control with non-negative value.
- Set the limit of speed change step with non-negative value.
- Set the maximum speed with non-negative value.

# Examples

## Basic Example

This is a basic example of using the Motor Position module in an application.

```
void motor_position_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = RM_MOTOR_POSITION_Open(g_motor_position0.p_ctrl, g_motor_position0.p_cfg);
    handle_error(err);

    /* Set working mode */
    RM_MOTOR_POSITION_ModeSet(g_motor_position0.p_ctrl,
MOTOR_POSITION_CTRL_MODE_STEP);

    /* Set position reference */
    RM_MOTOR_POSITION_PositionReferenceSet(g_motor_position0.p_ctrl, 180U);

    /* Basically run this module at cyclic interrupt (e.g. AGT timer).
```

```

* This implementation is an example. */
// while (true)
{
/* Application work here. */
/* Perform Position Control Process */
RM_MOTOR_POSITION_PositionControl(g_motor_position0.p_ctrl);
/* Perform Speed IPD Control Process */
RM_MOTOR_POSITION_IpdSpeedPControl(g_motor_position0.p_ctrl, 0.0F, 0.0F,
&temp_iq_ref);
/* Get Position */
RM_MOTOR_POSITION_PositionGet(g_motor_position0.p_ctrl, &temp_position);
/* Update parameters */
RM_MOTOR_POSITION_ParameterUpdate(g_motor_position0.p_ctrl,
&g_motor_position0.p_cfg);
}
/* Reset Speed Control */
RM_MOTOR_POSITION_Reset(g_motor_position0.p_ctrl);
/* Close Speed Control */
RM_MOTOR_POSITION_Close(g_motor_position0.p_ctrl);
}

```

## Enumerations

```
enum motor_position_ipd_lpf_t
```

## Enumeration Type Documentation

### ◆ motor\_position\_ipd\_lpf\_t

enum motor_position_ipd_lpf_t	
Enumerator	
MOTOR_POSITION_IPD_LPF_DISABLE	ipd control is disabled
MOTOR_POSITION_IPD_LPF_ENABLE	ipd control is enabled

## Function Documentation

◆ **RM\_MOTOR\_POSITION\_Open()**

```
fsp_err_t RM_MOTOR_POSITION_Open ( motor_position_ctrl_t *const p_ctrl, motor_position_cfg_t
const *const p_cfg )
```

Opens and configures the Motor Position Module. Implements [motor\\_position\\_api\\_t::open](#).

**Return values**

FSP_SUCCESS	Motor Position Module successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Set parameter is invalid.

◆ **RM\_MOTOR\_POSITION\_Close()**

```
fsp_err_t RM_MOTOR_POSITION_Close ( motor_position_ctrl_t *const p_ctrl)
```

Disables specified Motor Position Module. Implements [motor\\_position\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_Reset()**

```
fsp_err_t RM_MOTOR_POSITION_Reset ( motor_position_ctrl_t *const p_ctrl)
```

Reset the variables of Motor Position Module. Implements [motor\\_position\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_PositionGet()**

```
fsp_err_t RM_MOTOR_POSITION_PositionGet ( motor_position_ctrl_t *const p_ctrl, int16_t *const p_position )
```

Get Rotor Position Data [degree]. Implements `motor_position_api_t::positionGet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_POSITION\_PositionSet()**

```
fsp_err_t RM_MOTOR_POSITION_PositionSet ( motor_position_ctrl_t *const p_ctrl, float const position_rad )
```

Set Position Data from Encoder [radian]. Implements `motor_position_api_t::positionSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_PositionReferenceSet()**

```
fsp_err_t RM_MOTOR_POSITION_PositionReferenceSet ( motor_position_ctrl_t *const p_ctrl, int16_t const position_reference_deg )
```

Set Position Reference Data [degree]. Implements `motor_position_api_t::positionReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_ControlModeSet()**

```
fsp_err_t RM_MOTOR_POSITION_ControlModeSet ( motor_position_ctrl_t *const p_ctrl,
motor_position_ctrl_mode_t const mode )
```

Set Position Control Mode. Implements [motor\\_position\\_api\\_t::controlModeSet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_PositionControl()**

```
fsp_err_t RM_MOTOR_POSITION_PositionControl ( motor_position_ctrl_t *const p_ctrl)
```

Calculates internal position reference.(Main process of Position Control) Implements [motor\\_position\\_api\\_t::positionControl](#).

**Return values**

FSP_SUCCESS	Successful data calculation.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_POSITION\_IpdSpeedPControl()**

```
fsp_err_t RM_MOTOR_POSITION_IpdSpeedPControl ( motor_position_ctrl_t *const p_ctrl, float const
ref_speed_rad, float const speed_rad, float *const p_iq_ref )
```

Calculates the q-axis current reference by P control. Implements [motor\\_position\\_api\\_t::ipdSpeedPControl](#).

**Return values**

FSP_SUCCESS	Successful data calculation.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_POSITION\_SpeedReferencePControlGet()**

```
fsp_err_t RM_MOTOR_POSITION_SpeedReferencePControlGet ( motor_position_ctrl_t *const p_ctrl,
float *const p_speed_ref )
```

Get Speed Reference by P Control. Implements [motor\\_position\\_api\\_t::speedReferencePControlGet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_POSITION\_SpeedReferenceIpdControlGet()**

```
fsp_err_t RM_MOTOR_POSITION_SpeedReferenceIpdControlGet ( motor_position_ctrl_t *const p_ctrl,
float const max_speed_rad, float *const p_speed_ref )
```

Get Speed Reference by IPD Control. Implements [motor\\_position\\_api\\_t::speedReferenceIpdControlGet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_POSITION\_SpeedReferenceFeedforwardGet()**

```
fsp_err_t RM_MOTOR_POSITION_SpeedReferenceFeedforwardGet ( motor_position_ctrl_t *const
p_ctrl, float *const p_speed_ref )
```

Get Speed Reference by Feedforward. Implements [motor\\_position\\_api\\_t::speedReferenceFeedforwardGet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

### ◆ RM\_MOTOR\_POSITION\_ParameterUpdate()

```
fsp_err_t RM_MOTOR_POSITION_ParameterUpdate ( motor_position_ctrl_t *const p_ctrl,
motor_position_cfg_t const *const p_cfg )
```

Update the parameters of Position Control Calculation. Implements [motor\\_position\\_api\\_t::parameterUpdate](#).

#### Return values

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

## 4.2.90 Motor Angle and Speed Calculation with an Encoder (rm\_motor\_sense\_encoder)

Modules

### Functions

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Open (motor_angle_ctrl_t *const
p_ctrl, motor_angle_cfg_t const *const p_cfg)
```

Opens and configures the Angle Encoder module. Implements [motor\\_angle\\_api\\_t::open](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Close (motor_angle_ctrl_t *const
p_ctrl)
```

Disables specified Angle Encoder module. Implements [motor\\_angle\\_api\\_t::close](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Reset (motor_angle_ctrl_t *const
p_ctrl)
```

Reset variables of Angle Encoder module. Implements [motor\\_angle\\_api\\_t::reset](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_InternalCalculate (motor_angle_ctrl_t
*const p_ctrl)
```

Calculate internal parameters. Implements [motor\\_angle\\_api\\_t::internalCalculate](#). [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_AngleSpeedGet (motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)`

Gets the current rotor's angle and rotation speed. Implements `motor_angle_api_t::angleSpeedGet`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_AngleAdjust (motor_angle_ctrl_t *const p_ctrl)`

Angle Adjustment Process. Implements `motor_angle_api_t::angleAdjust`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_EncoderCyclic (motor_angle_ctrl_t *const p_ctrl)`

Encoder Cyclic Process (Call in cyclic timer). Implements `motor_angle_api_t::encoderCyclic`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_InfoGet (motor_angle_ctrl_t *const p_ctrl, motor_angle_encoder_info_t *const p_info)`

Gets information of Encoder Angle Module. Implements `motor_angle_api_t::infoGet`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_ParameterUpdate (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)`

Update the parameters of Angle&Speed calculation with an encoder. Implements `motor_angle_api_t::parameterUpdate`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_CurrentSet (motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)`

Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_SpeedSet (motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)`

Set Speed Information. Implements `motor_angle_api_t::speedSet`. [More...](#)

`fsp_err_t RM_MOTOR_SENSE_ENCODER_FlagPiCtrlSet (motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)`

Set the flag of PI Control runs. Implements

[motor\\_angle\\_api\\_t::flagPiCtrlSet. More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSE\\_ENCODER\\_EstimatedComponentGet](#)  
(`motor_angle_ctrl_t *const p_ctrl`, `float *const p_ed`, `float *const p_eq`)

Gets estimated d/q-axis component. Implements [motor\\_angle\\_api\\_t::estimatedComponentGet. More...](#)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor angle Interface](#).

## Overview

The motor angle and speed calculation with an encoder module is used to calculate rotor angle and rotational speed in an application. This module is designed to be used with the motor current module (`rm_motor_current`).

## Features

The motor angle and speed calculation with an encoder module has the features listed below.

- Calculate rotor angle [radian].
- Calculate rotational speed [radian/second].

## Configuration

### Build Time Configurations for `rm_motor_sense_encoder`

The following build time configurations are defined in `fsp_cfg/rm_motor_sense_encoder_cfg.h`:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor Angle Driver on `rm_motor_sense_encoder`

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Angle Driver on `rm_motor_sense_encoder`.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	<code>g_motor_sense_encode</code> <code>r0</code>	Module name.
Motor Parameter > Pole pairs	Must be a valid non-negative value.	7	Pole pairs

Motor Parameter > Resistance (ohm)	Must be a valid non-negative value.	0.453F	Resistance
Motor Parameter > Inductance of d-axis (H)	Must be a valid non-negative value.	0.0009447F	Inductance of d-axis
Motor Parameter > Inductance of q-axis (H)	Must be a valid non-negative value.	0.0009447F	Inductance of q-axis
Motor Parameter > Permanent magnetic flux (Wb)	Must be a valid non-negative value.	0.006198F	Permanent magnetic flux
Motor Parameter > Rotor inertia (kgm <sup>2</sup> )	Must be a valid non-negative value.	0.00000962F	Rotor inertia
Control Type	<ul style="list-style-type: none"> <li>• Speed</li> <li>• Position</li> </ul>	Position	Select control Type
Period of Current control (kHz)	Must be a valid non-negative value.	20.0F	Period of Current control
Period of Speed control (sec)	Must be a valid non-negative value.	0.0005F	Period of Speed control
PWM Carrier Frequency (kHz)	Must be a valid non-negative value.	20.0F	PWM Carrier Frequency
Decimation of Interrupt	Manual Entry	0U	Decimation of Interrupt
Counts per Rotation	Must be a valid non-negative value.	1200U	Encoder Counts per One Rotation
Counts for Angle Adjust	Must be a valid non-negative value.	512U	Counts for Angle Adjust (as working time)
Zero speed counts	Must be a valid non-negative value.	20000000U	Threshold counts to judge zero speed
Occupancy Time	Must be a valid non-negative value.	0.30F	Occupancy time of carrier interrupt
Carrier Time	Must be a valid non-negative value.	0.000013F	Processing time of carrier interrupt
Process Time	Must be a valid non-negative value.	0.000001F	Processing time of encoder interrupt
Highspeed Change Margin (rpm)	Must be a valid non-negative value.	150U	Margin of toggle speed for high speed mode
LPF parameter for Highspeed Filter	Must be a valid non-negative value.	0.1F	Highspeed mode speed LPF parameter
Counts to change speed	Must be a valid non-negative value.	8U	Counts for mode change of position speed calculation

## Clock Configuration

## Pin Configuration

# Usage Notes

## Limitations

Developers should be aware of the following limitations when using the motor angle and speed calculation with an encoder: all configurations should be set as positive values.

# Examples

## Basic Example

This is a basic example of minimal use of the motor angle and speed calculation with an encoder in an application.

```
void motor_sense_encoder_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_SENSE_ENCODER_Open(&g_mtr_angle0_ctrl, &g_mtr_angle_set0_cfg);
    assert(FSP_SUCCESS == err);
    /* Basically run this module at A/D conversion finish interrupt.
     * This implementation is an example. */
    // while (true)
    {
        /* Application work here. */
        /* Initialize motor with the encoder */
        (void) RM_MOTOR_SENSE_ENCODER_AngleAdjust(&g_mtr_angle0_ctrl);
        /* Perform cyclic encoder process*/
        (void) RM_MOTOR_SENSE_ENCODER_EncoderCyclic(&g_mtr_angle0_ctrl);
        /* Calculate information with encoder signal input */
        (void) RM_MOTOR_SENSE_ENCODER_InternalCalculate(&g_mtr_angle0_ctrl);
        /* Get angle/speed data */
        (void) RM_MOTOR_SENSE_ENCODER_AngleSpeedGet(&g_mtr_angle0_ctrl, &f_get_angle,
        &f_get_speed, &f_get_phase_err);
        /* Get calculated component */
        (void) RM_MOTOR_SENSE_ENCODER_InfoGet(&g_mtr_angle0_ctrl, &temp_info);
    }
    /* Reset the module */
}
```

```

(void) RM_MOTOR_SENSE_ENCODER_Reset(&g_mtr_angle0_ctrl);
/* Close the module */
(void) RM_MOTOR_SENSE_ENCODER_Close(&g_mtr_angle0_ctrl);
}

```

## Enumerations

```
enum motor_sense_encoder_loop_t
```

```
enum motor_sense_encoder_mode_t
```

## Enumeration Type Documentation

### ◆ motor\_sense\_encoder\_loop\_t

enum motor_sense_encoder_loop_t	
Enumerator	
MOTOR_SENSE_ENCODER_LOOP_SPEED	Speed control mode.
MOTOR_SENSE_ENCODER_LOOP_POSITION	Position control mode.

### ◆ motor\_sense\_encoder\_mode\_t

enum motor_sense_encoder_mode_t	
Enumerator	
MOTOR_SENSE_ENCODER_MODE_INIT	Initialize mode (Start status)
MOTOR_SENSE_ENCODER_MODE_BOOT	Boot mode (Angle adjustment status)
MOTOR_SENSE_ENCODER_MODE_DRIVE	Drive mode (Normal work status)

## Function Documentation

◆ **RM\_MOTOR\_SENSE\_ENCODER\_Open()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Open ( motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t
const *const p_cfg )
```

Opens and configures the Angle Encoder module. Implements [motor\\_angle\\_api\\_t::open](#).

**Return values**

FSP_SUCCESS	Angle Encoder module successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_Close()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Close ( motor_angle_ctrl_t *const p_ctrl)
```

Disables specified Angle Encoder module. Implements [motor\\_angle\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_Reset()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_Reset ( motor_angle_ctrl_t *const p_ctrl)
```

Reset variables of Angle Encoder module. Implements [motor\\_angle\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_InternalCalculate()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_InternalCalculate ( motor_angle_ctrl_t *const p_ctrl)
```

Calculate internal parameters. Implements `motor_angle_api_t::internalCalculate`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_AngleSpeedGet()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_AngleSpeedGet ( motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err )
```

Gets the current rotor's angle and rotation speed. Implements `motor_angle_api_t::angleSpeedGet`.

**Return values**

FSP_SUCCESS	Successfully data calculated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_AngleAdjust()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_AngleAdjust ( motor_angle_ctrl_t *const p_ctrl)
```

Angle Adjustment Process. Implements `motor_angle_api_t::angleAdjust`.

**Return values**

FSP_SUCCESS	Successfully data calculated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_EncoderCyclic()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_EncoderCyclic ( motor_angle_ctrl_t *const p_ctrl)
```

Encoder Cyclic Process (Call in cyclic timer). Implements `motor_angle_api_t::encoderCyclic`.

**Return values**

FSP_SUCCESS	Successfully data calculated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_InfoGet()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_InfoGet ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_encoder_info_t *const p_info )
```

Gets information of Encoder Angle Module. Implements `motor_angle_api_t::infoGet`.

**Return values**

FSP_SUCCESS	Successfully data calculated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_ParameterUpdate ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_cfg_t const *const p_cfg )
```

Update the parameters of Angle&Speed calculation with an encoder. Implements `motor_angle_api_t::parameterUpdate`.

**Return values**

FSP_SUCCESS	Successfully data is update.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SENSE\_ENCODER\_CurrentSet()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_CurrentSet ( motor_angle_ctrl_t *const p_ctrl,
motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage
)
```

Set d/q-axis Current Data & Voltage Reference. Implements `motor_angle_api_t::currentSet`.

**Return values**

FSP_ERR_UNSUPPORTED	Motor sense encoder software currentSet is not supported.
---------------------	---

◆ **RM\_MOTOR\_SENSE\_ENCODER\_SpeedSet()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_SpeedSet ( motor_angle_ctrl_t *const p_ctrl, float const
speed_ctrl, float const damp_speed )
```

Set Speed Information. Implements `motor_angle_api_t::speedSet`.

**Return values**

FSP_ERR_UNSUPPORTED	Motor sense encoder software speedSet is not supported.
---------------------	---

◆ **RM\_MOTOR\_SENSE\_ENCODER\_FlagPiCtrlSet()**

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_FlagPiCtrlSet ( motor_angle_ctrl_t *const p_ctrl, uint32_t
const flag_pi )
```

Set the flag of PI Control runs. Implements `motor_angle_api_t::flagPiCtrlSet`.

**Return values**

FSP_ERR_UNSUPPORTED	Motor sense encoder software flagPiCtrlSet is not supported.
---------------------	--

### ◆ RM\_MOTOR\_SENSE\_ENCODER\_EstimatedComponentGet()

```
fsp_err_t RM_MOTOR_SENSE_ENCODER_EstimatedComponentGet ( motor_angle_ctrl_t *const
p_ctrl, float *const p_ed, float *const p_eq )
```

Gets estimated d/q-axis component. Implements [motor\\_angle\\_api\\_t::estimatedComponentGet](#).

#### Return values

FSP_ERR_UNSUPPORTED	Motor sense encoder software estimatedComponentGet is not supported.
---------------------	--

## 4.2.91 Motor Sensorless Vector Control (rm\_motor\_sensorless)

### Modules

#### Functions

```
fsp_err_t RM_MOTOR_SENSORLESS_Open (motor_ctrl_t *const p_ctrl,
motor_cfg_t const *const p_cfg)
```

```
fsp_err_t RM_MOTOR_SENSORLESS_Close (motor_ctrl_t *const p_ctrl)
```

Disables specified Motor Sensorless Control block. Implements [motor\\_api\\_t::close](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSORLESS_Run (motor_ctrl_t *const p_ctrl)
```

Run Motor (Start motor rotation). Implements [motor\\_api\\_t::run](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSORLESS_Stop (motor_ctrl_t *const p_ctrl)
```

Stop Motor (Stop motor rotation). Implements [motor\\_api\\_t::stop](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSORLESS_Reset (motor_ctrl_t *const p_ctrl)
```

Reset Motor Sensorless Control block. Implements [motor\\_api\\_t::reset](#). [More...](#)

```
fsp_err_t RM_MOTOR_SENSORLESS_ErrorSet (motor_ctrl_t *const p_ctrl,
motor_error_t const error)
```

Set error information. Implements [motor\\_api\\_t::errorSet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_SpeedSet](#) (`motor_ctrl_t *const p_ctrl`, `float const speed_rpm`)

Set speed reference[rpm]. Implements [motor\\_api\\_t::speedSet](#).  
[More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_StatusGet](#) (`motor_ctrl_t *const p_ctrl`, `uint8_t *const p_status`)

Get current control status. Implements [motor\\_api\\_t::statusGet](#).  
[More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_AngleGet](#) (`motor_ctrl_t *const p_ctrl`, `float *const p_angle_rad`)

Get current rotor angle. Implements [motor\\_api\\_t::angleGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_SpeedGet](#) (`motor_ctrl_t *const p_ctrl`, `float *const p_speed_rpm`)

Get rotational speed. Implements [motor\\_api\\_t::speedGet](#). [More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_ErrorCheck](#) (`motor_ctrl_t *const p_ctrl`, `uint16_t *const p_error`)

Check the occurrence of Error. Implements [motor\\_api\\_t::errorCheck](#).  
[More...](#)

`fsp_err_t` [RM\\_MOTOR\\_SENSORLESS\\_PositionSet](#) (`motor_ctrl_t *const p_ctrl`, `motor_speed_position_data_t const *const p_position`)

Set position reference. Implements [motor\\_api\\_t::positionSet](#). [More...](#)

## Detailed Description

Usual control of a SPM motor on RA MCUs. This module implements the [Motor Sensorless Vector Control \(rm\\_motor\\_sensorless\)](#).

## Overview

The motor sensorless vector control is used to control a motor rotation in an application. This module is implemented with using SPM motor. User can start/stop motor rotation simply.

## Features

The Motor Sensorless Module has below features.

- Start/Stop a motor rotation
- Error detection (over current, over speed, over voltage, low voltage)

## Configuration

### Build Time Configurations for rm\_motor\_sensorless

The following build time configurations are defined in fsp\_cfg/rm\_motor\_sensorless\_cfg.h:

Configuration	Options	Default	Description
Parameter checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Configurations for Middleware > Motor > Motor sensorless vector control

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor sensorless vector control.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_sensorless0	Module name.
General > Limit of over current (A)	Manual Entry	0.42F	Limit of over current.(Detection threshold)
General > Limit of over voltage (V)	Manual Entry	28.0F	Limit of over voltage.(Detection threshold)
General > Limit of over speed (rpm)	Manual Entry	3000.0F	Limit of over speed.(Detection threshold)
General > Limit of low voltage (V)	Manual Entry	14.0F	Limit of low voltage.(Detection threshold)
Interrupts > Callback	Name must be a valid C symbol	NULL	A user callback function. If this callback function is provided, it is called at speed control cyclic interrupt.

### Clock Configuration

This module doesn't depend on clock setting, because this module is a simple status transition process.

### Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Limitations

- Set the limit of electric current with non-negative value.
- Set the limit of input voltage with non-negative value.
- Set the limit of rotational speed with non-negative value.

## Examples

### Basic Example

This is a basic example of minimal use of the Motor Sensorless in an application.

```
void motor_sensorless_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    /* Initializes the module. */
    err = RM_MOTOR_SENSORLESS_Open(g_motor_sensorless0.p_ctrl,
g_motor_sensorless0.p_cfg);
    assert(FSP_SUCCESS == err);
    /* Set speed reference before motor run */
    (void) RM_MOTOR_SENSORLESS_SpeedSet(g_motor_sensorless0.p_ctrl,
DEF_SENSORLESS_TEST_OVSPD_LIM);
    /* Start motor rotation */
    (void) RM_MOTOR_SENSORLESS_Run(g_motor_sensorless0.p_ctrl);
    /* Get current status */
    (void) RM_MOTOR_SENSORLESS_StatusGet(g_motor_sensorless0.p_ctrl, &smpl_status);
    /* Get current rotor angle */
    (void) RM_MOTOR_SENSORLESS_AngleGet(g_motor_sensorless0.p_ctrl, &smpl_angle);
    /* Get current motor speed */
    (void) RM_MOTOR_SENSORLESS_SpeedGet(g_motor_sensorless0.p_ctrl, &smpl_speed);
    /* Check error */
    (void) RM_MOTOR_SENSORLESS_ErrorCheck(g_motor_sensorless0.p_ctrl, &smpl_error);
    /* Stop motor rotation */
    (void) RM_MOTOR_SENSORLESS_Stop(g_motor_sensorless0.p_ctrl);
    /* Stop motor rotation */
    (void) RM_MOTOR_SENSORLESS_ErrorSet(g_motor_sensorless0.p_ctrl,
MOTOR_ERROR_OVER_CURRENT_HW);
}
```

```

/* Reset Speed Control */
(void) RM_MOTOR_SENSORLESS_Reset(g_motor_sensorless0.p_ctrl);
/* Close Speed Control */
(void) RM_MOTOR_SENSORLESS_Close(g_motor_sensorless0.p_ctrl);
}

```

## Data Structures

struct [motor\\_sensorless\\_callback\\_args\\_t](#)

## Enumerations

enum [motor\\_sensorless\\_callback\\_event\\_t](#)

## Data Structure Documentation

### ◆ motor\_sensorless\_callback\_args\_t

struct <a href="#">motor_sensorless_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data.
<a href="#">motor_sensorless_callback_event_t</a>	event	

## Enumeration Type Documentation

### ◆ motor\_sensorless\_callback\_event\_t

enum <a href="#">motor_sensorless_callback_event_t</a>	
Events that can trigger a callback function	
Enumerator	
MOTOR_SENSORLESS_CALLBACK_EVENT_SPEED_FORWARD	Event forward Speed Control.
MOTOR_SENSORLESS_CALLBACK_EVENT_SPEED_BACKWARD	Event backward Speed Control.
MOTOR_SENSORLESS_CALLBACK_EVENT_CURRENT_FORWARD	Event forward Current Control.
MOTOR_SENSORLESS_CALLBACK_EVENT_CURRENT_BACKWARD	Event backward Current Control.

## Function Documentation

### ◆ RM\_MOTOR\_SENSORLESS\_Open()

```
fsp_err_t RM_MOTOR_SENSORLESS_Open ( motor_ctrl_t *const p_ctrl, motor_cfg_t const *const p_cfg )
```

Configure the MOTOR in register start mode. Implements [motor\\_api\\_t::open](#).

This function should only be called once as MOTOR configuration registers can only be written to once so subsequent calls will have no effect.

Example:

```
/* Initializes the module. */
err = RM_MOTOR_SENSORLESS_Open(g_motor_sensorless0.p_ctrl,
g_motor_sensorless0.p_cfg);
```

#### Return values

FSP_SUCCESS	MOTOR successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_Close()

```
fsp_err_t RM_MOTOR_SENSORLESS_Close ( motor_ctrl_t *const p_ctrl)
```

Disables specified Motor Sensorless Control block. Implements [motor\\_api\\_t::close](#).

Example:

```
/* Close Speed Control */
(void) RM_MOTOR_SENSORLESS_Close(g_motor_sensorless0.p_ctrl);
```

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_SENSORLESS\_Run()**

```
fsp_err_t RM_MOTOR_SENSORLESS_Run ( motor_ctrl_t *const p_ctrl)
```

Run Motor (Start motor rotation). Implements [motor\\_api\\_t::run](#).

Example:

```
/* Start motor rotation */
(void) RM_MOTOR_SENSORLESS_Run(g_motor_sensorless0.p_ctrl);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

◆ **RM\_MOTOR\_SENSORLESS\_Stop()**

```
fsp_err_t RM_MOTOR_SENSORLESS_Stop ( motor_ctrl_t *const p_ctrl)
```

Stop Motor (Stop motor rotation). Implements [motor\\_api\\_t::stop](#).

Example:

```
/* Stop motor rotation */
(void) RM_MOTOR_SENSORLESS_Stop(g_motor_sensorless0.p_ctrl);
```

**Return values**

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_Reset()

```
fsp_err_t RM_MOTOR_SENSORLESS_Reset ( motor_ctrl_t *const p_ctrl)
```

Reset Motor Sensorless Control block. Implements `motor_api_t::reset`.

Example:

```
/* Reset Speed Control */
(void) RM_MOTOR_SENSORLESS_Reset(g_motor_sensorless0.p_ctrl);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_ErrorSet()

```
fsp_err_t RM_MOTOR_SENSORLESS_ErrorSet ( motor_ctrl_t *const p_ctrl, motor_error_t const error )
```

Set error information. Implements `motor_api_t::errorSet`.

Example:

```
/* Stop motor rotation */
(void) RM_MOTOR_SENSORLESS_ErrorSet(g_motor_sensorless0.p_ctrl,
MOTOR_ERROR_OVER_CURRENT_HW);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_SpeedSet()

```
fsp_err_t RM_MOTOR_SENSORLESS_SpeedSet ( motor_ctrl_t *const p_ctrl, float const speed_rpm )
```

Set speed reference[rpm]. Implements `motor_api_t::speedSet`.

Example:

```
/* Set speed reference before motor run */
(void) RM_MOTOR_SENSORLESS_SpeedSet(g_motor_sensorless0.p_ctrl,
DEF_SENSORLESS_TEST_OVSPD_LIM);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_StatusGet()

```
fsp_err_t RM_MOTOR_SENSORLESS_StatusGet ( motor_ctrl_t *const p_ctrl, uint8_t *const p_status )
```

Get current control status. Implements `motor_api_t::statusGet`.

Example:

```
/* Get current status */
(void) RM_MOTOR_SENSORLESS_StatusGet(g_motor_sensorless0.p_ctrl, &smpl_status);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_AngleGet()

```
fsp_err_t RM_MOTOR_SENSORLESS_AngleGet ( motor_ctrl_t *const p_ctrl, float *const p_angle_rad )
```

Get current rotor angle. Implements `motor_api_t::angleGet`.

Example:

```
/* Get current rotor angle */
(void) RM_MOTOR_SENSORLESS_AngleGet(g_motor_sensorless0.p_ctrl, &smpl_angle);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_SpeedGet()

```
fsp_err_t RM_MOTOR_SENSORLESS_SpeedGet ( motor_ctrl_t *const p_ctrl, float *const p_speed_rpm )
```

Get rotational speed. Implements `motor_api_t::speedGet`.

Example:

```
/* Get current motor speed */
(void) RM_MOTOR_SENSORLESS_SpeedGet(g_motor_sensorless0.p_ctrl, &smpl_speed);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_ErrorCheck()

```
fsp_err_t RM_MOTOR_SENSORLESS_ErrorCheck ( motor_ctrl_t *const p_ctrl, uint16_t *const p_error )
```

Check the occurrence of Error. Implements `motor_api_t::errorCheck`.

Example:

```
/* Check error */
(void) RM_MOTOR_SENSORLESS_ErrorCheck(g_motor_sensorless0.p_ctrl, &smpl_error);
```

#### Return values

FSP_SUCCESS	Successfully resetted.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Data received pointer is invalid..

*Note*

### ◆ RM\_MOTOR\_SENSORLESS\_PositionSet()

```
fsp_err_t RM_MOTOR_SENSORLESS_PositionSet ( motor_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position )
```

Set position reference. Implements `motor_api_t::positionSet`.

Example:

#### Return values

FSP_ERR_UNSUPPORTED	Unsupported.
---------------------	--------------

*Note*

## 4.2.92 Motor Speed (rm\_motor\_speed)

Modules

### Functions

```
fsp_err_t RM_MOTOR_SPEED_Open (motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)
```

Opens and configures the Motor Speed Module. Implements `motor_speed_api_t::open`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_Close (motor_speed_ctrl_t *const p_ctrl)`  
Disables specified Motor Speed Module. Implements `motor_speed_api_t::close`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_Reset (motor_speed_ctrl_t *const p_ctrl)`  
Reset the variables of Motor Speed Module. Implements `motor_speed_api_t::reset`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_Run (motor_speed_ctrl_t *const p_ctrl)`  
Run(Start) the Motor Speed Control. Implements `motor_speed_api_t::run`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_SpeedReferenceSet (motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm)`  
Set Speed Reference Data. Implements `motor_speed_api_t::speedReferenceSet`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_PositionReferenceSet (motor_speed_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position_data)`  
Set Position Reference Data. Implements `motor_speed_api_t::positionReferenceSet`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_ParameterSet (motor_speed_ctrl_t *const p_ctrl, motor_speed_input_t const *const p_st_input)`  
Set Input parameters. Implements `motor_speed_api_t::parameterSet`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_SpeedControl (motor_speed_ctrl_t *const p_ctrl)`  
Calculates the d/q-axis current reference.(Main process of Speed Control) Implements `motor_speed_api_t::speedControl`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_ParameterGet (motor_speed_ctrl_t *const p_ctrl, motor_speed_output_t *const p_st_output)`  
Get Speed Control Parameters. Implements `motor_speed_api_t::parameterGet`. [More...](#)

`fsp_err_t RM_MOTOR_SPEED_ParameterUpdate (motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)`

Update the parameters of Speed Control Calculation. Implements [motor\\_speed\\_api\\_t::parameterUpdate](#). [More...](#)

## Detailed Description

Calculation process for the motor control on RA MCUs. This module implements the [Motor speed Interface](#).

## Overview

The motor speed is used to control the speed of motor rotation in an application. This module should be called cyclically in an application (e.g. in cyclic timer interrupt). This module calculates d/q-axis current reference with input speed reference, current rotational speed, and d/q-axis current.

## Features

The motor speed module has below features.

- Calculate d/q-axis electric current reference.
- Flux weakening process at high speed rotation.
- Open loop damping control when using sensorless type.
- Low pass filter of input rotational speed.
- Speed observer function when using encoder type.

## Configuration

### Build Time Configurations for rm\_motor\_speed

The following build time configurations are defined in fsp\_cfg/rm\_motor\_speed\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Position Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable position algorithm support.

### Configurations for Middleware > Motor > Motor Speed Controller on rm\_motor\_speed

This module can be added to the Stacks tab via New Stack > Middleware > Motor > Motor Speed Controller on rm\_motor\_speed.

Configuration	Options	Default	Description
General > Name	Name must be a valid C symbol	g_motor_speed0	Module name.
General > Speed control period (sec)	Manual Entry	0.0005F	Period of speed control function.
General > Step of	Manual Entry	0.5F	Step of speed change

speed climbing (rpm)				at start of open-loop.
General > Maximum rotational speed (rpm)	Manual Entry		2650	Maximum rotational speed (Limit speed).
General > Speed LPF omega	Manual Entry		10.0F	Design parameter for speed LPF.
General > Speed at Id climbing (rpm)	Manual Entry		500	From this speed d-axis current is controlled climbing.
General > Limit of q-axis current (A)	Manual Entry		0.42F	Limit of q-axis current.
General > Step of speed feedback at open-loop	Manual Entry		0.20F	Step of speed feedback at open-loop.
General > Open-loop damping	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	Select enable/disable Open-loop damping control.
General > Flux weakening	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Disable	Select enable/disable flux weakening control.
General > Torque compensation for sensorless transition	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	Select enable/disable torque compensation for sensorless transition.
General > Speed observer	<ul style="list-style-type: none"> <li>• Disable</li> <li>• Enable</li> </ul>		Enable	Select enable/disable Speed observer process.
General > Control method	<ul style="list-style-type: none"> <li>• PID</li> <li>• IPD</li> </ul>		PID	Select the control method [PID or IPD].
General > Control type	<ul style="list-style-type: none"> <li>• Sensoreless</li> <li>• Encoder</li> </ul>		Sensoreless	
Open-Loop > Step of d-axis current climbing	Manual Entry		0.3F	Step of d-axis current climbing
Open-Loop > Step of d-axis current descending	Manual Entry		0.3F	Step of d-axis current descending
Open-Loop > Step of q-axis current descending ratio	Manual Entry		1.0F	Step of q-axis current descending ratio
Open-Loop > Reference of d-axis current	Manual Entry		0.3F	Reference of d-axis current
Open-Loop > Threshold of speed control descending	Manual Entry		600	When rotational speed reaches this speed, d-axis current is controlled descending.

Open-Loop > Threshold of speed control climbing	Manual Entry	500	Until rotational speed reaches this speed, d-axis current is controlled climbing.
Open-Loop > Period between open-loop to BEMF (sec)	Manual Entry	0.025F	Margin time between open-loop control changes to BEMF PI control.
Open-Loop > Phase error(degree) to decide sensor-less switch timing	Manual Entry	10	Phase error(degree) to decide sensor-less switch timing.
Design parameter > Speed PI loop omega	Manual Entry	5.0F	Speed PI loop omega
Design parameter > Speed PI loop zeta	Manual Entry	1.0F	Speed PI loop zeta
Design parameter > Estimated d-axis HPF omega	Manual Entry	2.5F	HPF cutoff frequency for ed (Hz)
Design parameter > Open-loop damping zeta	Manual Entry	1.0F	Damping ratio of open-loop damping control
Design parameter > Cutoff frequency of phase error LPF	Manual Entry	10.0F	Cutoff frequency of phase error LPF
Design parameter > Speed observer omega	Manual Entry	200.0F	Speed observer loop omega
Design parameter > Speed observer zeta	Manual Entry	1.0F	Speed observer loop zeta
Motor Parameter > Pole pairs	Manual Entry	2	Pole pairs
Motor Parameter > Resistance (ohm)	Manual Entry	8.5F	Resistance
Motor Parameter > Inductance of d-axis (H)	Manual Entry	0.0045F	Inductance of d-axis
Motor Parameter > Inductance of q-axis (H)	Manual Entry	0.0045F	Inductance of q-axis
Motor Parameter > Permanent magnetic flux (Wb)	Manual Entry	0.02159F	Permanent magnetic flux
Motor Parameter > Rotor inertia (kgm <sup>2</sup> )	Manual Entry	0.0000028F	Rotor inertia
Interrupts > Callback	Name must be a valid	NULL	A user callback

	C symbol		function. If this callback function is provided, it is called at timer interrupt.
Interrupts > Input data	Name must be a valid C symbol	NULL	Structure for Speed control Input. If you set this content, Speed Control function read these data automatically. (No need to use Set API.)
Interrupts > Output data	Name must be a valid C symbol	NULL	Structure for Speed control Output. If you set this content, Speed Control function write need data automatically. (No need to use Get API.)

## Clock Configuration

This module doesn't depend on clock setting, because this module is a simple calculation process.

## Pin Configuration

This module does not use I/O pins.

# Usage Notes

## Limitations

- Set the period of speed control with none-negative value.
- Set the limit of speed change step with none-negative value.
- Set the maximum speed with none-negative value.

# Examples

## Basic Example

This is a basic example of minimal use of the motor speed in an application.

```
void motor_speed_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;

    /* Initializes the module. */
    err = RM_MOTOR_SPEED_Open(g_motor_speed0.p_ctrl, g_motor_speed0.p_cfg);
    handle_error(err);

    /* Set speed reference before get current reference */
}
```

```
(void) RM_MOTOR_SPEED_SpeedReferenceSet(g_motor_speed0.p_ctrl, 104.72F);
/* Set position reference before get current reference
 * (Basically Exclusive to SpeedReferenceSet. This is only sample,) */
(void) RM_MOTOR_SPEED_PositionReferenceSet(g_motor_speed0.p_ctrl,
&g_posref_sample);
/* Basically run this module at cyclic interrupt (e.g. AGT timer).
 * This implementation is an example. */
// while (true)
{
/* Application work here. */
/* Set input parameter data before get current reference */
(void) RM_MOTOR_SPEED_ParameterSet(g_motor_speed0.p_ctrl,
&g_test_speed_input);
/* Activate Speed Process */
(void) RM_MOTOR_SPEED_Run(g_motor_speed0.p_ctrl);
/* Perform Speed Control Process */
(void) RM_MOTOR_SPEED_SpeedControl(g_motor_speed0.p_ctrl);
/* Get output parameters */
(void) RM_MOTOR_SPEED_ParameterGet(g_motor_speed0.p_ctrl,
&g_test_speed_output);
//
/* Update parameters */
(void) RM_MOTOR_SPEED_ParameterUpdate(g_motor_speed0.p_ctrl,
&g_motor_speed0.p_cfg);
}
/* Reset Speed Control */
(void) RM_MOTOR_SPEED_Reset(g_motor_speed0.p_ctrl);
/* Close Speed Control */
(void) RM_MOTOR_SPEED_Close(g_motor_speed0.p_ctrl);
}
```

## Enumerations

```
enum motor_speed_control_type_t
```

enum [motor\\_speed\\_openloop\\_damping\\_t](#)enum [motor\\_speed\\_flux\\_weaken\\_t](#)enum [motor\\_speed\\_less\\_switch\\_t](#)enum [motor\\_speed\\_observer\\_switch\\_t](#)enum [motor\\_speed\\_ctrl\\_status\\_t](#)

## Enumeration Type Documentation

### ◆ motor\_speed\_control\_type\_t

enum <a href="#">motor_speed_control_type_t</a>	
Enumerator	
MOTOR_SPEED_CONTROL_TYPE_SENSORLESS	Sensorless type.
MOTOR_SPEED_CONTROL_TYPE_ENCODER	Encoder type.

### ◆ motor\_speed\_openloop\_damping\_t

enum <a href="#">motor_speed_openloop_damping_t</a>	
Enumerator	
MOTOR_SPEED_OPENLOOP_DAMPING_DISABLE	Disable openloop damping.
MOTOR_SPEED_OPENLOOP_DAMPING_ENABLE	Enable openloop damping.

### ◆ motor\_speed\_flux\_weaken\_t

enum <a href="#">motor_speed_flux_weaken_t</a>	
Enumerator	
MOTOR_SPEED_FLUX_WEAKEN_DISABLE	Disable flux-weakening control.
MOTOR_SPEED_FLUX_WEAKEN_ENABLE	Enable flux-weakening control.

◆ **motor\_speed\_less\_switch\_t**

enum motor_speed_less_switch_t	
Enumerator	
MOTOR_SPEED_LESS_SWITCH_DISABLE	Disable soft switching between open-loop mode and normal FOC mode.
MOTOR_SPEED_LESS_SWITCH_ENABLE	Enable soft switching between open-loop mode and normal FOC mode.

◆ **motor\_speed\_observer\_switch\_t**

enum motor_speed_observer_switch_t	
Enumerator	
MOTOR_SPEED_OBSERVER_SWITCH_DISABLE	Disable speed observer.
MOTOR_SPEED_OBSERVER_SWITCH_ENABLE	Enable speed observer.

◆ **motor\_speed\_ctrl\_status\_t**

enum motor_speed_ctrl_status_t	
Enumerator	
MOTOR_SPEED_CTRL_STATUS_INIT	Speed control status is INIT.
MOTOR_SPEED_CTRL_STATUS_BOOT	Speed control status is BOOT.
MOTOR_SPEED_CTRL_STATUS_RUN	Speed control status is RUN.

**Function Documentation**

◆ **RM\_MOTOR\_SPEED\_Open()**

```
fsp_err_t RM_MOTOR_SPEED_Open ( motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg )
```

Opens and configures the Motor Speed Module. Implements [motor\\_speed\\_api\\_t::open](#).

**Return values**

FSP_SUCCESS	Motor Speed Module successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

◆ **RM\_MOTOR\_SPEED\_Close()**

```
fsp_err_t RM_MOTOR_SPEED_Close ( motor_speed_ctrl_t *const p_ctrl)
```

Disables specified Motor Speed Module. Implements [motor\\_speed\\_api\\_t::close](#).

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_Reset()**

```
fsp_err_t RM_MOTOR_SPEED_Reset ( motor_speed_ctrl_t *const p_ctrl)
```

Reset the variables of Motor Speed Module. Implements [motor\\_speed\\_api\\_t::reset](#).

**Return values**

FSP_SUCCESS	Successfully reset.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_Run()**

```
fsp_err_t RM_MOTOR_SPEED_Run ( motor_speed_ctrl_t *const p_ctrl)
```

Run(Start) the Motor Speed Control. Implements `motor_speed_api_t::run`.

**Return values**

FSP_SUCCESS	Successfully start.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_SpeedReferenceSet()**

```
fsp_err_t RM_MOTOR_SPEED_SpeedReferenceSet ( motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm )
```

Set Speed Reference Data. Implements `motor_speed_api_t::speedReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_PositionReferenceSet()**

```
fsp_err_t RM_MOTOR_SPEED_PositionReferenceSet ( motor_speed_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position_data )
```

Set Position Reference Data. Implements `motor_speed_api_t::positionReferenceSet`.

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Input structure pointer is NULL.

◆ **RM\_MOTOR\_SPEED\_ParameterSet()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterSet ( motor_speed_ctrl_t *const p_ctrl,
motor_speed_input_t const *const p_st_input )
```

Set Input parameters. Implements [motor\\_speed\\_api\\_t::parameterSet](#).

**Return values**

FSP_SUCCESS	Successfully data is set.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

◆ **RM\_MOTOR\_SPEED\_SpeedControl()**

```
fsp_err_t RM_MOTOR_SPEED_SpeedControl ( motor_speed_ctrl_t *const p_ctrl)
```

Calculates the d/q-axis current reference.(Main process of Speed Control) Implements [motor\\_speed\\_api\\_t::speedControl](#).

**Return values**

FSP_SUCCESS	Successful data calculation.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_MOTOR\_SPEED\_ParameterGet()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterGet ( motor_speed_ctrl_t *const p_ctrl,
motor_speed_output_t *const p_st_output )
```

Get Speed Control Parameters. Implements [motor\\_speed\\_api\\_t::parameterGet](#).

**Return values**

FSP_SUCCESS	Successfully the flag is gotten.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Output pointer is NULL.

**◆ RM\_MOTOR\_SPEED\_ParameterUpdate()**

```
fsp_err_t RM_MOTOR_SPEED_ParameterUpdate ( motor_speed_ctrl_t *const p_ctrl,
motor_speed_cfg_t const *const p_cfg )
```

Update the parameters of Speed Control Calculation. Implements [motor\\_speed\\_api\\_t::parameterUpdate](#).

**Return values**

FSP_SUCCESS	Successfully data was updated.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

## 4.2.93 Azure RTOS NetX Secure Crypto Hardware Acceleration (rm\_netx\_secure\_crypto)

[Modules](#)

### Detailed Description

Hardware acceleration for the Netx Crypto implementation of the Microsoft Azure RTOS NetX Crypto API.

## Overview

Please refer to the [NetXDuo - NetX Crypto documentation](#) for further details.

### HW Overview

Crypto Peripheral version	Devices
SCE9	RA6M4, RA4M3, RA4M2, RA6M5
SCE7	RA6M3, RA6M2, RA6M1, RA6T1
SCE5	RA4W1, RA4M1
AES Engine	RA2A1, RA2E1, RA2E2, RA2L1

*Note*

*NetX Crypto hardware acceleration is unsupported on 'SCE5' and 'AES Engine' crypto peripherals listed above.*

### Features

This module provides SCE9 hardware support for the following NetX Crypto operations

- SHA256 calculation
- SHA224 calculation
- MAC Operations
  - HMAC with SHA224
  - HMAC with SHA256
- AES
  - Keybits - 128, 192, 256
    - Encryption and Decryption.
    - Chaining Modes: CBC, CTR, GCM mode

AES Chaining Mode	HW Acceleration
CBC	Fully accelerated
CTR	Only block cipher unit is HW accelerated
GCM	Encrypt - Fully accelerated; Decrypt - Only GHASH and block cipher unit is HW accelerated
CCM	Only block cipher unit is HW accelerated

- Random number generation
- ECC
  - ECDSA: Supported Curves - SECP384R1, SECP256R1, SECP224R1.
  - ECDH: Supported Curves - SECP384R1, SECP256R1, SECP224R1.
- RSA
  - Signature Generation - RSA 2048 (Plain or Wrapped private) key. (This can be used for decryption)
  - Signature Verification - RSA 2048, RSA 3072 and RSA 4096 keys. (This can be used for encryption)
  - Supported encoding scheme: PKCS1V15 This module provides SCE7 hardware support for the following NetX Crypto operations
- AES
  - Keybits - 128, 256
    - Encryption and Decryption.
    - Chaining Modes: CBC, CTR, GCM mode

AES Chaining Mode	HW Acceleration
CBC	Fully accelerated
CTR	Only block cipher unit is HW accelerated
GCM	Only block cipher unit is HW accelerated
CCM	Only block cipher unit is HW accelerated

## Configuration

### Build Time Configurations for rm\_netx\_secure\_crypto\_sw\_port

The following build time configurations are defined in `fsp_cfg/middleware/rm_netx_secure_crypto_cfg.h`:

Configuration	Options	Default	Description
Standalone Usage	<ul style="list-style-type: none"> <li>Use Standalone Crypto Only</li> <li>Use with TLS</li> </ul>	Use Standalone Crypto Only	Defines <code>NX_CRYPTO_STANDALONE_ENABLE</code> .
Maximum RSA Modulus size (bits)	<ul style="list-style-type: none"> <li>1024</li> <li>2048</li> <li>3072</li> <li>4096</li> </ul>	4096	

### Build Time Configurations for `rm_netx_secure_crypto`

The following build time configurations are defined in `fsp_cfg/middleware/rm_netx_secure_crypto_cfg.h`:

Configuration	Options	Default	Description
Hardware Acceleration > Hash > SHA256/224	MCU Specific Options		Enables <code>NETX_SECURE_CRYPTO_NX_CRYPTO_METHODS_SHA256_ALT</code> .
Hardware Acceleration > Cipher > AES	MCU Specific Options		Enables <code>NETX_SECURE_CRYPTO_NX_CRYPTO_METHODS_AES_ALT</code> .
Hardware Acceleration > Public Key Cryptography (PKC) > ECC > ECC	MCU Specific Options		Enables <code>NETX_SECURE_CRYPTO_NX_CRYPTO_METHODS_ECC_ALT</code> .
Hardware Acceleration > Public Key Cryptography (PKC) > ECC > ECDSA Scratch Buffer Size (Bytes)	Value must be an integer	3016	Sets value of <code>NX_CRYPT_TO_ECDSA_SCRATCH_BUFFER_SIZE</code> .
Hardware Acceleration > Public Key Cryptography (PKC) > ECC > ECDH Scratch Buffer Size (Bytes)	Value must be an integer	2464	Sets value of <code>NX_CRYPT_TO_ECDH_SCRATCH_BUFFER_SIZE</code> .
Hardware Acceleration > Public Key Cryptography (PKC) > RSA > RSA	MCU Specific Options		Enables/Disables RSA HW support.
Hardware Acceleration > Public Key Cryptography (PKC) > RSA > RSA 2048 (HW)	MCU Specific Options		Enables <code>NETX_SECURE_CRYPTO_NX_CRYPTO_METHODS_RSA_2048_ALT</code> to allow HW support.
Hardware Acceleration > Public Key	MCU Specific Options		Enables <code>NETX_SECURE_CRYPTO_NX_CRYPTO_M</code> .

Cryptography (PKC) > RSA > RSA 3072 Verify/Encryption (HW)			ETHODS_RSA_3072_ALT to allow HW support
Hardware Acceleration > Public Key Cryptography (PKC) > RSA > RSA 4096 Verify/Encryption (HW)	MCU Specific Options		Enables RSA NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_RSA_4096_ALT to allow HW support
Hardware Acceleration > Public Key Cryptography (PKC) > RSA > RSA Scratch Buffer Size (Bytes)	MCU Specific Options		Sets value of NX_CRYPT_TO_RSA_SCRATCH_BUFFER_SIZE
Hardware Acceleration > TRNG	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Enables NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_TRNG_ALT.
Standalone Usage	<ul style="list-style-type: none"> <li>• Use Standalone Crypto Only</li> <li>• Use with TLS</li> </ul>	Use Standalone Crypto Only	Defines NX_CRYPT_STANDALONE_ENABLE.

## Random Number Generator Configuration

To enable hardware acceleration for the TRNG, the macro `NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_TRNG_ALT` must be defined in the configuration file. By default TRNG is enabled which can be disabled using the RA Configuration editor.

Once enabled 'rand' function will be mapped to HW TRNG; the 'srand' function is not supported, any calls to this function will have no effect. Functionality to re-seed the HW TRNG is not supported by the existing implementation.

If disabled, both 'rand' and 'srand' will be mapped to the C Standard Library. This would require setting up the heap as 'rand' implementation calls 'malloc'.

## SHA256 Configuration

To enable hardware acceleration for the SHA256/224 calculation, the macro `NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_SHA256_ALT` must be defined in the configuration file. By default SHA256 is enabled which can be disabled using the RA Configuration editor.

## AES Configuration

To enable hardware acceleration for the AES128/192/256 operation, the macro `NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_AES_ALT` must be defined in the configuration file. By default AES is enabled which can be disabled using the RA Configuration editor.

## ECC Configuration

To enable hardware acceleration for the ECDSA and ECDH for curves SECP384R1, SECP256R1 and SECP224R1, the macro `NETX_SECURE_CRYPTO_NX_CRYPT_TO_METHODS_ECC_ALT` must be defined in the configuration file. By default ECC operations are enabled which can be disabled using the RA Configuration editor.

## RSA Configuration

To enable hardware acceleration for the RSA Encrypt/Decrypt (or Sign/Verify) operation(s), the macro(s) below must be defined in the configuration file:

Configuration Macro	Feature / Operation
NETX_SECURE_CRYPT0_NX_CRYPT0_METHODS_ RSA_2048_ALT	Signature Generation / Signature Verification (Encryption / Decryption)
NETX_SECURE_CRYPT0_NX_CRYPT0_METHODS_ RSA_3072_ALT	Signature Verification (Encryption Only)
NETX_SECURE_CRYPT0_NX_CRYPT0_METHODS_ RSA_4096_ALT	Signature Verification (Encryption Only)

By default RSA 2048 is enabled which can be disabled using the RA Configuration editor.

RSA software implementation is completely disabled when any of the above macros are enabled.

## Usage Notes

### Memory Alignment

Use 32bit aligned buffer pointers as arguments to APIs for best performance.

### Hardware Initialization

`_nx_crypto_initialize()` must be invoked before using the NetX Crypto APIs to ensure that the SCE peripheral is initialized.

### Memory Usage

Sufficient memory must be allocated to be used as 'crypto\_metadata' for the chosen crypto operation(s). Refer [Azure RTOS NetX Crypto API description](#) for recommended 'crypto\_metadata\_size' based on selected crypto operations. Sufficient amount of memory must be allocated for the thread stack to support low level crypto operations when using this module in the standalone mode or through NetX Secure (TLS). A minimum stack of 0x1000 is required to use ECC and RSA. This is either the main stack in a bare metal application or the specific thread stack for an RTOS based application.

### AES Usage

#### GCM mode

The first byte of the IV must indicate the length of the subsequent IV. For example if the IV is {0x00, 0x00, 0x00}, then the IV pointer passed to the `_nx_crypto_method_aes_operation` must store the IV as {0x03, 0x00, 0x00, 0x00}. Refer to the example code for actual usage.

#### CTR mode

For CTR mode the IV pointer must be as defined in [Using Advanced Encryption Standard \(AES\) Counter Mode With IPsec Encapsulating Security Payload \(ESP\)](#) under 'Figure 2. Counter Block Format'. The IV must be 8 bytes in length. The Nonce field in the reference above must be 4 bytes and should be passed to `_nx_crypto_method_aes_operation` through the key pointer stored after the actual AES key. For Example, if the AES 128-bit Plain Key is {0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00} and the Nonce is {0x01, 0x07, 0xBD, 0xFD}, the key passed to the

`_nx_crypto_method_aes_operation` during Encryption/Decryption should be set as {0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x07, 0xBD, 0xFD}. This format would also be valid for Wrapped keys where the Nonce is appended at the end of the actual Wrapped key. Refer to the example code for actual usage.

The 'Block Counter' field in the above reference is fixed to {0x00, 0x00, 0x00, 0x01} at the beginning and increments internally after every subsequent AES block is processed. Test vectors that have the initial Block Counter not set to {0x00, 0x00, 0x00, 0x01} cannot be used in this implementation.

## ECC Usage

ECC operations include ECDH and ECDSA. As a part of ECDSA operation the input message can be hashed before signing or verification, or the message digest can be provided directly. ECC Scratch buffer size can be optionally reduced as supported ECC computations are now done by the HW. This is controlled by `NX_CRYPT0_ECDSA_SCRATCH_BUFFER_SIZE` and `NX_CRYPT0_ECDH_SCRATCH_BUFFER_SIZE` macros for ECDSA and ECDH respectively.

Operation	Key Format
ECDSA Signature	Plain private key; Wrapped private key
ECDSA Signature-Verify	Uncompressed public key
Key Generation using ECDSA operation API	Wrapped private key; Uncompressed public key
ECDH private key import	Plain private key; Wrapped private key (Allows for Uncompressed and Formatted public key)
ECDH public key export	Uncompressed public key
ECDH setup	Uncompressed public key
ECDH shared secret calculate	Uncompressed public key
Key Generation using ECDH operation API	Wrapped private key; Uncompressed public key

Note:

- Uncompressed public key is of the form (0x04 || Qx || Qy). Refer Section 2.2. Subject Public Key under [RFC5480](#)
- Formatted public key is of the form (Key Info (4 bytes) || Qx || Qy || Key Info (16 bytes)). This is the key which is used internally by SCE peripheral. (Qx and Qy are zero padded for 224 bit curves).

## RSA Usage

### Wrapped Key Usage

To use the NetX Crypto stack with wrapped private keys (for signature generation/decryption), a dummy pointer (non-NULL) should be passed to the 'key' parameter during `_nx_crypto_method_rsa_init` API call. However, the 'key\_size\_in\_bits' parameter should be equal to the intended RSA modulus length in bits. The actual wrapped key must be passed as the 'key' parameter to the `_nx_crypto_method_rsa_operation` API call with its length in bits passed through the 'key\_size\_in\_bits' parameter.

For PKCS1V15 operation 'key' and 'key\_size\_in\_bits' parameters of `_nx_crypto_method_pkcs1_v1_5_init` are unused. These can be passed as NULL and 0 respectively.

The actual wrapped key must be passed as the 'key' parameter to the `_nx_crypto_method_pkcs1_v1_5_operation` API call and the intended modulus length in bits must be passed through the 'key\_size\_in\_bits' parameter.

## Limitations

- Only little endian mode is supported.
- RSA CRT keys are not supported.
- ECJPAKE related operations are unsupported for NIST 224, 256 and 384 bit curves when HW ECC is enabled.

## Examples

### Initialization Example

This example shows how to initialize the HW crypto engine. This step must be performed before any crypto algorithm is used.

```
/* Setup the platform; initialize the SCE and the TRNG */  
err = _nx_crypto_initialize();  
assert(NX_CRYPTOSUCCESS == err);
```

### Hash Example

This is an example on calculating the SHA256 hash using the NetX Crypto API.

```
extern NX_CRYPTOMETHOD crypto_method_sha256;  
const uint8_t NIST_SHA256ShortMsgLen200[] =  
{  
    0x2e, 0x7e, 0xa8, 0x4d, 0xa4, 0xbc, 0x4d, 0x7c, 0xfb, 0x46, 0x3e, 0x3f, 0x2c,  
    0x86, 0x47, 0x05,  
    0x7a, 0xff, 0xf3, 0xfb, 0xec, 0xec, 0xa1, 0xd2, 00  
};  
const uint8_t NIST_SHA256ShortMsgLen200_expected[] =  
{  
    0x76, 0xe3, 0xac, 0xbc, 0x71, 0x88, 0x36, 0xf2, 0xdf, 0x8a, 0xd2, 0xd0, 0xd2,  
    0xd7, 0x6f, 0x0c,  
    0xfa, 0x5f, 0xea, 0x09, 0x86, 0xbe, 0x91, 0x8f, 0x10, 0xbc, 0xee, 0x73, 0x0d,  
    0xf4, 0x41, 0xb9  
};  
void netx_secure_crypto_sha256_example (void)
```

```
{
size_t   actual_hash_len = RM_NETX_SECURE_CRYPT0_EXAMPLE_SHA256_HASH_SIZE_BYTES;
uint8_t  actual_hash[RM_NETX_SECURE_CRYPT0_EXAMPLE_SHA256_HASH_SIZE_BYTES];
uint8_t  metadata[sizeof(NX_CRYPT0_SHA256)];
uint32_t metadata_size = sizeof(NX_CRYPT0_SHA256);
void     * handler      = NX_CRYPT0_NULL;
uint32_t err           = NX_CRYPT0_SUCCESS;
/* Setup the platform; initialize the SCE and the TRNG */
err = _nx_crypto_initialize();
assert(NX_CRYPT0_SUCCESS == err);
/* Nx Crypto SHA256 init */
err = _nx_crypto_method_sha256_init(&crypto_method_sha256, NX_CRYPT0_NULL, 0,
&handler, metadata, metadata_size);
assert(NX_CRYPT0_SUCCESS == err);
/* Nx Crypto SHA256 operation - NX_CRYPT0_HASH_INITIALIZE */
err = _nx_crypto_method_sha256_operation(NX_CRYPT0_HASH_INITIALIZE,
                                         handler,
                                         &crypto_method_sha256,
                                         NX_CRYPT0_NULL,
                                         0,
                                         NX_CRYPT0_NULL,
                                         0,
                                         NX_CRYPT0_NULL,
                                         NX_CRYPT0_NULL,
                                         0,
                                         metadata,
                                         metadata_size,
                                         NX_CRYPT0_NULL,
                                         NX_CRYPT0_NULL);

assert(NX_CRYPT0_SUCCESS == err);
/* Nx Crypto SHA256 operation - NX_CRYPT0_HASH_UPDATE,
 * call this multiple times if needed to hash multiple data batches */
err =
    _nx_crypto_method_sha256_operation(NX_CRYPT0_HASH_UPDATE,
```

```
        handler,  
        &crypto_method_sha256,  
        NX_CRYPTONULL,  
        0,  
        (uint8_t *) NIST_SHA256ShortMsgLen200,  
sizeof(NIST_SHA256ShortMsgLen200),  
        NX_CRYPTONULL,  
        NX_CRYPTONULL,  
        0,  
        metadata,  
        metadata_size,  
        NX_CRYPTONULL,  
        NX_CRYPTONULL);  
  
    assert(NX_CRYPTONUCCESS == err);  
/* Nx Crypto SHA256 operation - NX_CRYPTONHASH_CALCULATE */  
    err = _nx_crypto_method_sha256_operation(NX_CRYPTONHASH_CALCULATE,  
        handler,  
        &crypto_method_sha256,  
        NX_CRYPTONULL,  
        0,  
        NX_CRYPTONULL,  
        0,  
        NX_CRYPTONULL,  
        (uint8_t *) actual_hash,  
        actual_hash_len,  
        metadata,  
        metadata_size,  
        NX_CRYPTONULL,  
        NX_CRYPTONULL);  
  
    assert(NX_CRYPTONUCCESS == err);  
/* Ensure generated SHA256 hash matches the expected digest */  
    err = (uint32_t) memcmp(&actual_hash[0], &NIST_SHA256ShortMsgLen200_expected[0],  
actual_hash_len);  
    assert(0 == err);
```

```
}

```

## AES Example

This is an example on using the NetX Crypto API to encrypt and decrypt multi-block data.

## AES CBC Example

```
extern NX_CRYPT_METHOD crypto_method_aes_cbc_256;
/* fe8901fecd3ccd2ec5fdc7c7a0b50519c245b42d611a5ef9e90268d59f3edf33 */
const uint8_t NIST_AES256_CBC_key[] =
{
    0xfe, 0x89, 0x01, 0xfe, 0xcd, 0x3c, 0xcd, 0x2e, 0xc5, 0xfd, 0xc7, 0xc7, 0xa0,
    0xb5, 0x05, 0x19,
    0xc2, 0x45, 0xb4, 0x2d, 0x61, 0x1a, 0x5e, 0xf9, 0xe9, 0x02, 0x68, 0xd5, 0x9f,
    0x3e, 0xdf, 0x33
};
/* 851e8764776e6796aab722dbb644ace8 */
const uint8_t NIST_AES256_CBC_iv[] =
{
    0xbd, 0x41, 0x6c, 0xb3, 0xb9, 0x89, 0x22, 0x28, 0xd8, 0xf1, 0xdf, 0x57, 0x56,
    0x92, 0xe4, 0xd0
};
/* 6282b8c05c5c1530b97d4816ca434762 */
const uint8_t NIST_AES256_CBC_plaintext[] =
{
    0x8d, 0x3a, 0xa1, 0x96, 0xec, 0x3d, 0x7c, 0x9b, 0x5b, 0xb1, 0x22, 0xe7, 0xfe,
    0x77, 0xfb, 0x12,
    0x95, 0xa6, 0xda, 0x75, 0xab, 0xe5, 0xd3, 0xa5, 0x10, 0x19, 0x4d, 0x3a, 0x8a,
    0x41, 0x57, 0xd5,
    0xc8, 0x9d, 0x40, 0x61, 0x97, 0x16, 0x61, 0x98, 0x59, 0xda, 0x3e, 0xc9, 0xb2,
    0x47, 0xce, 0xd9
};
/* 6acc04142e100a65f51b97adf5172c41 */
const uint8_t NIST_AES256_CBC_ciphertext[] =
{

```

```
    0x60, 0x8e, 0x82, 0xc7, 0xab, 0x04, 0x00, 0x7a, 0xdb, 0x22, 0xe3, 0x89, 0xa4,
0x47, 0x97, 0xfe,
    0xd7, 0xde, 0x09, 0x0c, 0x8c, 0x03, 0xca, 0x8a, 0x2c, 0x5a, 0xcd, 0x9e, 0x84,
0xdf, 0x37, 0xfb,
    0xc5, 0x8c, 0xe8, 0xed, 0xb2, 0x93, 0xe9, 0x8f, 0x02, 0xb6, 0x40, 0xd6, 0xd1,
0xd7, 0x24, 0x64
};
void netx_secure_crypto_aes256cbc_multipart_example (void)
{
    uint8_t metadata[sizeof(NX_CRYPTTO_AES)];
    uint32_t metadata_size = sizeof(NX_CRYPTTO_AES);
    void * handler = NX_CRYPTTO_NULL;
    uint32_t err = NX_CRYPTTO_SUCCESS;
    /* 3 AES Blocks */
    uint8_t generated_ciphertext[3U * NX_CRYPTTO_AES_BLOCK_SIZE] = {0};
    uint8_t generated_plaintext[3U * NX_CRYPTTO_AES_BLOCK_SIZE] = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTTO_SUCCESS == err);
    err =
        _nx_crypto_method_aes_init(&crypto_method_aes_cbc_256, (uint8_t *)
NIST_AES256_CBC_key,
    sizeof(NIST_AES256_CBC_key) << 3U, &handler, metadata, metadata_size);
    assert(NX_CRYPTTO_SUCCESS == err);
    /* Encryption. */
    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_ENCRYPT,
        handler,
        &crypto_method_aes_cbc_256,
        NULL,
        0,
        (uint8_t *) NIST_AES256_CBC_plaintext,
        sizeof(NIST_AES256_CBC_plaintext),
        (uint8_t *) NIST_AES256_CBC_iv,
        generated_ciphertext,
```

```

sizeof(generated_ciphertext),

                                metadata,
                                metadata_size,
                                NX_CRYPTONULL,
                                NX_CRYPTONULL);

    assert(NX_CRYPTONUCCESS == err);
/* Verify generated ciphertext matches the expected ciphertext */
    err = (uint32_t) memcmp(generated_ciphertext, NIST_AES256_CBC_ciphertext,
sizeof(generated_ciphertext));
    assert(0 == err);
/* Decryption. */
    err = _nx_crypto_method_aes_operation(NX_CRYPTONDECRYPT,
                                handler,
                                &crypto_method_aes_cbc_256,
                                NULL,
                                0,
                                (uint8_t *) NIST_AES256_CBC_ciphertext,
sizeof(NIST_AES256_CBC_ciphertext),
                                (uint8_t *) NIST_AES256_CBC_iv,
                                generated_plaintext,
sizeof(generated_plaintext),
                                metadata,
                                metadata_size,
                                NX_CRYPTONULL,
                                NX_CRYPTONULL);

    assert(NX_CRYPTONUCCESS == err);
/* Verify generated plaintext matches the input plaintext */
    err = (uint32_t) memcmp(generated_plaintext, NIST_AES256_CBC_plaintext,
sizeof(generated_ciphertext));
    assert(0 == err);
}

```

## AES GCM Example

```
extern NX_CRYPTONMETHOD crypto_method_aes_128_gcm_16;
```

```
/* 83F9D97D4AB759FDDCC3EF54A0E2A8EC */
static const uint8_t key_gcm_128[] =
{
    0x83, 0xF9, 0xD9, 0x7D, 0x4A, 0xB7, 0x59, 0xFD, 0xDC, 0xC3, 0xEF, 0x54, 0xA0,
    0xE2, 0xA8, 0xEC
};

/* In case of IV the IV length must be the first byte followed by the actual IV.
 * In this example the IV length is 0x01 and the actual IV is 0xCF
 */
/* 01CF */
static const uint8_t iv_gcm_128[] =
{
    0x01, 0xCF
};

/* 77E6329CF9424F71C808DF9170BFD298 */
static const uint8_t plain_gcm_128[] =
{
    0x77, 0xE6, 0x32, 0x9C, 0xF9, 0x42, 0x4F, 0x71, 0xC8, 0x08, 0xDF, 0x91, 0x70,
    0xBF, 0xD2, 0x98
};

/* 6DD49EAE4103DAC8F97E3234946DD2D */
static const uint8_t aad_gcm_128[] =
{
    0x6D, 0xD4, 0x9E, 0xAE, 0xB4, 0x10, 0x3D, 0xAC, 0x8F, 0x97, 0xE3, 0x23, 0x49,
    0x46, 0xDD, 0x2D
};

/* 50DE86A7A92A8A5EA33DB5696B96CD77AA181E84BC8B4BF5A68927C409D422CB */
static const uint8_t secret_gcm_128[] =
{
    /* Ciphertext */
    0x50, 0xDE, 0x86, 0xA7, 0xA9, 0x2A, 0x8A, 0x5E, 0xA3, 0x3D, 0xB5, 0x69, 0x6B,
    0x96, 0xCD, 0x77,
    /* Tag */
    0xAA, 0x18, 0x1E, 0x84, 0xBC, 0x8B, 0x4B, 0xF5, 0xA6, 0x89, 0x27, 0xC4, 0x09,
```

```
0xD4, 0x22, 0xCB
};

void netx_secure_crypto_aes128gcm_multipart_example (void)
{
    uint8_t metadata[sizeof(NX_CRYPTTO_AES)];
    uint32_t metadata_size = sizeof(NX_CRYPTTO_AES);
    void * handler = NX_CRYPTTO_NULL;
    uint32_t err = NX_CRYPTTO_SUCCESS;
    /* 3 AES Blocks */
    uint8_t generated_ciphertext[3U * NX_CRYPTTO_AES_BLOCK_SIZE] = {0};
    uint8_t generated_plaintext[3U * NX_CRYPTTO_AES_BLOCK_SIZE] = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTTO_SUCCESS == err);
    err =
        _nx_crypto_method_aes_init(&crypto_method_aes_128_gcm_16,
                                   (uint8_t *) key_gcm_128,
                                   sizeof(key_gcm_128) << 3U,
                                   &handler,
                                   metadata,
                                   metadata_size);
    assert(NX_CRYPTTO_SUCCESS == err);
    /* Setup Additional Authentication Data */
    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_SET_ADDITIONAL_DATA,
                                         handler,
                                         &crypto_method_aes_128_gcm_16,
                                         NULL,
                                         0,
                                         (uint8_t *) aad_gcm_128,
                                         sizeof(aad_gcm_128),
                                         NULL,
                                         NULL,
                                         0,
                                         metadata,
```

```
        metadata_size,  
        NX_CRYPTTO_NULL,  
        NX_CRYPTTO_NULL);  
  
    assert(NX_CRYPTTO_SUCCESS == err);  
/* Encryption. */  
    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_ENCRYPT,  
        handler,  
        &crypto_method_aes_128_gcm_16,  
        NULL,  
        0,  
        (uint8_t *) plain_gcm_128,  
        sizeof(plain_gcm_128),  
        (uint8_t *) iv_gcm_128,  
        generated_ciphertext,  
        sizeof(generated_ciphertext),  
        metadata,  
        metadata_size,  
        NX_CRYPTTO_NULL,  
        NX_CRYPTTO_NULL);  
  
    assert(NX_CRYPTTO_SUCCESS == err);  
/* The 16 byte tag is appended to the generated ciphertext */  
/* Verify generated tag matches the expected tag */  
    err = (uint32_t) memcmp(&generated_ciphertext[sizeof(plain_gcm_128)],  
&secret_gcm_128[sizeof(plain_gcm_128)], 16U);  
    assert(0 == err);  
/* Verify generated ciphertext matches the expected ciphertext */  
    err = (uint32_t) memcmp(generated_ciphertext, secret_gcm_128, sizeof  
(secret_gcm_128));  
    assert(0 == err);  
/* Setup Additional Authentication Data */  
    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_SET_ADDITIONAL_DATA,  
        handler,  
        &crypto_method_aes_128_gcm_16,  
        NULL,
```

```
        0,
        (uint8_t *) aad_gcm_128,
sizeof(aad_gcm_128),
        NULL,
        NULL,
        0,
        metadata,
        metadata_size,
        NX_CRYPTONULL,
        NX_CRYPTONULL);

    assert(NX_CRYPTONUCCESS == err);
/* Decryption. */
    err = _nx_crypto_method_aes_operation(NX_CRYPTONDECRYPT,
        handler,
        &crypto_method_aes_128_gcm_16,
        NULL,
        0,
        (uint8_t *) generated_ciphertext,
sizeof(secret_gcm_128), /* ciphertext size + tag size */
        (uint8_t *) iv_gcm_128,
        generated_plaintext,
sizeof(generated_plaintext),
        metadata,
        metadata_size,
        NX_CRYPTONULL,
        NX_CRYPTONULL);

    assert(NX_CRYPTONUCCESS == err);
/* Verify generated plaintext matches the input plaintext */
    err = (uint32_t) memcmp(generated_plaintext, plain_gcm_128, sizeof
(plain_gcm_128));
    assert(0 == err);
}
```

## AES CTR Example

```

NX_CRYPTO_METHOD crypto_method_aes_ctr_256 =
{
    NX_CRYPTO_ENCRYPTION_AES_CTR,          /* AES crypto
algorithm                                  */
    NX_CRYPTO_AES_256_KEY_LEN_IN_BITS,     /* Key size in bits
*/
    NX_CRYPTO_AES_IV_LEN_IN_BITS,         /* IV size in
bits                                       */
    0,                                     /* ICV size in bits, not
used                                       */
    (NX_CRYPTO_AES_BLOCK_SIZE_IN_BITS >> 3), /* Block size in bytes
*/
    sizeof(NX_CRYPTO_AES),                 /* Metadata size in bytes          */
    _nx_crypto_method_aes_init,           /* AES-CBC initialization
routine                                  */
    _nx_crypto_method_aes_cleanup,       /* AES-CBC cleanup routine
*/
    _nx_crypto_method_aes_ctr_operation   /* AES-CBC
operation                                  */
};
/*Note: For CTR, the key_ctr is the conjunction of key and nonce. */
/* D0E78C4D0B30D33F5BF4A132B2F94A4A38963511A3904B117E35A37B5AAC8A193BF0D158 */
const uint8_t key_ctr_256[] =
{
    /* AES Key */
    0xD0, 0xE7, 0x8C, 0x4D, 0x0B, 0x30, 0xD3, 0x3F, 0x5B, 0xF4, 0xA1, 0x32, 0xB2,
    0xF9, 0x4A, 0x4A,
    0x38, 0x96, 0x35, 0x11, 0xA3, 0x90, 0x4B, 0x11, 0x7E, 0x35, 0xA3, 0x7B, 0x5A,
    0xAC, 0x8A, 0x19,
    /* Nonce */
    0x3B, 0xF0, 0xD1, 0x58,
};
/* A1A31704C8B7E16C */
const uint8_t iv_ctr_256[] =

```

```
{
    0xA1, 0xA3, 0x17, 0x04, 0xC8, 0xB7, 0xE1, 0x6C,
};
/* 981FA33222C5451017530155A4BF7F29 */
const uint8_t plain_ctr_256[] =
{
    0x98, 0x1F, 0xA3, 0x32, 0x22, 0xC5, 0x45, 0x10, 0x17, 0x53, 0x01, 0x55, 0xA4,
    0xBF, 0x7F, 0x29,
};
/* 643B91B4E541B20AAAEAB77F2D328566 */
const uint8_t secret_ctr_256[] =
{
    0x64, 0x3B, 0x91, 0xB4, 0xE5, 0x41, 0xB2, 0x0A, 0xAA, 0xEA, 0xB7, 0x7F, 0x2D,
    0x32, 0x85, 0x66,
};
void netx_secure_crypto_aes256ctr_multipart_example (void)
{
    uint8_t metadata[sizeof(NX_CRYPTO_AES)];
    uint32_t metadata_size = sizeof(NX_CRYPTO_AES);
    void * handler = NX_CRYPTO_NULL;
    uint32_t err = NX_CRYPTO_SUCCESS;
    /* 3 AES Blocks */
    uint8_t generated_ciphertext[3U * NX_CRYPTO_AES_BLOCK_SIZE] = {0};
    uint8_t generated_plaintext[3U * NX_CRYPTO_AES_BLOCK_SIZE] = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTO_SUCCESS == err);
    err =
        _nx_crypto_method_aes_init(&crypto_method_aes_ctr_256,
                                   (uint8_t *) key_ctr_256,
                                   crypto_method_aes_ctr_256.nx_crypto_key_size_in_bits,
                                   &handler,
                                   metadata,
```

```
        metadata_size);

    assert(NX_CRYPTTO_SUCCESS == err);

    /* Encryption. */

    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_ENCRYPT,

                                         handler,

                                         &crypto_method_aes_ctr_256,

                                         (uint8_t *) key_ctr_256,

crypto_method_aes_ctr_256.nx_crypto_key_size_in_bits,

                                         (uint8_t *) plain_ctr_256,

sizeof(plain_ctr_256),

                                         (uint8_t *) iv_ctr_256,

                                         generated_ciphertext,

sizeof(generated_ciphertext),

                                         metadata,

                                         metadata_size,

                                         NX_CRYPTTO_NULL,

                                         NX_CRYPTTO_NULL);

    assert(NX_CRYPTTO_SUCCESS == err);

    /* Verify generated ciphertext matches the expected ciphertext */

    err = (uint32_t) memcmp(generated_ciphertext, secret_ctr_256, sizeof

(secret_ctr_256));

    assert(0 == err);

    /* Decryption. */

    err = _nx_crypto_method_aes_operation(NX_CRYPTTO_DECRYPT,

                                         handler,

                                         &crypto_method_aes_ctr_256,

                                         (uint8_t *) key_ctr_256,

crypto_method_aes_ctr_256.nx_crypto_key_size_in_bits,

                                         (uint8_t *) secret_ctr_256,

sizeof(secret_ctr_256),

                                         (uint8_t *) iv_ctr_256,

                                         generated_plaintext,
```

```

sizeof(generated_plaintext),
                                metadata,
                                metadata_size,
                                NX_CRYPTONULL,
                                NX_CRYPTONULL);

assert(NX_CRYPTONUCCESS == err);
/* Verify generated plaintext matches the input plaintext */
err = (uint32_t) memcmp(generated_plaintext, plain_ctr_256, sizeof
(plain_ctr_256));
assert(0 == err);
}

```

## ECDSA Example

This is an example on using the NetX Crypto API to sign and verify input message data. Based on the hash algorithm selected a digest is computed of the plain input message before sign/verify.

```

extern NX_CRYPTONETHOD crypto_method_ecdsa;
extern NX_CRYPTONETHOD crypto_method_ec_secp256;
extern NX_CRYPTONETHOD crypto_method_sha256;
const uint8_t ECC_SECP256R1Keydata[] =
{
    0xf9, 0xa7, 0x68, 0x71, 0x24, 0x68, 0x9d, 0x32, 0x92, 0x6f, 0x1d, 0xfb, 0xbe,
    0xf2, 0x61, 0x41, // NOLINT(readability-magic-numbers)
    0x07, 0x54, 0x0d, 0xb9, 0xa8, 0x8a, 0x8b, 0xc2, 0xd5, 0xe9, 0x38, 0x4b, 0xf9,
    0xe5, 0x43, 0x5a // NOLINT(readability-magic-numbers)
};
const uint8_t ECC_SECP256R1PublicKeydata[] =
{
    0x04,
    /* ASN1 Constant */
    0x5b, 0xba, 0xd4, 0x2e, 0xb5, 0xc1, 0x07, 0xf2, 0x0e, 0x01, 0x95, 0x42, 0x6e,
    0x90, 0xb8, 0x4e, // NOLINT(readability-magic-numbers)
    0xe9, 0x5a, 0xa1, 0xe8, 0x4c, 0x6c, 0xa5, 0x32, 0x3c, 0xf3, 0x09, 0xf5, 0xff,
    0x8b, 0x3d, 0x26, // NOLINT(readability-magic-numbers)
}

```

```
    0xb6, 0x88, 0xc1, 0xdb, 0x02, 0xaf, 0x4d, 0xa5, 0x0e, 0x73, 0x61, 0x96, 0xb3,
0x59, 0x95, 0x6f, // NOLINT(readability-magic-numbers)
    0x5e, 0xc9, 0xa1, 0xf9, 0xb7, 0xb3, 0xb6, 0xdf, 0x54, 0x82, 0x79, 0xe3, 0xb6,
0x4e, 0xac, 0xb6 // NOLINT(readability-magic-numbers)
};
const uint8_t ECC_SECP256R1Message[] = "ASYMMETRIC_INPUT_FOR_SIGN.....";
void netx_secure_crypto_ecdsa_example (void)
{
    uint8_t metadata[sizeof(NX_CRYPTTO_ECDSA)];
    uint32_t metadata_size = sizeof(NX_CRYPTTO_ECDSA);
    void * handler = NX_CRYPTTO_NULL;
    uint32_t err = NX_CRYPTTO_SUCCESS;
    ULONG sig_length;
    NX_CRYPTTO_EXTENDED_OUTPUT extended_output;
    uint8_t output[RM_NETX_SECURE_CRYPTTO_EXAMPLE_OUTPUT_BUFFER_SIZE] = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTTO_SUCCESS == err);
    /* Call the crypto initialization function. */
    err = _nx_crypto_method_ecdsa_init(&crypto_method_ecdsa, NX_CRYPTTO_NULL, 0,
&handler, metadata, metadata_size);
    assert(NX_CRYPTTO_SUCCESS == err);
    /* Set hash method. */
    err = _nx_crypto_method_ecdsa_operation(NX_CRYPTTO_HASH_METHOD_SET,
                                            handler,
                                            &crypto_method_ecdsa,
                                            NX_CRYPTTO_NULL,
                                            0,
                                            (uint8_t *) &crypto_method_sha256,
                                            sizeof(NX_CRYPTTO_METHOD *),
                                            NX_CRYPTTO_NULL,
                                            NX_CRYPTTO_NULL,
                                            0,
                                            metadata,
```

```
        metadata_size,
        NX_CRYPTO_NULL,
        NX_CRYPTO_NULL);

    assert(NX_CRYPTO_SUCCESS == err);
/* Set EC curve. */
    err =
        _nx_crypto_method_ecdsa_operation(NX_CRYPTO_EC_CURVE_SET,
        handler,
        &crypto_method_ecdsa,
        NX_CRYPTO_NULL,
        0,
        (uint8_t *) &crypto_method_ec_secp256,
sizeof(NX_CRYPTO_METHOD *),
        NX_CRYPTO_NULL,
        NX_CRYPTO_NULL,
        0,
        metadata,
        metadata_size,
        NX_CRYPTO_NULL,
        NX_CRYPTO_NULL);

    assert(NX_CRYPTO_SUCCESS == err);
    extended_output.nx_crypto_extended_output_data = output;
    extended_output.nx_crypto_extended_output_length_in_byte = sizeof(output);
/* Sign the hash data using ECDSA. */
    err = _nx_crypto_method_ecdsa_operation(NX_CRYPTO_SIGNATURE_GENERATE,
        handler,
        &crypto_method_ec_secp256,
        (uint8_t *) ECC_SECP256R1Keydata,
sizeof(ECC_SECP256R1Keydata) << 3,
        (uint8_t *) ECC_SECP256R1Message,
sizeof(ECC_SECP256R1Message),
        NX_CRYPTO_NULL,
        (uint8_t *) &extended_output,
sizeof(extended_output),
```

```

    metadata,
    metadata_size,
    NX_CRYPTTO_NULL,
    NX_CRYPTTO_NULL);

assert(NX_CRYPTTO_SUCCESS == err);

sig_length = extended_output.nx_crypto_extended_output_actual_size;
/* Verify the generated signature. */
err = _nx_crypto_method_ecdsa_operation(NX_CRYPTTO_SIGNATURE_VERIFY,
                                       handler,
                                       &crypto_method_ec_secp256,
                                       (uint8_t *) ECC_SECP256R1PublicKeydata,
                                       sizeof(ECC_SECP256R1PublicKeydata) << 3,
                                       (uint8_t *) ECC_SECP256R1Message,
                                       sizeof(ECC_SECP256R1Message),
                                       NX_CRYPTTO_NULL,
                                       output,
                                       sig_length,
                                       metadata,
                                       metadata_size,
                                       NX_CRYPTTO_NULL,
                                       NX_CRYPTTO_NULL);

assert(NX_CRYPTTO_SUCCESS == err);
}

```

## ECDH Example

This is an example on using the NetX Crypto API to generate a shared secret using ECDH. A shared secret is computed using known public key (from peer) and generated private key. Another shared secret is computed using the generated public key and known private key (imported to mimic peer). Both the shared secrets are checked to be the same.

```

extern NX_CRYPTTO_METHOD crypto_method_ecdh;
/*Private key 59137e38152350b195c9718d39673d519838055ad908dd4757152fd8255c09bf */
const uint8_t ECC_SECP256R1Keydata_ecdh[] =
{
    0x59, 0x13, 0x7e, 0x38, 0x15, 0x23, 0x50, 0xb1, 0x95, 0xc9, 0x71, 0x8d, 0x39,

```

```
0x67, 0x3d, 0x51, // NOLINT(readability-magic-numbers)
    0x98, 0x38, 0x05, 0x5a, 0xd9, 0x08, 0xdd, 0x47, 0x57, 0x15, 0x2f, 0xd8, 0x25,
0x5c, 0x09, 0xbf, // NOLINT(readability-magic-numbers)
};
/*Public key 4, a8c5fdce8b62c5ada598f141adb3b26cf254c280b2857a63d2ad783a73115f6b,
806e1aafec4af80a0d786b3de45375b517a7e5b51ffb2c356537c9e6ef227d4a*/
const uint8_t ECC_SECP256R1PublicKeydata_ecdh[] =
{
    0x04,
    0xa8,0xc5, 0xfd, 0xce, 0x8b, 0x62, 0xc5, 0xad, 0xa5, 0x98, 0xf1, 0x41, 0xad,
0xb3, 0xb2, 0x6c, // NOLINT(readability-magic-numbers)
    0xf2,0x54, 0xc2, 0x80, 0xb2, 0x85, 0x7a, 0x63, 0xd2, 0xad, 0x78, 0x3a, 0x73,
0x11, 0x5f, 0x6b, // NOLINT(readability-magic-numbers)
    0x80,0x6e, 0x1a, 0xaf, 0xec, 0x4a, 0xf8, 0x0a, 0x0d, 0x78, 0x6b, 0x3d, 0xe4,
0x53, 0x75, 0xb5, // NOLINT(readability-magic-numbers)
    0x17,0xa7, 0xe5, 0xb5, 0x1f, 0xfb, 0x2c, 0x35, 0x65, 0x37, 0xc9, 0xe6, 0xef,
0x22, 0x7d, 0x4a, // NOLINT(readability-magic-numbers)
};
void netx_secure_crypto_ecdh_example (void)
{
    uint8_t metadata[sizeof(NX_CRYPTTO_ECDH)];
    uint32_t metadata_size = sizeof(NX_CRYPTTO_ECDH);
    uint32_t err          = NX_CRYPTTO_SUCCESS;
    uint8_t local_public_key[RM_NETX_SECURE_CRYPTTO_EXAMPLE_OUTPUT_BUFFER_SIZE] = {0};
    uint32_t local_public_key_len = 0;
    uint8_t shared_secret[RM_NETX_SECURE_CRYPTTO_EXAMPLE_OUTPUT_BUFFER_SIZE] = {0};
    uint32_t shared_secret_len = 0;
    uint8_t output[RM_NETX_SECURE_CRYPTTO_EXAMPLE_OUTPUT_BUFFER_SIZE] = {0};
    NX_CRYPTTO_EXTENDED_OUTPUT extended_output;
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTTO_SUCCESS == err);
    /* Call the crypto initialization function. */
    err = _nx_crypto_method_ecdh_init(&crypto_method_ecdh, NX_CRYPTTO_NULL, 0,
```

```
NX_CRYPTO_NULL, metadata, metadata_size);

    assert(NX_CRYPTO_SUCCESS == err);

    /* Set EC curve. */

    err = _nx_crypto_method_ecdh_operation(NX_CRYPTO_EC_CURVE_SET,

                                          NX_CRYPTO_NULL,

                                          &crypto_method_ecdh,

                                          NX_CRYPTO_NULL,

                                          0,

                                          (uint8_t *) &crypto_method_ec_secp256,

sizeof(NX_CRYPTO_METHOD *),

                                          NX_CRYPTO_NULL,

                                          NX_CRYPTO_NULL,

                                          0,

                                          metadata,

                                          metadata_size,

                                          NX_CRYPTO_NULL,

                                          NX_CRYPTO_NULL);

    assert(NX_CRYPTO_SUCCESS == err);

    /* Generate local public key. This will generate a key pair.

    * The private wrapped key will be held by the ecdh context and the public key

(local_public_key)

    * will be returned for sharing with the peer.

    */

    extended_output.nx_crypto_extended_output_data          = local_public_key;

    extended_output.nx_crypto_extended_output_length_in_byte = sizeof

(local_public_key);

    err = _nx_crypto_method_ecdh_operation(NX_CRYPTO_DH_SETUP,

                                          NX_CRYPTO_NULL,

                                          &crypto_method_ecdh,

                                          NX_CRYPTO_NULL,

                                          0,

                                          NX_CRYPTO_NULL,

                                          0,

                                          NX_CRYPTO_NULL,
```

```

                                                                    (uint8_t *) &extended_output,
sizeof(extended_output),
                                                                    metadata,
                                                                    metadata_size,
                                                                    NX_CRYPTO_NULL,
                                                                    NX_CRYPTO_NULL);

assert(NX_CRYPTO_SUCCESS == err);

local_public_key_len = extended_output.nx_crypto_extended_output_actual_size;
/* Calculate shared secret using the test (peer's) public key. */
extended_output.nx_crypto_extended_output_data = shared_secret;
extended_output.nx_crypto_extended_output_length_in_byte = sizeof(shared_secret);
err = _nx_crypto_method_ecdh_operation(NX_CRYPTO_DH_CALCULATE,
                                                                    NX_CRYPTO_NULL,
                                                                    &crypto_method_ecdh,
                                                                    NX_CRYPTO_NULL,
                                                                    0,
                                                                    (uint8_t *)
ECC_SECP256R1PublicKeydata_ecdh,
sizeof(ECC_SECP256R1PublicKeydata_ecdh),
                                                                    NX_CRYPTO_NULL,
                                                                    (uint8_t *) &extended_output,
sizeof(extended_output),
                                                                    metadata,
                                                                    metadata_size,
                                                                    NX_CRYPTO_NULL,
                                                                    NX_CRYPTO_NULL);

assert(NX_CRYPTO_SUCCESS == err);

shared_secret_len = extended_output.nx_crypto_extended_output_actual_size;
err = _nx_crypto_method_ecdh_cleanup(metadata);
assert(NX_CRYPTO_SUCCESS == err);
/* Verify. The below operations will be carried out by the peer. */
/* Call the crypto initialization function. */
err = _nx_crypto_method_ecdh_init(&crypto_method_ecdh, NX_CRYPTO_NULL, 0,
NX_CRYPTO_NULL, metadata, metadata_size);

```

```
assert(NX_CRYPTTO_SUCCESS == err);

/* Set EC curve. */

err = _nx_crypto_method_ecdh_operation(NX_CRYPTTO_EC_CURVE_SET,

                                       NX_CRYPTTO_NULL,

                                       &crypto_method_ecdh,

                                       NX_CRYPTTO_NULL,

                                       0,

                                       (uint8_t *) &crypto_method_ec_secp256,

sizeof(NX_CRYPTTO_METHOD *),

                                       NX_CRYPTTO_NULL,

                                       NX_CRYPTTO_NULL,

                                       0,

                                       metadata,

                                       metadata_size,

                                       NX_CRYPTTO_NULL,

                                       NX_CRYPTTO_NULL);

assert(NX_CRYPTTO_SUCCESS == err);

/* Import the test private key. The peer could generate its own key pair,
 * in this example a test private key is used for simplicity. */

err =

    _nx_crypto_method_ecdh_operation(NX_CRYPTTO_DH_KEY_PAIR_IMPORT,

                                     NX_CRYPTTO_NULL,

                                     &crypto_method_ecdh,

                                     (uint8_t *) ECC_SECP256R1Keydata_ecdh,

                                     (NX_CRYPTTO_KEY_SIZE)

(sizeof(ECC_SECP256R1Keydata_ecdh) << 3),

                                     (uint8_t *) ECC_SECP256R1PublicKeydata_ecdh,

sizeof(ECC_SECP256R1PublicKeydata_ecdh),

                                     NX_CRYPTTO_NULL,

                                     NX_CRYPTTO_NULL,

                                     0,

                                     metadata,

                                     metadata_size,

                                     NX_CRYPTTO_NULL,
```

```

        NX_CRYPTO_NULL);

    assert(NX_CRYPTO_SUCCESS == err);

    /* Calculate the shared secret using the local public key generated above and shared
with the peer. */

    extended_output.nx_crypto_extended_output_data          = output;
    extended_output.nx_crypto_extended_output_length_in_byte = sizeof(output);
    err = _nx_crypto_method_ecdh_operation(NX_CRYPTO_DH_CALCULATE,
                                          NX_CRYPTO_NULL,
                                          &crypto_method_ecdh,
                                          NX_CRYPTO_NULL,
                                          0,
                                          local_public_key,
                                          local_public_key_len,
                                          NX_CRYPTO_NULL,
                                          (uint8_t *) &extended_output,
                                          sizeof(extended_output),
                                          metadata,
                                          metadata_size,
                                          NX_CRYPTO_NULL,
                                          NX_CRYPTO_NULL);

    assert(NX_CRYPTO_SUCCESS == err);

    /* Validate the output. Both the parties must generate the same shared secret */
    err = (extended_output.nx_crypto_extended_output_actual_size !=
shared_secret_len);

    assert(NX_CRYPTO_SUCCESS == err);

    err = (uint32_t) memcmp(output, shared_secret,
extended_output.nx_crypto_extended_output_actual_size);

    assert(NX_CRYPTO_SUCCESS == err);
}

```

## RSA Example

This is an example on using the NetX Crypto API to encrypt and decrypt input message data.

```
extern NX_CRYPTO_METHOD crypto_method_rsa;
```

```
/* 00010001 */
const uint8_t public_e[] =
{
    0x00, 0x01, 0x00, 0x01,
};
/* 13FF7429F8E851F1079CCFCE3B3CD8606ABA8607AD85CBB3057501EBD58811F3C04823171F192C048E
1E883AF8CF958810151D3874AEDC8EC4F88D2065C581569F1E200852DD40B6DFD1652659085A9DD1D3B86
9EA3617D904D209DE156A60BA5929D02F16430273D10720C2F28D2B95684DCAA6B9F6A508EA2CBBC11B9F
3F30D6201EA6CFFBFBF1C44255CEC58EE70DBC872442BCCF115D8F743557B5DE5F42DDDA6CEAE7977793CC
9D90ADFE65E520F5520B615CF3B8C2DC82D7AC75EDB1297CF38AB23A37EED18D4DD45D9AD051B26401BE8
6E8C8E53F9585A702D02F1B5BD65F6739DFA6BFFE560CA130B6F1D4779C556C06D9CD29FB72D8851904F9
CDEE9 */
const uint8_t private_e_2048[] =
{
    0x13, 0xFF, 0x74, 0x29, 0xF8, 0xE8, 0x51, 0xF1, 0x07, 0x9C, 0xCF, 0xCE, 0x3B,
0x3C, 0xD8, 0x60,
    0x6A, 0xBA, 0x86, 0x07, 0xAD, 0x85, 0xCB, 0xB3, 0x05, 0x75, 0x01, 0xEB, 0xD5,
0x88, 0x11, 0xF3,
    0xC0, 0x48, 0x23, 0x17, 0x1F, 0x19, 0x2C, 0x04, 0x8E, 0x1E, 0x88, 0x3A, 0xF8,
0xCF, 0x95, 0x88,
    0x10, 0x15, 0x1D, 0x38, 0x74, 0xAE, 0xDC, 0x8E, 0xC4, 0xF8, 0x8D, 0x20, 0x65,
0xC5, 0x81, 0x56,
    0x9F, 0x1E, 0x20, 0x08, 0x52, 0xDD, 0x40, 0xB6, 0xDF, 0xD1, 0x65, 0x26, 0x59,
0x08, 0x5A, 0x9D,
    0xD1, 0xD3, 0xB8, 0x69, 0xEA, 0x36, 0x17, 0xD9, 0x04, 0xD2, 0x09, 0xDE, 0x15,
0x6A, 0x60, 0xBA,
    0x59, 0x29, 0xD0, 0x2F, 0x16, 0x43, 0x02, 0x73, 0xD1, 0x07, 0x20, 0xC2, 0xF2,
0x8D, 0x2B, 0x95,
    0x68, 0x4D, 0xCA, 0xA6, 0xB9, 0xF6, 0xA5, 0x08, 0xEA, 0x2C, 0xBB, 0xC1, 0x1B,
0x9F, 0x3F, 0x30,
    0xD6, 0x20, 0x1E, 0xA6, 0xCF, 0xFB, 0xBF, 0x1C, 0x44, 0x25, 0x5C, 0xEC, 0x58,
0xEE, 0x70, 0xDB,
    0xC8, 0x72, 0x44, 0x2B, 0xCC, 0xF1, 0x15, 0xD8, 0xF7, 0x43, 0x55, 0x7B, 0x5D,
0xE5, 0xF4, 0x2D,
```

```
    0xDD, 0xA6, 0xCE, 0xAE, 0x79, 0x77, 0x79, 0x3C, 0xC9, 0xD9, 0x0A, 0xDF, 0xE6,
0x5E, 0x52, 0x0F,
    0x55, 0x20, 0xB6, 0x15, 0xCF, 0x3B, 0x8C, 0x2D, 0xC8, 0x2D, 0x7A, 0xC7, 0x5E,
0xDB, 0x12, 0x97,
    0xCF, 0x38, 0xAB, 0x23, 0xA3, 0x7E, 0xED, 0x18, 0xD4, 0xDD, 0x45, 0xD9, 0xAD,
0x05, 0x1B, 0x26,
    0x40, 0x1B, 0xE8, 0x6E, 0x8C, 0x8E, 0x53, 0xF9, 0x58, 0x5A, 0x70, 0x2D, 0x02,
0xF1, 0xB5, 0xBD,
    0x65, 0xF6, 0x73, 0x9D, 0xFA, 0x6B, 0xFF, 0xE5, 0x60, 0xCA, 0x13, 0x0B, 0x6F,
0x1D, 0x47, 0x79,
    0xC5, 0x56, 0xC0, 0x6D, 0x9C, 0xD2, 0x9F, 0xB7, 0x2D, 0x88, 0x51, 0x90, 0x4F,
0x9C, 0xDE, 0xE9,
};
/* E0F5059966A8AEC4BF7CDAC8AE2430BDF61C54D09CAB9963CBF9A52AC641E384B6431D3B6A9D181151
9A2904E1170A44446C80E7638A4AF2720A7654AB740D8A151FDD216F3D6933422FD9AC14AEDE9CCD021EA
79E46925F4B18FD1AF2C0073CFC3A69AC71A2B3673D08136CDB01C379892601C7C857D68018DAE924CB8C
D29377A14C752B92BAFF14C3A49725AE2FEFAAD4686D8A7D9F94EB11BF81E05BD5D2586526FB129E73539
F9223D496B2ACA23CCACC34D5B18533BD0F5815A76F94F4F55D965FE61599B44BD8FBAD35F42B612A4C4F
2765B2097A5C0090EA8166D9C6DA1E03B6119736B794600491C48433132D0F15D5DE3BB4270DF6BC9012B
74931 */
const uint8_t m_2048[] =
{
    0xE0, 0xF5, 0x05, 0x99, 0x66, 0xA8, 0xAE, 0xC4, 0xBF, 0x7C, 0xDA, 0xC8, 0xAE,
0x24, 0x30, 0xBD,
    0xF6, 0x1C, 0x54, 0xD0, 0x9C, 0xAB, 0x99, 0x63, 0xCB, 0xF9, 0xA5, 0x2A, 0xC6,
0x41, 0xE3, 0x84,
    0xB6, 0x43, 0x1D, 0x3B, 0x6A, 0x9D, 0x18, 0x11, 0x51, 0x9A, 0x29, 0x04, 0xE1,
0x17, 0x0A, 0x44,
    0x44, 0x6C, 0x80, 0xE7, 0x63, 0x8A, 0x4A, 0xF2, 0x72, 0x0A, 0x76, 0x54, 0xAB,
0x74, 0x0D, 0x8A,
    0x15, 0x1F, 0xDD, 0x21, 0x6F, 0x3D, 0x69, 0x33, 0x42, 0x2F, 0xD9, 0xAC, 0x14,
0xAE, 0xDE, 0x9C,
    0xCD, 0x02, 0x1E, 0xA7, 0x9E, 0x46, 0x92, 0x5F, 0x4B, 0x18, 0xFD, 0x1A, 0xF2,
0xC0, 0x07, 0x3C,
```

```
    0xFC, 0x3A, 0x69, 0xAC, 0x71, 0xA2, 0xB3, 0x67, 0x3D, 0x08, 0x13, 0x6C, 0xDB,  
0x01, 0xC3, 0x79,  
    0x89, 0x26, 0x01, 0xC7, 0xC8, 0x57, 0xD6, 0x80, 0x18, 0xDA, 0xE9, 0x24, 0xCB,  
0x8C, 0xD2, 0x93,  
    0x77, 0xA1, 0x4C, 0x75, 0x2B, 0x92, 0xBA, 0xFF, 0x14, 0xC3, 0xA4, 0x97, 0x25,  
0xAE, 0x2F, 0xEF,  
    0xAA, 0xD4, 0x68, 0x6D, 0x8A, 0x7D, 0x9F, 0x94, 0xEB, 0x11, 0xBF, 0x81, 0xE0,  
0x5B, 0xD5, 0xD2,  
    0x58, 0x65, 0x26, 0xFB, 0x12, 0x9E, 0x73, 0x53, 0x9F, 0x92, 0x23, 0xD4, 0x96,  
0xB2, 0xAC, 0xA2,  
    0x3C, 0xCA, 0xCC, 0x34, 0xD5, 0xB1, 0x85, 0x33, 0xBD, 0x0F, 0x58, 0x15, 0xA7,  
0x6F, 0x94, 0xF4,  
    0xF5, 0x5D, 0x96, 0x5F, 0xE6, 0x15, 0x99, 0xB4, 0x4B, 0xD8, 0xFB, 0xAD, 0x35,  
0xF4, 0x2B, 0x61,  
    0x2A, 0x4C, 0x4F, 0x27, 0x65, 0xB2, 0x09, 0x7A, 0x5C, 0x00, 0x90, 0xEA, 0x81,  
0x66, 0xD9, 0xC6,  
    0xDA, 0x1E, 0x03, 0xB6, 0x11, 0x97, 0x36, 0xB7, 0x94, 0x60, 0x04, 0x91, 0xC4,  
0x84, 0x33, 0x13,  
    0x2D, 0x0F, 0x15, 0xD5, 0xDE, 0x3B, 0xB4, 0x27, 0x0D, 0xF6, 0xBC, 0x90, 0x12,  
0xB7, 0x49, 0x31,  
};  
/* 551C2E268F7ED44D0E8B063F5B2B510CB809F53BD54E9956971E243B2363DA123C29AB4A009EDE1FCE  
C54625971A4E3490F3EA398BF7386AAC34720E43FB0C795445B520AEE4D7694EE1474F60F77E1B5F09FE2  
ED004333658D212122F040322D1564512A1540400F27E18049A762A5EDC9F072CA4F49F408252D42B31BC  
35523373740E90DDDA6A8CE7865EEB7C694A662C74412406AB190FE0435DA2551F0C24A48939DDA58A023  
9706D40B4977473689DC36CE5A4DF4EF892816CBDE2780D9389B7384674C93B1DDAF728F292B5671679FC  
7175AC0A3B2197B809E7CF410417010F3B1316D10D82466C62F3A01667B70A714E0499400E255D4C39EA7  
DE55C */  
const uint8_t plain_2048[] =  
{  
    0x55, 0x1C, 0x2E, 0x26, 0x8F, 0x7E, 0xD4, 0x4D, 0x0E, 0x8B, 0x06, 0x3F, 0x5B,  
0x2B, 0x51, 0x0C,  
    0xB8, 0x09, 0xF5, 0x3B, 0xD5, 0x4E, 0x99, 0x56, 0x97, 0x1E, 0x24, 0x3B, 0x23,  
0x63, 0xDA, 0x12,
```

```
    0x3C, 0x29, 0xAB, 0x4A, 0x00, 0x9E, 0xDE, 0x1F, 0xCE, 0xC5, 0x46, 0x25, 0x97,  
0x1A, 0x4E, 0x34,  
    0x90, 0xF3, 0xEA, 0x39, 0x8B, 0xF7, 0x38, 0x6A, 0xAC, 0x34, 0x72, 0x0E, 0x43,  
0xFB, 0x0C, 0x79,  
    0x54, 0x45, 0xB5, 0x20, 0xAE, 0xE4, 0xD7, 0x69, 0x4E, 0xE1, 0x47, 0x4F, 0x60,  
0xF7, 0x7E, 0x1B,  
    0x5F, 0x09, 0xFE, 0x2E, 0xD0, 0x04, 0x33, 0x36, 0x58, 0xD2, 0x12, 0x12, 0x2F,  
0x04, 0x03, 0x22,  
    0xD1, 0x56, 0x45, 0x12, 0xA1, 0x54, 0x04, 0x00, 0xF2, 0x7E, 0x18, 0x04, 0x9A,  
0x76, 0x2A, 0x5E,  
    0xDC, 0x9F, 0x07, 0x2C, 0xA4, 0xF4, 0x9F, 0x40, 0x82, 0x52, 0xD4, 0x2B, 0x31,  
0xBC, 0x35, 0x52,  
    0x33, 0x73, 0x74, 0x0E, 0x90, 0xDD, 0xDA, 0x6A, 0x8C, 0xE7, 0x86, 0x5E, 0xEB,  
0x7C, 0x69, 0x4A,  
    0x66, 0x2C, 0x74, 0x41, 0x24, 0x06, 0xAB, 0x19, 0x0F, 0xE0, 0x43, 0x5D, 0xA2,  
0x55, 0x1F, 0x0C,  
    0x24, 0xA4, 0x89, 0x39, 0xDD, 0xA5, 0x8A, 0x02, 0x39, 0x70, 0x6D, 0x40, 0xB4,  
0x97, 0x74, 0x73,  
    0x68, 0x9D, 0xC3, 0x6C, 0xE5, 0xA4, 0xDF, 0x4E, 0xF8, 0x92, 0x81, 0x6C, 0xBD,  
0xE2, 0x78, 0x0D,  
    0x93, 0x89, 0xB7, 0x38, 0x46, 0x74, 0xC9, 0x3B, 0x1D, 0xDA, 0xF7, 0x28, 0xF2,  
0x92, 0xB5, 0x67,  
    0x16, 0x79, 0xFC, 0x71, 0x75, 0xAC, 0x0A, 0x3B, 0x21, 0x97, 0xB8, 0x09, 0xE7,  
0xCF, 0x41, 0x04,  
    0x17, 0x01, 0x0F, 0x3B, 0x13, 0x16, 0xD1, 0x0D, 0x82, 0x46, 0x6C, 0x62, 0xF3,  
0xA0, 0x16, 0x67,  
    0xB7, 0x0A, 0x71, 0x4E, 0x04, 0x99, 0x40, 0x0E, 0x25, 0x5D, 0x4C, 0x39, 0xEA,  
0x7D, 0xE5, 0x5C,  
};  
/* 10F904E071338569EC131401A7869F42F3BCAE252B5D3C8755FD24D47997A9CD4221D992B2871E0528  
3B98841FC5C379C5D0E35B3938279B344299C3CF1566E0C994D0A9013AF64174F1379A4B5E4E9DE57491F  
3078F6D10011EA55535D0763E538662C9996F4FCF8B64A768685AA417ADB6978743D3D1F513CF143DD6D3  
83AD6357728A88928D39E27EA4D0B2AF92FC7F63875F9D6A70FAE7993C1FF04DF9A2F99216874BC123D4B  
7DA7E7E8974CFC10ACF0C7BC8747526A8D16791F969082EA9B0C36D77B67C37B325682D74178E4234D52D
```

```
5635273301A6CC35E315AE74D659B1433576DAAE6780FA39E0550D971F2CB5817CAAFC24B5220E21C8CEE
E85DD */
const uint8_t secret_2048[] =
{
    0x10, 0xF9, 0x04, 0xE0, 0x71, 0x33, 0x85, 0x69, 0xEC, 0x13, 0x14, 0x01, 0xA7,
    0x86, 0x9F, 0x42,
    0xF3, 0xBC, 0xAE, 0x25, 0x2B, 0x5D, 0x3C, 0x87, 0x55, 0xFD, 0x24, 0xD4, 0x79,
    0x97, 0xA9, 0xCD,
    0x42, 0x21, 0xD9, 0x92, 0xB2, 0x87, 0x1E, 0x05, 0x28, 0x3B, 0x98, 0x84, 0x1F,
    0xC5, 0xC3, 0x79,
    0xC5, 0xD0, 0xE3, 0x5B, 0x39, 0x38, 0x27, 0x9B, 0x34, 0x42, 0x99, 0xC3, 0xCF,
    0x15, 0x66, 0xE0,
    0xC9, 0x94, 0xD0, 0xA9, 0x01, 0x3A, 0xF6, 0x41, 0x74, 0xF1, 0x37, 0x9A, 0x4B,
    0x5E, 0x4E, 0x9D,
    0xE5, 0x74, 0x91, 0xF3, 0x07, 0x8F, 0x6D, 0x10, 0x01, 0x1E, 0xA5, 0x55, 0x35,
    0xD0, 0x76, 0x3E,
    0x53, 0x86, 0x62, 0xC9, 0x99, 0x6F, 0x4F, 0xCF, 0x8B, 0x64, 0xA7, 0x68, 0x68,
    0x5A, 0xA4, 0x17,
    0xAD, 0xB6, 0x97, 0x87, 0x43, 0xD3, 0xD1, 0xF5, 0x13, 0xCF, 0x14, 0x3D, 0xD6,
    0xD3, 0x83, 0xAD,
    0x63, 0x57, 0x72, 0x8A, 0x88, 0x92, 0x8D, 0x39, 0xE2, 0x7E, 0xA4, 0xD0, 0xB2,
    0xAF, 0x92, 0xFC,
    0x7F, 0x63, 0x87, 0x5F, 0x9D, 0x6A, 0x70, 0xFA, 0xE7, 0x99, 0x3C, 0x1F, 0xF0,
    0x4D, 0xF9, 0xA2,
    0xF9, 0x92, 0x16, 0x87, 0x4B, 0xC1, 0x23, 0xD4, 0xB7, 0xDA, 0x7E, 0x7E, 0x89,
    0x74, 0xCF, 0xC1,
    0x0A, 0xCF, 0x0C, 0x7B, 0xC8, 0x74, 0x75, 0x26, 0xA8, 0xD1, 0x67, 0x91, 0xF9,
    0x69, 0x08, 0x2E,
    0xA9, 0xB0, 0xC3, 0x6D, 0x77, 0xB6, 0x7C, 0x37, 0xB3, 0x25, 0x68, 0x2D, 0x74,
    0x17, 0x8E, 0x42,
    0x34, 0xD5, 0x2D, 0x56, 0x35, 0x27, 0x33, 0x01, 0xA6, 0xCC, 0x35, 0xE3, 0x15,
    0xAE, 0x74, 0xD6,
    0x59, 0xB1, 0x43, 0x35, 0x76, 0xDA, 0xAE, 0x67, 0x80, 0xFA, 0x39, 0xE0, 0x55,
    0x0D, 0x97, 0x1F,
```

```
    0x2C, 0xB5, 0x81, 0x7C, 0xAA, 0xFC, 0x24, 0xB5, 0x22, 0x0E, 0x21, 0xC8, 0xCE,  
0xEE, 0x85, 0xDD,  
};  
void netx_secure_crypto_rsa_example (void)  
{  
    uint8_t metadata[sizeof(NX_CRYPTORSA)];  
    uint32_t metadata_size = sizeof(NX_CRYPTORSA);  
    uint32_t err          = NX_CRYPTO_SUCCESS;  
    void * handler       = NX_CRYPTO_NULL;  
    uint8_t output[RM_NETX_SECURE_CRYPTO_EXAMPLE_OUTPUT_BUFFER_SIZE] = {0};  
    /* Setup the platform; initialize the SCE and the TRNG */  
    err = _nx_crypto_initialize();  
    assert(NX_CRYPTO_SUCCESS == err);  
    /* Encryption. */  
    err =  
        _nx_crypto_method_rsa_init(&crypto_method_rsa,  
                                   (uint8_t *) m_2048,  
                                   RM_NETX_SECURE_CRYPTO_BYTES_TO_BITS(sizeof(m_2048)),  
                                   &handler,  
                                   metadata,  
                                   metadata_size);  
    assert(NX_CRYPTO_SUCCESS == err);  
    err = _nx_crypto_method_rsa_operation(NX_CRYPTO_ENCRYPT,  
                                         handler,  
                                         &crypto_method_rsa,  
                                         (uint8_t *) public_e,  
                                         RM_NETX_SECURE_CRYPTO_BYTES_TO_BITS(sizeof(public_e)),  
                                         (uint8_t *) plain_2048,  
                                         sizeof(m_2048),  
                                         NX_CRYPTO_NULL,  
                                         output,
```

```
sizeof(m_2048),  
  
        metadata,  
        metadata_size,  
        NX_CRYPTTO_NULL,  
        NX_CRYPTTO_NULL);  
  
assert(NX_CRYPTTO_SUCCESS == err);  
err = (uint32_t) memcmp(output, secret_2048, sizeof(m_2048));  
assert(0 == err);  
err = _nx_crypto_method_rsa_cleanup(metadata);  
assert(NX_CRYPTTO_SUCCESS == err);  
/* Decryption. */  
memset(output, 0, sizeof(output));  
err =  
    _nx_crypto_method_rsa_init(&crypto_method_rsa,  
                              (uint8_t *) m_2048,  
                              RM_NETX_SECURE_CRYPTTO_BYTES_TO_BITS(sizeof(m_2048)),  
                              &handler,  
                              metadata,  
                              metadata_size);  
assert(NX_CRYPTTO_SUCCESS == err);  
err = _nx_crypto_method_rsa_operation(NX_CRYPTTO_DECRYPT,  
                                      handler,  
                                      &crypto_method_rsa,  
                                      (uint8_t *) private_e_2048,  
                                      RM_NETX_SECURE_CRYPTTO_BYTES_TO_BITS(sizeof(private_e_2048)),  
                                      (uint8_t *) secret_2048,  
                                      sizeof(m_2048),  
                                      NX_CRYPTTO_NULL,  
                                      output,  
                                      sizeof(m_2048),  
                                      metadata,
```

```

        metadata_size,
        NX_CRYPTTO_NULL,
        NX_CRYPTTO_NULL);

assert(NX_CRYPTTO_SUCCESS == err);
err = (uint32_t) memcmp(output, plain_2048, sizeof(m_2048));
assert(0 == err);
}

```

### RSA PKCS1V1.5 Example

This is an example on using the NetX Crypto API to sign and verify input message data. The plain input message is PKCS1V1.5 encoded before signature generation.

#### PKCS1V15 Example

### HMAC SHA256 Example

This is an example on using the HMAC with SHA256 hash using the NetX Crypto API.

```

extern NX_CRYPTTO_METHOD crypto_method_hmac_sha256;
/*
C4DA057B81EA740B697FFE1B6EB8591356BA6D5EA7F1B96E4F048030449ACD64E4BB271CB4DCF94937E6
*/
const uint8_t key_256[] =
{
    0xC4, 0xDA, 0x05, 0x7B, 0x81, 0xEA, 0x74, 0x0B, 0x69, 0x7F, 0xFE, 0x1B, 0x6E,
    0xB8, 0x59, 0x13,
    0x56, 0xBA, 0x6D, 0x5E, 0xA7, 0xF1, 0xB9, 0x6E, 0x4F, 0x04, 0x80, 0x30, 0x44,
    0x9A, 0xCD, 0x64,
    0xE4, 0xBB, 0x27, 0x1C, 0xB4, 0xDC, 0xF9, 0x49, 0x37, 0xE6,
};
/* BDACB6555D294D3AFFC245520116062D98F88D64276BDA593492AE71CFE16E46CABC287CB00DF21D96
066D5856C2224EEF609D4896302540078F3A0EE325F5337E */
const uint8_t plain_256[] =
{
    0xBD, 0xAC, 0xB6, 0x55, 0x5D, 0x29, 0x4D, 0x3A, 0xFF, 0xC2, 0x45, 0x52, 0x01,
    0x16, 0x06, 0x2D,
    0x98, 0xF8, 0x8D, 0x64, 0x27, 0x6B, 0xDA, 0x59, 0x34, 0x92, 0xAE, 0x71, 0xCF,

```

```

0xE1, 0x6E, 0x46,
    0xCA, 0xBC, 0x28, 0x7C, 0xB0, 0x0D, 0xF2, 0x1D, 0x96, 0x06, 0x6D, 0x58, 0x56,
0xC2, 0x22, 0x4E,
    0xEF, 0x60, 0x9D, 0x48, 0x96, 0x30, 0x25, 0x40, 0x07, 0x8F, 0x3A, 0x0E, 0xE3,
0x25, 0xF5, 0x33,
    0x7E,
};
/* 940F986AC891C9000B72EF0CEC69AB66AF002E3A34EB8A3A5F94484E45C0396C */
const uint8_t secret_256[] =
{
    0x94, 0x0F, 0x98, 0x6A, 0xC8, 0x91, 0xC9, 0x00, 0x0B, 0x72, 0xEF, 0x0C, 0xEC,
0x69, 0xAB, 0x66,
    0xAF, 0x00, 0x2E, 0x3A, 0x34, 0xEB, 0x8A, 0x3A, 0x5F, 0x94, 0x48, 0x4E, 0x45,
0xC0, 0x39, 0x6C,
};
void netx_secure_crypto_hmac_sha256_example (void)
{
    uint8_t output[RM_NETX_SECURE_CRYPTO_EXAMPLE_SHA256_HASH_SIZE_BYTES] = {0};
    uint8_t metadata[sizeof(NX_CRYPTO_SHA256_HMAC)] = {0};
    uint32_t metadata_size = sizeof(NX_CRYPTO_SHA256_HMAC);
    void * handler = NX_CRYPTO_NULL;
    uint32_t err = NX_CRYPTO_SUCCESS;
    /* Setup the platform; initialize the SCE and the TRNG */
    err = _nx_crypto_initialize();
    assert(NX_CRYPTO_SUCCESS == err);
    /* Nx Crypto HMAC-SHA256 init */
    err = _nx_crypto_method_hmac_sha256_init(&crypto_method_hmac_sha256,
                                             (UCHAR *) key_256,
                                             RM_NETX_SECURE_CRYPTO_BYTES_TO_BITS(sizeof(key_256)),
                                             &handler,
                                             metadata,

```

```
        metadata_size);

    assert(NX_CRYPTOSUCCESS == err);

    /* Nx Crypto HMAC-SHA256 operation - NX_CRYPTOSHASH_INITIALIZE */
    err =
        _nx_crypto_method_hmac_sha256_operation(NX_CRYPTOSHASH_INITIALIZE,
                                                handler,
                                                &crypto_method_hmac_sha256,
                                                (UCHAR *) key_256,

RM_NETX_SECURE_CRYPTO_BYTES_TO_BITS(sizeof(key_256)),
                                                NX_CRYPTONULL,
                                                0,
                                                NX_CRYPTONULL,
                                                NX_CRYPTONULL,
                                                0,
                                                metadata,
                                                metadata_size,
                                                NX_CRYPTONULL,
                                                NX_CRYPTONULL);

    assert(NX_CRYPTOSUCCESS == err);

    /* Nx Crypto HMAC-SHA256 operation - NX_CRYPTOSHASH_UPDATE */
    err = _nx_crypto_method_hmac_sha256_operation(NX_CRYPTOSHASH_UPDATE,
                                                handler,
                                                &crypto_method_hmac_sha256,
                                                NX_CRYPTONULL,
                                                0,
                                                (UCHAR *) plain_256,
sizeof(plain_256),
                                                NX_CRYPTONULL,
                                                NX_CRYPTONULL,
                                                0,
                                                metadata,
                                                metadata_size,
                                                NX_CRYPTONULL,
```

```

                                                                 NX_CRYPTONULL);

assert(NX_CRYPTONUCCESS == err);

/* Nx Crypto HMAC-SHA256 operation - NX_CRYPTONHASH_CALCULATE */
err = _nx_crypto_method_hmac_sha256_operation(NX_CRYPTONHASH_CALCULATE,
                                              handler,
                                              &crypto_method_hmac_sha256,
                                              NX_CRYPTONNULL,
                                              0,
                                              NX_CRYPTONNULL,
                                              0,
                                              NX_CRYPTONNULL,
                                              (UCHAR *) output,
                                              sizeof(output),
                                              metadata,
                                              metadata_size,
                                              NX_CRYPTONNULL,
                                              NX_CRYPTONNULL);

assert(NX_CRYPTONUCCESS == err);

/* Ensure generated HMAC-SHA256 mac matches the expected mac */
err = (uint32_t) memcmp(output, secret_256, sizeof(secret_256));
assert(0 == err);
}

```

## 4.2.94 Azure RTOS NetX Duo Ether Driver (rm\_netxduo\_ether)

### Modules

## Overview

This module provides a NetX Duo driver that is implemented using the [Ethernet Interface](#).

Please refer to the [NetXDuo documentation](#) for further details.

### Features

- Packet Types Supported

- ARP
- IPv4
- IPv6
- Link status callback
- Configurable IP MTU

## Configuration

### Configurations for Middleware > Networking > NetX Duo Ethernet Driver

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_netxduo_ether_0	Module name.
IP MTU	Value must be in the range [576, 1500] bytes.	1500	IP MTU

## Usage Notes

### Calculating the Packet Size for an IP instance

In order to ensure that there is enough space to store an entire Ethernet frame, the packet pool used for receiving packets must have a payload size that is 32 bytes larger than the configured `ether_cfg_t::ether_buffer_size`. The extra 32 bytes is needed in order to ensure that the allocated packets are properly aligned to 32 bytes.

`ether_cfg_t::ether_buffer_size` is calculated from the IP MTU using the following formula:

$$\text{ceil}((\text{rm\_netxduo\_ether\_cfg\_t::mtu} + \text{Ethernet Header (14)} + \text{Padding Bytes (2)}) / 32) * 32$$

## Examples

### Basic Example

This is a basic example of minimal use of the NetX Duo Ether Driver in an application.

```
#define NETXDUO_EXAMPLE_IP_STACK_SIZE (2048U)
#define NETXDUO_EXAMPLE_ARP_CACHE_SIZE (2048U)
#define NETXDUO_EXAMPLE_PACKET_SIZE (1568U)
#define NETXDUO_EXAMPLE_PACKET_NUM (100U)
#define NETXDUO_EXAMPLE_PACKET_POOL_SIZE ((sizeof(NX_PACKET) +
NETXDUO_EXAMPLE_PACKET_SIZE) * \
    NETXDUO_EXAMPLE_PACKET_NUM)
static NX_IP g_ip;
static NX_PACKET_POOL g_packet_pool;
```

```
static uint8_t g_ip_stack_memory[NETXDUEXAMPLE_IP_STACK_SIZE]
BSP_ALIGN_VARIABLE(4);
static uint8_t g_packet_pool_memory[NETXDUEXAMPLE_PACKET_POOL_SIZE]
BSP_ALIGN_VARIABLE(4);
static uint8_t g_ip_arp_cache_memory[NETXDUEXAMPLE_ARP_CACHE_SIZE]
BSP_ALIGN_VARIABLE(4);
static void rm_netxduo_ether0 (NX_IP_DRIVER * driver_req_ptr)
{
    /* Pass the driver request and ethernet driver configuration to the NetX Duo Ether
Driver. */
    rm_netxduo_ether(driver_req_ptr, &g_netxduo_ether_instance);
}
void rm_netxduo_ether_example ()
{
    UINT status;
    nx_system_initialize();
    /* Create a packet pool for the IP instance. */
    status = nx_packet_pool_create(&g_packet_pool,
"Packet Pool",
                                NETXDUEXAMPLE_PACKET_SIZE,
                                &g_packet_pool_memory[0],
                                NETXDUEXAMPLE_PACKET_POOL_SIZE);
    assert(NX_SUCCESS == status);
    /* Create an IP instance using the rm_netxduo_ether driver and packet pool instance.
*/
    status = nx_ip_create(&g_ip,
"IP Instance",
                        IP_ADDRESS(192, 168, 1, 2),
                        IP_ADDRESS(255, 255, 255, 0),
                        &g_packet_pool,
                        rm_netxduo_ether0,
                        &g_ip_stack_memory[0],
                        sizeof(g_ip_stack_memory),
                        0);
}
```

```
    assert(NX_SUCCESS == status);

    /* Enable all modules that are required by the application. */
    status = nx_arp_enable(&g_ip, g_ip_arp_cache_memory, sizeof
(g_ip_arp_cache_memory));

    assert(NX_SUCCESS == status);

    status = nx_tcp_enable(&g_ip);

    assert(NX_SUCCESS == status);

    status = nx_icmp_enable(&g_ip);

    assert(NX_SUCCESS == status);
}
```

## 4.2.95 Azure RTOS NetX Duo WiFi Driver (rm\_netxduo\_wifi)

### Modules

## Overview

This module provides a NetX Duo driver that is implemented using the `rm_wifi_onchip_silex` driver.

Please refer to the [NetXDuo documentation](#) for further details.

### Features

- Packet Types Supported
  - TCP/IPv4
- Configurable IP MTU

## Configuration

### Build Time Configurations for `rm_netxduo_wifi`

The following build time configurations are defined in `fsp_cfg/middleware/rm_netxduo_wifi_cfg.h`:

Configuration	Options	Default	Description
IP MTU (bytes)	Value must be in the range [576, 1500] bytes.	1500	IP MTU

## Usage Notes

### Connecting to a Wireless Network

NetX Duo does not support connecting to a wireless network directly and instead the driver functions should be called directly to establish a connection.

- `rm_wifi_onchip_silex_open` should be called to initialize the WiFi module driver.
- `rm_wifi_onchip_silex_scan` should be used to scan for access points.
- `rm_wifi_onchip_silex_connect` should be used before opening a NetX IP instance in order to connect it to a network.

### Unsupported NetX Duo Features

TCP client sockets are the sole feature supported by both the hardware TCP/IP feature in NetX Duo and the WiFi driver as well, so any protocol that doesn't run over TCP will be unsupported.

- DNS is not supported. The user can preform a DNS lookup by calling `rm_wifi_onchip_silex_dns_query`.
- ICMP is not supported. The user can perform a ping by calling `rm_wifi_onchip_silex_ping`.
- ARP is not supported. This should be handled directly by the WiFi module.
- UDP is not supported. The WiFi module driver does not support UDP sockets.
- SNTP is not supported. See the public APIs for communication with time servers [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#).

## Examples

### Basic Example

This is a basic example of minimal use of the NetX Duo WiFi Driver in an application.

```
#define NETXDUO_EXAMPLE_IP_STACK_SIZE (2048U)
#define NETXDUO_EXAMPLE_ARP_CACHE_SIZE (2048U)
#define NETXDUO_EXAMPLE_PACKET_SIZE (1568U)
#define NETXDUO_EXAMPLE_PACKET_NUM (100U)
#define NETXDUO_EXAMPLE_PACKET_POOL_SIZE ((sizeof(NX_PACKET) +
NETXDUO_EXAMPLE_PACKET_SIZE) * \
    NETXDUO_EXAMPLE_PACKET_NUM)
#define NETXDUO_EXAMPLE_SSID "ssidName"
#define NETXDUO_EXAMPLE_PASSWORD "password"
static NX_IP g_ip0;
static NX_PACKET_POOL g_packet_pool0;
static uint8_t g_ip0_stack_memory[NETXDUO_EXAMPLE_IP_STACK_SIZE]
BSP_ALIGN_VARIABLE(4);
static uint8_t g_packet_pool0_pool_memory[NETXDUO_EXAMPLE_PACKET_POOL_SIZE]
```

```
BSP_ALIGN_VARIABLE(4);

extern wifi_onchip_silex_cfg_t g_wifi_onchip_silex_cfg;

void rm_netxduo_wifi_example ()
{
    UINT      status;

    fsp_err_t err;

    nx_system_initialize();

    /* Open WiFi module */

    err = rm_wifi_onchip_silex_open(&g_wifi_onchip_silex_cfg);

    assert(FSP_SUCCESS == err);

    /* Connect to desired AP */

    err = rm_wifi_onchip_silex_connect(NETXDUO_EXAMPLE_SSID, eWiFiSecurityWPA2,
NETXDUO_EXAMPLE_PASSWORD);

    assert(FSP_SUCCESS == err);

    /* Create a packet pool for the IP instance. */

    status = nx_packet_pool_create(&g_packet_pool0,
"Packet Pool",

                                NETXDUO_EXAMPLE_PACKET_SIZE,

                                &g_packet_pool0_pool_memory[0],

                                NETXDUO_EXAMPLE_PACKET_POOL_SIZE);

    assert(NX_SUCCESS == status);

    /* Create an IP instance using the rm_netxduo_wifi driver and packet pool instance.
*/

    status = nx_ip_create(&g_ip0,
"IP Instance",

                        IP_ADDRESS(192, 168, 1, 2),

                        IP_ADDRESS(255, 255, 255, 0),

                        &g_packet_pool0,

                        rm_netxduo_wifi,

                        &g_ip0_stack_memory[0],

                        sizeof(g_ip0_stack_memory),

                        0);

    assert(NX_SUCCESS == status);

    /* Enable all modules that are required by the application. */
```

```
status = nx_tcp_enable(&g_ip0);  
assert(NX_SUCCESS == status);  
}
```

## TLS Example

This is a basic example of connecting a TLS socket.

```
#define NETXDUO_EXAMPLE_CRYPTOMETADATA_BUFFER_SIZE (18000U)  
#define NETXDUO_EXAMPLE_TLS_PACKET_REASSEMBLY_BUFFER_SIZE (4000U)  
#define NETXDUO_EXAMPLE_PORT (3005U)  
#define NETXDUO_EXAMPLE_SERVER_PORT (9050U)  
#define NETXDUO_EXAMPLE_IP IP_ADDRESS(1, 2, 3, 5)  
NX_SECURE_TLS_CRYPTOMETADATA_BUFFER_SIZE g_nx_crypto_tls_test_ciphers;  
static UCHAR g_tls_crypto_metadata[NETXDUO_EXAMPLE_CRYPTOMETADATA_BUFFER_SIZE];  
static UCHAR g_tls_packet_buffer[NETXDUO_EXAMPLE_TLS_PACKET_REASSEMBLY_BUFFER_SIZE];  
static NX_SECURE_X509_CERT g_certificate;  
extern const UCHAR g_trusted_ca_data; // User trusted certificates  
extern USHORT g_trusted_ca_length;  
void rm_netxduo_wifi_tls_example ()  
{  
    UINT status;  
    fsp_err_t err;  
    NX_TCP_SOCKET * p_socket;  
    NX_SECURE_TLS_SESSION tls_session;  
    nx_system_initialize();  
    /* Initialize NetX Crypto */  
    status = nx_crypto_initialize();  
    assert(NX_SUCCESS == status);  
    /* Open WiFi module */  
    err = rm_wifi_onchip_silex_open(&g_wifi_onchip_silex_cfg);  
    assert(FSP_SUCCESS == err);  
    /* Connect to desired AP */  
    err = rm_wifi_onchip_silex_connect(NETXDUO_EXAMPLE_SSID, eWiFiSecurityWPA2,  
NETXDUO_EXAMPLE_PASSWORD);
```

```
    assert(FSP_SUCCESS == err);

/* Create a packet pool for the IP instance. */
    status = nx_packet_pool_create(&g_packet_pool0,
    "Packet Pool",
                                NETXDUO_EXAMPLE_PACKET_SIZE,
                                &g_packet_pool0_pool_memory[0],
                                NETXDUO_EXAMPLE_PACKET_POOL_SIZE);

    assert(NX_SUCCESS == status);

/* Create an IP instance using the rm_netxduo_wifi driver and packet pool instance.
*/
    status = nx_ip_create(&g_ip0,
    "IP Instance",
                                IP_ADDRESS(192, 168, 1, 2),
                                IP_ADDRESS(255, 255, 255, 0),
                                &g_packet_pool0,
                                rm_netxduo_wifi,
                                &g_ip0_stack_memory[0],
                                sizeof(g_ip0_stack_memory),
                                0);

    assert(NX_SUCCESS == status);

/* Enable all modules that are required by the application. */
    status = nx_tcp_enable(&g_ip0);
    assert(NX_SUCCESS == status);

/* Initialize the NetX Secure TLS system. */
    nx_secure_tls_initialize();

/* Create a TCP socket to use for the TLS session. */
    status = nx_tcp_socket_create(&g_ip0,
                                p_socket,
    "TLS Client Socket",
                                NX_IP_NORMAL,
                                NX_FRAGMENT_OKAY,
                                NX_IP_TIME_TO_LIVE,
                                1024 * 4,
                                NX_NULL,
```

```

        NX_NULL);

    assert(NX_SUCCESS == status);

/* Create a TLS session for our socket. This sets up the TLS session object for
 * later use */
    status =
        nx_secure_tls_session_create(&tls_session,
                                     &g_nx_crypto_tls_test_ciphers,
                                     g_tls_crypto_metadata,
                                     NETXDUEXAMPLE_CRYPTO_METADATA_BUFFER_SIZE);

    assert(NX_SUCCESS == status);

/* Set the packet reassembly buffer for this TLS session. */
    status = nx_secure_tls_session_packet_buffer_set(&tls_session,
                                                    g_tls_packet_buffer,
                                                    NETXDUEXAMPLE_TLS_PACKET_REASSEMBLY_BUFFER_SIZE);

    assert(NX_SUCCESS == status);

/* Initialize an X.509 certificate with the CA root certificate data. */
    status = nx_secure_x509_certificate_initialize(&g_certificate,
                                                (UCHAR *) g_trusted_ca_data,
                                                g_trusted_ca_length,
                                                NX_NULL,
                                                0,
                                                NX_NULL,
                                                0,
                                                NX_SECURE_X509_KEY_TYPE_NONE);

    assert(NX_SUCCESS == status);

/* Add the initialized certificate as a trusted root certificate. */
    status = nx_secure_tls_trusted_certificate_add(&tls_session, &g_certificate);
    assert(NX_SUCCESS == status);

/* Bind the socket to a port. */
    status = nx_tcp_client_socket_bind(p_socket, NETXDUEXAMPLE_PORT,
    NX_WAIT_FOREVER);

    assert(NX_SUCCESS == status);

/* Connect TCP socket */
```

```

    status = nx_tcp_client_socket_connect(p_socket, NETXDUEXAMPLE_IP,
NETXDUEXAMPLE_SERVER_PORT, NX_WAIT_FOREVER);

    assert(NX_SUCCESS == status);

/* Start the TLS Session using the connected TCP socket. This function will
* ascertain from the TCP socket state that this is a TLS Client session. */
    status = nx_secure_tls_session_start(&tls_session, p_socket, NX_WAIT_FOREVER);
    assert(NX_SUCCESS == status);
}

```

## 4.2.96 Crypto Middleware (rm\_psa\_crypto)

### Modules

#### Functions

`fsp_err_t` [RM\\_PSA\\_CRYPTO\\_TRNG\\_Read](#) (uint8\_t \*const p\_rngbuf, uint32\_t num\_req\_bytes, uint32\_t \*p\_num\_gen\_bytes)

Reads requested length of random data from the TRNG. Generate nbytes of random bytes and store them in p\_rngbuf buffer. [More...](#)

`int` [mbedtls\\_platform\\_setup](#) (mbedtls\_platform\_context \*ctx)

`void` [mbedtls\\_platform\\_teardown](#) (mbedtls\_platform\_context \*ctx)

#### Detailed Description

Hardware acceleration for the mbedCrypto implementation of the ARM PSA Crypto API.

## Overview

### Note

*The PSA Crypto module does not provide any interfaces to the user. This release uses the Mbed TLS version 2.24.0 which conforms to the PSA Crypto API 1.0 specification. Consult the ARM documentation at <https://armmbed.github.io/mbed-crypto/psa/#application-programming-interface> for further information. FSP 3.0 onward adopts a change by ARM where mbedCrypto has been integrated back to MbedTLS and the term mbedCrypto has been deprecated. The mbedCrypto term in FSP now refers to the crypto portion of the MbedTLS module.*

### HW Overview

Crypto Peripheral version	Devices
---------------------------	---------

SCE9	RA6M4, RA4M3, RA4M2
SCE7	RA6M3, RA6M2, RA6M1, RA6T1, RA6M5
SCE5	RA4W1, RA4M1
AES Engine	RA2A1, RA2E1, RA2E2, RA2L1

## Features

The PSA\_Crypto module provides hardware support for the following PSA Crypto operations

- SHA256 calculation
- SHA224 calculation
  - MAC Operations
- AES
  - Keybits - 128, 192, 256
  - Plain-Text Key Generation
  - Wrapped Key Generation
  - Encryption and Decryption with no padding and with PKCS7 padding.
  - CBC, CTR, CCM and GCM modes
  - MAC operations
  - Export and Import for Plaintext and Wrapped keys
- ECC
  - Curves:
    - SECP256R1
    - SECP256K1
    - Brainpool256R1
    - SECP384R1
    - Brainpool384R1
  - Plain-Text Key Generation (Unavailable on SCE9)
  - Wrapped Key Generation
  - Signing and Verification
  - Export and Import for Plaintext and Wrapped keys
  - ECDH Support
- RSA
  - Keybits - 2048. Verification only for 3072 and 4096 bits
  - Plain-Text Key Generation (Unavailable on SCE9)
  - Wrapped Key Generation
  - Signature Generation
  - Verification
  - Encryption and Decryption with PKCS1V15 and OAEP padding
  - Export and Import for Plaintext and Wrapped keys
- Random number generation
- Persistent Key Storage

## Configuration

### Build Time Configurations for mbedCrypto

The following build time configurations are defined in arm/mbedtls/config.h:

Configuration	Options	Default	Description
Hardware Acceleration > Key Format > AES	MCU Specific Options		Select AES key formats used

Hardware Acceleration > Key Format > ECC	MCU Specific Options			Select ECC key formats used
Hardware Acceleration > Key Format > RSA	MCU Specific Options			Select RSA key formats used
Hardware Acceleration > Hash > SHA256/224	MCU Specific Options			Defines MBEDTLS_SHA256_ALT and MBEDTLS_SHA256_PROCESS_ALT.
Hardware Acceleration > Cipher > AES	MCU Specific Options			Defines MBEDTLS_AES_ALT, MBEDTLS_AES_SETKEY_ENC_ALT, MBEDTLS_AES_SETKEY_DEC_ALT, MBEDTLS_AES_ENCRYPT_ALT and MBEDTLS_AES_DECRYPT_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > ECC	MCU Specific Options			Defines MBEDTLS_ECP_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > ECDSA	MCU Specific Options			Defines MBEDTLS_ECDSA_SIGN_ALT and MBEDTLS_ECDSA_VERIFY_ALT
Hardware Acceleration > Public Key Cryptography (PKC) > RSA	MCU Specific Options			Defines MBEDTLS_RSA_ALT.
Hardware Acceleration > Public Key Cryptography (PKC) > RSA 3072 Verify	MCU Specific Options			Enables RSA 3072 Verify.
Hardware Acceleration > Public Key Cryptography (PKC) > RSA 4096 Verify	MCU Specific Options			Enables RSA 4096 Verify.
Hardware Acceleration > TRNG	Enabled	Enabled		Defines MBEDTLS_ENTROPY_HARDWARE_ALT.
Hardware Acceleration > Secure Crypto Engine Initialization	Enabled	Enabled		MBEDTLS_PLATFORM_SETUP_TEAR_DOWN_ALT
Platform > Alternate > MBEDTLS_PLATFORM_EXIT_ALT	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine		MBEDTLS_PLATFORM_EXIT_ALT
Platform > Alternate > MBEDTLS_PLATFORM_TIME_ALT	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine		MBEDTLS_PLATFORM_TIME_ALT

Platform > Alternate > MBEDTLS_PLATFORM_FPRINTF_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_FPRINTF_ALT
Platform > Alternate > MBEDTLS_PLATFORM_PRINTF_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_PRINTF_ALT
Platform > Alternate > MBEDTLS_PLATFORM_SNPRINTF_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_SNPRINTF_ALT
Platform > Alternate > MBEDTLS_PLATFORM_VSNPRINTF_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_VSNPRINTF_ALT
Platform > Alternate > MBEDTLS_PLATFORM_NV_SEED_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_NV_SEED_ALT
Platform > Alternate > MBEDTLS_PLATFORM_ZEROIZE_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_ZEROIZE_ALT
Platform > Alternate > MBEDTLS_PLATFORM_GETTIME_R_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_GETTIME_R_ALT
Platform > MBEDTLS_HAVE_ASM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_ASM
Platform > MBEDTLS_NO_UDBL_DIVISION	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NO_UDBL_DIVISION
Platform > MBEDTLS_NO_64BIT_MULTIPLICATION	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NO_64BIT_MULTIPLICATION
Platform > MBEDTLS_HAVE_SSE2	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_SSE2
Platform > MBEDTLS_HAVE_TIME	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_TIME
Platform > MBEDTLS_HAVE_TIME_DATE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HAVE_TIME_DATE
Platform > MBEDTLS_PLATFORM_MEMORY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PLATFORM_MEMORY
Platform > MBEDTLS_PLATFORM_NO_STD_FUNCTIONS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_NO_STD_FUNCTIONS
Platform > MBEDTLS_TIMING_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_TIMING_ALT
Platform > MBEDTLS_NO_PLATFORM_ENTROPY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_NO_PLATFORM_ENTROPY
Platform >	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Define	MBEDTLS_ENTROPY_C

MBEDTLS_ENTROPY_C	• Undefine		
Platform > MBEDTLS_PLATFORM_C	• Define • Undefine	Define	MBEDTLS_PLATFORM_C
Platform > MBEDTLS_PLATFORM_STD_CALLOC	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_CALLOC
Platform > MBEDTLS_PLATFORM_STD_CALLOC value	Manual Entry	calloc	MBEDTLS_PLATFORM_STD_CALLOC value
Platform > MBEDTLS_PLATFORM_STD_FREE	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_FREE
Platform > MBEDTLS_PLATFORM_STD_FREE value	Manual Entry	free	MBEDTLS_PLATFORM_STD_FREE value
Platform > MBEDTLS_PLATFORM_STD_EXIT	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_EXIT
Platform > MBEDTLS_PLATFORM_STD_EXIT value	Manual Entry	exit	MBEDTLS_PLATFORM_STD_EXIT value
Platform > MBEDTLS_PLATFORM_STD_TIME	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_TIME
Platform > MBEDTLS_PLATFORM_STD_TIME value	Manual Entry	time	MBEDTLS_PLATFORM_STD_TIME value
Platform > MBEDTLS_PLATFORM_STD_FPRINTF	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_FPRINTF
Platform > MBEDTLS_PLATFORM_STD_FPRINTF value	Manual Entry	fprintf	MBEDTLS_PLATFORM_STD_FPRINTF value
Platform > MBEDTLS_PLATFORM_STD_PRINTF	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_PRINTF
Platform > MBEDTLS_PLATFORM_STD_PRINTF value	Manual Entry	printf	MBEDTLS_PLATFORM_STD_PRINTF value
Platform > MBEDTLS_PLATFORM_STD_SNPRINTF	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_SNPRINTF
Platform > MBEDTLS_PLATFORM_STD_SNPRINTF value	Manual Entry	snprintf	MBEDTLS_PLATFORM_STD_SNPRINTF value
Platform > MBEDTLS_PLATFORM_STD_EXIT_SUCCESS	• Define • Undefine	Undefine	MBEDTLS_PLATFORM_STD_EXIT_SUCCESS
Platform > MBEDTLS_PLATFORM_STD_EXIT_SUCCESS	Manual Entry	0	MBEDTLS_PLATFORM_STD_EXIT_SUCCESS

CCESS value			value
Platform > MBEDTLS_PLATFORM_STD_EXIT_FAILURE	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_EXIT_FAILURE
Platform > MBEDTLS_PLATFORM_STD_EXIT_FAILURE value	Manual Entry	1	MBEDTLS_PLATFORM_STD_EXIT_FAILURE value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_READ	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_READ
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_READ value	Manual Entry	mbdctl_platform_std_nv_seed_read	MBEDTLS_PLATFORM_STD_NV_SEED_READ value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_WRITE	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_WRITE
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_WRITE value	Manual Entry	mbdctl_platform_std_nv_seed_write	MBEDTLS_PLATFORM_STD_NV_SEED_WRITE value
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_FILE	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_STD_NV_SEED_FILE
Platform > MBEDTLS_PLATFORM_STD_NV_SEED_FILE value	Manual Entry	mbdctl_platform_std_nv_seed_file	MBEDTLS_PLATFORM_STD_NV_SEED_FILE value
Platform > MBEDTLS_PLATFORM_C_ALLOC_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_C_ALLOC_MACRO
Platform > MBEDTLS_PLATFORM_C_ALLOC_MACRO value	Manual Entry	calloc	MBEDTLS_PLATFORM_C_ALLOC_MACRO value
Platform > MBEDTLS_PLATFORM_FREE_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_FREE_MACRO
Platform > MBEDTLS_PLATFORM_FREE_MACRO value	Manual Entry	free	MBEDTLS_PLATFORM_FREE_MACRO value
Platform > MBEDTLS_PLATFORM_EXIT_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_EXIT_MACRO
Platform > MBEDTLS_PLATFORM_EXIT_MACRO value	Manual Entry	exit	MBEDTLS_PLATFORM_EXIT_MACRO value
Platform > MBEDTLS_PLATFORM_TIME_MACRO	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_TIME_MACRO
Platform > MBEDTLS_PLATFORM_TIME_MACRO value	Manual Entry	time	MBEDTLS_PLATFORM_TIME_MACRO

LATFORM_TIME_MACRO value			IME_MACRO value
Platform > MBEDTLS_P LATFORM_TIME_TYPE_ MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_T IME_TYPE_MACRO
Platform > MBEDTLS_P LATFORM_TIME_TYPE_ MACRO value	Manual Entry	time_t	MBEDTLS_PLATFORM_T IME_TYPE_MACRO value
Platform > MBEDTLS_P LATFORM_FPRINTF_MA CRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_F PRINTF_MACRO
Platform > MBEDTLS_P LATFORM_FPRINTF_MA CRO value	Manual Entry	fprintf	MBEDTLS_PLATFORM_F PRINTF_MACRO value
Platform > MBEDTLS_P LATFORM_PRINTF_MAC RO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_P RINTF_MACRO
Platform > MBEDTLS_P LATFORM_PRINTF_MAC RO value	Manual Entry	printf	MBEDTLS_PLATFORM_P RINTF_MACRO value
Platform > MBEDTLS_P LATFORM_SNPRINTF_M ACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_S NPRINTF_MACRO
Platform > MBEDTLS_P LATFORM_SNPRINTF_M ACRO value	Manual Entry	snprintf	MBEDTLS_PLATFORM_S NPRINTF_MACRO value
Platform > MBEDTLS_P LATFORM_VSNPRINTF_ MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_V SNPRINTF_MACRO
Platform > MBEDTLS_P LATFORM_VSNPRINTF_ MACRO value	Manual Entry	vsprintf	MBEDTLS_PLATFORM_V SNPRINTF_MACRO value
Platform > MBEDTLS_P LATFORM_NV_SEED_RE AD_MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_N V_SEED_READ_MACRO
Platform > MBEDTLS_P LATFORM_NV_SEED_RE AD_MACRO value	Manual Entry	MBEDTLS_PLATFORM_std_ nv_seed_read	MBEDTLS_PLATFORM_N V_SEED_READ_MACRO value
Platform > MBEDTLS_P ARAM_FAILED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PARAM_FAIL ED
Platform > MBEDTLS_P LATFORM_NV_SEED_W RITE_MACRO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PLATFORM_N V_SEED_WRITE_MACRO
Platform > MBEDTLS_P LATFORM_NV_SEED_W	Manual Entry	MBEDTLS_PLATFORM_std_ nv_seed_write	MBEDTLS_PLATFORM_N V_SEED_WRITE_MACRO

RITE_MACRO value			value
General > PSA_CRYPTO_SECURE	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	PSA_CRYPTO_SECURE
General > MBEDTLS_D EPRECATED_WARNING	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_DEPRECATED_WARNING
General > MBEDTLS_D EPRECATED_REMOVED	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_DEPRECATED_REMOVED
General > MBEDTLS_C HECK_PARAMS	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_CHECK_PARAMS
General > MBEDTLS_C HECK_PARAMS_ASSERT	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_CHECK_PARAMS_ASSERT
General > MBEDTLS_E RROR_STRERROR_DUM MY	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_ERROR_STRERROR_DUMMY
General > MBEDTLS_M EMORY_DEBUG	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_DEBUG
General > MBEDTLS_M EMORY_BACKTRACE	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_BACKTRACE
General > MBEDTLS_PS A_CRYPTO_SPM	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_SPM
General > MBEDTLS_SELF_TEST	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_SELF_TEST
General > MBEDTLS_T HREADING_ALT	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_THREADING_ALT
General > MBEDTLS_T HREADING_PTHREAD	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_THREADING_PTHREAD
General > MBEDTLS_U SE_PSA_CRYPTO	Undefine	Undefine	MBEDTLS_USE_PSA_CRYPTO
General > MBEDTLS_V ERSION_FEATURES	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_VERSION_FEATURES
General > MBEDTLS_ERROR_C	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_ERROR_C
General > MBEDTLS_M EMORY_BUFFER_ALLOC _C	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_MEMORY_BUFFER_ALLOC_C
General > MBEDTLS_PS A_CRYPTO_C	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_PSA_CRYPTO_C
General > MBEDTLS_PS A_CRYPTO_SE_C	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_SE_C
General > MBEDTLS_T HREADING_C	<ul style="list-style-type: none"> <li>Define</li> <li>Undefine</li> </ul>	Define	MBEDTLS_THREADING_C
General >	<ul style="list-style-type: none"> <li>Define</li> </ul>	Undefine	MBEDTLS_TIMING_C

MBEDTLS_TIMING_C	• Undefine		
General > MBEDTLS_VERSION_C	• Define • Undefine	Define	MBEDTLS_VERSION_C
General > MBEDTLS_M EMORY_ALIGN_MULTIPLE	• Define • Undefine	Undefine	MBEDTLS_MEMORY_ALI GN_MULTIPLE
General > MBEDTLS_M EMORY_ALIGN_MULTIPLE value	Manual Entry	4	MBEDTLS_MEMORY_ALI GN_MULTIPLE value
Cipher > Alternate > MBEDTLS_ARC4_ALT	• Define • Undefine	Undefine	MBEDTLS_ARC4_ALT
Cipher > Alternate > MBEDTLS_ARIA_ALT	• Define • Undefine	Undefine	MBEDTLS_ARIA_ALT
Cipher > Alternate > M BEDTLS_BLOWFISH_AL T	• Define • Undefine	Undefine	MBEDTLS_BLOWFISH_A LT
Cipher > Alternate > M BEDTLS_CAMELLIA_ALT	• Define • Undefine	Undefine	MBEDTLS_CAMELLIA_A LT
Cipher > Alternate > MBEDTLS_CCM_ALT	• Define • Undefine	Undefine	MBEDTLS_CCM_ALT
Cipher > Alternate > M BEDTLS_CHACHA20_AL T	• Define • Undefine	Undefine	MBEDTLS_CHACHA20_ ALT
Cipher > Alternate > M BEDTLS_CHACHAPOLY_ ALT	• Define • Undefine	Undefine	MBEDTLS_CHACHAPOL Y_ALT
Cipher > Alternate > MBEDTLS_CMAC_ALT	• Define • Undefine	Undefine	MBEDTLS_CMAC_ALT
Cipher > Alternate > MBEDTLS_DES_ALT	• Define • Undefine	Undefine	MBEDTLS_DES_ALT
Cipher > Alternate > MBEDTLS_GCM_ALT	MCU Specific Options		MBEDTLS_GCM_ALT
Cipher > Alternate > MBEDTLS_NIST_KW_AL T	• Define • Undefine	Undefine	MBEDTLS_NIST_KW_AL T
Cipher > Alternate > MBEDTLS_XTEA_ALT	• Define • Undefine	Undefine	MBEDTLS_XTEA_ALT
Cipher > Alternate > M BEDTLS_DES_SETKEY_A LT	• Define • Undefine	Undefine	MBEDTLS_DES_SETKEY _ALT
Cipher > Alternate > M BEDTLS_DES_CRYPT_E CB_ALT	• Define • Undefine	Undefine	MBEDTLS_DES_CRYPT_ ECB_ALT
Cipher > Alternate > M	• Define	Undefine	MBEDTLS_DES3_CRYPT

BEDTLS_DES3_CRYPT_E CB_ALT	• Undefine		_ECB_ALT
Cipher > AES > MBEDT LS_AES_ROM_TABLES	• Define • Undefine	Undefine	MBEDTLS_AES_ROM_TA BLES
Cipher > AES > MBEDT LS_AES_FEWER_TABLE S	• Define • Undefine	Undefine	MBEDTLS_AES_FEWER_ TABLES
Cipher > MBEDTLS_CA MELLIA_SMALL_MEMOR Y	• Define • Undefine	Undefine	MBEDTLS_CAMELLIA_S MALL_MEMORY
Cipher > MBEDTLS_CIP HER_MODE_CBC	• Define • Undefine	Define	MBEDTLS_CIPHER_MOD E_CBC
Cipher > MBEDTLS_CIP HER_MODE_CFB	• Define • Undefine	Define	MBEDTLS_CIPHER_MOD E_CFB
Cipher > MBEDTLS_CIP HER_MODE_CTR	• Define • Undefine	Define	MBEDTLS_CIPHER_MOD E_CTR
Cipher > MBEDTLS_CIP HER_MODE_OFB	• Define • Undefine	Undefine	MBEDTLS_CIPHER_MOD E_OFB
Cipher > MBEDTLS_CIP HER_MODE_XTS	• Define • Undefine	Undefine	MBEDTLS_CIPHER_MOD E_XTS
Cipher > MBEDTLS_CIP HER_NULL_CIPHER	• Define • Undefine	Undefine	MBEDTLS_CIPHER_NUL L_CIPHER
Cipher > MBEDTLS_CIP HER_PADDING_PKCS7	• Define • Undefine	Define	MBEDTLS_CIPHER_PAD DING_PKCS7
Cipher > MBEDTLS_CIP HER_PADDING_ONE_AN D_ZEROS	• Define • Undefine	Define	MBEDTLS_CIPHER_PAD DING_ONE_AND_ZEROS
Cipher > MBEDTLS_CIP HER_PADDING_ZEROS_ AND_LEN	• Define • Undefine	Define	MBEDTLS_CIPHER_PAD DING_ZEROS_AND_LEN
Cipher > MBEDTLS_CIP HER_PADDING_ZEROS	• Define • Undefine	Define	MBEDTLS_CIPHER_PAD DING_ZEROS
Cipher > MBEDTLS_AES_C	Define	Define	MBEDTLS_AES_C
Cipher > MBEDTLS_ARC4_C	• Define • Undefine	Undefine	MBEDTLS_ARC4_C
Cipher > MBEDTLS_BLOWFISH_C	• Define • Undefine	Undefine	MBEDTLS_BLOWFISH_C
Cipher > MBEDTLS_CAMELLIA_C	• Define • Undefine	Undefine	MBEDTLS_CAMELLIA_C
Cipher > MBEDTLS_ARIA_C	• Define • Undefine	Undefine	MBEDTLS_ARIA_C
Cipher >	• Define	Define	MBEDTLS_CCM_C

MBEDTLS_CCM_C	<ul style="list-style-type: none"> <li>• Undefine</li> </ul>		
Cipher > MBEDTLS_CHACHA20_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHA20_C
Cipher > MBEDTLS_CHACHAPOLY_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CHACHAPOLY_C
Cipher > MBEDTLS_CIPHER_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_CIPHER_C
Cipher > MBEDTLS_DES_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DES_C
Cipher > MBEDTLS_GCM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_GCM_C
Cipher > MBEDTLS_NIST_KW_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NIST_KW_C
Cipher > MBEDTLS_XTEA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_XTEA_C
Public Key Cryptography (PKC) > DHM > Alternate > MBEDTLS_DHM_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DHM_ALT
Public Key Cryptography (PKC) > DHM > MBEDTLS_DHM_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_DHM_C
Public Key Cryptography (PKC) > ECC > Alternate > MBEDTLS_ECJPAKE_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECJPAKE_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECDSA_GENKEY_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDSA_GENKEY_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_INTERNAL_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_INTERNAL_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_RANDOMIZE_JAC_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_RANDOMIZE_JAC_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_ADD_MIXED_ALT

DTLS_ECP_ADD_MIXED_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DOUBLE_JAC_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_DOUBLE_JAC_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_NORMALIZE_JAC_MANY_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_NORMALIZE_JAC_MANY_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_NORMALIZE_JAC_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_NORMALIZE_JAC_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DOUBLE_ADD_MXZ_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_DOUBLE_ADD_MXZ_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_RANDOMIZE_MXZ_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_RANDOMIZE_MXZ_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_NORMALIZE_MXZ_ALT
Public Key Cryptography (PKC) > ECC > Alternate > MBE DTLS_ECP_NORMALIZE_MXZ_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SECP192R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP192R1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SECP224R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP224R1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECP_DP_SECP256R1_ENABLED
Public Key Cryptography (PKC) > ECC > Curves > MBED TLS_ECP_DP_SECP256R1_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_DP_SECP384R1_ENABLED
Public Key Cryptography (PKC) >	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	

ECC > Curves > MBED  
 TLS\_ECP\_DP\_SECP384R  
 1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_SECP521R  
 1\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_SEC  
 P521R1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_SECP192K  
 1\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_SEC  
 P192K1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_SECP224K  
 1\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_SEC  
 P224K1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_SECP256K  
 1\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_SEC  
 P256K1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_BP256R1\_  
 ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_BP2  
 56R1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_BP384R1\_  
 ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_BP3  
 84R1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_BP512R1\_  
 ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_BP5  
 12R1\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_CURVE25  
 519\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_CUR  
 VE25519\_ENABLED

Public Key  
 Cryptography (PKC) >  
 ECC > Curves > MBED  
 TLS\_ECP\_DP\_CURVE44  
 8\_ENABLED

- Define
- Undefine

Undefine

MBEDTLS\_ECP\_DP\_CUR  
 VE448\_ENABLED

Public Key

- Define

Undefine

MBEDTLS\_ECDH\_GEN\_P

Cryptography (PKC) > ECC > MBEDTLS_ECDH _GEN_PUBLIC_ALT	<ul style="list-style-type: none"> <li>• Undefine</li> </ul>		UBLIC_ALT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH _COMPUTE_SHARED_AL T	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_COMP UTE_SHARED_ALT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_N IST_OPTIM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_NIST_OP TIM
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_R ESTARTABLE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_RESTAR TABLE
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH _LEGACY_CONTEXT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_LEGAC Y_CONTEXT
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDS A_DETERMINISTIC	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDSA_DETE RMINISTIC
Public Key Cryptography (PKC) > ECC > MBEDTLS_PK_PA RSE_EC_EXTENDED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PK_PARSE_E C_EXTENDED
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDSA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECDSA_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_ECP_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECJPAKE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECJPAKE_C
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ MAX_BITS	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_MAX_BI TS

Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ MAX_BITS value	Manual Entry	521	MBEDTLS_ECP_MAX_BITS value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ WINDOW_SIZE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_WINDOW_SIZE
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_ WINDOW_SIZE value	Manual Entry	6	MBEDTLS_ECP_WINDOW_SIZE value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_F IXED_POINT_OPTIM	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECP_FIXED_POINT_OPTIM
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECP_F IXED_POINT_OPTIM value	Manual Entry	1	MBEDTLS_ECP_FIXED_POINT_OPTIM value
Public Key Cryptography (PKC) > ECC > MBEDTLS_ECDH_ _VARIANT_EVEREST_ENABLED	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ECDH_VARIANT_EVEREST_ENABLED
Public Key Cryptography (PKC) > RSA > MBEDTLS_PK_RSA_ ALT_SUPPORT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PK_RSA_ALT_SUPPORT
Public Key Cryptography (PKC) > RSA > MBEDTLS_RSA_NO_CRT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RSA_NO_CRT
Public Key Cryptography (PKC) > RSA > MBEDTLS_RSA_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RSA_C
Public Key Cryptography (PKC) > MBEDTLS_GENPRIME	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_GENPRIME
Public Key Cryptography (PKC) > MBEDTLS_PKCS1_V15	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PKCS1_V15
Public Key Cryptography (PKC) > MBEDTLS_PKCS1_V21	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_PKCS1_V21
Public Key	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Define	MBEDTLS_ASN1_PARSE

Cryptography (PKC) > MBEDTLS_ASN1_PARSE_C	• Undefine		_C
Public Key Cryptography (PKC) > MBEDTLS_ASN1_WRITE_C	• Define • Undefine	Define	MBEDTLS_ASN1_WRITE_C
Public Key Cryptography (PKC) > MBEDTLS_BASE64_C	• Define • Undefine	Define	MBEDTLS_BASE64_C
Public Key Cryptography (PKC) > MBEDTLS_BIGNUM_C	• Define • Undefine	Define	MBEDTLS_BIGNUM_C
Public Key Cryptography (PKC) > MBEDTLS_OID_C	• Define • Undefine	Define	MBEDTLS_OID_C
Public Key Cryptography (PKC) > MBEDTLS_PEM_PARSE_C	• Define • Undefine	Define	MBEDTLS_PEM_PARSE_C
Public Key Cryptography (PKC) > MBEDTLS_PEM_WRITE_C	• Define • Undefine	Define	MBEDTLS_PEM_WRITE_C
Public Key Cryptography (PKC) > MBEDTLS_PK_C	• Define • Undefine	Define	MBEDTLS_PK_C
Public Key Cryptography (PKC) > MBEDTLS_PK_PARSE_C	• Define • Undefine	Define	MBEDTLS_PK_PARSE_C
Public Key Cryptography (PKC) > MBEDTLS_PK_WRITE_C	• Define • Undefine	Define	MBEDTLS_PK_WRITE_C
Public Key Cryptography (PKC) > MBEDTLS_PKCS5_C	• Define • Undefine	Define	MBEDTLS_PKCS5_C
Public Key Cryptography (PKC) > MBEDTLS_PKCS12_C	• Define • Undefine	Define	MBEDTLS_PKCS12_C
Public Key Cryptography (PKC) > MBEDTLS_MPI_WINDOW_SIZE	• Define • Undefine	Undefine	MBEDTLS_MPI_WINDOW_SIZE
Public Key Cryptography (PKC) > MBEDTLS_MPI_WINDOW_SIZE value	Manual Entry	6	MBEDTLS_MPI_WINDOW_SIZE value

Public Key Cryptography (PKC) > MBEDTLS_MPI_MAX_SIZ E	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MPI_MAX_SIZ E
Public Key Cryptography (PKC) > MBEDTLS_MPI_MAX_SIZ E value	Manual Entry	1024	MBEDTLS_MPI_MAX_SIZ E value
Hash > Alternate > MBEDTLS_MD2_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD2_ALT
Hash > Alternate > MBEDTLS_MD4_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD4_ALT
Hash > Alternate > MBEDTLS_MD5_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD5_ALT
Hash > Alternate > MB EDTLS_RIPEMD160_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_RIPEMD160_ ALT
Hash > Alternate > MBEDTLS_SHA1_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA1_ALT
Hash > Alternate > MBEDTLS_SHA512_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_ALT
Hash > Alternate > MB EDTLS_MD2_PROCESS_ ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD2_PROCE SS_ALT
Hash > Alternate > MB EDTLS_MD4_PROCESS_ ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD4_PROCE SS_ALT
Hash > Alternate > MB EDTLS_MD5_PROCESS_ ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD5_PROCE SS_ALT
Hash > Alternate > MB EDTLS_RIPEMD160_PR OCESS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_RIPEMD160_ PROCESS_ALT
Hash > Alternate > MB EDTLS_SHA1_PROCESS_ ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA1_PROCE SS_ALT
Hash > Alternate > MB EDTLS_SHA512_PROCE SS_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_PRO CESS_ALT
Hash > MBEDTLS_SHA2 56_SMALLER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA256_SMA LLER
Hash > MBEDTLS_SHA5 12_SMALLER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_SMA LLER
Hash > MBEDTLS_SHA5 12_NO_SHA384	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_NO_ SHA384

Hash > MBEDTLS_MD_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_MD_C
Hash > MBEDTLS_MD2_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD2_C
Hash > MBEDTLS_MD4_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_MD4_C
Hash > MBEDTLS_MD5_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_MD5_C
Hash > MBEDTLS_RIPEMD160_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_RIPEMD160_C
Hash > MBEDTLS_SHA1_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_SHA1_C
Hash > MBEDTLS_SHA256_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_SHA256_C
Hash > MBEDTLS_SHA512_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_SHA512_C
Message Authentication Code (MAC) > Alternate > M BEDTLS_POLY1305_ALT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_POLY1305_A LT
Message Authentication Code (MAC) > MBEDTLS_CMAC_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_CMAC_C
Message Authentication Code (MAC) > MBEDTLS_HKDF_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Define	MBEDTLS_HKDF_C
Message Authentication Code (MAC) > MBEDTLS_HM AC_DRBG_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG _C
Message Authentication Code (MAC) > MBEDTLS_POLY1305_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_POLY1305_C
RNG > MBEDTLS_TEST_ NULL_ENTROPY	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_TEST_NULL_ ENTROPY
RNG > MBEDTLS_NO_D EFAULT_ENTROPY_SOU RCES	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_NO_DEFAULT _ENTROPY_SOURCES
RNG > MBEDTLS_ENTR OPY_FORCE_SHA256	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_FO RCE_SHA256
RNG > MBEDTLS_ENTR	<ul style="list-style-type: none"> <li>• Define</li> </ul>	Undefine	MBEDTLS_ENTROPY_NV

OPY_NV_SEED	• Undefine		_SEED
RNG > MBEDTLS_PSA_I NJECT_ENTROPY	• Define • Undefine	Undefine	MBEDTLS_PSA_INJECT_ ENTROPY
RNG > MBEDTLS_CTR_DRBG_C	• Define • Undefine	Define	MBEDTLS_CTR_DRBG_C
RNG > MBEDTLS_CTR_ DRBG_C_ALT	Define	Define	MBEDTLS_CTR_DRBG_C _ALT
RNG > MBEDTLS_HAVEGE_C	• Define • Undefine	Undefine	MBEDTLS_HAVEGE_C
RNG > MBEDTLS_CTR_ DRBG_ENTROPY_LEN	• Define • Undefine	Undefine	RNG MBEDTLS_CTR_DR BG_ENTROPY_LEN
RNG > MBEDTLS_CTR_ DRBG_ENTROPY_LEN value	Manual Entry	48	RNG value MBEDTLS_C TR_DRBG_ENTROPY_LE N
RNG > MBEDTLS_CTR_ DRBG_RESEED_INTERV AL	• Define • Undefine	Undefine	RNG MBEDTLS_CTR_DR BG_RESEED_INTERVAL
RNG > MBEDTLS_CTR_ DRBG_RESEED_INTERV AL value	Manual Entry	10000	RNG value MBEDTLS_C TR_DRBG_RESEED_INT ERVAL
RNG > MBEDTLS_CTR_ DRBG_MAX_INPUT	• Define • Undefine	Undefine	MBEDTLS_CTR_DRBG_ MAX_INPUT
RNG > MBEDTLS_CTR_ DRBG_MAX_INPUT value	Manual Entry	256	MBEDTLS_CTR_DRBG_ MAX_INPUT value
RNG > MBEDTLS_CTR_ DRBG_MAX_REQUEST	• Define • Undefine	Undefine	MBEDTLS_CTR_DRBG_ MAX_REQUEST
RNG > MBEDTLS_CTR_ DRBG_MAX_REQUEST value	Manual Entry	1024	MBEDTLS_CTR_DRBG_ MAX_REQUEST value
RNG > MBEDTLS_CTR_ DRBG_MAX_SEED_INPU T	• Define • Undefine	Undefine	MBEDTLS_CTR_DRBG_ MAX_SEED_INPUT
RNG > MBEDTLS_CTR_ DRBG_MAX_SEED_INPU T value	Manual Entry	384	MBEDTLS_CTR_DRBG_ MAX_SEED_INPUT value
RNG > MBEDTLS_CTR_ DRBG_USE_128_BIT_KE Y	• Define • Undefine	Undefine	MBEDTLS_CTR_DRBG_U SE_128_BIT_KEY
RNG > MBEDTLS_HMAC _DRBG_RESEED_INTER VAL	• Define • Undefine	Undefine	MBEDTLS_HMAC_DRBG _RESEED_INTERVAL
RNG > MBEDTLS_HMAC _DRBG_RESEED_INTER	Manual Entry	10000	MBEDTLS_HMAC_DRBG _RESEED_INTERVAL

VAL value			value
RNG > MBEDTLS_HMAC_DRBG_MAX_INPUT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_INPUT
RNG > MBEDTLS_HMAC_DRBG_MAX_INPUT value	Manual Entry	256	MBEDTLS_HMAC_DRBG_MAX_INPUT value
RNG > MBEDTLS_HMAC_DRBG_MAX_REQUEST	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_REQUEST
RNG > MBEDTLS_HMAC_DRBG_MAX_REQUEST value	Manual Entry	1024	MBEDTLS_HMAC_DRBG_MAX_REQUEST value
RNG > MBEDTLS_HMAC_DRBG_MAX_SEED_INP UT	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT
RNG > MBEDTLS_HMAC_DRBG_MAX_SEED_INP UT value	Manual Entry	384	MBEDTLS_HMAC_DRBG_MAX_SEED_INPUT value
RNG > MBEDTLS_ENTROPY_MAX_SOURCES	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MAX_SOURCES
RNG > MBEDTLS_ENTROPY_MAX_SOURCES value	Manual Entry	20	MBEDTLS_ENTROPY_MAX_SOURCES value
RNG > MBEDTLS_ENTROPY_MAX_GATHER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MAX_GATHER
RNG > MBEDTLS_ENTROPY_MAX_GATHER value	Manual Entry	128	MBEDTLS_ENTROPY_MAX_GATHER value
RNG > MBEDTLS_ENTROPY_MIN_HARDWARE	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_ENTROPY_MIN_HARDWARE
RNG > MBEDTLS_ENTROPY_MIN_HARDWARE value	Manual Entry	32	MBEDTLS_ENTROPY_MIN_HARDWARE value
Storage > MBEDTLS_FS_IO	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_FS_IO
Storage > MBEDTLS_PSA_CRYPTO_KEY_ID_ENCODES_OWNER	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_KEY_ID_ENCODES_OWNER
Storage > MBEDTLS_PSA_CRYPTO_STORAGE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_CRYPTO_STORAGE_C
Storage > MBEDTLS_PSA_ITS_FILE_C	<ul style="list-style-type: none"> <li>• Define</li> <li>• Undefine</li> </ul>	Undefine	MBEDTLS_PSA_ITS_FILE_C

## SHA256 Configuration

To enable hardware acceleration for the SHA256/224 calculation, the macro `MBEDTLS_SHA256_ALT`

and MBEDTLS\_SHA256\_PROCESS\_ALT must be defined in the configuration file. By default SHA256 is enabled. SHA256 can be disabled, but SHA512 then needs to be enabled (software version) because the PSA implementation uses it for the entropy accumulator. This can be done using the RA Configuration editor.

## AES Configuration

To enable hardware acceleration for the AES128/256 operation, the macro MBEDTLS\_AES\_SETKEY\_ENC\_ALT, MBEDTLS\_AES\_SETKEY\_DEC\_ALT, MBEDTLS\_AES\_ENCRYPT\_ALT and MBEDTLS\_AES\_DECRYPT\_ALT must be defined in the configuration file. By default AES is enabled. AES cannot be disabled because the PSA implementation requires it for the CTR\_DRBG random number generator. This can be done using the RA Configuration editor.

## ECC Configuration

To enable hardware acceleration for the ECC Key Generation operation, the macro MBEDTLS\_ECP\_ALT must be defined in the configuration file. For ECDSA, the macros MBEDTLS\_ECDSA\_SIGN\_ALT and MBEDTLS\_ECDSA\_VERIFY\_ALT must be defined. By default ECC, ECDSA and ECDHE are enabled. To disable ECC, undefine MBEDTLS\_ECP\_C, MBEDTLS\_ECDSA\_C and MBEDTLS\_ECDH\_C. This can be done using the RA Configuration editor.

## RSA Configuration

To enable hardware acceleration for the RSA2048 operation, the macro MBEDTLS\_RSA\_ALT must be defined in the configuration file. By default RSA is enabled. To disable RSA, undefine MBEDTLS\_RSA\_C, MBEDTLS\_PK\_C, MBEDTLS\_PK\_PARSE\_C, MBEDTLS\_PK\_WRITE\_C. This can be done using the RA Configuration editor.

## Wrapped Key Usage

To use the Secure Crypto Engine to generate and use wrapped keys, use PSA\_KEY\_TYPE\_AES\_WRAPPED or PSA\_KEY\_TYPE\_ECC\_KEY\_PAIR\_WRAPPED(curve) or PSA\_KEY\_TYPE\_RSA\_KEY\_PAIR when setting the key type attribute. Setting the key's type attribute using this value will cause the SCE to use wrapped key mode for all operations related to that key. The user can use the export functionality to save the wrapped keys to user ROM and import it later for usage. This mode requires that Wrapped Key functionality for the algorithm is enabled in the project configuration.

*Note*

*On the SCE9 devices, only the RSA public key can be exported. A file system must be used to store the internally generated private key.*

## Persistent Key Storage

Persistent key storage can be enabled by defining MBEDTLS\_FS\_IO, MBEDTLS\_PSA\_CRYPTOSTORAGE\_C, and MBEDTLS\_PSA\_ITS\_FILE\_C. The key lifetime must also be specified as PSA\_KEY\_LIFETIME\_PERSISTENT. A lower level storage module must be added in the RA Configuration editor and initialized in the code before generating persistent keys. Persistent storage supports the use of plaintext and vendor keys. Refer to the lower level storage module documentation for information on how it should be initialized. To generate a persistent key the key must be assigned a unique id prior to calling generate using the psa\_set\_key\_id api.

```
if (PSA_KEY_LIFETIME_IS_PERSISTENT(lifetime))  
{
```

```

/* Set the id to a positive integer. */
    psa_set_key_id(&attributes, (psa_key_id_t) 5);
}

```

## Platform Configuration

To run the mbedCrypto implementation of the PSA Crypto API on the MCU, the macro `MBEDTLS_PLATFORM_SETUP_TEARDOWN_ALT` must be defined in the configuration file. This enables code that will initialize the SCE. Parameter checking (`General|MBEDTLS_CHECK_PARAMS`) is enabled by default. To reduce code size, disable parameter checking.

## Random Number Configuration

To run the mbedCrypto implementation of the PSA Crypto API on the MCU, the macro `MBEDTLS_ENTROPY_HARDWARE_ALT` must be defined in the configuration file. This enables using the TRNG as an entropy source. None of the other cryptographic operations (even in software only mode) will work without this feature.

## Usage Notes

### Hardware Initialization

`mbedtls_platform_setup()` must be invoked before using the PSA Crypto API to ensure that the SCE peripheral is initialized.

### Memory Usage

In general, depending on the mbedCrypto features being used a heap size of 0x1000 to 0x5000 bytes is required. The total allocated heap should be the **sum** of the heap requirements of the individual algorithms:

Algorithm	Required Heap (bytes)
SHA256/224	None
AES	0x200
Hardware ECC	0x400
Software ECC	0x1800
RSA	0x1500

A minimum stack of 0x1000 is required where the module is used. This is either the main stack in a bare metal application or the task stack of the task used for crypto operations.

### Limitations

- Only little endian mode is supported.

### SCE9 Usage

The crypto capabilities on the SCE9 are different resulting in the below usage limitations with mbedCrypto:

- The module includes **both** wrapped and plaintext keys code irrespective of whether the application requires it.
- Plaintext key generation is not supported for RSA and ECC; only wrapped keys can be generated.
- If ECDH is used, only wrapped key will be generated on SCE9 and will not return an error even if the user context is somehow set for plain key. This may be relevant only if the `psa_key_agreement()` function with plaintext key on SCE9 is attempted.

## Using PSA Crypto with TrustZone

Unlike FSP drivers, PSA Crypto cannot be configured as Non-secure callable in the RA Configurator for a secure project. The reason for this is that in order to achieve the security objective of controlling access to protected keys, both the PSA Crypto code as well as the keys must be placed in the secure region. Since the PSA Crypto API requires access to the keys directly during initialization and later via a key handle, allowing non-secure code to use the API by making it Non-secure callable will require the keys to be stored in non-secure memory.

This section will provide a short explanation of how to add PSA Crypto to a secure project and have it usable by the non-secure project without exposing the keys. In this example the secure project will contain an RSA private key and the non-secure project is expected to be able to perform sign and verify operations using that key.

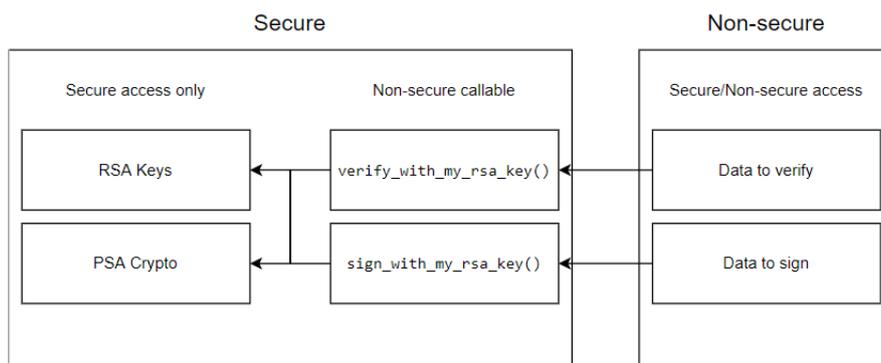


Figure 197: PSA Crypto Non-secure callable example

- Secure project
  - During secure project boot-up, `psa_crypto_init()` is called.
  - The RSA private key is programmed into secure flash either at the factory or by calling `psa_generate_key()` in persistent mode. Note that the data-flash area used by the LittleFS will have to be in the secure region if the key is generated as a persistent.
  - `psa_import_key()/psa_open_key()` are called with the resultant handle held in secure RAM.
  - The Non-secure callable section contains the following **user-defined** functions
    - `verify_with_my_rsa_key(input_signature, input_hash, verification_result)`
      - The implementation of this function in secure region will call `psa_verify_hash()` and return the result via `verification_result`.
    - `sign_with_my_rsa_key(input_hash, output_signature)`
      - The implementation of this function in secure region will call `psa_sign_hash()` and return the signature via `output_signature`.

- Non-secure project
  - Calls `verify_with_my_rsa_key()` to verify a signature. The implementation will use the public key that is present in the secure project.
  - Calls `sign_with_my_rsa_key()` to generate a signature. The implementation will use the private key that is present on the secure project.

For more details on how to add user-code to the Non-secure callable region refer to the "Security Design with Arm TrustZone - IP Protection (R11AN0467EU0100)" Application Note.

## Examples

### Hash Example

This is an example on calculating the SHA256 hash using the PSA Crypto API.

```
const uint8_t NIST_SHA256ShortMsgLen200[] =
{
    0x2e, 0x7e, 0xa8, 0x4d, 0xa4, 0xbc, 0x4d, 0x7c, 0xfb, 0x46, 0x3e, 0x3f, 0x2c,
    0x86, 0x47, 0x05,
    0x7a, 0xff, 0xf3, 0xfb, 0xec, 0xec, 0xa1, 0xd2, 00
};
const uint8_t NIST_SHA256ShortMsgLen200_expected[] =
{
    0x76, 0xe3, 0xac, 0xbc, 0x71, 0x88, 0x36, 0xf2, 0xdf, 0x8a, 0xd2, 0xd0, 0xd2,
    0xd7, 0x6f, 0x0c,
    0xfa, 0x5f, 0xea, 0x09, 0x86, 0xbe, 0x91, 0x8f, 0x10, 0xbc, 0xee, 0x73, 0x0d,
    0xf4, 0x41, 0xb9
};
void psa_crypto_sha256_example (void)
{
    psa_algorithm_t      alg                = PSA_ALG_SHA_256;
    psa_hash_operation_t operation         = {0};
    size_t               expected_hash_len = PSA_HASH_SIZE(alg);
    uint8_t              actual_hash[PSA_HASH_MAX_SIZE];
    size_t               actual_hash_len;
    mbedtls_platform_context ctx = {0};
    /* Setup the platform; initialize the SCE and the TRNG */
```

```
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
/* Platform initialization failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_hash_setup(&operation, alg))
{
/* Hash setup failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_hash_update(&operation, NIST_SHA256ShortMsgLen200,
sizeof(NIST_SHA256ShortMsgLen200)))
{
/* Hash calculation failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_hash_finish(&operation, &actual_hash[0], sizeof
(actual_hash), &actual_hash_len))
{
/* Reading calculated hash failed */
    debugger_break();
}
else if (0 != memcmp(&actual_hash[0], &NIST_SHA256ShortMsgLen200_expected[0],
actual_hash_len))
{
/* Hash compare of calculated value with expected value failed */
    debugger_break();
}
else if (0 != memcmp(&expected_hash_len, &actual_hash_len, sizeof
(expected_hash_len)))
{
/* Hash size compare of calculated value with expected value failed */
    debugger_break();
}
```

```
else
{
/* SHA256 calculation succeeded */
    debugger_break();
}

/* De-initialize the platform. This is currently a placeholder function which does
not do anything. */
mbedtls_platform_teardown(&ctx);
}
```

## AES Example

This is an example on using the PSA Crypto API to generate an AES256 key, encrypting and decrypting multi-block data and using PKCS7 padding.

```
static psa_status_t cipher_operation (psa_cipher_operation_t * operation,
const uint8_t      * input,
size_t             input_size,
size_t             part_size,
uint8_t            * output,
size_t             output_size,
size_t             * output_len)
{
    psa_status_t status;
    size_t      bytes_to_write = 0;
    size_t      bytes_written = 0;
    size_t      len            = 0;
    *output_len = 0;
    while (bytes_written != input_size)
    {
        bytes_to_write = (input_size - bytes_written > part_size ?
            part_size :
            input_size - bytes_written);
        status = psa_cipher_update(operation,
            input + bytes_written,
```

```
        bytes_to_write,
        output + *output_len,
        output_size - *output_len,
        &len);

if (PSA_SUCCESS != status)
{
return status;
}

bytes_written += bytes_to_write;
*output_len += len;
}

status = psa_cipher_finish(operation, output + *output_len, output_size -
*output_len, &len);
if (PSA_SUCCESS != status)
{
return status;
}

*output_len += len;
return status;
}

void psa_crypto_aes256cbcmultipart_example (void)
{
enum
{
    block_size = PSA_BLOCK_CIPHER_BLOCK_SIZE(PSA_KEY_TYPE_AES),
    key_bits    = 256,
    input_size  = 100,
    part_size   = 10,
};

mbedtls_platform_context ctx          = {0};
const psa_algorithm_t    alg          = PSA_ALG_CBC_PKCS7;
    psa_cipher_operation_t operation_1 = PSA_CIPHER_OPERATION_INIT;
    psa_cipher_operation_t operation_2 = PSA_CIPHER_OPERATION_INIT;
size_t iv_len = 0;
```

```
    psa_key_handle_t    key_handle        = 0;
size_t                encrypted_length = 0;
size_t                decrypted_length = 0;
uint8_t               iv[block_size]    = {0};
uint8_t               input[input_size] = {0};
uint8_t               encrypted_data[input_size + block_size] = {0};
uint8_t               decrypted_data[input_size + block_size] = {0};
psa_key_attributes_t  attributes = PSA_KEY_ATTRIBUTES_INIT;
psa_key_lifetime_t    lifetime;

/* Setup the platform; initialize the SCE */
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
    /* Platform initialization failed */
    debugger_break();
}
if (PSA_SUCCESS != psa_crypto_init())
{
    /* PSA Crypto Initialization failed */
    debugger_break();
}
/* Set key attributes */
psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_ENCRYPT |
PSA_KEY_USAGE_DECRYPT);
psa_set_key_algorithm(&attributes, alg);
/* To use wrapped keys instead of plaintext use PSA_KEY_TYPE_AES_WRAPPED. */
psa_set_key_type(&attributes, PSA_KEY_TYPE_AES);
psa_set_key_bits(&attributes, key_bits);
lifetime = PSA_KEY_LIFETIME_VOLATILE;
/* To use persistent keys:
*.....Use a lifetime value of PSA_KEY_LIFETIME_PERSISTENT
* - The file system must be initialized prior to calling the generate/import key
functions.
* - Refer to the littlefs example to see how to format and mount the filesystem. */
psa_set_key_lifetime(&attributes, lifetime);
```

```
if (PSA_KEY_LIFETIME_IS_PERSISTENT(lifetime))
{
/* Set the id to a positive integer. */
    psa_set_key_id(&attributes, (psa_key_id_t) 5);
}

if (PSA_SUCCESS != psa_generate_random(input, sizeof(input)))
{
/* Random number generation for input data failed */
    debugger_break();
}

else if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
{
/* Generating AES 256 key and allocating to key slot failed */
    debugger_break();
}

else if (PSA_SUCCESS != psa_cipher_encrypt_setup(&operation_1, key_handle, alg))
{
/* Initializing the encryption (with PKCS7 padding) operation handle failed */
    debugger_break();
}

else if (PSA_SUCCESS != psa_cipher_generate_iv(&operation_1, iv, sizeof(iv),
&iv_len))
{
/* Generating the random IV failed */
    debugger_break();
}

else if (PSA_SUCCESS !=
        cipher_operation(&operation_1, input, input_size, part_size,
encrypted_data, sizeof(encrypted_data),
                        &encrypted_length))
{
/* Encryption failed */
    debugger_break();
}
```

```
else if (PSA_SUCCESS != psa_cipher_abort(&operation_1))
{
/* Terminating the encryption operation failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_cipher_decrypt_setup(&operation_2, key_handle, alg))
{
/* Initializing the decryption (with PKCS7 padding) operation handle failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_cipher_set_iv(&operation_2, iv, sizeof(iv)))
{
/* Setting the IV failed */
    debugger_break();
}
else if (PSA_SUCCESS !=
        cipher_operation(&operation_2, encrypted_data, encrypted_length,
part_size, decrypted_data,
sizeof(decrypted_data), &decrypted_length))
{
/* Decryption failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_cipher_abort(&operation_2))
{
/* Terminating the decryption operation failed */
    debugger_break();
}
else if (0 != memcmp(input, decrypted_data, sizeof(input)))
{
/* Comparing the input data with decrypted data failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_destroy_key(key_handle))
```

```
{
/* Destroying the key handle failed */
    debugger_break();
}
else
{
/* All the operations succeeded */
}
/* Close the SCE */
mbedtls_platform_teardown(&ctx);
}
```

### AES-CCM Example

This is an example on using the PSA Crypto API to generate an AES256 key, encrypting and decrypting multi-block data and using PKCS7 padding using AES-CCM.

```
if (PSA_SUCCESS != psa_generate_random(input, sizeof(input)))
{
/* Random plaintext input generation failed */
    debugger_break();
}
else if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
{
/* Key generation failed */
    debugger_break();
}
/* AES-CCM Encryption */
else if (PSA_SUCCESS !=
        psa_aead_encrypt(key_handle, PSA_ALG_CCM, nonce, sizeof(nonce),
additional_data, sizeof(additional_data),
        input, sizeof(input), encrypt, sizeof(encrypt),
&output_len))
{
/* AES-CCM Encryption failed */
```

```
        debugger_break();
    }
    /* AES-CCM Decryption */
    else if (PSA_SUCCESS !=
             psa_aead_decrypt(key_handle, PSA_ALG_CCM, nonce, sizeof(nonce),
                             additional_data, sizeof(additional_data),
                             encrypt, output_len, decrypt, sizeof(decrypt),
                             &output_len))
    {
        /* AES-CCM Decryption failed */
        debugger_break();
    }
    else if (0U != memcmp(input, decrypt, sizeof(input)))
    {
        /* The decrypted result did not match the plaintext input */
        debugger_break();
    }
    else
    {
        /* All operations were successful */
    }
}
```

## CMAC Example

This is an example on using the PSA Crypto API to generate an AES256 key, followed by generation and verification of MAC for random data of known length.

```
if (PSA_SUCCESS != psa_generate_random(input, sizeof(input)))
{
    /* Random number generation failure */
    debugger_break();
}
else if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
{
    /* Key generation failure */
}
```

```
        debugger_break();
    }

    /* Steps to generate the MAC */
    else if (PSA_SUCCESS != psa_mac_sign_setup(&operation, key_handle, alg))
    {
        /* MAC Sign setup failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_mac_update(&operation, input, input_size))
    {
        /* MAC update failed */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_mac_sign_finish(&operation, AES_CMAC_mac, sizeof
(AES_CMAC_mac), &mac_ret))
    {
        /* MAC Sign operation failed */
        debugger_break();
    }
    else
    {
        /* All the operations succeeded for MAC generation */
    }

    /* Steps to verify the generated MAC */
    if (PSA_SUCCESS != psa_mac_verify_setup(&verify_operation, key_handle, alg))
    {
        /* MAC verification setup failure */
        debugger_break();
    }
    else if (PSA_SUCCESS != psa_mac_update(&verify_operation, input, input_size))
    {
        /* MAC update failure */
        debugger_break();
    }
}
```

```
else if (PSA_SUCCESS != psa_mac_verify_finish(&verify_operation, AES_CMAC_mac,
mac_ret))
{
/* MAC verification failed */
    debugger_break();
}
else
{
/* All the operations succeeded for MAC verification */
}
}
```

## ECC Example

This is an example on using the PSA Crypto API to generate an ECC-P256R1 key, signing and verifying data after hashing it first using SHA256.

### Note

*Unlike RSA, ECDSA does not have any padding schemes. Thus the hash argument for the ECC sign operation MUST have a size larger than or equal to the curve size; i.e. for PSA\_ECC\_CURVE\_SECP256R1 the payload size must be at least 256/8 bytes. nist.fips.186-4: "A hash function that provides a lower security strength than the security strength associated with the bit length of 'n' ordinarily should not be used, since this would reduce the security strength of the digital signature process to a level no greater than that provided by the hash function."*

```
#define ECC_256_BIT_LENGTH 256
#define ECC_256_EXPORTED_SIZE 500
uint8_t exportedECC_SECP256R1Key[ECC_256_EXPORTED_SIZE];
size_t exportedECC_SECP256R1Keylength = 0;
void psa_ecc256r1_example (void)
{
/* This example generates an ECC-P256R1 keypair, performs signing and verification
operations.
* It then exports the generated key into ASN1 DER format to a RAM array which can
then be programmed to flash.
* It then re-exports that key, and performs signing and verification operations. */
unsigned char    payload[] = "ASYMMETRIC_INPUT_FOR_SIGN.....";
unsigned char    signature1[PSA_SIGNATURE_MAX_SIZE] = {0};
unsigned char    signature2[PSA_SIGNATURE_MAX_SIZE] = {0};
size_t          signature_length1 = 0;
```

```
size_t          signature_length2 = 0;
psa_key_attributes_t  attributes      = PSA_KEY_ATTRIBUTES_INIT;
psa_key_attributes_t  read_attributes = PSA_KEY_ATTRIBUTES_INIT;
mbedtls_platform_context ctx          = {0};
psa_key_handle_t      ecc_key_handle  = {0};
psa_hash_operation_t hash_operation = {0};
uint8_t              payload_hash[PSA_HASH_MAX_SIZE];
size_t              payload_hash_len;
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
    debugger_break();
}
if (PSA_SUCCESS != psa_crypto_init())
{
    debugger_break();
}
/* Set key attributes */
psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_SIGN_HASH |
PSA_KEY_USAGE_VERIFY_HASH | PSA_KEY_USAGE_EXPORT);
psa_set_key_algorithm(&attributes, PSA_ALG_ECDSA(PSA_ALG_SHA_256));
/* To use wrapped keys instead of plaintext:
* - Use PSA_KEY_TYPE_ECC_KEY_PAIR_WRAPPED(PSA_ECC_FAMILY_SECP_R1).*/
psa_set_key_type(&attributes, PSA_KEY_TYPE_ECC_KEY_PAIR(PSA_ECC_FAMILY_SECP_R1));
psa_set_key_bits(&attributes, ECC_256_BIT_LENGTH);
/* To use persistent keys instead of volatile:
* - Use PSA_KEY_LIFETIME_PERSISTENT.
* - The file system must be initialized prior to calling the generate/import key
functions.
* - Refer to the littlefs example to see how to format and mount the filesystem. */
psa_set_key_lifetime(&attributes, PSA_KEY_LIFETIME_VOLATILE);
/* Generate ECC P256R1 Key pair */
if (PSA_SUCCESS != psa_generate_key(&attributes, &ecc_key_handle))
{
    debugger_break();
}
```

```
    }

    /* Test the key information */
    if (PSA_SUCCESS != psa_get_key_attributes(ecc_key_handle, &read_attributes))
    {
        debugger_break();
    }

    /* Calculate the hash of the message */
    if (PSA_SUCCESS != psa_hash_setup(&hash_operation, PSA_ALG_SHA_256))
    {
        debugger_break();
    }

    if (PSA_SUCCESS != psa_hash_update(&hash_operation, payload, sizeof(payload)))
    {
        debugger_break();
    }

    if (PSA_SUCCESS !=
        psa_hash_finish(&hash_operation, &payload_hash[0], sizeof(payload_hash),
&payload_hash_len))
    {
        debugger_break();
    }

    /* Sign message using the private key
    * NOTE: The hash argument (payload_hash here) MUST have a size equal to the curve
size;
    * i.e. for SECP256R1 the payload size must be 256/8 bytes.
    * Similarly for SECP384R1 the payload size must be 384/8 bytes.
    * nist.fips.186-4: " A hash function that provides a lower security strength than
    * the security strength associated with the bit length of 'n' ordinarily should not
be used, since this
    * would reduce the security strength of the digital signature process to a level no
greater than that
    * provided by the hash function." */
    if (PSA_SUCCESS !=
        psa_sign_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
```

```
payload_hash_len, signature1,
sizeof(signature1), &signature_length1)
{
    debugger_break();
}
/* Verify the signature1 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature1,
                    signature_length1))
{
    debugger_break();
}
/* Export the key. The exported key can then be save to flash for later usage. */
if (PSA_SUCCESS !=
    psa_export_key(ecc_key_handle, exportedECC_SECP256R1Key, sizeof
(exportedECC_SECP256R1Key),
                    &exportedECC_SECP256R1Keylength))
{
    debugger_break();
}
/* Destroy the key and handle */
if (PSA_SUCCESS != psa_destroy_key(ecc_key_handle))
{
    debugger_break();
}
/* Import the previously exported key pair */
if (PSA_SUCCESS !=
    psa_import_key(&attributes, exportedECC_SECP256R1Key,
exportedECC_SECP256R1Keylength, &ecc_key_handle))
{
    debugger_break();
}
/* Sign message using the private key */
```

```

if (PSA_SUCCESS !=
    psa_sign_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature2,
sizeof(signature2), &signature_length2))
{
    debugger_break();
}
/* Verify signature2 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(ecc_key_handle, PSA_ALG_ECDSA(PSA_ALG_SHA_256), payload_hash,
payload_hash_len, signature2,
signature_length2))
{
    debugger_break();
}
/* Signatures cannot be compared since ECC signatures vary for the same data unless
Deterministic ECC is used which is not supported by the HW.
* Only the verification operation can be used to validate signatures. */
}

```

## RSA Example

This is an example on using the PSA Crypto API to generate an RSA2048 key, encrypting and decrypting multi-block data and using PKCS7 padding.

```

#define RSA_2048_BIT_LENGTH 2048
#define RSA_2048_EXPORTED_SIZE 1210
/* The RSA 2048 key pair export in der format is roughly as follows
* RSA private keys:
* RSAPrivateKey ::= SEQUENCE { ----- 1 + 3
* version Version, ----- 1 + 1 + 1
* modulus INTEGER, ----- n ----- 1 + 3 + 256 + 1
* publicExponent INTEGER, ----- e ----- 1 + 4
* privateExponent INTEGER, ----- d ----- 1 + 3 + 256 (276
for Wrapped)

```

```

* prime1 INTEGER, ----- p ----- 1 + 3 + (256 / 2)
* prime2 INTEGER, ----- q ----- 1 + 3 + (256 / 2)
* exponent1 INTEGER, ----- d mod (p-1) ----- 1 + 2 + (256 / 2) (4 for
Wrapped)
* exponent2 INTEGER, ----- d mod (q-1) ----- 1 + 2 + (256 / 2) (4 for
Wrapped)
* coefficient INTEGER, ----- (inverse of q) mod p - 1 + 2 + (256 / 2) (4
for Wrapped)
* otherPrimeInfos OtherPrimeInfos OPTIONAL ----- 0 (not
supported)
* }
*/

uint8_t exportedRSA2048Key[RSA_2048_EXPORTED_SIZE];
size_t exportedRSA2048Keylength = 0;
void psa_rsa2048_example (void)
{
/* This example generates an RSA2048 keypair, performs signing and verification
operations.

* It then exports the generated key into ASN1 DER format to a RAM array which can
then be programmed to flash.

* It then re-imports that key, and performs signing and verification operations. */
mbedtls_platform_context ctx          = {0};
    psa_key_handle_t          key_handle = {0};
unsigned char                payload[] = "ASYMMETRIC_INPUT_FOR_SIGN";
unsigned char                signature1[PSA_SIGNATURE_MAX_SIZE] = {0};
unsigned char                signature2[PSA_SIGNATURE_MAX_SIZE] = {0};
size_t                      signature_length1 = 0;
size_t                      signature_length2 = 0;
    psa_key_attributes_t attributes          = PSA_KEY_ATTRIBUTES_INIT;
    psa_key_attributes_t read_attributes    = PSA_KEY_ATTRIBUTES_INIT;
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
{
    debugger_break();
}
}

```

```
if (PSA_SUCCESS != psa_crypto_init())
{
    debugger_break();
}

/* Set key attributes */
psa_set_key_usage_flags(&attributes, PSA_KEY_USAGE_SIGN_HASH |
PSA_KEY_USAGE_VERIFY_HASH | PSA_KEY_USAGE_EXPORT);

psa_set_key_algorithm(&attributes, PSA_ALG_RSA_PKCS1V15_SIGN_RAW);

/* To use wrapped keys instead of plaintext:
* - Use PSA_KEY_TYPE_RSA_KEY_PAIR_WRAPPED. */
psa_set_key_type(&attributes, PSA_KEY_TYPE_RSA_KEY_PAIR);
psa_set_key_bits(&attributes, RSA_2048_BIT_LENGTH);

/* To use persistent keys instead of volatile:
* - Use PSA_KEY_LIFETIME_PERSISTENT.
* - The file system must be initialized prior to calling the generate/import key
functions.
* - Refer to the littlefs example to see how to format and mount the filesystem. */
psa_set_key_lifetime(&attributes, PSA_KEY_LIFETIME_VOLATILE);

/* Generate RSA 2048 Key pair */
if (PSA_SUCCESS != psa_generate_key(&attributes, &key_handle))
{
    debugger_break();
}

/* Test the key information */
if (PSA_SUCCESS != psa_get_key_attributes(key_handle, &read_attributes))
{
    debugger_break();
}

/* Sign message using the private key */
if (PSA_SUCCESS !=
    psa_sign_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload, sizeof
(payload), signature1,
sizeof(signature1), &signature_length1))
{
```

```
    debugger_break();
}

/* Verify the signature1 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload,
sizeof(payload), signature1,
                    signature_length1))
{
    debugger_break();
}

/* Export the key */
if (PSA_SUCCESS !=
    psa_export_key(key_handle, exportedRSA2048Key, sizeof(exportedRSA2048Key),
&exportedRSA2048Keylength))
{
    debugger_break();
}

/* Destroy the key and handle */
if (PSA_SUCCESS != psa_destroy_key(key_handle))
{
    debugger_break();
}

/* Import the previously exported key pair */
if (PSA_SUCCESS != psa_import_key(&attributes, exportedRSA2048Key,
exportedRSA2048Keylength, &key_handle))
{
    debugger_break();
}

/* Sign message using the private key */
if (PSA_SUCCESS !=
    psa_sign_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload, sizeof
(payload), signature2,
sizeof(signature2), &signature_length2))
{
```

```

    debugger_break();
}

/* Verify signature2 using the public key */
if (PSA_SUCCESS !=
    psa_verify_hash(key_handle, PSA_ALG_RSA_PKCS1V15_SIGN_RAW, payload,
sizeof(payload), signature2,
                    signature_length2))
{
    debugger_break();
}

/* Compare signatures to verify that the same signature was generated */
if (0 != memcmp(signature2, signature1, signature_length2))
{
    debugger_break();
}

mbedtls_psa_crypto_free();
mbedtls_platform_teardown(&ctx);
}

```

## Function Documentation

### ◆ RM\_PSA\_CRYPTO\_TRNG\_Read()

`fsp_err_t RM_PSA_CRYPTO_TRNG_Read ( uint8_t*const p_rngbuf, uint32_t num_req_bytes, uint32_t* p_num_gen_bytes )`

Reads requested length of random data from the TRNG. Generate nbytes of random bytes and store them in p\_rngbuf buffer.

#### Return values

FSP_SUCCESS	Random number generation successful
FSP_ERR_ASSERTION	NULL input parameter(s).
FSP_ERR_CRYPTO_UNKNOWN	An unknown error occurred.

#### Returns

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- s\_generate\_16byte\_random\_data

### ◆ mbedtls\_platform\_setup()

```
int mbedtls_platform_setup ( mbedtls_platform_context * ctx)
```

This function initializes the SCE and the TRNG. It **must** be invoked before the crypto library can be used. This implementation is used if MBEDTLS\_PLATFORM\_SETUP\_TEARDOWN\_ALT is defined.

Example:

```
mbedtls_platform_context ctx = {0};

/* Setup the platform; initialize the SCE and the TRNG */
if (PSA_SUCCESS != mbedtls_platform_setup(&ctx))
```

#### Return values

0	Initialization was successful.
MBEDTLS_ERR_PLATFORM_HW_ACCEL_FAILED	SCE Initialization error.

### ◆ mbedtls\_platform\_teardown()

```
void mbedtls_platform_teardown ( mbedtls_platform_context * ctx)
```

This implementation is used if MBEDTLS\_PLATFORM\_SETUP\_TEARDOWN\_ALT is defined. It is intended to de-initialize any items that were initialized in the `mbedtls_platform_setup()` function, but currently is only a placeholder function.

Example:

```
/* De-initialize the platform. This is currently a placeholder function which does
not do anything. */
mbedtls_platform_teardown(&ctx);
```

#### Return values

N/A	
-----	--

## 4.2.97 Azure RTOS ThreadX Port (rm\_threadx\_port)

### Modules

ThreadX port for RA MCUs.

## Overview

*Note*

*The ThreadX Port does not provide any interfaces to the user. Consult the ThreadX documentation at <https://docs.microsoft.com/en-us/azure/rtos/threadx/> for further information.*

**Features**

The RA ThreadX port supports the following features:

- Standard ThreadX configurations
- Hardware stack monitor

**Configuration****Build Time Configurations for ThreadX**

The following build time configurations are defined in fsp\_cfg/azure/tx/tx\_user.h:

Configuration	Options	Default	Description
General > Custom tx_user.h	Manual Entry		Add a path to your custom tx_user.h file. It can be used to override some or all of the configurations defined here, and to define additional configurations.
General > Error Checking	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	The ThreadX basic API error checking can be bypassed by compiling with the symbol TX_DISABLE_ERROR_CHECKING defined.
General > Max Priorities	Value must be a multiple of 32 or empty	32	Define the priority levels for ThreadX. Legal values range from 32 to 1024 and MUST be evenly divisible by 32.
General > Minimum Stack	Value must be greater than 0 or empty	200	Define the minimum stack for a ThreadX thread on this processor. If the size supplied during thread creation is less than this value, the thread create call will return an error.
General > Stack Filling	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Determine if stack filling is enabled. By default, ThreadX stack filling is enabled, which

General > Preemption Threshold	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>places an 0xEF pattern in each byte of each thread's stack. This is used by debuggers with ThreadX-awareness and by the ThreadX run-time stack checking feature.</p> <p>Determine if preemption-threshold should be disabled. By default, preemption-threshold is disabled. If the application does not use preemption-threshold, it may be disabled to reduce code size and improve performance.</p>
General > Notify Callbacks	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Determine if the notify callback option should be disabled. By default, notify callbacks are disabled. If the application does not use notify callbacks, they may be disabled to reduce code size and improve performance.</p>
General > Inline Thread Resume Suspend	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Determine if the tx_thread_resume and tx_thread_suspend services should have their internal code in-line. This results in a larger image, but improves the performance of the thread resume and suspend services.</p>
General > Not Interruptable	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Determine if the internal ThreadX code is non-interruptable. This results in smaller code size and less processing overhead, but increases the interrupt lockout time.</p>
General > IAR Library Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	<p>Enable IAR library support (IAR compiler only). When IAR Library</p>

Support is Enabled, enable the linker option `--threaded_lib`. In the IAR IDE, this can be enabled in Project > Options > General Options > Library Configuration > Enable thread support in library.

General > BSD Support	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Defines <code>TX_THREAD_EXTENSION_1</code> to <code>bsd_err_no</code> in order to support NXD BSD.
General > FileX Pointer	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Determine if there is a FileX pointer in the thread control block. By default, the pointer is there for legacy/backwards compatibility. The pointer must also be there for applications using FileX. Disable this to save space in the thread control block.
Timer > Timer Ticks Per Second	Value must be greater than 0 or empty	100	Define the number of times the system timer runs per second. Default is 100 ticks per second, which results in a tick every 10ms.
Timer > Timer Thread Stack Size	Value must be greater than 0 or empty	1024	Define the system timer thread's default stack size and priority. These are only applicable if <code>TX_TIMER_PROCESS_IN_ISR</code> is disabled.
Timer > Timer Thread Priority	Value must be greater than 0 or empty	0	Define the system timer thread's default stack size and priority. These are only applicable if <code>TX_TIMER_PROCESS_IN_ISR</code> is disabled.
Timer > Timer Process In ISR	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Determine if timer expirations (application timers, timeouts, and <code>tx_thread_sleep</code> calls should be processed

within the a system timer thread or directly in the timer ISR. When disabled, the timer thread is used. When enabled, timer expiration processing is done directly from the timer ISR, thereby eliminating the timer thread control block, stack, and context switching to activate it.

Timer > Reactivate Inline	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Determine if in-line timer reactivation should be used within the timer expiration processing. By default, this is disabled and a function call is used. When enabled, reactivating is performed in-line resulting in faster timer processing but slightly larger code size.
Timer > Timer	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Enabled	Determine if no timer processing is required. This option will help eliminate the timer processing when not needed.
Trace > Event Trace	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Determine if the trace event logging code should be enabled. This causes slight increases in code size and overhead, but provides the ability to generate system trace information which is available for viewing in TraceX.
Trace > Trace Buffer Name	Name must be a valid C symbol	g_tx_trace_buffer	Name of trace buffer symbol, only used if Event Trace is enabled.
Trace > Memory section for Trace Buffer	Manual Entry	.bss	Specify the memory section where the Trace Buffer will be allocated, only used if Event Trace is enabled. To view TraceX data,

export this buffer as raw binary data to a file (.trx extension recommended) and open it with Microsoft Azure RTOS TraceX.

Trace > Trace Buffer Size	Value must be greater than 0	65536	Trace buffer size in bytes, only used if Event Trace is enabled
Trace > Trace Buffer Number of Registries	Value must be greater than 0	30	Number of registries available to TraceX, only used if Event Trace is enabled
Performance > Block Pool Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers block pool performance information.
Performance > Byte Pool Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers byte pool performance information.
Performance > Event Flags Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers event flags performance information.
Performance > Mutex Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers mutex performance information.
Performance > Queue Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers queue performance information.
Performance > Semaphore Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers semaphore performance information.
Performance > Thread Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers thread performance information.
Performance > Timer Performance Info	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	When enabled, ThreadX gathers timer performance information.
RA > Hardware Thread Stack Monitoring	MCU Specific Options		Use RA Hardware Stack Monitors to monitor

thread stacks for overflow. Not available on MCUs that support PSPLIM.

Select the SysTick interrupt priority.

The maximum priority (lowest numerical value) an interrupt can have and use scheduler services. Interrupts with higher priority can interrupt most scheduler critical sections. Setting this to Priority 0 (highest) disables this feature. This feature is not available on MCUs that do not have the BASEPRI register.

Interrupts > SysTick Interrupt Priority      MCU Specific Options

Interrupts > Maximum Interrupt Priority      MCU Specific Options

## Clock Configuration

The ThreadX port uses the SysTick timer as the system clock. The timer rate is configured in the ThreadX component under General > Timer Ticks Per Second.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

### Interrupt Priorities

When no threads are ready to run, the ThreadX port spins in the PendSV\_Handler, which is fixed at the lowest interrupt priority. The MCU does not service any other interrupts of the lowest priority while no threads are ready to run.

To get around this limitation, the application can create an idle thread that is always ready to run. If the idle thread enters a lower power mode, make sure all interrupts that are required to resume the scheduler can wake the MCU in the configured power mode. If the application expects to wake after a certain number of ticks, the idle thread should not enter standby mode because the SysTick cannot wake the MCU from standby mode. See [Low Power Modes \(r\\_lpm\)](#) for more information regarding low power modes.

#### Warning

Do not attempt to wake a thread from an interrupt with the lowest available interrupt priority unless the application has created an idle thread.

## Hardware Stack Monitor

The hardware stack monitor generates an NMI if the PSP goes out of the memory area for the stack

allocated for the current thread. A callback can be registered using `R_BSP_GroupIrqWrite()` to be called whenever a stack overflow or underflow of the PSP for a particular thread is detected.

## Low Power Modes

The idle processing executes `WFI()` when no thread is ready to run. If the MCU is configured to enter software standby mode or deep software standby mode when the idle processing executes `WFI()`, the RA ThreadX port changes the low power mode to sleep mode so the idle processing can wake from `SysTick`. The low power mode settings are restored when the MCU wakes from sleep mode.

## TrustZone Integration

When using an RTOS in a TrustZone project, ARM recommends keeping the RTOS in the non-secure project. Tasks may call non-secure callable functions if the thread has allocated a secure context (using `tx_thread_secure_stack_allocate`).

The secure context can be freed by deleting the thread or calling `tx_thread_secure_stack_free`.

## Examples

### Stack Monitor Example

This is an example of using the stack monitor in an application.

```
#if BSP_FEATURE_BSP_HAS_SP_MON
void stack_monitor_callback(bsp_grp_irq_t irq);
void stack_monitor_callback (bsp_grp_irq_t irq)
{
    FSP_PARAMETER_NOT_USED(irq);
    if (1U == R_MPU_SPMON->SP[0].CTL_b.ERROR)
    {
        /* Handle main stack monitor error here. */
    }
    if (1U == R_MPU_SPMON->SP[1].CTL_b.ERROR)
    {
        /* Handle process stack monitor error here. */
    }
}
void rm_threadx_port_stack_monitor_example (void)
{
    /* Register a callback to be called when the stack goes outside the allocated stack
area. */
    R_BSP_GroupIrqWrite(BSP_GRP_IRQ_MPU_STACK, stack_monitor_callback);
}
```

```
}
#else
/* Allocate stack space to return from UsageFault. */
uint32_t g_stack_overflow_exception_stack[8] BSP_ALIGN_VARIABLE(BSP_STACK_ALIGNMENT)
BSP_PLACE_IN_SECTION(
    BSP_SECTION_STACK);
/* MCUs that do not have an SPMON stack monitor use PSPLIM to detect stack overflows.
When a stack overflow error
* occurs, the UsageFault_Handler fires if it has been enabled. */
void UsageFault_Handler (void)
{
    register uint32_t cfsr = SCB->CFSR;
    if (cfsr & SCB_CFSR_STKOF_Msk)
    {
        /* Update PSP and PSPLIM to point to an exception stack frame allocated for stack
overflows. */
        register uint32_t * p_exception_stack_frame = (uint32_t *)
(&g_stack_overflow_exception_stack);
        __set_PSP((uint32_t) p_exception_stack_frame);
        __set_PSPLIM((uint32_t) p_exception_stack_frame);
        /* Clear XPSR, only set T-bit. */
        p_exception_stack_frame[7] = 1U << 24;
        /* Set PC to stack overflow error while loop. When execution returns from the
UsageFault, it will go to the
* stack_overflow_error_occurred function. It cannot return to the location where
the fault occurred because
* the MCU does not save the exception stack frame to the stack when a stack
overflow error occurs. */
        p_exception_stack_frame[6] = (uint32_t) stack_overflow_error_occurred;
    }
    /* Clear flags. */
    SCB->CFSR = cfsr;
}
/* This function is called from UsageFault_Handler after a stack overflow occurs. */
```

```
void stack_overflow_error_occurred (void)
{
    /* When recovering from a stack overflow, move the thread to a while(1) loop. */
    while (1)
    {
        /* Do nothing. */
    }
}

void rm_threadx_port_stack_monitor_example (void)
{
    /* Enable usage fault. */
    SCB->SHCSR |= SCB_SHCSR_USGFAULTENA_Msk;
}

#endif
```

## TrustZone Example

This is an example of calling `tx_thread_secure_stack_allocate` before calling any non-secure callable functions in a thread.

```
extern TX_THREAD * _tx_thread_current_ptr;

void rm_threadx_port_trustzone_thread_example (void)
{
    /* When ThreadX is used in a non-secure TrustZone application,
    tx_thread_secure_stack_allocate must be called prior
    * to calling any non-secure callable function in a thread. The first parameter is a
    pointer to the thread control block.
    * This function can be called when the thread is created or in the thread before an
    non-secure callable function is
    * called. The second parameter is unused in the FSP implementation. */
    UINT status = tx_thread_secure_stack_allocate(_tx_thread_current_ptr, 0);
    assert(TX_SUCCESS == status);
    rm_threadx_port_nsc_function();
}
```

## 4.2.98 Intel TinyCrypt (rm\_tinycrypt\_port)

### Modules

#### Functions

`fsp_err_t` `RM_TINCRYPT_PORT_TRNG_Read` (uint8\_t \*const p\_rngbuf, uint32\_t num\_req\_bytes)

Reads requested length of random data from the TRNG. Generate num\_req\_bytes of random bytes and store them in p\_rngbuf buffer. [More...](#)

`fsp_err_t` `RM_TINCRYPT_PORT_Init` (void)

`int` `default_CSPRNG` (uint8\_t \*dest, unsigned int size)

Implements the Cryptographically Secure Pseudo-Random Number Generator function required by TinyCrypt. [More...](#)

### Detailed Description

AES128 Hardware acceleration for TinyCrypt on the RA2 family.

## Overview

#### Note

*The TinyCrypt port module does not provide any interfaces to the user. Consult the documentation at <https://github.com/intel/tinycrypt/blob/master/documentation/tinycrypt.rst> for further information.*

TinyCrypt is designed as a small footprint software crypto implementation to be used on resource constrained devices. The software only module is available in FSP on all RA devices. Hardware acceleration for AES-128 is provided only for the RA2 family. This release uses TinyCrypt v0.2.8.

### Hardware Overview

Crypto Peripheral version	Devices
AES Engine	RA2A1, RA2E1, RA2L1

### Features

For features supported by the software-only version, refer to the TinyCrypt documentation.

The TinyCrypt port module provides hardware support for the following operations

- AES
  - Keybits - 128
  - ECB, CBC, CTR, CCM and CMAC modes -TRNG

# Configuration

## Build Time Configurations for TinyCrypt\_Acceleration

The following build time configurations are defined in fsp\_cfg/rm\_tinycrypt\_port\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

## AES Configuration

To enable hardware acceleration for the AES128 operation, choose TinyCrypt (H/W Accelerated) from the stack options . This feature is only supported on the RA2 family.

# Usage Notes

## Hardware Initialization

Invoke `RM_TINCRYPT_PORT_Init ()` to initialize the hardware before using TinyCrypt if either hardware acceleration or the TRNG is to be used.

## Random Number Generation

There are two Pseudo-random Number Generators (PRNG) provided in TinyCrypt

- CTR-PRNG which uses AES128 internally in its implementation. Enabling AES128 hardware acceleration will improve the performance of this module.
- HMAC-PRNG which uses SHA256 internally in its implementation.

**Both these implementations will only be able to provide a random pseudo-random number sequence if they are seeded with truly random data. The TRNG module that is present in hardware and available in `rm_tinycrypt_port` must be used to seed these modules.** When using CTR-PRNG or HMAC-PRNG, use the `RM_TINCRYPT_PORT_TRNG_Read()` function to obtain random data from the TRNG hardware and use that to seed the PRNG modules before invoking the pseudo-random number generation. If purely random data is sufficient for the application, then `RM_TINCRYPT_PORT_TRNG_Read()` can be used directly instead. The hardware TRNG implements the CTR\_DRBG spec.

## Default CSPRNG

The TinyCrypt ECC implementation requires a platform specific implementation of the `default_CSPRNG()` function. This function has been implemented using the hardware TRNG in the port to support software ECC usage. When using TinyCrypt in S/W mode, it is necessary to implement `default_CSPRNG()` if using ECC signature generation (ECDSA) or key derivation (ECDH).

## AES-128 Usage

The AES ECB mode implementation is provided in `aes_encrypt.decrypt.c`. All the other modes of AES operation including CBC, CCN, CMAC and CTR use the ECB mode for the block operation. On the RA2, the ECB mode has been hardware accelerated which improves performance of the other modes as well. Additionally the CBC mode has also been accelerated.

To use the different AES modes, first initialize the hardware (on the RA2) and then use the functions defined in the header file of each AES mode. Note that TinyCrypt does not provide any type of padding or buffering so the data provided to these modes should be multiples of AES block size.

## Memory Usage

TinyCrypt does not use dynamic allocation so there is no heap requirement.

## Limitations

### Usage with RA4 and RA6 devices

TinyCrypt (S/W Only) can be used on RA4 and RA6 devices. However, since ECC signature generation (ECDSA) and key derivation (ECDH) requires a random number source, that operation is currently not supported on these devices when using TinyCrypt (S/W Only). In order to support those operations the function `default_CSPRNG()` must be implemented in the user code.

## TinyCrypt

- No padding is supported; the user is expected to provide adequately padded data depending on the algorithm used.
- AES Key generation is not supported.
- Key encoding/decoding is not supported.

## TinyCrypt Port

- AES CTR is currently only partially hardware accelerated.

## Using TinyCrypt with TrustZone

Unlike FSP drivers, TinyCrypt cannot be configured as Non-secure callable in the RA Configurator for a secure project. The reason for this is that in order to achieve the security objective of controlling access to protected keys, both the crypto code as well as the keys must be placed in the secure region. Since the tinyCrypt API requires access to the keys directly during initialization and later via a key handle, allowing non-secure code to use the API by making it Non-secure callable will require the keys to be stored in non-secure memory.

This limitation is identical to that for PSA Crypto. Refer to the documentation of that module on how to create a crypto Non-Secure Callable layer to be used in such situations.

# Examples

## AES-CBC Example

This is an example on using TinyCrypt to encrypt and decrypt data using an AES-128 key in CBC mode.

```
#define TC_INPUT_PLAINTEXT_SIZE 64U
#define TF_AES_IV_SIZE TC_AES_BLOCK_SIZE
#define TC_OUTPUT_CIPHERTEXT_SIZE (TC_INPUT_PLAINTEXT_SIZE + TF_AES_IV_SIZE)
/*
 * NIST test vectors from SP 800-38a:
```

```
*
* Block #1
* Plaintext 6bc1bee22e409f96e93d7e117393172a
* Input Block 6bc0bce12a459991e134741a7f9e1925
* Output Block 7649abac8119b246cee98e9b12e9197d
* Ciphertext 7649abac8119b246cee98e9b12e9197d
* Block #2
* Plaintext ae2d8a571e03ac9c9eb76fac45af8e51
* Input Block d86421fb9f1a1eda505ee1375746972c
* Output Block 5086cb9b507219ee95db113a917678b2
* Ciphertext 5086cb9b507219ee95db113a917678b2
* Block #3
* Plaintext 30c81c46a35ce411e5fbc1191a0a52ef
* Input Block 604ed7ddf32efdff7020d0238b7c2a5d
* Output Block 73bed6b8e3c1743b7116e69e22229516
* Ciphertext 73bed6b8e3c1743b7116e69e22229516
* Block #4
* Plaintext f69f2445df4f9b17ad2b417be66c3710
* Input Block 8521f2fd3c8eef2cdc3da7e5c44ea206
* Output Block 3ff1caa1681fac09120eca307586e1a7
* Ciphertext 3ff1caa1681fac09120eca307586e1a7
*/
const uint8_t cbc_key[TC_AES_KEY_SIZE] =
{
    0x2b, 0x7e, 0x15, 0x16, 0x28, 0xae, 0xd2, 0xa6, 0xab, 0xf7, 0x15, 0x88, 0x09,
    0xcf, 0x4f, 0x3c
};
uint8_t cbc_iv[TC_AES_KEY_SIZE] =
{
    0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0a, 0x0b, 0x0c,
    0x0d, 0x0e, 0x0f
};
const uint8_t cbc_plaintext[64] =
{
```

```
    0x6b, 0xc1, 0xbe, 0xe2, 0x2e, 0x40, 0x9f, 0x96, 0xe9, 0x3d, 0x7e, 0x11, 0x73,
0x93, 0x17, 0x2a,
    0xae, 0x2d, 0x8a, 0x57, 0x1e, 0x03, 0xac, 0x9c, 0x9e, 0xb7, 0x6f, 0xac, 0x45,
0xaf, 0x8e, 0x51,
    0x30, 0xc8, 0x1c, 0x46, 0xa3, 0x5c, 0xe4, 0x11, 0xe5, 0xfb, 0xc1, 0x19, 0x1a,
0x0a, 0x52, 0xef,
    0xf6, 0x9f, 0x24, 0x45, 0xdf, 0x4f, 0x9b, 0x17, 0xad, 0x2b, 0x41, 0x7b, 0xe6,
0x6c, 0x37, 0x10
};
uint8_t cbc_expected_ciphertext[TC_OUTPUT_CIPHERTEXT_SIZE] =
{
    0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0a, 0x0b, 0x0c,
0x0d, 0x0e, 0x0f, // NOLINT(readability-magic-numbers)
    0x76, 0x49, 0xab, 0xac, 0x81, 0x19, 0xb2, 0x46, 0xce, 0xe9, 0x8e, 0x9b, 0x12,
0xe9, 0x19, 0x7d, // NOLINT(readability-magic-numbers)
    0x50, 0x86, 0xcb, 0x9b, 0x50, 0x72, 0x19, 0xee, 0x95, 0xdb, 0x11, 0x3a, 0x91,
0x76, 0x78, 0xb2, // NOLINT(readability-magic-numbers)
    0x73, 0xbe, 0xd6, 0xb8, 0xe3, 0xc1, 0x74, 0x3b, 0x71, 0x16, 0xe6, 0x9e, 0x22,
0x22, 0x95, 0x16, // NOLINT(readability-magic-numbers)
    0x3f, 0xf1, 0xca, 0xa1, 0x68, 0x1f, 0xac, 0x09, 0x12, 0x0e, 0xca, 0x30, 0x75,
0x86, 0xe1, 0xa7 // NOLINT(readability-magic-numbers)
};
void tinycrypt_aes128cbc_example (void)
{
    struct tc_aes_key_sched_struct aes_keyschedule;
    uint8_t cbc_encrypted[TC_OUTPUT_CIPHERTEXT_SIZE] = {0U};
    uint8_t cbc_decrypted[TC_OUTPUT_CIPHERTEXT_SIZE] = {0U};
    if (TC_CRYPTOSUCCESS != tc_aes128_set_encrypt_key(&aes_keyschedule, cbc_key))
    {
        debugger_break();
    }
    else if (TC_CRYPTOSUCCESS !=
            tc_cbc_mode_encrypt(cbc_encrypted, sizeof(cbc_plaintext) +
TC_AES_BLOCK_SIZE, cbc_plaintext,
```

```
sizeof(cbc_plaintext), cbc_iv, &aes_keyschedule))
{
    debugger_break();
}
else if (0 != memcmp(&cbc_encrypted[0], &cbc_expected_ciphertext[0], sizeof
(cbc_encrypted)))
{
    debugger_break();
}
else if (TC_CRYPTOSUCCESS !=
        tc_cbc_mode_decrypt(cbc_decrypted, sizeof(cbc_encrypted),
&cbc_encrypted[TC_AES_BLOCK_SIZE],
sizeof(cbc_encrypted), cbc_encrypted, &aes_keyschedule))
{
    debugger_break();
}
else if (0 != memcmp(&cbc_plaintext[0], &cbc_decrypted[0], sizeof(cbc_plaintext)))
{
    debugger_break();
}
else
{
    /* Operation successful. */
    while (1)
    {
        ;
    }
}
}
```

## CTR-PRNG Example

This is an example on using the CTR\_PRNG module in TinyCrypt to obtain random data.

```
#define TC_ENTROPY_SIZE 64U
```

```
#define TC_CTRPRNG_OUTPUT_SIZE 32U
void tinycrypt_ctr_prng_example (void)
{
    TCctrPrng_t cprng_ctx;
    uint8_t     seed[TC_ENTROPY_SIZE];
    uint8_t     ctr_prng_output_1[TC_CTRPRNG_OUTPUT_SIZE] = {0};
    uint8_t     ctr_prng_output_2[TC_CTRPRNG_OUTPUT_SIZE] = {0};
    /* Setup the platform; initialize the crypto engine. */
    if (0 != RM_TINYCRYPT_PORT_Init())
    {
        debugger_break();
    }
    /* Read random data from the TRNG to use as seed for the CTR_PRNG. */
    else if (FSP_SUCCESS != RM_TINYCRYPT_PORT_TRNG_Read(seed, sizeof(seed)))
    {
        debugger_break();
    }
    /* Initialize and seed the CTR_PRNG with the random data from the TRNG. */
    else if (TC_CRYPTOSUCCESS != tc_ctr_prng_init(&cprng_ctx, seed, sizeof(seed), 0,
0))
    {
        debugger_break();
    }
    /* Read random data from the CTR_PRNG. */
    else if (TC_CRYPTOSUCCESS !=
            tc_ctr_prng_generate(&cprng_ctx, 0, 0, ctr_prng_output_1, sizeof
(ctr_prng_output_1)))
    {
        debugger_break();
    }
    /* Check that the generated value is not 0. */
    else if (0 != memcmp(&ctr_prng_output_1[0], &ctr_prng_output_2[0], sizeof
(ctr_prng_output_1)))
    {

```

```
        debugger_break();
    }

    /* Read random data again from the TRNG. */
    else if (TC_CRYPTTO_SUCCESS !=
            tc_ctr_prng_generate(&cprng_ctx, 0, 0, ctr_prng_output_1, sizeof
(ctr_prng_output_1)))
    {
        debugger_break();
    }

    /* Check that the generated value is different than the previous call. */
    else if (0 != memcmp(&ctr_prng_output_1[0], &ctr_prng_output_2[0], sizeof
(ctr_prng_output_1)))
    {
        debugger_break();
    }
else
    {
        /* Operation successful. */
        while (1)
            {
                ;

            }
    }
}
```

## Function Documentation

---

◆ **RM\_TINCYRYPT\_PORT\_TRNG\_Read()**

```
fsp_err_t RM_TINCYRYPT_PORT_TRNG_Read ( uint8_t *const p_rngbuf, uint32_t num_req_bytes )
```

Reads requested length of random data from the TRNG. Generate num\_req\_bytes of random bytes and store them in p\_rngbuf buffer.

**Return values**

FSP_SUCCESS	Random number generation successful
FSP_ERR_ASSERTION	NULL input parameter(s).
FSP_ERR_CRYPT_UNKNOWN	An unknown error occurred.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- HW\_SCE\_RNG\_Read

◆ **RM\_TINCYRYPT\_PORT\_Init()**

```
fsp_err_t RM_TINCYRYPT_PORT_Init ( )
```

Initialize the SCE.

◆ **default\_CSPRNG()**

```
int default_CSPRNG ( uint8_t * dest, unsigned int size )
```

Implements the Cryptographically Secure Pseudo-Random Number Generator function required by TinyCrypt.

**Return values**

TC_CRYPT_SUCCESS	Random number generation successful
TC_CRYPT_FAIL	Random number generation failed.

**Returns**

See [Common Error Codes](#) or functions called by this function for other possible return codes. This function calls:

- RM\_TINCYRYPT\_PORT\_TRNG\_Read

**4.2.99 Capacitive Touch Middleware (rm\_touch)****Modules****Functions**

```
fsp_err_t RM_TOUCH_Open (touch_ctrl_t *const p_ctrl, touch_cfg_t const *const
```

p\_cfg)

Opens and configures the TOUCH Middle module. Implements [touch\\_api\\_t::open](#). [More...](#)

fsp\_err\_t [RM\\_TOUCH\\_ScanStart](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl)

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with [RM\\_TOUCH\\_DataGet\(\)](#). If a different control block scan should be run, check the scan is complete before executing. Implements [touch\\_api\\_t::scanStart](#). [More...](#)

fsp\_err\_t [RM\\_TOUCH\\_DataGet](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl, [uint64\\_t](#) \*p\_button\_status, [uint16\\_t](#) \*p\_slider\_position, [uint16\\_t](#) \*p\_wheel\_position)

Gets the 64-bit mask indicating which buttons are pressed. Also, this function gets the current position of where slider or wheel is being pressed. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [touch\\_api\\_t::dataGet](#). [More...](#)

fsp\_err\_t [RM\\_TOUCH\\_PadDataGet](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl, [uint16\\_t](#) \*p\_pad\_rx\_coordinate, [uint16\\_t](#) \*p\_pad\_tx\_coordinate, [uint8\\_t](#) \*p\_pad\_num\_touch)

This function gets the current position of pad is being pressed. Implements [touch\\_api\\_t::padDataGet](#) , [g\\_touch\\_on\\_ctsu](#). [More...](#)

fsp\_err\_t [RM\\_TOUCH\\_CallbackSet](#) ([touch\\_ctrl\\_t](#) \*const p\_api\_ctrl, void(\*p\_callback)([touch\\_callback\\_args\\_t](#) \*), void const \*const p\_context, [touch\\_callback\\_args\\_t](#) \*const p\_callback\_memory)

fsp\_err\_t [RM\\_TOUCH\\_Close](#) ([touch\\_ctrl\\_t](#) \*const p\_ctrl)

Disables specified TOUCH control block. Implements [touch\\_api\\_t::close](#). [More...](#)

## Detailed Description

This module supports the Capacitive Touch Sensing Unit (CTSUs). It implements the [Touch Middleware Interface](#).

## Overview

The Touch Middleware uses the [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#) API and provides application-

level APIs for scanning touch buttons, sliders, and wheels. This module is configured via the [QE for Capacitive Touch](#).

## Features

- Supports touch buttons (Self and Mutual), sliders, and wheels
- Can retrieve the status of up to 64 buttons at once
- Software and external triggering
- Callback on scan end
- Collects and calculates usable scan results:
  - Slider position from 0 to 100 (percent)
  - Wheel position from 0 to 359 (degrees)
- Optional (build time) support for real-time monitoring functionality through the QE tool over UART

## Configuration

### Note

*This module is configured via the [QE for Capacitive Touch](#). For information on how to use the QE tool, once the tool is installed click [Help](#) -> [Help Contents in e2 studio](#) and search for "QE".*

*Multiple configurations can be defined within a single project allowing for different scan procedures or button layouts.*

### Build Time Configurations for rm\_touch

The following build time configurations are defined in fsp\_cfg/rm\_touch\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Support for QE monitoring using UART	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Enable SCI_UART support for QE monitoring.

### Configurations for Middleware > CapTouch > TOUCH Driver on rm\_touch

This module can be added to the Stacks tab via New Stack > Middleware > CapTouch > TOUCH Driver on rm\_touch. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
---------------	---------	---------	-------------

### Interrupt Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_ctorsu\)](#) section for details.

### Clock Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_ctorsu\)](#) section for details.

### Pin Configuration

Refer to the [Capacitive Touch Sensing Unit \(r\\_cts\)](#) section for details.

## Usage Notes

### Sliders and Wheels

Sliders and wheels are subject so some limitations:

	Slider	Wheel
Electrode type	Self capacitance only	Self capacitance only
Number of electrodes	4+	3-5
Touch position output range	0-100	0-359
Default value (no touch)	0xFFFF	0xFFFF

### Touch Judgement

Touch data is judged as touched or not-touched based on the threshold and hysteresis values determined during the QE tool tuning process. Refer to the QE for Capacitive Touch tool documentation in e2 studio Help for details on how these values are set.

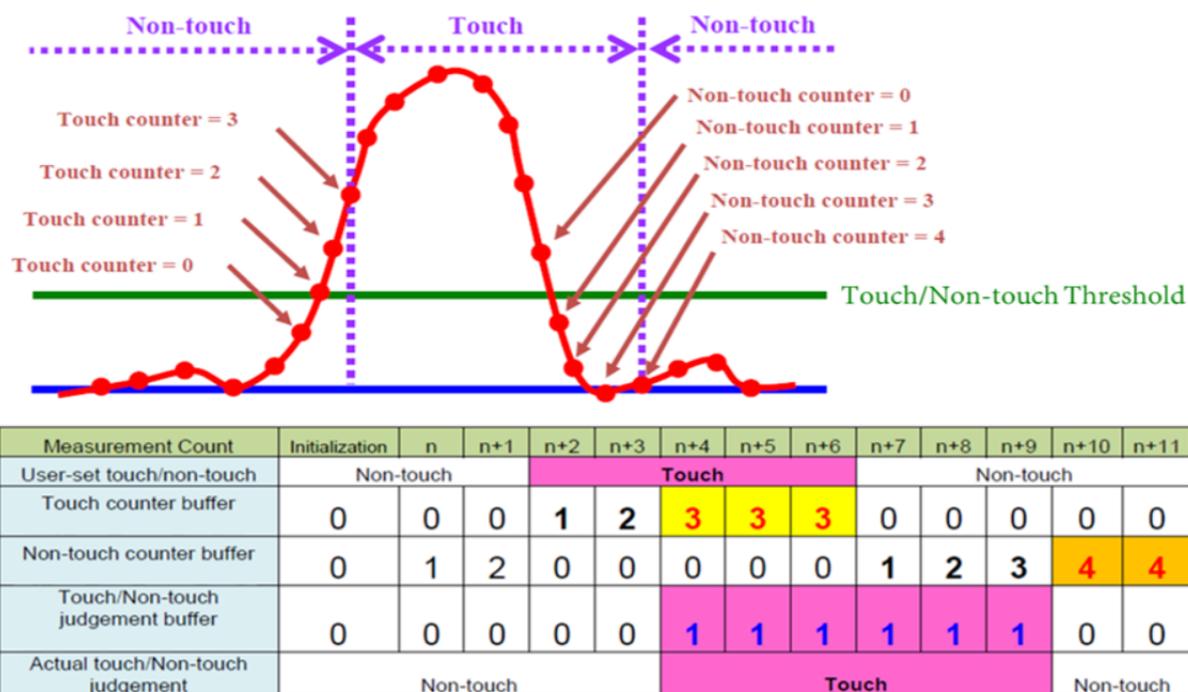


Figure 198: Touch/Non-touch judgement Image

### TrustZone Support

In r\_cts and rm\_touch module, Non-Secure Callable Guard Functions are only generated from QE for Capacitive Touch. QE can be used for tuning in secure or flat project, but not in non-secure project. If you want to use in non-secure project, copy the output file from secure or flat project. Refer to QE Help for more information.

# Examples

## Basic Example

This is a basic example of minimal use of the TOUCH in an application.

```
void touch_basic_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    err = RM_TOUCH_Open(&g_touch_ctrl, &g_touch_cfg);
    /* Handle any errors. This function should be defined by the user. */
    assert(FSP_SUCCESS == err);
    while (true)
    {
        RM_TOUCH_ScanStart(&g_touch_ctrl);
        while (0 == g_flag)
        {
            /* Wait scan end callback */
        }
        g_flag = 0;
        err = RM_TOUCH_DataGet(&g_touch_ctrl, &button, slider, wheel);
        if (FSP_SUCCESS == err)
        {
            /* Application specific data processing. */
        }
    }
}
```

## Multi Mode Example

This is a optional example of using both Self-capacitance and Mutual-capacitance. Refer to the Multi Mode Example in CTSU usage notes.

```
void touch_optional_example (void)
{
    fsp_err_t err = FSP_SUCCESS;
    err = RM_TOUCH_Open(&g_touch_ctrl, &g_touch_cfg);
```

```
assert(FSP_SUCCESS == err);

err = RM_TOUCH_Open(&g_touch_ctrl_mutual, &g_touch_cfg_mutual);

assert(FSP_SUCCESS == err);

while (true)
{
    RM_TOUCH_ScanStart(&g_touch_ctrl);

    while (0 == g_flag)
    {
        /* Wait scan end callback */
    }

    g_flag = 0;

    RM_TOUCH_ScanStart(&g_touch_ctrl_mutual);

    while (0 == g_flag)
    {
        /* Wait scan end callback */
    }

    g_flag = 0;

    err = RM_TOUCH_DataGet(&g_touch_ctrl, &button, slider, wheel);

    if (FSP_SUCCESS == err)
    {
        /* Application specific data processing. */
    }

    err = RM_TOUCH_DataGet(&g_touch_ctrl_mutual, &button, slider, wheel);

    if (FSP_SUCCESS == err)
    {
        /* Application specific data processing. */
    }
    }
}
```

## Data Structures

struct [touch\\_button\\_info\\_t](#)

struct [touch\\_slider\\_info\\_t](#)

struct [touch\\_wheel\\_info\\_t](#)

```
struct touch_pad_info_t
```

```
struct touch_instance_ctrl_t
```

## Data Structure Documentation

### ◆ touch\_button\_info\_t

struct touch_button_info_t		
Information of button		
Data Fields		
uint64_t	status	Touch result bitmap.
uint16_t *	p_threshold	Pointer to Threshold value array. g_touch_button_threshold[] is set by Open API.
uint16_t *	p_hysteresis	Pointer to Hysteresis value array. g_touch_button_hysteresis[] is set by Open API.
uint16_t *	p_reference	Pointer to Reference value array. g_touch_button_reference[] is set by Open API.
uint16_t *	p_on_count	Continuous touch counter. g_touch_button_on_count[] is set by Open API.
uint16_t *	p_off_count	Continuous non-touch counter. g_touch_button_off_count[] is set by Open API.
uint32_t *	p_drift_buf	Drift reference value. g_touch_button_drift_buf[] is set by Open API.
uint16_t *	p_drift_count	Drift counter. g_touch_button_drift_count[] is set by Open API.
uint8_t	on_freq	Copy from config by Open API.
uint8_t	off_freq	Copy from config by Open API.
uint16_t	drift_freq	Copy from config by Open API.
uint16_t	cancel_freq	Copy from config by Open API.

### ◆ touch\_slider\_info\_t

struct touch_slider_info_t		
----------------------------	--	--

Information of slider		
Data Fields		
uint16_t *	p_position	Calculated Position data. g_touch_slider_position[] is set by Open API.
uint16_t *	p_threshold	Copy from config by Open API. g_touch_slider_threshold[] is set by Open API.

#### ◆ touch\_wheel\_info\_t

struct touch_wheel_info_t		
Information of wheel		
Data Fields		
uint16_t *	p_position	Calculated Position data. g_touch_wheel_position[] is set by Open API.
uint16_t *	p_threshold	Copy from config by Open API. g_touch_wheel_threshold[] is set by Open API.

#### ◆ touch\_pad\_info\_t

struct touch_pad_info_t		
Information of pad		
Data Fields		
uint16_t *	p_rx_coordinate	RX coordinate.
uint16_t *	p_tx_coordinate	TX coordinate.
uint16_t *	p_num_touch	number of touch
uint16_t *	p_threshold	Coordinate calculation threshold value.
uint16_t *	p_base_buf	ScanData Base Value Buffer.
uint16_t *	p_rx_pixel	X coordinate resolution.
uint16_t *	p_tx_pixel	Y coordinate resolution.
uint8_t *	p_max_touch	Maximum number of touch judgments used by the pad.
int32_t *	p_drift_buf	Drift reference value. g_touch_button_drift_buf[] is set by Open API.
uint16_t *	p_drift_count	Drift counter. g_touch_button_drift_count[] is set by Open API.
uint8_t	num_drift	Copy from config by Open API.

## ◆ touch\_instance\_ctrl\_t

struct touch_instance_ctrl_t		
TOUCH private control block. DO NOT MODIFY. Initialization occurs when <code>RM_TOUCH_Open()</code> is called.		
Data Fields		
<code>uint32_t</code>	<code>open</code>	Whether or not driver is open.
<code>touch_button_info_t</code>	<code>binfo</code>	Information of button.
<code>touch_slider_info_t</code>	<code>sinfo</code>	Information of slider.
<code>touch_wheel_info_t</code>	<code>winfo</code>	Information of wheel.
<code>touch_pad_info_t</code>	<code>pinfo</code>	Information of pad.
<code>touch_cfg_t</code> const *	<code>p_touch_cfg</code>	Pointer to initial configurations.
<code>ctsu_instance_t</code> const *	<code>p_ctsu_instance</code>	Pointer to CTSU instance.

## Function Documentation

## ◆ RM\_TOUCH\_Open()

fsp_err_t RM_TOUCH_Open ( touch_ctrl_t *const p_ctrl, touch_cfg_t const *const p_cfg )	
Opens and configures the TOUCH Middle module. Implements <code>touch_api_t::open</code> .	
Example:	
<pre>err = RM_TOUCH_Open(&amp;g_touch_ctrl, &amp;g_touch_cfg);</pre>	
Return values	
FSP_SUCCESS	TOUCH successfully configured.
FSP_ERR_ASSERTION	Null pointer, or one or more configuration options is invalid.
FSP_ERR_ALREADY_OPEN	Module is already open. This module can only be opened once.
FSP_ERR_INVALID_ARGUMENT	Configuration parameter error.

### ◆ RM\_TOUCH\_ScanStart()

```
fsp_err_t RM_TOUCH_ScanStart ( touch_ctrl_t *const p_ctrl)
```

This function should be called each time a periodic timer expires. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Before starting the next scan, first get the data with [RM\\_TOUCH\\_DataGet\(\)](#). If a different control block scan should be run, check the scan is complete before executing. Implements [touch\\_api\\_t::scanStart](#).

#### Return values

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance or other.
FSP_ERR_CTSU_NOT_GET_DATA	The previous data has not been retrieved by DataGet.

### ◆ RM\_TOUCH\_DataGet()

```
fsp_err_t RM_TOUCH_DataGet ( touch_ctrl_t *const p_ctrl, uint64_t * p_button_status, uint16_t * p_slider_position, uint16_t * p_wheel_position )
```

Gets the 64-bit mask indicating which buttons are pressed. Also, this function gets the current position of where slider or wheel is being pressed. If initial offset tuning is enabled, The first several calls are used to tuning for the sensors. Implements [touch\\_api\\_t::dataGet](#).

#### Return values

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.
FSP_ERR_CTSU_INCOMPLETE_TUNING	Incomplete initial offset tuning.

◆ **RM\_TOUCH\_PadDataGet()**

```
fsp_err_t RM_TOUCH_PadDataGet ( touch_ctrl_t *const p_ctrl, uint16_t * p_pad_rx_coordinate,
uint16_t * p_pad_tx_coordinate, uint8_t * p_pad_num_touch )
```

This function gets the current position of pad is being pressed. Implements `touch_api_t::padDataGet` , `g_touch_on_ctsu`.

**Return values**

FSP_SUCCESS	Successfully data decoded.
FSP_ERR_ASSERTION	Null pointer.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_CTSU_SCANNING	Scanning this instance.

◆ **RM\_TOUCH\_CallbackSet()**

```
fsp_err_t RM_TOUCH_CallbackSet ( touch_ctrl_t *const p_api_ctrl, void(*) (touch_callback_args_t *)
p_callback, void const *const p_context, touch_callback_args_t *const p_callback_memory )
```

Updates the user callback and has option of providing memory for callback structure. Implements `touch_api_t::callbackSet`

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.

◆ **RM\_TOUCH\_Close()**

```
fsp_err_t RM_TOUCH_Close ( touch_ctrl_t *const p_ctrl)
```

Disables specified TOUCH control block. Implements `touch_api_t::close`.

**Return values**

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

## 4.2.100 USBX Porting Layer (rm\_usbx\_port)

### Modules

### Functions

Refer to [USB \(r\\_usb\\_basic\)](#) for the common API (r\_usb\_basic) to be called from the application.

## Overview

This USB driver works by combining USBX and r\_usb\_basic module.

## How to Configuration

- Using a class other than HMSC. The following describes how to configure USBX using PCDC as an example.

1. Select [New Stack]->[Azure RTOS]->[USBX]->[PCDC]

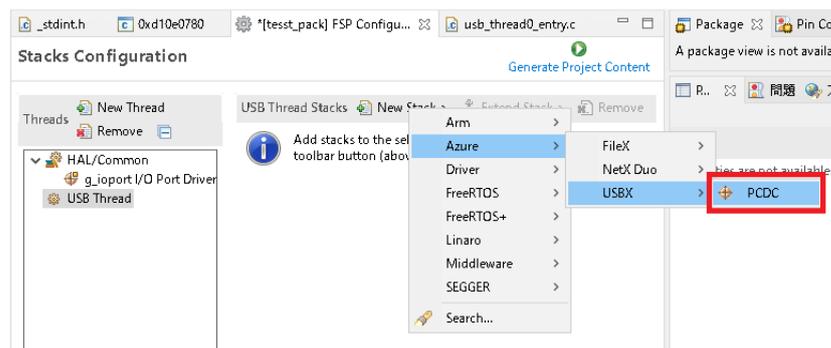


Figure 199: Select USB Device Class

2. The following is displayed when selecting USBX PCDC.

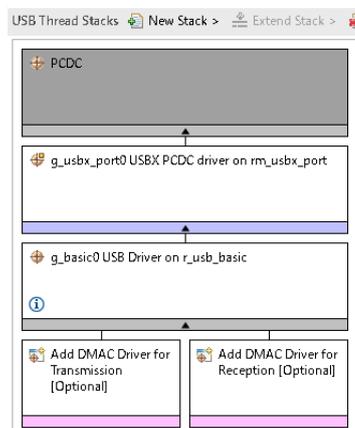


Figure 200: USBX PCDC Stack

3. Select the USB pipe to use.

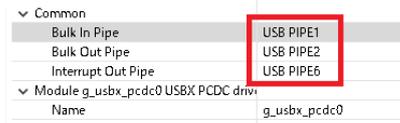


Figure 201: Select using USB Pipe

- Using HMSC. Since HMSC is used in a different way from other USBX modules, the usage is described below.

1. Select [New Stack]->[Azure RTOS]->[FileX]->[FileX on USBX]

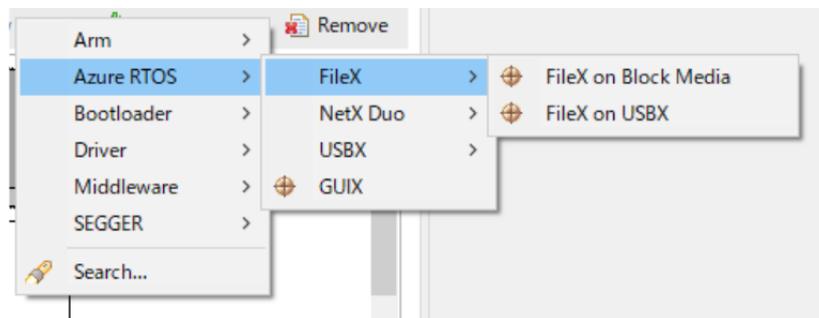


Figure 202: Select USB Device Class

2. The following is displayed when selecting Filex on USBX.

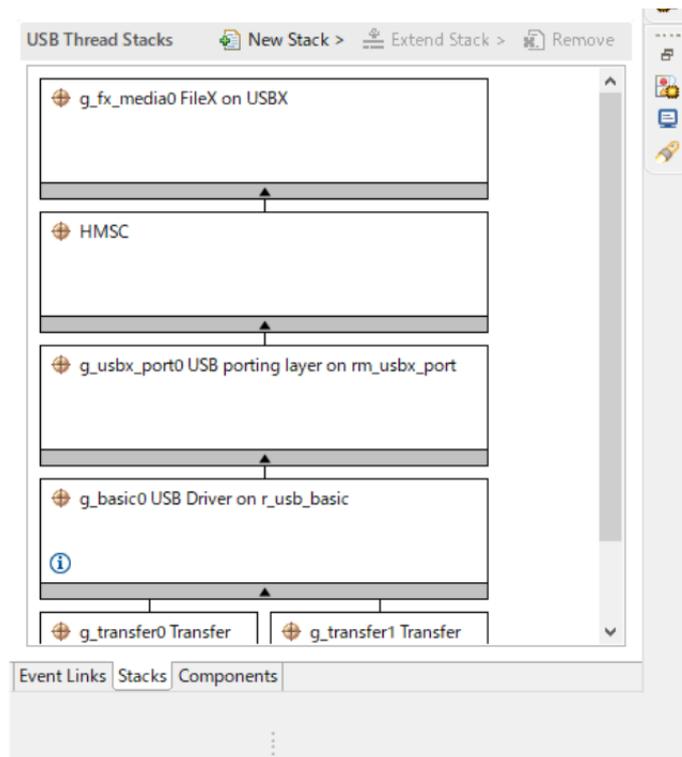


Figure 203: FileX on USBX Stack

## Note

- The following are notes on using the `ux_host_class_cdc_acm_read` function or the `ux_device_class_cdc_acm_read` function.
  1. Please specify a multiple of `MaxPacketSize` to the 3rd argument(`requested_length`). since If the value of the 3rd argument is not multiple of `MaxPacketSize`, all data sent by USB Host or USB Peripheral may not be received correctly.
  2. Please specify start address of thr area allocated a size larger than 3rd argument(`requested_length`) to the 2nd argument(`data_pointer` or `buffer`).
- HMSC uses FileX. For more information on FileX, please refer to the following URL.  
<https://docs.microsoft.com/en-us/azure/rtos/filex/>

## Limitations

1.Please call the initialization function in the application program. Please be sure to call `R_USB_Open` function after calling the following functions.

- Peripheral
  - PCDC / PHID
    - `ux_system_initialize`
    - `ux_device_stack_initialize`
    - `ux_device_stack_class_register`
  - PMSC
    - `ux_system_initialize`
    - `ux_device_stack_initialize`
- Host
  - HCDC / HHID
    - `ux_system_initialize`
    - `ux_host_stack_initialize`
  - HMSC
    - `ux_system_initialize`
    - `ux_host_stack_initialize`
    - `fx_system_initialize`

2.Set the value for 1000 Ticks per second in the "Timer Ticks Per Second" item.

Property	Value
Common	
General	
Timer	
Timer Ticks Per Second	1000
Timer Thread Stack Size	1024
Timer Thread Priority	0
Timer Process In ISR	Enabled
Reactivate Inline	Disabled
Timer	Enabled

Figure 204: Specify value of Timer Ticks Per Second

3.Set the Thread priority to a value of 21.

▼ Thread	
Symbol	usb_thread0
Name	USB Thread
Stack size (bytes)	1024
Priority	15
Auto start	Enabled
Time slicing interval (ticks)	1

Figure 205: Specify value of Thread priority

4. When using the following functions, call the following functions in the following order after calling the R\_USB\_Close function.

- Peripheral
  - PCDC / PHID
    - \_ux\_device\_stack\_class\_unregister
    - \_ux\_device\_stack\_uninitialize
  - PMSC
    - \_ux\_device\_stack\_uninitialize
- Host
  - \_ux\_host\_stack\_uninitialize

5. The USBX HID class does not support OUT transfer.

6. When using USBX HHID, please use Wired device.

## Descriptor

Templates for USBX descriptors can be found in ra/fsp/src/rm\_usbx\_port folder. Also, please be sure to use your vendor ID.

Change the descriptor.c.template file for each class as follows if High-speed mode is used.

- rm\_usbx\_pcdc\_descriptor.c.template
  1. Comment on lines 108 and 243.
  2. Delete the "/" on lines 109 and 242.
- rm\_usbx\_pmsc\_descriptor.c.template
  1. Comment on lines 78 and 153.
  2. Delete the "/" on lines 79 and 152.

## Examples

### USBX PCDC Example

PCDC loopback example is as follows.

```
#define VALUE_105 (105)
#define VALUE_2 (2)
#define VALUE_103 (103)
#define VALUE_93 (93)
/*****
```

```

* Function Name : ux_cdc_device0_instance_activate
* Description : Get instance
* Arguments : void * cdc_instance : Pointer to the area store the instance pointer
* Return value : none
*****/
static void ux_cdc_device0_instance_activate (void * cdc_instance)
{
/* Save the CDC instance. */
    g_cdc = (UX_SLAVE_CLASS_CDC_ACM *) cdc_instance;
}
/*****/
* End of function ux_cdc_device0_instance_activate
*****/
/*****/
* Function Name : ux_cdc_device0_instance_deactivate
* Description : Clear instance
* Arguments : void * cdc_instance : Pointer to area store the instance pointer
* Return value : none
*****/
static void ux_cdc_device0_instance_deactivate (void * cdc_instance)
{
    FSP_PARAMETER_NOT_USED(cdc_instance);
    g_cdc = UX_NULL;
}
/*****/
* End of function ux_cdc_device0_instance_deactivate
*****/
/*****/
* Function Name : apl_status_change_cb
* Description : USB callback function for USB status change
* Arguments : ULONG status : USB status
* Return value : UX_SUCCESS
*****/
UINT apl_status_change_cb (ULONG status)

```

```
{
switch (status)
{
case UX_DEVICE_ATTACHED:
    g_attach = USB_YES;
break;
case UX_DEVICE_REMOVED:
    g_attach = USB_NO;
break;
default:
break;
}
return UX_SUCCESS;
}
/*****
* End of function apl_status_change_cb
*****/
/*****
* Function Name : usb_x_pcdc_sample
* Description : Application task (loopback processing)
* Arguments : none
* Return value : none
*****/
void usb_x_pcdc_sample (void)
{
    fsp_err_t err;
    uint32_t ret;
    uint32_t size;
    _ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    _ux_device_stack_initialize(g_device_framework_hi_speed,
                               VALUE_103,
                               g_device_framework_full_speed,
                               VALUE_93,
                               g_string_framework,
```

```
        VALUE_105,  
        g_language_id_framework,  
        VALUE_2,  
        apl_status_change_cb);  
  
    g_ux_device_class_cdc_acm0_parameter.ux_slave_class_cdc_acm_instance_activate =  
ux_cdc_device0_instance_activate;  
  
    g_ux_device_class_cdc_acm0_parameter.ux_slave_class_cdc_acm_instance_deactivate =  
        ux_cdc_device0_instance_deactivate;  
  
    _ux_device_stack_class_register(_ux_system_slave_class_cdc_acm_name,  
_ux_device_class_cdc_acm_entry, 1, 0x00,  
        (void *) &g_ux_device_class_cdc_acm0_parameter);  
  
    err = g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);  
if (FSP_SUCCESS == err)  
    {  
while (1)  
    {  
if (USB_YES == g_attach)  
    {  
while (g_cdc == UX_NULL)  
    {  
        ;  
    }  
  
        ret = _ux_device_class_cdc_acm_read(g_cdc, g_buf, DATA_LEN,  
&g_actual_length);  
if (UX_SUCCESS == ret)  
    {  
        size = g_actual_length;  
        _ux_device_class_cdc_acm_write(g_cdc, g_buf, size,  
&g_actual_length);  
    }  
    }  
    }  
    }  
}
```

```

/*****
 * End of function usbx_pcdc_sample
 *****/

```

## USBX HCDC Example

The main functions of the HCDC loopback example are as follows:

1. Virtual UART control settings are configured by transmitting the class request SET\_LINE\_CODING to the CDC device.
2. Sends receive (Bulk In transfer) requests to a CDC peripheral device and receives data.
3. Loops received data back to the peripheral by means of Bulk Out transfers.

The main loop performs loopback processing in which data received from a CDC peripheral device is transmitted unaltered back to the peripheral.

```

#define VALUE_100 (100)
UINT ux_host_usr_event_notification (ULONG event, UX_HOST_CLASS * host_class, VOID *
instance)
{
    if (_ux_utility_memory_compare(_ux_system_host_class_cdc_acm_name, host_class,
_ux_utility_string_length_get(_ux_system_host_class_cdc_acm_name)) ==
        UX_SUCCESS)
    {
        if (event == UX_FSP_DEVICE_INSERTION) /* Check if there is a device insertion. */
        {
            p_cdc_acm = (UX_HOST_CLASS_CDC_ACM *) instance;
            if
(p_cdc_acm->ux_host_class_cdc_acm_interface->ux_interface_descriptor.bInterfaceClass
!=
                UX_HOST_CLASS_CDC_DATA_CLASS)
            {
                /* It seems the DATA class is on the second interface. Or we hope ! */
                p_cdc_acm = p_cdc_acm->ux_host_class_cdc_acm_next_instance;
                /* Check again this interface, if this is not the data interface, we give up. */
                if
(p_cdc_acm->ux_host_class_cdc_acm_interface->ux_interface_descriptor.bInterfaceClass

```

```
!=
    UX_HOST_CLASS_CDC_DATA_CLASS)
    {
    /* We did not find a proper data interface. */
        p_cdc_acm = UX_NULL;
    }
}
if (p_cdc_acm != UX_NULL)
    {
        tx_event_flags_set(&g_cdcacm_activate_event_flags0, CDCACM_FLAG,
TX_OR);
    }
}
else if (event == UX_FSP_DEVICE_REMOVAL) /* Check if there is a device removal. */
    {
        tx_event_flags_set(&g_cdcacm_activate_event_flags0, ~CDCACM_FLAG,
TX_AND);
        p_cdc_acm = UX_NULL;
    }
else
    {
    }
}
return UX_SUCCESS;
}
void buffer_clear (uint8_t * p)
{
    uint16_t counter;
    for (counter = 0; counter < DATA_LEN; counter++)
        {
            *p = 0U;
        }
}
/*****
```

```
* Function Name : usbx_hcdc_sample
* Description : Application task (loopback processing)
* Arguments : none
* Return value : none
*****/
/* CDCACM Host Thread entry function */
void usbx_hcdc_sample (void)
{
    uint32_t status;
    ULONG    actual_flags;
    uint16_t counter = 0;
    for (counter = 0; counter < DATA_LEN; counter++)
    {
        g_write_buf[counter] = (uint8_t) counter;
    }
    ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    ux_host_stack_initialize(ux_host_usr_event_notification);
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
        tx_event_flags_get(&g_cdcacm_activate_event_flags0, CDCACM_FLAG, TX_OR,
&actual_flags, TX_WAIT_FOREVER);
        if (p_cdc_acm != UX_NULL)
        {
            if (0 == g_is_communicate)
            {
                tx_thread_sleep(VALUE_100);
                g_is_communicate = 1;
            }
            status = ux_host_class_cdc_acm_write(p_cdc_acm, g_write_buf, DATA_LEN,
&g_write_actual_length);
            if ((UX_SUCCESS == status) && (DATA_LEN == g_write_actual_length))
            {
                g_read_actual_length = 0;
            }
        }
    }
}
```

```
        buffer_clear(g_read_buf);

        status = ux_host_class_cdc_acm_read(p_cdc_acm, g_read_buf, DATA_LEN,
&g_read_actual_length);

    if ((UX_SUCCESS == status) && (DATA_LEN == g_read_actual_length))
        {
    for (counter = 0; counter < DATA_LEN; counter++)
        {
    if ((uint8_t) counter != g_read_buf[counter])
        {
    while (1)
        {
                ;

        }
        }
        }
        }
        }
        }
        }
        }
    }
}
```

## USBX PMSC Example

PMSC storage example is as follows.

```
const rm_block_media_cfg_t g_rm_block_media0_cfg =
{.p_extend = NULL, .p_callback = NULL, .p_context = NULL, };
rm_block_media_instance_t g_rm_block_media0 =
{.p_api = &g_rm_block_media_on_user_media, .p_ctrl = NULL, .p_cfg =
&g_rm_block_media0_cfg, };
/*****
* Function Name : usbx_pmsc_sample
* Description : Application task (loopback processing)
* Arguments : none
* Return value : none
*****/
```

```
***** /
void usbx_pmsc_sample (void)
{
    fsp_err_t err;

    UINT      ret;

    ULONG     size;

    _ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    _ux_device_stack_initialize(
        g_device_framework_hi_speed,
        60,
        g_device_framework_full_speed,
        50,
        g_string_framework,
        93,
        g_language_id_framework,
        2,
        UX_NULL
    );

    err = g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    if (FSP_SUCCESS == err)
    {
        while (1)
        {
            ;

        }
    }
}
```

## USBX HMSC Example

HMSC storage example is as follows.

```
#define UX_STORAGE_BUFFER_SIZE (64 * 1024)
#define EVENT_USB_PLUG_IN (1UL << 0)
#define EVENT_USB_PLUG_OUT (1UL << 1)
```

```
#define MEMPOOL_SIZE (63488)
#define DATA_LEN (2048)
#define VALUE_32 (32)
#define VALUE_100 (100)
#define VALUE_200 (200)
#define VALUE_256 (256)
#define VALUE_1024 (1024)
#define DEVICE_INSERTION (0x01U)
#define DEVICE_REMOVAL (0x02U)
static uint16_t g_read_buf[UX_STORAGE_BUFFER_SIZE];
static uint16_t g_write_buf[UX_STORAGE_BUFFER_SIZE];
static FX_FILE g_file;
static uint8_t g_ux_pool_memory[MEMPOOL_SIZE];
static FX_MEDIA * g_p_media = UX_NULL;
TX_EVENT_FLAGS_GROUP g_usb_plug_events;
UINT usb_host_plug_event_notification(ULONG usb_event, UX_HOST_CLASS * host_class,
VOID * instance);
UINT ux_system_host_storage_fx_media_get(UX_HOST_CLASS_STORAGE * instance,
UX_HOST_CLASS_STORAGE_MEDIA **
p_storage_media,
FX_MEDIA ** p_fx_media);
static UINT apl_change_function (ULONG event, UX_HOST_CLASS * host_class, VOID *
instance)
{
    UINT status = UX_SUCCESS;
    UX_HOST_CLASS * class;
    UX_HOST_CLASS_STORAGE * storage;
    UX_HOST_CLASS_STORAGE_MEDIA * storage_media;
    (void) instance;
    /* Check the class container if it is for a USBX Host Mass Storage class. */
    if (UX_SUCCESS ==
        _ux_utility_memory_compare(_ux_system_host_class_storage_name, host_class,
        _ux_utility_string_length_get(_ux_system_host_class_storage_name)))
```

```
{
/* Check if there is a device insertion. */
if (DEVICE_INSERTION == event)
{
    status = ux_host_stack_class_get(_ux_system_host_class_storage_name,
&class);
if (UX_SUCCESS != status)
{
return status;
}
    status = ux_host_stack_class_instance_get(class, 0, (void **) &storage);
if (UX_SUCCESS != status)
{
return status;
}
if (UX_HOST_CLASS_INSTANCE_LIVE != storage->ux_host_class_storage_state)
{
return UX_ERROR;
}
    storage_media = class->ux_host_class_media;
    g_p_media      = &storage_media->ux_host_class_storage_media;
    tx_event_flags_set(&g_usb_plug_events, EVENT_USB_PLUG_IN, TX_OR);
}
else if (DEVICE_REMOVAL == event) /* Check if there is a device removal. */
{
    g_p_media = UX_NULL;
    tx_event_flags_set(&g_usb_plug_events, EVENT_USB_PLUG_OUT, TX_OR);
}
else
{
}
}
return status;
}
```

```
/*
*****
* Function Name : usb_x_hmsc_sample
* Description : Application task (loopback processing)
* Arguments : none
* Return value : none
*****
*/
void usb_x_hmsc_sample (void)
{
    CHAR          volume[VALUE_32];
    FX_MEDIA * p_media;
    ULONG         actual_length = 0;
    ULONG         actual_flags;
    UINT          tx_return;
    UINT          fx_return;
    uint16_t      data_count = 0;
    fx_system_initialize();
    ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    ux_host_stack_initialize(apl_change_function);
    tx_event_flags_create(&g_usb_plug_events, (CHAR *) "USB Plug Event Flags");
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
    while (1)
    {
        // Wait until device inserted.
        tx_return = tx_event_flags_get(&g_usb_plug_events,
                                     EVENT_USB_PLUG_IN,
                                     TX_OR_CLEAR,
                                     &actual_flags,
                                     TX_WAIT_FOREVER);

        if (TX_SUCCESS != tx_return)
        {
            tx_thread_sleep(TX_WAIT_FOREVER);
        }

        // Get the pointer to FileX Media Control Block for a USB flash device
        p_media = g_p_media;
    }
}
```

```
// Retrieve the volume name of the opened media from the Data sector
    fx_return = fx_media_volume_get(p_media, volume, FX_DIRECTORY_SECTOR);
if (FX_SUCCESS == fx_return)
    {
// Set the default directory in the opened media, arbitrary name called "firstdir"
    fx_directory_default_set(p_media, "firstdir");
// Suspend this thread for 200 time-ticks
    tx_thread_sleep(VALUE_100);
// Try to open the file, 'counter.txt'.
    fx_return = fx_file_open(p_media, &g_file, "counter.txt",
(FX_OPEN_FOR_READ | FX_OPEN_FOR_WRITE));
if (FX_SUCCESS != fx_return)
    {
// The 'counter.txt' file is not found, so create a new file
    fx_return = fx_file_create(p_media, "counter.txt");
if (FX_SUCCESS != fx_return)
    {
break;
    }
// Open that file
    fx_return = fx_file_open(p_media, &g_file, "counter.txt",
(FX_OPEN_FOR_READ | FX_OPEN_FOR_WRITE));
if (FX_SUCCESS != fx_return)
    {
break;
    }
}
// Already open a file, then read the file in blocks
// Set a specified byte offset for reading
    fx_return = fx_file_seek(&g_file, 0);
if (FX_SUCCESS == fx_return)
    {
    fx_return = fx_file_read(&g_file, g_read_buf, DATA_LEN,
&actual_length);
```

```
if ((FX_SUCCESS == fx_return) || (FX_END_OF_FILE == fx_return))
{
if (data_count == VALUE_1024)
{
// empty file

data_count = 0;

}
for (uint16_t data_max_count = data_count; data_count < (data_max_count +
VALUE_256); data_count++)
{

g_write_buf[data_count] = data_count;

}
// Set the specified byte offset for writing
fx_return = fx_file_seek(&g_file, 0);
if (FX_SUCCESS == fx_return)
{
// Write the file in blocks

fx_return = fx_file_write(&g_file, g_write_buf, DATA_LEN);
if (FX_SUCCESS == fx_return)
{

}
}
else
{

tx_thread_sleep(TX_WAIT_FOREVER);

}
}
}
}
else
{

tx_thread_sleep(TX_WAIT_FOREVER);

}

// Close already opened file
fx_return = fx_file_close(&g_file);
```

```
if (FX_SUCCESS != fx_return)
{
    tx_thread_sleep(TX_WAIT_FOREVER);
}

tx_thread_sleep(VALUE_200);
}
else
{
    tx_thread_sleep(TX_WAIT_FOREVER);
}
/* flush the media */
fx_return = fx_media_flush(p_media);
if (FX_SUCCESS != fx_return)
{
    tx_thread_sleep(TX_WAIT_FOREVER);
}
/* close the media */
fx_return = fx_media_close(p_media);
if (FX_SUCCESS != fx_return)
{
    tx_thread_sleep(TX_WAIT_FOREVER);
}
// Wait for unplugging the USB
tx_event_flags_get(&g_usb_plug_events, EVENT_USB_PLUG_OUT, TX_OR_CLEAR,
&actual_flags, TX_WAIT_FOREVER);
} // while(1)
}
```

## USBX PHID Example

PHID keyboard example is as follows.

```
/* *****
* Function Name : usbx_phid_keyboard_sample
* Description : Application task (loopback processing)
***** */
```

```
* Arguments : none
* Return value : none
*****/
void usbx_phid_keyboard_sample (void)
{
    UX_SLAVE_CLASS_HID_EVENT hid_event;
    UCHAR    key;
    fsp_err_t err;
    _ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    _ux_device_stack_initialize(NULL,
                                0,
                                g_device_framework_full_speed,
                                VALUE_52,
                                g_string_framework,
                                VALUE_53,
                                g_language_id_framework,
                                VALUE_2,
                                apl_status_change_cb);
    g_ux_device_class_hid_parameter.ux_slave_class_hid_instance_activate =
    ux_hid_instance_activate;
    g_ux_device_class_hid_parameter.ux_slave_class_hid_instance_deactivate =
    ux_hid_instance_deactivate;
    g_ux_device_class_hid_parameter.ux_device_class_hid_parameter_report_address =
    g_apl_report;
    g_ux_device_class_hid_parameter.ux_device_class_hid_parameter_report_length =
    REPORT_DESCRIPTOR_LENGTH;
    g_ux_device_class_hid_parameter.ux_device_class_hid_parameter_callback =
    apl_hid_set_report_cb;
    g_ux_device_class_hid_parameter.ux_device_class_hid_parameter_report_id = 0;
    ux_device_stack_class_register(_ux_system_slave_class_hid_name,
                                   _ux_device_class_hid_entry,
                                   1,
                                   0x00,
                                   (void *) &g_ux_device_class_hid_parameter);
```

```
/* Set the first key to 'a' which is 04. */
key = 0x04;

/* reset the HID event structure. */
ux_utility_memory_set(&hid_event, 0, sizeof(UX_SLAVE_CLASS_HID_EVENT));
err = g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
if (FSP_SUCCESS == err)
{
while (1)
{
if (USB_NO == g_suspend)
{
while (UX_NULL == g_hid)
{
/* Then wait. */
tx_thread_sleep(10);
}
/* 5sec wait */
usb_cpu_delay_xms((uint16_t) VALUE_5000);
/* Then insert a key into the keyboard event. Length is fixed to 8. */
hid_event.ux_device_class_hid_event_length = 8;
/* First byte is a modifier byte. */
hid_event.ux_device_class_hid_event_buffer[0] = 0;
/* Second byte is reserved. */
hid_event.ux_device_class_hid_event_buffer[1] = 0;
/* The 6 next bytes are keys. We only have one key here. */
hid_event.ux_device_class_hid_event_buffer[2] = key;
/* Set the keyboard event. */
ux_device_class_hid_event_set(g_hid, &hid_event);
/* Next event has the key depressed. */
hid_event.ux_device_class_hid_event_buffer[2] = 0;
/* Length is fixed to 8. */
hid_event.ux_device_class_hid_event_length = 8;
/* Set the keyboard event. */
ux_device_class_hid_event_set(g_hid, &hid_event);
```

```
/* Are we at the end of alphabet ? */
if (key != (0x04 + 26))
    {
    /* Next key. */

        key++;

    }
else
    {
    /* Start over again. */
    key = 0x04;
    }

    apl_status_change_cb(UX_DEVICE_SUSPENDED);

}
else
    {
if (USB_NO == g_remote_wakeup)
    {

        tx_thread_sleep(VALUE_10000);

/* Remote wakeup processing */
        g_remote_wakeup = USB_YES;
        ux_device_stack_host_wakeup();
        apl_status_change_cb(UX_DEVICE_RESUMED);

    }
    }
}
}
```

## USBX HHID Example

HHID user interface example is as follows.

```
void keyboard_update_task (ULONG thread_input)
{
    ULONG usbx_return_value;
```

```
/* keyboard button masks, set by ux_host_class_hid_keyboard_buttons_get call */
    ULONG keyboard_key = 0;
/* keyboard state masks, set by ux_host_class_hid_keyboard_buttons_get call */
    ULONG keyboard_state = 0;
FSP_PARAMETER_NOT_USED(thread_input);
while (1)
    {
        usbx_return_value = ux_host_class_hid_keyboard_key_get(
            (UX_HOST_CLASS_HID_KEYBOARD *)
hid_keyboard_client->ux_host_class_hid_client_local_instance,
            &keyboard_key,
            &keyboard_state);
        if ((usbx_return_value == UX_SUCCESS) || (usbx_return_value == UX_NO_KEY_PRESS))
            {
                hid_devices_info.device_connected = KEYBOARD_DEVICE;
                hid_devices_info.key = keyboard_key;
                hid_devices_info.keyboard_status = keyboard_state;
/* Clear the states for next read */
                keyboard_key = 0;
                keyboard_state = 0;
/* copy the keyboard states to queue */
                tx_queue_send(&device_parameters, &hid_devices_info, TX_NO_WAIT);
            }
            tx_thread_sleep(10);
        }
}
void mouse_update_task (ULONG thread_input)
{
/* mouse button masks, set by ux_host_class_hid_mouse_buttons_get call */
    ULONG mouse_buttons;
/* X co-ordinate displacement of mouse */
    SLONG mouse_x_position = 0;
/* Y co-ordinate displacement of mouse */
    SLONG mouse_y_position = 0;
```

```
/* variable to hold USBX return values */
ULONG usbx_return_value;
FSP_PARAMETER_NOT_USED(thread_input);
while (1)
{
    usbx_return_value = ux_host_class_hid_mouse_buttons_get(
        (UX_HOST_CLASS_HID_MOUSE *)
hid_mouse_client->ux_host_class_hid_client_local_instance,
        &mouse_buttons);
    if (usbx_return_value == UX_SUCCESS)
    {
        usbx_return_value = ux_host_class_hid_mouse_position_get(
            (UX_HOST_CLASS_HID_MOUSE *)
hid_mouse_client->ux_host_class_hid_client_local_instance,
            &mouse_x_position,
            &mouse_y_position);
    }
    if (usbx_return_value == UX_SUCCESS)
    {
        hid_devices_info.device_connected = MOUSE_DEVICE;
        hid_devices_info.key = mouse_buttons;
        hid_devices_info.mouse_direction_X = mouse_x_position;
        hid_devices_info.mouse_direction_Y = mouse_y_position;
        tx_queue_send(&device_parameters, &hid_devices_info, TX_NO_WAIT);
    }
    tx_thread_sleep(10);
}
}
void usbx_hhid_sample (void)
{
    uint8_t i;
    ux_system_initialize((CHAR *) g_ux_pool_memory, MEMPOOL_SIZE, UX_NULL, 0);
    ux_host_stack_initialize(ux_system_host_hid_change_function);
    g_usb_on_usb.open(&g_basic0_ctrl, &g_basic0_cfg);
}
```

```
tx_thread_create(&keyboard_update,
                (CHAR *) "keyboard_update_task",
                keyboard_update_task,
                (ULONG) NULL,
                &keyboard_update_stack,
                2048,
                22,
                2,
                1,
                TX_AUTO_START);

tx_thread_create(&mouse_update,
                (CHAR *) "mouse_update_task",
                mouse_update_task,
                (ULONG) NULL,
                &mouse_update_stack,
                1024,
                22,
                2,
                1,
                TX_AUTO_START);

while (1)
{
for (i = 0; i < UX_HOST_CLASS_HID_MAX_CLIENTS; i++)
{
/* Check whether the instance registered? through USB HID device insertion callback?
*/
if (NULL != hid_class_keyboard_instance[i])
{
UX_HOST_CLASS_HID_CLIENT * hid_client =
hid_class_keyboard_instance[i]->ux_host_class_hid_client;
hid_keyboard_client = hid_client;
tx_thread_sleep(10);
}
/* Check whether the instance registered? through USB HID device insertion callback?
```

```

*/
if (NULL != hid_class_mouse_instance[i])
{
    UX_HOST_CLASS_HID_CLIENT * hid_client =
hid_class_mouse_instance[i]->ux_host_class_hid_client;
    hid_mouse_client = hid_client;
    tx_thread_sleep(10);
}
/* If multiple similar type devices are connected, allow them one by one share data
with application */
    tx_thread_sleep(10);
}
}
}
}

```

## 4.2.101 Virtual EEPROM (rm\_vee\_flash)

### Modules

#### Functions

fsp_err_t	RM_VEE_FLASH_Open (rm_vee_ctrl_t *const p_api_ctrl, rm_vee_cfg_t const *const p_cfg)
fsp_err_t	RM_VEE_FLASH_RecordWrite (rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t const num_bytes)
fsp_err_t	RM_VEE_FLASH_RecordPtrGet (rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)
fsp_err_t	RM_VEE_FLASH_RefDataWrite (rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data)
fsp_err_t	RM_VEE_FLASH_RefDataPtrGet (rm_vee_ctrl_t *const p_api_ctrl, uint8_t **const pp_ref_data)
fsp_err_t	RM_VEE_FLASH_StatusGet (rm_vee_ctrl_t *const p_api_ctrl, rm_vee_status_t *const p_status)
fsp_err_t	RM_VEE_FLASH_Refresh (rm_vee_ctrl_t *const p_api_ctrl)

```
fsp_err_t RM_VEE_FLASH_Format (rm_vee_ctrl_t *const p_api_ctrl, uint8_t
const *const p_ref_data)
```

```
fsp_err_t RM_VEE_FLASH_CallbackSet (rm_vee_ctrl_t *const p_api_ctrl,
void(*p_callback)(rm_vee_callback_args_t *), void const *const
p_context, rm_vee_callback_args_t *const p_callback_memory)
```

```
fsp_err_t RM_VEE_FLASH_Close (rm_vee_ctrl_t *const p_api_ctrl)
```

## Detailed Description

Virtual EEPROM on RA MCUs. This module implements the [Virtual EEPROM Interface](#).

## Overview

This VEE module emulates basic EEPROM capabilities. Support is provided for reading and writing both common records and reference data (originally programmed during product assembly or test). A count of the number of segments erased throughout the lifetime of the application is maintained and can be accessed at any time. Wear leveling is handled automatically by the driver.

### Features

- Writing and reading user defined records of any length to data flash.
- Wear leveling is handled automatically.
- Reference data such as calibration data programmed at assembly or test time is preserved.
- Reference data can be updated at run time.
- Fault resilient design.

### Data Flash Segmentation

Wear leveling is handled by changing the location in the data flash where a record is stored every time that it is updated. This change in physical location of the record is transparent to the user. Any time an update for a specific record ID is written, it is written to the next unused location in data flash and its location is stored in RAM for quick look-up later. When required, only the most recent version of these records is automatically copied to the next blank segment in data flash. The data flash area is divided into a number of equal-size segments. There is only one segment active at a time. A segment contains two areas- the record area (which is the vast majority of the segment) and the reference data area which contains optional data typically programmed during assembly or final test. Records and updated reference data are written to this segment until one of the two areas becomes full. The record area must be able to hold at least one of every record ID possible and still have space left over for record updates.

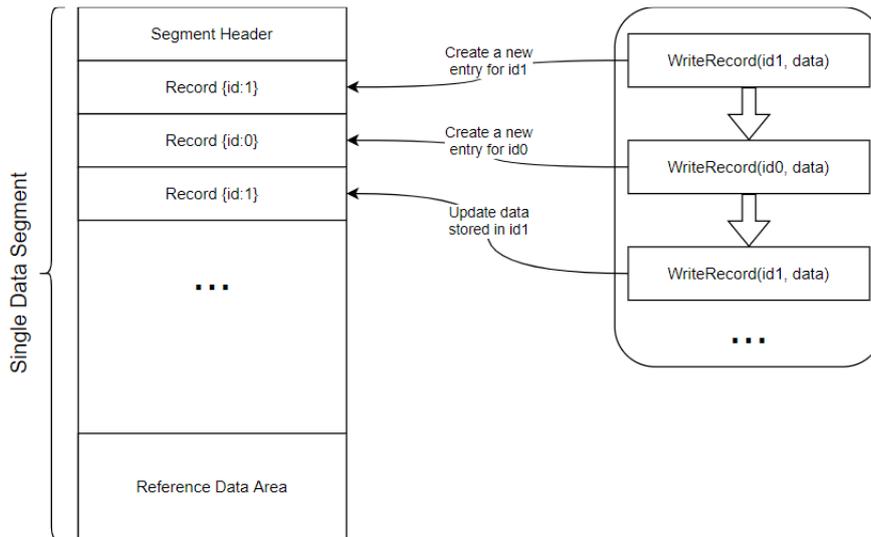


Figure 206: Segment Data Format

When a segment does not have sufficient space for additional records or updated reference data, a Refresh occurs. This process copies the most recent record for each ID as well as the latest version of reference data (if any) to the next segment. The very first time VEE runs on an MCU, it marks the last segment as active whether there is reference data configured or not. The end of VEE data flash area is used to provide an easily identified physical flash address that can be used while programming reference data without requiring Virtual EEPROM middleware.

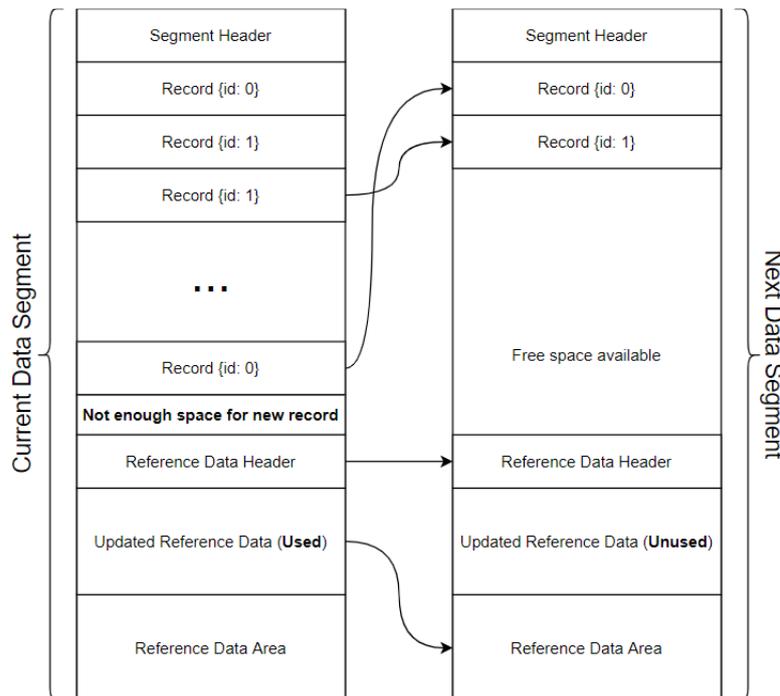


Figure 207: Refresh Operation

### Record Format

Each record begins with a header that contains the record size, followed by the data, and the trailer.

The trailer contains a validation code which is used for internal purposes only and is not a 16-bit CRC or ECC value. If that level of error checking is desired, the user should include that in the record data passed to the driver.

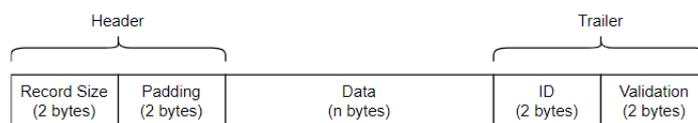


Figure 208: Record Format

## Reference Data Area

VEE can be configured for the presence of reference data. The original programmed reference data must be located at the end of the VEE data flash area. An area of equal size is reserved below this in case updated reference data becomes available later. Below that is a header which indicates whether the update area has been written to.

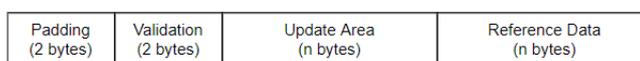


Figure 209: Reference Data Area Format

Just as with records, the validation code is used for internal purposes only and is not a 16-bit CRC or ECC value. If that level of error checking is desired, the user should include that in the updated reference data passed to the driver.

## Fault Tolerance

The Virtual EEPROM has a fault tolerant design. If for any reason an operation fails before it is completed the next time the module is opened a refresh will occur. Any corrupted data will be discarded.

# Configuration

## Build Time Configurations for rm\_vee\_flash

The following build time configurations are defined in fsp\_cfg/rm\_vee\_flash\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>Default (BSP)</li> <li>Enabled</li> <li>Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.
Reference Data Support	<ul style="list-style-type: none"> <li>Enabled</li> <li>Disabled</li> </ul>	Disabled	Support writing reference data to the end of the segment.
Refresh Buffer Size	Value must be an integer greater than 0 and a multiple of 4 bytes.	32	The size of the internal buffer used to copying data from one flash segment to another

during a refresh operation. This is required because data flash to data flash transfers are not supported by the hardware.

## Configurations for Middleware > Storage > Virtual EEPROM on Flash

This module can be added to the Stacks tab via New Stack > Middleware > Storage > Virtual EEPROM on Flash. Non-secure callable guard functions can be generated for this module by right clicking the module in the RA Configuration tool and checking the "Non-secure Callable" box.

Configuration	Options	Default	Description
Name	Name must be a valid C symbol	g_vee0	Module name.
Record Max ID	Value must be an integer.	16	Set this value to the highest record ID in use.
Number of Segments	Value must be an integer.	2	Set value to number of segments desired in data flash (minimum 2). The fewer the segments, the fewer refreshes occur, but the longer refreshes take to complete (erase time).
Start Address	Manual Entry	BSP_FEATURE_FLASH_DATA_FLASH_START	Start address of the flash area used by Virtual EEPROM.
Total Size	Manual Entry	BSP_DATA_FLASH_SIZE_BYTES	The total size (In bytes) of the flash area used by Virtual EEPROM.
Reference Data Size	Value must be an integer.	0	The size of the reference area (In bytes) used by Virtual EEPROM.
Callback	Name must be a valid C symbol	vee_callback	A user callback function can be provided. If this callback function is provided, it will be called from the flash interrupt service routine (ISR).

## Clock Configuration

There is no clock configuration for the RM\_VEE\_FLASH module.

## Pin Configuration

This module does not use I/O pins.

## Usage Notes

A refresh buffer is required to copy data between segments. Data flash cannot be simultaneously read from and written to. Data will be temporarily copied into RAM during refresh operations.

## Examples

### Basic Example

This is a basic example of minimal use of the RM\_VEE\_FLASH module in an application.

```
volatile bool callback_called = false;
/* Record ID to use for storing pressure data. */
#define ID_PRESSURE (0U)
/* Example data structure. */
typedef struct st_pressure
{
    uint32_t timestamp;
    uint16_t low;
    uint16_t average;
    uint16_t high;
} pressure_t;
void rm_vee_example ()
{
    /* Open the Virtual EEPROM Module. */
    fsp_err_t err = RM_VEE_FLASH_Open(&g_vee_ctrl, &g_vee_cfg);
    if (FSP_SUCCESS != err)
    {
        error_handler();
    }
    /* Read pressure data from external sensor. */
    pressure_t pressure_data;
    get_pressure_data(&pressure_data);
    /* Write the pressure data to a Virtual EEPROM Record. */
```

```
err = RM_VEE_FLASH_RecordWrite(&g_vee_ctrl, ID_PRESSURE, (uint8_t *)
&pressure_data, sizeof(pressure_t));
if (FSP_SUCCESS != err)
{
    error_handler();
}
/* Wait for the Virtual EEPROM callback to indicate it finished writing data. */
while (false == callback_called)
{
    ;
}
/* Get a pointer to the record that is stored in data flash. */
uint32_t    length;
pressure_t * p_pressure_data;
err = RM_VEE_FLASH_RecordPtrGet(&g_vee_ctrl, ID_PRESSURE, (uint8_t **)
&p_pressure_data, &length);
if (FSP_SUCCESS != err)
{
    error_handler();
}
/* Close the Virtual EEPROM Module. */
err = RM_VEE_FLASH_Close(&g_vee_ctrl);
if (FSP_SUCCESS != err)
{
    error_handler();
}
}
void rm_vee_tests_callback (rm_vee_callback_args_t * p_args)
{
    callback_called = true;
    FSP_PARAMETER_NOT_USED(p_args);
}
```

## Data Structures

```
struct  rm_vee_flash_cfg_t
```

```
struct rm_vee_flash_instance_ctrl_t
```

## Data Structure Documentation

### ◆ rm\_vee\_flash\_cfg\_t

struct rm_vee_flash_cfg_t		
User configuration structure, used in open function		
Data Fields		
flash_instance_t const *	p_flash	Pointer to a flash instance.

### ◆ rm\_vee\_flash\_instance\_ctrl\_t

struct rm_vee_flash_instance_ctrl_t
Instance control block. This is private to the FSP and should not be used or modified by the application.

## Function Documentation

### ◆ RM\_VEE\_FLASH\_Open()

fsp_err_t RM_VEE_FLASH_Open ( rm_vee_ctrl_t *const p_api_ctrl, rm_vee_cfg_t const *const p_cfg )	
Open the RM_VEE_FLASH driver module	
Implements <a href="#">rm_vee_api_t::open</a>	
Initializes the driver's internal structures and opens the Flash driver. The Flash driver must be closed prior to opening VEE. The error code FSP_SUCCESS_RECOVERY indicates that VEE detected corrupted data; most likely due to a power loss during a data flash write or erase. In these cases, an automatic internal Refresh is performed and the partially written data is lost.	
<b>Return values</b>	
FSP_SUCCESS	Successful. FSP_SUCCESS_RECOVERY changed to FSP_SUCCESS
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_ALREADY_OPEN	This function has already been called.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Interrupts disabled outside of VEE
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.
FSP_ERR_INVALID_ARGUMENT	The supplied configuration is invalid.

### ◆ RM\_VEE\_FLASH\_RecordWrite()

```
fsp_err_t RM_VEE_FLASH_RecordWrite ( rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id,
uint8_t const *const p_rec_data, uint32_t const num_bytes )
```

Writes a record to data flash.

Implements `rm_vee_api_t::recordWrite`

This function writes `num_bytes` of data pointed to by `p_rec_data` to data flash. This function returns immediately after starting the flash write. BE SURE NOT TO MODIFY the data buffer contents until after the write completes. This includes exiting the calling function when the data buffer is a local variable (stack may be used by another function and corrupt the data buffer contents).

#### Return values

FSP_SUCCESS	Write started successfully.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_INVALID_ARGUMENT	An argument contains an illegal value.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_RecordPtrGet()**

```
fsp_err_t RM_VEE_FLASH_RecordPtrGet ( rm_vee_ctrl_t *const p_api_ctrl, uint32_t const rec_id,
uint8_t **const pp_rec_data, uint32_t *const p_num_bytes )
```

Gets a pointer to the most recent record data.

Implements `rm_vee_api_t::recordPtrGet`

This function sets the argument pointer to the most recent version of the record data in flash. Flash cannot be accessed for reading and writing at the same time. Therefore, reading the data at `p_ref_data` must be completed prior to initiating any type of Flash write.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	<code>p_ref_data</code> is NULL.
FSP_ERR_INVALID_ARGUMENT	Record data not configured.
FSP_ERR_NOT_FOUND	The record associated with the requested ID could not be found.

### ◆ RM\_VEE\_FLASH\_RefDataWrite()

```
fsp_err_t RM_VEE_FLASH_RefDataWrite ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data )
```

Writes new Reference data to the reference update area.

Implements `rm_vee_api_t::refDataWrite`

This function writes VEE\_CFG\_REF\_DATA\_SIZE bytes pointed to by p\_ref\_data to data flash. This function returns immediately after starting the flash write. BE SURE NOT TO MODIFY the data buffer contents until after the write completes.

#### Return values

FSP_SUCCESS	Write started successfully.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_UNSUPPORTED	Reference data is not supported in the current configuration.
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_RefDataPtrGet()**

```
fsp_err_t RM_VEE_FLASH_RefDataPtrGet ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t **const pp_ref_data )
```

Gets a pointer to the most recent reference data.

Implements `rm_vee_api_t::recordPtrGet`

This function sets the argument pointer to the most recent version of the reference data in flash. Flash cannot be accessed for reading and writing at the same time.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_UNSUPPORTED	Reference data is not supported in the current configuration.
FSP_ERR_NOT_FOUND	No reference data was found.

◆ **RM\_VEE\_FLASH\_StatusGet()**

```
fsp_err_t RM_VEE_FLASH_StatusGet ( rm_vee_ctrl_t *const p_api_ctrl, rm_vee_status_t *const p_status )
```

Get the current status of the driver.

Implements `rm_vee_api_t::statusGet`

This command is typically used to verify that the last Write or Refresh command has completed before attempting to perform another API call.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.

◆ **RM\_VEE\_FLASH\_Refresh()**

```
fsp_err_t RM_VEE_FLASH_Refresh ( rm_vee_ctrl_t *const p_api_ctrl)
```

Manually start a refresh operation

Implements `rm_vee_api_t::refresh`

This function is used to start a segment Refresh at any time. The Refresh process by default occurs automatically when no more record or reference data space is available and a Write is requested. However, the app may desire to force a refresh when it knows it is running low on space and large amounts of data are about to be recorded.

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed in hardware.
FSP_ERR_INVALID_MODE	The operation cannot be started in the current mode.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_Format()**

```
fsp_err_t RM_VEE_FLASH_Format ( rm_vee_ctrl_t *const p_api_ctrl, uint8_t const *const p_ref_data )
```

Start a manual format operation.

Implements `rm_vee_api_t::format`

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_IN_USE	Last API call still executing.
FSP_ERR_PE_FAILURE	This error indicates that a flash programming, erase, or blankcheck operation has failed
FSP_ERR_ASSERTION	An input parameter is NULL.
FSP_ERR_TIMEOUT	Flash write timed out (Should not be possible when flash bgo is used).
FSP_ERR_NOT_INITIALIZED	Corruption found. A refresh is required.

◆ **RM\_VEE\_FLASH\_CallbackSet()**

```
fsp_err_t RM_VEE_FLASH_CallbackSet ( rm_vee_ctrl_t *const p_api_ctrl, void(*) (rm_vee_callback_args_t *) p_callback, void const *const p_context, rm_vee_callback_args_t *const p_callback_memory )
```

Updates the user callback with the option to provide memory for the callback argument structure.

Implements `rm_vee_api_t::callbackSet`.

**Return values**

FSP_SUCCESS	Callback updated successfully.
FSP_ERR_ASSERTION	A required pointer is NULL.
FSP_ERR_NOT_OPEN	The control block has not been opened.
FSP_ERR_NO_CALLBACK_MEMORY	<code>p_callback</code> is non-secure and <code>p_callback_memory</code> is either secure or NULL.

◆ **RM\_VEE\_FLASH\_Close()**

```
fsp_err_t RM_VEE_FLASH_Close ( rm_vee_ctrl_t *const p_api_ctrl)
```

Closes the Flash driver and VEE driver.

Implements `rm_vee_api_t::close`

**Return values**

FSP_SUCCESS	Successful.
FSP_ERR_NOT_OPEN	The module has not been opened.
FSP_ERR_ASSERTION	An input parameter is NULL.

**4.2.102 AWS Device Provisioning**

## Modules

AWS Device Provisioning example software.

**Overview****Terminology**

The terminology defined below will be used in the following sections.

Term	Description
Service Provider	Entity that provides the cloud infrastructure and associated services, for example, AWS/Azure.
Device Manufacturer	Entity that provides the MCU, for example, Renesas.
OEM	Entity that uses the MCU to create a product.
Customer	End user of OEM product.

**Device ID**

For systems that intend to use Public Key Certificate (PKC), the Device ID is in the form of a key pair (RSA or ECC). A PKC comprises of a **public key**, metadata, and finally a signature over all that. This signature is generated by the entity that issues the certificate and is known as a CA (Certificate Authority). The most common format for a public certificate is the [X.509 format](#) which is typically PEM (base 64) encoded such that the certificate is human-readable. It can also be DER encoded which is binary encoding and thus not human readable. The **public key** portion of the Device ID is used for the Device Certificate.

## Provisioning

Device Provisioning refers to the process by which a service provider links a certificate to a Device ID and thus a device. Depending on the provisioning model, an existing certificate from the device may be used or a new one will be issued at this stage. Provisioning (also referred to as Registration) occurs with respect to a particular service provider, for example, AWS or Azure. It is necessary that the certificate is issued by the service provider or a CA known to those providers. When a device is provisioned with AWS for example, the AWS IoT service associates the Device ID (and thus the device) with a specific certificate. The certificate will be programmed into the device and for all future transactions with AWS, the certificate will be used as the means of identifying the device. The public and private key are also stored on the MCU.

### Provisioning Models

Provisioning services vary between [service providers](#). There are essentially three general provisioning models.

1. Provisioning happens on the production line. This requires the provisioning Infrastructure to be present on the production line. This is the most secure model, but is expensive.
2. Devices are programmed with a shared credential that is linked into the code at build time and the provisioning occurs when a customer uses the device for the first time. The shared credential and a unique device serial number are used to uniquely identify the device during the provisioning process. So long as the product only has the shared credential, it will only operate with limited (as defined by certificate policy) functionality. Once the provisioning is done, then the device will be fully functional. This is the most common use case for consumer products where no sensitive information is being transmitted. AWS provides an [example](#) of this model.
3. Devices have no identity programmed in the factory; provisioning occurs through some other device like a smartphone which is already trusted by the service provider.

In all these cases, the Device Identity

1. Is unique to the device
2. Must have restricted access within the device
3. Can be used to issue more than one certificate and the certificates themselves have to be updatable in the field.

AWS uses the PKCS11 API to erase, store and retrieve certificates. These PKCS11 functions (Write, Read and Erase) are separated out into a Physical Abstraction Layer (PAL) which the OEM/Device Manufacturer is expected to implement for the type of memory that they intend to use. The internal `rm_aws_pkcs11_pal` module implements these requirements on RA MCU data flash.

## AWS Provisioning Example

AWS provides an **example** implementation to support device provisioning. This implementation uses the PKCS11 API to store device credentials into the PKCS11 defined memory. The implementation (`aws_dev_mode_key_provisioning.c`) exposes two functions:

1. `vDevModeKeyProvisioning()`
2. `vAlternateKeyProvisioning()`

Both of these functions require that the device credentials be provided in PEM format. Using either of these example functions as is in production is not recommended; but `vAlternateKeyProvisioning()` provides more flexibility because of the ability to provide credentials as arguments.

Credentials can be created as follows:

- [Create your own CA](#) and use that to generate the device certificate. This CA will have to be registered with the service provider with which the product will be used, for example [Register your CA with AWS](#).
- [Use AWS](#) to generate the device certificate.

## Examples

### Basic Example

This is a basic example of provisioning a device using the AWS demo implementation.

```
#define keyCLIENT_CERTIFICATE_PEM \
    "-----BEGIN CERTIFICATE-----\n" \
    "MIIDETCCAfkCFHwd2yn8zn5qB2ChYUT9Mvbi9Xp1MA0GCSqGS1b3DQEBCwUAMEUx\n" \
    "CzAJBgNVBAYTAKFVMRMwEQYDVQQIDApTb211LVN0YXR1MSEwHwYDVQQKBhJbnRl\n" \
    "cm5ldCBXaWRnaXRzIFB0eSBMdGQwHhcNMkVOTExMjU0WhcNMjAwOTExMjU0\n" \
    "MjU0WjBFMQswCQYDVQQGEwJBVTEFTMBEGA1UECAwKU29tZS1TdGF0ZTEhMB8GA1UE\n" \
    "CgwYSW50ZXJuZXQvZ21kZ210cyBqdHhkZHRkMIIBIjANBgkqhkiG9w0BAQEFAAO\n" \
    "CQ8AMIIBCgKCAQEAo8oThJXSMD041oL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
    "iXPnZkhVppLnj++/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
    "bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRC05Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
    "dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPWo/G4DyW34jOXzzEM\n" \
    "FLWvQOQLCKUZ0gjjBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
    "c64sS/ZBGPZFOPJmb4tG2nipygZ1h0/r++jCbWIDAQABMA0GCSqGS1b3DQEBCwUA\n" \
    "A4IBAQCdq59ubdRY9EiV3bleKXeqG7+8HgBHdm0X9dgq10nD37p00YLyuZLE9NM\n" \
    "066G/VcflGrx/Nzw+/UuI7/UuBbBS/3ppHRnsZqBI18nnr/ULrFQy8z3vKtL1q3C\n" \
    "DxabjPONlPO2keJeTTA71N/RCEMwJoa8i0XKXGdu/hQo6x4n+Gq73fEiGC199xsc\n" \
    "4tIO4yPS4lv+uXBzEUzoEy0CLikiDesnt5lLeCyPmUNoU89HU95IusZT7kygCHHD\n" \
    "72amlic3X8PKc268KT3ilr3VMhK67C+iIikfrM5AiU+oOIRrIHSC/p0RigJg3rXA\n" \
    "GBIRHvt+OYF9fDeG7U4QDJNcfGW+\n" \
    "-----END CERTIFICATE-----"

#define keyCLIENT_PRIVATE_KEY_PEM \
    "-----BEGIN RSA PRIVATE KEY-----\n" \
    "MIIEowIBAAKCAQEAo8oThJXSMD041oL7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \
    "iXPnZkhVppLnj++/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
    "bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRC05Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
    "dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPWo/G4DyW34jOXzzEM\n"
```

```
"FLWvQOQLCKUZ0gjJBnFdbx8o00wMkYCChbV7gqPE6cw0Zy26CvlLQiINyonLPbNT\n" \
"c64sS/ZBGPZFOPJmb4tG2nipYgZ1h0/r++jCbWIDAQABAoIBAQCGR2hC/ZVJhqiM\n" \
"c2uuJZKpElpIIBBPOObZwwS3IYR4UUjzVgMn7Ubbmxf1LXD8lzfZU4YVp0vTH5lC\n" \
"07qvYuXpHqtnj+GEok837VYctUY9AuHeDM/2paV3awNV15E1PFG1Jd3pqnH7tJw6\n" \
"VBZBDiGNntlagN/UnoSlmfvpU0r8VGPXCBNxe3JY5QyBJPIlwF4LcxRI+eYmr7Ja\n" \
"/cjn97DZotgz4B7gUNu8XIEkUOTwPabZINylzcLWiXTMA+8qTniPVk653h14Xqt4\n" \
"4o4D4YCTpwJcmxSV1m21/6+uyuXr9SIKAE+Ys2cYLA46x+rwLaW5fUoQ5hHa0Ytb\n" \
"RYJ4SrtBAoGBANwtw1E69N0hq5xDPckSbnGubIeG8P4mBhGkJxIqYoqugGLMDiGX\n" \
"4bltrjr2TPWaxTo3pPavLJiBMIsENA5KU+c/r0jLkxgEp9MIVJrtNgkCiDQqogBG\n" \
"j4IjL2iQwXoLCqk2tx/dh9Mww+7SETE7EPNrv4UrYaGN5AEvpf5W+NHPAoGBAMQ6\n" \
"wVa0Mx1PlA4enY2rfe3WXP8bzjleSOWr75JXqG2WbPC0/cszwbyPWOEqRpBZfvD\n" \
"QFkKx06xp1C09XwiQanr2gDucYXHeEKg/9iuJV1UkMQp95ojlhtSXdrZV7/14pmN\n" \
"fpB2vcAptX/4gY4tDrWMO08JNnrjE7duC+rmmk1hAoGAS4L0QLCNB/h2JOq+Uuhn\n" \
"/FGfmOVfFPFrA6D3DbxcxpWUWVwzSLvb0SOpHryzxbfEKyau7V5KbDp7ZSU/IC20\n" \
"KOyggjSEkAkDi7fjrrTRW/Cgg6g6G4YIOBO4qCtHdDbwJMHNdk6096qw5EzS67qLp\n" \
"Apz5OZ5zChySjri/+HnTxJECgYBysGSP6IJ3fytplTtAshnU5JU2BWpi3ViBoXoE\n" \
"bndilajWhvJO8dEqBB5OfAcCF0y6TnWt1T8oH21LHnjcNKlsRw0Dv1lbdloylybx\n" \
"3da41dRG0sCEtof1MB7nHdDLt/DZDnoKtVvyFG6gfp47utn+Ahgn+Zp6K+46J3eP\n" \
"s3g8AQKBgE/PJiaF8pbBXaZOuwRRA9GOMSbDIF6+jBYTYp4L9wk4+LZArKtyI+4k\n" \
Md2DUvHwMC+ddOtKqjYnLm+V5cSbvU7aPvBZtwxghzTUDcf7EvnA3V/bQBh3R0z7\n" \
pVsxTyGRmBSeLdbUWACUbx9LXdpuDarPAJ59daWmP3mBEVmwDzUw\n" \
"-----END RSA PRIVATE KEY-----"
```

```
void device_provisioning_example (void)
{
    /* Initialize IOT FreeRTOS Libraries */
    SYSTEM_Init();

    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);

    ProvisioningParams_t params;

    /* Provision device with provided credentials. The provided credentials are written
to data flash.

    * In production, the credentials can be provided over a comms channel instead of
being linked into the image.

    * The same example provisioning function, vAlternateKeyProvisioning, can be used in
```

```
that case. */
    params.pucClientPrivateKey      = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;
    params.pucClientCertificate     = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
    params.ulClientPrivateKeyLength = 1 + strlen((const char *)
params.pucClientPrivateKey);
    params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
    params.pucJITPCertificate       = NULL;
    params.ulJITPCertificateLength  = 0;
    vAlternateKeyProvisioning(&params);
}
```

## Limitations

The provisioning code is an example provided by AWS. It must be modified to meet product requirements.

### 4.2.103 AWS HTTPS

#### Modules

This module provides the AWS HTTPS integration documentation.

## Overview

The AWS HTTPS core library can be used to send HTTP and HTTPS requests. The documentation for the library can be found at the following link: [coreHTTP](#).

### Features

- Secure and Non-secure HTTP requests
- [Mutually authenticated connections](#)

## Configuration

### Memory Usage

The AWS HTTPS library relies heavily on dynamic memory allocation for thread/task creation as well as other uses. It is recommended to tweak the thread stack configuration values based on usage. Notable values are:

## AWS IoT Common

- IoT Thread Default Stack Size
- IoT Network Receive Task Stack Size

## FreeRTOS Thread

- General|Minimal Stack Size

## FreeRTOS Plus TCP

- Stack size in words (not bytes)

# Usage Notes

## Limitations

- MbedTLS must be initialized and key provisioning must be done before starting a secure connection. Refer to [AWS Secure Sockets](#).

## Examples

### HTTPS GET request

```
/* Certificate copied from https://www.amazontrust.com/repository/AmazonRootCA1.pem
*/
static const char g_server_certificate[] = "-----BEGIN CERTIFICATE-----\n" \
"MIIDQTCCAimgAwIBAgITBmyfz5m/jAo54vB4ikPmljZbyjANBgkqhkiG9w0BAQsF\n" \
"ADA5MQswCQYDVQQGEwJVUzEPMA0GA1UEChMGQW1hem9uMRkwFwYDVQQDExBBbWF6\n" \
"b24gUm9vdCBDQSAxMB4XDTE1MDUyNjAwMDAwMFoXDTE1MDUyNjAwMDAwMFowOTEL\n" \
"MAkGA1UEBhMCVVMxDzANBgNVBAoTBkFtYXNjaEYwZjEzZDk1ZDk1ZDk1ZDk1ZDk1\n" \
"b3QgQ0EgMTCCASIwDQYJKoZIhvcNAQEBBQADggEPADCCAQoCggEBALJ4gHHKeNXj\n" \
"ca9HgFB0fW7Y14h29Jlo91ghYPl0hAEvraIthtOgQ3p0sqTQNroBvo3bSMgHFzZM\n" \
"906II8c+6zfltrn4SWiw3te5djgdYZ6k/oI2peVKVuRF4fn9tBb6dNqcmzU5L/qw\n" \
"IFAGbHrQgLKm+a/sRxmPUDgH3KKHOVj4utWp+UhnMJbulHheb4mjUcAwhmahRWa6\n" \
"VOujw5H5SNz/0egwLX0tdHA114gk957EWW67c4cX8jJGKLhD+rcdqsq08p8kDi1L\n" \
"93FcXmn/6pUCyziKrlA4b9v7LWIbxcceVOF34GfID5yHI9Y/QCB/IIDEgEw+OyQm\n" \
"jgSubJrIqg0CAwEAAaNCMEAwDwYDVR0TAQH/BAUwAwEB/zAOBgNVHQ8BAf8EBAMC\n" \
"AYYwHQYDVR0OBBYEFIQYzIU07LwMlJQuCFmcx7IQTgoIMA0GCSqGSIb3DQEBCwUA\n" \
"A4IBAQC8jdaQZChGsV2USggNiMOruYou6r4lK5IpDB/G/wk jUu0yKGX9rbxenDI\n" \
"U5PMCCjjmCXPI6T53iHTfIUJrU6adTrCC2qJeHZERxh1bI1Bjtt/msv0tadQ1wUs\n" \
"N+gDS63pYaACbvXy8MWy7Vu33PqUXHeeE6V/Uq2V8viT096LXFvKWLJbYK8U90vv\n" \
"o/ufQJVtMVT8QtPHRh8jrdkPSHca2XV4cdFyQzR1bldZwgJcJmApzyMZFo6IQ6XU\n"
```

```
"5MsI+yMRQ+hDKXJioaldXgjUkK642M4UwtBV8ob2xJNDd2ZhwLnoQdeXeGADbkpy\n" \
"rqXRfboQnoZsG4q5WTP468SQvvG5\n" \
"-----END CERTIFICATE-----";
/* Default settings to use if DHCP fails. */
const uint8_t g_default_ip_address[4] = {192, 168, 0, 100};
const uint8_t g_default_subnet_mask[4] = {255, 255, 255, 0};
const uint8_t g_default_gateway[4] = {192, 168, 0, 1};
const uint8_t g_default_dns[4] = {8, 8, 8, 8};
void https_example_entry (void * pvParameters)
{
    FSP_PARAMETER_NOT_USED(pvParameters);
    /* Initialize IOT FreeRTOS Libraries */
    SYSTEM_Init();
    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);
    /* Initialize the logging task. */
    assert(pdPASS == xLoggingTaskInitialize(256, 1, 10));
    /* In order to use the PKCS11 PAL, littlefs must be configured. */
    fsp_err_t fsp_err_status = RM_LITTLEFS_FLASH_Open(g_rm_littlefs0.p_ctrl,
g_rm_littlefs0.p_cfg);
    assert(FSP_SUCCESS == fsp_err_status);
    /* Reformat littlefs to ensure that data flash is in a known state. */
    assert(0 == lfs_format(&g_rm_littlefs0_lfs, &g_rm_littlefs0_lfs_cfg));
    /* Mount littlefs. */
    assert(0 == lfs_mount(&g_rm_littlefs0_lfs, &g_rm_littlefs0_lfs_cfg));
    /*
    * Write the keys into data flash using the PKCS11 PAL so that they can be used
during TLS setup
    * Note that in an application this will only be done when provisioning a device
with a private key.
    * Once a device has been provisioned, the keys will persist in data flash.
    */
    ProvisioningParams_t params;
    params.pucClientPrivateKey = (uint8_t *) g_client_private_key;
```

```
params.pucClientCertificate      = (uint8_t *) g_client_certificate;
params.ulClientPrivateKeyLength = sizeof(g_client_private_key);
params.ulClientCertificateLength = sizeof(g_client_certificate);
params.pucJITPCertificate        = NULL;
params.ulJITPCertificateLength   = 0;
uint32_t err = (uint32_t) vAlternateKeyProvisioning(&params);
assert(0 == err);
/* Start up the network stack. */
FreeRTOS_IPInit(g_default_ip_address,
                g_default_subnet_mask,
                g_default_gateway,
                g_default_dns,
                g_ether0.p_cfg->p_mac_address);
while (pdFALSE == FreeRTOS_IsNetworkUp())
{
    vTaskDelay(10);
}
ServerInfo_t      xServerInfo      = {0};
SocketsConfig_t   xSocketsConfig   = {0};
TransportSocketStatus_t xNetworkStatus = TRANSPORT_SOCKET_STATUS_SUCCESS;
/* Initializer server information. */
xServerInfo.pHostName      = "postman-echo.com";
xServerInfo.hostNameLength = strlen(xServerInfo.pHostName);
xServerInfo.port           = HTTPS_EXAMPLE_TLS_PORT;
/* Configure credentials for TLS authenticated session. */
xSocketsConfig.enableTls      = true;
xSocketsConfig.pAlpnProtos    = NULL;
xSocketsConfig.maxFragmentLength = 0;
xSocketsConfig.disableSni     = false;
xSocketsConfig.pRootCa        = g_server_certificate;
xSocketsConfig.rootCaSize     = sizeof(g_server_certificate);
xSocketsConfig.sendTimeoutMs  = HTTPS_EXAMPLE_TIMEOUT;
xSocketsConfig.recvTimeoutMs  = HTTPS_EXAMPLE_TIMEOUT;
NetworkContext_t xNetworkContext = {0};
```

```
/* Attempt to create a authenticated TLS connection. */
    xNetworkStatus = SecureSocketsTransport_Connect(&xNetworkContext, &xServerInfo,
&xSocketsConfig);

    assert(TRANSPORT_SOCKET_STATUS_SUCCESS == xNetworkStatus);

    TransportInterface_t xTransportInterface;
/* Define the transport interface. */
    xTransportInterface.pNetworkContext = &xNetworkContext;
    xTransportInterface.send           = SecureSocketsTransport_Send;
    xTransportInterface.recv          = SecureSocketsTransport_Recv;
    HTTPRequestInfo_t    xRequestInfo    = {0};
    HTTPRequestHeaders_t xRequestHeaders = {0};
/* Configure a GET request. */
    xRequestInfo.pHost      = "postman-echo.com";
    xRequestInfo.hostLen   = strlen(xRequestInfo.pHost);
    xRequestInfo.pMethod   = HTTP_METHOD_GET;
    xRequestInfo.methodLen = strlen(HTTP_METHOD_GET);
    xRequestInfo.pPath     = "/get?arg1=val1&arg2=val2";
    xRequestInfo.pathLen   = strlen(xRequestInfo.pPath);
    xRequestInfo.reqFlags = HTTP_REQUEST_KEEP_ALIVE_FLAG;
/* Set the buffer used for storing request headers. */
static uint8_t ucUserBuffer[HTTPS_EXAMPLE_USER_BUFFER_SIZE];
    xRequestHeaders.pBuffer = ucUserBuffer;
    xRequestHeaders.bufferLen = sizeof(ucUserBuffer);
/* Initialize the request. */
    HTTPStatus_t xHTTPStatus = HTTPClient_InitializeRequestHeaders(&xRequestHeaders,
&xRequestInfo);
    assert(HTTPSSuccess == xHTTPStatus);
/* Reuse the user buffer for storing the response headers. */
    HTTPResponse_t xResponse = {0};
    xResponse.pBuffer = ucUserBuffer;
    xResponse.bufferLen = sizeof(ucUserBuffer);
/* Send the request. */
    xHTTPStatus = HTTPClient_Send(&xTransportInterface, &xRequestHeaders, (uint8_t *)
NULL, 0, &xResponse, 0);
```

```
assert(HTTPSSuccess == xHTTPStatus);  
  
xNetworkStatus = SecureSocketsTransport_Disconnect(&xNetworkContext);  
  
assert(TRANSPORT_SOCKET_STATUS_SUCCESS == xNetworkStatus);  
  
/* The HTTPS request has completed. The result is stored in xResponse. */  
}
```

## 4.2.104 AWS MQTT

### Modules

This module provides the AWS MQTT integration documentation.

## Overview

The AWS MQTT library can connect to either AWS or a third party MQTT broker such as [Mosquitto](#). The documentation for the library can be found on the [AWS IoT Device SDK C: MQTT](#) website.

### Features

- MQTT connections over TLS to an AWS IoT Endpoint or Mosquitto server
- Unsecure MQTT connections to Mosquitto servers. This is not recommended for production and should only be done to a local server for testing.

## Configuration

### Memory Usage

The AWS MQTT library relies heavily on dynamic memory allocation for thread/task creation as well as other uses. Depending on the configuration it may be required to provide as much as 110k heap. To decrease this it is recommended to tweak the thread stack configuration values based on usage. Notable values are:

### AWS IoT Common

- IoT Thread Default Stack Size
- IoT Network Receive Task Stack Size

### FreeRTOS Thread

- General|Minimal Stack Size

### FreeRTOS Plus TCP

- Stack size in words (not bytes)

## Usage Notes

The AWS MQTT library utilizes a system taskpool to queue up messages. This system task pool must be created before calling into the MQTT library. `iot_init.c` has been provided for easy initialization of this taskpool via `lotSdk_Init()`.

The AWS MQTT Demo has been provided to easily demonstrate MQTT functionality. An example of initializing the system taskpool and running the MQTT demo has been provided below.

### Limitations

- `aws_clientcredential.h` and `aws_clientcredential_keys.h` need to be added manually.
- The IoT Thread must have a higher priority than the Network Receive Thread.
- MbedTLS must be initialized and key provisioning must be done before starting a secure connection. Refer to [AWS Secure Sockets](#).

### Examples

#### Non-secure connection to a Mosquitto server

```
#define IOT_LOG_STACK_SIZE (256)
const uint8_t g_ip_address[4] = {169, 254, 57, 49};
const uint8_t g_net_mask[4] = {255, 255, 0, 0};
const uint8_t g_gateway_address[4] = {169, 254, 57, 49};
const uint8_t g_dns_address[4] = {8, 8, 8, 8};
const uint8_t g_mac_address[6] = {0x66, 0x66, 0x66, 0x66, 0x66, 0x66};
void mqtt_non_secure_example ()
{
    /* Initialize IOT FreeRTOS Libraries */
    SYSTEM_Init();
    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);
    xLoggingTaskInitialize(IOT_LOG_STACK_SIZE, 1, 10);
    /* Start up the network stack. */
    FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
    while (pdFALSE == FreeRTOS_IsNetworkUp())
    {
        vTaskDelay(1);
    }
    Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKETS_IPPROTO_TCP);
```

```

if (SOCKETS_INVALID_SOCKET == socket)
{
/* Could not create socket. */
    __BKPT(0);
}

/* AWS MQTT APIs can now be called. Please refer to the documentation linked above.
*/

/* If using the MQTT Wrapper IotSdk_Init() must be called prior to using MQTT. */
}

```

## Secure connection to a Mosquitto server

### Note

*MbedTLS must be initialized and key provisioning must be done before starting a secure connection. Refer to [AWS Secure Sockets](#).*

```

#define keyCLIENT_CERTIFICATE_PEM \
    "-----BEGIN CERTIFICATE-----\n" \
    "example_certificate_formatting\n" \
    "-----END CERTIFICATE-----"

#define keyCLIENT_PRIVATE_KEY_PEM \
    "-----BEGIN RSA PRIVATE KEY-----\n" \
    "example_certificate_formatting\n" \
    "-----END RSA PRIVATE KEY-----"

void mqtt_secure_example ()
{
/* Initialize IOT FreeRTOS Libraries */
    SYSTEM_Init();

/* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);

    xLoggingTaskInitialize(IOT_LOG_STACK_SIZE, 1, 10);

    ProvisioningParams_t params;

/* Write the keys into a secure region in data flash. */
    params.pucClientPrivateKey      = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;
    params.pucClientCertificate     = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
    params.ulClientPrivateKeyLength = 1 + strlen((const char *)

```

```

params.pucClientPrivateKey);
    params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
    params.pucJITPCertificate      = NULL;
    params.ulJITPCertificateLength = 0;
    vAlternateKeyProvisioning(&params);
/* Start up the network stack. */
    FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
while (pdFALSE == FreeRTOS_IsNetworkUp())
    {
        vTaskDelay(1);
    }
    Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKETS_IPPROTO_TCP);
if (SOCKETS_INVALID_SOCKET == socket)
    {
/* Could not create socket. */
        __BKPT(0);
    }
/* AWS MQTT APIs can now be called. Please refer to the documentation linked above.
*/
/* If using the MQTT Wrapper IotSdk_Init() must be called prior to using MQTT. */
}

```

## 4.2.105 Wifi Middleware (rm\_wifi\_onchip\_silex)

### Modules

#### Functions

fsp\_err\_t RM\_WIFI\_ONCHIP\_SILEX\_EpochTimeGet (time\_t \*p\_utc\_time)

fsp\_err\_t RM\_WIFI\_ONCHIP\_SILEX\_LocalTimeGet (uint8\_t \*p\_local\_time,  
uint32\_t size\_string)

fsp\_err\_t RM\_WIFI\_ONCHIP\_SILEX\_SntpEnableSet

(wifi\_onchip\_silex\_sntp\_enable\_t enable)

fsp\_err\_t RM\_WIFI\_ONCHIP\_SILEX\_SntpServerIpAddressSet (uint8\_t \*p\_ip\_address)

fsp\_err\_t RM\_WIFI\_ONCHIP\_SILEX\_SntpTimeZoneSet (int32\_t hours, uint32\_t minutes, wifi\_onchip\_silex\_sntp\_daylight\_savings\_enable\_t daylightSavingsEnable)

## Detailed Description

Wifi and Socket implementation using the Silex SX-ULPGN WiFi module on RA MCUs.

## Overview

This Middleware module supplies an implementation for the [FreeRTOS Secure Sockets and WiFi interfaces](#) using the Silex SX-ULPGN module.

You can find specifics about the WiFi and Secure Socket interface APIs supported by this module at these web sites: [Secure Sockets API](#) or [Wifi API](#).

The SX-ULPGN is a low-power, compact IEEE 802.11b/g/n 2.4GHz 1x1 Wireless LAN module equipped with the Qualcomm® QCA4010 Wireless SOC. The module comes readily equipped with radio certification for Japan, North America and Europe. More information about this module can be found at the [Silex Web Site](#)

## Features

The WiFi Onchip Silex Middleware driver supplies these features:

- Supports connect/disconnect to a b/g/n (2.4GHz) WiFi Access Point using Open, WPA, and WPA2 security. Encryption types can be either TKIP, or CCMP(AES).
- Supports retrieval of the module device MAC address.
- Once connected you can acquire the assigned module device IP.
- Supports a WiFi network scan capability to get a list of local Access Points.
- Supports a Ping function to test network connectivity.
- Supports a DNS Query call to retrieve the IPv4 address of a supplied URL.
- Supports a BSD style Secure Socket interface.
- Drive supports 1 or 2 UARTs for interfacing with the SX-ULPGN module. The second UART is considered optional.

## Configuration

### Build Time Configurations for rm\_wifi\_onchip\_silex

The following build time configurations are defined in fsp\_cfg/rm\_wifi\_onchip\_silex\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

Number of supported socket instances	Refer to the RA Configuration tool for available options.	1	Enable number of socket instances
Size of RX buffer for socket	Manual Entry	4096	
Size of TX buffer for CMD Port	Manual Entry	1500	
Size of RX buffer for CMD Port	Manual Entry	3000	
Semaphore maximum timeout	Manual Entry	10000	
Number of retries for AT commands	Manual Entry	10	
Module Reset Port	Refer to the RA Configuration tool for available options.	06	Specify the module reset pin port for the MCU.
Module Reset Pin	Refer to the RA Configuration tool for available options.	03	Specify the module reset pin for the MCU.
Enable SNTP Client	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Should the SNTP client of the module be enabled

### Configurations for Middleware > WiFi > WiFi Onchip Silex Driver using r\_sci\_uart

Configuration	Options	Default	Description
SNTP server IPv4 address	Must be a valid IPv4 address	0.0.0.0	
STNP Timezone Offset from UTC Hours	Must be between 12 and -12 hours	0	Value in hours from 12 to -12
STNP Timezone Offset from UTC Minutes	Must be between 0 and 59 minutes	0	Value in minutes from 0 to 59
Use Daylight Savings Time	<ul style="list-style-type: none"> <li>• Enabled</li> <li>• Disabled</li> </ul>	Disabled	Specify if daytime savings should be used for local time calculation

Note: It is suggested that when using the Silex Module that DTC and FIFO are enabled in the UART configuration to facilitate a more reliable data transfer between module and MCU.

Note: If you wish to use flow control then you must enable flow control in the RA Configuration editor. This can be found in the UART setting. It is advantageous to use flow control all the time since it allows the hardware to gate the flow of data across the serial bus. Without hardware flow control for faster data rate you will most likely see an overflow condition between MCU and the module device.

Note: Higher baud rates are supported in the RA Configuration editor and should be changed in the first UART configuration. There is no need to change the second UART baud rate since it is only used

as an AT command channel.

Note: It is a good idea to also enable the FIFO in the UART configuration settings if you plan to use higher baud rates.

## Interrupt Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#). `R_SCI_UART_Open()` is called by [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#).

## Clock Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#).

## Pin Configuration

Refer to [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#). `R_SCI_UART_Open()` is called by [Wifi Middleware \(rm\\_wifi\\_onchip\\_silex\)](#)

# Usage Notes

## Limitations

- WiFi AP connections do not currently support WEP security.
- When operating with a single UART only single socket connections are possible. To support multiple sockets two UART channels must be connected to the module. When using the Renesas-provided SX-ULPGN PMOD board the second UART channel is on pins 9 and 10 of the PMOD header.
- Network connection parameters SSID and Passphrase for the Access Point can not contain any commas. This is a current limitation of the Silex module firmware. The `rm_wifi_onchip_silex_connect()` function will return an error if a comma is detected.
- When operating with a single UART and there is an active socket connection you cannot call `WIFI_Scan()`, `WIFI_Ping()`, `SOCKETS_GetHostByName()`, `WIFI_GetMAC()`, or `WIFI_GetIPInfo()`. Calling one of these function will return an error code in this situation. These commands are blocked in the one UART case during an active socket connection because they could cause data loss. To avoid this limitation please configure the hardware to use both UARTs.
- The Silex WiFi modules SNTP support requires all configuration changes to be made when the WiFi is disconnected from an Access Point. This is a limitation of the Silex module firmware. If changes to the default SNTP settings are required then the application will have to close the current AP connection, make the necessary SNTP changes, and then re-establish the original connection.

# Examples

## Basic Example

This is a basic example of minimal use of WiFi Middleware in an application.

```
void wifi_onchip_basic_example (void)
{
    WIFIReturnCode_t wifi_err;

    /* Setup Access Point connection parameters */
```

```
WIFINetworkParams_t net_params =
{
    .ucChannel                = 0,
    .xPassword.xWPA.cPassphrase = "password",
    .ucSSID                   = "access_point_ssid",
    .xPassword.xWPA.ucLength  = 8,
    .ucSSIDLength             = 17,
    .xSecurity                 = eWiFiSecurityWPA2,
};

SocketsSockaddr_t addr        = {0};
int32_t            number_bytes_rx = 0;
int32_t            number_bytes_tx = 0;

memset(scan_data, 0, sizeof(WIFIScanResult_t) * MAX_WIFI_SCAN_RESULTS);
memset(g_socket_recv_buffer, 0, sizeof(uint8_t) * SX_WIFI_SOCKET_RX_BUFFER_SIZE);
/* Open connection to the Wifi Module */
wifi_err = WIFI_On();
assert(eWiFiSuccess == wifi_err);
/* Connect to the Access Point */
wifi_err = WIFI_ConnectAP(&net_params);
assert(eWiFiSuccess == wifi_err);
/* Get address assigned by AP */
WIFIIPConfiguration_t ipInfo;
wifi_err = WIFI_GetIPInfo(&ipInfo);
assert(eWiFiSuccess == wifi_err);
/* Ping an address accessible on the network */
uint8_t ip_address[4] = {216, 58, 194, 174}; // NOLINT
const uint16_t ping_count    = 3;
const uint32_t intervalMS   = 100;
wifi_err = WIFI_Ping(&ip_address[0], ping_count, intervalMS);
assert(eWiFiSuccess == wifi_err);
/* Scan the local Wifi network for other APs */
wifi_err = WIFI_Scan(&scan_data[0], MAX_WIFI_SCAN_RESULTS);
assert(eWiFiSuccess == wifi_err);
/* Do a DNS Query for IP address of server */
```

```
    addr.ulAddress = SOCKETS_GetHostByName("www.renesas.com");
    addr.usPort    = SOCKETS_htons(80);
/* Initialize the Socket Interface */
    BaseType_t sock_err = SOCKETS_Init();
    assert(pdPASS == sock_err);
/* Create a socket instance */
    Socket_t socket1 = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKET_IPPROTO_TCP);
    assert(NULL != socket1);
/* Connect to an server using address */
    sock_err = SOCKETS_Connect(socket1, &addr, sizeof(SocketsSockaddr_t));
    assert(pdPASS == sock_err);
/* Send a HTTP Get call to server */
    number_bytes_tx = SOCKETS_Send(socket1, HTTP_GET_string, strlen(HTTP_GET_string),
0);
    assert(number_bytes_tx > 0);
/* Receive the HTTP GET call reply */
    number_bytes_rx = SOCKETS_Recv(socket1, g_socket_recv_buffer,
SX_WIFI_SOCKET_RX_BUFFER_SIZE, 0);
    assert(number_bytes_rx > 0);
/* Close the socket connection */
    SOCKETS_Close(socket1);
/* Shutdown the WIFI and Socket Interfaces */
    WIFI_Off();
}
```

## SNTP example

An example of using Simple Network Time Protocol (SNTP) on WiFi in an application.

```
#define RM_WIFI_ONCHIP_SILEX_TEMP_BUFFER_SIZE (64)
/*
 * Example of the use of SNTP with Wifi. Example gets the epoch time and local
 * system time strings. It is also demonstrated how the user will need to disconnect
 * from the access point to make changes to the SNTP configuration during runtime.
 */
```

```
*
* Function assumes that the SNTP has been enabled and configured with proper
* SNTP server address. For brevity error checking has not been implemented.
*
*/
void wifi_onchip_sntp_example (void)
{
    /* Setup Access Point connection parameters */
    WIFINetworkParams_t net_params =
    {
        .ucSSID                = "access_point_ssid",
        .ucSSIDLength          = 17,
        .xPassword.xWPA.cPassphrase = "password",
        .xPassword.xWPA.ucLength  = 8,
        .ucChannel              = 0,
        .xSecurity               = eWiFiSecurityWPA2
    };
    uint8_t local_time[RM_WIFI_ONCHIP_SILEX_TEMP_BUFFER_SIZE];
    time_t current_sys_time = 0;
    // SNTP IP address
    uint8_t ip_address_sntp_server_valid[4] = {216, 239, 35, 0}; // NOLINT : Static
IP address
    memset(local_time, 0, sizeof(local_time));
    /* Open connection to the Wifi Module */
    WIFI_On();
    /* Connect to the Access Point */
    WIFI_ConnectAP(&net_params);
    /* Get the Epoch time in seconds since Jan 1, 1970 UTC */
    RM_WIFI_ONCHIP_SILEX_EpochTimeGet(&current_sys_time);
    /* Get the local time string */
    RM_WIFI_ONCHIP_SILEX_LocalTimeGet((uint8_t *) local_time, sizeof(local_time));
    /* Disconnect from the access point to make changes to the SNTP configuration */
    WIFI_Disconnect();
    /* Change the IP address of the server */
}
```

```

RM_WIFI_ONCHIP_SILEX_SntpServerIpAddressSet((uint8_t *)
ip_address_sntp_server_valid);
/* Change the timezone to PST with daylight saving enabled */
RM_WIFI_ONCHIP_SILEX_SntpTimeZoneSet(-7, 0,
WIFI_ONCHIP_SILEX_SNTP_DAYLIGHT_SAVINGS_ENABLE);
/* Connect back to the access point */
WIFI_ConnectAP(&net_params);
/* Get the Epoch time in seconds since Jan 1, 1970 UTC */
RM_WIFI_ONCHIP_SILEX_EpochTimeGet(&current_sys_time);
/* Get the local time string in format [DayOfWeek Month DayOfMonth Year
Hour:Minute:Second] */
RM_WIFI_ONCHIP_SILEX_LocalTimeGet((uint8_t *) local_time, sizeof(local_time));
/* Disconnect from the Access Point and shutdown the WIFI module*/
WIFI_Disconnect();
WIFI_Off();
}

```

## Multi-Socket Example

### Data Structures

```
struct wifi_onchip_silex_cfg_t
```

```
struct ulpgn_socket_t
```

```
struct wifi_onchip_silex_instance_ctrl_t
```

### Enumerations

```
enum sx_ulpgn_socket_status_t
```

```
enum sx_ulpgn_socket_rw
```

```
enum wifi_onchip_silex_sntp_enable_t
```

```
enum wifi_onchip_silex_sntp_daylight_savings_enable_t
```

## Data Structure Documentation

### ◆ wifi\_onchip\_silex\_cfg\_t

```
struct wifi_onchip_silex_cfg_t
```

User configuration structure, used in open function		
Data Fields		
const uint32_t	num_uarts	Number of UART interfaces to use.
const uint32_t	num_sockets	Number of sockets to initialize.
const bsp_io_port_pin_t	reset_pin	Reset pin used for module.
const uart_instance_t *	uart_instances[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	SCI UART instances.
const wifi_onchip_silex_sntp_enable_t	sntp_enabled	Enable/Disable the SNTP Client.
const uint8_t *	sntp_server_ip	The SNTP server IP address string.
const int32_t	sntp_timezone_offset_from_utc_hours	Timezone offset from UTC in (+/-) hours.
const uint32_t	sntp_timezone_offset_from_utc_minutes	Timezone offset from UTC in minutes.
const wifi_onchip_silex_sntp_daylight_savings_enable_t	sntp_timezone_use_daylight_savings	Enable/Disable use of daylight saving time.
void const *	p_context	User defined context passed into callback function.
void const *	p_extend	Pointer to extended configuration by instance of interface.

#### ◆ ulpgn\_socket\_t

struct ulpgn_socket_t		
Silex ULPGN Wifi internal socket instance structure		
Data Fields		
StreamBufferHandle_t	socket_byteq_hdl	Socket stream buffer handle.
StaticStreamBuffer_t	socket_byteq_struct	Structure to hold stream buffer info.
uint8_t	socket_recv_buff[WIFI_ONCHIP_SILEX_CFG_MAX_SOCKET_RX_SIZE]	Socket receive buffer used by byte queue.
uint32_t	socket_status	Current socket status.
uint32_t	socket_recv_error_count	Socket receive error count.
uint32_t	socket_create_flag	Flag to determine if socket has been created.
uint32_t	socket_read_write_flag	flag to determine if read and/or

write channels are active.

◆ **wifi\_onchip\_silex\_instance\_ctrl\_t**

struct wifi_onchip_silex_instance_ctrl_t		
WIFI_ONCHIP_SILEX private control block. DO NOT MODIFY.		
Data Fields		
uint32_t	open	Flag to indicate if wifi instance has been initialized.
wifi_onchip_silex_cfg_t const *	p_wifi_onchip_silex_cfg	Pointer to initial configurations.
bsp_io_port_pin_t	reset_pin	Wifi module reset pin.
uint32_t	num_uarts	number of UARTS currently used for communication with module
uint32_t	tx_data_size	Size of the data to send.
uint32_t	num_creatable_sockets	Number of simultaneous sockets supported.
uint32_t	curr_cmd_port	Current UART instance index for AT commands.
uint32_t	curr_data_port	Current UART instance index for data.
uint8_t	cmd_rx_queue_buf[WIFI_ONCHIP_SILEX_CFG_CMD_RX_BUF_SIZE]	Command port receive buffer used by byte queue // FreeRTOS.
StreamBufferHandle_t	socket_byteq_hdl	Socket stream buffer handle.
StaticStreamBuffer_t	socket_byteq_struct	Structure to hold stream buffer info.
volatile uint32_t	curr_socket_index	Currently active socket instance.
uint8_t	cmd_tx_buff[WIFI_ONCHIP_SILEX_CFG_CMD_TX_BUF_SIZE]	Command send buffer.
uint8_t	cmd_rx_buff[WIFI_ONCHIP_SILEX_CFG_CMD_RX_BUF_SIZE]	Command receive buffer.
uint32_t	at_cmd_mode	Current command mode.
uint8_t	curr_ipaddr[4]	Current IP address of module.
uint8_t	curr_subnetmask[4]	Current Subnet Mask of module.
uint8_t	curr_gateway[4]	Current GATeway of module.
SemaphoreHandle_t	tx_sem	Transmit binary semaphore handle.
SemaphoreHandle_t	rx_sem	Receive binary semaphore

		handle.
uint8_t	last_data[WIFI_ONCHIP_SILEX_RETURN_TEXT_LENGTH]	Tailing buffer used for command parser.
uart_instance_t*	uart_instance_objects[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	UART instance objects.
SemaphoreHandle_t	uart_tei_sem[WIFI_ONCHIP_SILEX_CFG_MAX_NUMBER_UART_PORTS]	UART transmission end binary semaphore.
ulpgn_socket_t	sockets[WIFI_ONCHIP_SILEX_CFG_NUM_CREATEABLE_SOCKETS]	Internal socket instances.

## Enumeration Type Documentation

### ◆ sx\_ulpgn\_socket\_status\_t

enum <a href="#">sx_ulpgn_socket_status_t</a>
Silex ULPGN Wifi socket status types

### ◆ sx\_ulpgn\_socket\_rw

enum <a href="#">sx_ulpgn_socket_rw</a>
Silex socket shutdown channels

### ◆ wifi\_onchip\_silex\_sntp\_enable\_t

enum <a href="#">wifi_onchip_silex_sntp_enable_t</a>
Silex WiFi module enable/disable for SNTP

### ◆ wifi\_onchip\_silex\_sntp\_daylight\_savings\_enable\_t

enum <a href="#">wifi_onchip_silex_sntp_daylight_savings_enable_t</a>
Silex WiFi module enable/disable for SNTP

## Function Documentation

◆ **RM\_WIFI\_ONCHIP\_SILEX\_EpochTimeGet()**

`fsp_err_t RM_WIFI_ONCHIP_SILEX_EpochTimeGet ( time_t * p_utc_time)`

Get the current system time as the number of seconds since epoch 1970-01-01 00:00:00 UTC

This will retrieve time info from an NTP server at the address entered via an during configuration. If the server isn't set or the client isn't enabled, then it will return an error. The date/time is retrieved as the number of seconds since 00:00:00 UTC January 1, 1970

**Parameters**

[out]	p_utc_time	Returns the epoch time in seconds.
-------	------------	------------------------------------

**Return values**

FSP_SUCCESS	Successfully retrieved the system time from module.
FSP_ERR_ASSERTION	The parameter utc_time or p_instance_ctrl is NULL.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_WIFI\_ONCHIP\_SILEX\_LocalTimeGet()**

```
fsp_err_t RM_WIFI_ONCHIP_SILEX_LocalTimeGet ( uint8_t * p_local_time, uint32_t size_string )
```

Get the current local time based on current timezone in a string format

Get the current local time based on current timezone in a string . Exp: Wed Oct 15 1975 07:06:00

**Parameters**

[out]	p_local_time	Returns local time in string format.
[in]	size_string	Size of p_local_time string buffer.The size of this string needs to be at least 25 bytes

**Return values**

FSP_SUCCESS	Successfully returned the local time string.
FSP_ERR_ASSERTION	The parameter local_time or p_instance_ctrl is NULL.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_SIZE	String size value passed in exceeds maximum.

◆ **RM\_WIFI\_ONCHIP\_SILEX\_SntpEnableSet()**

```
fsp_err_t RM_WIFI_ONCHIP_SILEX_SntpEnableSet ( wifi_onchip_silex_sntp_enable_t enable)
```

Enable or Disable the SNTP Client Service

Set the SNTP Client to Enable or Disable

**Parameters**

[in]	enable	Can be set to enable/disable for SNTP support.
------	--------	--

**Return values**

FSP_SUCCESS	Successfully set the value.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.

◆ **RM\_WIFI\_ONCHIP\_SILEX\_SntpServerIpAddressSet()**

`fsp_err_t RM_WIFI_ONCHIP_SILEX_SntpServerIpAddressSet ( uint8_t * p_ip_address)`

Update the SNTP Server IP Address

Set the SNTP Client Server IP Address

**Parameters**

[in]	p_ip_address	Pointer to IP address of SNTP server in byte array format.
------	--------------	--

**Return values**

FSP_SUCCESS	Successfully set the value.
FSP_ERR_ASSERTION	The parameter p_ip_address or p_instance_ctrl is NULL.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ RM\_WIFI\_ONCHIP\_SILEX\_SntpTimeZoneSet()

```
fsp_err_t RM_WIFI_ONCHIP_SILEX_SntpTimeZoneSet ( int32_t hours, uint32_t minutes,
wifi_onchip_silex_sntp_daylight_savings_enable_t daylightSavingsEnable )
```

Update the SNTP Timezone

Set the SNTP Client Timezone

#### Parameters

[in]	hours	Number of hours (+/-) used for timezone offset from GMT.
[in]	minutes	Number of minutes used for timezone offset from GMT.
[in]	daylightSavingsEnable	Enable/Disable daylight saving in the timezone calculation.

#### Return values

FSP_SUCCESS	Successfully set the value.
FSP_ERR_WIFI_FAILED	Error occurred with command to Wifi module.
FSP_ERR_NOT_OPEN	Module is not open.
FSP_ERR_INVALID_ARGUMENT	Parameter passed into function was invalid.

## 4.2.106 AWS Secure Sockets

### Modules

This module provides the AWS Secure Sockets implementation.

## Overview

### Features

Information about the features provided by the AWS Secure Sockets Library is available in the [FreeRTOS Libraries User Guide](#).

The FSP implementation supports using Secure Sockets with either Ethernet or WiFi. These stacks can be added in FSP via the RA Configuration editor under FreeRTOS | Secure Sockets.

### Dependencies

The Secure Sockets library has two dependencies:

1. A TCP/IP implementation
2. A TLS implementation

For TCP/IP, AWS have provided the FreeRTOS TCP/IP implementation. For TLS, AWS have chosen mbedTLS, but use PKCS11 for storage and invoking the crypto portion of mbedTLS. For more information about AWS Secure Sockets, refer to the [AWS documentation](#). An example of Secure Sockets usage is on the same page.

## mbedTLS

[mbedTLS](#) is ARM's implementation of the TLS and SSL protocols as well as the cryptographic primitives required by those implementations. mbedTLS is also solely used for its cryptographic features even if the TLS/SSL portions are not used. With [PSA](#), ARM have created a separate API for cryptography. Starting with mbedTLS3, crypto implementation has been moved out to a new module called mbedCrypto (PSA Crypto API) and a build time configuration can direct the mbedTLS3 implementation to use either the old mbedtls cryptography functions or use the new PSA Crypto API. Since the current version of mbedCrypto (PSA Crypto API) implements both the old mbedtls crypto API as well as the new PSA Crypto API, either option is functional for now.

## CipherSuites

During the TLS connection setup stage, the client has to indicate to the server the type of cryptographic operations that it supports. This is referred to as the ciphersuite. The entire list of ciphersuites supported by mbedTLS can be found in `mbedtls/ssl_ciphersuites.h`.

## Configuration

In FSP, Secure Sockets can be added as a new stack via FreeRTOS | Secure Sockets | Secure Sockets on WiFi or Secure Sockets on FreeRTOS Plus TCP. All required dependant modules, except heap, are automatically added. To complete the configuration,

- Add a heap instance and use the same one for all dependencies.
- Resolve the module configuration requirements.

## Usage Notes

For detailed documentation on Secure Sockets consult the [AWS documentation](#).

## Examples

### Basic Example

This is a basic example of using the Secure Sockets API with Ethernet. The message "hello, world!" is sent to a remote socket.

```
#define SECURE_SOCKETS_EXAMPLE_BUFFER_SIZE (64)
static const char SERVER_CERTIFICATE_PEM[] =
"-----BEGIN CERTIFICATE-----\n"
"MIIDazCCA1OgAwIBAgIURabL79ayIywQv0y8SPnbZ1FYDRIwDQYJKoZIhvcNAQEL\n"
```

```

"BQAwRTELMAkGA1UEBhMCQVUxEzARBgNVBAGMClNvbWUtU3RhdGUxITAfBgNVBAoM\n"
"GE1udGVybmV0IFdpZGdpdHMgUHR5IEEx0ZDAeFw0xOTA5MTEyMTIyMjZaFw0yMDA5\n"
"MTAyMTIyMjZaMEUxCzAJBgNVBAYTAFVMRMwEQYDVQQLIDApTb211LVN0YXR1MSEw\n"
"HwYDVQQKBHJbnRlcm5ldCBXaWRnaXRzIFB0eSBMdGQwggEiMA0GCSqGSIb3DQEB\n"
"AQUAA4IBDwAwggEKAoIBAQDSA3h+5sT58FHgnovnQzsVHQ0H/3TsnEKwVzyBwTQ1\n"
"s4PbG6VXCWyyJWjdJ4XMH1oU8gAlxauFbw0098Aquei4K3Pi/ynKNBeX4VJcLyE5\n"
"Azq7nRIIwt4+OoZ5kV7v8JIoLY5i+Ktn3zq1t0y1ZmK6Uk/rRPonb+Kx7wQPX7jq\n"
"ZIZGda+CgF6ZedidPcABuggqDly3U2gLiRPObhe9nN2hG60rRp7vhhbWMF0pzTDXu\n"
"BKF7XSTbhYz3pl6NeOCLh5E3t8x908Ui5W1zDN3iOysrcwQFtCiGTvzNtxSflil+\n"
"PugIt9Q2vlymuz5qI+juxHftJSX086M5SV7exqUOXP9RagMBAAGjUzBRMB0GA1Ud\n"
"DgQWBQBQ8VNJEJUjptKMjmrOY3XApNp5lDAfBgNVHSMEGDAWgBQG8VNJEJUjptKM\n"
"jmrOY3XApNp5lDAPBgNVHRMBAf8EBTADAQH/MA0GCSqGSIb3DQEBCwUAA4IBAQA\n"
"CabfjsYUnG8tt3/GDdhjsuG+SfeQe1lS73pZi3+L616bPH5MNUv+LkgR/1AFEqt5\n"
"WadKVTgzW5Ork1t7CfkYwrOHbyhyaaDPzERjMcfCc18lQluBy6vE/1Eb0hWq6XlO\n"
"f6+8i+VKxWkSIXs2ZQqQYSOTTzAjHSsiuE5WsC00ErvCvnC7uD6+3Y7W1uQRkFZ\n"
"uSd9AN1ixPvAFi69FF/ymlJv6vII5GXOVDriwdr50bMNuezMEex6qMNDADRH8ieaL\n"
"JaSgfk1czGi1li7MPD4JTtsXOgKwxcBDAA0zQDVA5uBGEIOhva3m5X70N4i07W0V\n"
"eEhZekKeg3F13t/CXi81\n"
"-----END CERTIFICATE-----";

#define keyCLIENT_CERTIFICATE_PEM \
"-----BEGIN CERTIFICATE-----\n" \
"MIIDETCCAfKCFHwd2yn8zn5qB2ChYUT9Mvbi9Xp1MA0GCSqGSIb3DQEBCwUAMEUx\n" \
"CzAJBgNVBAYTAFVMRMwEQYDVQQLIDApTb211LVN0YXR1MSEwHwYDVQQKBHJbnRl\n" \
"cm5ldCBXaWRnaXRzIFB0eSBMdGQwHhcNMTEwOTExMjU0WhcNMjU0WhcNMjU0\n" \
"MjU0WjBFMQswCQYDVQQGEwJBVTEETMBEGA1UECAwKU29tZS1TdGF0ZTEhMB8GA1UE\n" \
"CgwYSW50ZXJuZXQgV2lkZ2l0cyBQdHkgTHRkMIIBIjANBgkqhkiG9w0BAQEFAAO\n" \
"AQ8AMIIBCgKCAQEAO8oThJXSMDo41oL7HTpC4TX8Na1BvnkFw30Av67dl/oZDjVA\n" \
"iXpNzkhVppLnj++/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \
"bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPwo/G4DyW34jOXzZEM\n" \
"FLWvQOQLCKUZogjJBnFdbx8o00wMkYCChbV7gqPE6cw0Zy26Cv1LQiINyonLPbNT\n" \
"c64sS/ZBGPZfOPJmb4tG2nipYgZ1h0/r++jCbWIDAQABMA0GCSqGSIb3DQEBCwU\n" \
"A4IBAQCdq59ubdRY9EiV3bleKXeQ7+8HgBHdm0X9dgq10nD37p00YLyuZLE9NM\n" \
"066G/VcflGrx/Nzw+/UuI7/UuBbBS/3ppHRnsZqBI18nnr/ULrFQy8z3vKtL1q3C\n"

```

```
"DxabjPONlPO2keJeTTA7lN/RCEMwJoa8i0XKXGdu/hQo6x4n+Gq73fEiGCl99xsc\n" \  
"4tIO4yPS4lv+uXBzEUzoEy0CLIKiDesnT5lLeCyPmUNoU89HU95IusZT7kygCHHD\n" \  
"72amlic3X8PKc268KT3ilr3VMhK67C+iIIkfrM5AiU+oOIRrIHSC/p0RigJg3rXA\n" \  
"GBIRHvt+OYF9fDeG7U4QDJNCfGW+\n" \  
"-----END CERTIFICATE-----"  
#define keyCLIENT_PRIVATE_KEY_PEM \  
"-----BEGIN RSA PRIVATE KEY-----\n" \  
"MIIEowIBAAKCAQEAo8oThJXSMDo4l0L7HTpC4TX8NalBvnkFw30Av67dl/oZDjVA\n" \  
"iXpNzkhVppLnj++0/Oed0M7UwNUO2nurQt6yTYrvW7E8ZPjAlC7ueJcGYZhOaVv2\n" \  
"bhSmigjFQru2lw5odSuYy5+22CCgxf58nrRCo5Bk+GwWgZmcrxe/BzutRHQ7X4x\n" \  
"dYJhyhBOi2R1Kt8XsbuWilfgfkVhkhVklFeKqiypdQM6cnPwo/G4DyW34jOXzzEM\n" \  
"FLWvQOQLCKUZogjJBnFdbx8o0OwMkYcChbV7gqPE6cw0Zy26Cv1LQiINyonLPBNT\n" \  
"c64sS/ZBGPZFOPJmb4tG2nipYgZlh0/r++jCbWIDAQABAoIBAQCGR2hC/ZVJhqIM\n" \  
"c2uuJZKpElpIIBBPOObZwwS3IYR4UUjzVgMn7Ubbmxf1LXD8lzfZU4YVp0vTH5lC\n" \  
"07qvYuXpHqtnj+GEok837VYctUY9AuHeDM/2paV3awNV15E1PFG1Jd3pqnH7tJw6\n" \  
"VBZBDiGNnt1agN/UnoSlmfvpU0r8VGPXCbnxe3JY5QyBJPI1wF4LcxRI+eYmr7Ja\n" \  
"/cjn97DZotgz4B7gUNu8XIEkUOTwPabZINY1zcLWiXTMA+8qTniPVk653h14Xqt4\n" \  
"4o4D4YCTpwJcmxSV1m21/6+uyuXr9SIKAE+Ys2cYLA46x+rwLaW5fUoQ5hHa0Ytb\n" \  
"RYJ4SrtBAoGBANwtwLE69N0hq5xDPckSbNGubIeG8P4mBhGkJxIqYoquGLMDiGX\n" \  
"4bltrjr2TPWaxTo3pPavLJiBMIsENA5KU+c/r0jLkxgEp9MIVJrtNgkCiDQqogBG\n" \  
"j4IjL2iQwXoLcQk2tx/dh9Mww+7SETE7EPNrv4UrYaGN5AEvPf5W+NHPAoGBAMQ6\n" \  
"wVa0Mx1PlA4enY2rfe3WXP8bzjleSOWr75JXqG2WbPC0/cszwbyPWOEqRpBZfvD\n" \  
"QFkKx06xp1C09XwiQanr2gDucYXHeEKg/9iuJV1UkMQp95ojlhtSXdRZV7/14pmN\n" \  
"fpB2vcAptX/4gY4tDrWMO08JNnrjE7duC+rmmk1hAoGAS4L0QLCNB/h2JOq+Uuhn\n" \  
"/FGfm0VfFPFrA6D3DbxcxpWUWVWzSLvb0S0phryzxbfEKyau7V5KbDp7ZSU/IC20\n" \  
"KOygyjSEkAkDi7fjrrTRW/Cgg6g6G4YIOBO4qCtHdDbwJMHNdk6096qw5EzS67qLp\n" \  
"Apz5OZ5zChySjri/+HnTxJECgYBySGSP6IJ3fytplTtAshnU5JU2BWpi3ViBoXoE\n" \  
"bndilajWhvJO8dEqBB5OfAcCF0y6TnWt1T8oH2lLHnjcNKlsRw0Dv1lbdloylybx\n" \  
"3da41dRG0sCEtoflMB7nHdDLt/DZDnoKtVvyFG6gfP47utn+Ahgn+Zp6K+46J3eP\n" \  
"s3g8AQKBgE/PJiaF8pbBXaZOuwRRA9GOMSbdIF6+jBYTYp4L9wk4+LZArKtyI+4k\n" \  
"Md2DUvHwMC+ddOtKqjYnLm+V5cSbvU7aPvBZtwxghzTUDcf7EvnA3V/bQBh3R0z7\n" \  
"pVsxTyGRmBSeLdbUWACUbx9LXdpuDarPAJ59daWmP3mBEVmWdzUw\n" \  
"-----END RSA PRIVATE KEY-----"  
const uint8_t g_ip_address[4] = {169, 254, 57, 49};
```

```
const uint8_t g_net_mask[4] = {255, 255, 0, 0};
const uint8_t g_gateway_address[4] = {169, 254, 57, 49};
const uint8_t g_dns_address[4] = {8, 8, 8, 8};
const uint8_t g_mac_address[6] = {0x66, 0x66, 0x66, 0x66, 0x66, 0x66};
static uint8_t g_buffer[SECURE_SOCKETS_EXAMPLE_BUFFER_SIZE];
/*****
*****
* Refer to the following link for detailed API information:
* https://docs.aws.amazon.com/freertos/latest/lib-ref/html2/secure\_sockets/secure\_sockets\_function\_primary.html
*****
*****/
void secure_sockets_ethernet_example (void)
{
    /* Initialize the crypto hardware acceleration. */
    mbedtls_platform_setup(NULL);
    xLoggingTaskInitialize(256, 1, 10); // NOLINT(readability-magic-numbers)
    ProvisioningParams_t params;
    /* Write the keys into a secure region in data flash. */
    params.pucClientPrivateKey      = (uint8_t *) keyCLIENT_PRIVATE_KEY_PEM;
    params.pucClientCertificate     = (uint8_t *) keyCLIENT_CERTIFICATE_PEM;
    params.ulClientPrivateKeyLength = 1 + strlen((const char *)
params.pucClientPrivateKey);
    params.ulClientCertificateLength = 1 + strlen((const char *)
params.pucClientCertificate);
    params.pucJITPCertificate       = NULL;
    params.ulJITPCertificateLength  = 0;
    vAlternateKeyProvisioning(&params);
    /* Start up the network stack. */
    FreeRTOS_IPInit(g_ip_address, g_net_mask, g_gateway_address, g_dns_address,
g_mac_address);
    while (pdFALSE == FreeRTOS_IsNetworkUp())
    {
        vTaskDelay(1);
    }
}
```

```
    }

    Socket_t socket = SOCKETS_Socket(SOCKETS_AF_INET, SOCKETS SOCK_STREAM,
SOCKETS_IPPROTO_TCP);

    if (SOCKETS_INVALID_SOCKET == socket)
    {
        /* Could not create socket. */
        __BKPT(0);
    }

    /* Enable TLS and configure the server certificate. */
    SOCKETS_SetSockOpt(socket, 0, SOCKETS_SO_REQUIRE_TLS, NULL, (size_t) 0);
    SOCKETS_SetSockOpt(socket, 0, SOCKETS_SO_TRUSTED_SERVER_CERTIFICATE,
SERVER_CERTIFICATE_PEM,
sizeof(SERVER_CERTIFICATE_PEM));
    /* Connect to a remote server */
    SocketsSockaddr_t server_addr;

    server_addr.usPort = SOCKETS_htons(9001);
    server_addr.ulAddress = SOCKETS_inet_addr_quick(192, 168, 0, 3);
    if (0 != SOCKETS_Connect(socket, &server_addr, sizeof(server_addr)))
    {
        /* Could not connect to server. */
        __BKPT(0);
    }

    /* Send a message and check that the correct number of bytes were transferred */
    const char msg[] = "hello, world!\n";
    if (sizeof(msg) != SOCKETS_Send(socket, msg, sizeof(msg), 0))
    {
        /* Failed to send data. */
        __BKPT(0);
    }

    if (0 != SOCKETS_Shutdown(socket, SOCKETS_SHUT_RDWR))
    {
        __BKPT(0);
    }

    /* Follow socket shutdown example:
```

```

* https://freertos.org/FreeRTOS-Plus/FreeRTOS_Plus_TCP/API/close.html
*/
while (0 <= SOCKETS_Recv(socket, g_buffer, sizeof(g_buffer), 0))
{
    vTaskDelay(10);
}
SOCKETS_Close(socket);
}
const char * pcApplicationHostnameHook (void)
{
    /* Assign the name "FreeRTOS" to this network node. This function will
    * be called during the DHCP: the machine will be registered with an IP
    * address plus this name. */
    return "FreeRTOS";
}
void vApplicationIPNetworkEventHook (eIPCallbackEvent_t eNetworkEvent)
{
    FSP_PARAMETER_NOT_USED(eNetworkEvent);
}

```

## 4.2.107 ZMOD4XXX Sensor Middleware (rm\_zmod4xxx)

### Modules

### Functions

**fsp\_err\_t** **RM\_ZMOD4XXX\_Open** (rm\_zmod4xxx\_ctrl\_t \*const p\_api\_ctrl, rm\_zmod4xxx\_cfg\_t const \*const p\_cfg)

This function should be called when start a measurement and when measurement data is stale data. Sends the slave address to the zmod4xxx and start a measurement. Implements [rm\\_zmod4xxx\\_api\\_t::open](#). [More...](#)

**fsp\_err\_t** **RM\_ZMOD4XXX\_MeasurementStart** (rm\_zmod4xxx\_ctrl\_t \*const p\_api\_ctrl)

This function should be called when start a measurement. Implements [rm\\_zmod4xxx\\_api\\_t::measurementStart](#). [More...](#)

`fsp_err_t RM_ZMOD4XXX_MeasurementStop (rm_zmod4xxx_ctrl_t *const p_api_ctrl)`

This function should be called when stop a measurement. Implements `rm_zmod4xxx_api_t::measurementStop`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_StatusCheck (rm_zmod4xxx_ctrl_t *const p_api_ctrl)`

This function should be called when polling is used. It reads the status of sensor. Implements `rm_zmod4xxx_api_t::statusCheck`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_Read (rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data)`

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements `rm_zmod4xxx_api_t::read`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_TemperatureAndHumiditySet (rm_zmod4xxx_ctrl_t *const p_api_ctrl, float temperature, float humidity)`

This function is valid only for OAQ\_2nd\_Gen. This function should be called before `DataCalculate`. Humidity and temperature measurements are needed for ambient compensation. Implements `rm_zmod4xxx_api_t::temperatureAndHumiditySet`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_Iaq1stGenDataCalculate (rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_1st_data_t *const p_zmod4xxx_data)`

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements `rm_zmod4xxx_api_t::iaq1stGenDataCalculate`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_Iaq2ndGenDataCalculate (rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_2nd_data_t *const p_zmod4xxx_data)`

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements `rm_zmod4xxx_api_t::iaq2ndGenDataCalculate`. [More...](#)

`fsp_err_t RM_ZMOD4XXX_OdorDataCalculate (rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_odor_data_t *const p_zmod4xxx_data)`

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used.

Implements [rm\\_zmod4xxx\\_api\\_t::odorDataCalculate](#). [More...](#)

`fsp_err_t` [RM\\_ZMOD4XXX\\_SulfurOdorDataCalculate](#) (`rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_sulfur_odor_data_t *const p_zmod4xxx_data`)

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::sulfurOdorDataCalculate](#). [More...](#)

`fsp_err_t` [RM\\_ZMOD4XXX\\_Oaq1stGenDataCalculate](#) (`rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_1st_data_t *const p_zmod4xxx_data`)

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::oaq1stGenDataCalculate](#). [More...](#)

`fsp_err_t` [RM\\_ZMOD4XXX\\_Oaq2ndGenDataCalculate](#) (`rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_2nd_data_t *const p_zmod4xxx_data`)

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::oaq2ndGenDataCalculate](#). [More...](#)

`fsp_err_t` [RM\\_ZMOD4XXX\\_Close](#) (`rm_zmod4xxx_ctrl_t *const p_api_ctrl`)

This function should be called when close the sensor. Implements [rm\\_zmod4xxx\\_api\\_t::close](#). [More...](#)

`void` [rm\\_zmod4xxx\\_comms\\_i2c\\_callback](#) (`rm_comms_callback_args_t *p_args`)

ZMOD4XXX callback function called in the I2C Communications Middleware callback function. [More...](#)

## Detailed Description

Middleware to implement the ZMOD4XXX sensor interface. This module implements the [ZMOD4XXX Middleware Interface](#).

## Overview

This module provides an API for configuring and controlling the ZMOD4XXX sensor. Supported ZMOD4XXX sensors are below.

- ZMOD4410
- ZMOD4510

I2C communication with the ZMOD4XXX sensor is realized by connecting with the rm\_comms\_i2c module.

## Features

The ZMOD4XXX sensor interface implementation has the following key features:

- Initialize the sensor for measurement
- Start a measurement at any time
- Read status register for wait until the measurement is done. This will also be signaled by an interrupt
- Get the ADC data from the sensor
- Input the ADC data and acquire the air quality values by calculation in the library.

## Configuration

RM\_ZMOD4XXX\_CFG\_OPERATION\_MODE is set according to the library selected.

### Build Time Configurations for rm\_zmod4xxx

The following build time configurations are defined in fsp\_cfg/rm\_zmod4xxx\_cfg.h:

Configuration	Options	Default	Description
Parameter Checking	<ul style="list-style-type: none"> <li>• Default (BSP)</li> <li>• Enabled</li> <li>• Disabled</li> </ul>	Default (BSP)	If selected code for parameter checking is included in the build.

### Build Time Configurations for rm\_zmod4410\_iaq\_1st

The following build time configurations are defined in fsp\_cfg/rm\_zmod4xxx\_lib\_cfg.h:

Configuration	Options	Default	Description
Power mode	<ul style="list-style-type: none"> <li>• Continuous</li> <li>• Low Power</li> </ul>	Continuous	Select power mode

### Configurations for Middleware > Sensor > ZMOD4XXX on rm\_zmod4xxx

This module can be added to the Stacks tab via New Stack > Middleware > Sensor > ZMOD4XXX on rm\_zmod4xxx.

Configuration	Options	Default	Description
Name	Manual Entry	g_zmod4xxx_sensor0	Module name.
Comms I2C Callback	Name must be a valid C symbol	zmod4xxx_comms_i2c_callback	A user COMMS I2C callback function can be provided.
IRQ Callback	Name must be a valid C symbol	zmod4xxx_irq_callback	A user IRQ callback function can be

provided.

## Pin Configuration

This module use SDA and SCL pins of I2C Master and SCI I2C.

## Usage Notes

[ZMOD4410 datasheet is here.](#)

The ZMOD4410 has five modes of operation.

Mode	Method	Description
Operation Mode 1	IAQ 1st Generation Continuous	Measurement of UBA levels for IAQ and eCO <sub>2</sub> , provides continuous data
Operation Mode 2	IAQ 1st Generation Low Power	Measurement of UBA levels for IAQ and eCO <sub>2</sub> , fixed sampling interval of 6 seconds
Operation Mode 3	IAQ 2nd Generation	Using AI for improved ppm TVOC, IAQ and eCO <sub>2</sub> functionality (recommended for new designs)
Operation Mode 4	Odor	Control signal based on Air Quality Changes
Operation Mode 5	Sulfur-based Odor Discrimination	The odors in "sulfur" (sulfur based) and "acceptable" (organic based) and shows an intensity level of the smell

[ZMOD4510 datasheet is here.](#)

The ZMOD4510 has two modes of operation.

Mode	Method	Description
Operation Mode 1	OAQ 1st Generation	Measurement of Air Quality
Operation Mode 2	OAQ 2nd Generation	Selective Ozone featuring Ultra-Low Power

A library corresponding to each of these modes is required. By setting in RA Configuration, the library will be generated in the ra/fsp/lib/rm\_zmod4xxx folder of your project.

## Initialization

Initialize with `RM_ZMOD4XXX_Open()`. One channel of timer is required to measure the waiting time at initialization.

## From measurement start to data acquisition

After normal completion, start the measurement with `RM_ZMOD4XXX_MeasurementStart()`. An endless loop continuously checks the status of the ZMOD4XXX sensor and reads its data. The raw

data is subsequently processed, and the air quality values are calculated.

### If IRQ is enabled

1. Call `RM_ZMOD4XXX_MeasurementStart()`.
2. Wait until `RM_ZMOD4XXX_EVENT_MEASUREMENT_COMPLETE` is received via IRQ callback.
3. Call `RM_ZMOD4XXX_Read()`. This function will read the ADC data.
4. Wait until `RM_ZMOD4XXX_EVENT_SUCCESS` is received.
5. Call the DataCalculate API according to the mode.

### If IRQ is disabled

1. Call `RM_ZMOD4XXX_MeasurementStart()`.
2. Wait until `RM_ZMOD4XXX_EVENT_SUCCESS` is received.
3. Call `RM_ZMOD4XXX_StatusCheck()`. This function will execute a status check over I2C.
4. If `RM_ZMOD4XXX_EVENT_MEASUREMENT_NOT_COMPLETE` is received in callback, user should wait some time and then call `RM_ZMOD4XXX_StatusCheck()` again.
5. Wait until `RM_ZMOD4XXX_EVENT_MEASUREMENT_COMPLETE` is received.
6. Call `RM_ZMOD4XXX_Read()` and read the ADC data.
7. Wait until `RM_ZMOD4XXX_EVENT_SUCCESS` is received.
8. Call the DataCalculate API according to the mode.

## Examples

### Basic Example

This is a basic example of minimal use of ZMOD4XXX sensor implementation in an application.

```
void rm_zmod4xxx_basic_example (void)
{
    fsp_err_t          err = FSP_SUCCESS;
    rm_zmod4xxx_raw_data_t g_zmod4xxx_raw_data;
    #if ((RM_ZMOD4XXX_CFG_OPERATION_MODE == 1) || (RM_ZMOD4XXX_CFG_OPERATION_MODE == 2))
        rm_zmod4xxx_iaq_1st_data_t g_zmod4xxx_data;
    #elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 3)
        rm_zmod4xxx_iaq_2nd_data_t g_zmod4xxx_data;
    #elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 4)
        rm_zmod4xxx_odor_data_t g_zmod4xxx_data;
    #elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 5)
        rm_zmod4xxx_sulfur_odor_data_t g_zmod4xxx_data;
    #elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 6)
        rm_zmod4xxx_oaq_1st_data_t g_zmod4xxx_data;
    #elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 7)
        rm_zmod4xxx_oaq_2nd_data_t g_zmod4xxx_data;
```

```
#endif

/* Open the I2C bus if it is not already open. */
rm_comms_i2c_bus_extended_cfg_t * p_extend =
    (rm_comms_i2c_bus_extended_cfg_t *)
g_zmod4xxx_cfg.p_comms_instance->p_cfg->p_extend;
i2c_master_instance_t * p_driver_instance = (i2c_master_instance_t *)
p_extend->p_driver_instance;

p_driver_instance->p_api->open(p_driver_instance->p_ctrl,
p_driver_instance->p_cfg);

do
{
    err = RM_ZMOD4XXX_Open(&g_zmod4xxx_ctrl, &g_zmod4xxx_cfg);
} while ((FSP_ERR_ABORTED == err) || (FSP_ERR_TIMEOUT == err));
/* Handle any errors. This function should be defined by the user. */
handle_error(err);

g_zmod4xxx_callback_flag = 0;
err = RM_ZMOD4XXX_MeasurementStart(&g_zmod4xxx_ctrl);
handle_error(err);

while (0U == g_zmod4xxx_callback_flag)
{
}

while (1)
{
do
{
    g_zmod4xxx_callback_flag = 0;

    err = RM_ZMOD4XXX_Read(&g_zmod4xxx_ctrl, &g_zmod4xxx_raw_data);
if (err == FSP_ERR_SENSOR_MEASUREMENT_NOT_FINISHED)
{
    R_BSP_SoftwareDelay(ZMOD4XXX_WAIT_50, BSP_DELAY_UNITS_MILLISECONDS);
}
} while (err != FSP_SUCCESS);

while (0U == g_zmod4xxx_callback_flag)
{
```

```
    }
#if (RM_ZMOD4XXX_CFG_OPERATION_MODE == 1) || (RM_ZMOD4XXX_CFG_OPERATION_MODE == 2)
    err = RM_ZMOD4XXX_Iaq1stGenDataCalculate(&g_zmod4xxx_ctrl,
&g_zmod4xxx_raw_data, &g_zmod4xxx_data);
#elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 3)
    err = RM_ZMOD4XXX_Iaq2ndGenDataCalculate(&g_zmod4xxx_ctrl,
&g_zmod4xxx_raw_data, &g_zmod4xxx_data);
#elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 4)
    err = RM_ZMOD4XXX_OdorDataCalculate(&g_zmod4xxx_ctrl, &g_zmod4xxx_raw_data,
&g_zmod4xxx_data);
#elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 5)
    err = RM_ZMOD4XXX_SulfurOdorDataCalculate(&g_zmod4xxx_ctrl,
&g_zmod4xxx_raw_data, &g_zmod4xxx_data);
#elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 6)
    err = RM_ZMOD4XXX_Oaq1stGenDataCalculate(&g_zmod4xxx_ctrl,
&g_zmod4xxx_raw_data, &g_zmod4xxx_data);
#elif (RM_ZMOD4XXX_CFG_OPERATION_MODE == 7)
    err = RM_ZMOD4XXX_Oaq2ndGenDataCalculate(&g_zmod4xxx_ctrl,
&g_zmod4xxx_raw_data, &g_zmod4xxx_data);
#endif
if (FSP_SUCCESS == err)
    {
    /* Describe the process by referring to g_zmod4xxx_data */
    }
else if (FSP_ERR_SENSOR_IN_STABILIZATION == err)
    {
    /* Delay required time */
    R_BSP_SoftwareDelay(RM_ZMOD4XXX_ALG_REQ_DELAY_IN_MS, BSP_DELAY_UNITS_MILLISECONDS);
    }
else
    {
    handle_error(err);
    }
}
```

}

## Data Structures

```
struct rm\_zmod4xxx\_init\_process\_params\_t
```

```
struct rm\_zmod4xxx\_instance\_ctrl\_t
```

## Data Structure Documentation

### ◆ [rm\\_zmod4xxx\\_init\\_process\\_params\\_t](#)

struct <a href="#">rm_zmod4xxx_init_process_params_t</a>		
ZMOD4XXX initialization process block		
Data Fields		
volatile uint32_t	<a href="#">delay_ms</a>	Delay milliseconds.
volatile bool	<a href="#">communication_finished</a>	Communication flag for blocking.
volatile bool	<a href="#">measurement_finished</a>	IRQ flag.
volatile <a href="#">rm_zmod4xxx_event_t</a>	<a href="#">event</a>	Callback event.

### ◆ [rm\\_zmod4xxx\\_instance\\_ctrl\\_t](#)

struct <a href="#">rm_zmod4xxx_instance_ctrl_t</a>		
ZMOD4XXX control block		
<b>Data Fields</b>		
uint32_t	<a href="#">open</a>	
		Open flag.
uint8_t	<a href="#">buf</a> [RM_ZMOD4XXX_MAX_I2C_BUF_SIZE]	
		Buffer for I2C communications.
uint8_t	<a href="#">register_address</a>	
		Register address to access.
<a href="#">rm_zmod4xxx_status_params_t</a>	<a href="#">status</a>	
		Status parameter.

volatile rm_zmod4xxx_event_t	event
	Callback event.
rm_zmod4xxx_init_process_params_t	init_process_params
	For the initialization process.
rm_zmod4xxx_cfg_t const *	p_cfg
	Pointer of configuration block.
rm_comms_instance_t const *	p_comms_i2c_instance
	Pointer of I2C Communications Middleware instance structure.
void const *	p_timer_instance
	Pointer to Timer driver instance.
void const *	p_irq_instance
	Pointer to IRQ instance.
void *	p_zmod4xxx_device
	Pointer to ZMOD4XXX device structure.
void *	p_zmod4xxx_handle
	Pointer to ZMOD4XXX library handler.
void *	p_zmod4xxx_results
	Pointer to ZMOD4XXX library results.

float	<a href="#">temperature</a>
	Temperature for OAQ 2nd.
float	<a href="#">humidity</a>
	Humidity for OAQ 2nd.
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.
void(*	<a href="#">p_comms_callback</a> )(rm_zmod4xxx_callback_args_t *p_args)
	I2C Communications callback.
void(*	<a href="#">p_irq_callback</a> )(rm_zmod4xxx_callback_args_t *p_args)
	IRQ callback.

## Function Documentation

### ◆ RM\_ZMOD4XXX\_Open()

```
fsp_err_t RM_ZMOD4XXX_Open ( rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_cfg_t const *const p_cfg )
```

This function should be called when start a measurement and when measurement data is stale data. Sends the slave address to the zmod4xxx and start a measurement. Implements [rm\\_zmod4xxx\\_api\\_t::open](#).

#### Return values

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_ALREADY_OPEN	Module is already open.
FSP_ERR_UNSUPPORTED	Unsupport product ID.
FSP_ERR_TIMEOUT	communication is timeout.
FSP_ERR_ABORTED	communication is aborted.

◆ **RM\_ZMOD4XXX\_MeasurementStart()**

```
fsp_err_t RM_ZMOD4XXX_MeasurementStart ( rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

This function should be called when start a measurement. Implements [rm\\_zmod4xxx\\_api\\_t::measurementStart](#).

**Return values**

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_TIMEOUT	communication is timeout.
FSP_ERR_ABORTED	communication is aborted.

◆ **RM\_ZMOD4XXX\_MeasurementStop()**

```
fsp_err_t RM_ZMOD4XXX_MeasurementStop ( rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

This function should be called when stop a measurement. Implements [rm\\_zmod4xxx\\_api\\_t::measurementStop](#).

**Return values**

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_TIMEOUT	communication is timeout.
FSP_ERR_ABORTED	communication is aborted.

◆ **RM\_ZMOD4XXX\_StatusCheck()**

```
fsp_err_t RM_ZMOD4XXX_StatusCheck ( rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

This function should be called when polling is used. It reads the status of sensor. Implements `rm_zmod4xxx_api_t::statusCheck`.

**Return values**

FSP_SUCCESS	Successfully started.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_TIMEOUT	communication is timeout.
FSP_ERR_ABORTED	communication is aborted.

◆ **RM\_ZMOD4XXX\_Read()**

```
fsp_err_t RM_ZMOD4XXX_Read ( rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements `rm_zmod4xxx_api_t::read`.

**Return values**

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_TIMEOUT	Communication is timeout.
FSP_ERR_ABORTED	Communication is aborted.
FSP_ERR_SENSOR_MEASUREMENT_NOT_FINISHED	Measurement is not finished.

### ◆ RM\_ZMOD4XXX\_TemperatureAndHumiditySet()

```
fsp_err_t RM_ZMOD4XXX_TemperatureAndHumiditySet ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
float temperature, float humidity )
```

This function is valid only for OAQ\_2nd\_Gen. This function should be called before DataCalculate. Humidity and temperature measurements are needed for ambient compensation. Implements [rm\\_zmod4xxx\\_api\\_t::temperatureAndHumiditySet](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.

### ◆ RM\_ZMOD4XXX\_Iaq1stGenDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_Iaq1stGenDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_1st_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::Iaq1stGenDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_Iaq2ndGenDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_Iaq2ndGenDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_2nd_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::iaq2ndGenDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_OdorDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_OdorDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_odor_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::odorDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_SulfurOdorDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_SulfurOdorDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_sulfur_odor_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::sulfurOdorDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_Oaq1stGenDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_Oaq1stGenDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_1st_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::oaq1stGenDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_Oaq2ndGenDataCalculate()

```
fsp_err_t RM_ZMOD4XXX_Oaq2ndGenDataCalculate ( rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_2nd_data_t *const
p_zmod4xxx_data )
```

This function should be called when measurement finishes. To check measurement status either polling or busy/interrupt pin can be used. Implements [rm\\_zmod4xxx\\_api\\_t::oaq2ndGenDataCalculate](#).

#### Return values

FSP_SUCCESS	Successfully results are read.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not opened configured.
FSP_ERR_SENSOR_IN_STABILIZATION	Module is stabilizing.
FSP_ERR_UNSUPPORTED	Operation mode is not supported.

### ◆ RM\_ZMOD4XXX\_Close()

```
fsp_err_t RM_ZMOD4XXX_Close ( rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

This function should be called when close the sensor. Implements [rm\\_zmod4xxx\\_api\\_t::close](#).

#### Return values

FSP_SUCCESS	Successfully closed.
FSP_ERR_ASSERTION	Null pointer passed as a parameter.
FSP_ERR_NOT_OPEN	Module is not open.

### ◆ rm\_zmod4xxx\_comms\_i2c\_callback()

```
void rm_zmod4xxx_comms_i2c_callback ( rm_comms_callback_args_t * p_args)
```

ZMOD4XXX callback function called in the I2C Communications Middleware callback function.  
(end addtogroup ZMOD4XXX)

## 4.3 Interfaces

### Detailed Description

The FSP interfaces provide APIs for common functionality. They can be implemented by one or more modules. Modules can use other modules as dependencies using this interface layer.

## Modules

### ADC Interface

Interface for A/D Converters.

### BLE Interface

Interface for Bluetooth Low Energy functions.

### CAC Interface

Interface for clock frequency accuracy measurements.

### CAN Interface

Interface for CAN peripheral.

### CEC Interface

Interface for CEC peripheral.

### CGC Interface

Interface for clock generation.

### Comparator Interface

Interface for comparators.

### CRC Interface

Interface for cyclic redundancy checking.

### CTSU Interface

Interface for Capacitive Touch Sensing Unit (CTSU) functions.

### DAC Interface

Interface for D/A converters.

### Display Interface

Interface for LCD panel displays.

#### DOC Interface

Interface for the Data Operation Circuit.

#### ELC Interface

Interface for the Event Link Controller.

#### Ethernet Interface

Interface for Ethernet functions.

#### Ethernet PHY Interface

Interface for Ethernet PHY functions.

#### External IRQ Interface

Interface for detecting external interrupts.

#### Flash Interface

Interface for the Flash Memory.

#### I2C Master Interface

Interface for I2C master communication.

#### I2C Slave Interface

Interface for I2C slave communication.

#### I2S Interface

Interface for I2S audio communication.

#### I/O Port Interface

Interface for accessing I/O ports and configuring I/O functionality.

#### JPEG Codec Interface

Interface for JPEG functions.

### Key Matrix Interface

Interface for key matrix functions.

### Low Power Modes Interface

Interface for accessing low power modes.

### Low Voltage Detection Interface

Interface for Low Voltage Detection.

### OPAMP Interface

Interface for Operational Amplifiers.

### PDC Interface

Interface for PDC functions.

### POEG Interface

Interface for the Port Output Enable for GPT.

### PTP Interface

Interface for PTP functions.

### RTC Interface

Interface for accessing the Realtime Clock.

### SD/MMC Interface

Interface for accessing SD, eMMC, and SDIO devices.

### SLCDC Interface

Interface for Segment LCD controllers.

### SPI Interface

Interface for SPI communications.

**SPI Flash Interface**

Interface for accessing external SPI flash devices.

**Three-Phase Interface**

Interface for three-phase timer functions.

**Timer Interface**

Interface for timer functions.

**Transfer Interface**

Interface for data transfer functions.

**UART Interface**

Interface for UART communications.

**USB Interface**

Interface for USB functions.

**USB HCD interface**

Interface for USB HCD functions.

**USB HID Interface**

Interface for USB HID functions.

**USB HMSC Interface**

Interface for USB HMSC functions.

**USB PCDC Interface**

Interface for USB PCDC functions.

**USB PHID Interface**

Interface for USB PHID functions.

**USB PMSC Interface**

Interface for USB PMSC functions.

#### WDT Interface

Interface for watch dog timer functions.

#### ADPCM Decoder Interface

Interface for ADPCM decoder.

#### AUDIO PLAYBACK Interface

Interface for the Audio Playback.

#### BLE ABS Interface

Interface for Bluetooth Low Energy Abstraction functions.

#### Block Media Interface

Interface for block media memory access.

#### Communicatons Middleware Interface

Interface for Communications Middleware functions.

#### FileX Block Media Port Interface

Interface for FileX Block Media port.

#### FreeRTOS+FAT Port Interface

Interface for FreeRTOS+FAT port.

#### HS300X Middleware Interface

Interface for HS300X Middleware functions.

#### LittleFS Interface

Interface for LittleFS access.

#### Motor angle Interface

Interface for motor angle and speed calculation functions.

**Motor Interface**

Interface for Motor functions.

**Motor current Interface**

Interface for motor current functions.

**Motor driver Interface**

Interface for motor driver functions.

**Motor position Interface**

Interface for motor position functions.

**Motor speed Interface**

Interface for motor speed functions.

**Touch Middleware Interface**

Interface for Touch Middleware functions.

**Virtual EEPROM Interface**

Interface for Virtual EEPROM access.

**ZMOD4XXX Middleware Interface**

Interface for ZMOD4XXX Middleware functions.

**SCE Interface**

Interface for Secure Crypto Engine (SCE) functions.

## 4.3.1 ADC Interface

### Interfaces

#### Detailed Description

---

Interface for A/D Converters.

## Summary

The ADC interface provides standard ADC functionality including one-shot mode (single scan), continuous scan and group scan. It also allows configuration of hardware and software triggers for starting scans. After each conversion an interrupt can be triggered, and if a callback function is provided, the call back is invoked with the appropriate event information.

Implemented by: [Analog to Digital Converter \(r\\_adc\)](#)

### Data Structures

struct [adc\\_status\\_t](#)

struct [adc\\_callback\\_args\\_t](#)

struct [adc\\_info\\_t](#)

struct [adc\\_cfg\\_t](#)

struct [adc\\_api\\_t](#)

struct [adc\\_instance\\_t](#)

### Typedefs

typedef void [adc\\_ctrl\\_t](#)

### Enumerations

enum [adc\\_mode\\_t](#)

enum [adc\\_resolution\\_t](#)

enum [adc\\_alignment\\_t](#)

enum [adc\\_trigger\\_t](#)

enum [adc\\_event\\_t](#)

enum [adc\\_channel\\_t](#)

enum [adc\\_state\\_t](#)

### Data Structure Documentation

#### ◆ [adc\\_status\\_t](#)

struct [adc\\_status\\_t](#)

ADC status.		
Data Fields		
<a href="#">adc_state_t</a>	state	Current state.

#### ◆ [adc\\_callback\\_args\\_t](#)

struct <a href="#">adc_callback_args_t</a>		
ADC callback arguments definitions		
Data Fields		
uint16_t	unit	ADC device in use.
<a href="#">adc_event_t</a>	event	ADC callback event.
void const *	p_context	Placeholder for user data.
<a href="#">adc_channel_t</a>	channel	Channel of conversion result. Only valid for ADC_EVENT_CONVERSION_COMPLETE.

#### ◆ [adc\\_info\\_t](#)

struct <a href="#">adc_info_t</a>		
ADC Information Structure for Transfer Interface		
Data Fields		
__l uint16_t *	p_address	The address to start reading the data from.
uint32_t	length	The total number of transfers to read.
<a href="#">transfer_size_t</a>	transfer_size	The size of each transfer.
<a href="#">elc_peripheral_t</a>	elc_peripheral	Name of the peripheral in the ELC list.
<a href="#">elc_event_t</a>	elc_event	Name of the ELC event for the peripheral.
uint32_t	calibration_data	Temperature sensor calibration data (0xFFFFFFFF if unsupported) for reference voltage.
int16_t	slope_microvolts	Temperature sensor slope in microvolts/degrees C.
bool	calibration_ongoing	Calibration is in progress.

#### ◆ [adc\\_cfg\\_t](#)

struct <a href="#">adc_cfg_t</a>		
ADC general configuration		
<b>Data Fields</b>		

<code>uint16_t</code>	<code>unit</code>
	ADC unit to be used.
<code>adc_mode_t</code>	<code>mode</code>
	ADC operation mode.
<code>adc_resolution_t</code>	<code>resolution</code>
	ADC resolution.
<code>adc_alignment_t</code>	<code>alignment</code>
	Specify left or right alignment; ignored if addition used.
<code>adc_trigger_t</code>	<code>trigger</code>
	Default and Group A trigger source.
<code>IRQn_Type</code>	<code>scan_end_irq</code>
	Scan end IRQ number.
<code>IRQn_Type</code>	<code>scan_end_b_irq</code>
	Scan end group B IRQ number.
<code>uint8_t</code>	<code>scan_end_ipl</code>
	Scan end interrupt priority.
<code>uint8_t</code>	<code>scan_end_b_ipl</code>
	Scan end group B interrupt priority.
<code>void(*</code>	<code>p_callback )(adc_callback_args_t *p_args)</code>

	Callback function; set to NULL for none.
void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to the user callback in <a href="#">adc_callback_args_t</a> .
void const *	<a href="#">p_extend</a>
	Extension parameter for hardware specific settings.

#### ◆ [adc\\_api\\_t](#)

struct <a href="#">adc_api_t</a>	
ADC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(adc_ctrl_t *const p_ctrl, <a href="#">adc_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">scanCfg</a> )(adc_ctrl_t *const p_ctrl, void const *const p_extend)
<a href="#">fsp_err_t</a> (*	<a href="#">scanStart</a> )(adc_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">scanStop</a> )(adc_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">scanStatusGet</a> )(adc_ctrl_t *const p_ctrl, <a href="#">adc_status_t</a> *p_status)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(adc_ctrl_t *const p_ctrl, <a href="#">adc_channel_t</a> const reg_id, uint16_t *const p_data)
<a href="#">fsp_err_t</a> (*	<a href="#">read32</a> )(adc_ctrl_t *const p_ctrl, <a href="#">adc_channel_t</a> const reg_id, uint32_t *const p_data)
<a href="#">fsp_err_t</a> (*	<a href="#">calibrate</a> )(adc_ctrl_t *const p_ctrl, void *const p_extend)
<a href="#">fsp_err_t</a> (*	<a href="#">offsetSet</a> )(adc_ctrl_t *const p_ctrl, <a href="#">adc_channel_t</a> const reg_id, int32_t const offset)

<code>fsp_err_t(*</code>	<code>callbackSet )(adc_ctrl_t *const p_api_ctrl, void(*p_callback)(adc_callback_args_t *), void const *const p_context, adc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(adc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(adc_ctrl_t *const p_ctrl, adc_info_t *const p_adc_info)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* adc_api_t::open) (adc_ctrl_t *const p_ctrl, adc_cfg_t const *const p_cfg)`

Initialize ADC Unit; apply power, set the operational mode, trigger sources, interrupt priority, and configurations common to all channels and sensors.

### Implemented as

- `R_ADC_Open()`
- `R_SDADC_Open()`

### Precondition

Configure peripheral clocks, ADC pins and IRQs prior to calling this function.

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control handle structure
[in]	<code>p_cfg</code>	Pointer to configuration structure

## ◆ scanCfg

```
fsp_err_t(* adc_api_t::scanCfg) (adc_ctrl_t *const p_ctrl, void const *const p_extend)
```

Configure the scan including the channels, groups, and scan triggers to be used for the unit that was initialized in the open call. Some configurations are not supported for all implementations. See implementation for details.

**Implemented as**

- R\_ADC\_ScanCfg()
- R\_SDADC\_ScanCfg()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	p_extend	See implementation for details

## ◆ scanStart

```
fsp_err_t(* adc_api_t::scanStart) (adc_ctrl_t *const p_ctrl)
```

Start the scan (in case of a software trigger), or enable the hardware trigger.

**Implemented as**

- R\_ADC\_ScanStart()
- R\_SDADC\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

## ◆ scanStop

```
fsp_err_t(* adc_api_t::scanStop) (adc_ctrl_t *const p_ctrl)
```

Stop the ADC scan (in case of a software trigger), or disable the hardware trigger.

**Implemented as**

- R\_ADC\_ScanStop()
- R\_SDADC\_ScanStop()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **scanStatusGet**

```
fsp_err_t(* adc_api_t::scanStatusGet) (adc_ctrl_t *const p_ctrl, adc_status_t *p_status)
```

Check scan status.

**Implemented as**

- R\_ADC\_StatusGet()
- R\_SDADC\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_status	Pointer to store current status in

◆ **read**

```
fsp_err_t(* adc_api_t::read) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, uint16_t *const p_data)
```

Read ADC conversion result.

**Implemented as**

- R\_ADC\_Read()
- R\_SDADC\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	p_data	Pointer to variable to load value into.

◆ **read32**

```
fsp_err_t(* adc_api_t::read32) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, uint32_t *const p_data)
```

Read ADC conversion result into a 32-bit word.

**Implemented as**

- [R\\_SDADC\\_Read32\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	p_data	Pointer to variable to load value into.

◆ **calibrate**

```
fsp_err_t(* adc_api_t::calibrate) (adc_ctrl_t *const p_ctrl, void *const p_extend)
```

Calibrate ADC or associated PGA (programmable gain amplifier). The driver may require implementation specific arguments to the p\_extend input. Not supported for all implementations. See implementation for details.

**Implemented as**

- [R\\_SDADC\\_Calibrate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	p_extend	Pointer to implementation specific arguments

◆ **offsetSet**

```
fsp_err_t(* adc_api_t::offsetSet) (adc_ctrl_t *const p_ctrl, adc_channel_t const reg_id, int32_t const offset)
```

Set offset for input PGA configured for differential input. Not supported for all implementations. See implementation for details.

**Implemented as**

- R\_SDADC\_OffsetSet()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	reg_id	ADC channel to read (see enumeration adc_channel_t)
[in]	offset	See implementation for details.

◆ **callbackSet**

```
fsp_err_t(* adc_api_t::callbackSet) (adc_ctrl_t *const p_api_ctrl, void(*p_callback)(adc_callback_args_t *), void const *const p_context, adc_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_ADC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the ADC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* adc_api_t::close) (adc_ctrl_t *const p_ctrl)
```

Close the specified ADC unit by ending any scan in progress, disabling interrupts, and removing power to the specified A/D unit.

**Implemented as**

- R\_ADC\_Close()
- R\_SDADC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **infoGet**

```
fsp_err_t(* adc_api_t::infoGet) (adc_ctrl_t *const p_ctrl, adc_info_t *const p_adc_info)
```

Return the ADC data register address of the first (lowest number) channel and the total number of bytes to be read in order for the DTC/DMAC to read the conversion results of all configured channels. Return the temperature sensor calibration and slope data.

**Implemented as**

- R\_ADC\_InfoGet()
- R\_SDADC\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_adc_info	Pointer to ADC information structure

◆ **adc\_instance\_t**

```
struct adc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

adc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
adc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
void const *	p_channel_cfg	Pointer to the channel configuration structure for this instance.
adc_api_t const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `adc_ctrl_t`

```
typedef void adc_ctrl_t
```

ADC control block. Allocate using driver instance control structure from driver instance header file.

## Enumeration Type Documentation

### ◆ `adc_mode_t`

```
enum adc_mode_t
```

ADC operation mode definitions

#### Enumerator

<code>ADC_MODE_SINGLE_SCAN</code>	Single scan - one or more channels.
<code>ADC_MODE_GROUP_SCAN</code>	Two trigger sources to trigger scan for two groups which contain one or more channels.
<code>ADC_MODE_CONTINUOUS_SCAN</code>	Continuous scan - one or more channels.

### ◆ `adc_resolution_t`

```
enum adc_resolution_t
```

ADC data resolution definitions

#### Enumerator

<code>ADC_RESOLUTION_12_BIT</code>	12 bit resolution
<code>ADC_RESOLUTION_10_BIT</code>	10 bit resolution
<code>ADC_RESOLUTION_8_BIT</code>	8 bit resolution
<code>ADC_RESOLUTION_14_BIT</code>	14 bit resolution
<code>ADC_RESOLUTION_16_BIT</code>	16 bit resolution
<code>ADC_RESOLUTION_24_BIT</code>	24 bit resolution

◆ **adc\_alignment\_t**

enum <a href="#">adc_alignment_t</a>	
ADC data alignment definitions	
Enumerator	
ADC_ALIGNMENT_RIGHT	Data alignment right.
ADC_ALIGNMENT_LEFT	Data alignment left.

◆ **adc\_trigger\_t**

enum <a href="#">adc_trigger_t</a>	
ADC trigger mode definitions	
Enumerator	
ADC_TRIGGER_SOFTWARE	Software trigger; not for group modes.
ADC_TRIGGER_SYNC_ELC	Synchronous trigger via ELC.
ADC_TRIGGER_ASYNC_EXTERNAL	External asynchronous trigger; not for group modes.

◆ **adc\_event\_t**

enum <a href="#">adc_event_t</a>	
ADC callback event definitions	
Enumerator	
ADC_EVENT_SCAN_COMPLETE	Normal/Group A scan complete.
ADC_EVENT_SCAN_COMPLETE_GROUP_B	Group B scan complete.
ADC_EVENT_CALIBRATION_COMPLETE	Calibration complete.
ADC_EVENT_CONVERSION_COMPLETE	Conversion complete.

◆ **adc\_channel\_t**

enum <code>adc_channel_t</code>	
ADC channels	
Enumerator	
<code>ADC_CHANNEL_0</code>	ADC channel 0.
<code>ADC_CHANNEL_1</code>	ADC channel 1.
<code>ADC_CHANNEL_2</code>	ADC channel 2.
<code>ADC_CHANNEL_3</code>	ADC channel 3.
<code>ADC_CHANNEL_4</code>	ADC channel 4.
<code>ADC_CHANNEL_5</code>	ADC channel 5.
<code>ADC_CHANNEL_6</code>	ADC channel 6.
<code>ADC_CHANNEL_7</code>	ADC channel 7.
<code>ADC_CHANNEL_8</code>	ADC channel 8.
<code>ADC_CHANNEL_9</code>	ADC channel 9.
<code>ADC_CHANNEL_10</code>	ADC channel 10.
<code>ADC_CHANNEL_11</code>	ADC channel 11.
<code>ADC_CHANNEL_12</code>	ADC channel 12.
<code>ADC_CHANNEL_13</code>	ADC channel 13.
<code>ADC_CHANNEL_14</code>	ADC channel 14.
<code>ADC_CHANNEL_15</code>	ADC channel 15.
<code>ADC_CHANNEL_16</code>	ADC channel 16.
<code>ADC_CHANNEL_17</code>	ADC channel 17.
<code>ADC_CHANNEL_18</code>	ADC channel 18.
<code>ADC_CHANNEL_19</code>	ADC channel 19.
<code>ADC_CHANNEL_20</code>	ADC channel 20.

ADC_CHANNEL_21	ADC channel 21.
ADC_CHANNEL_22	ADC channel 22.
ADC_CHANNEL_23	ADC channel 23.
ADC_CHANNEL_24	ADC channel 24.
ADC_CHANNEL_25	ADC channel 25.
ADC_CHANNEL_26	ADC channel 26.
ADC_CHANNEL_27	ADC channel 27.
ADC_CHANNEL_28	ADC channel 28.
ADC_CHANNEL_DUPLEX_A	Data duplexing register A.
ADC_CHANNEL_DUPLEX_B	Data duplexing register B.
ADC_CHANNEL_DUPLEX	Data duplexing register.
ADC_CHANNEL_TEMPERATURE	Temperature sensor output.
ADC_CHANNEL_VOLT	Internal reference voltage.

#### ◆ adc\_state\_t

enum <code>adc_state_t</code>	
ADC states.	
Enumerator	
ADC_STATE_IDLE	ADC is idle.
ADC_STATE_SCAN_IN_PROGRESS	ADC scan in progress.

## 4.3.2 BLE Interface

### Interfaces

#### Detailed Description

Interface for Bluetooth Low Energy functions.

## Summary

The BLE interface for the Bluetooth Low Energy (BLE) peripheral provides Bluetooth Low Energy functionality.

The Bluetooth Low Energy interface can be implemented by:

- [Bluetooth Low Energy Library \(r\\_ble\)](#)

### Macros

```
#define BLE_VERSION_MAJOR
```

```
#define BLE_VERSION_MINOR
```

```
#define BLE_LIB_EXTENDED
```

```
#define BLE_LIB_BALANCE
```

```
#define BLE_LIB_COMPACT
```

### Macro Definition Documentation

#### ◆ BLE\_VERSION\_MAJOR

```
#define BLE_VERSION_MAJOR
```

BLE Module Major Version.

#### ◆ BLE\_VERSION\_MINOR

```
#define BLE_VERSION_MINOR
```

BLE Module Minor Version.

#### ◆ BLE\_LIB\_EXTENDED

```
#define BLE_LIB_EXTENDED
```

BLE Protocol Stack Library Extended type.

#### ◆ BLE\_LIB\_BALANCE

```
#define BLE_LIB_BALANCE
```

BLE Protocol Stack Library Balance type.

## ◆ BLE\_LIB\_COMPACT

```
#define BLE_LIB_COMPACT
```

BLE Protocol Stack Library Compacity type.

### 4.3.3 CAC Interface

#### Interfaces

#### Detailed Description

Interface for clock frequency accuracy measurements.

## Summary

The interface for the clock frequency accuracy measurement circuit (CAC) peripheral is used to check a system clock frequency with a reference clock signal by counting the number of pulses of the clock to be measured.

Implemented by: [Clock Frequency Accuracy Measurement Circuit \(r\\_cac\)](#)

#### Data Structures

struct [cac\\_ref\\_clock\\_config\\_t](#)

struct [cac\\_meas\\_clock\\_config\\_t](#)

struct [cac\\_callback\\_args\\_t](#)

struct [cac\\_cfg\\_t](#)

struct [cac\\_api\\_t](#)

struct [cac\\_instance\\_t](#)

#### Typedefs

typedef void [cac\\_ctrl\\_t](#)

#### Enumerations

enum [cac\\_event\\_t](#)

enum [cac\\_clock\\_type\\_t](#)

enum [cac\\_clock\\_source\\_t](#)

enum [cac\\_ref\\_divider\\_t](#)enum [cac\\_ref\\_digfilter\\_t](#)enum [cac\\_ref\\_edge\\_t](#)enum [cac\\_meas\\_divider\\_t](#)

## Data Structure Documentation

### ◆ [cac\\_ref\\_clock\\_config\\_t](#)

struct [cac\\_ref\\_clock\\_config\\_t](#)

Structure defining the settings that apply to reference clock configuration.

#### Data Fields

<a href="#">cac_ref_divider_t</a>	divider	Divider specification for the Reference clock.
<a href="#">cac_clock_source_t</a>	clock	Clock source for the Reference clock.
<a href="#">cac_ref_digfilter_t</a>	digfilter	Digital filter selection for the CACREF ext clock.
<a href="#">cac_ref_edge_t</a>	edge	Edge detection for the Reference clock.

### ◆ [cac\\_meas\\_clock\\_config\\_t](#)

struct [cac\\_meas\\_clock\\_config\\_t](#)

Structure defining the settings that apply to measurement clock configuration.

#### Data Fields

<a href="#">cac_meas_divider_t</a>	divider	Divider specification for the Measurement clock.
<a href="#">cac_clock_source_t</a>	clock	Clock source for the Measurement clock.

### ◆ [cac\\_callback\\_args\\_t](#)

struct [cac\\_callback\\_args\\_t](#)

Callback function parameter data

#### Data Fields

<a href="#">cac_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Value provided in configuration structure.

◆ **cac\_cfg\_t**

struct cac_cfg_t	
CAC Configuration	
<b>Data Fields</b>	
<a href="#">cac_ref_clock_config_t</a>	<a href="#">cac_ref_clock</a>
	Reference clock specific settings.
<a href="#">cac_meas_clock_config_t</a>	<a href="#">cac_meas_clock</a>
	Measurement clock specific settings.
<a href="#">uint16_t</a>	<a href="#">cac_upper_limit</a>
	The upper limit counter threshold.
<a href="#">uint16_t</a>	<a href="#">cac_lower_limit</a>
	The lower limit counter threshold.
<a href="#">IRQn_Type</a>	<a href="#">mendi_irq</a>
	Measurement End IRQ number.
<a href="#">IRQn_Type</a>	<a href="#">ovfi_irq</a>
	Measurement Overflow IRQ number.
<a href="#">IRQn_Type</a>	<a href="#">ferri_irq</a>
	Frequency Error IRQ number.
<a href="#">uint8_t</a>	<a href="#">mendi_ipl</a>
	Measurement end interrupt priority.
<a href="#">uint8_t</a>	<a href="#">ovfi_ipl</a>

	Overflow interrupt priority.
uint8_t	<a href="#">ferri_ipl</a>
	Frequency error interrupt priority.
void(*	<a href="#">p_callback</a> )(cac_callback_args_t *p_args)
	Callback provided when a CAC interrupt ISR occurs.
void const *	<a href="#">p_context</a>
	Passed to user callback in <a href="#">cac_callback_args_t</a> .
void const *	<a href="#">p_extend</a>
	CAC hardware dependent configuration */.

#### ◆ cac\_api\_t

struct cac_api_t	
CAC functions implemented at the HAL layer API	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(cac_ctrl_t *const p_ctrl, <a href="#">cac_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">startMeasurement</a> )(cac_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">stopMeasurement</a> )(cac_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )(cac_ctrl_t *const p_api_ctrl, void(*p_callback)(cac_callback_args_t *), void const *const p_context, <a href="#">cac_callback_args_t</a> *const p_callback_memory)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(cac_ctrl_t *const p_ctrl)

## Field Documentation

### ◆ open

```
fsp_err_t(* cac_api_t::open) (cac_ctrl_t *const p_ctrl, cac_cfg_t const *const p_cfg)
```

Open function for CAC device.

#### Parameters

[out]	p_ctrl	Pointer to CAC device control. Must be declared by user.
[in]	cac_cfg_t	Pointer to CAC configuration structure.

### ◆ startMeasurement

```
fsp_err_t(* cac_api_t::startMeasurement) (cac_ctrl_t *const p_ctrl)
```

Begin a measurement for the CAC peripheral.

#### Parameters

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------

### ◆ stopMeasurement

```
fsp_err_t(* cac_api_t::stopMeasurement) (cac_ctrl_t *const p_ctrl)
```

End a measurement for the CAC peripheral.

#### Parameters

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------

## ◆ read

```
fsp_err_t(* cac_api_t::read) (cac_ctrl_t *const p_ctrl, uint16_t *const p_counter)
```

Read function for CAC peripheral.

**Parameters**

[in]	p_ctrl	Control for the CAC device context.
[in]	p_counter	Pointer to variable in which to store the current CACNTBR register contents.

## ◆ callbackSet

```
fsp_err_t(* cac_api_t::callbackSet) (cac_ctrl_t *const p_api_ctrl,
void(*p_callback)(cac_callback_args_t *), void const *const p_context, cac_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CAC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">cac_api_t::open</a> call
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

## ◆ close

```
fsp_err_t(* cac_api_t::close) (cac_ctrl_t *const p_ctrl)
```

Close function for CAC device.

**Parameters**

[in]	p_ctrl	Pointer to CAC device control.
------	--------	--------------------------------

## ◆ cac\_instance\_t

struct cac_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<a href="#">cac_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">cac_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">cac_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [cac\\_ctrl\\_t](#)

typedef void <a href="#">cac_ctrl_t</a>
CAC control block. Allocate an instance specific control block to pass into the CAC API calls.
<b>Implemented as</b>
◦ <a href="#">cac_instance_ctrl_t</a>

## Enumeration Type Documentation

### ◆ [cac\\_event\\_t](#)

enum <a href="#">cac_event_t</a>	
Event types returned by the ISR callback when used in CAC interrupt mode	
Enumerator	
CAC_EVENT_FREQUENCY_ERROR	Frequency error.
CAC_EVENT_MEASUREMENT_COMPLETE	Measurement complete.
CAC_EVENT_COUNTER_OVERFLOW	Counter overflow.

◆ **cac\_clock\_type\_t**

enum <code>cac_clock_type_t</code>	
Enumeration of the two possible clocks.	
Enumerator	
<code>CAC_CLOCK_MEASURED</code>	Measurement clock.
<code>CAC_CLOCK_REFERENCE</code>	Reference clock.

◆ **cac\_clock\_source\_t**

enum <code>cac_clock_source_t</code>	
Enumeration of the possible clock sources for both the reference and measurement clocks.	
Enumerator	
<code>CAC_CLOCK_SOURCE_MAIN_OSC</code>	Main clock oscillator.
<code>CAC_CLOCK_SOURCE_SUBCLOCK</code>	Sub-clock.
<code>CAC_CLOCK_SOURCE_HOCO</code>	HOCO (High speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_MOCO</code>	MOCO (Middle speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_LOCO</code>	LOCO (Low speed on chip oscillator)
<code>CAC_CLOCK_SOURCE_PCLKB</code>	PCLKB (Peripheral Clock B)
<code>CAC_CLOCK_SOURCE_IWDT</code>	IWDT-dedicated on-chip oscillator.
<code>CAC_CLOCK_SOURCE_EXTERNAL</code>	Externally supplied measurement clock on CACREF pin.

◆ **cac\_ref\_divider\_t**

enum <code>cac_ref_divider_t</code>	
Enumeration of available dividers for the reference clock.	
Enumerator	
<code>CAC_REF_DIV_32</code>	Reference clock divided by 32.
<code>CAC_REF_DIV_128</code>	Reference clock divided by 128.
<code>CAC_REF_DIV_1024</code>	Reference clock divided by 1024.
<code>CAC_REF_DIV_8192</code>	Reference clock divided by 8192.

◆ **cac\_ref\_digfilter\_t**

enum <code>cac_ref_digfilter_t</code>	
Enumeration of available digital filter settings for an external reference clock.	
Enumerator	
<code>CAC_REF_DIGITAL_FILTER_OFF</code>	No digital filter on the CACREF pin for reference clock.
<code>CAC_REF_DIGITAL_FILTER_1</code>	Sampling clock for digital filter = measuring frequency.
<code>CAC_REF_DIGITAL_FILTER_4</code>	Sampling clock for digital filter = measuring frequency/4.
<code>CAC_REF_DIGITAL_FILTER_16</code>	Sampling clock for digital filter = measuring frequency/16.

◆ **cac\_ref\_edge\_t**

enum <code>cac_ref_edge_t</code>	
Enumeration of available edge detect settings for the reference clock.	
Enumerator	
<code>CAC_REF_EDGE_RISE</code>	Rising edge detect for the Reference clock.
<code>CAC_REF_EDGE_FALL</code>	Falling edge detect for the Reference clock.
<code>CAC_REF_EDGE_BOTH</code>	Both Rising and Falling edges detect for the Reference clock.

◆ **cac\_meas\_divider\_t**

enum <code>cac_meas_divider_t</code>	
Enumeration of available dividers for the measurement clock	
Enumerator	
<code>CAC_MEAS_DIV_1</code>	Measurement clock divided by 1.
<code>CAC_MEAS_DIV_4</code>	Measurement clock divided by 4.
<code>CAC_MEAS_DIV_8</code>	Measurement clock divided by 8.
<code>CAC_MEAS_DIV_32</code>	Measurement clock divided by 32.

## 4.3.4 CAN Interface

### Interfaces

#### Detailed Description

Interface for CAN peripheral.

## Summary

The CAN interface provides common APIs for CAN HAL drivers. CAN interface supports following features.

- Full-duplex CAN communication
- Generic CAN parameter setting

- Interrupt driven transmit/receive processing
- Callback function support with returning event code
- Hardware resource locking during a transaction

Implemented by:

- [Controller Area Network \(r\\_can\)](#)
- [Controller Area Network - Flexible Data \(r\\_canfd\)](#)

## Data Structures

struct [can\\_info\\_t](#)

struct [can\\_bit\\_timing\\_cfg\\_t](#)

struct [can\\_frame\\_t](#)

struct [can\\_callback\\_args\\_t](#)

struct [can\\_cfg\\_t](#)

struct [can\\_api\\_t](#)

struct [can\\_instance\\_t](#)

## Typedefs

typedef void [can\\_ctrl\\_t](#)

## Enumerations

enum [can\\_event\\_t](#)

enum [can\\_operation\\_mode\\_t](#)

enum [can\\_test\\_mode\\_t](#)

enum [can\\_id\\_mode\\_t](#)

enum [can\\_frame\\_type\\_t](#)

## Data Structure Documentation

### ◆ can\_info\_t

struct can_info_t		
CAN status info		
Data Fields		
uint32_t	status	Useful information from the CAN status register.

uint32_t	rx_mb_status	RX Message Buffer New Data flags.
uint32_t	rx_fifo_status	RX FIFO Empty flags.
uint8_t	error_count_transmit	Transmit error count.
uint8_t	error_count_receive	Receive error count.
uint32_t	error_code	Error code, cleared after reading.

#### ◆ can\_bit\_timing\_cfg\_t

struct can_bit_timing_cfg_t		
CAN bit rate configuration.		
Data Fields		
uint32_t	baud_rate_prescaler	Baud rate prescaler. Valid values: 1 - 1024.
uint32_t	time_segment_1	Time segment 1 control.
uint32_t	time_segment_2	Time segment 2 control.
uint32_t	synchronization_jump_width	Synchronization jump width.

#### ◆ can\_frame\_t

struct can_frame_t		
CAN data Frame		
Data Fields		
uint32_t	id	CAN ID.
<a href="#">can_id_mode_t</a>	id_mode	Standard or Extended ID (IDE).
<a href="#">can_frame_type_t</a>	type	Frame type (RTR).
uint8_t	data_length_code	CAN Data Length Code (DLC).
uint32_t	options	Implementation-specific options.
uint8_t	data[CAN_DATA_BUFFER_LENGTH]	CAN data.

#### ◆ can\_callback\_args\_t

struct can_callback_args_t		
CAN callback parameter definition		
Data Fields		
uint32_t	channel	Device channel number.
<a href="#">can_event_t</a>	event	Event code.
uint32_t	error	Error code.

union <a href="#">can_callback_args_t</a>	<code>__unnamed__</code>	
<a href="#">can_frame_t</a> *	<code>p_frame</code>	
void const *	<code>p_context</code>	Context provided to user during callback.
<a href="#">can_frame_t</a>	<code>frame</code>	Received frame data.

◆ [can\\_cfg\\_t](#)

struct <a href="#">can_cfg_t</a>		
CAN Configuration		
<b>Data Fields</b>		
<code>uint32_t</code>	<a href="#">channel</a>	
		CAN channel.
<a href="#">can_bit_timing_cfg_t</a> *	<a href="#">p_bit_timing</a>	
		CAN bit timing.
<code>void(*</code>	<a href="#">p_callback</a> )( <a href="#">can_callback_args_t</a> * <code>p_args</code> )	
		Pointer to callback function.
<code>void const *</code>	<a href="#">p_context</a>	
		User defined callback context.
<code>void const *</code>	<a href="#">p_extend</a>	
		CAN hardware dependent configuration.
<code>uint8_t</code>	<a href="#">ipl</a>	
		Error/Transmit/Receive interrupt priority.
<code>IRQn_Type</code>	<a href="#">error_irq</a>	
		Error IRQ number.

IRQn_Type	<a href="#">rx_irq</a>
	Receive IRQ number.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit IRQ number.

### ◆ can\_api\_t

struct can_api_t	
Shared Interface definition for CAN	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(can_ctrl_t *const p_ctrl, can_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(can_ctrl_t *const p_ctrl, uint32_t buffer_number, can_frame_t *const p_frame)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(can_ctrl_t *const p_ctrl, uint32_t buffer_number, can_frame_t *const p_frame)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(can_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">modeTransition</a> )(can_ctrl_t *const p_api_ctrl, can_operation_mode_t operation_mode, can_test_mode_t test_mode)
<a href="#">fsp_err_t</a> (*	<a href="#">infoGet</a> )(can_ctrl_t *const p_ctrl, can_info_t *const p_info)
<a href="#">fsp_err_t</a> (*	<a href="#">callbackSet</a> )(can_ctrl_t *const p_api_ctrl, void(*p_callback)(can_callback_args_t *), void const *const p_context, can_callback_args_t *const p_callback_memory)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* can_api_t::open) (can_ctrl_t *const p_ctrl, can_cfg_t const *const p_cfg)
```

Open function for CAN device

**Implemented as**

- R\_CAN\_Open()
- R\_CANFD\_Open()

**Parameters**

[in,out]	p_ctrl	Pointer to the CAN control block. Must be declared by user. Value set here.
[in]	can_cfg_t	Pointer to CAN configuration structure. All elements of this structure must be set by user.

◆ **write**

```
fsp_err_t(* can_api_t::write) (can_ctrl_t *const p_ctrl, uint32_t buffer_number, can_frame_t *const p_frame)
```

Write function for CAN device

**Implemented as**

- R\_CAN\_Write()
- R\_CANFD\_Write()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
[in]	buffer	Buffer number (mailbox or message buffer) to write to.
[in]	p_frame	Pointer for frame of CAN ID, DLC, data and frame type to write.

## ◆ read

```
fsp_err_t(* can_api_t::read) (can_ctrl_t *const p_ctrl, uint32_t buffer_number, can_frame_t *const p_frame)
```

Read function for CAN device

**Implemented as**

- R\_CANFD\_Read()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
[in]	buffer	Message buffer (number) to read from.
[in]	p_frame	Pointer to store the CAN ID, DLC, data and frame type.

## ◆ close

```
fsp_err_t(* can_api_t::close) (can_ctrl_t *const p_ctrl)
```

Close function for CAN device

**Implemented as**

- R\_CAN\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
------	--------	-----------------------------------

## ◆ modeTransition

```
fsp_err_t(* can_api_t::modeTransition) (can_ctrl_t *const p_api_ctrl, can_operation_mode_t operation_mode, can_test_mode_t test_mode)
```

Mode Transition function for CAN device

**Implemented as**

- R\_CAN\_ModeTransition()
- R\_CANFD\_ModeTransition()

**Parameters**

[in]	p_ctrl	Pointer to the CAN control block.
[in]	operation_mode	Destination CAN operation state.
[in]	test_mode	Destination CAN test state.

## ◆ infoGet

```
fsp_err_t(* can_api_t::infoGet) (can_ctrl_t *const p_ctrl, can_info_t *const p_info)
```

Get CAN channel info.

**Implemented as**

- R\_CAN\_InfoGet()
- R\_CANFD\_InfoGet()

**Parameters**

[in]	p_ctrl	Handle for channel (pointer to channel control block)
[out]	p_info	Memory address to return channel specific data to.

## ◆ callbackSet

```
fsp_err_t(* can_api_t::callbackSet) (can_ctrl_t *const p_api_ctrl, void(*p_callback)(can_callback_args_t *), void const *const p_context, can_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CAN\_CallbackSet()
- R\_CANFD\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">can_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

## ◆ can\_instance\_t

```
struct can_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">can_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
------------------------------	--------	---

<code>can_cfg_t</code> const *	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>can_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `can_ctrl_t`

typedef void `can_ctrl_t`

CAN control block. Allocate an instance specific control block to pass into the CAN API calls.

#### Implemented as

- `can_instance_ctrl_t`
- `canfd_instance_ctrl_t`

## Enumeration Type Documentation

◆ **can\_event\_t**

enum <code>can_event_t</code>	
CAN event codes	
Enumerator	
<code>CAN_EVENT_ERR_WARNING</code>	Error Warning event.
<code>CAN_EVENT_ERR_PASSIVE</code>	Error Passive event.
<code>CAN_EVENT_ERR_BUS_OFF</code>	Bus Off event.
<code>CAN_EVENT_BUS_RECOVERY</code>	Bus Off Recovery event.
<code>CAN_EVENT_MAILBOX_MESSAGE_LOST</code>	Mailbox has been overrun.
<code>CAN_EVENT_ERR_BUS_LOCK</code>	Bus lock detected (32 consecutive dominant bits).
<code>CAN_EVENT_ERR_CHANNEL</code>	Channel error has occurred.
<code>CAN_EVENT_TX_ABORTED</code>	Transmit abort event.
<code>CAN_EVENT_RX_COMPLETE</code>	Receive complete event.
<code>CAN_EVENT_TX_COMPLETE</code>	Transmit complete event.
<code>CAN_EVENT_ERR_GLOBAL</code>	Global error has occurred.
<code>CAN_EVENT_TX_FIFO_EMPTY</code>	Transmit FIFO is empty.

◆ **can\_operation\_mode\_t**

enum <code>can_operation_mode_t</code>	
CAN Operation modes	
Enumerator	
<code>CAN_OPERATION_MODE_NORMAL</code>	CAN Normal Operation Mode.
<code>CAN_OPERATION_MODE_RESET</code>	CAN Reset Operation Mode.
<code>CAN_OPERATION_MODE_HALT</code>	CAN Halt Operation Mode.
<code>CAN_OPERATION_MODE_SLEEP</code>	CAN Sleep Operation Mode.

◆ **can\_test\_mode\_t**

enum <code>can_test_mode_t</code>	
CAN Test modes	
Enumerator	
<code>CAN_TEST_MODE_DISABLED</code>	CAN Test Mode Disabled.
<code>CAN_TEST_MODE_LISTEN</code>	CAN Test Listen Mode.
<code>CAN_TEST_MODE_LOOPBACK_EXTERNAL</code>	CAN Test External Loopback Mode.
<code>CAN_TEST_MODE_LOOPBACK_INTERNAL</code>	CAN Test Internal Loopback Mode.
<code>CAN_TEST_MODE_INTERNAL_BUS</code>	CANFD Internal CAN Bus Communication Test Mode.

◆ **can\_id\_mode\_t**

enum <code>can_id_mode_t</code>	
CAN ID modes	
Enumerator	
<code>CAN_ID_MODE_STANDARD</code>	Standard IDs of 11 bits used.
<code>CAN_ID_MODE_EXTENDED</code>	Extended IDs of 29 bits used.

◆ **can\_frame\_type\_t**

enum <code>can_frame_type_t</code>	
CAN frame types	
Enumerator	
<code>CAN_FRAME_TYPE_DATA</code>	Data frame.
<code>CAN_FRAME_TYPE_REMOTE</code>	Remote frame.

**4.3.5 CEC Interface**[Interfaces](#)

## Detailed Description

Interface for CEC peripheral.

## Summary

The CEC interface provides common APIs for CEC HAL drivers and supports the following features:

- Opening and closing the CEC module.
- Allocation for full range of local address settings (TV, Recording Device, Playback Device, etc.)
- Supports a user-callback function (required), invoked when transmit, receive, or error interrupts are received.

Implemented by:

- [Consumer Electronics Control \(r\\_cec\)](#)

## Data Structures

union [cec\\_message\\_t](#)

struct [cec\\_callback\\_args\\_t](#)

struct [cec\\_cfg\\_t](#)

struct [cec\\_api\\_t](#)

struct [cec\\_instance\\_t](#)

## Typedefs

typedef void [cec\\_ctrl\\_t](#)

## Enumerations

enum [cec\\_addr\\_t](#)

enum [cec\\_clock\\_source\\_t](#)

enum [cec\\_state\\_t](#)

enum [cec\\_error\\_t](#)

enum [cec\\_event\\_t](#)

## Data Structure Documentation

### ◆ [cec\\_message\\_t](#)

union [cec\\_message\\_t](#)

CEC message		
Data Fields		
struct <a href="#">cec_message_t</a>	<code>__unnamed__</code>	
uint8_t	<code>raw_data[CEC_DATA_BUFFER_LENGTH+2 *sizeof(uint8_t)]</code>	Contiguous raw data.

◆ **cec\_callback\_args\_t**

struct <a href="#">cec_callback_args_t</a>		
CEC callback parameter definition		
Data Fields		
<a href="#">cec_event_t</a>	<code>event</code>	Event code.
<code>void const *</code>	<code>p_context</code>	Context provided to user during callback.
<code>bool</code>	<code>addr_match</code>	Local address matches message destination.
uint8_t	<code>data_byte</code>	Received data byte (INTDA)
<a href="#">cec_status_t</a>	<code>status</code>	CEC Module status data.
<a href="#">cec_error_t</a>	<code>errors</code>	Error code bitfield.

◆ **cec\_cfg\_t**

struct <a href="#">cec_cfg_t</a>		
CEC Configuration		
<b>Data Fields</b>		
<code>cec_timing_t const *</code>	<a href="#">bit_timing_cfg</a>	
		CEC Bit Timing Configuration.
<code>uint16_t</code>	<a href="#">rx_data_sample_time</a>	
		Receive Data Sample Time Setting.
<code>uint16_t</code>	<a href="#">rx_data_bit_reference_width</a>	
		Receive Data Bit Reference Width.
<code>void(*</code>	<code>p_callback)(<a href="#">cec_callback_args_t</a> *p_args)</code>	
		Pointer to callback function.

void const *	<a href="#">p_context</a>
	User defined callback context.
uint8_t	<a href="#">ipl</a>
	Error/Data/Message interrupt priority level.
IRQn_Type	<a href="#">error_irq</a>
	Error IRQ number.
IRQn_Type	<a href="#">data_irq</a>
	Data IRQ number.
IRQn_Type	<a href="#">msg_irq</a>
	Communication Complete IRQ number.
void *	<a href="#">p_extend</a>
	Pointer to extended configuration structure.

◆ **cec\_api\_t**

struct cec_api_t	
Shared Interface definition for CEC	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">cec_ctrl_t</a> *const p_ctrl, <a href="#">cec_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">medialnit</a> )( <a href="#">cec_ctrl_t</a> *const p_ctrl, <a href="#">cec_addr_t</a> local_address)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )( <a href="#">cec_ctrl_t</a> *const p_ctrl, <a href="#">cec_message_t</a> const *const p_message, uint32_t message_size)

<code>fsp_err_t(*</code>	<code>close )(cec_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(cec_ctrl_t *const p_ctrl, cec_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(cec_ctrl_t *const p_ctrl, void(*p_callback)(cec_callback_args_t *), void const *const p_context, cec_callback_args_t *const p_callback_memory)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* cec_api_t::open) (cec_ctrl_t *const p_ctrl, cec_cfg_t const *const p_cfg)`

Open function for CEC device

#### Implemented as

- `R_CEC_Open()`

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to the CEC control block. Must be declared by user. Value set here.
[in]	<code>p_cfg</code>	Pointer to CEC configuration structure. All elements of this structure must be set by user.

### ◆ medialnit

`fsp_err_t(* cec_api_t::medialnit) (cec_ctrl_t *const p_ctrl, cec_addr_t local_address)`

Initializes the CEC device. May be called any time after the CEC module has been opened. This API blocks until the device initialization procedure is complete.

#### Implemented as

- `R_CEC_Medialnit()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to CEC instance control block.
[out]	<code>local_address</code>	Desired Logical address for local device.

## ◆ write

```
fsp_err_t(* cec_api_t::write) (cec_ctrl_t *const p_ctrl, cec_message_t const *const p_message,
uint32_t message_size)
```

Write function for CEC device

**Implemented as**

- R\_CEC\_Write()

**Parameters**

[in]	p_ctrl	Pointer to CEC instance control block
[in]	p_message	Message data
[in]	message_size	Total size of entire message

## ◆ close

```
fsp_err_t(* cec_api_t::close) (cec_ctrl_t *const p_ctrl)
```

Close function for CEC device

**Implemented as**

- R\_CEC\_Close()

**Parameters**

[in]	p_ctrl	Pointer to CEC instance control block
[out]	p_message	Message data

## ◆ statusGet

```
fsp_err_t(* cec_api_t::statusGet) (cec_ctrl_t *const p_ctrl, cec_status_t *const p_status)
```

Get CEC channel info.

**Implemented as**

- R\_CEC\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to CEC instance control block
[out]	p_status	Memory address to return channel specific data to.

◆ **callbackSet**

```
fsp_err_t(* cec_api_t::callbackSet) (cec_ctrl_t *const p_ctrl, void(*p_callback)(cec_callback_args_t *),
void const *const p_context, cec_callback_args_t *const p_callback_memory)
```

Specify callback function, optional context pointer and working memory pointer.

**Implemented as**

- R\_CEC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">cec_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_callback_memory	Pointer to volatile memory where callback structure cec be allocated. Callback arguments allocated here are only valid during the callback.

◆ **cec\_instance\_t**

```
struct cec_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">cec_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">cec_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">cec_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **cec\_ctrl\_t**

```
typedef void cec_ctrl_t
```

CEC control block. Allocate an instance specific control block to pass into the CEC API calls.

**Implemented as**

- [cec\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ cec\_addr\_t

enum cec_addr_t	
CEC Addresses	
Enumerator	
CEC_ADDR_TV	CEC Address for TV.
CEC_ADDR_RECORDING_DEVICE_1	CEC Address for Recording Device 1.
CEC_ADDR_RECORDING_DEVICE_2	CEC Address for Recording Device 2.
CEC_ADDR_TUNER_1	CEC Address for Tuner 1.
CEC_ADDR_PLAYBACK_DEVICE_1	CEC Address for Playback Device 1.
CEC_ADDR_AUDIO_SYSTEM	CEC Address for Audio System.
CEC_ADDR_TUNER_2	CEC Address for Tuner 2.
CEC_ADDR_TUNER_3	CEC Address for Tuner 3.
CEC_ADDR_PLAYBACK_DEVICE_2	CEC Address for Playback Device 2.
CEC_ADDR_RECORDING_DEVICE_3	CEC Address for Recording Device 3.
CEC_ADDR_TUNER_4	CEC Address for Tuner 4.
CEC_ADDR_PLAYBACK_DEVICE_3	CEC Address for Playback Device 3.
CEC_ADDR_SPECIFIC_USE	CEC Address for Specific Use.
CEC_ADDR_UNREGISTERED	CEC Address for Unregistered Devices.
CEC_ADDR_BROADCAST	CEC Broadcast message.

◆ **cec\_clock\_source\_t**

enum <code>cec_clock_source_t</code>	
CEC Source Clock	
Enumerator	
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_32</code>	PCLKB / 32 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_64</code>	PCLKB / 64 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_128</code>	PCLKB / 128 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_256</code>	PCLKB / 256 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_512</code>	PCLKB / 512 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_PCLKB_DIV_1024</code>	PCLKB / 1024 is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_CECCLK</code>	CECCLK is the source of the CEC Clock.
<code>CEC_CLOCK_SOURCE_CECCLK_DIV_256</code>	CECCLK / 256 is the source of the CEC Clock.

◆ **cec\_state\_t**

enum <code>cec_state_t</code>	
CEC State	
Enumerator	
<code>CEC_STATE_UNINIT</code>	Module requires initialization.
<code>CEC_STATE_READY</code>	Module ready for operation.
<code>CEC_STATE_TX_ACTIVE</code>	Transmit in progress, either direct or broadcast.
<code>CEC_STATE_RX_ACTIVE</code>	Receive in progress, either direct or broadcast.
<code>CEC_STATE_BUSY</code>	CEC Signal Free Time has not yet elapsed.

◆ **cec\_error\_t**

enum <code>cec_error_t</code>	
CEC Error Code	
Enumerator	
<code>CEC_ERROR_NONE</code>	No errors currently active.
<code>CEC_ERROR_OERR</code>	Overrun error.
<code>CEC_ERROR_UERR</code>	Unterrun Error.
<code>CEC_ERROR_ACKERR</code>	ACK Error.
<code>CEC_ERROR_TERR</code>	Timing Error.
<code>CEC_ERROR_TXERR</code>	Transmission Error.
<code>CEC_ERROR_AERR</code>	Bus arbitration Loss.
<code>CEC_ERROR_BLERR</code>	Bus lock error.
<code>CEC_ERROR_ADDR</code>	Address allocation error.

◆ **cec\_event\_t**

enum <code>cec_event_t</code>	
CEC event codes	
Enumerator	
<code>CEC_EVENT_RX_DATA</code>	Receive Data byte event.
<code>CEC_EVENT_RX_COMPLETE</code>	Receive complete event.
<code>CEC_EVENT_TX_COMPLETE</code>	Transmit complete event.
<code>CEC_EVENT_READY</code>	CEC Address allocated and module is now ready.
<code>CEC_EVENT_ERR</code>	Error has occurred.

**4.3.6 CGC Interface**

## Interfaces

### Detailed Description

---

Interface for clock generation.

## Summary

The CGC interface provides the ability to configure and use all of the CGC module's capabilities. Among the capabilities is the selection of several clock sources to use as the system clock source. Additionally, the system clocks can be divided down to provide a wide range of frequencies for various system and peripheral needs.

Clock stability can be checked and clocks may also be stopped to save power when not needed. The API has a function to return the frequency of the system and system peripheral clocks at run time. There is also a feature to detect when the main oscillator has stopped, with the option of calling a user provided callback function.

The CGC interface is implemented by:

- [Clock Generation Circuit \(r\\_cgc\)](#)

### Data Structures

---

struct [cgc\\_callback\\_args\\_t](#)

struct [cgc\\_pll\\_cfg\\_t](#)

union [cgc\\_divider\\_cfg\\_t](#)

struct [cgc\\_cfg\\_t](#)

struct [cgc\\_clocks\\_cfg\\_t](#)

struct [cgc\\_api\\_t](#)

struct [cgc\\_instance\\_t](#)

### Typedefs

---

typedef void [cgc\\_ctrl\\_t](#)

### Enumerations

---

enum [cgc\\_event\\_t](#)

enum [cgc\\_clock\\_t](#)

enum [cgc\\_pll\\_div\\_t](#)

enum [cgc\\_pll\\_mul\\_t](#)

enum [cgc\\_sys\\_clock\\_div\\_t](#)enum [cgc\\_usb\\_clock\\_div\\_t](#)enum [cgc\\_clock\\_change\\_t](#)

## Data Structure Documentation

### ◆ [cgc\\_callback\\_args\\_t](#)

struct <a href="#">cgc_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">cgc_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

### ◆ [cgc\\_pll\\_cfg\\_t](#)

struct <a href="#">cgc_pll_cfg_t</a>		
Clock configuration structure - Used as an input parameter to the <a href="#">cgc_api_t::clockStart</a> function for the PLL clock.		
Data Fields		
<a href="#">cgc_clock_t</a>	source_clock	PLL source clock (main oscillator or HOCO)
<a href="#">cgc_pll_div_t</a>	divider	PLL divider.
<a href="#">cgc_pll_mul_t</a>	multiplier	PLL multiplier.

### ◆ [cgc\\_divider\\_cfg\\_t](#)

union <a href="#">cgc_divider_cfg_t</a>		
Clock configuration structure - Used as an input parameter to the <a href="#">cgc_api_t::systemClockSet</a> and <a href="#">cgc_api_t::systemClockGet</a> functions.		
Data Fields		
uint32_t	sckdivcr_w	(@ 0x4001E020) System clock Division control register
struct <a href="#">cgc_divider_cfg_t</a>	__unnamed__	

### ◆ [cgc\\_cfg\\_t](#)

struct <a href="#">cgc_cfg_t</a>		
Configuration options.		

◆ **cgc\_clocks\_cfg\_t**

struct cgc_clocks_cfg_t		
Clock configuration		
Data Fields		
cgc_clock_t	system_clock	System clock source enumeration.
cgc_pll_cfg_t	pll_cfg	PLL configuration structure.
cgc_pll_cfg_t	pll2_cfg	PLL2 configuration structure.
cgc_divider_cfg_t	divider_cfg	Clock dividers structure.
cgc_clock_change_t	loco_state	State of LOCO.
cgc_clock_change_t	moco_state	State of MOCO.
cgc_clock_change_t	hoco_state	State of HOCO.
cgc_clock_change_t	mainosc_state	State of Main oscillator.
cgc_clock_change_t	pll_state	State of PLL.
cgc_clock_change_t	pll2_state	State of PLL2.

◆ **cgc\_api\_t**

struct cgc_api_t	
CGC functions implemented at the HAL layer follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg)
fsp_err_t(*)	clocksCfg )(cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg)
fsp_err_t(*)	clockStart )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg)
fsp_err_t(*)	clockStop )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
fsp_err_t(*)	clockCheck )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
fsp_err_t(*)	systemClockSet )(cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)
fsp_err_t(*)	systemClockGet )(cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source, cgc_divider_cfg_t *const p_divider_cfg)

<code>fsp_err_t(*</code>	<code>oscStopDetectEnable )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>oscStopDetectDisable )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>oscStopStatusClear )(cgc_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(cgc_ctrl_t *const p_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* cgc_api_t::open) (cgc_ctrl_t *const p_ctrl, cgc_cfg_t const *const p_cfg)`

Initial configuration

### Implemented as

- `R_CGC_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to instance control block
[in]	<code>p_cfg</code>	Pointer to configuration

◆ **clocksCfg**

```
fsp_err_t(* cgc_api_t::clocksCfg) (cgc_ctrl_t *const p_ctrl, cgc_clocks_cfg_t const *const p_clock_cfg)
```

Configure all system clocks.

**Implemented as**

- R\_CGC\_ClocksCfg()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	p_clock_cfg	Pointer to desired configuration of system clocks

◆ **clockStart**

```
fsp_err_t(* cgc_api_t::clockStart) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_pll_cfg_t const *const p_pll_cfg)
```

Start a clock.

**Implemented as**

- R\_CGC\_ClockStart()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Clock source to start
[in]	p_pll_cfg	Pointer to PLL configuration, can be NULL if clock_source is not CGC_CLOCK_PLL or CGC_CLOCK_PLL2

◆ **clockStop**

```
fsp_err_t(* cgc_api_t::clockStop) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
```

Stop a clock.

**Implemented as**

- R\_CGC\_ClockStop()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	The clock source to stop

◆ **clockCheck**

```
fsp_err_t(* cgc_api_t::clockCheck) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source)
```

Check the stability of the selected clock.

**Implemented as**

- R\_CGC\_ClockCheck()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Which clock source to check for stability

◆ **systemClockSet**

```
fsp_err_t(* cgc_api_t::systemClockSet) (cgc_ctrl_t *const p_ctrl, cgc_clock_t clock_source, cgc_divider_cfg_t const *const p_divider_cfg)
```

Set the system clock.

**Implemented as**

- R\_CGC\_SystemClockSet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	clock_source	Clock source to set as system clock
[in]	p_divider_cfg	Pointer to the clock divider configuration

### ◆ systemClockGet

```
fsp_err_t(* cgc_api_t::systemClockGet) (cgc_ctrl_t *const p_ctrl, cgc_clock_t *const p_clock_source,
cgc_divider_cfg_t *const p_divider_cfg)
```

Get the system clock information.

#### Implemented as

- R\_CGC\_SystemClockGet()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[out]	p_clock_source	Returns the current system clock
[out]	p_divider_cfg	Returns the current system clock dividers

### ◆ oscStopDetectEnable

```
fsp_err_t(* cgc_api_t::oscStopDetectEnable) (cgc_ctrl_t *const p_ctrl)
```

Enable and optionally register a callback for Main Oscillator stop detection.

#### Implemented as

- R\_CGC\_OscStopDetectEnable()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	p_callback	Callback function that will be called by the NMI interrupt when an oscillation stop is detected. If the second argument is "false", then this argument can be NULL.
[in]	enable	Enable/disable Oscillation Stop Detection

◆ **oscStopDetectDisable**

```
fsp_err_t(* cgc_api_t::oscStopDetectDisable) (cgc_ctrl_t *const p_ctrl)
```

Disable Main Oscillator stop detection.

**Implemented as**

- [R\\_CGC\\_OscStopDetectDisable\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **oscStopStatusClear**

```
fsp_err_t(* cgc_api_t::oscStopStatusClear) (cgc_ctrl_t *const p_ctrl)
```

Clear the oscillator stop detection flag.

**Implemented as**

- [R\\_CGC\\_OscStopStatusClear\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **callbackSet**

```
fsp_err_t(* cgc_api_t::callbackSet) (cgc_ctrl_t *const p_api_ctrl, void(*p_callback)(cgc_callback_args_t *), void const *const p_context, cgc_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_CGC\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the CGC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* cgc_api_t::close) (cgc_ctrl_t *const p_ctrl)
```

Close the CGC driver.

**Implemented as**

- [R\\_CGC\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **cgc\_instance\_t**

```
struct cgc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">cgc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">cgc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">cgc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **cgc\_ctrl\_t**

```
typedef void cgc_ctrl_t
```

CGC control block. Allocate an instance specific control block to pass into the CGC API calls.

**Implemented as**

- [cgc\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **cgc\_event\_t**

enum <code>cgc_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>CGC_EVENT_OSC_STOP_DETECT</code>	Oscillator stop detection has caused the event.

◆ **cgc\_clock\_t**

enum <code>cgc_clock_t</code>	
System clock source identifiers - The source of ICLK, BCLK, FCLK, PCLKS A-D and UCLK prior to the system clock divider	
Enumerator	
<code>CGC_CLOCK_HOCO</code>	The high speed on chip oscillator.
<code>CGC_CLOCK_MOCO</code>	The middle speed on chip oscillator.
<code>CGC_CLOCK_LOCO</code>	The low speed on chip oscillator.
<code>CGC_CLOCK_MAIN_OSC</code>	The main oscillator.
<code>CGC_CLOCK_SUBCLOCK</code>	The subclock oscillator.
<code>CGC_CLOCK_PLL</code>	The PLL oscillator.
<code>CGC_CLOCK_PLL2</code>	The PLL2 oscillator.

◆ **cgc\_pll\_div\_t**

enum <code>cgc_pll_div_t</code>	
PLL divider values	
Enumerator	
<code>CGC_PLL_DIV_1</code>	PLL divider of 1.
<code>CGC_PLL_DIV_2</code>	PLL divider of 2.
<code>CGC_PLL_DIV_3</code>	PLL divider of 3 (S7, S5 only)
<code>CGC_PLL_DIV_4</code>	PLL divider of 4 (S3 only)

◆ **cgc\_pll\_mul\_t**

enum <code>cgc_pll_mul_t</code>	
PLL multiplier values	
Enumerator	
<code>CGC_PLL_MUL_8_0</code>	PLL multiplier of 8.0.
<code>CGC_PLL_MUL_9_0</code>	PLL multiplier of 9.0.
<code>CGC_PLL_MUL_10_0</code>	PLL multiplier of 10.0.
<code>CGC_PLL_MUL_10_5</code>	PLL multiplier of 10.5.
<code>CGC_PLL_MUL_11_0</code>	PLL multiplier of 11.0.
<code>CGC_PLL_MUL_11_5</code>	PLL multiplier of 11.5.
<code>CGC_PLL_MUL_12_0</code>	PLL multiplier of 12.0.
<code>CGC_PLL_MUL_12_5</code>	PLL multiplier of 12.5.
<code>CGC_PLL_MUL_13_0</code>	PLL multiplier of 13.0.
<code>CGC_PLL_MUL_13_5</code>	PLL multiplier of 13.5.
<code>CGC_PLL_MUL_14_0</code>	PLL multiplier of 14.0.
<code>CGC_PLL_MUL_14_5</code>	PLL multiplier of 14.5.
<code>CGC_PLL_MUL_15_0</code>	PLL multiplier of 15.0.
<code>CGC_PLL_MUL_15_5</code>	PLL multiplier of 15.5.
<code>CGC_PLL_MUL_16_0</code>	PLL multiplier of 16.0.
<code>CGC_PLL_MUL_16_5</code>	PLL multiplier of 16.5.
<code>CGC_PLL_MUL_17_0</code>	PLL multiplier of 17.0.
<code>CGC_PLL_MUL_17_5</code>	PLL multiplier of 17.5.
<code>CGC_PLL_MUL_18_0</code>	PLL multiplier of 18.0.
<code>CGC_PLL_MUL_18_5</code>	PLL multiplier of 18.5.
<code>CGC_PLL_MUL_19_0</code>	PLL multiplier of 19.0.

CGC_PLL_MUL_19_5	PLL multiplier of 19.5.
CGC_PLL_MUL_20_0	PLL multiplier of 20.0.
CGC_PLL_MUL_20_5	PLL multiplier of 20.5.
CGC_PLL_MUL_21_0	PLL multiplier of 21.0.
CGC_PLL_MUL_21_5	PLL multiplier of 21.5.
CGC_PLL_MUL_22_0	PLL multiplier of 22.0.
CGC_PLL_MUL_22_5	PLL multiplier of 22.5.
CGC_PLL_MUL_23_0	PLL multiplier of 23.0.
CGC_PLL_MUL_23_5	PLL multiplier of 23.5.
CGC_PLL_MUL_24_0	PLL multiplier of 24.0.
CGC_PLL_MUL_24_5	PLL multiplier of 24.5.
CGC_PLL_MUL_25_0	PLL multiplier of 25.0.
CGC_PLL_MUL_25_5	PLL multiplier of 25.5.
CGC_PLL_MUL_26_0	PLL multiplier of 26.0.
CGC_PLL_MUL_26_5	PLL multiplier of 26.5.
CGC_PLL_MUL_27_0	PLL multiplier of 27.0.
CGC_PLL_MUL_27_5	PLL multiplier of 27.5.
CGC_PLL_MUL_28_0	PLL multiplier of 28.0.
CGC_PLL_MUL_28_5	PLL multiplier of 28.5.
CGC_PLL_MUL_29_0	PLL multiplier of 29.0.
CGC_PLL_MUL_29_5	PLL multiplier of 29.5.
CGC_PLL_MUL_30_0	PLL multiplier of 30.0.
CGC_PLL_MUL_31_0	PLL multiplier of 31.0.

◆ **cgc\_sys\_clock\_div\_t**

enum <code>cgc_sys_clock_div_t</code>	
System clock divider values - The individually selectable divider of each of the system clocks, ICLK, BCLK, FCLK, PCLKS A-D.	
Enumerator	
<code>CGC_SYS_CLOCK_DIV_1</code>	System clock divided by 1.
<code>CGC_SYS_CLOCK_DIV_2</code>	System clock divided by 2.
<code>CGC_SYS_CLOCK_DIV_4</code>	System clock divided by 4.
<code>CGC_SYS_CLOCK_DIV_8</code>	System clock divided by 8.
<code>CGC_SYS_CLOCK_DIV_16</code>	System clock divided by 16.
<code>CGC_SYS_CLOCK_DIV_32</code>	System clock divided by 32.
<code>CGC_SYS_CLOCK_DIV_64</code>	System clock divided by 64.

◆ **cgc\_usb\_clock\_div\_t**

enum <code>cgc_usb_clock_div_t</code>	
USB clock divider values	
Enumerator	
<code>CGC_USB_CLOCK_DIV_3</code>	Divide USB source clock by 3.
<code>CGC_USB_CLOCK_DIV_4</code>	Divide USB source clock by 4.
<code>CGC_USB_CLOCK_DIV_5</code>	Divide USB source clock by 5.

◆ **cgc\_clock\_change\_t**

enum <code>cgc_clock_change_t</code>	
Clock options	
Enumerator	
<code>CGC_CLOCK_CHANGE_START</code>	Start the clock.
<code>CGC_CLOCK_CHANGE_STOP</code>	Stop the clock.
<code>CGC_CLOCK_CHANGE_NONE</code>	No change to the clock.

**4.3.7 Comparator Interface**[Interfaces](#)**Detailed Description**

Interface for comparators.

**Summary**

The comparator interface provides standard comparator functionality, including generating an event when the comparator result changes.

Implemented by:

- [High-Speed Analog Comparator \(r\\_acmphs\)](#)
- [Low-Power Analog Comparator \(r\\_acmplp\)](#)

**Data Structures**

struct [comparator\\_info\\_t](#)

struct [comparator\\_status\\_t](#)

struct [comparator\\_callback\\_args\\_t](#)

struct [comparator\\_cfg\\_t](#)

struct [comparator\\_api\\_t](#)

struct [comparator\\_instance\\_t](#)

**Typedefs**

```
typedef void comparator_ctrl_t
```

## Enumerations

```
enum comparator_mode_t
```

```
enum comparator_trigger_t
```

```
enum comparator_polarity_invert_t
```

```
enum comparator_pin_output_t
```

```
enum comparator_filter_t
```

```
enum comparator_state_t
```

## Data Structure Documentation

### ◆ comparator\_info\_t

struct comparator_info_t		
Comparator information.		
Data Fields		
uint32_t	min_stabilization_wait_us	Minimum stabilization wait time in microseconds.

### ◆ comparator\_status\_t

struct comparator_status_t		
Comparator status.		
Data Fields		
comparator_state_t	state	Current comparator state.

### ◆ comparator\_callback\_args\_t

struct comparator_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">comparator_api_t::open</a> function in <a href="#">comparator_cfg_t</a> .
uint32_t	channel	The physical hardware channel that caused the interrupt.

### ◆ comparator\_cfg\_t

struct comparator_cfg_t		
-------------------------	--	--

User configuration structure, used in open function

### Data Fields

uint8_t	channel
	Hardware channel used.
comparator_mode_t	mode
	Normal or window mode.
comparator_trigger_t	trigger
	Trigger setting.
comparator_filter_t	filter
	Digital filter clock divisor setting.
comparator_polarity_invert_t	invert
	Whether to invert output.
comparator_pin_output_t	pin_output
	Whether to include output on output pin.
uint8_t	vref_select
	Internal Vref Select.
uint8_t	ipl
	Interrupt priority.
IRQn_Type	irq
	NVIC interrupt number.

void(*	<a href="#">p_callback</a> )(comparator_callback_args_t *p_args)
void const *	<a href="#">p_context</a>
void const *	<a href="#">p_extend</a>
	Comparator hardware dependent configuration.

## Field Documentation

### ◆ [p\\_callback](#)

void(\* comparator\_cfg\_t::p\_callback) ([comparator\\_callback\\_args\\_t](#) \*p\_args)

Callback called when comparator event occurs.

### ◆ [p\\_context](#)

void const\* comparator\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in [comparator\\_callback\\_args\\_t](#).

### ◆ [comparator\\_api\\_t](#)

struct comparator\_api\_t

Comparator functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(comparator_ctrl_t *const p_ctrl, <a href="#">comparator_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">outputEnable</a> )(comparator_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">infoGet</a> )(comparator_ctrl_t *const p_ctrl, <a href="#">comparator_info_t</a> *const p_info)
<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )(comparator_ctrl_t *const p_ctrl, <a href="#">comparator_status_t</a> *const p_status)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(comparator_ctrl_t *const p_ctrl)

## Field Documentation

◆ **open**

```
fsp_err_t(* comparator_api_t::open) (comparator_ctrl_t *const p_ctrl, comparator_cfg_t const *const p_cfg)
```

Initialize the comparator.

**Implemented as**

- R\_ACMPHS\_Open()
- R\_ACMPLP\_Open()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	p_cfg	Pointer to configuration

◆ **outputEnable**

```
fsp_err_t(* comparator_api_t::outputEnable) (comparator_ctrl_t *const p_ctrl)
```

Start the comparator.

**Implemented as**

- R\_ACMPHS\_OutputEnable()
- R\_ACMPLP\_OutputEnable()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **infoGet**

```
fsp_err_t(* comparator_api_t::infoGet) (comparator_ctrl_t *const p_ctrl, comparator_info_t *const p_info)
```

Provide information such as the recommended minimum stabilization wait time.

**Implemented as**

- R\_ACMPHS\_InfoGet()
- R\_ACMPLP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_info	Comparator information stored here

◆ **statusGet**

```
fsp_err_t(* comparator_api_t::statusGet) (comparator_ctrl_t *const p_ctrl, comparator_status_t *const p_status)
```

Provide current comparator status.

**Implemented as**

- R\_ACMPHS\_StatusGet()
- R\_ACMPLP\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_status	Status stored here

◆ **close**

```
fsp_err_t(* comparator_api_t::close) (comparator_ctrl_t *const p_ctrl)
```

Stop the comparator.

**Implemented as**

- R\_ACMPHS\_Close()
- R\_ACMPLP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **comparator\_instance\_t**

```
struct comparator_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

comparator_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
comparator_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
comparator_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **comparator\_ctrl\_t**typedef void [comparator\\_ctrl\\_t](#)

Includes board and MCU related header files. Comparator control block. Allocate an instance specific control block to pass into the comparator API calls.

**Implemented as**

- [acmphs\\_instance\\_ctrl\\_t](#)
- [acmplp\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **comparator\_mode\_t**enum [comparator\\_mode\\_t](#)

Select whether to invert the polarity of the comparator output.

## Enumerator

COMPARATOR_MODE_NORMAL	Normal mode.
COMPARATOR_MODE_WINDOW	Window mode, not supported by all implementations.

◆ **comparator\_trigger\_t**enum [comparator\\_trigger\\_t](#)

Trigger type: rising edge, falling edge, both edges, low level.

## Enumerator

COMPARATOR_TRIGGER_RISING	Rising edge trigger.
COMPARATOR_TRIGGER_FALLING	Falling edge trigger.
COMPARATOR_TRIGGER_BOTH_EDGE	Both edges trigger.

◆ **comparator\_polarity\_invert\_t**

enum <code>comparator_polarity_invert_t</code>	
Select whether to invert the polarity of the comparator output.	
Enumerator	
<code>COMPARATOR_POLARITY_INVERT_OFF</code>	Do not invert polarity.
<code>COMPARATOR_POLARITY_INVERT_ON</code>	Invert polarity.

◆ **comparator\_pin\_output\_t**

enum <code>comparator_pin_output_t</code>	
Select whether to include the comparator output on the output pin.	
Enumerator	
<code>COMPARATOR_PIN_OUTPUT_OFF</code>	Do not include comparator output on output pin.
<code>COMPARATOR_PIN_OUTPUT_ON</code>	Include comparator output on output pin.

◆ **comparator\_filter\_t**

enum <code>comparator_filter_t</code>	
Comparator digital filtering sample clock divisor settings.	
Enumerator	
<code>COMPARATOR_FILTER_OFF</code>	Disable debounce filter.
<code>COMPARATOR_FILTER_1</code>	Filter using PCLK divided by 1, not supported by all implementations.
<code>COMPARATOR_FILTER_8</code>	Filter using PCLK divided by 8.
<code>COMPARATOR_FILTER_16</code>	Filter using PCLK divided by 16, not supported by all implementations.
<code>COMPARATOR_FILTER_32</code>	Filter using PCLK divided by 32.

◆ **comparator\_state\_t**

enum <code>comparator_state_t</code>	
Current comparator state.	
Enumerator	
<code>COMPARATOR_STATE_OUTPUT_LOW</code>	VCMP < VREF if polarity is not inverted, VCMP > VREF if inverted.
<code>COMPARATOR_STATE_OUTPUT_HIGH</code>	VCMP > VREF if polarity is not inverted, VCMP < VREF if inverted.
<code>COMPARATOR_STATE_OUTPUT_DISABLED</code>	<code>comparator_api_t::outputEnable()</code> has not been called

## 4.3.8 CRC Interface

### Interfaces

#### Detailed Description

Interface for cyclic redundancy checking.

## Summary

The CRC (Cyclic Redundancy Check) calculator generates CRC codes using five different polynomials including 8 bit, 16 bit, and 32 bit variations. Calculation can be performed by sending data to the block using the CPU or by snooping on read or write activity on one of 10 SCI channels.

Implemented by:

- [Cyclic Redundancy Check \(CRC\) Calculator \(`r\_crc`\)](#)

#### Data Structures

struct `crc_input_t`

struct `crc_cfg_t`

struct `crc_api_t`

struct `crc_instance_t`

#### Typedefs

typedef void `crc_ctrl_t`

## Enumerations

enum [crc\\_polynomial\\_t](#)

enum [crc\\_bit\\_order\\_t](#)

enum [crc\\_snoop\\_direction\\_t](#)

enum [crc\\_snoop\\_address\\_t](#)

## Data Structure Documentation

### ◆ [crc\\_input\\_t](#)

struct <a href="#">crc_input_t</a>
Structure for CRC inputs

### ◆ [crc\\_cfg\\_t](#)

struct <a href="#">crc_cfg_t</a>		
User configuration structure, used in open function		
Data Fields		
<a href="#">crc_polynomial_t</a>	polynomial	CRC Generating Polynomial Switching (GPS)
<a href="#">crc_bit_order_t</a>	bit_order	CRC Calculation Switching (LMS)
<a href="#">crc_snoop_address_t</a>	snoop_address	Register Snoop Address (CRCSA)
void const *	p_extend	CRC Hardware Dependent Configuration.

### ◆ [crc\\_api\\_t](#)

struct <a href="#">crc_api_t</a>	
CRC driver structure. General CRC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">crc_ctrl_t</a> *const p_ctrl, <a href="#">crc_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )( <a href="#">crc_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">crcResultGet</a> )( <a href="#">crc_ctrl_t</a> *const p_ctrl, <a href="#">uint32_t</a> *crc_result)
<a href="#">fsp_err_t</a> (*	<a href="#">snoopEnable</a> )( <a href="#">crc_ctrl_t</a> *const p_ctrl, <a href="#">uint32_t</a> crc_seed)

fsp_err_t(*	snoopDisable )(crc_ctrl_t *const p_ctrl)
-------------	--

fsp_err_t(*	calculate )(crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *p_crc_result)
-------------	---

## Field Documentation

### ◆ open

fsp_err_t(* crc_api_t::open) (	crc_ctrl_t *const p_ctrl, crc_cfg_t const *const p_cfg)
--------------------------------	---

Open the CRC driver module.

#### Implemented as

- [R\\_CRC\\_Open\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to CRC device handle.
[in]	p_cfg	Pointer to a configuration structure.

### ◆ close

fsp_err_t(* crc_api_t::close) (	crc_ctrl_t *const p_ctrl)
---------------------------------	---------------------------

Close the CRC module driver

#### Implemented as

- [R\\_CRC\\_Close\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to crc device handle
------	--------	------------------------------

#### Return values

FSP_SUCCESS	Configuration was successful.
-------------	-------------------------------

◆ **crcResultGet**

```
fsp_err_t(* crc_api_t::crcResultGet) (crc_ctrl_t *const p_ctrl, uint32_t *crc_result)
```

Return the current calculated value.

**Implemented as**

- R\_CRC\_CalculatedValueGet()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
[out]	crc_result	The calculated value from the last CRC calculation.

◆ **snoopEnable**

```
fsp_err_t(* crc_api_t::snoopEnable) (crc_ctrl_t *const p_ctrl, uint32_t crc_seed)
```

Configure and Enable snooping.

**Implemented as**

- R\_CRC\_SnoopEnable()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
[in]	crc_seed	CRC seed.

◆ **snoopDisable**

```
fsp_err_t(* crc_api_t::snoopDisable) (crc_ctrl_t *const p_ctrl)
```

Disable snooping.

**Implemented as**

- R\_CRC\_SnoopDisable()

**Parameters**

[in]	p_ctrl	Pointer to CRC device handle.
------	--------	-------------------------------

◆ **calculate**

```
fsp_err_t(* crc_api_t::calculate) (crc_ctrl_t *const p_ctrl, crc_input_t *const p_crc_input, uint32_t *p_crc_result)
```

Perform a CRC calculation on a block of data.

**Implemented as**

- [R\\_CRC\\_Calculate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to crc device handle.
[in]	p_crc_input	A pointer to structure for CRC inputs
[out]	crc_result	The calculated value of the CRC calculation.

◆ **crc\_instance\_t**

```
struct crc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

crc_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
crc_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
crc_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **crc\_ctrl\_t**

```
typedef void crc_ctrl_t
```

CRC control block. Allocate an instance specific control block to pass into the CRC API calls.

**Implemented as**

- [crc\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **crc\_polynomial\_t**

enum <code>crc_polynomial_t</code>	
CRC Generating Polynomial Switching (GPS).	
Enumerator	
<code>CRC_POLYNOMIAL_CRC_8</code>	8-bit CRC-8 ( $X^8 + X^2 + X + 1$ )
<code>CRC_POLYNOMIAL_CRC_16</code>	16-bit CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ )
<code>CRC_POLYNOMIAL_CRC_CCITT</code>	16-bit CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ )
<code>CRC_POLYNOMIAL_CRC_32</code>	32-bit CRC-32 ( $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ )
<code>CRC_POLYNOMIAL_CRC_32C</code>	32-bit CRC-32C ( $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ )

◆ **crc\_bit\_order\_t**

enum <code>crc_bit_order_t</code>	
CRC Calculation Switching (LMS)	
Enumerator	
<code>CRC_BIT_ORDER_LMS_LSB</code>	Generates CRC for LSB first communication.
<code>CRC_BIT_ORDER_LMS_MSB</code>	Generates CRC for MSB first communication.

◆ **crc\_snoop\_direction\_t**

enum <code>crc_snoop_direction_t</code>	
Snoop-On-Write/Read Switch (CRCSWR)	
Enumerator	
<code>CRC_SNOOP_DIRECTION_RECEIVE</code>	Snoop-on-read.
<code>CRC_SNOOP_DIRECTION_TRANSMIT</code>	Snoop-on-write.

◆ **enum crc\_snoop\_address\_t**

enum <code>enum crc_snoop_address_t</code>	
Snoop SCI register Address (lower 14 bits)	
Enumerator	
<code>CRC_SNOOP_ADDRESS_NONE</code>	Snoop mode disabled.
<code>CRC_SNOOP_ADDRESS_SCI0_TDR</code>	Snoop SCI0 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI1_TDR</code>	Snoop SCI1 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI2_TDR</code>	Snoop SCI2 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI3_TDR</code>	Snoop SCI3 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI4_TDR</code>	Snoop SCI4 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI5_TDR</code>	Snoop SCI5 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI6_TDR</code>	Snoop SCI6 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI7_TDR</code>	Snoop SCI7 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI8_TDR</code>	Snoop SCI8 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI9_TDR</code>	Snoop SCI9 transmit data register.
<code>CRC_SNOOP_ADDRESS_SCI0_FTDRL</code>	Snoop SCI0 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI1_FTDRL</code>	Snoop SCI1 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI2_FTDRL</code>	Snoop SCI2 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI3_FTDRL</code>	Snoop SCI3 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI4_FTDRL</code>	Snoop SCI4 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI5_FTDRL</code>	Snoop SCI5 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI6_FTDRL</code>	Snoop SCI6 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI7_FTDRL</code>	Snoop SCI7 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI8_FTDRL</code>	Snoop SCI8 transmit FIFO data register.
<code>CRC_SNOOP_ADDRESS_SCI9_FTDRL</code>	Snoop SCI9 transmit FIFO data register.

CRC_SNOOP_ADDRESS_SCI0_RDR	Snoop SCI0 receive data register.
CRC_SNOOP_ADDRESS_SCI1_RDR	Snoop SCI1 receive data register.
CRC_SNOOP_ADDRESS_SCI2_RDR	Snoop SCI2 receive data register.
CRC_SNOOP_ADDRESS_SCI3_RDR	Snoop SCI3 receive data register.
CRC_SNOOP_ADDRESS_SCI4_RDR	Snoop SCI4 receive data register.
CRC_SNOOP_ADDRESS_SCI5_RDR	Snoop SCI5 receive data register.
CRC_SNOOP_ADDRESS_SCI6_RDR	Snoop SCI6 receive data register.
CRC_SNOOP_ADDRESS_SCI7_RDR	Snoop SCI7 receive data register.
CRC_SNOOP_ADDRESS_SCI8_RDR	Snoop SCI8 receive data register.
CRC_SNOOP_ADDRESS_SCI9_RDR	Snoop SCI9 receive data register.
CRC_SNOOP_ADDRESS_SCI0_FRDRL	Snoop SCI0 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI1_FRDRL	Snoop SCI1 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI2_FRDRL	Snoop SCI2 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI3_FRDRL	Snoop SCI3 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI4_FRDRL	Snoop SCI4 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI5_FRDRL	Snoop SCI5 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI6_FRDRL	Snoop SCI6 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI7_FRDRL	Snoop SCI7 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI8_FRDRL	Snoop SCI8 receive FIFO data register.
CRC_SNOOP_ADDRESS_SCI9_FRDRL	Snoop SCI9 receive FIFO data register.

### 4.3.9 CTSU Interface

#### Interfaces

## Detailed Description

---

Interface for Capacitive Touch Sensing Unit (CTSU) functions.

## Summary

The CTSU interface provides CTSU functionality.

The CTSU interface can be implemented by:

- [Capacitive Touch Sensing Unit \(r\\_ctsu\)](#)

## Data Structures

---

struct [ctsu\\_callback\\_args\\_t](#)

struct [ctsu\\_element\\_cfg\\_t](#)

struct [ctsu\\_cfg\\_t](#)

struct [ctsu\\_api\\_t](#)

struct [ctsu\\_instance\\_t](#)

## Typedefs

---

typedef void [ctsu\\_ctrl\\_t](#)

## Enumerations

---

enum [ctsu\\_event\\_t](#)

enum [ctsu\\_cap\\_t](#)

enum [ctsu\\_txvsel\\_t](#)

enum [ctsu\\_txvsel2\\_t](#)

enum [ctsu\\_atune1\\_t](#)

enum [ctsu\\_atune12\\_t](#)

enum [ctsu\\_md\\_t](#)

enum [ctsu\\_posel\\_t](#)

enum [ctsu\\_ssdiv\\_t](#)

---

## Data Structure Documentation

---

### ◆ [ctsu\\_callback\\_args\\_t](#)

struct ctsu_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">ctsu_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data. Set in <a href="#">ctsu_api_t::open</a> function in <a href="#">ctsu_cfg_t</a> .

◆ **ctsu\_element\_cfg\_t**

struct ctsu_element_cfg_t		
CTSU Configuration parameters. Element Configuration		
Data Fields		
<a href="#">ctsu_sdiv_t</a>	ssdiv	CTSU Spectrum Diffusion Frequency Division Setting (CTSU Only)
uint16_t	so	CTSU Sensor Offset Adjustment.
uint8_t	snum	CTSU Measurement Count Setting.
uint8_t	sdpa	CTSU Base Clock Setting.

◆ **ctsu\_cfg\_t**

struct ctsu_cfg_t	
User configuration structure, used in open function	
Data Fields	
<a href="#">ctsu_cap_t</a>	cap
	CTSU Scan Start Trigger Select.
<a href="#">ctsu_txvsel_t</a>	txvsel
	CTSU Transmission Power Supply Select.
<a href="#">ctsu_txvsel2_t</a>	txvsel2
	CTSU Transmission Power Supply Select 2 (CTSU2 Only)
<a href="#">ctsu_atune1_t</a>	atune1

	CTSU Power Supply Capacity Adjustment (CTSU Only)
<code>cts_u_atune12_t</code>	<code>atune12</code>
	CTSU Power Supply Capacity Adjustment (CTSU2 Only)
<code>cts_u_md_t</code>	<code>md</code>
	CTSU Measurement Mode Select.
<code>cts_u_posel_t</code>	<code>posel</code>
	CTSU Non-Measured Channel Output Select (CTSU2 Only)
<code>uint8_t</code>	<code>cts_uhac0</code>
	TS00-TS07 enable mask.
<code>uint8_t</code>	<code>cts_uhac1</code>
	TS08-TS15 enable mask.
<code>uint8_t</code>	<code>cts_uhac2</code>
	TS16-TS23 enable mask.
<code>uint8_t</code>	<code>cts_uhac3</code>
	TS24-TS31 enable mask.
<code>uint8_t</code>	<code>cts_uhac4</code>
	TS32-TS39 enable mask.
<code>uint8_t</code>	<code>cts_uhtrc0</code>
	TS00-TS07 mutual-tx mask.

uint8_t	<a href="#">ctsuchtrc1</a>
	TS08-TS15 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc2</a>
	TS16-TS23 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc3</a>
	TS24-TS31 mutual-tx mask.
uint8_t	<a href="#">ctsuchtrc4</a>
	TS32-TS39 mutual-tx mask.
<a href="#">ctsu_element_cfg_t</a> const *	<a href="#">p_elements</a>
	Pointer to elements configuration array.
uint8_t	<a href="#">num_rx</a>
	Number of receive terminals.
uint8_t	<a href="#">num_tx</a>
	Number of transmit terminals.
uint16_t	<a href="#">num_moving_average</a>
	Number of moving average for measurement data.
bool	<a href="#">tunning_enable</a>
	Initial offset tuning flag.

bool	<a href="#">judge_multifreq_disable</a>
	Disable to judge multi frequency.
void(*	<a href="#">p_callback</a> )(ctsu_callback_args_t *p_args)
	Callback provided when CTSUFN ISR occurs.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_tx</a>
	DTC instance for transmit at CTSUWR. Set to NULL if unused.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_rx</a>
	DTC instance for receive at CTSURD. Set to NULL if unused.
<a href="#">adc_instance_t</a> const *	<a href="#">p_adc_instance</a>
	ADC instance for temperature correction.
IRQn_Type	<a href="#">write_irq</a>
	CTSU_CTSUWR interrupt vector.
IRQn_Type	<a href="#">read_irq</a>
	CTSU_CTSURD interrupt vector.
IRQn_Type	<a href="#">end_irq</a>
	CTSU_CTSUFN interrupt vector.
void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>

	Pointer to extended configuration by instance of interface.
--	---

### ◆ ctsu\_api\_t

struct ctsu\_api\_t

Functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*)	open )(ctsu_ctrl_t *const p_ctrl, ctsu_cfg_t const *const p_cfg)
fsp_err_t(*)	scanStart )(ctsu_ctrl_t *const p_ctrl)
fsp_err_t(*)	dataGet )(ctsu_ctrl_t *const p_ctrl, uint16_t *p_data)
fsp_err_t(*)	diagnosis )(ctsu_ctrl_t *const p_ctrl)
fsp_err_t(*)	callbackSet )(ctsu_ctrl_t *const p_api_ctrl, void(*p_callback)(ctsu_callback_args_t *), void const *const p_context, ctsu_callback_args_t *const p_callback_memory)
fsp_err_t(*)	close )(ctsu_ctrl_t *const p_ctrl)

#### Field Documentation

##### ◆ open

fsp\_err\_t(\*) ctsu\_api\_t::open (ctsu\_ctrl\_t \*const p\_ctrl, ctsu\_cfg\_t const \*const p\_cfg)

Open driver.

#### Implemented as

- R\_CTSU\_Open()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

## ◆ scanStart

```
fsp_err_t(* ctsu_api_t::scanStart) (ctsu_ctrl_t *const p_ctrl)
```

Scan start.

**Implemented as**

- R\_CTSU\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

## ◆ dataGet

```
fsp_err_t(* ctsu_api_t::dataGet) (ctsu_ctrl_t *const p_ctrl, uint16_t *p_data)
```

Data get.

**Implemented as**

- R\_CTSU\_DataGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_data	Pointer to get data array.

## ◆ diagnosis

```
fsp_err_t(* ctsu_api_t::diagnosis) (ctsu_ctrl_t *const p_ctrl)
```

Diagnosis.

**Implemented as**

- R\_CTSU\_Diagnosis()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **callbackSet**

```
fsp_err_t(* ctsu_api_t::callbackSet) (ctsu_ctrl_t *const p_api_ctrl,
void(*p_callback)(ctsu_callback_args_t *), void const *const p_context, ctsu_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_CTSU\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the CTSU control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* ctsu_api_t::close) (ctsu_ctrl_t *const p_ctrl)
```

Close driver.

**Implemented as**

- R\_CTSU\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **ctsu\_instance\_t**

```
struct ctsu_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

ctsu_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
ctsu_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
ctsu_api_t const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `ctsu_ctrl_t`

typedef void `ctsu_ctrl_t`

CTSU Control block. Allocate an instance specific control block to pass into the API calls.

#### Implemented as

- `ctsu_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `ctsu_event_t`

enum `ctsu_event_t`

CTSU Events for callback function

#### Enumerator

<code>CTSU_EVENT_SCAN_COMPLETE</code>	Normal end.
<code>CTSU_EVENT_OVERFLOW</code>	Sensor counter overflow (CTSUST.CTUSOVF set)
<code>CTSU_EVENT_ICOMP</code>	Abnormal TSCAP voltage (CTSUERRS.CTSUICOMP set)
<code>CTSU_EVENT_ICOMP1</code>	Abnormal sensor current (CTSUSR.ICOMP1 set)

### ◆ `ctsu_cap_t`

enum `ctsu_cap_t`

CTSU Scan Start Trigger Select

#### Enumerator

<code>CTSU_CAP_SOFTWARE</code>	Scan start by software trigger.
<code>CTSU_CAP_EXTERNAL</code>	Scan start by external trigger.

◆ **ctsu\_txvsel\_t**

enum <a href="#">ctsu_txvsel_t</a>	
CTSU Transmission Power Supply Select	
Enumerator	
CTSU_TXVSEL_VCC	VCC selected.
CTSU_TXVSEL_INTERNAL_POWER	Internal logic power supply selected.

◆ **ctsu\_txvsel2\_t**

enum <a href="#">ctsu_txvsel2_t</a>	
CTSU Transmission Power Supply Select 2 (CTSU2 Only)	
Enumerator	
CTSU_TXVSEL_MODE	Follow TXVSEL setting.
CTSU_TXVSEL_VCC_PRIVATE	VCC private selected.

◆ **ctsu\_atune1\_t**

enum <a href="#">ctsu_atune1_t</a>	
CTSU Power Supply Capacity Adjustment (CTSU Only)	
Enumerator	
CTSU_ATUNE1_NORMAL	Normal output (40uA)
CTSU_ATUNE1_HIGH	High-current output (80uA)

◆ **ctsu\_atune12\_t**

enum <code>ctsu_atune12_t</code>	
CTSU Power Supply Capacity Adjustment (CTSUS2 Only)	
Enumerator	
<code>CTSU_ATUNE12_80UA</code>	High-current output (80uA)
<code>CTSU_ATUNE12_40UA</code>	Normal output (40uA)
<code>CTSU_ATUNE12_20UA</code>	Low-current output (20uA)
<code>CTSU_ATUNE12_160UA</code>	Very high-current output (160uA)

◆ **ctsu\_md\_t**

enum <code>ctsu_md_t</code>	
CTSU Measurement Mode Select	
Enumerator	
<code>CTSU_MODE_SELF_MULTI_SCAN</code>	Self-capacitance multi scan mode.
<code>CTSU_MODE_MUTUAL_FULL_SCAN</code>	Mutual capacitance full scan mode.
<code>CTSU_MODE_MUTUAL_CFC_SCAN</code>	Mutual capacitance cfc scan mode (CTSUS2 Only)
<code>CTSU_MODE_CURRENT_SCAN</code>	Current scan mode (CTSUS2 Only)
<code>CTSU_MODE_CORRECTION_SCAN</code>	Correction scan mode (CTSUS2 Only)
<code>CTSU_MODE_DIAGNOSIS_SCAN</code>	Diagnosis scan mode.

◆ **ctsu\_posel\_t**

enum <code>ctsu_posel_t</code>	
CTSU Non-Measured Channel Output Select (CTS2 Only)	
Enumerator	
<code>CTSU_POSEL_LOW_GPIO</code>	Output low through GPIO.
<code>CTSU_POSEL_HI_Z</code>	Hi-Z.
<code>CTSU_POSEL_LOW</code>	Output low through the power setting by the TXVSEL[1:0] bits.
<code>CTSU_POSEL_SAME_PULSE</code>	Same phase pulse output as transmission channel through the power setting by the TXVSEL[1:0] bits.

◆ **ctsu\_ssddiv\_t**

enum <code>ctsu_ssddiv_t</code>	
CTSU Spectrum Diffusion Frequency Division Setting (CTSU Only)	
Enumerator	
<code>CTSU_SSDIV_4000</code>	4.00 <= Base clock frequency (MHz)
<code>CTSU_SSDIV_2000</code>	2.00 <= Base clock frequency (MHz) < 4.00
<code>CTSU_SSDIV_1330</code>	1.33 <= Base clock frequency (MHz) < 2.00
<code>CTSU_SSDIV_1000</code>	1.00 <= Base clock frequency (MHz) < 1.33
<code>CTSU_SSDIV_0800</code>	0.80 <= Base clock frequency (MHz) < 1.00
<code>CTSU_SSDIV_0670</code>	0.67 <= Base clock frequency (MHz) < 0.80
<code>CTSU_SSDIV_0570</code>	0.57 <= Base clock frequency (MHz) < 0.67
<code>CTSU_SSDIV_0500</code>	0.50 <= Base clock frequency (MHz) < 0.57
<code>CTSU_SSDIV_0440</code>	0.44 <= Base clock frequency (MHz) < 0.50
<code>CTSU_SSDIV_0400</code>	0.40 <= Base clock frequency (MHz) < 0.44
<code>CTSU_SSDIV_0360</code>	0.36 <= Base clock frequency (MHz) < 0.40
<code>CTSU_SSDIV_0330</code>	0.33 <= Base clock frequency (MHz) < 0.36
<code>CTSU_SSDIV_0310</code>	0.31 <= Base clock frequency (MHz) < 0.33
<code>CTSU_SSDIV_0290</code>	0.29 <= Base clock frequency (MHz) < 0.31
<code>CTSU_SSDIV_0270</code>	0.27 <= Base clock frequency (MHz) < 0.29
<code>CTSU_SSDIV_0000</code>	0.00 <= Base clock frequency (MHz) < 0.27

**4.3.10 DAC Interface**[Interfaces](#)**Detailed Description**

Interface for D/A converters.

## Summary

The DAC interface provides standard Digital/Analog Converter functionality. A DAC application writes digital sample data to the device and generates analog output on the DAC output pin.

Implemented by:

- Digital to Analog Converter (r\_dac)
- Digital to Analog Converter (r\_dac8)

### Data Structures

struct `dac_info_t`

struct `dac_cfg_t`

struct `dac_api_t`

struct `dac_instance_t`

### Typedefs

typedef void `dac_ctrl_t`

### Enumerations

enum `dac_data_format_t`

### Data Structure Documentation

#### ◆ `dac_info_t`

struct <code>dac_info_t</code>		
DAC information structure to store various information for a DAC		
Data Fields		
<code>uint8_t</code>	<code>bit_width</code>	Resolution of the DAC.

#### ◆ `dac_cfg_t`

struct <code>dac_cfg_t</code>		
DAC Open API configuration parameter		
Data Fields		
<code>uint8_t</code>	<code>channel</code>	ID associated with this DAC channel.
<code>bool</code>	<code>ad_da_synchronized</code>	AD/DA synchronization.
<code>void const *</code>	<code>p_extend</code>	

◆ **dac\_api\_t**

struct dac\_api\_t

DAC driver structure. General DAC functions implemented at the HAL layer follow this API.

**Data Fields**fsp\_err\_t(\* **open** )(dac\_ctrl\_t \*const p\_ctrl, dac\_cfg\_t const \*const p\_cfg)fsp\_err\_t(\* **close** )(dac\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* **write** )(dac\_ctrl\_t \*const p\_ctrl, uint16\_t value)fsp\_err\_t(\* **start** )(dac\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* **stop** )(dac\_ctrl\_t \*const p\_ctrl)**Field Documentation**◆ **open**

fsp\_err\_t(\* dac\_api\_t::open) (dac\_ctrl\_t \*const p\_ctrl, dac\_cfg\_t const \*const p\_cfg)

Initial configuration.

**Implemented as**

- R\_DAC\_Open()
- R\_DAC8\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **close**

```
fsp_err_t(* dac_api_t::close) (dac_ctrl_t *const p_ctrl)
```

Close the D/A Converter.

**Implemented as**

- [R\\_DAC\\_Close\(\)](#)
- [R\\_DAC8\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---

◆ **write**

```
fsp_err_t(* dac_api_t::write) (dac_ctrl_t *const p_ctrl, uint16_t value)
```

Write sample value to the D/A Converter.

**Implemented as**

- [R\\_DAC\\_Write\(\)](#)
- [R\\_DAC8\\_Write\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
[in]	value	Sample value to be written to the D/A Converter.

◆ **start**

```
fsp_err_t(* dac_api_t::start) (dac_ctrl_t *const p_ctrl)
```

Start the D/A Converter if it has not been started yet.

**Implemented as**

- [R\\_DAC\\_Start\(\)](#)
- [R\\_DAC8\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---

◆ **stop**

```
fsp_err_t(* dac_api_t::stop) (dac_ctrl_t *const p_ctrl)
```

Stop the D/A Converter if the converter is running.

**Implemented as**

- R\_DAC\_Stop()
- R\_DAC8\_Stop()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">dac_api_t::open</a> call for this timer.
------	--------	---

◆ **dac\_instance\_t**

```
struct dac_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">dac_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">dac_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">dac_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **dac\_ctrl\_t**

```
typedef void dac_ctrl_t
```

DAC control block. Allocate an instance specific control block to pass into the DAC API calls.

**Implemented as**

- [dac\\_instance\\_ctrl\\_t](#)
- [dac8\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **dac\_data\_format\_t**

enum <code>dac_data_format_t</code>	
DAC Open API data format settings.	
Enumerator	
<code>DAC_DATA_FORMAT_FLUSH_RIGHT</code>	LSB of data is flush to the right leaving the top 4 bits unused.
<code>DAC_DATA_FORMAT_FLUSH_LEFT</code>	MSB of data is flush to the left leaving the bottom 4 bits unused.

### 4.3.11 Display Interface

#### Interfaces

#### Detailed Description

Interface for LCD panel displays.

## Summary

The display interface provides standard display functionality:

- Signal timing configuration for LCD panels with RGB interface.
- Dot clock source selection (internal or external) and frequency divider.
- Blending of multiple graphics layers on the background screen.
- Color correction (brightness/configuration/gamma correction).
- Interrupts and callback function.

Implemented by: [Graphics LCD Controller \(r\\_glcdc\)](#)

#### Data Structures

struct [display\\_timing\\_t](#)

struct [display\\_color\\_t](#)

struct [display\\_coordinate\\_t](#)

struct [display\\_brightness\\_t](#)

struct [display\\_contrast\\_t](#)

struct [display\\_correction\\_t](#)

struct	<a href="#">gamma_correction_t</a>
--------	------------------------------------

struct	<a href="#">display_gamma_correction_t</a>
--------	--

struct	<a href="#">display_clut_t</a>
--------	--------------------------------

struct	<a href="#">display_input_cfg_t</a>
--------	-------------------------------------

struct	<a href="#">display_output_cfg_t</a>
--------	--------------------------------------

struct	<a href="#">display_layer_t</a>
--------	---------------------------------

struct	<a href="#">display_callback_args_t</a>
--------	---

struct	<a href="#">display_cfg_t</a>
--------	-------------------------------

struct	<a href="#">display_runtime_cfg_t</a>
--------	---------------------------------------

struct	<a href="#">display_clut_cfg_t</a>
--------	------------------------------------

struct	<a href="#">display_status_t</a>
--------	----------------------------------

struct	<a href="#">display_api_t</a>
--------	-------------------------------

struct	<a href="#">display_instance_t</a>
--------	------------------------------------

---

## Typedefs

typedef void	<a href="#">display_ctrl_t</a>
--------------	--------------------------------

---

## Enumerations

enum	<a href="#">display_frame_layer_t</a>
------	---------------------------------------

enum	<a href="#">display_state_t</a>
------	---------------------------------

enum	<a href="#">display_event_t</a>
------	---------------------------------

enum	<a href="#">display_in_format_t</a>
------	-------------------------------------

enum	<a href="#">display_out_format_t</a>
------	--------------------------------------

enum	<a href="#">display_endian_t</a>
------	----------------------------------

enum	<a href="#">display_color_order_t</a>
------	---------------------------------------

enum	<a href="#">display_signal_polarity_t</a>
------	---

enum	<a href="#">display_sync_edge_t</a>
------	-------------------------------------

enum [display\\_fade\\_control\\_t](#)enum [display\\_fade\\_status\\_t](#)**Data Structure Documentation****◆ display\_timing\_t**

struct display_timing_t		
Display signal timing setting		
Data Fields		
uint16_t	total_cyc	Total cycles in one line or total lines in one frame.
uint16_t	display_cyc	Active video cycles or lines.
uint16_t	back_porch	Back porch cycles or lines.
uint16_t	sync_width	Sync signal asserting width.
<a href="#">display_signal_polarity_t</a>	sync_polarity	Sync signal polarity.

**◆ display\_color\_t**

struct display_color_t		
RGB Color setting		

**◆ display\_coordinate\_t**

struct display_coordinate_t		
Contrast (gain) correction setting		
Data Fields		
int16_t	x	Coordinate X, this allows to set signed value.
int16_t	y	Coordinate Y, this allows to set signed value.

**◆ display\_brightness\_t**

struct display_brightness_t		
Brightness (DC) correction setting		
Data Fields		
bool	enable	Brightness Correction On/Off.
uint16_t	r	Brightness (DC) adjustment for R channel.
uint16_t	g	Brightness (DC) adjustment for G channel.

uint16_t	b	Brightness (DC) adjustment for B channel.
----------	---	---

#### ◆ display\_contrast\_t

struct display_contrast_t		
Contrast (gain) correction setting		
Data Fields		
bool	enable	Contrast Correction On/Off.
uint8_t	r	Contrast (gain) adjustment for R channel.
uint8_t	g	Contrast (gain) adjustment for G channel.
uint8_t	b	Contrast (gain) adjustment for B channel.

#### ◆ display\_correction\_t

struct display_correction_t		
Color correction setting		
Data Fields		
<a href="#">display_brightness_t</a>	brightness	Brightness.
<a href="#">display_contrast_t</a>	contrast	Contrast.

#### ◆ gamma\_correction\_t

struct gamma_correction_t		
Gamma correction setting for each color		
Data Fields		
bool	enable	Gamma Correction On/Off.
uint16_t *	gain	Gain adjustment.
uint16_t *	threshold	Start threshold.

#### ◆ display\_gamma\_correction\_t

struct display_gamma_correction_t		
Gamma correction setting		
Data Fields		
<a href="#">gamma_correction_t</a>	r	Gamma correction for R channel.
<a href="#">gamma_correction_t</a>	g	Gamma correction for G channel.
<a href="#">gamma_correction_t</a>	b	Gamma correction for B

channel.

◆ **display\_clut\_t**

struct display_clut_t		
CLUT setting		
Data Fields		
uint32_t	color_num	The number of colors in CLUT.
const uint32_t *	p_clut	Address of the area storing the CLUT data (in ARGB8888 format)

◆ **display\_input\_cfg\_t**

struct display_input_cfg_t		
Graphics plane input configuration structure		
Data Fields		
uint32_t *	p_base	Base address to the frame buffer.
uint16_t	hsize	Horizontal pixel size in a line.
uint16_t	vsize	Vertical pixel size in a frame.
uint32_t	hstride	Memory stride (bytes) in a line.
<a href="#">display_in_format_t</a>	format	Input format setting.
bool	line_descending_enable	Line descending enable.
bool	lines_repeat_enable	Line repeat enable.
uint16_t	lines_repeat_times	Expected number of line repeating.

◆ **display\_output\_cfg\_t**

struct display_output_cfg_t		
Display output configuration structure		
Data Fields		
<a href="#">display_timing_t</a>	htiming	Horizontal display cycle setting.
<a href="#">display_timing_t</a>	vtiming	Vertical display cycle setting.
<a href="#">display_out_format_t</a>	format	Output format setting.
<a href="#">display_endian_t</a>	endian	Bit order of output data.
<a href="#">display_color_order_t</a>	color_order	Color order in pixel.
<a href="#">display_signal_polarity_t</a>	data_enable_polarity	Data Enable signal polarity.
<a href="#">display_sync_edge_t</a>	sync_edge	Signal sync edge selection.
<a href="#">display_color_t</a>	bg_color	Background color.

<a href="#">display_brightness_t</a>	brightness	Brightness setting.
<a href="#">display_contrast_t</a>	contrast	Contrast setting.
<a href="#">display_gamma_correction_t</a> *	p_gamma_correction	Pointer to gamma correction setting.
bool	dithering_on	Dithering on/off.

◆ **display\_layer\_t**

struct display_layer_t		
Graphics layer blend setup parameter structure		
Data Fields		
<a href="#">display_coordinate_t</a>	coordinate	Blending location (starting point of image)
<a href="#">display_color_t</a>	bg_color	Color outside region.
<a href="#">display_fade_control_t</a>	fade_control	Layer fade-in/out control on/off.
uint8_t	fade_speed	Layer fade-in/out frame rate.

◆ **display\_callback\_args\_t**

struct display_callback_args_t		
Display callback parameter definition		
Data Fields		
<a href="#">display_event_t</a>	event	Event code.
void const *	p_context	Context provided to user during callback.

◆ **display\_cfg\_t**

struct display_cfg_t		
Display main configuration structure		
<b>Data Fields</b>		
<a href="#">display_input_cfg_t</a>	input [2]	
		Graphics input frame setting. <a href="#">More...</a>
<a href="#">display_output_cfg_t</a>	output	
		Graphics output frame setting.
<a href="#">display_layer_t</a>	layer [2]	
		Graphics layer blend setting.

uint8_t	<a href="#">line_detect_ipl</a>
	Line detect interrupt priority.
uint8_t	<a href="#">underflow_1_ipl</a>
	Underflow 1 interrupt priority.
uint8_t	<a href="#">underflow_2_ipl</a>
	Underflow 2 interrupt priority.
IRQn_Type	<a href="#">line_detect_irq</a>
	Line detect interrupt vector.
IRQn_Type	<a href="#">underflow_1_irq</a>
	Underflow 1 interrupt vector.
IRQn_Type	<a href="#">underflow_2_irq</a>
	Underflow 2 interrupt vector.
void(*	<a href="#">p_callback</a> )(display_callback_args_t *p_args)
	Pointer to callback function. <a href="#">More...</a>
void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	Display hardware dependent configuration. <a href="#">More...</a>

## Field Documentation

### ◆ input

`display_input_cfg_t display_cfg_t::input[2]`

Graphics input frame setting.

Generic configuration for display devices

### ◆ p\_callback

`void(* display_cfg_t::p_callback) (display_callback_args_t *p_args)`

Pointer to callback function.

Configuration for display event processing

### ◆ p\_extend

`void const* display_cfg_t::p_extend`

Display hardware dependent configuration.

Pointer to display peripheral specific configuration

### ◆ display\_runtime\_cfg\_t

`struct display_runtime_cfg_t`

Display main configuration structure

#### Data Fields

<code>display_input_cfg_t</code>	input	Graphics input frame setting. Generic configuration for display devices
<code>display_layer_t</code>	layer	Graphics layer alpha blending setting.

### ◆ display\_clut\_cfg\_t

`struct display_clut_cfg_t`

Display CLUT configuration structure

#### Data Fields

<code>uint32_t *</code>	p_base	Pointer to CLUT source data.
<code>uint16_t</code>	start	Beginning of CLUT entry to be updated.
<code>uint16_t</code>	size	Size of CLUT entry to be updated.

### ◆ display\_status\_t

`struct display_status_t`

Display Status		
Data Fields		
<a href="#">display_state_t</a>	state	Status of GLCDC module.
<a href="#">display_fade_status_t</a>	fade_status[ <a href="#">DISPLAY_FRAME_LAYER_2+1</a> ]	Status of fade-in/fade-out status.

◆ **display\_api\_t**

struct display_api_t		
Shared Interface definition for display peripheral		
Data Fields		
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">display_ctrl_t</a> *const p_ctrl, <a href="#">display_cfg_t</a> const *const p_cfg)	
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )( <a href="#">display_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">start</a> )( <a href="#">display_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">stop</a> )( <a href="#">display_ctrl_t</a> *const p_ctrl)	
<a href="#">fsp_err_t</a> (*	<a href="#">layerChange</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">display_runtime_cfg_t</a> const *const p_cfg, <a href="#">display_frame_layer_t</a> frame)	
<a href="#">fsp_err_t</a> (*	<a href="#">bufferChange</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">uint8_t</a> *const framebuffer, <a href="#">display_frame_layer_t</a> frame)	
<a href="#">fsp_err_t</a> (*	<a href="#">correction</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">display_correction_t</a> const *const p_param)	
<a href="#">fsp_err_t</a> (*	<a href="#">clut</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">display_clut_cfg_t</a> const *const p_clut_cfg, <a href="#">display_frame_layer_t</a> layer)	
<a href="#">fsp_err_t</a> (*	<a href="#">clutEdit</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">display_frame_layer_t</a> layer, <a href="#">uint8_t</a> index, <a href="#">uint32_t</a> color)	
<a href="#">fsp_err_t</a> (*	<a href="#">statusGet</a> )( <a href="#">display_ctrl_t</a> const *const p_ctrl, <a href="#">display_status_t</a> *const p_status)	

## Field Documentation

### ◆ open

`fsp_err_t(* display_api_t::open) (display_ctrl_t *const p_ctrl, display_cfg_t const *const p_cfg)`

Open display device.

#### Implemented as

- [R\\_GLCDC\\_Open\(\)](#)

#### Parameters

[in,out]	p_ctrl	Pointer to display interface control block. Must be declared by user. Value set here.
[in]	p_cfg	Pointer to display configuration structure. All elements of this structure must be set by user.

### ◆ close

`fsp_err_t(* display_api_t::close) (display_ctrl_t *const p_ctrl)`

Close display device.

#### Implemented as

- [R\\_GLCDC\\_Close\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

### ◆ start

`fsp_err_t(* display_api_t::start) (display_ctrl_t *const p_ctrl)`

Display start.

#### Implemented as

- [R\\_GLCDC\\_Start\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

## ◆ stop

```
fsp_err_t(* display_api_t::stop) (display_ctrl_t *const p_ctrl)
```

Display stop.

**Implemented as**

- R\_GLCDC\_Stop()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

## ◆ layerChange

```
fsp_err_t(* display_api_t::layerChange) (display_ctrl_t const *const p_ctrl, display_runtime_cfg_t const *const p_cfg, display_frame_layer_t frame)
```

Change layer parameters at runtime.

**Implemented as**

- R\_GLCDC\_LayerChange()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	p_cfg	Pointer to run-time layer configuration structure.
[in]	frame	Number of graphic frames.

## ◆ bufferChange

```
fsp_err_t(* display_api_t::bufferChange) (display_ctrl_t const *const p_ctrl, uint8_t *const framebuffer, display_frame_layer_t frame)
```

Change layer framebuffer pointer.

**Implemented as**

- R\_GLCDC\_BufferChange()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	framebuffer	Pointer to desired framebuffer.
[in]	frame	Number of graphic frames.

◆ **correction**

```
fsp_err_t(* display_api_t::correction) (display_ctrl_t const *const p_ctrl, display_correction_t const *const p_param)
```

Color correction.

**Implemented as**

- R\_GLCDC\_ColorCorrection()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	param	Pointer to color correction configuration structure.

◆ **clut**

```
fsp_err_t(* display_api_t::clut) (display_ctrl_t const *const p_ctrl, display_clut_cfg_t const *const p_clut_cfg, display_frame_layer_t layer)
```

Set CLUT for display device.

**Implemented as**

- R\_GLCDC\_ClutUpdate()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	p_clut_cfg	Pointer to CLUT configuration structure.
[in]	layer	Layer number corresponding to the CLUT.

◆ **clutEdit**

```
fsp_err_t(* display_api_t::clutEdit) (display_ctrl_t const *const p_ctrl, display_frame_layer_t layer,
uint8_t index, uint32_t color)
```

Set CLUT element for display device.

**Implemented as**

- R\_GLCDC\_ClutEdit()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	layer	Layer number corresponding to the CLUT.
[in]	index	CLUT element index.
[in]	color	Desired CLUT index color.

◆ **statusGet**

```
fsp_err_t(* display_api_t::statusGet) (display_ctrl_t const *const p_ctrl, display_status_t *const
p_status)
```

Get status for display device.

**Implemented as**

- R\_GLCDC\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	status	Pointer to display interface status structure.

◆ **display\_instance\_t**

```
struct display_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

display_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
display_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
display_api_t const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ display\_ctrl\_t

typedef void [display\\_ctrl\\_t](#)

Display control block. Allocate an instance specific control block to pass into the display API calls.

#### Implemented as

- `glcdc_instance_ctrl_t` Display control block

## Enumeration Type Documentation

### ◆ display\_frame\_layer\_t

enum [display\\_frame\\_layer\\_t](#)

Display frame number

Enumerator

DISPLAY_FRAME_LAYER_1	Frame layer 1.
DISPLAY_FRAME_LAYER_2	Frame layer 2.

### ◆ display\_state\_t

enum [display\\_state\\_t](#)

Display interface operation state

Enumerator

DISPLAY_STATE_CLOSED	Display closed.
DISPLAY_STATE_OPENED	Display opened.
DISPLAY_STATE_DISPLAYING	Displaying.

◆ **display\_event\_t**

enum <code>display_event_t</code>	
Display event codes	
Enumerator	
<code>DISPLAY_EVENT_GR1_UNDERFLOW</code>	Graphics frame1 underflow occurs.
<code>DISPLAY_EVENT_GR2_UNDERFLOW</code>	Graphics frame2 underflow occurs.
<code>DISPLAY_EVENT_LINE_DETECTION</code>	Designated line is processed.

◆ **display\_in\_format\_t**

enum <code>display_in_format_t</code>	
Input format setting	
Enumerator	
<code>DISPLAY_IN_FORMAT_32BITS_ARGB8888</code>	ARGB8888, 32 bits.
<code>DISPLAY_IN_FORMAT_32BITS_RGB888</code>	RGB888, 32 bits.
<code>DISPLAY_IN_FORMAT_16BITS_RGB565</code>	RGB565, 16 bits.
<code>DISPLAY_IN_FORMAT_16BITS_ARGB1555</code>	ARGB1555, 16 bits.
<code>DISPLAY_IN_FORMAT_16BITS_ARGB4444</code>	ARGB4444, 16 bits.
<code>DISPLAY_IN_FORMAT_CLUT8</code>	CLUT8.
<code>DISPLAY_IN_FORMAT_CLUT4</code>	CLUT4.
<code>DISPLAY_IN_FORMAT_CLUT1</code>	CLUT1.

◆ **display\_out\_format\_t**

enum <code>display_out_format_t</code>	
Output format setting	
Enumerator	
<code>DISPLAY_OUT_FORMAT_24BITS_RGB888</code>	RGB888, 24 bits.
<code>DISPLAY_OUT_FORMAT_18BITS_RGB666</code>	RGB666, 18 bits.
<code>DISPLAY_OUT_FORMAT_16BITS_RGB565</code>	RGB565, 16 bits.
<code>DISPLAY_OUT_FORMAT_8BITS_SERIAL</code>	SERIAL, 8 bits.

◆ **display\_endian\_t**

enum <code>display_endian_t</code>	
Data endian select	
Enumerator	
<code>DISPLAY_ENDIAN_LITTLE</code>	Little-endian.
<code>DISPLAY_ENDIAN_BIG</code>	Big-endian.

◆ **display\_color\_order\_t**

enum <code>display_color_order_t</code>	
RGB color order select	
Enumerator	
<code>DISPLAY_COLOR_ORDER_RGB</code>	Color order RGB.
<code>DISPLAY_COLOR_ORDER_BGR</code>	Color order BGR.

◆ **display\_signal\_polarity\_t**

enum <code>display_signal_polarity_t</code>	
Polarity of a signal select	
Enumerator	
<code>DISPLAY_SIGNAL_POLARITY_LOACTIVE</code>	Low active signal.
<code>DISPLAY_SIGNAL_POLARITY_HIACTIVE</code>	High active signal.

◆ **display\_sync\_edge\_t**

enum <code>display_sync_edge_t</code>	
Signal synchronization edge select	
Enumerator	
<code>DISPLAY_SIGNAL_SYNC_EDGE_RISING</code>	Signal is synchronized to rising edge.
<code>DISPLAY_SIGNAL_SYNC_EDGE_FALLING</code>	Signal is synchronized to falling edge.

◆ **display\_fade\_control\_t**

enum <code>display_fade_control_t</code>	
Fading control	
Enumerator	
<code>DISPLAY_FADE_CONTROL_NONE</code>	Applying no fading control.
<code>DISPLAY_FADE_CONTROL_FADEIN</code>	Applying fade-in control.
<code>DISPLAY_FADE_CONTROL_FADEOUT</code>	Applying fade-out control.

◆ **display\_fade\_status\_t**

enum <code>display_fade_status_t</code>	
Fading status	
Enumerator	
<code>DISPLAY_FADE_STATUS_NOT_UNDERWAY</code>	Fade-in/fade-out is not in progress.
<code>DISPLAY_FADE_STATUS_FADING_UNDERWAY</code>	Fade-in or fade-out is in progress.
<code>DISPLAY_FADE_STATUS_PENDING</code>	Fade-in/fade-out is configured but not yet started.

**4.3.12 DOC Interface**[Interfaces](#)**Detailed Description**

Interface for the Data Operation Circuit.

Defines the API and data structures for the DOC implementation of the Data Operation Circuit (DOC) interface.

**Summary**

This module implements the `DOC_API` using the Data Operation Circuit (DOC).

Implemented by: [Data Operation Circuit \(r\\_doc\)](#)

**Data Structures**

```
struct doc\_status\_t
```

```
struct doc\_callback\_args\_t
```

```
struct doc\_cfg\_t
```

```
struct doc\_api\_t
```

```
struct doc\_instance\_t
```

**Typedefs**

```
typedef void doc\_ctrl\_t
```

## Enumerations

enum [doc\\_event\\_t](#)

## Data Structure Documentation

### ◆ [doc\\_status\\_t](#)

struct <a href="#">doc_status_t</a>
DOC status

### ◆ [doc\\_callback\\_args\\_t](#)

struct <a href="#">doc_callback_args_t</a>		
Callback function parameter data.		
Data Fields		
void const *	<a href="#">p_context</a>	Set in <a href="#">doc_api_t::open</a> function in <a href="#">doc_cfg_t</a> .  Placeholder for user data.

### ◆ [doc\\_cfg\\_t](#)

struct <a href="#">doc_cfg_t</a>		
User configuration structure, used in the open function.		
<b>Data Fields</b>		
<a href="#">doc_event_t</a>	<a href="#">event</a>	Select enumerated value from <a href="#">doc_event_t</a> .
<a href="#">uint16_t</a>	<a href="#">doc_data</a>	Initial/reference value for DODSR register.
<a href="#">uint8_t</a>	<a href="#">ipl</a>	DOC interrupt priority.
<a href="#">IRQn_Type</a>	<a href="#">irq</a>	NVIC interrupt number assigned to this instance.

void(*	<a href="#">p_callback</a> )(doc_callback_args_t *p_args)
void const *	<a href="#">p_context</a>

## Field Documentation

### ◆ [p\\_callback](#)

void(\* doc\_cfg\_t::p\_callback) (doc\_callback\_args\_t \*p\_args)

Callback provided when a DOC ISR occurs.

### ◆ [p\\_context](#)

void const\* doc\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in [doc\\_callback\\_args\\_t](#).

### ◆ [doc\\_api\\_t](#)

struct doc\_api\_t

Data Operation Circuit (DOC) API structure. DOC functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*	<a href="#">open</a> )(doc_ctrl_t *const p_ctrl, doc_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(doc_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">statusGet</a> )(doc_ctrl_t *const p_ctrl, doc_status_t *p_status)
fsp_err_t(*	<a href="#">write</a> )(doc_ctrl_t *const p_ctrl, uint16_t data)
fsp_err_t(*	<a href="#">callbackSet</a> )(doc_ctrl_t *const p_api_ctrl, void(*p_callback)(doc_callback_args_t *), void const *const p_context, doc_callback_args_t *const p_callback_memory)

## Field Documentation

◆ **open**

```
fsp_err_t(* doc_api_t::open) (doc_ctrl_t *const p_ctrl, doc_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_DOC\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **close**

```
fsp_err_t(* doc_api_t::close) (doc_ctrl_t *const p_ctrl)
```

Allow the driver to be reconfigured. Will reduce power consumption.

**Implemented as**

- R\_DOC\_Close()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">doc_api_t::open</a> call.
------	--------	--

◆ **statusGet**

```
fsp_err_t(* doc_api_t::statusGet) (doc_ctrl_t *const p_ctrl, doc_status_t *p_status)
```

Gets the result of addition/subtraction and stores it in the provided pointer p\_data.

**Implemented as**

- R\_DOC\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">doc_api_t::open</a> call.
[out]	p_data	Provides the 16 bit result of the addition/subtraction operation at the user defined location.

## ◆ write

```
fsp_err_t(* doc_api_t::write) (doc_ctrl_t *const p_ctrl, uint16_t data)
```

Write to the DODIR register.

**Implemented as**

- R\_DOC\_Write()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">doc_api_t::open</a> call.
[in]	data	data to be written to DOC DODIR register.

## ◆ callbackSet

```
fsp_err_t(* doc_api_t::callbackSet) (doc_ctrl_t *const p_api_ctrl,
void(*p_callback)(doc_callback_args_t *), void const *const p_context, doc_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_DOC\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the DOC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

## ◆ doc\_instance\_t

```
struct doc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">doc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">doc_cfg_t</a> const *	p_cfg	Pointer to the configuration

		structure for this instance.
<code>doc_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `doc_ctrl_t`

```
typedef void doc_ctrl_t
```

DOC control block. Allocate an instance specific control block to pass into the DOC API calls.

#### Implemented as

- `doc_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `doc_event_t`

```
enum doc_event_t
```

Event that can trigger a callback function.

#### Enumerator

<code>DOC_EVENT_COMPARISON_MISMATCH</code>	Comparison of data has resulted in a mismatch.
<code>DOC_EVENT_ADDITION</code>	Addition of data has resulted in a value greater than H'FFFF.
<code>DOC_EVENT_SUBTRACTION</code>	Subtraction of data has resulted in a value less than H'0000.
<code>DOC_EVENT_COMPARISON_MATCH</code>	Comparison of data has resulted in a match.

## 4.3.13 ELC Interface

### Interfaces

#### Detailed Description

Interface for the Event Link Controller.

#### Data Structures

```
struct elc_cfg_t
```

```
struct elc_api_t
```

```
struct elc_instance_t
```

## Typedefs

```
typedef void elc_ctrl_t
```

## Enumerations

```
enum elc_peripheral_t
```

```
enum elc_software_event_t
```

## Data Structure Documentation

### ◆ elc\_cfg\_t

struct elc_cfg_t		
Main configuration structure for the Event Link Controller		
Data Fields		
elc_event_t const	link[ELC_PERIPHERAL_NUM]	Event link register (ELSR) settings.

### ◆ elc\_api\_t

struct elc_api_t	
ELC driver structure. General ELC functions implemented at the HAL layer follow this API.	
<b>Data Fields</b>	
fsp_err_t(*	open )(elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg)
fsp_err_t(*	close )(elc_ctrl_t *const p_ctrl)
fsp_err_t(*	softwareEventGenerate )(elc_ctrl_t *const p_ctrl, elc_software_event_t event_num)
fsp_err_t(*	linkSet )(elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal)
fsp_err_t(*	linkBreak )(elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral)
fsp_err_t(*	enable )(elc_ctrl_t *const p_ctrl)

`fsp_err_t(* disable)(elc_ctrl_t *const p_ctrl)`

## Field Documentation

### ◆ open

`fsp_err_t(* elc_api_t::open)(elc_ctrl_t *const p_ctrl, elc_cfg_t const *const p_cfg)`

Initialize all links in the Event Link Controller.

#### Implemented as

- `R_ELC_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* elc_api_t::close)(elc_ctrl_t *const p_ctrl)`

Disable all links in the Event Link Controller and close the API.

#### Implemented as

- `R_ELC_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
------	---------------------	-------------------------------

### ◆ softwareEventGenerate

`fsp_err_t(* elc_api_t::softwareEventGenerate)(elc_ctrl_t *const p_ctrl, elc_software_event_t event_num)`

Generate a software event in the Event Link Controller.

#### Implemented as

- `R_ELC_SoftwareEventGenerate()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>eventNum</code>	Software event number to be generated.

**◆ linkSet**

```
fsp_err_t(* elc_api_t::linkSet) (elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral, elc_event_t signal)
```

Create a single event link.

**Implemented as**

- R\_ELC\_LinkSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	peripheral	The peripheral block that will receive the event signal.
[in]	signal	The event signal.

**◆ linkBreak**

```
fsp_err_t(* elc_api_t::linkBreak) (elc_ctrl_t *const p_ctrl, elc_peripheral_t peripheral)
```

Break an event link.

**Implemented as**

- R\_ELC\_LinkBreak()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	peripheral	The peripheral that should no longer be linked.

**◆ enable**

```
fsp_err_t(* elc_api_t::enable) (elc_ctrl_t *const p_ctrl)
```

Enable the operation of the Event Link Controller.

**Implemented as**

- R\_ELC\_Enable()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **disable**

```
fsp_err_t(* elc_api_t::disable) (elc_ctrl_t *const p_ctrl)
```

Disable the operation of the Event Link Controller.

**Implemented as**

- [R\\_ELC\\_Disable\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **elc\_instance\_t**

```
struct elc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">elc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">elc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">elc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **elc\_ctrl\_t**

```
typedef void elc_ctrl_t
```

ELC control block. Allocate an instance specific control block to pass into the ELC API calls.

**Implemented as**

- [elc\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **elc\_peripheral\_t**

```
enum elc_peripheral_t
```

Possible peripherals to be linked to event signals (not all available on all MCUs)

### ◆ `elc_software_event_t`

enum <code>elc_software_event_t</code>	
Software event number	
Enumerator	
<code>ELC_SOFTWARE_EVENT_0</code>	Software event 0.
<code>ELC_SOFTWARE_EVENT_1</code>	Software event 1.

## 4.3.14 Ethernet Interface

### Interfaces

#### Detailed Description

Interface for Ethernet functions.

## Summary

The Ethernet interface provides Ethernet functionality. The Ethernet interface supports the following features:

- Transmit/receive processing (Blocking and Non-Blocking)
- Callback function with returned event code
- Magic packet detection mode support
- Auto negotiation support
- Flow control support
- Multicast filtering support

Implemented by:

- [Ethernet \(`r\_ether`\)](#)

#### Data Structures

struct [ether\\_instance\\_descriptor\\_t](#)

struct [ether\\_callback\\_args\\_t](#)

struct [ether\\_cfg\\_t](#)

struct [ether\\_api\\_t](#)

struct [ether\\_instance\\_t](#)

## Typedefs

```
typedef void ether_ctrl_t
```

## Enumerations

```
enum ether_wake_on_lan_t
```

```
enum ether_flow_control_t
```

```
enum ether_multicast_t
```

```
enum ether_promiscuous_t
```

```
enum ether_zerocopy_t
```

```
enum ether_event_t
```

## Data Structure Documentation

### ◆ ether\_instance\_descriptor\_t

```
struct ether_instance_descriptor_t
```

EDMAC descriptor as defined in the hardware manual. Structure must be packed at 1 byte.

### ◆ ether\_callback\_args\_t

```
struct ether_callback_args_t
```

Callback function parameter data

#### Data Fields

uint32_t	channel	Device channel number.
<a href="#">ether_event_t</a>	event	Event code.
uint32_t	status_ecsr	ETHERC status register for interrupt handler.
uint32_t	status_eesr	ETHERC/EDMAC status register for interrupt handler.
void const *	p_context	Placeholder for user data. Set in <a href="#">ether_api_t::open</a> function in <a href="#">ether_cfg_t</a> .

### ◆ ether\_cfg\_t

```
struct ether_cfg_t
```

Configuration parameters.

#### Data Fields

```
uint8_t channel
```

	Channel.
<code>ether_zerocopy_t</code>	<code>zerocopy</code>
	Zero copy enable or disable in Read/Write function.
<code>ether_multicast_t</code>	<code>multicast</code>
	Multicast enable or disable.
<code>ether_promiscuous_t</code>	<code>promiscuous</code>
	Promiscuous mode enable or disable.
<code>ether_flow_control_t</code>	<code>flow_control</code>
	Flow control functionally enable or disable.
<code>ether_padding_t</code>	<code>padding</code>
	Padding length inserted into the received Ethernet frame.
<code>uint32_t</code>	<code>padding_offset</code>
	Offset of the padding inserted into the received Ethernet frame.
<code>uint32_t</code>	<code>broadcast_filter</code>
	Limit of the number of broadcast frames received continuously.
<code>uint8_t *</code>	<code>p_mac_address</code>
	Pointer of MAC address.
<code>ether_instance_descriptor_t *</code>	<code>p_rx_descriptors</code>

	Receive descriptor buffer pool.
<code>ether_instance_descriptor_t *</code>	<code>p_tx_descriptors</code>
	Transmit descriptor buffer pool.
<code>uint8_t</code>	<code>num_tx_descriptors</code>
	Number of transmission descriptor.
<code>uint8_t</code>	<code>num_rx_descriptors</code>
	Number of receive descriptor.
<code>uint8_t **</code>	<code>pp_ether_buffers</code>
	Transmit and receive buffer.
<code>uint32_t</code>	<code>ether_buffer_size</code>
	Size of transmit and receive buffer.
<code>IRQn_Type</code>	<code>irq</code>
	NVIC interrupt number.
<code>uint32_t</code>	<code>interrupt_priority</code>
	NVIC interrupt priority.
<code>void(*</code>	<code>p_callback )(ether_callback_args_t *p_args)</code>
	Callback provided when an ISR occurs.
<code>ether_phy_instance_t const *</code>	<code>p_ether_phy_instance</code>

	Pointer to ETHER_PHY instance.
void const *	<a href="#">p_context</a>
	Placeholder for user data. <a href="#">More...</a>
void const *	<a href="#">p_extend</a>
	Placeholder for user extension.

## Field Documentation

### ◆ [p\\_context](#)

void const\* ether\_cfg\_t::p\_context

Placeholder for user data.

Placeholder for user data. Passed to the user callback in [ether\\_callback\\_args\\_t](#).

### ◆ [ether\\_api\\_t](#)

struct ether\_api\_t

Functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(ether_ctrl_t *const p_api_ctrl, <a href="#">ether_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(ether_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t *const length_bytes)
<a href="#">fsp_err_t</a> (*	<a href="#">bufferRelease</a> )(ether_ctrl_t *const p_api_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">rxBufferUpdate</a> )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t const frame_length)
<a href="#">fsp_err_t</a> (*	<a href="#">linkProcess</a> )(ether_ctrl_t *const p_api_ctrl)

fsp_err_t(*	wakeOnLANEnable )(ether_ctrl_t *const p_api_ctrl)
-------------	---

fsp_err_t(*	txStatusGet )(ether_ctrl_t *const p_api_ctrl, void *const p_buffer_address)
-------------	---

## Field Documentation

### ◆ open

fsp_err_t(* ether_api_t::open) (ether_ctrl_t *const p_api_ctrl, ether_cfg_t const *const p_cfg)
---

Open driver.

#### Implemented as

- R\_ETHER\_Open()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

### ◆ close

fsp_err_t(* ether_api_t::close) (ether_ctrl_t *const p_api_ctrl)
--

Close driver.

#### Implemented as

- R\_ETHER\_Close()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **read**

```
fsp_err_t(* ether_api_t::read) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t *const length_bytes)
```

Read packet if data is available.

**Implemented as**

- R\_ETHER\_Read()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buffer	Pointer to where to store read data.
[in]	length_bytes	Number of bytes in buffer

◆ **bufferRelease**

```
fsp_err_t(* ether_api_t::bufferRelease) (ether_ctrl_t *const p_api_ctrl)
```

Release rx buffer from buffer pool process in zero-copy read operation.

**Implemented as**

- R\_ETHER\_BufferRelease()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **rxBufferUpdate**

```
fsp_err_t(* ether_api_t::rxBufferUpdate) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer)
```

Update the buffer pointer in the current receive descriptor.

**Implemented as**

- R\_ETHER\_RxBufferUpdate()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buffer	New address to write into the rx buffer descriptor.

◆ **write**

`fsp_err_t(* ether_api_t::write) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer, uint32_t const frame_length)`

Write packet.

**Implemented as**

- `R_ETHER_Write()`

**Parameters**

[in]	<code>p_api_ctrl</code>	Pointer to control structure.
[in]	<code>p_buffer</code>	Pointer to data to write.
[in]	<code>frame_length</code>	Send ethernet frame size (without 4 bytes of CRC data size).

◆ **linkProcess**

`fsp_err_t(* ether_api_t::linkProcess) (ether_ctrl_t *const p_api_ctrl)`

Process link.

**Implemented as**

- `R_ETHER_LinkProcess()`

**Parameters**

[in]	<code>p_api_ctrl</code>	Pointer to control structure.
------	-------------------------	-------------------------------

◆ **wakeOnLANEnable**

`fsp_err_t(* ether_api_t::wakeOnLANEnable) (ether_ctrl_t *const p_api_ctrl)`

Enable magic packet detection.

**Implemented as**

- `R_ETHER_WakeOnLANEnable()`

**Parameters**

[in]	<code>p_api_ctrl</code>	Pointer to control structure.
------	-------------------------	-------------------------------

◆ **txStatusGet**

```
fsp_err_t(* ether_api_t::txStatusGet) (ether_ctrl_t *const p_api_ctrl, void *const p_buffer_address)
```

Get the address of the most recently sent buffer.

**Implemented as**

- [R\\_ETHER\\_TxStatusGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[out]	p_buffer_address	Pointer to the address of the most recently sent buffer.

◆ **ether\_instance\_t**

```
struct ether_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">ether_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">ether_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">ether_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **ether\_ctrl\_t**

```
typedef void ether_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [ether\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

## ◆ ether\_wake\_on\_lan\_t

enum ether_wake_on_lan_t	
Wake on LAN	
Enumerator	
ETHER_WAKE_ON_LAN_DISABLE	Disable Wake on LAN.
ETHER_WAKE_ON_LAN_ENABLE	Enable Wake on LAN.

## ◆ ether\_flow\_control\_t

enum ether_flow_control_t	
Flow control functionality	
Enumerator	
ETHER_FLOW_CONTROL_DISABLE	Disable flow control functionality.
ETHER_FLOW_CONTROL_ENABLE	Enable flow control functionality with pause frames.

## ◆ ether\_multicast\_t

enum ether_multicast_t	
Multicast Filter	
Enumerator	
ETHER_MULTICAST_DISABLE	Disable reception of multicast frames.
ETHER_MULTICAST_ENABLE	Enable reception of multicast frames.

## ◆ ether\_promiscuous\_t

enum ether_promiscuous_t	
Promiscuous Mode	
Enumerator	
ETHER_PROMISCUOUS_DISABLE	Only receive packets with current MAC address, multicast, and broadcast.
ETHER_PROMISCUOUS_ENABLE	Receive all packets.

## ◆ ether\_zerocopy\_t

enum ether_zerocopy_t	
Zero copy	
Enumerator	
ETHER_ZEROCOPY_DISABLE	Disable zero copy in Read/Write function.
ETHER_ZEROCOPY_ENABLE	Enable zero copy in Read/Write function.

## ◆ ether\_event\_t

enum ether_event_t	
Event code of callback function	
Enumerator	
ETHER_EVENT_WAKEON_LAN	Magic packet detection event.
ETHER_EVENT_LINK_ON	Link up detection event.
ETHER_EVENT_LINK_OFF	Link down detection event.
ETHER_EVENT_INTERRUPT	Interrupt event.

### 4.3.15 Ethernet PHY Interface

#### Interfaces

#### Detailed Description

Interface for Ethernet PHY functions.

## Summary

The Ethernet PHY module (r\_ether\_phy) provides an API for standard Ethernet PHY communications applications that use the ETHERC peripheral.

The Ethernet PHY interface supports the following features:

- Auto negotiation support
- Flow control support
- Link status check support

Implemented by:

- Ethernet PHY (r\_ether\_phy)

## Data Structures

struct [ether\\_phy\\_cfg\\_t](#)

struct [ether\\_phy\\_api\\_t](#)

struct [ether\\_phy\\_instance\\_t](#)

## Typedefs

typedef void [ether\\_phy\\_ctrl\\_t](#)

## Enumerations

enum [ether\\_phy\\_flow\\_control\\_t](#)

enum [ether\\_phy\\_link\\_speed\\_t](#)

enum [ether\\_phy\\_mii\\_type\\_t](#)

## Data Structure Documentation

### ◆ ether\_phy\_cfg\_t

struct ether_phy_cfg_t		
Configuration parameters.		
Data Fields		
uint8_t	channel	Channel.
uint8_t	phy_lsi_address	Address of PHY-LSI.
uint32_t	phy_reset_wait_time	Wait time for PHY-LSI reboot.
int32_t	mii_bit_access_wait_time	Wait time for MII/RMII access.
<a href="#">ether_phy_flow_control_t</a>	flow_control	Flow control functionally enable or disable.
<a href="#">ether_phy_mii_type_t</a>	mii_type	Interface type is MII or RMII.
void const *	p_context	Placeholder for user data. Passed to the user callback in ether_phy_callback_args_t.
void const *	p_extend	Placeholder for user extension.

### ◆ ether\_phy\_api\_t

struct ether_phy_api_t	
Functions implemented at the HAL layer will follow this API.	

Data Fields		
<code>fsp_err_t(*</code>	<code>open )(ether_phy_ctrl_t *const p_api_ctrl, ether_phy_cfg_t const *const p_cfg)</code>	
<code>fsp_err_t(*</code>	<code>close )(ether_phy_ctrl_t *const p_api_ctrl)</code>	
<code>fsp_err_t(*</code>	<code>startAutoNegotiate )(ether_phy_ctrl_t *const p_api_ctrl)</code>	
<code>fsp_err_t(*</code>	<code>linkPartnerAbilityGet )(ether_phy_ctrl_t *const p_api_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause)</code>	
<code>fsp_err_t(*</code>	<code>linkStatusGet )(ether_phy_ctrl_t *const p_api_ctrl)</code>	
Field Documentation		
◆ <b>open</b>		
<code>fsp_err_t(* ether_phy_api_t::open) (ether_phy_ctrl_t *const p_api_ctrl, ether_phy_cfg_t const *const p_cfg)</code>		
Open driver.		
<b>Implemented as</b>		
◦ <a href="#">R_ETHER_PHY_Open()</a>		
<b>Parameters</b>		
[in]	<code>p_api_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to pin configuration structure.
◆ <b>close</b>		
<code>fsp_err_t(* ether_phy_api_t::close) (ether_phy_ctrl_t *const p_api_ctrl)</code>		
Close driver.		
<b>Implemented as</b>		
◦ <a href="#">R_ETHER_PHY_Close()</a>		
<b>Parameters</b>		
[in]	<code>p_api_ctrl</code>	Pointer to control structure.

### ◆ startAutoNegotiate

`fsp_err_t(* ether_phy_api_t::startAutoNegotiate) (ether_phy_ctrl_t *const p_api_ctrl)`

Start auto negotiation.

#### Implemented as

- [R\\_ETHER\\_PHY\\_StartAutoNegotiate\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

### ◆ linkPartnerAbilityGet

`fsp_err_t(* ether_phy_api_t::linkPartnerAbilityGet) (ether_phy_ctrl_t *const p_api_ctrl, uint32_t *const p_line_speed_duplex, uint32_t *const p_local_pause, uint32_t *const p_partner_pause)`

Get the partner ability.

#### Implemented as

- [R\\_ETHER\\_PHY\\_LinkPartnerAbilityGet\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[out]	p_line_speed_duplex	Pointer to the location of both the line speed and the duplex.
[out]	p_local_pause	Pointer to the location to store the local pause bits.
[out]	p_partner_pause	Pointer to the location to store the partner pause bits.

### ◆ linkStatusGet

`fsp_err_t(* ether_phy_api_t::linkStatusGet) (ether_phy_ctrl_t *const p_api_ctrl)`

Get Link status from PHY-LSI interface.

#### Implemented as

- [R\\_ETHER\\_PHY\\_LinkStatusGet\(\)](#)

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

### ◆ ether\_phy\_instance\_t

`struct ether_phy_instance_t`

This structure encompasses everything that is needed to use an instance of this interface.

Data Fields		
<code>ether_phy_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>ether_phy_cfg_t const *</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>ether_phy_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `ether_phy_ctrl_t`

```
typedef void ether_phy_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

#### Implemented as

- `ether_phy_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `ether_phy_flow_control_t`

```
enum ether_phy_flow_control_t
```

Flow control functionality

#### Enumerator

<code>ETHER_PHY_FLOW_CONTROL_DISABLE</code>	Disable flow control functionality.
<code>ETHER_PHY_FLOW_CONTROL_ENABLE</code>	Enable flow control functionality with pause frames.

## ◆ ether\_phy\_link\_speed\_t

enum ether_phy_link_speed_t	
Link speed	
Enumerator	
ETHER_PHY_LINK_SPEED_NO_LINK	Link is not established.
ETHER_PHY_LINK_SPEED_10H	Link status is 10Mbit/s and half duplex.
ETHER_PHY_LINK_SPEED_10F	Link status is 10Mbit/s and full duplex.
ETHER_PHY_LINK_SPEED_100H	Link status is 100Mbit/s and half duplex.
ETHER_PHY_LINK_SPEED_100F	Link status is 100Mbit/s and full duplex.

## ◆ ether\_phy\_mii\_type\_t

enum ether_phy_mii_type_t	
Media-independent interface	
Enumerator	
ETHER_PHY_MII_TYPE_MII	MII.
ETHER_PHY_MII_TYPE_RMII	RMII.

## 4.3.16 External IRQ Interface

### Interfaces

#### Detailed Description

Interface for detecting external interrupts.

## Summary

The External IRQ Interface is for configuring interrupts to fire when a trigger condition is detected on an external IRQ pin.

The External IRQ Interface can be implemented by:

- [Interrupt Controller Unit \(r\\_icu\)](#)

## Data Structures

struct [external\\_irq\\_callback\\_args\\_t](#)

struct [external\\_irq\\_cfg\\_t](#)

struct [external\\_irq\\_api\\_t](#)

struct [external\\_irq\\_instance\\_t](#)

## Typedefs

typedef void [external\\_irq\\_ctrl\\_t](#)

## Enumerations

enum [external\\_irq\\_trigger\\_t](#)

enum [external\\_irq\\_pclk\\_div\\_t](#)

## Data Structure Documentation

### ◆ external\_irq\_callback\_args\_t

struct <a href="#">external_irq_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	<a href="#">p_context</a>	Placeholder for user data. Set in <a href="#">external_irq_api_t::open</a> function in <a href="#">external_irq_cfg_t</a> .
uint32_t	<a href="#">channel</a>	The physical hardware channel that caused the interrupt.

### ◆ external\_irq\_cfg\_t

struct <a href="#">external_irq_cfg_t</a>		
User configuration structure, used in <code>open</code> function		
<b>Data Fields</b>		
uint8_t	<a href="#">channel</a>	Hardware channel used.
uint8_t	<a href="#">ipl</a>	Interrupt priority.

IRQn_Type	irq
	NVIC interrupt number assigned to this instance.
external_irq_trigger_t	trigger
	Trigger setting.
external_irq_pclk_div_t	pclk_div
	Digital filter clock divisor setting.
bool	filter_enable
	Digital filter enable/disable setting.
void(*	p_callback )(external_irq_callback_args_t *p_args)
void const *	p_context
void const *	p_extend
	External IRQ hardware dependent configuration.

## Field Documentation

### ◆ p\_callback

void(\* external\_irq\_cfg\_t::p\_callback) (external\_irq\_callback\_args\_t \*p\_args)

Callback provided external input trigger occurs.

### ◆ p\_context

void const\* external\_irq\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in external\_irq\_callback\_args\_t.

### ◆ external\_irq\_api\_t

struct external\_irq\_api\_t

External interrupt driver structure. External interrupt functions implemented at the HAL layer will follow this API.

Data Fields		
<code>fsp_err_t(*</code>	<code>open</code>	<code>)(external_irq_ctrl_t *const p_ctrl, external_irq_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>enable</code>	<code>)(external_irq_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>disable</code>	<code>)(external_irq_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>callbackSet</code>	<code>)(external_irq_ctrl_t *const p_api_ctrl, void(*p_callback)(external_irq_callback_args_t *), void const *const p_context, external_irq_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close</code>	<code>)(external_irq_ctrl_t *const p_ctrl)</code>
Field Documentation		
◆ <b>open</b>		
<code>fsp_err_t(* external_irq_api_t::open) (external_irq_ctrl_t *const p_ctrl, external_irq_cfg_t const *const p_cfg)</code>		
Initial configuration.		
<b>Implemented as</b>		
◦ <code>R_ICU_ExternalIrqOpen()</code>		
<b>Parameters</b>		
[out]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Value set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of the structure must be set by user.

◆ **enable**

```
fsp_err_t(* external_irq_api_t::enable) (external_irq_ctrl_t *const p_ctrl)
```

Enable callback when an external trigger condition occurs.

**Implemented as**

- [R\\_ICU\\_ExtrenalIrqEnable\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	---

◆ **disable**

```
fsp_err_t(* external_irq_api_t::disable) (external_irq_ctrl_t *const p_ctrl)
```

Disable callback when external trigger condition occurs.

**Implemented as**

- [R\\_ICU\\_ExtrenalIrqDisable\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	---

◆ **callbackSet**

```
fsp_err_t(* external_irq_api_t::callbackSet) (external_irq_ctrl_t *const p_api_ctrl, void(
*p_callback)(external_irq_callback_args_t *), void const *const p_context,
external_irq_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_ICU\_ExtrenalIrqCallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the External IRQ control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* external_irq_api_t::close) (external_irq_ctrl_t *const p_ctrl)
```

Allow driver to be reconfigured. May reduce power consumption.

**Implemented as**

- R\_ICU\_ExtrenalIrqClose()

**Parameters**

[in]	p_ctrl	Control block set in Open call for this external interrupt.
------	--------	---

◆ **external\_irq\_instance\_t**

```
struct external_irq_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

external_irq_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
external_irq_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.

<code>external_irq_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.
---	--------------------	---

## Typedef Documentation

### ◆ `external_irq_ctrl_t`

typedef void `external_irq_ctrl_t`

External IRQ control block. Allocate an instance specific control block to pass into the external IRQ API calls.

#### Implemented as

- `icu_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `external_irq_trigger_t`

enum `external_irq_trigger_t`

Condition that will trigger an interrupt when detected.

#### Enumerator

<code>EXTERNAL_IRQ_TRIG_FALLING</code>	Falling edge trigger.
<code>EXTERNAL_IRQ_TRIG_RISING</code>	Rising edge trigger.
<code>EXTERNAL_IRQ_TRIG_BOTH_EDGE</code>	Both edges trigger.
<code>EXTERNAL_IRQ_TRIG_LEVEL_LOW</code>	Low level trigger.

### ◆ `external_irq_pclk_div_t`

enum `external_irq_pclk_div_t`

External IRQ input pin digital filtering sample clock divisor settings. The digital filter rejects trigger conditions that are shorter than 3 periods of the filter clock.

#### Enumerator

<code>EXTERNAL_IRQ_PCLK_DIV_BY_1</code>	Filter using PCLK divided by 1.
<code>EXTERNAL_IRQ_PCLK_DIV_BY_8</code>	Filter using PCLK divided by 8.
<code>EXTERNAL_IRQ_PCLK_DIV_BY_32</code>	Filter using PCLK divided by 32.
<code>EXTERNAL_IRQ_PCLK_DIV_BY_64</code>	Filter using PCLK divided by 64.

## 4.3.17 Flash Interface

### Interfaces

#### Detailed Description

Interface for the Flash Memory.

## Summary

The Flash interface provides the ability to read, write, erase, and blank check the code flash and data flash regions.

The Flash interface is implemented by:

- Low-Power Flash Driver (`r_flash_lp`)

#### Data Structures

struct `flash_block_info_t`

struct `flash_regions_t`

struct `flash_info_t`

struct `flash_callback_args_t`

struct `flash_cfg_t`

struct `flash_api_t`

struct `flash_instance_t`

#### Typedefs

typedef void `flash_ctrl_t`

#### Enumerations

enum `flash_result_t`

enum `flash_startup_area_swap_t`

enum `flash_event_t`

enum `flash_id_code_mode_t`

enum `flash_status_t`

## Data Structure Documentation

### ◆ flash\_block\_info\_t

struct flash_block_info_t		
Flash block details stored in factory flash.		
Data Fields		
uint32_t	block_section_st_addr	Starting address for this block section (blocks of this size)
uint32_t	block_section_end_addr	Ending address for this block section (blocks of this size)
uint32_t	block_size	Flash erase block size.
uint32_t	block_size_write	Flash write block size.

### ◆ flash\_regions\_t

struct flash_regions_t		
Flash block details		
Data Fields		
uint32_t	num_regions	Length of block info array.
flash_block_info_t const *	p_block_array	Block info array base address.

### ◆ flash\_info\_t

struct flash_info_t		
Information about the flash blocks		
Data Fields		
flash_regions_t	code_flash	Information about the code flash regions.
flash_regions_t	data_flash	Information about the code flash regions.

### ◆ flash\_callback\_args\_t

struct flash_callback_args_t		
Callback function parameter data		
Data Fields		
flash_event_t	event	Event can be used to identify what caused the callback (flash ready or error).
void const *	p_context	Placeholder for user data. Set in <a href="#">flash_api_t::open</a> function in <a href="#">in::flash_cfg_t</a> .

## ◆ flash\_cfg\_t

struct flash_cfg_t	
FLASH Configuration	
<b>Data Fields</b>	
bool	<a href="#">data_flash_bgo</a>
	True if BGO (Background Operation) is enabled for Data Flash.
void(*)	<a href="#">p_callback</a> (flash_callback_args_t *p_args)
	Callback provided when a Flash interrupt ISR occurs.
void const *	<a href="#">p_extend</a>
	FLASH hardware dependent configuration.
void const *	<a href="#">p_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">flash_callback_args_t</a> .
uint8_t	<a href="#">ipl</a>
	Flash ready interrupt priority.
IRQn_Type	<a href="#">irq</a>
	Flash ready interrupt number.
uint8_t	<a href="#">err_ipl</a>
	Flash error interrupt priority (unused in <a href="#">r_flash_lp</a> )
IRQn_Type	<a href="#">err_irq</a>
	Flash error interrupt number (unused in <a href="#">r_flash_lp</a> )

## ◆ flash\_api\_t

struct flash_api_t	
Shared Interface definition for FLASH	
Data Fields	
fsp_err_t(*)	open )(flash_ctrl_t *const p_ctrl, flash_cfg_t const *const p_cfg)
fsp_err_t(*)	write )(flash_ctrl_t *const p_ctrl, uint32_t const src_address, uint32_t const flash_address, uint32_t const num_bytes)
fsp_err_t(*)	erase )(flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_blocks)
fsp_err_t(*)	blankCheck )(flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_bytes, flash_result_t *const p_blank_check_result)
fsp_err_t(*)	infoGet )(flash_ctrl_t *const p_ctrl, flash_info_t *const p_info)
fsp_err_t(*)	close )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*)	statusGet )(flash_ctrl_t *const p_ctrl, flash_status_t *const p_status)
fsp_err_t(*)	accessWindowSet )(flash_ctrl_t *const p_ctrl, uint32_t const start_addr, uint32_t const end_addr)
fsp_err_t(*)	accessWindowClear )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*)	idCodeSet )(flash_ctrl_t *const p_ctrl, uint8_t const *const p_id_bytes, flash_id_code_mode_t mode)
fsp_err_t(*)	reset )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*)	updateFlashClockFreq )(flash_ctrl_t *const p_ctrl)
fsp_err_t(*)	startupAreaSelect )(flash_ctrl_t *const p_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)

<code>fsp_err_t(*</code>	<code>bankSwap )(flash_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(flash_ctrl_t *const p_api_ctrl, void(*p_callback)(flash_callback_args_t *), void const *const p_context, flash_callback_args_t *const p_callback_memory)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* flash_api_t::open) (flash_ctrl_t *const p_ctrl, flash_cfg_t const *const p_cfg)`

Open FLASH device.

#### Implemented as

- `R_FLASH_LP_Open()`
- `R_FLASH_HP_Open()`

#### Parameters

[out]	<code>p_ctrl</code>	Pointer to FLASH device control. Must be declared by user. Value set here.
[in]	<code>flash_cfg_t</code>	Pointer to FLASH configuration structure. All elements of this structure must be set by the user.

## ◆ write

```
fsp_err_t(* flash_api_t::write) (flash_ctrl_t *const p_ctrl, uint32_t const src_address, uint32_t const flash_address, uint32_t const num_bytes)
```

Write FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Write()
- R\_FLASH\_HP\_Write()

**Parameters**

[in]	p_ctrl	Control for the FLASH device context.
[in]	src_address	Address of the buffer containing the data to write to Flash.
[in]	flash_address	Code Flash or Data Flash address to write. The address must be on a programming line boundary.
[in]	num_bytes	The number of bytes to write. This number must be a multiple of the programming size. For Code Flash this is FLASH_MIN_PGM_SIZE_CF. For Data Flash this is FLASH_MIN_PGM_SIZE_DF.

**Warning**

Specifying a number that is not a multiple of the programming size will result in SF\_FLASH\_ERR\_BYTES being returned and no data written.

◆ **erase**

```
fsp_err_t(* flash_api_t::erase) (flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t const num_blocks)
```

Erase FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Erase()
- R\_FLASH\_HP\_Erase()

**Parameters**

[in]	p_ctrl	Control for the FLASH device.
[in]	address	The block containing this address is the first block erased.
[in]	num_blocks	Specifies the number of blocks to be erased, the starting block determined by the block_erase_address.

◆ **blankCheck**

```
fsp_err_t(* flash_api_t::blankCheck) (flash_ctrl_t *const p_ctrl, uint32_t const address, uint32_t
const num_bytes, flash_result_t *const p_blank_check_result)
```

Blank check FLASH device.

**Implemented as**

- R\_FLASH\_LP\_BlankCheck()
- R\_FLASH\_HP\_BlankCheck()

**Parameters**

[in]	p_ctrl	Control for the FLASH device context.
[in]	address	The starting address of the Flash area to blank check.
[in]	num_bytes	Specifies the number of bytes that need to be checked. See the specific handler for details.
[out]	p_blank_check_result	Pointer that will be populated by the API with the results of the blank check operation in non-BGO (blocking) mode. In this case the blank check operation completes here and the result is returned. In Data Flash BGO mode the blank check operation is only started here and the result obtained later when the supplied callback routine is called. In this case FLASH_RESULT_BGO_ACTIVE will be returned in p_blank_check_result.

## ◆ infoGet

```
fsp_err_t(* flash_api_t::infoGet) (flash_ctrl_t *const p_ctrl, flash_info_t *const p_info)
```

Close FLASH device.

**Implemented as**

- R\_FLASH\_LP\_InfoGet()
- R\_FLASH\_HP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
[out]	p_info	Pointer to FLASH info structure.

## ◆ close

```
fsp_err_t(* flash_api_t::close) (flash_ctrl_t *const p_ctrl)
```

Close FLASH device.

**Implemented as**

- R\_FLASH\_LP\_Close()
- R\_FLASH\_HP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
------	--------	----------------------------------

## ◆ statusGet

```
fsp_err_t(* flash_api_t::statusGet) (flash_ctrl_t *const p_ctrl, flash_status_t *const p_status)
```

Get Status for FLASH device.

**Implemented as**

- R\_FLASH\_LP\_StatusGet()
- R\_FLASH\_HP\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
[out]	p_status	Pointer to the current flash status.

### ◆ accessWindowSet

`fsp_err_t(* flash_api_t::accessWindowSet) (flash_ctrl_t *const p_ctrl, uint32_t const start_addr, uint32_t const end_addr)`

Set Access Window for FLASH device.

#### Implemented as

- `R_FLASH_LP_AccessWindowSet()`
- `R_FLASH_HP_AccessWindowSet()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
[in]	start_addr	Determines the Starting block for the Code Flash access window.
[in]	end_addr	Determines the Ending block for the Code Flash access window. This address will not be within the access window.

### ◆ accessWindowClear

`fsp_err_t(* flash_api_t::accessWindowClear) (flash_ctrl_t *const p_ctrl)`

Clear any existing Code Flash access window for FLASH device.

#### Implemented as

- `R_FLASH_LP_AccessWindowClear()`
- `R_FLASH_HP_AccessWindowClear()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
[in]	start_addr	Determines the Starting block for the Code Flash access window.
[in]	end_addr	Determines the Ending block for the Code Flash access window.

◆ **idCodeSet**

```
fsp_err_t(* flash_api_t::idCodeSet) (flash_ctrl_t *const p_ctrl, uint8_t const *const p_id_bytes,
flash_id_code_mode_t mode)
```

Set ID Code for FLASH device. Setting the ID code can restrict access to the device. The ID code will be required to connect to the device. Bits 126 and 127 are set based on the mode.

For example, `uint8_t id_bytes[] = {0x00, 0x11, 0x22, 0x33, 0x44, 0x55, 0x66, 0x77, 0x88, 0x99, 0xaa, 0xbb, 0xcc, 0xdd, 0xee, 0x00};` with mode `FLASH_ID_CODE_MODE_LOCKED_WITH_ALL_ERASE_SUPPORT` will result in an ID code of `00112233445566778899aabbccddeec0`

With mode `FLASH_ID_CODE_MODE_LOCKED`, it will result in an ID code of `00112233445566778899aabbccdee80`

**Implemented as**

- `R_FLASH_LP_IdCodeSet()`
- `R_FLASH_HP_IdCodeSet()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to FLASH device control.
[in]	<code>p_id_bytes</code>	Ponter to the ID Code to be written.
[in]	<code>mode</code>	Mode used for checking the ID code.

◆ **reset**

```
fsp_err_t(* flash_api_t::reset) (flash_ctrl_t *const p_ctrl)
```

Reset function for FLASH device.

**Implemented as**

- `R_FLASH_LP_Reset()`
- `R_FLASH_HP_Reset()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to FLASH device control.
------	---------------------	----------------------------------

### ◆ updateFlashClockFreq

`fsp_err_t(* flash_api_t::updateFlashClockFreq) (flash_ctrl_t *const p_ctrl)`

Update Flash clock frequency (FCLK) and recalculate timeout values

#### Implemented as

- `R_FLASH_LP_UpdateFlashClockFreq()`
- `R_FLASH_HP_UpdateFlashClockFreq()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
------	--------	----------------------------------

### ◆ startupAreaSelect

`fsp_err_t(* flash_api_t::startupAreaSelect) (flash_ctrl_t *const p_ctrl, flash_startup_area_swap_t swap_type, bool is_temporary)`

Select which block - Default (Block 0) or Alternate (Block 1) is used as the start-up area block.

#### Implemented as

- `R_FLASH_LP_StartUpAreaSelect()`
- `R_FLASH_HP_StartUpAreaSelect()`

#### Parameters

[in]	p_ctrl	Pointer to FLASH device control.
[in]	swap_type	FLASH_STARTUP_AREA_BLOCK0, FLASH_STARTUP_AREA_BLOCK1 or FLASH_STARTUP_AREA_BTFLG.
[in]	is_temporary	True or false. See table below.

swap_type	is_temporary	Operation
FLASH_STARTUP_AREA_BLOCK0	false	On next reset Startup area will be Block 0.
FLASH_STARTUP_AREA_BLOCK1	true	Startup area is immediately, but temporarily switched to Block 1.
FLASH_STARTUP_AREA_BTFLG	true	Startup area is immediately, but temporarily switched to the Block determined by the Configuration BTFLG.

◆ **bankSwap**

```
fsp_err_t(* flash_api_t::bankSwap) (flash_ctrl_t *const p_ctrl)
```

Swap the bank used as the startup area. Only valid in dual bank mode.

**Implemented as**

- [R\\_FLASH\\_HP\\_BankSwap\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to FLASH device control.
------	--------	----------------------------------

◆ **callbackSet**

```
fsp_err_t(* flash_api_t::callbackSet) (flash_ctrl_t *const p_api_ctrl,
void(*p_callback)(flash_callback_args_t *), void const *const p_context, flash_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_FLASH\\_HP\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">flash_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **flash\_instance\_t**

```
struct flash_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">flash_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">flash_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.

<code>flash_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.
----------------------------------	--------------------	---

## Typedef Documentation

### ◆ `flash_ctrl_t`

```
typedef void flash_ctrl_t
```

Flash control block. Allocate an instance specific control block to pass into the flash API calls.

#### Implemented as

- `flash_lp_instance_ctrl_t`
- `flash_hp_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `flash_result_t`

```
enum flash_result_t
```

Result type for certain operations

#### Enumerator

<code>FLASH_RESULT_BLANK</code>	Return status for Blank Check Function.
<code>FLASH_RESULT_NOT_BLANK</code>	Return status for Blank Check Function.
<code>FLASH_RESULT_BGO_ACTIVE</code>	Flash is configured for BGO mode. Result is returned in callback.

### ◆ `flash_startup_area_swap_t`

```
enum flash_startup_area_swap_t
```

Parameter for specifying the startup area swap being requested by `startupAreaSelect()`

#### Enumerator

<code>FLASH_STARTUP_AREA_BTFLG</code>	Startup area will be set based on the value of the BTFLG.
<code>FLASH_STARTUP_AREA_BLOCK0</code>	Startup area will be set to Block 0.
<code>FLASH_STARTUP_AREA_BLOCK1</code>	Startup area will be set to Block 1.

◆ **flash\_event\_t**

enum <code>flash_event_t</code>	
Event types returned by the ISR callback when used in Data Flash BGO mode	
Enumerator	
<code>FLASH_EVENT_ERASE_COMPLETE</code>	Erase operation successfully completed.
<code>FLASH_EVENT_WRITE_COMPLETE</code>	Write operation successfully completed.
<code>FLASH_EVENT_BLANK</code>	Blank check operation successfully completed. Specified area is blank.
<code>FLASH_EVENT_NOT_BLANK</code>	Blank check operation successfully completed. Specified area is NOT blank.
<code>FLASH_EVENT_ERR_DF_ACCESS</code>	Data Flash operation failed. Can occur when writing an unerased section.
<code>FLASH_EVENT_ERR_CF_ACCESS</code>	Code Flash operation failed. Can occur when writing an unerased section.
<code>FLASH_EVENT_ERR_CMD_LOCKED</code>	Operation failed, FCU is in Locked state (often result of an illegal command)
<code>FLASH_EVENT_ERR_FAILURE</code>	Erase or Program Operation failed.
<code>FLASH_EVENT_ERR_ONE_BIT</code>	A 1-bit error has been corrected when reading the flash memory area by the sequencer.

◆ **flash\_id\_code\_mode\_t**

enum <code>flash_id_code_mode_t</code>	
ID Code Modes for writing to ID code registers	
Enumerator	
<code>FLASH_ID_CODE_MODE_UNLOCKED</code>	ID code is ignored.
<code>FLASH_ID_CODE_MODE_LOCKED_WITH_ALL_ERASE_SUPPORT</code>	ID code is checked. All erase is available.
<code>FLASH_ID_CODE_MODE_LOCKED</code>	ID code is checked.

◆ **flash\_status\_t**

enum flash_status_t	
Flash status	
Enumerator	
FLASH_STATUS_IDLE	The flash is idle.
FLASH_STATUS_BUSY	The flash is currently processing a command.

**4.3.18 I2C Master Interface**[Interfaces](#)**Detailed Description**

Interface for I2C master communication.

**Summary**

The I2C master interface provides a common API for I2C HAL drivers. The I2C master interface supports:

- Interrupt driven transmit/receive processing
- Callback function support which can return an event code

Implemented by:

- [I2C Master on IIC \(r\\_iic\\_master\)](#)

**Data Structures**

```
struct i2c_master_callback_args_t
```

```
struct i2c_master_status_t
```

```
struct i2c_master_cfg_t
```

```
struct i2c_master_api_t
```

```
struct i2c_master_instance_t
```

**Typedefs**

```
typedef void i2c_master_ctrl_t
```

## Enumerations

enum [i2c\\_master\\_rate\\_t](#)

enum [i2c\\_master\\_addr\\_mode\\_t](#)

enum [i2c\\_master\\_event\\_t](#)

## Data Structure Documentation

### ◆ [i2c\\_master\\_callback\\_args\\_t](#)

struct <a href="#">i2c_master_callback_args_t</a>		
I2C callback parameter definition		
Data Fields		
void const *	<a href="#">p_context</a>	Pointer to user-provided context.
<a href="#">i2c_master_event_t</a>	<a href="#">event</a>	Event code.

### ◆ [i2c\\_master\\_status\\_t](#)

struct <a href="#">i2c_master_status_t</a>		
I2C status indicators		
Data Fields		
bool	<a href="#">open</a>	True if driver is open.

### ◆ [i2c\\_master\\_cfg\\_t](#)

struct <a href="#">i2c_master_cfg_t</a>		
I2C configuration block		
<b>Data Fields</b>		
uint8_t	<a href="#">channel</a>	Identifier recognizable by implementation. <a href="#">More...</a>
<a href="#">i2c_master_rate_t</a>	<a href="#">rate</a>	Device's maximum clock rate from enum <a href="#">i2c_rate_t</a> .
uint32_t	<a href="#">slave</a>	The address of the slave device.

<code>i2c_master_addr_mode_t</code>	<code>addr_mode</code>
	Indicates how slave fields should be interpreted.
<code>uint8_t</code>	<code>ipl</code>
	Interrupt priority level. Same for RXI, TXI, TEI and ERI.
<code>IRQn_Type</code>	<code>rx_irq</code>
	Receive IRQ number.
<code>IRQn_Type</code>	<code>tx_irq</code>
	Transmit IRQ number.
<code>IRQn_Type</code>	<code>te_irq</code>
	Transmit end IRQ number.
<code>IRQn_Type</code>	<code>eri_irq</code>
	Error IRQ number.
<code>transfer_instance_t const *</code>	<code>p_transfer_tx</code>
	DTC instance for I2C transmit. Set to NULL if unused. <a href="#">More...</a>
<code>transfer_instance_t const *</code>	<code>p_transfer_rx</code>
	DTC instance for I2C receive. Set to NULL if unused.
<code>void(*</code>	<code>p_callback</code> <code>)(i2c_master_callback_args_t *p_args)</code>
	Pointer to callback function. <a href="#">More...</a>
<code>void const *</code>	<code>p_context</code>

	Pointer to the user-provided context.
void const *	<a href="#">p_extend</a>
	Any configuration data needed by the hardware. <a href="#">More...</a>
<b>Field Documentation</b>	
◆ <b>channel</b>	
uint8_t i2c_master_cfg_t::channel	
Identifier recognizable by implementation. Generic configuration	
◆ <b>p_transfer_tx</b>	
<a href="#">transfer_instance_t</a> const* i2c_master_cfg_t::p_transfer_tx	
DTC instance for I2C transmit.Set to NULL if unused. DTC support	
◆ <b>p_callback</b>	
void(* i2c_master_cfg_t::p_callback) ( <a href="#">i2c_master_callback_args_t</a> *p_args)	
Pointer to callback function. Parameters to control software behavior	
◆ <b>p_extend</b>	
void const* i2c_master_cfg_t::p_extend	
Any configuration data needed by the hardware. Implementation-specific configuration	
◆ <b>i2c_master_api_t</b>	
struct i2c_master_api_t	
Interface definition for I2C access as master	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(i2c_master_ctrl_t *const p_ctrl, i2c_master_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)

<code>fsp_err_t(*</code>	<code>write</code> )( <code>i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart</code> )
<code>fsp_err_t(*</code>	<code>abort</code> )( <code>i2c_master_ctrl_t *const p_ctrl</code> )
<code>fsp_err_t(*</code>	<code>slaveAddressSet</code> )( <code>i2c_master_ctrl_t *const p_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode</code> )
<code>fsp_err_t(*</code>	<code>callbackSet</code> )( <code>i2c_master_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_master_callback_args_t *), void const *const p_context, i2c_master_callback_args_t *const p_callback_memory</code> )
<code>fsp_err_t(*</code>	<code>statusGet</code> )( <code>i2c_master_ctrl_t *const p_api_ctrl, i2c_master_status_t *p_status</code> )
<code>fsp_err_t(*</code>	<code>close</code> )( <code>i2c_master_ctrl_t *const p_ctrl</code> )

## Field Documentation

### ◆ open

`fsp_err_t(* i2c_master_api_t::open)` (`i2c_master_ctrl_t *const p_ctrl, i2c_master_cfg_t const *const p_cfg`)

Opens the I2C Master driver and initializes the hardware.

### Implemented as

- `R_IIC_MASTER_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements are set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

## ◆ read

```
fsp_err_t(* i2c_master_api_t::read) (i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes, bool const restart)
```

Performs a read operation on an I2C Master device.

**Implemented as**

- R\_IIC\_MASTER\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	p_dest	Pointer to the location to store read data.
[in]	bytes	Number of bytes to read.
[in]	restart	Specify if the restart condition should be issued after reading.

## ◆ write

```
fsp_err_t(* i2c_master_api_t::write) (i2c_master_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes, bool const restart)
```

Performs a write operation on an I2C Master device.

**Implemented as**

- R\_IIC\_MASTER\_Write()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	p_src	Pointer to the location to get write data from.
[in]	bytes	Number of bytes to write.
[in]	restart	Specify if the restart condition should be issued after writing.

◆ **abort**

```
fsp_err_t(* i2c_master_api_t::abort) (i2c_master_ctrl_t *const p_ctrl)
```

Performs a reset of the peripheral.

**Implemented as**

- R\_IIC\_MASTER\_Abort()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
------	--------	--

◆ **slaveAddressSet**

```
fsp_err_t(* i2c_master_api_t::slaveAddressSet) (i2c_master_ctrl_t *const p_ctrl, uint32_t const slave, i2c_master_addr_mode_t const addr_mode)
```

Sets address of the slave device without reconfiguring the bus.

**Implemented as**

- R\_IIC\_MASTER\_SlaveAddressSet()

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
[in]	slave_address	Address of the slave device.
[in]	address_mode	Addressing mode.

### ◆ callbackSet

```
fsp_err_t(* i2c_master_api_t::callbackSet) (i2c_master_ctrl_t *const p_api_ctrl,
void(*p_callback)(i2c_master_callback_args_t*), void const *const p_context,
i2c_master_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- R\_IIC\_MASTER\_CallbackSet()

#### Parameters

[in]	p_ctrl	Pointer to the IIC Master control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ statusGet

```
fsp_err_t(* i2c_master_api_t::statusGet) (i2c_master_ctrl_t *const p_api_ctrl, i2c_master_status_t *p_status)
```

Gets the status of the configured I2C device.

#### Implemented as

- R\_IIC\_MASTER\_StatusGet()

#### Parameters

[in]	p_ctrl	Pointer to the IIC Master control block.
[out]	p_status	Pointer to store current status.

◆ **close**

```
fsp_err_t(* i2c_master_api_t::close) (i2c_master_ctrl_t *const p_ctrl)
```

Closes the driver and releases the I2C Master device.

**Implemented as**

- [R\\_IIC\\_MASTER\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in i2c_api_master_t::open call.
------	--------	--

◆ **i2c\_master\_instance\_t**

```
struct i2c_master_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

i2c_master_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
i2c_master_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
i2c_master_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **i2c\_master\_ctrl\_t**

```
typedef void i2c_master_ctrl_t
```

I2C control block. Allocate an instance specific control block to pass into the I2C API calls.

**Implemented as**

- [iic\\_master\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **i2c\_master\_rate\_t**

enum i2c_master_rate_t	
Communication speed options	
Enumerator	
I2C_MASTER_RATE_STANDARD	100 kHz
I2C_MASTER_RATE_FAST	400 kHz
I2C_MASTER_RATE_FASTPLUS	1 MHz

◆ **i2c\_master\_addr\_mode\_t**

enum i2c_master_addr_mode_t	
Addressing mode options	
Enumerator	
I2C_MASTER_ADDR_MODE_7BIT	Use 7-bit addressing mode.
I2C_MASTER_ADDR_MODE_10BIT	Use 10-bit addressing mode.

◆ **i2c\_master\_event\_t**

enum i2c_master_event_t	
Callback events	
Enumerator	
I2C_MASTER_EVENT_ABORTED	A transfer was aborted.
I2C_MASTER_EVENT_RX_COMPLETE	A receive operation was completed successfully.
I2C_MASTER_EVENT_TX_COMPLETE	A transmit operation was completed successfully.

**4.3.19 I2C Slave Interface**[Interfaces](#)**Detailed Description**

Interface for I2C slave communication.

## Summary

The I2C slave interface provides a common API for I2C HAL drivers. The I2C slave interface supports:

- Interrupt driven transmit/receive processing
- Callback function support which returns a event codes

Implemented by:

- [I2C Slave on IIC \(r\\_iic\\_slave\)](#)

### Data Structures

struct [i2c\\_slave\\_callback\\_args\\_t](#)

struct [i2c\\_slave\\_cfg\\_t](#)

struct [i2c\\_slave\\_api\\_t](#)

struct [i2c\\_slave\\_instance\\_t](#)

### Typedefs

typedef void [i2c\\_slave\\_ctrl\\_t](#)

### Enumerations

enum [i2c\\_slave\\_rate\\_t](#)

enum [i2c\\_slave\\_addr\\_mode\\_t](#)

enum [i2c\\_slave\\_event\\_t](#)

### Data Structure Documentation

#### ◆ [i2c\\_slave\\_callback\\_args\\_t](#)

struct <a href="#">i2c_slave_callback_args_t</a>		
I2C callback parameter definition		
Data Fields		
void const *	<a href="#">p_context</a>	Pointer to user-provided context.
<a href="#">uint32_t</a>	<a href="#">bytes</a>	Number of received/transmitted bytes in buffer.
<a href="#">i2c_slave_event_t</a>	<a href="#">event</a>	Event code.

#### ◆ [i2c\\_slave\\_cfg\\_t](#)

struct i2c_slave_cfg_t	
I2C configuration block	
<b>Data Fields</b>	
uint8_t	channel
	Identifier recognizable by implementation. <a href="#">More...</a>
i2c_slave_rate_t	rate
	Device's maximum clock rate from enum i2c_rate_t.
uint16_t	slave
	The address of the slave device.
i2c_slave_addr_mode_t	addr_mode
	Indicates how slave fields should be interpreted.
bool	general_call_enable
	Allow a General call from master.
IRQn_Type	rx_irq
	Receive IRQ number.
IRQn_Type	tx_irq
	Transmit IRQ number.
IRQn_Type	tei_irq
	Transmit end IRQ number.
IRQn_Type	eri_irq
	Error IRQ number.

uint8_t	<a href="#">ipl</a>
	Interrupt priority level for RXI, TXI and TER interrupts.
uint8_t	<a href="#">eri_ipl</a>
	Interrupt priority level for ERI interrupt.
bool	<a href="#">clock_stretching_enable</a>
	Low Hold SCL during reception for the period between the 9th and the 1st clock cycle.
void(*	<a href="#">p_callback</a> )(i2c_slave_callback_args_t *p_args)
	Pointer to callback function. <a href="#">More...</a>
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.
void const *	<a href="#">p_extend</a>
	Any configuration data needed by the hardware. <a href="#">More...</a>

## Field Documentation

### ◆ channel

uint8\_t i2c\_slave\_cfg\_t::channel

Identifier recognizable by implementation.

Generic configuration

### ◆ p\_callback

void(\* i2c\_slave\_cfg\_t::p\_callback) (i2c\_slave\_callback\_args\_t \*p\_args)

Pointer to callback function.

Parameters to control software behavior

◆ **p\_extend**

```
void const* i2c_slave_cfg_t::p_extend
```

Any configuration data needed by the hardware.

Implementation-specific configuration

◆ **i2c\_slave\_api\_t**

```
struct i2c_slave_api_t
```

Interface definition for I2C access as slave

**Data Fields**

<code>fsp_err_t(*</code>	<code>open</code> )(i2c_slave_ctrl_t *const p_ctrl, i2c_slave_cfg_t const *const p_cfg)
--------------------------	---

<code>fsp_err_t(*</code>	<code>read</code> )(i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
--------------------------	--

<code>fsp_err_t(*</code>	<code>write</code> )(i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes)
--------------------------	--

<code>fsp_err_t(*</code>	<code>callbackSet</code> )(i2c_slave_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_slave_callback_args_t *), void const *const p_context, i2c_slave_callback_args_t *const p_callback_memory)
--------------------------	---

<code>fsp_err_t(*</code>	<code>close</code> )(i2c_slave_ctrl_t *const p_ctrl)
--------------------------	--

**Field Documentation**

## ◆ open

```
fsp_err_t(* i2c_slave_api_t::open) (i2c_slave_ctrl_t *const p_ctrl, i2c_slave_cfg_t const *const p_cfg)
```

Opens the I2C Slave driver and initializes the hardware.

**Implemented as**

- R\_IIC\_SLAVE\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements are set here.
[in]	p_cfg	Pointer to configuration structure.

## ◆ read

```
fsp_err_t(* i2c_slave_api_t::read) (i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

Performs a read operation on an I2C Slave device.

**Implemented as**

- R\_IIC\_SLAVE\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control block set in <code>i2c_slave_api_t::open</code> call.
[in]	p_dest	Pointer to the location to store read data.
[in]	bytes	Number of bytes to read.

## ◆ write

```
fsp_err_t(* i2c_slave_api_t::write) (i2c_slave_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes)
```

Performs a write operation on an I2C Slave device.

**Implemented as**

- R\_IIC\_SLAVE\_Write()

**Parameters**

[in]	p_ctrl	Pointer to control block set in <code>i2c_slave_api_t::open</code> call.
[in]	p_src	Pointer to the location to get write data from.
[in]	bytes	Number of bytes to write.

## ◆ callbackSet

```
fsp_err_t(* i2c_slave_api_t::callbackSet) (i2c_slave_ctrl_t *const p_api_ctrl, void(*p_callback)(i2c_slave_callback_args_t *), void const *const p_context, i2c_slave_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_IIC\_SLAVE\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the IIC Slave control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* i2c_slave_api_t::close) (i2c_slave_ctrl_t *const p_ctrl)
```

Closes the driver and releases the I2C Slave device.

**Implemented as**

- [R\\_IIC\\_SLAVE\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block set in <a href="#">i2c_slave_api_t::open</a> call.
------	--------	---

◆ **i2c\_slave\_instance\_t**

```
struct i2c_slave_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">i2c_slave_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">i2c_slave_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">i2c_slave_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **i2c\_slave\_ctrl\_t**

```
typedef void i2c_slave_ctrl_t
```

I2C control block. Allocate an instance specific control block to pass into the I2C API calls.

**Implemented as**

- [iic\\_slave\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **i2c\_slave\_rate\_t**

enum i2c_slave_rate_t	
Communication speed options	
Enumerator	
I2C_SLAVE_RATE_STANDARD	100 kHz
I2C_SLAVE_RATE_FAST	400 kHz
I2C_SLAVE_RATE_FASTPLUS	1 MHz

◆ **i2c\_slave\_addr\_mode\_t**

enum i2c_slave_addr_mode_t	
Addressing mode options	
Enumerator	
I2C_SLAVE_ADDR_MODE_7BIT	Use 7-bit addressing mode.
I2C_SLAVE_ADDR_MODE_10BIT	Use 10-bit addressing mode.

◆ **i2c\_slave\_event\_t**

enum i2c_slave_event_t	
Callback events	
Enumerator	
I2C_SLAVE_EVENT_ABORTED	A transfer was aborted.
I2C_SLAVE_EVENT_RX_COMPLETE	A receive operation was completed successfully.
I2C_SLAVE_EVENT_TX_COMPLETE	A transmit operation was completed successfully.
I2C_SLAVE_EVENT_RX_REQUEST	A read operation expected from slave. Detected a write from master.
I2C_SLAVE_EVENT_TX_REQUEST	A write operation expected from slave. Detected a read from master.
I2C_SLAVE_EVENT_RX_MORE_REQUEST	A read operation expected from slave. Master sends out more data than configured to be read in slave.
I2C_SLAVE_EVENT_TX_MORE_REQUEST	A write operation expected from slave. Master requests more data than configured to be written by slave.
I2C_SLAVE_EVENT_GENERAL_CALL	General Call address received from Master. Detected a write from master.

**4.3.20 I2S Interface**[Interfaces](#)**Detailed Description**

Interface for I2S audio communication.

**Summary**

The I2S (Inter-IC Sound) interface provides APIs and definitions for I2S audio communication.

**Known Implementations**

## Serial Sound Interface (r\_ssi)

**Data Structures**struct [i2s\\_callback\\_args\\_t](#)struct [i2s\\_status\\_t](#)struct [i2s\\_cfg\\_t](#)struct [i2s\\_api\\_t](#)struct [i2s\\_instance\\_t](#)**Typedefs**typedef void [i2s\\_ctrl\\_t](#)**Enumerations**enum [i2s\\_pcm\\_width\\_t](#)enum [i2s\\_word\\_length\\_t](#)enum [i2s\\_event\\_t](#)enum [i2s\\_mode\\_t](#)enum [i2s\\_mute\\_t](#)enum [i2s\\_ws\\_continue\\_t](#)enum [i2s\\_state\\_t](#)**Data Structure Documentation**◆ **[i2s\\_callback\\_args\\_t](#)**

struct <a href="#">i2s_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	<a href="#">p_context</a>	Placeholder for user data. Set in <a href="#">i2s_api_t::open</a> function in <a href="#">i2s_cfg_t</a> .
<a href="#">i2s_event_t</a>	<a href="#">event</a>	The event can be used to identify what caused the callback (overflow or error).

◆ **[i2s\\_status\\_t](#)**

struct i2s_status_t		
I2S status.		
Data Fields		
i2s_state_t	state	Current I2S state.

## ◆ i2s\_cfg\_t

struct i2s_cfg_t		
User configuration structure, used in open function		
<b>Data Fields</b>		
uint32_t	channel	
i2s_pcm_width_t	pcm_width	Audio PCM data width.
i2s_word_length_t	word_length	Audio word length, bits must be $\geq$ i2s_cfg_t::pcm_width bits.
i2s_ws_continue_t	ws_continue	Whether to continue WS transmission during idle state.
i2s_mode_t	operating_mode	Master or slave mode.
transfer_instance_t const *	p_transfer_tx	
transfer_instance_t const *	p_transfer_rx	
void(*	p_callback	(i2s_callback_args_t *p_args)
void const *	p_context	
void const *	p_extend	

	Extension parameter for hardware specific settings.
uint8_t	<a href="#">rx_ipl</a>
	Receive interrupt priority.
uint8_t	<a href="#">tx_ipl</a>
	Transmit interrupt priority.
uint8_t	<a href="#">idle_err_ipl</a>
	Idle/Error interrupt priority.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit IRQ number.
IRQn_Type	<a href="#">rx_irq</a>
	Receive IRQ number.
IRQn_Type	<a href="#">int_irq</a>
	Idle/Error IRQ number.

## Field Documentation

### ◆ channel

uint32\_t i2s\_cfg\_t::channel

Select a channel corresponding to the channel number of the hardware.

### ◆ p\_transfer\_tx

transfer\_instance\_t const\* i2s\_cfg\_t::p\_transfer\_tx

To use DTC during write, link a DTC instance here. Set to NULL if unused.

◆ **p\_transfer\_rx**

```
transfer_instance_t const* i2s_cfg_t::p_transfer_rx
```

To use DTC during read, link a DTC instance here. Set to NULL if unused.

◆ **p\_callback**

```
void(* i2s_cfg_t::p_callback)(i2s_callback_args_t *p_args)
```

Callback provided when an I2S ISR occurs. Set to NULL for no CPU interrupt.

◆ **p\_context**

```
void const* i2s_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in `i2s_callback_args_t`.

◆ **i2s\_api\_t**

```
struct i2s_api_t
```

I2S functions implemented at the HAL layer will follow this API.

**Data Fields**

<code>fsp_err_t(*</code>	<code>open</code> )( <code>i2s_ctrl_t *const p_ctrl, i2s_cfg_t const *const p_cfg</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>stop</code> )( <code>i2s_ctrl_t *const p_ctrl</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>mute</code> )( <code>i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>write</code> )( <code>i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>read</code> )( <code>i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>writeRead</code> )( <code>i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest, uint32_t const bytes</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>statusGet</code> )( <code>i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status</code> )
--------------------------	---

<code>fsp_err_t(*</code>	<code>close</code> )( <code>i2s_ctrl_t *const p_ctrl</code> )
--------------------------	---

<code>fsp_err_t(*</code>	<code>callbackSet</code> )( <code>i2s_ctrl_t *const p_api_ctrl, void(*p_callback)(i2s_callback_args_t *), void const *const p_context,</code>
--------------------------	---

i2s\_callback\_args\_t \*const p\_callback\_memory)

## Field Documentation

### ◆ open

fsp\_err\_t(\* i2s\_api\_t::open) (i2s\_ctrl\_t \*const p\_ctrl, i2s\_cfg\_t const \*const p\_cfg)

Initial configuration.

#### Implemented as

- R\_SSI\_Open()

#### Precondition

Peripheral clocks and any required output pins should be configured prior to calling this function.

#### Note

To reconfigure after calling this function, call *i2s\_api\_t::close* first.

#### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ stop

fsp\_err\_t(\* i2s\_api\_t::stop) (i2s\_ctrl\_t \*const p\_ctrl)

Stop communication. Communication is stopped when callback is called with I2S\_EVENT\_IDLE.

#### Implemented as

- R\_SSI\_Stop()

#### Parameters

[in]	p_ctrl	Control block set in <i>i2s_api_t::open</i> call for this instance.
------	--------	---

◆ **mute**

```
fsp_err_t(* i2s_api_t::mute) (i2s_ctrl_t *const p_ctrl, i2s_mute_t const mute_enable)
```

Enable or disable mute.

**Implemented as**

- R\_SSI\_Mute()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	mute_enable	Whether to enable or disable mute.

◆ **write**

```
fsp_err_t(* i2s_api_t::write) (i2s_ctrl_t *const p_ctrl, void const *const p_src, uint32_t const bytes)
```

Write I2S data. All transmit data is queued when callback is called with I2S\_EVENT\_TX\_EMPTY. Transmission is complete when callback is called with I2S\_EVENT\_IDLE.

**Implemented as**

- R\_SSI\_Write()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_src	Buffer of PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffer. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, padding 0s will be added to transmission to make it a multiple of 8.

## ◆ read

```
fsp_err_t(* i2s_api_t::read) (i2s_ctrl_t *const p_ctrl, void *const p_dest, uint32_t const bytes)
```

Read I2S data. Reception is complete when callback is called with I2S\_EVENT\_RX\_EMPTY.

**Implemented as**

- R\_SSI\_Read()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_dest	Buffer to store PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffer. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, receive will stop at the multiple of 8 below requested bytes.

◆ **writeRead**

```
fsp_err_t(* i2s_api_t::writeRead) (i2s_ctrl_t *const p_ctrl, void const *const p_src, void *const p_dest, uint32_t const bytes)
```

Simultaneously write and read I2S data. Transmission and reception are complete when callback is called with I2S\_EVENT\_IDLE.

**Implemented as**

- R\_SSI\_WriteRead()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[in]	p_src	Buffer of PCM samples. Must be 4 byte aligned.
[in]	p_dest	Buffer to store PCM samples. Must be 4 byte aligned.
[in]	bytes	Number of bytes in the buffers. Recommended requesting a multiple of 8 bytes. If not a multiple of 8, padding 0s will be added to transmission to make it a multiple of 8, and receive will stop at the multiple of 8 below requested bytes.

◆ **statusGet**

```
fsp_err_t(* i2s_api_t::statusGet) (i2s_ctrl_t *const p_ctrl, i2s_status_t *const p_status)
```

Get current status and store it in provided pointer p\_status.

**Implemented as**

- R\_SSI\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
[out]	p_status	Current status of the driver.

◆ **close**

```
fsp_err_t(* i2s_api_t::close) (i2s_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

**Implemented as**

- [R\\_SSI\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">i2s_api_t::open</a> call for this instance.
------	--------	--

◆ **callbackSet**

```
fsp_err_t(* i2s_api_t::callbackSet) (i2s_ctrl_t *const p_api_ctrl, void(*p_callback)(i2s_callback_args_t *), void const *const p_context, i2s_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_SSI\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the I2S control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **i2s\_instance\_t**

```
struct i2s_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">i2s_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">i2s_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">i2s_api_t</a> const *	p_api	Pointer to the API structure for

		this instance.
--	--	----------------

## Typedef Documentation

### ◆ i2s\_ctrl\_t

```
typedef void i2s_ctrl_t
```

I2S control block. Allocate an instance specific control block to pass into the I2S API calls.

#### Implemented as

- [ssi\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ i2s\_pcm\_width\_t

```
enum i2s_pcm_width_t
```

Audio PCM width

Enumerator

I2S_PCM_WIDTH_8_BITS	Using 8-bit PCM.
I2S_PCM_WIDTH_16_BITS	Using 16-bit PCM.
I2S_PCM_WIDTH_18_BITS	Using 18-bit PCM.
I2S_PCM_WIDTH_20_BITS	Using 20-bit PCM.
I2S_PCM_WIDTH_22_BITS	Using 22-bit PCM.
I2S_PCM_WIDTH_24_BITS	Using 24-bit PCM.
I2S_PCM_WIDTH_32_BITS	Using 24-bit PCM.

◆ **i2s\_word\_length\_t**

enum i2s_word_length_t	
Audio system word length.	
Enumerator	
I2S_WORD_LENGTH_8_BITS	Using 8-bit system word length.
I2S_WORD_LENGTH_16_BITS	Using 16-bit system word length.
I2S_WORD_LENGTH_24_BITS	Using 24-bit system word length.
I2S_WORD_LENGTH_32_BITS	Using 32-bit system word length.
I2S_WORD_LENGTH_48_BITS	Using 48-bit system word length.
I2S_WORD_LENGTH_64_BITS	Using 64-bit system word length.
I2S_WORD_LENGTH_128_BITS	Using 128-bit system word length.
I2S_WORD_LENGTH_256_BITS	Using 256-bit system word length.

◆ **i2s\_event\_t**

enum i2s_event_t	
Events that can trigger a callback function	
Enumerator	
I2S_EVENT_IDLE	Communication is idle.
I2S_EVENT_TX_EMPTY	Transmit buffer is below FIFO trigger level.
I2S_EVENT_RX_FULL	Receive buffer is above FIFO trigger level.

◆ **i2s\_mode\_t**

enum <a href="#">i2s_mode_t</a>	
I2S communication mode	
Enumerator	
I2S_MODE_SLAVE	Slave mode.
I2S_MODE_MASTER	Master mode.

◆ **i2s\_mute\_t**

enum <a href="#">i2s_mute_t</a>	
Mute audio samples.	
Enumerator	
I2S_MUTE_OFF	Disable mute.
I2S_MUTE_ON	Enable mute.

◆ **i2s\_ws\_continue\_t**

enum <a href="#">i2s_ws_continue_t</a>	
Whether to continue WS (word select line) transmission during idle state.	
Enumerator	
I2S_WS_CONTINUE_ON	Enable WS continue mode.
I2S_WS_CONTINUE_OFF	Disable WS continue mode.

◆ **i2s\_state\_t**

enum <a href="#">i2s_state_t</a>	
Possible status values returned by <a href="#">i2s_api_t::statusGet</a> .	
Enumerator	
I2S_STATE_IN_USE	I2S is in use.
I2S_STATE_STOPPED	I2S is stopped.

## 4.3.21 I/O Port Interface

### Interfaces

#### Detailed Description

Interface for accessing I/O ports and configuring I/O functionality.

## Summary

The IOPort shared interface provides the ability to access the IOPorts of a device at both bit and port level. Port and pin direction can be changed.

IOPORT Interface description: [I/O Ports \(r\\_ioport\)](#)

#### Data Structures

struct [ioport\\_pin\\_cfg\\_t](#)

struct [ioport\\_cfg\\_t](#)

struct [ioport\\_api\\_t](#)

struct [ioport\\_instance\\_t](#)

#### Typedefs

typedef uint16\_t [ioport\\_size\\_t](#)  
IO port size on this device. [More...](#)

typedef void [ioport\\_ctrl\\_t](#)

#### Enumerations

enum [ioport\\_peripheral\\_t](#)

enum [ioport\\_ethernet\\_channel\\_t](#)

enum [ioport\\_ethernet\\_mode\\_t](#)

enum [ioport\\_cfg\\_options\\_t](#)

enum [ioport\\_pwpr\\_t](#)

#### Data Structure Documentation

##### ◆ [ioport\\_pin\\_cfg\\_t](#)

struct ioport_pin_cfg_t		
Pin identifier and pin PFS pin configuration value		
Data Fields		
uint32_t	pin_cfg	Pin PFS configuration - Use ioport_cfg_options_t parameters to configure.
bsp_io_port_pin_t	pin	Pin identifier.

## ◆ ioport\_cfg\_t

struct ioport_cfg_t		
Multiple pin configuration data for loading into PFS registers by R_IOPORT_Init()		
Data Fields		
uint16_t	number_of_pins	Number of pins for which there is configuration data.
ioport_pin_cfg_t const *	p_pin_cfg_data	Pin configuration data.

## ◆ ioport\_api\_t

struct ioport_api_t	
IOPort driver structure. IOPort functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t(*)	close )(ioport_ctrl_t *const p_ctrl)
fsp_err_t(*)	pinsCfg )(ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
fsp_err_t(*)	pinCfg )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
fsp_err_t(*)	pinEventInputRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_event)
fsp_err_t(*)	pinEventOutputWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t pin_value)
fsp_err_t(*)	pinEthernetModeCfg )(ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t channel, ioport_ethernet_mode_t mode)

<code>fsp_err_t(*</code>	<code>pinRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)</code>
<code>fsp_err_t(*</code>	<code>pinWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)</code>
<code>fsp_err_t(*</code>	<code>portDirectionSet )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)</code>
<code>fsp_err_t(*</code>	<code>portEventInputRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_event_data)</code>
<code>fsp_err_t(*</code>	<code>portEventOutputWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t event_data, ioport_size_t mask_value)</code>
<code>fsp_err_t(*</code>	<code>portRead )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)</code>
<code>fsp_err_t(*</code>	<code>portWrite )(ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* ioport_api_t::open) (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)`

Initialize internal driver data and initial pin configurations. Called during startup. Do not call this API during runtime. Use `ioport_api_t::pinsCfg` for runtime reconfiguration of multiple pins.

### Implemented as

- `R_IOPORT_Open()`

### Parameters

[in]	<code>p_cfg</code>	Pointer to pin configuration data array.
------	--------------------	--

◆ **close**

```
fsp_err_t(* ioport_api_t::close) (ioport_ctrl_t *const p_ctrl)
```

Close the API.

**Implemented as**

- R\_IOPORT\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **pinsCfg**

```
fsp_err_t(* ioport_api_t::pinsCfg) (ioport_ctrl_t *const p_ctrl, const ioport_cfg_t *p_cfg)
```

Configure multiple pins.

**Implemented as**

- R\_IOPORT\_PinsCfg()

**Parameters**

[in]	p_cfg	Pointer to pin configuration data array.
------	-------	--

◆ **pinCfg**

```
fsp_err_t(* ioport_api_t::pinCfg) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, uint32_t cfg)
```

Configure settings for an individual pin.

**Implemented as**

- R\_IOPORT\_PinCfg()

**Parameters**

[in]	pin	Pin to be read.
[in]	cfg	Configuration options for the pin.

◆ **pinEventInputRead**

```
fsp_err_t(* ioport_api_t::pinEventInputRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t *p_pin_event)
```

Read the event input data of the specified pin and return the level.

**Implemented as**

- R\_IOPORT\_PinEventInputRead()

**Parameters**

[in]	pin	Pin to be read.
[in]	p_pin_event	Pointer to return the event data.

◆ **pinEventOutputWrite**

```
fsp_err_t(* ioport_api_t::pinEventOutputWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin,
bsp_io_level_t pin_value)
```

Write pin event data.

**Implemented as**

- R\_IOPORT\_PinEventOutputWrite()

**Parameters**

[in]	pin	Pin event data is to be written to.
[in]	pin_value	Level to be written to pin output event.

◆ **pinEthernetModeCfg**

```
fsp_err_t(* ioport_api_t::pinEthernetModeCfg) (ioport_ctrl_t *const p_ctrl, ioport_ethernet_channel_t
channel, ioport_ethernet_mode_t mode)
```

Configure the PHY mode of the Ethernet channels.

**Implemented as**

- R\_IOPORT\_EthernetModeCfg()

**Parameters**

[in]	channel	Channel configuration will be set for.
[in]	mode	PHY mode to set the channel to.

◆ **pinRead**

```
fsp_err_t(* ioport_api_t::pinRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t *p_pin_value)
```

Read level of a pin.

**Implemented as**

- [R\\_IOPORT\\_PinRead\(\)](#)

**Parameters**

[in]	pin	Pin to be read.
[in]	p_pin_value	Pointer to return the pin level.

◆ **pinWrite**

```
fsp_err_t(* ioport_api_t::pinWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_pin_t pin, bsp_io_level_t level)
```

Write specified level to a pin.

**Implemented as**

- [R\\_IOPORT\\_PinWrite\(\)](#)

**Parameters**

[in]	pin	Pin to be written to.
[in]	level	State to be written to the pin.

◆ **portDirectionSet**

```
fsp_err_t(* ioport_api_t::portDirectionSet) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t direction_values, ioport_size_t mask)
```

Set the direction of one or more pins on a port.

**Implemented as**

- [R\\_IOPORT\\_PortDirectionSet\(\)](#)

**Parameters**

[in]	port	Port being configured.
[in]	direction_values	Value controlling direction of pins on port (1 - output, 0 - input).
[in]	mask	Mask controlling which pins on the port are to be configured.

### ◆ portEventInputRead

```
fsp_err_t(* ioport_api_t::portEventInputRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t *p_event_data)
```

Read captured event data for a port.

#### Implemented as

- [R\\_IOPORT\\_PortEventInputRead\(\)](#)

#### Parameters

[in]	port	Port to be read.
[in]	p_event_data	Pointer to return the event data.

### ◆ portEventOutputWrite

```
fsp_err_t(* ioport_api_t::portEventOutputWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port,
ioport_size_t event_data, ioport_size_t mask_value)
```

Write event output data for a port.

#### Implemented as

- [R\\_IOPORT\\_PortEventOutputWrite\(\)](#)

#### Parameters

[in]	port	Port event data will be written to.
[in]	event_data	Data to be written as event data to specified port.
[in]	mask_value	Each bit set to 1 in the mask corresponds to that bit's value in event data. being written to port.

## ◆ portRead

```
fsp_err_t(* ioport_api_t::portRead) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t *p_port_value)
```

Read states of pins on the specified port.

**Implemented as**

- R\_IOPORT\_PortRead()

**Parameters**

[in]	port	Port to be read.
[in]	p_port_value	Pointer to return the port value.

## ◆ portWrite

```
fsp_err_t(* ioport_api_t::portWrite) (ioport_ctrl_t *const p_ctrl, bsp_io_port_t port, ioport_size_t value, ioport_size_t mask)
```

Write to multiple pins on a port.

**Implemented as**

- R\_IOPORT\_PortWrite()

**Parameters**

[in]	port	Port to be written to.
[in]	value	Value to be written to the port.
[in]	mask	Mask controlling which pins on the port are written to.

## ◆ ioport\_instance\_t

```
struct ioport_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

ioport_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
ioport_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
ioport_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **ioport\_size\_t**

typedef uint16\_t ioport\_size\_t

IO port size on this device.

IO port type used with ports

◆ **ioport\_ctrl\_t**

typedef void ioport\_ctrl\_t

IOPORT control block. Allocate an instance specific control block to pass into the IOPORT API calls.

**Implemented as**◦ [ioport\\_instance\\_ctrl\\_t](#)**Enumeration Type Documentation**◆ **ioport\_peripheral\_t**

enum ioport\_peripheral\_t

Superset of all peripheral functions.

## Enumerator

IOPORT_PERIPHERAL_IO	Pin will functions as an IO pin
IOPORT_PERIPHERAL_DEBUG	Pin will function as a DEBUG pin
IOPORT_PERIPHERAL_AGT	Pin will function as an AGT peripheral pin
IOPORT_PERIPHERAL_GPT0	Pin will function as a GPT peripheral pin
IOPORT_PERIPHERAL_GPT1	Pin will function as a GPT peripheral pin
IOPORT_PERIPHERAL_SCI0_2_4_6_8	Pin will function as an SCI peripheral pin
IOPORT_PERIPHERAL_SCI1_3_5_7_9	Pin will function as an SCI peripheral pin
IOPORT_PERIPHERAL_SPI	Pin will function as a SPI peripheral pin
IOPORT_PERIPHERAL_IIC	Pin will function as a IIC peripheral pin
IOPORT_PERIPHERAL_KEY	Pin will function as a KEY peripheral pin
IOPORT_PERIPHERAL_CLKOUT_COMP_RTC	Pin will function as a clock/comparator/RTC peripheral pin

IOPORT_PERIPHERAL_CAC_AD	Pin will function as a CAC/ADC peripheral pin
IOPORT_PERIPHERAL_BUS	Pin will function as a BUS peripheral pin
IOPORT_PERIPHERAL_CTSU	Pin will function as a CTSU peripheral pin
IOPORT_PERIPHERAL_LCDC	Pin will function as a segment LCD peripheral pin
IOPORT_PERIPHERAL_DALI	Pin will function as a DALI peripheral pin
IOPORT_PERIPHERAL_CAN	Pin will function as a CAN peripheral pin
IOPORT_PERIPHERAL_QSPI	Pin will function as a QSPI peripheral pin
IOPORT_PERIPHERAL_SSI	Pin will function as an SSI peripheral pin
IOPORT_PERIPHERAL_USB_FS	Pin will function as a USB full speed peripheral pin
IOPORT_PERIPHERAL_USB_HS	Pin will function as a USB high speed peripheral pin
IOPORT_PERIPHERAL_SDHI_MMC	Pin will function as an SD/MMC peripheral pin
IOPORT_PERIPHERAL_ETHER_MII	Pin will function as an Ethernet MMI peripheral pin
IOPORT_PERIPHERAL_ETHER_RMII	Pin will function as an Ethernet RMMI peripheral pin
IOPORT_PERIPHERAL_PDC	Pin will function as a PDC peripheral pin
IOPORT_PERIPHERAL_LCD_GRAPHICS	Pin will function as a graphics LCD peripheral pin
IOPORT_PERIPHERAL_TRACE	Pin will function as a debug trace peripheral pin
IOPORT_PERIPHERAL_OSPI	Pin will function as a OSPI peripheral pin
IOPORT_PERIPHERAL_CEC	Pin will function as a CEC peripheral pin

◆ **ioport\_ethernet\_channel\_t**

enum <code>ioport_ethernet_channel_t</code>	
Superset of Ethernet channels.	
Enumerator	
<code>IOPORT_ETHERNET_CHANNEL_0</code>	Used to select Ethernet channel 0.
<code>IOPORT_ETHERNET_CHANNEL_1</code>	Used to select Ethernet channel 1.
<code>IOPORT_ETHERNET_CHANNEL_END</code>	Marks end of enum - used by parameter checking.

◆ **ioport\_ethernet\_mode\_t**

enum <code>ioport_ethernet_mode_t</code>	
Superset of Ethernet PHY modes.	
Enumerator	
<code>IOPORT_ETHERNET_MODE_RMII</code>	Ethernet PHY mode set to MII.
<code>IOPORT_ETHERNET_MODE_MII</code>	Ethernet PHY mode set to RMII.
<code>IOPORT_ETHERNET_MODE_END</code>	Marks end of enum - used by parameter checking.

◆ **ioport\_cfg\_options\_t**

enum <code>ioport_cfg_options_t</code>	
Options to configure pin functions	
Enumerator	
<code>IOPORT_CFG_PORT_DIRECTION_INPUT</code>	Sets the pin direction to input (default)
<code>IOPORT_CFG_PORT_DIRECTION_OUTPUT</code>	Sets the pin direction to output.
<code>IOPORT_CFG_PORT_OUTPUT_LOW</code>	Sets the pin level to low.
<code>IOPORT_CFG_PORT_OUTPUT_HIGH</code>	Sets the pin level to high.
<code>IOPORT_CFG_PULLUP_ENABLE</code>	Enables the pin's internal pull-up.
<code>IOPORT_CFG_PIM_TTL</code>	Enables the pin's input mode.
<code>IOPORT_CFG_NMOS_ENABLE</code>	Enables the pin's NMOS open-drain output.
<code>IOPORT_CFG_PMOS_ENABLE</code>	Enables the pin's PMOS open-drain output.
<code>IOPORT_CFG_DRIVE_MID</code>	Sets pin drive output to medium.
<code>IOPORT_CFG_DRIVE_HS_HIGH</code>	Sets pin drive output to high along with supporting high speed.
<code>IOPORT_CFG_DRIVE_MID_IIC</code>	Sets pin to drive output needed for IIC on a 20mA port.
<code>IOPORT_CFG_DRIVE_HIGH</code>	Sets pin drive output to high.
<code>IOPORT_CFG_EVENT_RISING_EDGE</code>	Sets pin event trigger to rising edge.
<code>IOPORT_CFG_EVENT_FALLING_EDGE</code>	Sets pin event trigger to falling edge.
<code>IOPORT_CFG_EVENT_BOTH_EDGES</code>	Sets pin event trigger to both edges.
<code>IOPORT_CFG_IRQ_ENABLE</code>	Sets pin as an IRQ pin.
<code>IOPORT_CFG_ANALOG_ENABLE</code>	Enables pin to operate as an analog pin.
<code>IOPORT_CFG_PERIPHERAL_PIN</code>	Enables pin to operate as a peripheral pin.

◆ **ioport\_pwpr\_t**

enum ioport_pwpr_t	
Enumerator	
IOPORT_PFS_WRITE_DISABLE	Disable PFS write access.
IOPORT_PFS_WRITE_ENABLE	Enable PFS write access.

**4.3.22 JPEG Codec Interface**[Interfaces](#)**Detailed Description**

Interface for JPEG functions.

**Data Structures**

struct [jpeg\\_encode\\_image\\_size\\_t](#)

struct [jpeg\\_callback\\_args\\_t](#)

struct [jpeg\\_cfg\\_t](#)

struct [jpeg\\_api\\_t](#)

struct [jpeg\\_instance\\_t](#)

**Typedefs**

typedef void [jpeg\\_ctrl\\_t](#)

**Enumerations**

enum [jpeg\\_color\\_space\\_t](#)

enum [jpeg\\_data\\_order\\_t](#)

enum [jpeg\\_status\\_t](#)

enum [jpeg\\_decode\\_pixel\\_format\\_t](#)

enum [jpeg\\_decode\\_subsampling\\_t](#)

## Data Structure Documentation

### ◆ jpeg\_encode\_image\_size\_t

struct jpeg_encode_image_size_t		
Image parameter structure		
Data Fields		
uint16_t	horizontal_stride_pixels	Horizontal stride.
uint16_t	horizontal_resolution	Horizontal Resolution in pixels.
uint16_t	vertical_resolution	Vertical Resolution in pixels.

### ◆ jpeg\_callback\_args\_t

struct jpeg_callback_args_t		
Callback status structure		
Data Fields		
<a href="#">jpeg_status_t</a>	status	JPEG status.
uint32_t	image_size	JPEG image size.
void const *	p_context	Pointer to user-provided context.

### ◆ jpeg\_cfg\_t

struct jpeg_cfg_t		
User configuration structure, used in open function.		
<b>Data Fields</b>		
IRQn_Type	<a href="#">jedi_irq</a>	
		Data transfer interrupt IRQ number.
IRQn_Type	<a href="#">jdti_irq</a>	
		Decompression interrupt IRQ number.
uint8_t	<a href="#">jdti_ipl</a>	
		Data transfer interrupt priority.
uint8_t	<a href="#">jedi_ipl</a>	
		Decompression interrupt priority.

<code>jpeg_mode_t</code>	<a href="#">default_mode</a>
	Mode to use at startup.
<code>jpeg_data_order_t</code>	<a href="#">decode_input_data_order</a>
	Input data stream byte order.
<code>jpeg_data_order_t</code>	<a href="#">decode_output_data_order</a>
	Output data stream byte order.
<code>jpeg_decode_pixel_format_t</code>	<a href="#">pixel_format</a>
	Pixel format.
<code>uint8_t</code>	<a href="#">alpha_value</a>
	Alpha value to be applied to decoded pixel data. Only valid for ARGB8888 format.
<code>void(*</code>	<a href="#">p_decode_callback</a> )(jpeg_callback_args_t *p_args)
	User-supplied callback functions.
<code>void const *</code>	<a href="#">p_decode_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">jpeg_callback_args_t</a> .
<code>jpeg_data_order_t</code>	<a href="#">encode_input_data_order</a>
	Input data stream byte order.
<code>jpeg_data_order_t</code>	<a href="#">encode_output_data_order</a>
	Output data stream byte order.

uint16_t	<a href="#">dri_marker</a>
	DRI Marker setting (0 = No DRI or RST marker)
uint16_t	<a href="#">horizontal_resolution</a>
	Horizontal resolution of input image.
uint16_t	<a href="#">vertical_resolution</a>
	Vertical resolution of input image.
uint16_t	<a href="#">horizontal_stride_pixels</a>
	Horizontal stride of input image.
uint8_t const *	<a href="#">p_quant_luma_table</a>
	Luma quantization table.
uint8_t const *	<a href="#">p_quant_chroma_table</a>
	Chroma quantization table.
uint8_t const *	<a href="#">p_huffman_luma_ac_table</a>
	Huffman AC table for luma.
uint8_t const *	<a href="#">p_huffman_luma_dc_table</a>
	Huffman DC table for luma.
uint8_t const *	<a href="#">p_huffman_chroma_ac_table</a>
	Huffman AC table for chroma.

uint8_t const *	<a href="#">p_huffman_chroma_dc_table</a>
	Huffman DC table for chroma.
void(*	<a href="#">p_encode_callback</a> )(jpeg_callback_args_t *p_args)
	User-supplied callback functions.
void const *	<a href="#">p_encode_context</a>
	Placeholder for user data. Passed to user callback in <a href="#">jpeg_callback_args_t</a> .

◆ **jpeg\_api\_t**

struct jpeg_api_t	
JPEG functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">inputBufferSet</a> )(jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
fsp_err_t(*	<a href="#">outputBufferSet</a> )(jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
fsp_err_t(*	<a href="#">statusGet</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_status_t *const p_status)
fsp_err_t(*	<a href="#">close</a> )(jpeg_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">horizontalStrideSet</a> )(jpeg_ctrl_t *const p_ctrl, uint32_t horizontal_stride)
fsp_err_t(*	<a href="#">pixelFormatGet</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_color_space_t *const p_color_space)
fsp_err_t(*	<a href="#">imageSubsampleSet</a> )(jpeg_ctrl_t *const p_ctrl, jpeg_decode_subsample_t horizontal_subsample,

	<code>jpeg_decode_subsample_t vertical_subsample)</code>
<code>fsp_err_t(*</code>	<code>linesDecodedGet )(jpeg_ctrl_t *const p_ctrl, uint32_t *const p_lines)</code>
<code>fsp_err_t(*</code>	<code>imageSizeGet )(jpeg_ctrl_t *const p_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)</code>
<code>fsp_err_t(*</code>	<code>imageSizeSet )(jpeg_ctrl_t *const p_ctrl, jpeg_encode_image_size_t *p_image_size)</code>
<code>fsp_err_t(*</code>	<code>modeSet )(jpeg_ctrl_t *const p_ctrl, jpeg_mode_t mode)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* jpeg_api_t::open) (jpeg_ctrl_t *const p_ctrl, jpeg_cfg_t const *const p_cfg)`

Initial configuration

#### Implemented as

- `R_JPEG_Open()`

#### Precondition

none

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ inputBufferSet

```
fsp_err_t(* jpeg_api_t::inputBufferSet) (jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
```

Assign input data buffer to JPEG codec.

#### Implemented as

- R\_JPEG\_InputBufferSet()

#### Precondition

the JPEG codec module must have been opened properly.

#### Note

*The buffer starting address must be 8-byte aligned.*

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	p_buffer	Pointer to the input buffer space
[in]	buffer_size	Size of the input buffer

### ◆ outputBufferSet

```
fsp_err_t(* jpeg_api_t::outputBufferSet) (jpeg_ctrl_t *const p_ctrl, void *p_buffer, uint32_t buffer_size)
```

Assign output buffer to JPEG codec for storing output data.

#### Implemented as

- R\_JPEG\_OutputBufferSet()

#### Precondition

The JPEG codec module must have been opened properly.

#### Note

*The buffer starting address must be 8-byte aligned. For the decoding process, the HLD driver automatically computes the number of lines of the image to decoded so the output data fits into the given space. If the supplied output buffer is not able to hold the entire frame, the application should call the Output Full Callback function so it can be notified when additional buffer space is needed.*

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	p_buffer	Pointer to the output buffer space
[in]	buffer_size	Size of the output buffer

◆ **statusGet**

```
fsp_err_t(* jpeg_api_t::statusGet) (jpeg_ctrl_t *const p_ctrl, jpeg_status_t *const p_status)
```

Retrieve current status of the JPEG codec module.

**Implemented as**

- R\_JPEG\_StatusGet()

**Precondition**

the JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_status	JPEG module status

◆ **close**

```
fsp_err_t(* jpeg_api_t::close) (jpeg_ctrl_t *const p_ctrl)
```

Cancel an outstanding operation.

**Implemented as**

- R\_JPEG\_Close()

**Precondition**

the JPEG codec module must have been opened properly.

*Note*

*If the encoding or the decoding operation is finished without errors, the HLD driver automatically closes the device. In this case, application does not need to explicitly close the JPEG device.*

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
------	--------	---

◆ **horizontalStrideSet**

```
fsp_err_t(* jpeg_api_t::horizontalStrideSet) (jpeg_ctrl_t *const p_ctrl, uint32_t horizontal_stride)
```

Configure the horizontal stride value.

**Implemented as**

- [R\\_JPEG\\_DecodeHorizontalStrideSet\(\)](#)

**Precondition**

The JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	horizontal_stride	Horizontal stride value to be used for the decoded image data.
[in]	buffer_size	Size of the output buffer

◆ **pixelFormatGet**

```
fsp_err_t(* jpeg_api_t::pixelFormatGet) (jpeg_ctrl_t *const p_ctrl, jpeg_color_space_t *const p_color_space)
```

Get the input pixel format.

**Implemented as**

- [R\\_JPEG\\_DecodePixelFormatGet\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_color_space	JPEG input format.

### ◆ imageSubsampleSet

```
fsp_err_t(* jpeg_api_t::imageSubsampleSet) (jpeg_ctrl_t *const p_ctrl, jpeg_decode_subsample_t
horizontal_subsample, jpeg_decode_subsample_t vertical_subsample)
```

Configure the horizontal and vertical subsample settings.

#### Implemented as

- R\_JPEG\_DecodeImageSubsampleSet()

#### Precondition

The JPEG codec module must have been opened properly.

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	horizontal_subsample	Horizontal subsample value
[in]	vertical_subsample	Vertical subsample value

### ◆ linesDecodedGet

```
fsp_err_t(* jpeg_api_t::linesDecodedGet) (jpeg_ctrl_t *const p_ctrl, uint32_t *const p_lines)
```

Return the number of lines decoded into the output buffer.

#### Implemented as

- R\_JPEG\_DecodeLinesDecodedGet()

#### Precondition

the JPEG codec module must have been opened properly.

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_lines	Number of lines decoded

◆ **imageSizeGet**

```
fsp_err_t(* jpeg_api_t::imageSizeGet) (jpeg_ctrl_t *const p_ctrl, uint16_t *p_horizontal_size, uint16_t *p_vertical_size)
```

Retrieve image size during decoding operation.

**Implemented as**

- [R\\_JPEG\\_DecodeImageSizeGet\(\)](#)

**Precondition**

the JPEG codec module must have been opened properly.

**Note**

*If the encoding or the decoding operation is finished without errors, the HLD driver automatically closes the device. In this case, application does not need to explicitly close the JPEG device.*

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[out]	p_horizontal_size	Image horizontal size, in number of pixels.
[out]	p_vertical_size	Image vertical size, in number of pixels.

◆ **imageSizeSet**

```
fsp_err_t(* jpeg_api_t::imageSizeSet) (jpeg_ctrl_t *const p_ctrl, jpeg_encode_image_size_t *p_image_size)
```

Set image parameters to JPEG Codec

**Implemented as**

- [R\\_JPEG\\_EncodeImageSizeSet\(\)](#)

**Precondition**

The JPEG codec module must have been opened properly.

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_image_size	Pointer to the RAW image parameters

◆ **modeSet**

```
fsp_err_t(* jpeg_api_t::modeSet) (jpeg_ctrl_t *const p_ctrl, jpeg_mode_t mode)
```

Switch between encode and decode mode or vice-versa.

**Implemented as**

- [R\\_JPEG\\_ModeSet\(\)](#)

**Precondition**

The JPEG codec module must have been opened properly. The JPEG Codec can only perform one operation at a time and requires different configuration for encode and decode. This function facilitates easy switching between the two modes in case both are needed in an application.

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">jpeg_api_t::open</a> call.
[in]	mode	Mode to switch to

◆ **jpeg\_instance\_t**

```
struct jpeg_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">jpeg_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">jpeg_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">jpeg_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **jpeg\_ctrl\_t**

```
typedef void jpeg_ctrl_t
```

JPEG decode control block. Allocate an instance specific control block to pass into the JPEG decode API calls.

**Implemented as**

- [jpeg\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

## ◆ jpeg\_color\_space\_t

enum jpeg_color_space_t	
Configuration for this module Image color space definitions	
Enumerator	
JPEG_COLOR_SPACE_YCBCR444	Color Space YCbCr 444.
JPEG_COLOR_SPACE_YCBCR422	Color Space YCbCr 422.
JPEG_COLOR_SPACE_YCBCR420	Color Space YCbCr 420.
JPEG_COLOR_SPACE_YCBCR411	Color Space YCbCr 411.

## ◆ jpeg\_data\_order\_t

enum jpeg_data_order_t	
Multi-byte Data Format	
Enumerator	
JPEG_DATA_ORDER_NORMAL	(1)(2)(3)(4)(5)(6)(7)(8) Normal byte order
JPEG_DATA_ORDER_BYTE_SWAP	(2)(1)(4)(3)(6)(5)(8)(7) Byte Swap
JPEG_DATA_ORDER_WORD_SWAP	(3)(4)(1)(2)(7)(8)(5)(6) Word Swap
JPEG_DATA_ORDER_WORD_BYTE_SWAP	(4)(3)(2)(1)(8)(7)(6)(5) Word-Byte Swap
JPEG_DATA_ORDER_LONGWORD_SWAP	(5)(6)(7)(8)(1)(2)(3)(4) Longword Swap
JPEG_DATA_ORDER_LONGWORD_BYTE_SWAP	(6)(5)(8)(7)(2)(1)(4)(3) Longword Byte Swap
JPEG_DATA_ORDER_LONGWORD_WORD_SWAP	(7)(8)(5)(6)(3)(4)(1)(2) Longword Word Swap
JPEG_DATA_ORDER_LONGWORD_WORD_BYTE_SWAP	(8)(7)(6)(5)(4)(3)(2)(1) Longword Word Byte Swap

## ◆ jpeg\_status\_t

enum jpeg_status_t	
JPEG HLD driver internal status information. The driver can simultaneously be in more than any one status at the same time. Parse the status bit-fields using the definitions in this enum to determine driver status	
Enumerator	
JPEG_STATUS_NONE	JPEG codec module is not initialized.
JPEG_STATUS_IDLE	JPEG Codec module is open but not running.
JPEG_STATUS_RUNNING	JPEG Codec is running.
JPEG_STATUS_HEADER_PROCESSING	JPEG Codec module is reading the JPEG header information.
JPEG_STATUS_INPUT_PAUSE	JPEG Codec paused waiting for more input data.
JPEG_STATUS_OUTPUT_PAUSE	JPEG Codec paused after it decoded the number of lines specified by user.
JPEG_STATUS_IMAGE_SIZE_READY	JPEG decoding operation obtained image size, and paused.
JPEG_STATUS_ERROR	JPEG Codec module encountered an error.
JPEG_STATUS_OPERATION_COMPLETE	JPEG Codec has completed the operation.

## ◆ jpeg\_decode\_pixel\_format\_t

enum jpeg_decode_pixel_format_t	
Pixel Data Format	
Enumerator	
JPEG_DECODE_PIXEL_FORMAT_ARGB8888	Pixel Data ARGB8888 format.
JPEG_DECODE_PIXEL_FORMAT_RGB565	Pixel Data RGB565 format.

### ◆ jpeg\_decode\_subsample\_t

enum jpeg_decode_subsample_t	
Data type for horizontal and vertical subsample settings. This setting applies only to the decoding operation.	
Enumerator	
JPEG_DECODE_OUTPUT_NO_SUBSAMPLE	No subsample. The image is decoded with no reduction in size.
JPEG_DECODE_OUTPUT_SUBSAMPLE_HALF	The output image size is reduced by half.
JPEG_DECODE_OUTPUT_SUBSAMPLE_ONE_QUARTER	The output image size is reduced to one-quarter.
JPEG_DECODE_OUTPUT_SUBSAMPLE_ONE_EIGHTH	The output image size is reduced to one-eighth.

## 4.3.23 Key Matrix Interface

### Interfaces

#### Detailed Description

Interface for key matrix functions.

## Summary

The KEYMATRIX interface provides standard Key Matrix functionality including event generation on a rising or falling edge for one or more channels at the same time. The generated event indicates all channels that are active in that instant via a bit mask. This allows the interface to be used with a matrix configuration or a one-to-one hardware implementation that is triggered on either a rising or a falling edge.

Implemented by:

- [Key Interrupt \(r\\_kint\)](#)

#### Data Structures

struct [keymatrix\\_callback\\_args\\_t](#)

struct [keymatrix\\_cfg\\_t](#)

struct [keymatrix\\_api\\_t](#)

```
struct keymatrix_instance_t
```

## Typedefs

```
typedef void keymatrix_ctrl_t
```

## Enumerations

```
enum keymatrix_trigger_t
```

## Data Structure Documentation

### ◆ keymatrix\_callback\_args\_t

struct keymatrix_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Holder for user data. Set in <a href="#">keymatrix_api_t::open</a> function in <a href="#">keymatrix_cfg_t</a> .
uint32_t	channel_mask	Bit vector representing the physical hardware channel(s) that caused the interrupt.

### ◆ keymatrix\_cfg\_t

struct keymatrix_cfg_t		
User configuration structure, used in open function		
Data Fields		
uint32_t	<a href="#">channel_mask</a>	
		Key Input channel(s). Bit mask of channels to open.
<a href="#">keymatrix_trigger_t</a>	<a href="#">trigger</a>	
		Key Input trigger setting.
uint8_t	<a href="#">ipl</a>	
		Interrupt priority level.
IRQn_Type	<a href="#">irq</a>	
		NVIC IRQ number.

void(*	<a href="#">p_callback</a> )(keymatrix_callback_args_t *p_args)
	Callback for key interrupt ISR.
void const *	<a href="#">p_context</a>
	Holder for user data. Passed to callback in keymatrix_user_cb_data_t.
void const *	<a href="#">p_extend</a>
	Extension parameter for hardware specific settings.

#### ◆ keymatrix\_api\_t

struct keymatrix_api_t	
Key Matrix driver structure. Key Matrix functions implemented at the HAL layer will use this API.	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(keymatrix_ctrl_t *const p_ctrl, keymatrix_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">enable</a> )(keymatrix_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">disable</a> )(keymatrix_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">close</a> )(keymatrix_ctrl_t *const p_ctrl)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* keymatrix_api_t::open) (keymatrix_ctrl_t *const p_ctrl, keymatrix_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_KINT\_Open()

**Parameters**

[out]	p_ctrl	Pointer to control block. Must be declared by user. Value set in this function.
[in]	p_cfg	Pointer to configuration structure. All elements of the structure must be set by user.

◆ **enable**

```
fsp_err_t(* keymatrix_api_t::enable) (keymatrix_ctrl_t *const p_ctrl)
```

Enable Key interrupt

**Implemented as**

- R\_KINT\_Enable()

**Parameters**

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	--

◆ **disable**

```
fsp_err_t(* keymatrix_api_t::disable) (keymatrix_ctrl_t *const p_ctrl)
```

Disable Key interrupt.

**Implemented as**

- R\_KINT\_Disable()

**Parameters**

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	--

◆ **close**

```
fsp_err_t(* keymatrix_api_t::close) (keymatrix_ctrl_t *const p_ctrl)
```

Allow driver to be reconfigured. May reduce power consumption.

**Implemented as**

- R\_KINT\_Close()

**Parameters**

[in]	p_ctrl	Control block pointer set in Open call for this Key interrupt.
------	--------	--

◆ **keymatrix\_instance\_t**

```
struct keymatrix_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

keymatrix_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
keymatrix_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
keymatrix_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **keymatrix\_ctrl\_t**

```
typedef void keymatrix_ctrl_t
```

Key matrix control block. Allocate an instance specific control block to pass into the key matrix API calls.

**Implemented as**

- kint\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **keymatrix\_trigger\_t**

enum <code>keymatrix_trigger_t</code>	
Trigger type: rising edge, falling edge	
Enumerator	
<code>KEYMATRIX_TRIG_FALLING</code>	Falling edge trigger.
<code>KEYMATRIX_TRIG_RISING</code>	Rising edge trigger.

**4.3.24 Low Power Modes Interface**

## Interfaces

**Detailed Description**

Interface for accessing low power modes.

**Summary**

This section defines the API for the LPM (Low Power Mode) Driver. The LPM Driver provides functions for controlling power consumption by configuring and transitioning to a low power mode. The LPM driver supports configuration of MCU low power modes using the LPM hardware peripheral. The LPM driver supports low power modes deep standby, standby, sleep, and snooze.

*Note*

*Not all low power modes are available on all MCUs.*

The LPM interface is implemented by:

- [Low Power Modes \(r\\_lpm\)](#)

**Data Structures**

struct `lpm_cfg_t`

struct `lpm_api_t`

struct `lpm_instance_t`

**Typedefs**

typedef void `lpm_ctrl_t`

**Enumerations**

enum `lpm_mode_t`

enum [lpm\\_snooze\\_request\\_t](#)enum [lpm\\_snooze\\_end\\_t](#)enum [lpm\\_snooze\\_cancel\\_t](#)enum [lpm\\_snooze\\_dtc\\_t](#)enum [lpm\\_standby\\_wake\\_source\\_t](#)enum [lpm\\_io\\_port\\_t](#)enum [lpm\\_power\\_supply\\_t](#)enum [lpm\\_deep\\_standby\\_cancel\\_edge\\_t](#)enum [lpm\\_deep\\_standby\\_cancel\\_source\\_t](#)enum [lpm\\_output\\_port\\_enable\\_t](#)

## Data Structure Documentation

### ◆ [lpm\\_cfg\\_t](#)

struct <a href="#">lpm_cfg_t</a>		
User configuration structure, used in open function		
Data Fields		
<a href="#">lpm_mode_t</a>	low_power_mode	Low Power Mode
<a href="#">lpm_standby_wake_source_bits_t</a>	standby_wake_sources	Bitwise list of sources to wake from standby
<a href="#">lpm_snooze_request_t</a>	snooze_request_source	Snooze request source
<a href="#">lpm_snooze_end_bits_t</a>	snooze_end_sources	Bitwise list of snooze end sources
<a href="#">lpm_snooze_cancel_t</a>	snooze_cancel_sources	List of snooze cancel sources
<a href="#">lpm_snooze_dtc_t</a>	dtc_state_in_snooze	State of DTC in snooze mode, enabled or disabled
void const *	p_extend	Placeholder for extension.

### ◆ [lpm\\_api\\_t](#)

struct <a href="#">lpm_api_t</a>	
LPM driver structure. General LPM functions implemented at the HAL layer will follow this API.	
Data Fields	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">lpm_ctrl_t</a> *const p_api_ctrl, <a href="#">lpm_cfg_t</a> const *const p_cfg)

<code>fsp_err_t(*</code>	<code>close )(lpm_ctrl_t *const p_api_ctrl)</code>
<code>fsp_err_t(*</code>	<code>lowPowerReconfigure )(lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>lowPowerModeEnter )(lpm_ctrl_t *const p_api_ctrl)</code>
<code>fsp_err_t(*</code>	<code>ioKeepClear )(lpm_ctrl_t *const p_api_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* lpm_api_t::open) (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)`

Initialization function

#### Implemented as

- `R_LPM_Open()`

### ◆ close

`fsp_err_t(* lpm_api_t::close) (lpm_ctrl_t *const p_api_ctrl)`

Initialization function

#### Implemented as

- `R_LPM_Close()`

### ◆ lowPowerReconfigure

`fsp_err_t(* lpm_api_t::lowPowerReconfigure) (lpm_ctrl_t *const p_api_ctrl, lpm_cfg_t const *const p_cfg)`

Configure a low power mode.

#### Implemented as

- `R_LPM_LowPowerReconfigure()`

#### Parameters

[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.
------	--------------------	---

◆ **lowPowerModeEnter**

```
fsp_err_t(* lpm_api_t::lowPowerModeEnter) (lpm_ctrl_t *const p_api_ctrl)
```

Enter low power mode (sleep/standby/deep standby) using WFI macro. Function will return after waking from low power mode.

**Implemented as**

- [R\\_LPM\\_LowPowerModeEnter\(\)](#)

◆ **ioKeepClear**

```
fsp_err_t(* lpm_api_t::ioKeepClear) (lpm_ctrl_t *const p_api_ctrl)
```

Clear the IOKEEP bit after deep software standby.

◦ **Implemented as**

- [R\\_LPM\\_IoKeepClear\(\)](#)

◆ **lpm\_instance\_t**

```
struct lpm_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">lpm_ctrl_t *</a>	<a href="#">p_ctrl</a>	Pointer to the control structure for this instance.
<a href="#">lpm_cfg_t const *const</a>	<a href="#">p_cfg</a>	Pointer to the configuration structure for this instance.
<a href="#">lpm_api_t const *const</a>	<a href="#">p_api</a>	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **lpm\_ctrl\_t**

```
typedef void lpm_ctrl_t
```

LPM control block. Allocate an instance specific control block to pass into the LPM API calls.

**Implemented as**

- [lpm\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **lpm\_mode\_t**

enum <code>lpm_mode_t</code>	
Low power modes	
Enumerator	
<code>LPM_MODE_SLEEP</code>	Sleep mode.
<code>LPM_MODE_STANDBY</code>	Software Standby mode.
<code>LPM_MODE_STANDBY_SNOOZE</code>	Software Standby mode with Snooze mode enabled.
<code>LPM_MODE_DEEP</code>	Deep Software Standby mode.

◆ **lpm\_snooze\_request\_t**

enum <code>lpm_snooze_request_t</code>	
Snooze request sources	
Enumerator	
<code>LPM_SNOOZE_REQUEST_RXD0_FALLING</code>	Enable RXD0 falling edge snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ0</code>	Enable IRQ0 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ1</code>	Enable IRQ1 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ2</code>	Enable IRQ2 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ3</code>	Enable IRQ3 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ4</code>	Enable IRQ4 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ5</code>	Enable IRQ5 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ6</code>	Enable IRQ6 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ7</code>	Enable IRQ7 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ8</code>	Enable IRQ8 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ9</code>	Enable IRQ9 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ10</code>	Enable IRQ10 pin snooze request.
<code>LPM_SNOOZE_REQUEST_IRQ11</code>	Enable IRQ11 pin snooze request.

LPM_SNOOZE_REQUEST_IRQ12	Enable IRQ12 pin snooze request.
LPM_SNOOZE_REQUEST_IRQ13	Enable IRQ13 pin snooze request.
LPM_SNOOZE_REQUEST_IRQ14	Enable IRQ14 pin snooze request.
LPM_SNOOZE_REQUEST_IRQ15	Enable IRQ15 pin snooze request.
LPM_SNOOZE_REQUEST_KEY	Enable KR snooze request.
LPM_SNOOZE_REQUEST_ACMPS0	Enable High-speed analog comparator 0 snooze request.
LPM_SNOOZE_REQUEST_RTC_ALARM	Enable RTC alarm snooze request.
LPM_SNOOZE_REQUEST_RTC_PERIOD	Enable RTC period snooze request.
LPM_SNOOZE_REQUEST_AGT1_UNDERFLOW	Enable AGT1 underflow snooze request.
LPM_SNOOZE_REQUEST_AGT1_COMPARE_A	Enable AGT1 compare match A snooze request.
LPM_SNOOZE_REQUEST_AGT1_COMPARE_B	Enable AGT1 compare match B snooze request.
LPM_SNOOZE_REQUEST_AGT3_UNDERFLOW	Enable AGT3 underflow snooze request.
LPM_SNOOZE_REQUEST_AGT3_COMPARE_A	Enable AGT3 compare match A snooze request.
LPM_SNOOZE_REQUEST_AGT3_COMPARE_B	Enable AGT3 compare match B snooze request.

◆ **lpm\_snooze\_end\_t**

enum <a href="#">lpm_snooze_end_t</a>	
Snooze end control	
Enumerator	
LPM_SNOOZE_END_STANDBY_WAKE_SOURCES	Transition from Snooze to Normal mode directly.
LPM_SNOOZE_END_AGT1_UNDERFLOW	AGT1 underflow.
LPM_SNOOZE_END_DTC_TRANS_COMPLETE	Last DTC transmission completion.
LPM_SNOOZE_END_DTC_TRANS_COMPLETE_NEGATED	Not Last DTC transmission completion.
LPM_SNOOZE_END_ADC0_COMPARE_MATCH	ADC Channel 0 compare match.
LPM_SNOOZE_END_ADC0_COMPARE_MISMATCH	ADC Channel 0 compare mismatch.
LPM_SNOOZE_END_ADC1_COMPARE_MATCH	ADC 1 compare match.
LPM_SNOOZE_END_ADC1_COMPARE_MISMATCH	ADC 1 compare mismatch.
LPM_SNOOZE_END_SCI0_ADDRESS_MATCH	SCI0 address mismatch.
LPM_SNOOZE_END_AGT3_UNDERFLOW	AGT3 underflow.

◆ **lpm\_snooze\_cancel\_t**

enum <a href="#">lpm_snooze_cancel_t</a>	
Snooze cancel control	
Enumerator	
LPM_SNOOZE_CANCEL_SOURCE_NONE	No snooze cancel source.
LPM_SNOOZE_CANCEL_SOURCE_ADC0_WCMPPM	ADC Channel 0 window compare match.
LPM_SNOOZE_CANCEL_SOURCE_ADC0_WCMPUM	ADC Channel 0 window compare mismatch.
LPM_SNOOZE_CANCEL_SOURCE_DTC_COMPLETE	DTC transfer completion.
LPM_SNOOZE_CANCEL_SOURCE_DOC_DOPCI	Data operation circuit interrupt.

◆ **lpm\_snooze\_dtc\_t**

enum <code>lpm_snooze_dtc_t</code>	
DTC Enable in Snooze Mode	
Enumerator	
<code>LPM_SNOOZE_DTC_DISABLE</code>	Disable DTC operation.
<code>LPM_SNOOZE_DTC_ENABLE</code>	Enable DTC operation.

◆ **lpm\_standby\_wake\_source\_t**

enum <code>lpm_standby_wake_source_t</code>	
Wake from standby mode sources, does not apply to sleep or deep standby modes	
Enumerator	
<code>LPM_STANDBY_WAKE_SOURCE_IRQ0</code>	IRQ0.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ1</code>	IRQ1.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ2</code>	IRQ2.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ3</code>	IRQ3.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ4</code>	IRQ4.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ5</code>	IRQ5.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ6</code>	IRQ6.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ7</code>	IRQ7.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ8</code>	IRQ8.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ9</code>	IRQ9.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ10</code>	IRQ10.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ11</code>	IRQ11.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ12</code>	IRQ12.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ13</code>	IRQ13.
<code>LPM_STANDBY_WAKE_SOURCE_IRQ14</code>	IRQ14.

LPM_STANDBY_WAKE_SOURCE_IRQ15	IRQ15.
LPM_STANDBY_WAKE_SOURCE_IWDT	Independent watchdog interrupt.
LPM_STANDBY_WAKE_SOURCE_KEY	Key interrupt.
LPM_STANDBY_WAKE_SOURCE_LVD1	Low Voltage Detection 1 interrupt.
LPM_STANDBY_WAKE_SOURCE_LVD2	Low Voltage Detection 2 interrupt.
LPM_STANDBY_WAKE_SOURCE_VBATT	VBATT Monitor interrupt.
LPM_STANDBY_WAKE_SOURCE_ACMPHS0	Analog Comparator High-speed 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_ACMPLP0	Analog Comparator Low-speed 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_RTCALM	RTC Alarm interrupt.
LPM_STANDBY_WAKE_SOURCE_RTCPRD	RTC Period interrupt.
LPM_STANDBY_WAKE_SOURCE_USBHS	USB High-speed interrupt.
LPM_STANDBY_WAKE_SOURCE_USBFS	USB Full-speed interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1UD	AGT1 underflow interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1CA	AGT1 compare match A interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT1CB	AGT1 compare match B interrupt.
LPM_STANDBY_WAKE_SOURCE_IIC0	I2C 0 interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3UD	AGT3 underflow interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3CA	AGT3 compare match A interrupt.
LPM_STANDBY_WAKE_SOURCE_AGT3CB	AGT3 compare match B interrupt.

◆ **lpm\_io\_port\_t**

enum <code>lpm_io_port_t</code>	
I/O port state after Deep Software Standby mode	
Enumerator	
<code>LPM_IO_PORT_RESET</code>	When the Deep Software Standby mode is canceled, the I/O ports are in the reset state
<code>LPM_IO_PORT_NO_CHANGE</code>	When the Deep Software Standby mode is canceled, the I/O ports are in the same state as in the Deep Software Standby mode

◆ **lpm\_power\_supply\_t**

enum <code>lpm_power_supply_t</code>	
Power supply control	
Enumerator	
<code>LPM_POWER_SUPPLY_DEEPCUT0</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is supplied in deep software standby mode
<code>LPM_POWER_SUPPLY_DEEPCUT1</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is not supplied in deep software standby mode
<code>LPM_POWER_SUPPLY_DEEPCUT3</code>	Power to the standby RAM, Low-speed on-chip oscillator, AGTn, and USBFS/HS resume detecting unit is not supplied in deep software standby mode. In addition, LVD is disabled and the low power function in a poweron reset circuit is enabled

◆ **lpm\_deep\_standby\_cancel\_edge\_t**

enum <code>lpm_deep_standby_cancel_edge_t</code>	
Deep Standby Interrupt Edge	
Enumerator	
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_EDGE_NONE</code>	No options for a deep standby cancel source.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0_RIS</code>	

ING	IRQ0-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0_FALLING	IRQ0-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1_RISING	IRQ1-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1_FALLING	IRQ1-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2_RISING	IRQ2-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2_FALLING	IRQ2-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3_RISING	IRQ3-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3_FALLING	IRQ3-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4_RISING	IRQ4-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4_FALLING	IRQ4-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5_RISING	IRQ5-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5_FALLING	IRQ5-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6_RISING	IRQ6-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6_FALLING	IRQ6-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7_RISING	IRQ7-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7_FALLING	IRQ7-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8_RISING	IRQ8-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8_FALLING	IRQ8-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9_RISING	IRQ9-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9_FALLING	IRQ9-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10_RISING	IRQ10-DS Pin Rising Edge.

LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10_FALLING	IRQ10-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11_RISING	IRQ11-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11_FALLING	IRQ11-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12_RISING	IRQ12-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12_FALLING	IRQ12-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13_RISING	IRQ13-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13_FALLING	IRQ13-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14_RISING	IRQ14-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14_FALLING	IRQ14-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15_RISING	IRQ14-DS Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15_FALLING	IRQ14-DS Pin Falling Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1_RISING	LVD1 Rising Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1_FALLING	LVD1 Falling Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2_RISING	LVD2 Rising Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2_FALLING	LVD2 Falling Slope.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI_RISING	NMI Pin Rising Edge.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI_FALLING	NMI Pin Falling Edge.

◆ **lpm\_deep\_standby\_cancel\_source\_t**

enum <code>lpm_deep_standby_cancel_source_t</code>	
Deep Standby cancel sources	
Enumerator	
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_RESET_ONLY</code>	Cancel deep standby only by reset.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ0</code>	IRQ0.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ1</code>	IRQ1.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ2</code>	IRQ2.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ3</code>	IRQ3.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ4</code>	IRQ4.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ5</code>	IRQ5.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ6</code>	IRQ6.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ7</code>	IRQ7.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ8</code>	IRQ8.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ9</code>	IRQ9.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ10</code>	IRQ10.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ11</code>	IRQ11.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ12</code>	IRQ12.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ13</code>	IRQ13.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ14</code>	IRQ14.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_IRQ15</code>	IRQ15.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD1</code>	LVD1.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_LVD2</code>	LVD2.
<code>LPM_DEEP_STANDBY_CANCEL_SOURCE_RTC_INTERVAL</code>	RTC Interval Interrupt.

LPM_DEEP_STANDBY_CANCEL_SOURCE_RTC_ALARM	RTC Alarm Interrupt.
LPM_DEEP_STANDBY_CANCEL_SOURCE_NMI	NMI.
LPM_DEEP_STANDBY_CANCEL_SOURCE_USBFS	USBFS Suspend/Resume.
LPM_DEEP_STANDBY_CANCEL_SOURCE_USBHS	USBHS Suspend/Resume.
LPM_DEEP_STANDBY_CANCEL_SOURCE_AGT1	AGT1 Underflow.

#### ◆ lpm\_output\_port\_enable\_t

enum lpm_output_port_enable_t	
Output port enable	
Enumerator	
LPM_OUTPUT_PORT_ENABLE_HIGH_IMPEDANCE	0: In Software Standby Mode or Deep Software Standby Mode, the address output pins, data output pins, and other bus control signal output pins are set to the high-impedance state. In Snooze, the status of the address bus and bus control signals are same as before entering Software Standby Mode.
LPM_OUTPUT_PORT_ENABLE_RETAIN	1: In Software Standby Mode, the address output pins, data output pins, and other bus control signal output pins retain the output state.

## 4.3.25 Low Voltage Detection Interface

### Interfaces

#### Detailed Description

Interface for Low Voltage Detection.

## Summary

The LVD driver provides functions for configuring the LVD voltage monitors and detectors.

Implemented by:

- [Low Voltage Detection \(r\\_lvd\)](#)

## Data Structures

struct [lvd\\_status\\_t](#)

struct [lvd\\_callback\\_args\\_t](#)

struct [lvd\\_cfg\\_t](#)

struct [lvd\\_api\\_t](#)

struct [lvd\\_instance\\_t](#)

## Typedefs

typedef void [lvd\\_ctrl\\_t](#)

## Enumerations

enum [lvd\\_threshold\\_t](#)

enum [lvd\\_response\\_t](#)

enum [lvd\\_voltage\\_slope\\_t](#)

enum [lvd\\_sample\\_clock\\_t](#)

enum [lvd\\_negation\\_delay\\_t](#)

enum [lvd\\_threshold\\_crossing\\_t](#)

enum [lvd\\_current\\_state\\_t](#)

## Data Structure Documentation

### ◆ [lvd\\_status\\_t](#)

struct <a href="#">lvd_status_t</a>		
Current state of a voltage monitor.		
Data Fields		
<a href="#">lvd_threshold_crossing_t</a>	crossing_detected	Threshold crossing detection (latched)
<a href="#">lvd_current_state_t</a>	current_state	Instantaneous status of monitored voltage (above or below threshold)

### ◆ [lvd\\_callback\\_args\\_t](#)

struct <a href="#">lvd_callback_args_t</a>
LVD callback parameter definition

Data Fields		
uint32_t	monitor_number	Monitor number.
lvd_current_state_t	current_state	Current state of the voltage monitor.
void const *	p_context	Placeholder for user data.

#### ◆ lvd\_cfg\_t

struct lvd_cfg_t		
LVD configuration structure		
<b>Data Fields</b>		
uint32_t	monitor_number	
lvd_threshold_t	voltage_threshold	
lvd_response_t	detection_response	
lvd_voltage_slope_t	voltage_slope	
lvd_negation_delay_t	negation_delay	
lvd_sample_clock_t	sample_clock_divisor	
IRQn_Type	irq	
uint8_t	monitor_ipl	
void(*	p_callback )(lvd_callback_args_t *p_args)	
void const *	p_context	
void const *	p_extend	
<b>Field Documentation</b>		

◆ **monitor\_number**

uint32\_t lvd\_cfg\_t::monitor\_number

Monitor number, 1, 2, ...

◆ **voltage\_threshold**

lvd\_threshold\_t lvd\_cfg\_t::voltage\_threshold

Threshold for out of range voltage detection

◆ **detection\_response**

lvd\_response\_t lvd\_cfg\_t::detection\_response

Response on detecting a threshold crossing

◆ **voltage\_slope**

lvd\_voltage\_slope\_t lvd\_cfg\_t::voltage\_slope

Direction of voltage crossing that will trigger a detection (Rising Edge, Falling Edge, Both).

◆ **negation\_delay**

lvd\_negation\_delay\_t lvd\_cfg\_t::negation\_delay

Negation of LVD signal follows reset or voltage in range

◆ **sample\_clock\_divisor**

lvd\_sample\_clock\_t lvd\_cfg\_t::sample\_clock\_divisor

Sample clock divider, use LVD\_SAMPLE\_CLOCK\_DISABLED to disable digital filtering

◆ **irq**

IRQn\_Type lvd\_cfg\_t::irq

Interrupt number.

◆ **monitor\_ipl**

uint8\_t lvd\_cfg\_t::monitor\_ipl

Interrupt priority level.

◆ **p\_callback**

void(\* lvd\_cfg\_t::p\_callback) (lvd\_callback\_args\_t \*p\_args)

User function to be called from interrupt

◆ **p\_context**

void const\* lvd\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in

◆ **p\_extend**

void const\* lvd\_cfg\_t::p\_extend

Extension parameter for hardware specific settings

◆ **lvd\_api\_t**

struct lvd\_api\_t

LVD driver API structure. LVD driver functions implemented at the HAL layer will adhere to this API.

**Data Fields**

fsp\_err\_t(\* open )(lvd\_ctrl\_t \*const p\_ctrl, lvd\_cfg\_t const \*const p\_cfg)

fsp\_err\_t(\* statusGet )(lvd\_ctrl\_t \*const p\_ctrl, lvd\_status\_t \*p\_lvd\_status)

fsp\_err\_t(\* statusClear )(lvd\_ctrl\_t \*const p\_ctrl)

fsp\_err\_t(\* callbackSet )(lvd\_ctrl\_t \*const p\_api\_ctrl, void(\*p\_callback)(lvd\_callback\_args\_t \*), void const \*const p\_context, lvd\_callback\_args\_t \*const p\_callback\_memory)

fsp\_err\_t(\* close )(lvd\_ctrl\_t \*const p\_ctrl)

**Field Documentation**◆ **open**

fsp\_err\_t(\* lvd\_api\_t::open) (lvd\_ctrl\_t \*const p\_ctrl, lvd\_cfg\_t const \*const p\_cfg)

Initializes a low voltage detection driver according to the passed-in configuration structure.

**Implemented as**

- R\_LVD\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure for the driver instance
[in]	p_cfg	Pointer to the configuration structure for the driver instance

◆ **statusGet**

```
fsp_err_t(* lvd_api_t::statusGet) (lvd_ctrl_t *const p_ctrl, lvd_status_t *p_lvd_status)
```

Get the current state of the monitor, (threshold crossing detected, voltage currently above or below threshold). Must be used if the peripheral was initialized with `lvd_response_t` set to `LVD_RESPONSE_NONE`.

**Implemented as**

- `R_LVD_StatusGet()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the control structure for the driver instance
[in,out]	<code>p_lvd_status</code>	Pointer to a <code>lvd_status_t</code> structure

◆ **statusClear**

```
fsp_err_t(* lvd_api_t::statusClear) (lvd_ctrl_t *const p_ctrl)
```

Clears the latched status of the monitor. Must be used if the peripheral was initialized with `lvd_response_t` set to `LVD_RESPONSE_NONE`.

**Implemented as**

- `R_LVD_StatusClear()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the control structure for the driver instance
------	---------------------	--

◆ **callbackSet**

```
fsp_err_t(* lvd_api_t::callbackSet) (lvd_ctrl_t*const p_api_ctrl, void(*p_callback)(lvd_callback_args_t*), void const*const p_context, lvd_callback_args_t*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_LVD\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the LVD control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* lvd_api_t::close) (lvd_ctrl_t*const p_ctrl)
```

Disables the LVD peripheral. Closes the driver instance.

**Implemented as**

- R\_LVD\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the control structure for the driver instance
------	--------	--

◆ **lvd\_instance\_t**

```
struct lvd_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

lvd_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
lvd_cfg_t const *	p_cfg	Pointer to the configuration structure for this interface instance.

`lvd_api_t` const \*`p_api`

Pointer to the API structure for this interface instance.

## Typedef Documentation

### ◆ `lvd_ctrl_t`

typedef void `lvd_ctrl_t`

LVD control block. Allocate an instance specific control block to pass into the LVD API calls.

#### Implemented as

- `lvd_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `lvd_threshold_t`

enum `lvd_threshold_t`Register definitions, common services, and error codes. Voltage detection level The thresholds supported by each MCU are in the MCU User's Manual as well as in the `r_lvd` module description on the stack tab of the RA project.

#### Enumerator

<code>LVD_THRESHOLD_MONITOR_1_LEVEL_4_29V</code>	4.29V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_4_14V</code>	4.14V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_4_02V</code>	4.02V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_3_84V</code>	3.84V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_3_10V</code>	3.10V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_3_00V</code>	3.00V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_90V</code>	2.90V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_79V</code>	2.79V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_68V</code>	2.68V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_58V</code>	2.58V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_48V</code>	2.48V
<code>LVD_THRESHOLD_MONITOR_1_LEVEL_2_20V</code>	2.20V

LVD_THRESHOLD_MONITOR_1_LEVEL_1_96V	1.96V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_86V	1.86V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_75V	1.75V
LVD_THRESHOLD_MONITOR_1_LEVEL_1_65V	1.65V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_99V	2.99V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_92V	2.92V
LVD_THRESHOLD_MONITOR_1_LEVEL_2_85V	2.85V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_29V	4.29V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_14V	4.14V
LVD_THRESHOLD_MONITOR_2_LEVEL_4_02V	4.02V
LVD_THRESHOLD_MONITOR_2_LEVEL_3_84V	3.84V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_99V	2.99V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_92V	2.92V
LVD_THRESHOLD_MONITOR_2_LEVEL_2_85V	2.85V

#### ◆ lvd\_response\_t

enum <code>lvd_response_t</code>	
Response types for handling threshold crossing event.	
Enumerator	
LVD_RESPONSE_NMI	Non-maskable interrupt.
LVD_RESPONSE_INTERRUPT	Maskable interrupt.
LVD_RESPONSE_RESET	Reset.
LVD_RESPONSE_NONE	No response, status must be requested via <code>statusGet</code> function.

◆ **lvd\_voltage\_slope\_t**

enum <code>lvd_voltage_slope_t</code>	
The direction from which Vcc must cross the threshold to trigger a detection (rising, falling, or both).	
Enumerator	
<code>LVD_VOLTAGE_SLOPE_RISING</code>	When VCC $\geq$ Vdet2 (rise) is detected.
<code>LVD_VOLTAGE_SLOPE_FALLING</code>	When VCC $<$ Vdet2 (drop) is detected.
<code>LVD_VOLTAGE_SLOPE_BOTH</code>	When drop and rise are detected.

◆ **lvd\_sample\_clock\_t**

enum <code>lvd_sample_clock_t</code>	
Sample clock divider, use <code>LVD_SAMPLE_CLOCK_DISABLED</code> to disable digital filtering	
Enumerator	
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_2</code>	Digital filter sample clock is LOCO divided by 2.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_4</code>	Digital filter sample clock is LOCO divided by 4.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_8</code>	Digital filter sample clock is LOCO divided by 8.
<code>LVD_SAMPLE_CLOCK_LOCO_DIV_16</code>	Digital filter sample clock is LOCO divided by 16.
<code>LVD_SAMPLE_CLOCK_DISABLED</code>	Digital filter is disabled.

◆ **lvd\_negation\_delay\_t**

enum <code>lvd_negation_delay_t</code>	
Negation delay of LVD reset signal follows reset or voltage in range	
Enumerator	
<code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>	Negation follows a stabilization time ( $t_{LVDn}$ ) after $VCC > V_{det1}$ is detected. If a transition to software standby or deep software standby is to be made, the only possible value for the RN bit is <code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>
<code>LVD_NEGATION_DELAY_FROM_RESET</code>	Negation follows a stabilization time ( $t_{LVDn}$ ) after assertion of the LVDn reset. If a transition to software standby or deep software standby is to be made, the only possible value for the RN bit is <code>LVD_NEGATION_DELAY_FROM_VOLTAGE</code>

◆ **lvd\_threshold\_crossing\_t**

enum <code>lvd_threshold_crossing_t</code>	
Threshold crossing detection (latched)	
Enumerator	
<code>LVD_THRESHOLD_CROSSING_NOT_DETECTED</code>	Threshold crossing has not been detected.
<code>LVD_THRESHOLD_CROSSING_DETECTED</code>	Threshold crossing has been detected.

◆ **lvd\_current\_state\_t**

enum <code>lvd_current_state_t</code>	
Instantaneous status of VCC (above or below threshold)	
Enumerator	
<code>LVD_CURRENT_STATE_BELOW_THRESHOLD</code>	$VCC < \text{threshold}$ .
<code>LVD_CURRENT_STATE_ABOVE_THRESHOLD</code>	$VCC \geq \text{threshold}$ or monitor is disabled.

**4.3.26 OPAMP Interface**

## Interfaces

## Detailed Description

Interface for Operational Amplifiers.

## Summary

The OPAMP interface provides standard operational amplifier functionality, including starting and stopping the amplifier.

Implemented by: [Operational Amplifier \(r\\_opamp\)](#)

### Data Structures

struct [opamp\\_trim\\_args\\_t](#)

struct [opamp\\_info\\_t](#)

struct [opamp\\_status\\_t](#)

struct [opamp\\_cfg\\_t](#)

struct [opamp\\_api\\_t](#)

struct [opamp\\_instance\\_t](#)

### Typedefs

typedef void [opamp\\_ctrl\\_t](#)

### Enumerations

enum [opamp\\_trim\\_cmd\\_t](#)

enum [opamp\\_trim\\_input\\_t](#)

### Data Structure Documentation

#### ◆ [opamp\\_trim\\_args\\_t](#)

struct <a href="#">opamp_trim_args_t</a>		
OPAMP trim arguments.		
Data Fields		
<a href="#">uint8_t</a>	channel	Channel.
<a href="#">opamp_trim_input_t</a>	input	Which input of the channel above.

#### ◆ [opamp\\_info\\_t](#)

struct opamp_info_t		
OPAMP information.		
Data Fields		
uint32_t	min_stabilization_wait_us	Minimum stabilization wait time in microseconds.

## ◆ opamp\_status\_t

struct opamp_status_t		
OPAMP status.		
Data Fields		
uint32_t	operating_channel_mask	Bitmask of channels currently operating.

## ◆ opamp\_cfg\_t

struct opamp_cfg_t		
OPAMP general configuration.		
Data Fields		
void const *	p_extend	Extension parameter for hardware specific settings.

## ◆ opamp\_api\_t

struct opamp_api_t		
OPAMP functions implemented at the HAL layer will follow this API.		
<b>Data Fields</b>		
fsp_err_t(*)	open	(opamp_ctrl_t *const p_ctrl, opamp_cfg_t const *const p_cfg)
fsp_err_t(*)	start	(opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
fsp_err_t(*)	stop	(opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
fsp_err_t(*)	trim	(opamp_ctrl_t *const p_ctrl, opamp_trim_cmd_t const cmd, opamp_trim_args_t const *const p_args)
fsp_err_t(*)	infoGet	(opamp_ctrl_t *const p_ctrl, opamp_info_t *const p_info)
fsp_err_t(*)	statusGet	(opamp_ctrl_t *const p_ctrl, opamp_status_t *const p_status)

```
fsp_err_t(* close )(opamp_ctrl_t *const p_ctrl)
```

## Field Documentation

### ◆ open

```
fsp_err_t(* opamp_api_t::open) (opamp_ctrl_t *const p_ctrl, opamp_cfg_t const *const p_cfg)
```

Initialize the operational amplifier.

#### Implemented as

- R\_OPAMP\_Open()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	p_cfg	Pointer to configuration

### ◆ start

```
fsp_err_t(* opamp_api_t::start) (opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
```

Start the op-amp(s).

#### Implemented as

- R\_OPAMP\_Start()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	channel_mask	Bitmask of channels to start

### ◆ stop

```
fsp_err_t(* opamp_api_t::stop) (opamp_ctrl_t *const p_ctrl, uint32_t const channel_mask)
```

Stop the op-amp(s).

#### Implemented as

- R\_OPAMP\_Stop()

#### Parameters

[in]	p_ctrl	Pointer to instance control block
[in]	channel_mask	Bitmask of channels to stop

## ◆ trim

```
fsp_err_t(* opamp_api_t::trim) (opamp_ctrl_t *const p_ctrl, opamp_trim_cmd_t const cmd,
opamp_trim_args_t const *const p_args)
```

Trim the op-amp(s). Not supported on all MCUs. See implementation for procedure details.

**Implemented as**

- R\_OPAMP\_Trim()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[in]	cmd	Trim command
[in]	p_args	Pointer to arguments for the command

## ◆ infoGet

```
fsp_err_t(* opamp_api_t::infoGet) (opamp_ctrl_t *const p_ctrl, opamp_info_t *const p_info)
```

Provide information such as the recommended minimum stabilization wait time.

**Implemented as**

- R\_OPAMP\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_info	OPAMP information stored here

## ◆ statusGet

```
fsp_err_t(* opamp_api_t::statusGet) (opamp_ctrl_t *const p_ctrl, opamp_status_t *const p_status)
```

Provide status of each op-amp channel.

**Implemented as**

- R\_OPAMP\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
[out]	p_status	Status stored here

◆ **close**

```
fsp_err_t(* opamp_api_t::close) (opamp_ctrl_t *const p_ctrl)
```

Close the specified OPAMP unit by ending any scan in progress, disabling interrupts, and removing power to the specified A/D unit.

**Implemented as**

- R\_OPAMP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to instance control block
------	--------	-----------------------------------

◆ **opamp\_instance\_t**

```
struct opamp_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

opamp_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
opamp_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
opamp_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **opamp\_ctrl\_t**

```
typedef void opamp_ctrl_t
```

OPAMP control block. Allocate using driver instance control structure from driver instance header file.

**Enumeration Type Documentation**

◆ **opamp\_trim\_cmd\_t**

enum <code>opamp_trim_cmd_t</code>	
Includes board and MCU related header files. Trim command.	
Enumerator	
OPAMP_TRIM_CMD_START	Initialize trim state machine.
OPAMP_TRIM_CMD_NEXT_STEP	Move to next step in state machine.
OPAMP_TRIM_CMD_CLEAR_BIT	Clear trim bit.

◆ **opamp\_trim\_input\_t**

enum <code>opamp_trim_input_t</code>	
Trim input.	
Enumerator	
OPAMP_TRIM_INPUT_PCH	Trim non-inverting (+) input.
OPAMP_TRIM_INPUT_NCH	Trim inverting (-) input.

## 4.3.27 PDC Interface

### Interfaces

#### Detailed Description

Interface for PDC functions.

## Summary

The PDC interface provides the functionality for capturing an image from an image sensor/camera. When a capture is complete a transfer complete interrupt is triggered.

Implemented by:

- [Parallel Data Capture \(r\\_pdc\)](#)

#### Data Structures

struct `pdc_callback_args_t`

struct `pdc_cfg_t`

```
struct pdc_api_t
```

```
struct pdc_instance_t
```

## Typedefs

```
typedef void pdc_ctrl_t
```

## Enumerations

```
enum pdc_clock_division_t
```

```
enum pdc_endian_t
```

```
enum pdc_hsync_polarity_t
```

```
enum pdc_vsync_polarity_t
```

```
enum pdc_event_t
```

## Data Structure Documentation

### ◆ pdc\_callback\_args\_t

struct pdc_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">pdc_event_t</a>	event	Event causing the callback.
uint8_t *	p_buffer	Pointer to buffer containing the captured data.
void const *	p_context	Placeholder for user data. Set in <a href="#">pdc_api_t::open</a> function in <a href="#">pdc_cfg_t</a> .

### ◆ pdc\_cfg\_t

struct pdc_cfg_t		
PDC configuration parameters.		
Data Fields		
uint16_t	<a href="#">x_capture_start_pixel</a>	
		Horizontal position to start capture.
uint16_t	<a href="#">x_capture_pixels</a>	
		Number of horizontal pixels to capture.

uint16_t	<a href="#">y_capture_start_pixel</a>
	Vertical position to start capture.
uint16_t	<a href="#">y_capture_pixels</a>
	Number of vertical lines/pixels to capture.
<a href="#">pdc_clock_division_t</a>	<a href="#">clock_division</a>
	Clock divider.
<a href="#">pdc_endian_t</a>	<a href="#">endian</a>
	Endian of capture data.
<a href="#">pdc_hsync_polarity_t</a>	<a href="#">hsync_polarity</a>
	Polarity of HSYNC input.
<a href="#">pdc_vsync_polarity_t</a>	<a href="#">vsync_polarity</a>
	Polarity of VSYNC input.
uint8_t *	<a href="#">p_buffer</a>
	Pointer to buffer to write image into.
uint8_t	<a href="#">bytes_per_pixel</a>
	Number of bytes per pixel.
uint8_t	<a href="#">pdc_ipl</a>
	PDC interrupt priority.

uint8_t	<a href="#">transfer_req_ipl</a>
	Transfer interrupt priority.
IRQn_Type	<a href="#">pdc_irq</a>
	PDC IRQ number.
IRQn_Type	<a href="#">transfer_req_irq</a>
	Transfer request IRQ number.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_lower_lvl_transfer</a>
	Pointer to the transfer instance the PDC should use.
void(*	<a href="#">p_callback</a> )(pdc_callback_args_t *p_args)
	Callback provided when a PDC transfer ISR occurs.
void const *	<a href="#">p_context</a>
	User defined context passed to callback function.
void const *	<a href="#">p_extend</a>
	Placeholder for user data.

#### ◆ pdc\_api\_t

struct pdc_api_t	
PDC functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(pdc_ctrl_t *const p_ctrl, pdc_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )(pdc_ctrl_t *const p_ctrl)

`fsp_err_t(* captureStart )(pdc_ctrl_t *const p_ctrl, uint8_t *const p_buffer)`

## Field Documentation

### ◆ open

`fsp_err_t(* pdc_api_t::open) (pdc_ctrl_t *const p_ctrl, pdc_cfg_t const *const p_cfg)`

Initial configuration.

#### Implemented as

- `R_PDC_Open()`

#### Note

To reconfigure after calling this function, call `pdc_api_t::close` first.

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

### ◆ close

`fsp_err_t(* pdc_api_t::close) (pdc_ctrl_t *const p_ctrl)`

Closes the driver and allows reconfiguration. May reduce power consumption.

#### Implemented as

- `R_PDC_Close()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ captureStart

`fsp_err_t(* pdc_api_t::captureStart) (pdc_ctrl_t *const p_ctrl, uint8_t *const p_buffer)`

Start a capture.

#### Implemented as

- `R_PDC_CaptureStart()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_buffer	Pointer to store captured image data.

### ◆ pdc\_instance\_t

struct pdc_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<a href="#">pdc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">pdc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">pdc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [pdc\\_ctrl\\_t](#)

typedef void <a href="#">pdc_ctrl_t</a>
PDC control block. Allocate an instance specific control block to pass into the PDC API calls.
<b>Implemented as</b>
◦ <a href="#">pdc_instance_ctrl_t</a>

## Enumeration Type Documentation

### ◆ [pdc\\_clock\\_division\\_t](#)

enum <a href="#">pdc_clock_division_t</a>	
Clock divider applied to PDC clock to provide PCKO output frequency	
Enumerator	
PDC_CLOCK_DIVISION_2	CLK / 2.
PDC_CLOCK_DIVISION_4	CLK / 4.
PDC_CLOCK_DIVISION_6	CLK / 6.
PDC_CLOCK_DIVISION_8	CLK / 8.
PDC_CLOCK_DIVISION_10	CLK / 10.
PDC_CLOCK_DIVISION_12	CLK / 12.
PDC_CLOCK_DIVISION_14	CLK / 14.
PDC_CLOCK_DIVISION_16	CLK / 16.

◆ **pdc\_endian\_t**

enum <a href="#">pdc_endian_t</a>	
Endian of captured data	
Enumerator	
PDC_ENDIAN_LITTLE	Data is in little endian format.
PDC_ENDIAN_BIG	Data is in big endian format.

◆ **pdc\_hsync\_polarity\_t**

enum <a href="#">pdc_hsync_polarity_t</a>	
Polarity of input HSYNC signal	
Enumerator	
PDC_HSYNC_POLARITY_HIGH	HSYNC signal is active high.
PDC_HSYNC_POLARITY_LOW	HSYNC signal is active low.

◆ **pdc\_vsync\_polarity\_t**

enum <a href="#">pdc_vsync_polarity_t</a>	
Polarity of input VSYNC signal	
Enumerator	
PDC_VSYNC_POLARITY_HIGH	VSYNC signal is active high.
PDC_VSYNC_POLARITY_LOW	VSYNC signal is active low.

◆ **pdc\_event\_t**

enum <a href="#">pdc_event_t</a>	
PDC events	
Enumerator	
PDC_EVENT_TRANSFER_COMPLETE	Complete frame transferred by DMAC/DTC.
PDC_EVENT_RX_DATA_READY	Receive data ready interrupt.
PDC_EVENT_FRAME_END	Frame end interrupt.
PDC_EVENT_ERR_OVERRUN	Overrun interrupt.
PDC_EVENT_ERR_UNDERRUN	Underrun interrupt.
PDC_EVENT_ERR_V_SET	Vertical line setting error interrupt.
PDC_EVENT_ERR_H_SET	Horizontal byte number setting error interrupt.

**4.3.28 POEG Interface**[Interfaces](#)**Detailed Description**

Interface for the Port Output Enable for GPT.

Defines the API and data structures for the Port Output Enable for GPT (POEG) interface.

**Summary**

The POEG disables GPT output pins based on configurable events.

Implemented by: [Port Output Enable for GPT \(r\\_poeg\)](#)

**Data Structures**

struct [poeg\\_status\\_t](#)

struct [poeg\\_callback\\_args\\_t](#)

struct [poeg\\_cfg\\_t](#)

struct [poeg\\_api\\_t](#)

struct [poeg\\_instance\\_t](#)

## Typedefs

typedef void [poeg\\_ctrl\\_t](#)

## Enumerations

enum [poeg\\_state\\_t](#)

enum [poeg\\_trigger\\_t](#)

enum [poeg\\_gtetrg\\_polarity\\_t](#)

enum [poeg\\_gtetrg\\_noise\\_filter\\_t](#)

## Data Structure Documentation

### ◆ [poeg\\_status\\_t](#)

struct <a href="#">poeg_status_t</a>		
POEG status		
Data Fields		
<a href="#">poeg_state_t</a>	state	Current state of POEG.

### ◆ [poeg\\_callback\\_args\\_t](#)

struct <a href="#">poeg_callback_args_t</a>		
Callback function parameter data.		
Data Fields		
void const *	p_context	Placeholder for user data, set in <a href="#">poeg_cfg_t</a> .

### ◆ [poeg\\_cfg\\_t](#)

struct <a href="#">poeg_cfg_t</a>		
User configuration structure, used in the open function.		
<b>Data Fields</b>		
<a href="#">poeg_trigger_t</a>	trigger	
		Select one or more triggers for the POEG.
<a href="#">poeg_gtetrg_polarity_t</a>	polarity	
		Select the polarity for the GTETRG pin.

<a href="#">poeg_gtetrg_noise_filter_t</a>	<a href="#">noise_filter</a>
	Configure the GTETRG noise filter.
<code>void(*</code>	<code>p_callback )(poeg_callback_args_t *p_args)</code>
<code>void const *</code>	<code>p_context</code>
<code>uint32_t</code>	<code>channel</code>
	Channel 0 corresponds to GTETRGA, 1 to GTETRGA, etc.
<code>IRQn_Type</code>	<code>irq</code>
	NVIC interrupt number assigned to this instance.
<code>uint8_t</code>	<code>ipl</code>
	POEG interrupt priority.

## Field Documentation

### ◆ [p\\_callback](#)

`void(* poeg_cfg_t::p_callback) (poeg\_callback\_args\_t *p_args)`

Callback called when a POEG interrupt occurs.

### ◆ [p\\_context](#)

`void const* poeg_cfg_t::p_context`

Placeholder for user data. Passed to the user callback in [poeg\\_callback\\_args\\_t](#).

### ◆ [poeg\\_api\\_t](#)

`struct poeg_api_t`

Port Output Enable for GPT (POEG) API structure. POEG functions implemented at the HAL layer will follow this API.

#### Data Fields

`fsp_err_t(*` `open) (poeg_ctrl_t *const p_ctrl, poeg\_cfg\_t const *const p_cfg)`

<code>fsp_err_t(*</code>	<code>statusGet )(poeg_ctrl_t *const p_ctrl, poeg_status_t *p_status)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(poeg_ctrl_t *const p_api_ctrl, void(*p_callback)(poeg_callback_args_t *), void const *const p_context, poeg_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>outputDisable )(poeg_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>reset )(poeg_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>close )(poeg_ctrl_t *const p_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* poeg_api_t::open) (poeg_ctrl_t *const p_ctrl, poeg_cfg_t const *const p_cfg)`

Initial configuration.

### Implemented as

- `R_POEG_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **statusGet**

```
fsp_err_t(* poeg_api_t::statusGet) (poeg_ctrl_t *const p_ctrl, poeg_status_t *p_status)
```

Gets the current driver state.

**Implemented as**

- R\_POEG\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
[out]	p_status	Provides the current state of the POEG.

◆ **callbackSet**

```
fsp_err_t(* poeg_api_t::callbackSet) (poeg_ctrl_t *const p_api_ctrl,
void(*p_callback)(poeg_callback_args_t *), void const *const p_context, poeg_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_POEG\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **outputDisable**

```
fsp_err_t(* poeg_api_t::outputDisable) (poeg_ctrl_t *const p_ctrl)
```

Disables GPT output pins by software request.

**Implemented as**

- [R\\_POEG\\_OutputDisable\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
------	--------	---

◆ **reset**

```
fsp_err_t(* poeg_api_t::reset) (poeg_ctrl_t *const p_ctrl)
```

Attempts to clear status flags to reenable GPT output pins. Confirm all status flags are cleared after calling this function by calling [poeg\\_api\\_t::statusGet\(\)](#).

**Implemented as**

- [R\\_POEG\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
------	--------	---

◆ **close**

```
fsp_err_t(* poeg_api_t::close) (poeg_ctrl_t *const p_ctrl)
```

Disables POEG interrupt.

**Implemented as**

- [R\\_POEG\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">poeg_api_t::open</a> call.
------	--------	---

◆ **poeg\_instance\_t**

```
struct poeg_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">poeg_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">poeg_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.

<code>poeg_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.
---------------------------------	--------------------	---

## Typedef Documentation

### ◆ `poeg_ctrl_t`

typedef void <code>poeg_ctrl_t</code>
DOC control block. Allocate an instance specific control block to pass into the DOC API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <code>poeg_instance_ctrl_t</code></li> </ul>

## Enumeration Type Documentation

### ◆ `poeg_state_t`

enum <code>poeg_state_t</code>	
POEG states.	
Enumerator	
<code>POEG_STATE_NO_DISABLE_REQUEST</code>	GPT output is not disabled by POEG.
<code>POEG_STATE_PIN_DISABLE_REQUEST</code>	GPT output disabled due to GTETRGM pin level.
<code>POEG_STATE_GPT_OR_COMPARATOR_DISABLE_REQUEST</code>	GPT output disabled due to high speed analog comparator or GPT.
<code>POEG_STATE_OSCILLATION_STOP_DISABLE_REQUEST</code>	GPT output disabled due to main oscillator stop.
<code>POEG_STATE_SOFTWARE_STOP_DISABLE_REQUEST</code>	GPT output disabled due to <code>poeg_api_t::outputDisable()</code>
<code>POEG_STATE_PIN_DISABLE_REQUEST_ACTIVE</code>	GPT output disable request active from the GTETRGM pin. If a filter is used, this flag represents the state of the filtered input.

## ◆ poeg\_trigger\_t

enum poeg_trigger_t	
Triggers that will disable GPT output pins.	
Enumerator	
POEG_TRIGGER_SOFTWARE	Software disable is always supported with POEG. Select this option if no other triggers are used.
POEG_TRIGGER_PIN	Disable GPT output based on GTETRIG input level.
POEG_TRIGGER_GPT_OUTPUT_LEVEL	Disable GPT output based on GPT output pin levels.
POEG_TRIGGER_OSCILLATION_STOP	Disable GPT output based on main oscillator stop.
POEG_TRIGGER_ACMPHS0	Disable GPT output based on ACMPHS0 comparator result.
POEG_TRIGGER_ACMPHS1	Disable GPT output based on ACMPHS1 comparator result.
POEG_TRIGGER_ACMPHS2	Disable GPT output based on ACMPHS2 comparator result.
POEG_TRIGGER_ACMPHS3	Disable GPT output based on ACMPHS3 comparator result.
POEG_TRIGGER_ACMPHS4	Disable GPT output based on ACMPHS4 comparator result.
POEG_TRIGGER_ACMPHS5	Disable GPT output based on ACMPHS5 comparator result.

◆ **poeg\_gtetrg\_polarity\_t**

enum <a href="#">poeg_gtetrg_polarity_t</a>	
GTETRG polarity.	
Enumerator	
POEG_GTETRG_POLARITY_ACTIVE_HIGH	Disable GPT output based when GTETRG input level is high.
POEG_GTETRG_POLARITY_ACTIVE_LOW	Disable GPT output based when GTETRG input level is low.

◆ **poeg\_gtetrg\_noise\_filter\_t**

enum <a href="#">poeg_gtetrg_noise_filter_t</a>	
GTETRG noise filter. For the input signal to pass through the noise filter, the active level set in <a href="#">poeg_gtetrg_polarity_t</a> must be read 3 consecutive times at the sampling clock selected.	
Enumerator	
POEG_GTETRG_NOISE_FILTER_DISABLED	No noise filter applied to GTETRG input.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_1	Apply noise filter with sample clock PCLKB.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_8	Apply noise filter with sample clock PCLKB/8.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_32	Apply noise filter with sample clock PCLKB/32.
POEG_GTETRG_NOISE_FILTER_PCLKB_DIV_128	Apply noise filter with sample clock PCLKB/128.

**4.3.29 PTP Interface**[Interfaces](#)**Detailed Description**

Interface for PTP functions.

**Summary**

The PTP interface provides the functionality for using PTP.

Implemented by:

- [Precision Time Protocol \(r\\_ptp\)](#)

## Data Structures

struct [ptp\\_clock\\_properties\\_t](#)

struct [ptp\\_time\\_t](#)

struct [ptp\\_message\\_flags\\_t](#)

struct [ptp\\_message\\_header\\_t](#)

struct [ptp\\_message\\_sync\\_t](#)

struct [ptp\\_message\\_pdelay\\_req\\_t](#)

struct [ptp\\_message\\_pdelay\\_resp\\_t](#)

struct [ptp\\_message\\_announce\\_t](#)

struct [ptp\\_message\\_signaling\\_t](#)

struct [ptp\\_message\\_management\\_t](#)

struct [ptp\\_message\\_t](#)

struct [ptp\\_callback\\_args\\_t](#)

struct [ptp\\_pulse\\_timer\\_common\\_cfg\\_t](#)

struct [ptp\\_pulse\\_timer\\_cfg\\_t](#)

struct [ptp\\_sync\\_state\\_cfg\\_t](#)

struct [ptp\\_synfp\\_cfg\\_t](#)

struct [ptp\\_synfp\\_cfg\\_t.ether](#)

struct [ptp\\_synfp\\_cfg\\_t.ipv4](#)

struct [ptp\\_stca\\_cfg\\_t](#)

struct [ptp\\_cfg\\_t](#)

struct [ptp\\_api\\_t](#)

struct [ptp\\_instance\\_t](#)

## Typedefs

```
typedef enum PTP_PACKED ptp_ctrl_field_t  
    e_ptp_ctrl_field
```

```
typedef ptp_message_sync_t ptp_message_delay_req_t
```

```
typedef ptp_message_sync_t ptp_message_follow_up_t
```

```
typedef ptp_message_delay_resp_t  
    ptp_message_pdelay_resp_t
```

```
typedef ptp_message_pdelay_resp_follow_up_t  
    ptp_message_delay_resp_t
```

## Enumerations

```
enum ptp_message_type_t
```

```
enum ptp_port_state_t
```

```
enum ptp_clock_delay_mechanism_t
```

```
enum ptp_frame_format_t
```

```
enum ptp_frame_filter_mode_t
```

```
enum ptp_stca_clock_freq_t
```

```
enum ptp_stca_clock_sel_t
```

```
enum ptp_message_interval_t
```

```
enum ptp_clock_correction_mode_t
```

```
enum ptp_event_t
```

```
enum ptp_ethernet_phy_interface_t
```

## Variables

```
enum PTP_PACKED e_ptp_ctrl_field
```

## Data Structure Documentation

### ◆ ptp\_clock\_properties\_t

```
struct ptp_clock_properties_t
```

Clock properties used in the best master clock algorithm (BMCA) in order to determine the grandmaster clock.

In master mode, these properties will be advertised in announce messages.

Note: The final property used in BMCA is the clock ID. This is usually configured at runtime because it is often based on the hardware address.

Data Fields		
uint8_t	priority1	Priority1 value used in best master calculation.
uint8_t	cclass	Class value.
uint8_t	accuracy	Accuracy of the clock.
uint16_t	variance	Variance of the clock.
uint8_t	priority2	Priority2 value used as secondary priority in best master calculation.

#### ◆ ptp\_time\_t

Data Fields		
uint16_t	seconds_upper	Upper 16 bits of the seconds.
uint32_t	seconds_lower	Lower 32 bits of the seconds.
uint32_t	nanoseconds	Nanoseconds.

#### ◆ ptp\_message\_flags\_t

Data Fields		
uint8_t	message_type: 4	The message type.
uint8_t	sdoid_major: 4	Standard Organization ID Major.
uint8_t	version: 4	PTP Version.
uint8_t	minor_version: 4	PTP Minor Version.
uint16_t	message_length	The total message length (Including the header).
uint8_t	domain	The clock domain.

#### ◆ ptp\_message\_header\_t

Data Fields		
uint8_t	message_type: 4	The message type.
uint8_t	sdoid_major: 4	Standard Organization ID Major.
uint8_t	version: 4	PTP Version.
uint8_t	minor_version: 4	PTP Minor Version.
uint16_t	message_length	The total message length (Including the header).
uint8_t	domain	The clock domain.

uint8_t	sdoid_minor: 8	Standard Organization ID minor.
<a href="#">ptp_message_flags_t</a>	flags	Flags set in the message.
uint64_t	correction_field	Correction Field that is updated when a message passes through a transparent clock.
uint32_t	reserved	
uint8_t	clock_id[8]	Clock ID that the message was sent from.
uint16_t	source_port_id	Port ID that the message was sent from.
uint16_t	sequence_id	Sequence ID of the message.
<a href="#">ptp_ctrl_field_t</a>	control_field	Control field (Message specific).
uint8_t	log_message_interval	Logbase2 of the message period.

◆ **ptp\_message\_sync\_t**

struct ptp_message_sync_t		
Sync Message Type (0x00).		
Data Fields		
<a href="#">ptp_time_t</a>	origin_timestamp	Timestamp when the message was transmitted.

◆ **ptp\_message\_pdelay\_req\_t**

struct ptp_message_pdelay_req_t		
PDelay_req Message Type (0x02).		
Data Fields		
<a href="#">ptp_time_t</a>	origin_timestamp	Timestamp when the message was transmitted.
uint8_t	reserved[10]	

◆ **ptp\_message\_pdelay\_resp\_t**

struct ptp_message_pdelay_resp_t		
PDelay_resp Message Type (0x03).		
Data Fields		
<a href="#">ptp_time_t</a>	origin_timestamp	Timestamp when the message was transmitted.
uint8_t	source_port_identity[10]	Clock ID + sourcePortId.

◆ **ptp\_message\_announce\_t**

--	--	--

struct ptp_message_announce_t		
Announce Message Type (0x0B).		
Data Fields		
ptp_time_t	origin_timestamp	Timestamp when the message was transmitted.
uint16_t	current_utc_offset	Offset from UTC in seconds.
uint8_t	reserved	
ptp_clock_properties_t	clock_properties	Clock properties used in Best Master Clock Algorithm.
uint8_t	clock_id[8]	Clock ID that the message was sent from.
uint16_t	steps_removed	The number of boundary clocks between the clock and the grand master clock.
uint8_t	time_source	The source of time (Eg. INTERNAL_OSC).

#### ◆ ptp\_message\_signaling\_t

struct ptp_message_signaling_t		
Signaling Message Type (0x0C).		
Data Fields		
uint8_t	target_clock_id[8]	ID of the target PTP instance.
uint16_t	target_port_id	Port of the target PTP instance.

#### ◆ ptp\_message\_management\_t

struct ptp_message_management_t		
Management Message Type (0x0D).		
Data Fields		
uint8_t	target_clock_id[8]	ID of the target PTP instance.
uint16_t	target_port_id	Port of the target PTP instance.
uint8_t	starting_boundary_hops	The starting number of times the message is retransmitted by boundary clocks.
uint8_t	boundary_hops	The remaining number of retransmissions.
uint8_t	action	The action that will be taken on reception of the message.
uint8_t	reserved	

#### ◆ ptp\_message\_t

struct ptp_message_t		
Complete PTP Message.		
Data Fields		
ptp_message_header_t	header	Header of the message.
union ptp_message_t	__unnamed__	

#### ◆ ptp\_callback\_args\_t

struct ptp_callback_args_t		
Arguments passed to p_ptp_callback.		
Data Fields		
ptp_event_t	event	Event that caused the callback.
ptp_message_t const *	p_message	The message received (PTP message fields will be little endian).
uint8_t const *	p_tlv_data	Start of TLV data (TLV data will be big endian).
uint16_t	tlv_data_size	Total bytes of TLV data.
uint32_t	pulse_timer_channel	Channel of the pulse timer that caused <a href="#">ptp_event_t::PTP_EVENT_PULSE_TIMER_MINT_RISING_EDGE</a> .
void const *	p_context	Context value set in the configuration.

#### ◆ ptp\_pulse\_timer\_common\_cfg\_t

struct ptp_pulse_timer_common_cfg_t		
Structure for configuring the IPLS IRQ settings that are common to all pulse timer channels.		
Data Fields		
ptp_enable_t	ipls_rising_irq	Enable the IPLS IRQ when a rising edge is detected.
ptp_enable_t	ipls_falling_irq	Enable the IPLS IRQ when a falling edge is detected.
ptp_enable_t	ipls_rising_irq_auto_clear	Auto disable the rising edge IRQ after the first rising edge is detected.
ptp_enable_t	ipls_falling_irq_auto_clear	Auto disable the falling edge IRQ after the first falling edge is detected.

#### ◆ ptp\_pulse\_timer\_cfg\_t

struct ptp_pulse_timer_cfg_t		
------------------------------	--	--

Structure for configuring a pulse timer channel.		
Data Fields		
<a href="#">ptp_time_t</a>	start_time	The exact time when the timer will start.
uint32_t	period	The period of the timer in nanoseconds.
uint32_t	pulse	The pulse width of the timer in nanoseconds.
ptp_enable_t	mint_rising_irq	Enable MINT rising edge IRQ.
ptp_enable_t	ipls_rising_event	Enable IPLS rising edge ELC event.
ptp_enable_t	ipls_falling_event	Enable IPLS falling edge ELC event.
ptp_enable_t	ipls_rising_event_auto_clear	Enable IPLS rising edge ELC event.
ptp_enable_t	ipls_falling_event_auto_clear	Enable IPLS falling edge ELC event.
ptp_enable_t	ipls_irq_source	Enable using this channel as a source for the IPLS IRQ.

#### ◆ ptp\_sync\_state\_cfg\_t

struct ptp_sync_state_cfg_t		
Configuration settings for determining when the PTP clock is synchronized.		
Data Fields		
uint64_t	threshold	The maximum clock offset required to transition between synchronization states.
uint8_t	count	The number of times the clock must be above the threshold in order to transition between synchronization states.

#### ◆ ptp\_synfp\_cfg\_t

struct ptp_synfp_cfg_t		
Configuration settings for the SYNFP.		
Data Fields		
<a href="#">ptp_ethernet_phy_interface_t</a>	ethernet_phy_interface	The type of interface used to communicate with the PHY.
<a href="#">ptp_frame_format_t</a>	frame_format	Frame format used to transport PTP messages.
<a href="#">ptp_frame_filter_mode_t</a>	frame_filter	Frame filter mode.

uint8_t	clock_domain	Clock domain that the clock operates in.
ptp_enable_t	clock_domain_filter	Filter out messages from other clock domains.
ptp_message_interval_t	announce_interval	Interval for transmitting announce messages.
ptp_message_interval_t	sync_interval	Interval for transmitting sync messages.
ptp_message_interval_t	delay_req_interval	Interval for transmitting delay_req messages.
uint32_t	message_timeout	Timeout in milliseconds for receiving PTP messages.
ptp_clock_properties_t	clock_properties	Clock properties used in announce messages.
uint8_t	timesource	TimeSource field used in announce messages.
uint8_t *	p_multicast_addr_filter	Filter for multicast packets.
struct ptp_synfp_cfg_t	ether	Valid if frame_format is set to Ethernet II or IEEE 802.3.
struct ptp_synfp_cfg_t	ipv4	Valid if frame_format is set to IPV4_UDP.

#### ◆ ptp\_synfp\_cfg\_t.ether

struct ptp_synfp_cfg_t.ether		
Valid if frame_format is set to Ethernet II or IEEE 802.3.		
Data Fields		
uint8_t *	p_primary_mac_addr	The MAC address to send primary messages.
uint8_t *	p_pdelay_mac_addr	The MAC address to send p2p messages.

#### ◆ ptp\_synfp\_cfg\_t.ipv4

struct ptp_synfp_cfg_t.ipv4		
Valid if frame_format is set to IPV4_UDP.		
Data Fields		
uint32_t	primary_ip_addr	The IP address to send primary messages.
uint32_t	pdelay_ip_addr	The IP address to send pdelay messages.
uint8_t	event_tos	Type of service for event messages.

uint8_t	general_tos	Type of service for general messages.
uint8_t	primary_ttl	Time to live for primary messages.
uint8_t	pdelay_ttl	Time to live for pdelay messages.
uint16_t	event_udp_port	The port to send event messages.
uint16_t	general_udp_port	The port to send general messages.

#### ◆ ptp\_stca\_cfg\_t

struct ptp_stca_cfg_t		
Configuration settings for the STCA.		
Data Fields		
ptp_stca_clock_freq_t	clock_freq	Select the clock frequency of the STCA.
ptp_stca_clock_sel_t	clock_sel	Select the input clock to the STCA.
ptp_clock_correction_mode_t	clock_correction_mode	Select the clock correction mode.
uint8_t	gradient_worst10_interval	Select the interval for the gradient worst10 acquisition.
ptp_sync_state_cfg_t	sync_threshold	Configure the synchronization threshold.
ptp_sync_state_cfg_t	sync_loss_threshold	Configure the SYNchronization lost threshold.

#### ◆ ptp\_cfg\_t

struct ptp_cfg_t		
User configuration structure, used in open function		
<b>Data Fields</b>		
ptp_synfp_cfg_t	synfp	Configuration settings for the SYNFP.
ptp_stca_cfg_t	stca	Configuration settings for the STCA.

edmac_instance_t *	<a href="#">p_edmac_instance</a>
	Pointer to PTP edmac instance.
uint16_t	<a href="#">buffer_size</a>
	The maximum Ethernet packet size that can be transmitted or received.
uint8_t **	<a href="#">p_rx_buffers</a>
	Pointer to list of buffers used to receive PTP packets.
uint8_t **	<a href="#">p_tx_buffers</a>
	Pointer to list of buffers used to transmit PTP packets.
IRQn_Type	<a href="#">mint_irq</a>
	Interrupt number for PTP event IRQ.
IRQn_Type	<a href="#">ipls_irq</a>
	Interrupt number for PTP timer IRQ.
uint8_t	<a href="#">mint_ipl</a>
	Interrupt priority of the PTP event IRQ.
uint8_t	<a href="#">ipls_ipl</a>
	Interrupt priority of the PTP timer IRQ.
void(*	<a href="#">p_callback</a> )(ptp_callback_args_t *p_args)

## Field Documentation

◆ **p\_callback**

```
void(* ptp_cfg_t::p_callback) (ptp_callback_args_t *p_args)
```

Callback for handling received PTP events.

◆ **ptp\_api\_t**

```
struct ptp_api_t
```

Timer API structure. General timer functions implemented at the HAL layer follow this API.

**Data Fields**

fsp_err_t(*)	<a href="#">open</a> )(ptp_ctrl_t *const p_ctrl, <a href="#">ptp_cfg_t</a> const *const p_cfg)
--------------	--

fsp_err_t(*)	<a href="#">macAddrSet</a> )(ptp_ctrl_t *const p_ctrl, uint8_t const *const p_mac_addr)
--------------	---

fsp_err_t(*)	<a href="#">ipAddrSet</a> )(ptp_ctrl_t *const p_ctrl, uint32_t ip_addr)
--------------	---

fsp_err_t(*)	<a href="#">localClockIdSet</a> )(ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id)
--------------	--

fsp_err_t(*)	<a href="#">masterClockIdSet</a> )(ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id, uint16_t port_id)
--------------	---

fsp_err_t(*)	<a href="#">messageFlagsSet</a> )(ptp_ctrl_t *const p_ctrl, <a href="#">ptp_message_type_t</a> message_type, <a href="#">ptp_message_flags_t</a> flags)
--------------	---

fsp_err_t(*)	<a href="#">currentUtcOffsetSet</a> )(ptp_ctrl_t *const p_ctrl, uint16_t offset)
--------------	--

fsp_err_t(*)	<a href="#">portStateSet</a> )(ptp_ctrl_t *const p_ctrl, uint32_t state)
--------------	--

fsp_err_t(*)	<a href="#">messageSend</a> )(ptp_ctrl_t *const p_ctrl, <a href="#">ptp_message_t</a> const *const p_message, uint8_t const *const p_tlv_data, uint16_t tlv_data_size)
--------------	--

fsp_err_t(*)	<a href="#">localClockValueSet</a> )(ptp_ctrl_t *const p_ctrl, <a href="#">ptp_time_t</a> const *const p_time)
--------------	--

fsp_err_t(*)	<a href="#">localClockValueGet</a> )(ptp_ctrl_t *const p_ctrl, <a href="#">ptp_time_t</a> *const p_time)
--------------	--

<code>fsp_err_t(*</code>	<code>pulseTimerCommonConfig )(ptp_ctrl_t *const p_ctrl, ptp_pulse_timer_common_cfg_t *p_timer_cfg)</code>
<code>fsp_err_t(*</code>	<code>pulseTimerEnable )(ptp_ctrl_t *const p_ctrl, uint32_t channel, ptp_pulse_timer_cfg_t *const p_timer_cfg)</code>
<code>fsp_err_t(*</code>	<code>pulseTimerDisable )(ptp_ctrl_t *const p_ctrl, uint32_t channel)</code>
<code>fsp_err_t(*</code>	<code>close )(ptp_ctrl_t *const p_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* ptp_api_t::open) (ptp_ctrl_t *const p_ctrl, ptp_cfg_t const *const p_cfg)`

Initial configuration.

#### Implemented as

- `R_PTP_Open()`

#### Note

To reconfigure after calling this function, call `ptp_api_t::close` first.

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to pin configuration structure.

### ◆ macAddrSet

`fsp_err_t(* ptp_api_t::macAddrSet) (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_mac_addr)`

Set the MAC address for the PTP.

#### Implemented as

- `R_PTP_MacAddrSet()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_hw_addr</code>	Pointer to the 6 byte MAC address.

◆ **ipAddrSet**

```
fsp_err_t(* ptp_api_t::ipAddrSet) (ptp_ctrl_t *const p_ctrl, uint32_t ip_addr)
```

Set the IP address for the PTP.

**Implemented as**

- R\_PTP\_IpAddrSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	ip_addr	32 bit IPv4 address of the PTP.

◆ **localClockIdSet**

```
fsp_err_t(* ptp_api_t::localClockIdSet) (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id)
```

Set the local clock ID (Usually based off of the PTP MAC address).

**Implemented as**

- R\_PTP\_LocalClockIdSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_clock_id	Pointer to 8 byte clock ID.

◆ **masterClockIdSet**

```
fsp_err_t(* ptp_api_t::masterClockIdSet) (ptp_ctrl_t *const p_ctrl, uint8_t const *const p_clock_id, uint16_t port_id)
```

Set the master clock ID (Usually obtained from previously received announce message).

**Implemented as**

- R\_PTP\_MasterClockIdSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_clock_id	Pointer to 8 byte clock ID.
[in]	port_id	The port on the master clock.

### ◆ messageFlagsSet

```
fsp_err_t(* ptp_api_t::messageFlagsSet) (ptp_ctrl_t *const p_ctrl, ptp_message_type_t message_type, ptp_message_flags_t flags)
```

Set the flags field for the given message type.

#### Implemented as

- R\_PTP\_MessageFlagsSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	message_type	The message type.
[in]	flags	Flags to set.

### ◆ currentUtcOffsetSet

```
fsp_err_t(* ptp_api_t::currentUtcOffsetSet) (ptp_ctrl_t *const p_ctrl, uint16_t offset)
```

Sets the offsetFromMaster field in announce messages.

#### Implemented as

- R\_PTP\_CurrentUtcOffsetSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	offset	New currentUtcOffset value.

### ◆ portStateSet

```
fsp_err_t(* ptp_api_t::portStateSet) (ptp_ctrl_t *const p_ctrl, uint32_t state)
```

Transition to a new clock state.

#### Implemented as

- R\_PTP\_PortStateSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	state	The state to transition into.

### ◆ messageSend

```
fsp_err_t(* ptp_api_t::messageSend) (ptp_ctrl_t *const p_ctrl, ptp_message_t const *const p_message, uint8_t const *const p_tlv_data, uint16_t tlv_data_size)
```

Send a PTP message. Appropriate fields in the PTP message will be endian swapped. The application must ensure that the TLV data is in big endian format.

#### Implemented as

- R\_PTP\_MessageSend()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_message	Pointer to a PTP message.
[in]	p_tlv_data	Pointer to TLV data that is appended to the end of the PTP message.
[in]	tlv_data_size	Size of the TLV data in bytes.

### ◆ localClockValueSet

```
fsp_err_t(* ptp_api_t::localClockValueSet) (ptp_ctrl_t *const p_ctrl, ptp_time_t const *const p_time)
```

Set the local clock value.

#### Implemented as

- R\_PTP\_LocalClockValueSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_time	Pointer to the new time setting.

### ◆ localClockValueGet

```
fsp_err_t(* ptp_api_t::localClockValueGet) (ptp_ctrl_t *const p_ctrl, ptp_time_t *const p_time)
```

Get the local clock value.

#### Implemented as

- R\_PTP\_LocalClockValueGet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_time	Pointer to store the current time setting.

### ◆ pulseTimerCommonConfig

```
fsp_err_t(* ptp_api_t::pulseTimerCommonConfig) (ptp_ctrl_t *const p_ctrl,
ptp_pulse_timer_common_cfg_t *p_timer_cfg)
```

Configuration that is common to all of the pulse timers.

#### Implemented as

- R\_PTP\_PulseTimerCommonConfig()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_timer_cfg	Pointer to the pulse timer common configuration.

### ◆ pulseTimerEnable

```
fsp_err_t(* ptp_api_t::pulseTimerEnable) (ptp_ctrl_t *const p_ctrl, uint32_t channel,
ptp_pulse_timer_cfg_t *const p_timer_cfg)
```

Setup a pulse timer.

#### Implemented as

- R\_PTP\_PulseTimerEnable()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	channel	The pulse timer channel to setup.
[in]	p_timer_cfg	Pointer to the pulse timer configuration.

### ◆ pulseTimerDisable

```
fsp_err_t(* ptp_api_t::pulseTimerDisable) (ptp_ctrl_t *const p_ctrl, uint32_t channel)
```

Stop a pulse timer.

#### Implemented as

- R\_PTP\_PulseTimerDisable()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	channel	The pulse timer channel to stop.

◆ **close**

```
fsp_err_t(* ptp_api_t::close) (ptp_ctrl_t *const p_ctrl)
```

Stop PTP operation.

**Implemented as**

- R\_PTP\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **ptp\_instance\_t**

```
struct ptp_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

ptp_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
ptp_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
ptp_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **ptp\_ctrl\_field\_t**

```
typedef enum PTP_PACKED e_ptp_ctrl_field ptp_ctrl_field_t
```

The control field for PTP message header.

◆ **ptp\_message\_delay\_req\_t**

```
typedef ptp_message_sync_t ptp_message_delay_req_t
```

Delay\_req Message Type (0x01).

◆ **ptp\_message\_follow\_up\_t**

```
typedef ptp_message_sync_t ptp_message_follow_up_t
```

Follow\_up Message Type (0x08).

◆ **ptp\_message\_delay\_resp\_t**typedef [ptp\\_message\\_pdelay\\_resp\\_t](#) [ptp\\_message\\_delay\\_resp\\_t](#)

Delay\_resp Message Type (0x09).

◆ **ptp\_message\_pdelay\_resp\_follow\_up\_t**typedef [ptp\\_message\\_delay\\_resp\\_t](#) [ptp\\_message\\_pdelay\\_resp\\_follow\\_up\\_t](#)

PDelay\_resp\_follow\_up Message Type (0x0A).

**Enumeration Type Documentation**◆ **ptp\_message\_type\_t**enum [ptp\\_message\\_type\\_t](#)

Standard PTP message types.

## Enumerator

PTP_MESSAGE_TYPE_SYNC	Sync Message Type.
PTP_MESSAGE_TYPE_DELAY_REQ	Delay_req Message Type.
PTP_MESSAGE_TYPE_PDELAY_REQ	PDelay_req Message Type.
PTP_MESSAGE_TYPE_PDELAY_RESP	PDelay_resp Message Type.
PTP_MESSAGE_TYPE_FOLLOW_UP	Follow_up Message Type.
PTP_MESSAGE_TYPE_DELAY_RESP	Delay_resp Message Type.
PTP_MESSAGE_TYPE_PDELAY_RESP_FOLLOW_UP	PDelay_resp_follow_up Message Type.
PTP_MESSAGE_TYPE_ANNOUNCE	Announce Message Type.
PTP_MESSAGE_TYPE_SIGNALING	Signaling Message Type.
PTP_MESSAGE_TYPE_MANAGEMENT	Management Message Type.

◆ **ptp\_port\_state\_t**

enum <a href="#">ptp_port_state_t</a>	
Possible states that the PTP instance can be in.	
Enumerator	
PTP_PORT_STATE_GENERATE_ANNOUNCE	Generate Announce Messages.
PTP_PORT_STATE_GENERATE_SYNC	Generate Sync Messages.
PTP_PORT_STATE_GENERATE_DELAY_REQ	Generate Delay_req Messages.
PTP_PORT_STATE_GENERATE_PDELAY_REQ	Generate PDelay_req Messages.
PTP_PORT_STATE_RECEIVE_ANNOUNCE	Receive Announce Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_SYNC	Receive Sync Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_FOLLOW_UP	Receive Follow_up Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_DELAY_REQ	Receive Delay_req Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_DELAY_RESP	Receive Delay_resp Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_PDELAY_REQ	Receive PDelay_req Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_PDELAY_RESP	Receive PDelay_resp Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_PDELAY_RESP_FOLLOW_UP	Receive PDelay_resp_follow_up Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_MANAGEMENT	Receive Management Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_RECEIVE_SIGNALING	Receive Signaling Messages from <a href="#">ptp_cfg_t::p_callback</a> .
PTP_PORT_STATE_PROCESS_SYNC	Enable Sync Message processing.
PTP_PORT_STATE_PROCESS_FOLLOW_UP	Enable Follow_up Message processing.

PTP_PORT_STATE_PROCESS_DELAY_REQ	Enable Delay_req Message processing.
PTP_PORT_STATE_PROCESS_DELAY_RESP	Enable Delay_resp Message processing.
PTP_PORT_STATE_PROCESS_PDELAY_REQ	Enable PDelay_req Message processing.
PTP_PORT_STATE_PROCESS_PDELAY_RESP	Enable PDelay_resp Message processing.
PTP_PORT_STATE_PROCESS_PDELAY_RESP_FOLLOW_UP	Enable PDelay_resp_follow_up Message processing.
PTP_PORT_STATE_PASSIVE	Configure the PTP instance to only receive Announce, Management, and Signaling Messages.
PTP_PORT_STATE_E2E_MASTER	Configure the PTP instance to operate as a E2E Master.
PTP_PORT_STATE_E2E_SLAVE	Configure the PTP instance to operate as a E2E Slave.
PTP_PORT_STATE_P2P_MASTER	Configure the PTP instance to operate as a P2P Master.
PTP_PORT_STATE_P2P_SLAVE	Configure the PTP instance to operate as a P2P Slave.
PTP_PORT_STATE_RECEIVE_ALL	Configure the PTP instance to receive all messages.
PTP_PORT_STATE_DISABLE	Disable all PTP message generation, processing, and reception.

#### ◆ ptp\_clock\_delay\_mechanism\_t

enum <a href="#">ptp_clock_delay_mechanism_t</a>	
The mechanism used for delay messages.	
Enumerator	
PTP_CLOCK_DELAY_MECHANISM_E2E	End to end delay mechanism.
PTP_CLOCK_DELAY_MECHANISM_P2P	Peer to peer delay mechanism.

◆ **ptp\_frame\_format\_t**

enum <code>ptp_frame_format_t</code>	
Frame formats that PTP messages can be encapsulated in.	
Enumerator	
<code>PTP_FRAME_FORMAT_ETHERII</code>	Send PTP messages using Ethernet II frames.
<code>PTP_FRAME_FORMAT_IEEE802_3</code>	Send PTP messages using IEEE802_3 frames.
<code>PTP_FRAME_FORMAT_ETHERII_IPV4_UDP</code>	Send PTP messages using Ethernet II frames with an IP and UDP header.
<code>PTP_FRAME_FORMAT_IEEE802_3_IPV4_UDP</code>	Send PTP messages using IEEE802.3 frames with an IP and UDP header.

◆ **ptp\_frame\_filter\_mode\_t**

enum <code>ptp_frame_filter_mode_t</code>	
Filter PTP messages based on destination MAC address. Messages that pass the filter will be transferred to the ETHERC EDMAC.	
Enumerator	
<code>PTP_FRAME_FILTER_MODE_EXT_PROMISCUOUS_MODE</code>	Receive all packets.
<code>PTP_FRAME_FILTER_MODE_UNICAST_MULTICAST</code>	Receive all unicast packets destined for the PTP and all multicast packets.
<code>PTP_FRAME_FILTER_MODE_UNICAST_MULTICAST_FILTERED</code>	Receive Unicast packets destined for the PTP and filter configured multicast packets.
<code>PTP_FRAME_FILTER_MODE_UNICAST</code>	Receive unicast packets destined for the PTP.

◆ **ptp\_stca\_clock\_freq\_t**

enum <code>ptp_stca_clock_freq_t</code>	
STCA input clock frequency.	
Enumerator	
<code>PTP_STCA_CLOCK_FREQ_20MHZ</code>	20 Mhz Input Clock
<code>PTP_STCA_CLOCK_FREQ_25MHZ</code>	25 Mhz Input Clock
<code>PTP_STCA_CLOCK_FREQ_50MHZ</code>	50 Mhz Input Clock
<code>PTP_STCA_CLOCK_FREQ_100MHZ</code>	100 Mhz Input Clock

◆ **ptp\_stca\_clock\_sel\_t**

enum <code>ptp_stca_clock_sel_t</code>	
STCA input clock selection.	
Enumerator	
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_1</code>	PCLKA.
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_2</code>	PCLKA Divided by 2.
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_3</code>	PCLKA Divided by 3.
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_4</code>	PCLKA Divided by 4.
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_5</code>	PCLKA Divided by 5.
<code>PTP_STCA_CLOCK_SEL_PCLKA_DIV_6</code>	PCLKA Divided by 6.
<code>PTP_STCA_CLOCK_SEL_REF50CK0</code>	50-MHz Reference Signal for timing in RMII mode (STCA clock frequency is 25 Mhz when REF50CK0 is used).

◆ **ptp\_message\_interval\_t**

enum <code>ptp_message_interval_t</code>	
Message interval for transmitting PTP messages.	
Enumerator	
<code>PTP_MESSAGE_INTERVAL_1_128</code>	1 / 128 seconds
<code>PTP_MESSAGE_INTERVAL_1_64</code>	1 / 64 seconds
<code>PTP_MESSAGE_INTERVAL_1_32</code>	1 / 32 seconds
<code>PTP_MESSAGE_INTERVAL_1_16</code>	1 / 16 seconds
<code>PTP_MESSAGE_INTERVAL_1_8</code>	1 / 8 seconds
<code>PTP_MESSAGE_INTERVAL_1_4</code>	1 / 4 seconds
<code>PTP_MESSAGE_INTERVAL_1_2</code>	1 / 2 seconds
<code>PTP_MESSAGE_INTERVAL_1</code>	1 seconds
<code>PTP_MESSAGE_INTERVAL_2</code>	2 seconds
<code>PTP_MESSAGE_INTERVAL_4</code>	4 seconds
<code>PTP_MESSAGE_INTERVAL_8</code>	8 seconds
<code>PTP_MESSAGE_INTERVAL_16</code>	16 seconds
<code>PTP_MESSAGE_INTERVAL_32</code>	32 seconds
<code>PTP_MESSAGE_INTERVAL_64</code>	64 seconds

◆ **ptp\_clock\_correction\_mode\_t**

enum <code>ptp_clock_correction_mode_t</code>	
Clock correction mode.	
Enumerator	
<code>PTP_CLOCK_CORRECTION_MODE1</code>	Correct the local clock using the current <code>offsetFromMaster</code> value.
<code>PTP_CLOCK_CORRECTION_MODE2</code>	Correct the local clock using the calculated clock gradient.

◆ **ptp\_event\_t**

enum <code>ptp_event_t</code>	
PTP events provided by <code>ptp_cfg_t::p_callback</code> .	
Enumerator	
<code>PTP_EVENT_SYNC_ACQUIRED</code>	The local clock is synchronized to the master clock.
<code>PTP_EVENT_SYNC_LOST</code>	The local clock is not synchronized to the master clock.
<code>PTP_EVENT_SYNC_MESSAGE_TIMEOUT</code>	A sync message has not been received for the configured time.
<code>PTP_EVENT_WORST10_ACQUIRED</code>	Gradient worst10 values has been calculated.
<code>PTP_EVENT_OFFSET_FROM_MASTER_UPDATED</code>	The offset from the master clock has been updated.
<code>PTP_EVENT_LOG_MESSAGE_INT_CHANGED</code>	The message interval was changed.
<code>PTP_EVENT_MEAN_PATH_DELAY_UPDATED</code>	The mean path delay has been updated.
<code>PTP_EVENT_DELAY_RESP_TIMEOUT</code>	A <code>delay_resp</code> has not been received for the configured time.
<code>PTP_EVENT_LOG_MESSAGE_INT_OUT_OF_RANGE</code>	The updated message interval is out of range.
<code>PTP_EVENT_DELAY_REQ_FIFO_OVERFLOW</code>	The FIFO buffer for storing information from received <code>Delay_Req</code> messages holds 32 or more entries.
<code>PTP_EVENT_LOOP_RECEPTION_DETECTED</code>	A packet with the same sourcePortIdentity as the local clock was received.
<code>PTP_EVENT_CTRL_INFO_ABNORMALITY</code>	A malformed frame was received (EDMAC, ETHERC, and EPTPC must be reset).
<code>PTP_EVENT_DELAY_RESP_PROCESSING_HALTED</code>	Processing of <code>delay_resp</code> messages has been halted.
<code>PTP_EVENT_MESSAGE_GENERATION_HALTED</code>	Generation of messages has been halted.
<code>PTP_EVENT_MESSAGE_RECEIVED</code>	A PTP message was received from the EDMAC.
<code>PTP_EVENT_MESSAGE_TRANSMIT_COMPLETE</code>	A PTP message has been transmitted.

PTP_EVENT_PULSE_TIMER_MINT_RISING_EDGE	A rising edge occurred on a pulse timer channel.
PTP_EVENT_PULSE_TIMER_IPLS_COMMON	A rising or falling edge occurred on any pulse timer channel.

#### ◆ ptp\_ethernet\_phy\_interface\_t

enum ptp_ethernet_phy_interface_t	
The Ethernet PHY interface type.	
Enumerator	
PTP_ETHERNET_PHY_INTERFACE_MII	Media-independant interface.
PTP_ETHERNET_PHY_INTERFACE_RMII	Reduced media-independant interface.

### Variable Documentation

#### ◆ e\_ptp\_ctrl\_field

enum PTP_PACKED e_ptp_ctrl_field
The control field for PTP message header.

## 4.3.30 RTC Interface

### Interfaces

#### Detailed Description

Interface for accessing the Realtime Clock.

## Summary

The RTC Interface is for configuring Real Time Clock (RTC) functionality including alarm, periodic notification and error adjustment.

The Real Time Clock Interface can be implemented by:

- [Realtime Clock \(r\\_rtc\)](#)

#### Data Structures

```
struct rtc_callback_args_t
```

struct [rtc\\_error\\_adjustment\\_cfg\\_t](#)

struct [rtc\\_alarm\\_time\\_t](#)

struct [rtc\\_info\\_t](#)

struct [rtc\\_cfg\\_t](#)

struct [rtc\\_api\\_t](#)

struct [rtc\\_instance\\_t](#)

## Typedefs

typedef struct tm [rtc\\_time\\_t](#)

typedef void [rtc\\_ctrl\\_t](#)

## Enumerations

enum [rtc\\_event\\_t](#)

enum [rtc\\_clock\\_source\\_t](#)

enum [rtc\\_status\\_t](#)

enum [rtc\\_error\\_adjustment\\_t](#)

enum [rtc\\_error\\_adjustment\\_mode\\_t](#)

enum [rtc\\_error\\_adjustment\\_period\\_t](#)

enum [rtc\\_periodic\\_irq\\_select\\_t](#)

## Data Structure Documentation

### ◆ [rtc\\_callback\\_args\\_t](#)

struct <a href="#">rtc_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">rtc_event_t</a>	event	The event can be used to identify what caused the callback (compare match or error).
void const *	p_context	Placeholder for user data.

### ◆ [rtc\\_error\\_adjustment\\_cfg\\_t](#)

struct rtc_error_adjustment_cfg_t		
Time error adjustment value configuration		
Data Fields		
<a href="#">rtc_error_adjustment_mode_t</a>	adjustment_mode	Automatic Adjustment Enable/Disable.
<a href="#">rtc_error_adjustment_period_t</a>	adjustment_period	Error Adjustment period.
<a href="#">rtc_error_adjustment_t</a>	adjustment_type	Time error adjustment setting.
uint32_t	adjustment_value	Value of the prescaler for error adjustment.

◆ **rtc\_alarm\_time\_t**

struct rtc_alarm_time_t		
Alarm time setting structure		
Data Fields		
<a href="#">rtc_time_t</a>	time	Time structure.
bool	sec_match	Enable the alarm based on a match of the seconds field.
bool	min_match	Enable the alarm based on a match of the minutes field.
bool	hour_match	Enable the alarm based on a match of the hours field.
bool	mday_match	Enable the alarm based on a match of the days field.
bool	mon_match	Enable the alarm based on a match of the months field.
bool	year_match	Enable the alarm based on a match of the years field.
bool	dayofweek_match	Enable the alarm based on a match of the dayofweek field.

◆ **rtc\_info\_t**

struct rtc_info_t		
RTC Information Structure for information returned by infoGet()		
Data Fields		
<a href="#">rtc_clock_source_t</a>	clock_source	Clock source for the RTC block.
<a href="#">rtc_status_t</a>	status	RTC run status.

◆ **rtc\_cfg\_t**

struct rtc_cfg_t		
User configuration structure, used in open function		

Data Fields	
<code>rtc_clock_source_t</code>	<code>clock_source</code>
	Clock source for the RTC block.
<code>uint32_t</code>	<code>freq_compare_value_loco</code>
	The frequency comparison value for LOCO.
<code>rtc_error_adjustment_cfg_t</code> <code>const *const</code>	<code>p_err_cfg</code>
	Pointer to Error Adjustment configuration.
<code>uint8_t</code>	<code>alarm_ipl</code>
	Alarm interrupt priority.
<code>IRQn_Type</code>	<code>alarm_irq</code>
	Alarm interrupt vector.
<code>uint8_t</code>	<code>periodic_ipl</code>
	Periodic interrupt priority.
<code>IRQn_Type</code>	<code>periodic_irq</code>
	Periodic interrupt vector.
<code>uint8_t</code>	<code>carry_ipl</code>
	Carry interrupt priority.
<code>IRQn_Type</code>	<code>carry_irq</code>
	Carry interrupt vector.

void(*	<a href="#">p_callback</a> )(rtc_callback_args_t *p_args)
	Called from the ISR.
void const *	<a href="#">p_context</a>
	User defined context passed into callback function.
void const *	<a href="#">p_extend</a>
	RTC hardware dependant configuration.

#### ◆ rtc\_api\_t

struct rtc_api_t	
RTC driver structure. General RTC functions implemented at the HAL layer follow this API.	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_cfg_t</a> const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(rtc_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">calendarTimeSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_time_t</a> *const p_time)
fsp_err_t(*	<a href="#">calendarTimeGet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_time_t</a> *const p_time)
fsp_err_t(*	<a href="#">calendarAlarmSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_alarm_time_t</a> *const p_alarm)
fsp_err_t(*	<a href="#">calendarAlarmGet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_alarm_time_t</a> *const p_alarm)
fsp_err_t(*	<a href="#">periodicIrqRateSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_periodic_irq_select_t</a> const rate)
fsp_err_t(*	<a href="#">errorAdjustmentSet</a> )(rtc_ctrl_t *const p_ctrl, <a href="#">rtc_error_adjustment_cfg_t</a> const *const err_adj_cfg)

<code>fsp_err_t(*</code>	<code>callbackSet )(rtc_ctrl_t *const p_ctrl, void(*p_callback)(rtc_callback_args_t *), void const *const p_context, rtc_callback_args_t *const p_callback_memory)</code>
--------------------------	---

<code>fsp_err_t(*</code>	<code>infoGet )(rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info)</code>
--------------------------	--

## Field Documentation

### ◆ open

<code>fsp_err_t(* rtc_api_t::open) (rtc_ctrl_t *const p_ctrl, rtc_cfg_t const *const p_cfg)</code>
--

Open the RTC driver.

#### Implemented as

- [R\\_RTC\\_Open\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to RTC device handle
[in]	p_cfg	Pointer to the configuration structure

### ◆ close

<code>fsp_err_t(* rtc_api_t::close) (rtc_ctrl_t *const p_ctrl)</code>
---

Close the RTC driver.

#### Implemented as

- [R\\_RTC\\_Close\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to RTC device handle.
------	--------	-------------------------------

◆ **calendarTimeSet**

```
fsp_err_t(* rtc_api_t::calendarTimeSet) (rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time)
```

Set the calendar time and start the calendar counter

**Implemented as**

- [R\\_RTC\\_CalendarTimeSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	p_time	Pointer to a time structure that contains the time to set
[in]	clock_start	Flag that starts the clock right after it is set

◆ **calendarTimeGet**

```
fsp_err_t(* rtc_api_t::calendarTimeGet) (rtc_ctrl_t *const p_ctrl, rtc_time_t *const p_time)
```

Get the calendar time.

**Implemented as**

- [R\\_RTC\\_CalendarTimeGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[out]	p_time	Pointer to a time structure that contains the time to get

◆ **calendarAlarmSet**

```
fsp_err_t(* rtc_api_t::calendarAlarmSet) (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
```

Set the calendar alarm time and enable the alarm interrupt.

**Implemented as**

- [R\\_RTC\\_CalendarAlarmSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	p_alarm	Pointer to an alarm structure that contains the alarm time to set
[in]	irq_enable_flag	Enable the ALARM irq if set

◆ **calendarAlarmGet**

```
fsp_err_t(* rtc_api_t::calendarAlarmGet) (rtc_ctrl_t *const p_ctrl, rtc_alarm_time_t *const p_alarm)
```

Get the calendar alarm time.

**Implemented as**

- [R\\_RTC\\_CalendarAlarmGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[out]	p_alarm	Pointer to an alarm structure to fill up with the alarm time

◆ **periodicIrqRateSet**

```
fsp_err_t(* rtc_api_t::periodicIrqRateSet) (rtc_ctrl_t *const p_ctrl, rtc_periodic_irq_select_t const rate)
```

Set the periodic irq rate

**Implemented as**

- [R\\_RTC\\_PeriodicIrqRateSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to RTC device handle
[in]	rate	Rate of periodic interrupts

◆ **errorAdjustmentSet**

```
fsp_err_t(* rtc_api_t::errorAdjustmentSet) (rtc_ctrl_t *const p_ctrl, rtc_error_adjustment_cfg_t const *const err_adj_cfg)
```

Set time error adjustment.

**Implemented as**

- [R\\_RTC\\_ErrorAdjustmentSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	err_adj_cfg	Pointer to the Error Adjustment Config

◆ **callbackSet**

```
fsp_err_t(* rtc_api_t::callbackSet) (rtc_ctrl_t *const p_ctrl, void(*p_callback)(rtc_callback_args_t *),
void const *const p_context, rtc_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_RTC\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the RTC control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated

◆ **infoGet**

```
fsp_err_t(* rtc_api_t::infoGet) (rtc_ctrl_t *const p_ctrl, rtc_info_t *const p_rtc_info)
```

Return the currently configure clock source for the RTC

**Implemented as**

- [R\\_RTC\\_InfoGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[out]	p_rtc_info	Pointer to RTC information structure

◆ **rtc\_instance\_t**

```
struct rtc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">rtc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rtc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rtc_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ rtc\_time\_t

```
typedef struct tm rtc_time_t
```

Date and time structure defined in C standard library <time.h>

### ◆ rtc\_ctrl\_t

```
typedef void rtc_ctrl_t
```

RTC control block. Allocate an instance specific control block to pass into the RTC API calls.

#### Implemented as

- [rtc\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ rtc\_event\_t

```
enum rtc_event_t
```

Events that can trigger a callback function

Enumerator

RTC\_EVENT\_ALARM\_IRQ

Real Time Clock ALARM IRQ.

RTC\_EVENT\_PERIODIC\_IRQ

Real Time Clock PERIODIC IRQ.

### ◆ rtc\_clock\_source\_t

```
enum rtc_clock_source_t
```

Clock source for the RTC block

Enumerator

RTC\_CLOCK\_SOURCE\_SUBCLK

Sub-clock oscillator.

RTC\_CLOCK\_SOURCE\_LOCO

Low power On Chip Oscillator.

◆ **rtc\_status\_t**

enum <code>rtc_status_t</code>	
RTC run state	
Enumerator	
<code>RTC_STATUS_STOPPED</code>	RTC counter is stopped.
<code>RTC_STATUS_RUNNING</code>	RTC counter is running.

◆ **rtc\_error\_adjustment\_t**

enum <code>rtc_error_adjustment_t</code>	
Time error adjustment settings	
Enumerator	
<code>RTC_ERROR_ADJUSTMENT_NONE</code>	Adjustment is not performed.
<code>RTC_ERROR_ADJUSTMENT_ADD_PRESCALER</code>	Adjustment is performed by the addition to the prescaler.
<code>RTC_ERROR_ADJUSTMENT_SUBTRACT_PRESCALER</code>	Adjustment is performed by the subtraction from the prescaler.

◆ **rtc\_error\_adjustment\_mode\_t**

enum <code>rtc_error_adjustment_mode_t</code>	
Time error adjustment mode settings	
Enumerator	
<code>RTC_ERROR_ADJUSTMENT_MODE_MANUAL</code>	Adjustment mode is set to manual.
<code>RTC_ERROR_ADJUSTMENT_MODE_AUTOMATIC</code>	Adjustment mode is set to automatic.

◆ **rtc\_error\_adjustment\_period\_t**

enum <a href="#">rtc_error_adjustment_period_t</a>	
Time error adjustment period settings	
Enumerator	
RTC_ERROR_ADJUSTMENT_PERIOD_1_MINUTE	Adjustment period is set to every one minute.
RTC_ERROR_ADJUSTMENT_PERIOD_10_SECOND	Adjustment period is set to every ten second.
RTC_ERROR_ADJUSTMENT_PERIOD_NONE	Adjustment period not supported in manual mode.

◆ **rtc\_periodic\_irq\_select\_t**

enum <a href="#">rtc_periodic_irq_select_t</a>	
Periodic Interrupt select	
Enumerator	
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_256_SECONDS	A periodic irq is generated every 1/256 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_128_SECONDS	A periodic irq is generated every 1/128 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_64_SECONDS	A periodic irq is generated every 1/64 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_32_SECONDS	A periodic irq is generated every 1/32 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_16_SECONDS	A periodic irq is generated every 1/16 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_8_SECONDS	A periodic irq is generated every 1/8 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_4_SECONDS	A periodic irq is generated every 1/4 second.
RTC_PERIODIC_IRQ_SELECT_1_DIV_BY_2_SECONDS	A periodic irq is generated every 1/2 second.
RTC_PERIODIC_IRQ_SELECT_1_SECOND	A periodic irq is generated every 1 second.
RTC_PERIODIC_IRQ_SELECT_2_SECONDS	A periodic irq is generated every 2 seconds.

## 4.3.31 SD/MMC Interface

### Interfaces

#### Detailed Description

Interface for accessing SD, eMMC, and SDIO devices.

## Summary

The `r_sdhi` interface provides standard SD and eMMC media functionality. This interface also supports SDIO.

The SD/MMC interface is implemented by:

- SD/MMC Host Interface (`r_sdhi`)

#### Data Structures

struct `sdmmc_status_t`

struct `sdmmc_device_t`

struct `sdmmc_callback_args_t`

struct `sdmmc_cfg_t`

struct `sdmmc_api_t`

struct `sdmmc_instance_t`

#### Typedefs

typedef void `sdmmc_ctrl_t`

#### Enumerations

enum `sdmmc_card_type_t`

enum `sdmmc_bus_width_t`

enum `sdmmc_io_transfer_mode_t`

enum `sdmmc_io_address_mode_t`

enum `sdmmc_io_write_mode_t`

enum `sdmmc_event_t`

enum `sdmmc_card_detect_t`

enum [sdmmc\\_write\\_protect\\_t](#)enum [sdmmc\\_r1\\_state\\_t](#)

## Data Structure Documentation

### ◆ [sdmmc\\_status\\_t](#)

struct <a href="#">sdmmc_status_t</a>		
Current status.		
Data Fields		
bool	initialized	False if card was removed (only applies if MCU supports card detection and SDnCD pin is connected), true otherwise.  If ready is false, call <a href="#">sdmmc_api_t::medialnit</a> to reinitialize it
bool	transfer_in_progress	true = Card is busy
bool	card_inserted	Card detect status, true if card detect is not used.

### ◆ [sdmmc\\_device\\_t](#)

struct <a href="#">sdmmc_device_t</a>		
Information obtained from the media device.		
Data Fields		
<a href="#">sdmmc_card_type_t</a>	card_type	SD, eMMC, or SDIO.
bool	write_protected	true = Card is write protected
uint32_t	clock_rate	Current clock rate.
uint32_t	sector_count	Sector count.
uint32_t	sector_size_bytes	Sector size.
uint32_t	erase_sector_count	Minimum erasable unit (in 512 byte sectors)

### ◆ [sdmmc\\_callback\\_args\\_t](#)

struct <a href="#">sdmmc_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">sdmmc_event_t</a>	event	The event can be used to identify what caused the callback.

sdmmc_response_t	response	Response from card, only valid if SDMMC_EVENT_RESPONSE is set in event.
void const *	p_context	Placeholder for user data.

◆ **sdmmc\_cfg\_t**

struct sdmmc_cfg_t		
SD/MMC Configuration		
<b>Data Fields</b>		
uint8_t	channel	
		Channel of SD/MMC host interface.
sdmmc_bus_width_t	bus_width	
		Device bus width is 1, 4 or 8 bits wide.
transfer_instance_t const *	p_lower_lvl_transfer	
		Transfer instance used to move data with DMA or DTC.
void(*	p_callback )(sdmmc_callback_args_t *p_args)	
		Pointer to callback function.
void const *	p_context	
		User defined context passed into callback function.
void const *	p_extend	
		SD/MMC hardware dependent configuration.
uint32_t	block_size	
sdmmc_card_detect_t	card_detect	

<code>sdmcc_write_protect_t</code>	<code>write_protect</code>
<code>IRQn_Type</code>	<code>access_irq</code>
	Access IRQ number.
<code>IRQn_Type</code>	<code>sdio_irq</code>
	SDIO IRQ number.
<code>IRQn_Type</code>	<code>card_irq</code>
	Card IRQ number.
<code>IRQn_Type</code>	<code>dma_req_irq</code>
	DMA request IRQ number.
<code>uint8_t</code>	<code>access_ipl</code>
	Access interrupt priority.
<code>uint8_t</code>	<code>sdio_ipl</code>
	SDIO interrupt priority.
<code>uint8_t</code>	<code>card_ipl</code>
	Card interrupt priority.
<code>uint8_t</code>	<code>dma_req_ipl</code>
	DMA request interrupt priority.
<b>Field Documentation</b>	

◆ **block\_size**

uint32\_t sdmmc\_cfg\_t::block\_size

Block size in bytes. Block size must be 512 bytes for SD cards and eMMC devices. Block size can be 1-512 bytes for SDIO.

◆ **card\_detect**

sdmmc\_card\_detect\_t sdmmc\_cfg\_t::card\_detect

Whether or not card detection is used.

◆ **write\_protect**

sdmmc\_write\_protect\_t sdmmc\_cfg\_t::write\_protect

Select whether or not to use the write protect pin. Select Not Used if the MCU or device does not have a write protect pin.

◆ **sdmmc\_api\_t**

struct sdmmc\_api\_t

SD/MMC functions implemented at the HAL layer API.

**Data Fields**

fsp_err_t(*)	<a href="#">open</a> )(sdmmc_ctrl_t *const p_ctrl, sdmmc_cfg_t const *const p_cfg)
fsp_err_t(*)	<a href="#">mediaInit</a> )(sdmmc_ctrl_t *const p_ctrl, sdmmc_device_t *const p_device)
fsp_err_t(*)	<a href="#">read</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t(*)	<a href="#">write</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source, uint32_t const start_sector, uint32_t const sector_count)
fsp_err_t(*)	<a href="#">readlo</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address)
fsp_err_t(*)	<a href="#">writel0</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
fsp_err_t(*)	<a href="#">readloExt</a> )(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t transfer_mode,

	<code>sdmmc_io_address_mode_t address_mode)</code>
<code>fsp_err_t(*</code>	<code>writelExt )(sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source, uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t transfer_mode, sdmmc_io_address_mode_t address_mode)</code>
<code>fsp_err_t(*</code>	<code>ioIntEnable )(sdmmc_ctrl_t *const p_ctrl, bool enable)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(sdmmc_ctrl_t *const p_ctrl, sdmmc_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>erase )(sdmmc_ctrl_t *const p_ctrl, uint32_t const start_sector, uint32_t const sector_count)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(sdmmc_ctrl_t *const p_api_ctrl, void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(sdmmc_ctrl_t *const p_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* sdmmc_api_t::open) (sdmmc_ctrl_t *const p_ctrl, sdmmc_cfg_t const *const p_cfg)`

Open the SD/MMC driver.

### Implemented as

- `R_SDHI_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to SD/MMC instance control block.
[in]	<code>p_cfg</code>	Pointer to SD/MMC instance configuration structure.

◆ **medialnit**

```
fsp_err_t(* sdmmc_api_t::medialnit) (sdmmc_ctrl_t *const p_ctrl, sdmmc_device_t *const p_device)
```

Initializes an SD/MMC device. If the device is a card, the card must be plugged in prior to calling this API. This API blocks until the device initialization procedure is complete.

**Implemented as**

- [R\\_SDHI\\_Medialnit\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to SD/MMC instance control block.
[out]	p_device	Pointer to store device information.

◆ **read**

```
fsp_err_t(* sdmmc_api_t::read) (sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const start_sector, uint32_t const sector_count)
```

Read data from an SD/MMC channel. This API is not supported for SDIO devices.

**Implemented as**

- [R\\_SDHI\\_Read\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_dest	Pointer to data buffer to read data to.
[in]	start_sector	First sector address to read.
[in]	sector_count	Number of sectors to read. All sectors must be in the range of <a href="#">sdmmc_device_t::sector_count</a> .

## ◆ write

```
fsp_err_t(*sdmmc_api_t::write)(sdmmc_ctrl_t*const p_ctrl, uint8_t const*const p_source, uint32_t const start_sector, uint32_t const sector_count)
```

Write data to SD/MMC channel. This API is not supported for SDIO devices.

**Implemented as**

- R\_SDHI\_Write()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	p_source	Pointer to data buffer to write data from.
[in]	start_sector	First sector address to write to.
[in]	sector_count	Number of sectors to write. All sectors must be in the range of <code>sdmmc_device_t::sector_count</code> .

## ◆ readlo

```
fsp_err_t(*sdmmc_api_t::readlo)(sdmmc_ctrl_t*const p_ctrl, uint8_t*const p_data, uint32_t const function, uint32_t const address)
```

Read one byte of I/O data from an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_Readlo()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_data	Pointer to location to store data byte.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.

◆ **writel0**

```
fsp_err_t(*sdmmc_api_t::writel0)(sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_data, uint32_t const
function, uint32_t const address, sdmmc_io_write_mode_t const read_after_write)
```

Write one byte of I/O data to an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_Writel0()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in,out]	p_data	Pointer to data byte to write. Read data is also provided here if read_after_write is true.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.
[in]	read_after_write	Whether or not to read back the same register after writing

## ◆ readloExt

```
fsp_err_t(* sdmmc_api_t::readloExt) (sdmmc_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t
const function, uint32_t const address, uint32_t *const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode)
```

Read multiple bytes or blocks of I/O data from an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_ReadloExt()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_dest	Pointer to data buffer to read data to.
[in]	function	SDIO Function Number.
[in]	address	SDIO register address.
[in]	count	Number of bytes or blocks to read, maximum 512 bytes or 511 blocks.
[in]	transfer_mode	Byte or block mode
[in]	address_mode	Fixed or incrementing address mode

◆ **writeloExt**

```
fsp_err_t(* sdmmc_api_t::writeloExt) (sdmmc_ctrl_t *const p_ctrl, uint8_t const *const p_source,
uint32_t const function, uint32_t const address, uint32_t const count, sdmmc_io_transfer_mode_t
transfer_mode, sdmmc_io_address_mode_t address_mode)
```

Write multiple bytes or blocks of I/O data to an SDIO device. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_WriteloExt()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	p_source	Pointer to data buffer to write data from.
[in]	function_number	SDIO Function Number.
[in]	address	SDIO register address.
[in]	count	Number of bytes or blocks to write, maximum 512 bytes or 511 blocks.
[in]	transfer_mode	Byte or block mode
[in]	address_mode	Fixed or incrementing address mode

◆ **ioIntEnable**

```
fsp_err_t(* sdmmc_api_t::ioIntEnable) (sdmmc_ctrl_t *const p_ctrl, bool enable)
```

Enables SDIO interrupt for SD/MMC instance. This API is not supported for SD or eMMC memory devices.

**Implemented as**

- R\_SDHI\_IoIntEnable

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	enable	Interrupt enable = true, interrupt disable = false.

◆ **statusGet**

```
fsp_err_t(* sdmmc_api_t::statusGet) (sdmmc_ctrl_t *const p_ctrl, sdmmc_status_t *const p_status)
```

Get SD/MMC device status.

**Implemented as**

- [R\\_SDHI\\_StatusGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[out]	p_status	Pointer to current driver status.

◆ **erase**

```
fsp_err_t(* sdmmc_api_t::erase) (sdmmc_ctrl_t *const p_ctrl, uint32_t const start_sector, uint32_t const sector_count)
```

Erase SD/MMC sectors. The sector size for erase is fixed at 512 bytes. This API is not supported for SDIO devices.

**Implemented as**

- [R\\_SDHI\\_Erase](#)

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
[in]	start_sector	First sector to erase. Must be a multiple of <a href="#">sdmmc_device_t::erase_sector_count</a> .
[in]	sector_count	Number of sectors to erase. Must be a multiple of <a href="#">sdmmc_device_t::erase_sector_count</a> . All sectors must be in the range of <a href="#">sdmmc_device_t::sector_count</a> .

◆ **callbackSet**

```
fsp_err_t(* sdmmc_api_t::callbackSet) (sdmmc_ctrl_t *const p_api_ctrl,
void(*p_callback)(sdmmc_callback_args_t *), void const *const p_context, sdmmc_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SDHI\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">sdmmc_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* sdmmc_api_t::close) (sdmmc_ctrl_t *const p_ctrl)
```

Close open SD/MMC device.

**Implemented as**

- R\_SDHI\_Close()

**Parameters**

[in]	p_ctrl	Pointer to an open SD/MMC instance control block.
------	--------	---

◆ **sdmmc\_instance\_t**

```
struct sdmmc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">sdmmc_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">sdmmc_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">sdmmc_api_t</a> const *	p_api	Pointer to the API structure for

		this instance.
--	--	----------------

## Typedef Documentation

### ◆ sdmmc\_ctrl\_t

```
typedef void sdmmc_ctrl_t
```

SD/MMC control block. Allocate an instance specific control block to pass into the SD/MMC API calls.

#### Implemented as

- sdmmc\_instance\_ctrl\_t

## Enumeration Type Documentation

### ◆ sdmmc\_card\_type\_t

```
enum sdmmc_card_type_t
```

SD/MMC media uses SD protocol or MMC protocol.

#### Enumerator

SDMMC_CARD_TYPE_MMC	The media is an eMMC device.
SDMMC_CARD_TYPE_SD	The media is an SD card.
SDMMC_CARD_TYPE_SDIO	The media is an SDIO card.

### ◆ sdmmc\_bus\_width\_t

```
enum sdmmc_bus_width_t
```

SD/MMC data bus is 1, 4 or 8 bits wide.

#### Enumerator

SDMMC_BUS_WIDTH_1_BIT	Data bus is 1 bit wide.
SDMMC_BUS_WIDTH_4_BITS	Data bus is 4 bits wide.
SDMMC_BUS_WIDTH_8_BITS	Data bus is 8 bits wide.

◆ **sdmmc\_io\_transfer\_mode\_t**

enum <a href="#">sdmmc_io_transfer_mode_t</a>	
SDIO transfer mode, configurable in SDIO read/write extended commands.	
Enumerator	
SDMMC_IO_MODE_TRANSFER_BYTE	SDIO byte transfer mode.
SDMMC_IO_MODE_TRANSFER_BLOCK	SDIO block transfer mode.

◆ **sdmmc\_io\_address\_mode\_t**

enum <a href="#">sdmmc_io_address_mode_t</a>	
SDIO address mode, configurable in SDIO read/write extended commands.	
Enumerator	
SDMMC_IO_ADDRESS_MODE_FIXED	Write all data to the same address.
SDMMC_IO_ADDRESS_MODE_INCREMENT	Increment destination address after each write.

◆ **sdmmc\_io\_write\_mode\_t**

enum <a href="#">sdmmc_io_write_mode_t</a>	
Controls the RAW (read after write) flag of CMD52. Used to read back the status after writing a control register.	
Enumerator	
SDMMC_IO_WRITE_MODE_NO_READ	Write only (do not read back)
SDMMC_IO_WRITE_READ_AFTER_WRITE	Read back the register after write.

◆ **sdmmc\_event\_t**

enum <a href="#">sdmmc_event_t</a>	
Events that can trigger a callback function	
Enumerator	
SDMMC_EVENT_CARD_REMOVED	Card removed event.
SDMMC_EVENT_CARD_INSERTED	Card inserted event.
SDMMC_EVENT_RESPONSE	Response event.
SDMMC_EVENT_SDIO	IO event.
SDMMC_EVENT_TRANSFER_COMPLETE	Read or write complete.
SDMMC_EVENT_TRANSFER_ERROR	Read or write failed.
SDMMC_EVENT_ERASE_COMPLETE	Erase completed.
SDMMC_EVENT_ERASE_BUSY	Erase timeout, poll <a href="#">sdmmc_api_t::statusGet</a> .

◆ **sdmmc\_card\_detect\_t**

enum <a href="#">sdmmc_card_detect_t</a>	
Card detection configuration options.	
Enumerator	
SDMMC_CARD_DETECT_NONE	Card detection unused.
SDMMC_CARD_DETECT_CD	Card detection using the CD pin.

◆ **sdmmc\_write\_protect\_t**

enum <a href="#">sdmmc_write_protect_t</a>	
Write protection configuration options.	
Enumerator	
SDMMC_WRITE_PROTECT_NONE	Write protection unused.
SDMMC_WRITE_PROTECT_WP	Write protection using WP pin.

◆ **sdmmc\_r1\_state\_t**

enum <code>sdmmc_r1_state_t</code>	
Card state when receiving the prior command.	
Enumerator	
<code>SDMMC_R1_STATE_IDLE</code>	Idle State.
<code>SDMMC_R1_STATE_READY</code>	Ready State.
<code>SDMMC_R1_STATE_IDENT</code>	Identification State.
<code>SDMMC_R1_STATE_STBY</code>	Stand-by State.
<code>SDMMC_R1_STATE_TRAN</code>	Transfer State.
<code>SDMMC_R1_STATE_DATA</code>	Sending-data State.
<code>SDMMC_R1_STATE_RCV</code>	Receive-data State.
<code>SDMMC_R1_STATE_PRG</code>	Programming State.
<code>SDMMC_R1_STATE_DIS</code>	Disconnect State (between programming and stand-by)
<code>SDMMC_R1_STATE_IO</code>	This is an I/O card and memory states do not apply.

**4.3.32 SLCDC Interface**[Interfaces](#)**Detailed Description**

Interface for Segment LCD controllers.

**Data Structures**

struct [slcdc\\_cfg\\_t](#)

struct [slcdc\\_api\\_t](#)

struct [slcdc\\_instance\\_t](#)

## Typedefs

```
typedef void slcdc_ctrl_t
```

## Enumerations

```
enum slcdc_bias_method_t
```

```
enum slcdc_time_slice_t
```

```
enum slcdc_waveform_t
```

```
enum slcdc_drive_volt_gen_t
```

```
enum slcdc_display_area_control_blink_t
```

```
enum slcdc_display_area_t
```

```
enum slcdc_contrast_t
```

```
enum slcdc_display_on_off_t
```

```
enum slcdc_display_enable_disable_t
```

```
enum slcdc_display_clock_t
```

```
enum slcdc_clk_div_t
```

## Data Structure Documentation

### ◆ slcdc\_cfg\_t

struct slcdc_cfg_t		
SLCDC configuration block		
Data Fields		
<a href="#">slcdc_display_clock_t</a>	slcdc_clock	LCD clock source (LCDSCKSEL)
<a href="#">slcdc_clk_div_t</a>	slcdc_clock_setting	LCD clock setting (LCDC0)
<a href="#">slcdc_bias_method_t</a>	bias_method	LCD display bias method select (LBAS bit)
<a href="#">slcdc_time_slice_t</a>	time_slice	Time slice of LCD display select (LDTY bit)
<a href="#">slcdc_waveform_t</a>	waveform	LCD display waveform select (LWAVE bit)
<a href="#">slcdc_drive_volt_gen_t</a>	drive_volt_gen	LCD Drive Voltage Generator Select (MDSET bit)
<a href="#">slcdc_contrast_t</a>	contrast	LCD Boost Level (contrast setting)

◆ **slcdc\_api\_t**

struct slcdc\_api\_t

SLCDC functions implemented at the HAL layer will follow this API.

**Data Fields**fsp\_err\_t(\* [open](#) )(slcdc\_ctrl\_t \*const p\_ctrl, slcdc\_cfg\_t const \*const p\_cfg)fsp\_err\_t(\* [write](#) )(slcdc\_ctrl\_t \*const p\_ctrl, uint8\_t const start\_segment, uint8\_t const \*p\_data, uint8\_t const segment\_count)fsp\_err\_t(\* [modify](#) )(slcdc\_ctrl\_t \*const p\_ctrl, uint8\_t const segment, uint8\_t const data\_mask, uint8\_t const data)fsp\_err\_t(\* [start](#) )(slcdc\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* [stop](#) )(slcdc\_ctrl\_t \*const p\_ctrl)fsp\_err\_t(\* [setContrast](#) )(slcdc\_ctrl\_t \*const p\_ctrl, slcdc\_contrast\_t const contrast)fsp\_err\_t(\* [setDisplayArea](#) )(slcdc\_ctrl\_t \*const p\_ctrl, slcdc\_display\_area\_t const display\_area)fsp\_err\_t(\* [close](#) )(slcdc\_ctrl\_t \*const p\_ctrl)**Field Documentation**

◆ **open**

```
fsp_err_t(* slcdc_api_t::open) (slcdc_ctrl_t *const p_ctrl, slcdc_cfg_t const *const p_cfg)
```

Open SLCDC.

**Implemented as**

- R\_SLCDC\_Open()

**Parameters**

[in,out]	p_ctrl	Pointer to display interface control block. Must be declared by user.
[in]	p_cfg	Pointer to display configuration structure. All elements of this structure must be set by the user.

◆ **write**

```
fsp_err_t(* slcdc_api_t::write) (slcdc_ctrl_t *const p_ctrl, uint8_t const start_segment, uint8_t const *p_data, uint8_t const segment_count)
```

Write data to the SLCDC segment data array. Specifies the initial display data. Except when using 8-time slice mode, store values in the lower 4 bits when writing to the A-pattern area and in the upper 4 bits when writing to the B-pattern area.

**Implemented as**

- R\_SLCDC\_Write()

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	start_segment	Specify the start segment number to be written.
[in]	p_data	Pointer to the display data to be written to the specified segments.
[in]	segment_count	Number of segments to be written.

◆ **modify**

```
fsp_err_t(* slcdc_api_t::modify) (slcdc_ctrl_t *const p_ctrl, uint8_t const segment, uint8_t const data_mask, uint8_t const data)
```

Rewrite data in the SLCDC segment data array. Rewrites the LCD display data in 1-bit units. If a bit is not specified for rewriting, the value stored in the bit is held as it is.

**Implemented as**

- [R\\_SLCDC\\_Modify\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	segment	The segment to be written.
[in]	data_mask	Mask the data being displayed. Set 0 to the bit to be rewritten and set 1 to the other bits. Multiple bits can be rewritten.
[in]	data	Specify display data to rewrite to the specified segment.

◆ **start**

```
fsp_err_t(* slcdc_api_t::start) (slcdc_ctrl_t *const p_ctrl)
```

Enable display signal output. Displays the segment data on the LCD.

**Implemented as**

- [R\\_SLCDC\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

◆ **stop**

```
fsp_err_t(* slcdc_api_t::stop) (slcdc_ctrl_t *const p_ctrl)
```

Disable display signal output. Stops displaying data on the LCD.

**Implemented as**

- [R\\_SLCDC\\_Stop\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

◆ **setContrast**

```
fsp_err_t(* slcdc_api_t::setContrast) (slcdc_ctrl_t *const p_ctrl, slcdc_contrast_t const contrast)
```

Set the display contrast. This function can be used only when the internal voltage boosting method is used for drive voltage generation.

**Implemented as**

- [R\\_SLCDC\\_SetContrast\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

◆ **setDisplayArea**

```
fsp_err_t(* slcdc_api_t::setDisplayArea) (slcdc_ctrl_t *const p_ctrl, slcdc_display_area_t const display_area)
```

Set LCD display area. This function sets a specified display area, A-pattern or B-pattern. This function can be used to 'blink' the display between A-pattern and B-pattern area data.

When using blinking, the RTC is required to operate before this function is executed. To configure the RTC, follow the steps below. 1) Open RTC 2) Set Periodic IRQ 3) Start RTC counter 4) Enable IRQ, RTC\_EVENT\_PERIODIC\_IRQ Refer to the User's Manual for the detailed procedure.

**Implemented as**

- [R\\_SLCDC\\_SetDisplayArea\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
[in]	display_area	Display area to be used, A-pattern or B-pattern area.

◆ **close**

```
fsp_err_t(* slcdc_api_t::close) (slcdc_ctrl_t *const p_ctrl)
```

Close SLCDC.

**Implemented as**

- [R\\_SLCDC\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to display interface control block.
------	--------	---

◆ **slcdc\_instance\_t**

```
struct slcdc_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

<code>slcdc_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>slcdc_cfg_t const *</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>slcdc_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `slcdc_ctrl_t`

```
typedef void slcdc_ctrl_t
```

SLCDC control block. Allocate an instance specific control block to pass into the SLCDC API calls.

#### Implemented as

- `slcdc_instance_ctrl_t` SLCDC control block

## Enumeration Type Documentation

### ◆ `slcdc_bias_method_t`

```
enum slcdc_bias_method_t
```

LCD display bias method.

#### Enumerator

<code>SLCDC_BIAS_2</code>	1/2 bias method
<code>SLCDC_BIAS_3</code>	1/3 bias method
<code>SLCDC_BIAS_4</code>	1/4 bias method

◆ **slcdc\_time\_slice\_t**

enum <a href="#">slcdc_time_slice_t</a>	
Time slice of LCD display.	
Enumerator	
SLCDC_STATIC	Static.
SLCDC_SLICE_2	2-time slice
SLCDC_SLICE_3	3-time slice
SLCDC_SLICE_4	4-time slice
SLCDC_SLICE_8	8-time slice

◆ **slcdc\_waveform\_t**

enum <a href="#">slcdc_waveform_t</a>	
LCD display waveform select.	
Enumerator	
SLCDC_WAVE_A	Waveform A.
SLCDC_WAVE_B	Waveform B.

◆ **slcdc\_drive\_volt\_gen\_t**

enum <a href="#">slcdc_drive_volt_gen_t</a>	
LCD Drive Voltage Generator Select.	
Enumerator	
SLCDC_VOLT_EXTERNAL	External resistance division method.
SLCDC_VOLT_INTERNAL	Internal voltage boosting method.
SLCDC_VOLT_CAPACITOR	Capacitor split method.

◆ **slcdc\_display\_area\_control\_blink\_t**

enum <code>slcdc_display_area_control_blink_t</code>	
Display Data Area Control	
Enumerator	
SLCDC_NOT_BLINKING	Display either A-pattern or B-pattern data.
SLCDC_BLINKING	Alternately display A-pattern and B-pattern data.

◆ **slcdc\_display\_area\_t**

enum <code>slcdc_display_area_t</code>	
Display Area data	
Enumerator	
SLCDC_DISP_A	Display A-pattern data.
SLCDC_DISP_B	Display B-pattern data.
SLCDC_DISP_BLINK	Blink between A- and B-pattern.

◆ **slcdc\_contrast\_t**

enum <code>slcdc_contrast_t</code>	
LCD Boost Level (contrast) settings	
Enumerator	
<code>SLCDC_CONTRAST_0</code>	Contrast level 0.
<code>SLCDC_CONTRAST_1</code>	Contrast level 1.
<code>SLCDC_CONTRAST_2</code>	Contrast level 2.
<code>SLCDC_CONTRAST_3</code>	Contrast level 3.
<code>SLCDC_CONTRAST_4</code>	Contrast level 4.
<code>SLCDC_CONTRAST_5</code>	Contrast level 5.
<code>SLCDC_CONTRAST_6</code>	Contrast level 6.
<code>SLCDC_CONTRAST_7</code>	Contrast level 7.
<code>SLCDC_CONTRAST_8</code>	Contrast level 8.
<code>SLCDC_CONTRAST_9</code>	Contrast level 9.
<code>SLCDC_CONTRAST_10</code>	Contrast level 10.
<code>SLCDC_CONTRAST_11</code>	Contrast level 11.
<code>SLCDC_CONTRAST_12</code>	Contrast level 12.
<code>SLCDC_CONTRAST_13</code>	Contrast level 13.
<code>SLCDC_CONTRAST_14</code>	Contrast level 14.
<code>SLCDC_CONTRAST_15</code>	Contrast level 15.

◆ **slcdc\_display\_on\_off\_t**

enum <code>slcdc_display_on_off_t</code>	
LCD Display Enable/Disable	
Enumerator	
SLCDC_DISP_OFF	Display off.
SLCDC_DISP_ON	Display on.

◆ **slcdc\_display\_enable\_disable\_t**

enum <code>slcdc_display_enable_disable_t</code>	
LCD Display output enable	
Enumerator	
SLCDC_DISP_DISABLE	Output ground level to segment/common pins.
SLCDC_DISP_ENABLE	Output enable.

◆ **slcdc\_display\_clock\_t**

enum <code>slcdc_display_clock_t</code>	
LCD Display clock selection	
Enumerator	
SLCDC_CLOCK_LOCO	Display clock source LOCO.
SLCDC_CLOCK_SOSC	Display clock source SOSC.
SLCDC_CLOCK_MOSC	Display clock source MOSC.
SLCDC_CLOCK_HOCO	Display clock source HOCO.

◆ **slcdc\_clk\_div\_t**

enum <code>slcdc_clk_div_t</code>	
LCD clock settings	
Enumerator	
SLCDC_CLK_DIVISOR_LOCO_4	LOCO Clock/4.

SLCDC_CLK_DIVISOR_LOCO_8	LOCO Clock/8.
SLCDC_CLK_DIVISOR_LOCO_16	LOCO Clock/16.
SLCDC_CLK_DIVISOR_LOCO_32	LOCO Clock/32.
SLCDC_CLK_DIVISOR_LOCO_64	LOCO Clock/64.
SLCDC_CLK_DIVISOR_LOCO_128	LOCO Clock/128.
SLCDC_CLK_DIVISOR_LOCO_256	LOCO Clock/256.
SLCDC_CLK_DIVISOR_LOCO_512	LOCO Clock/512.
SLCDC_CLK_DIVISOR_LOCO_1024	LOCO Clock/1024.
SLCDC_CLK_DIVISOR_HOCO_256	HOCO Clock/256.
SLCDC_CLK_DIVISOR_HOCO_512	HOCO Clock/512.
SLCDC_CLK_DIVISOR_HOCO_1024	HOCO Clock/1024.
SLCDC_CLK_DIVISOR_HOCO_2048	HOCO Clock/2048.
SLCDC_CLK_DIVISOR_HOCO_4096	HOCO Clock/4096.
SLCDC_CLK_DIVISOR_HOCO_8192	HOCO Clock/8192.
SLCDC_CLK_DIVISOR_HOCO_16384	HOCO Clock/16384.
SLCDC_CLK_DIVISOR_HOCO_32768	HOCO Clock/32768.
SLCDC_CLK_DIVISOR_HOCO_65536	HOCO Clock/65536.
SLCDC_CLK_DIVISOR_HOCO_131072	HOCO Clock/131072.
SLCDC_CLK_DIVISOR_HOCO_262144	HOCO Clock/262144.
SLCDC_CLK_DIVISOR_HOCO_524288	HOCO Clock/524288.

### 4.3.33 SPI Interface

#### [Interfaces](#)

## Detailed Description

Interface for SPI communications.

## Summary

Provides a common interface for communication using the SPI Protocol.

Implemented by:

- [Serial Peripheral Interface \(r\\_spi\)](#)
- [Serial Communications Interface \(SCI\) SPI \(r\\_sci\\_spi\)](#)

## Data Structures

struct [spi\\_callback\\_args\\_t](#)

struct [spi\\_write\\_read\\_guard\\_args\\_t](#)

struct [spi\\_cfg\\_t](#)

struct [spi\\_api\\_t](#)

struct [spi\\_instance\\_t](#)

## Typedefs

typedef void [spi\\_ctrl\\_t](#)

## Enumerations

enum [spi\\_bit\\_width\\_t](#)

enum [spi\\_mode\\_t](#)

enum [spi\\_clk\\_phase\\_t](#)

enum [spi\\_clk\\_polarity\\_t](#)

enum [spi\\_mode\\_fault\\_t](#)

enum [spi\\_bit\\_order\\_t](#)

enum [spi\\_event\\_t](#)

## Data Structure Documentation

### ◆ [spi\\_callback\\_args\\_t](#)

struct [spi\\_callback\\_args\\_t](#)

Common callback parameter definition

Data Fields		
uint32_t	channel	Device channel number.
<a href="#">spi_event_t</a>	event	Event code.
void const *	p_context	Context provided to user during callback.

#### ◆ [spi\\_write\\_read\\_guard\\_args\\_t](#)

struct <a href="#">spi_write_read_guard_args_t</a>
Non-secure arguments for write-read guard function

#### ◆ [spi\\_cfg\\_t](#)

struct <a href="#">spi_cfg_t</a>	
SPI interface configuration	
<b>Data Fields</b>	
uint8_t	<a href="#">channel</a>
	Channel number to be used.
IRQn_Type	<a href="#">rx_irq</a>
	Receive Buffer Full IRQ number.
IRQn_Type	<a href="#">tx_irq</a>
	Transmit Buffer Empty IRQ number.
IRQn_Type	<a href="#">tei_irq</a>
	Transfer Complete IRQ number.
IRQn_Type	<a href="#">eri_irq</a>
	Error IRQ number.
uint8_t	<a href="#">rx_ipl</a>
	Receive Interrupt priority.

uint8_t	<a href="#">txi_ipl</a>
	Transmit Interrupt priority.
uint8_t	<a href="#">tei_ipl</a>
	Transfer Complete Interrupt priority.
uint8_t	<a href="#">eri_ipl</a>
	Error Interrupt priority.
spi_mode_t	<a href="#">operating_mode</a>
	Select master or slave operating mode.
spi_clk_phase_t	<a href="#">clk_phase</a>
	Data sampling on odd or even clock edge.
spi_clk_polarity_t	<a href="#">clk_polarity</a>
	Clock level when idle.
spi_mode_fault_t	<a href="#">mode_fault</a>
	Mode fault error (master/slave conflict) flag.
spi_bit_order_t	<a href="#">bit_order</a>
	Select to transmit MSB/LSB first.
<a href="#">transfer_instance_t</a> const *	<a href="#">p_transfer_tx</a>
	To use SPI DTC/DMA write transfer, link a DTC/DMA instance here. Set to NULL if unused.

<code>transfer_instance_t</code> const *	<code>p_transfer_rx</code>
	To use SPI DTC/DMA read transfer, link a DTC/DMA instance here. Set to NULL if unused.
<code>void</code> (* <code>p_callback</code> )( <code>spi_callback_args_t</code> * <code>p_args</code> )	
	Pointer to user callback function.
<code>void</code> const *	<code>p_context</code>
	User defined context passed to callback function.
<code>void</code> const *	<code>p_extend</code>
	Extended SPI hardware dependent configuration.

◆ **spi\_api\_t**

struct <code>spi_api_t</code>	
Shared Interface definition for SPI	
<b>Data Fields</b>	
<code>fsp_err_t</code> (* <code>open</code> )( <code>spi_ctrl_t</code> * <code>p_ctrl</code> , <code>spi_cfg_t</code> const * <code>const p_cfg</code> )	
<code>fsp_err_t</code> (* <code>read</code> )( <code>spi_ctrl_t</code> * <code>const p_ctrl</code> , void * <code>p_dest</code> , <code>uint32_t</code> const <code>length</code> , <code>spi_bit_width_t</code> const <code>bit_width</code> )	
<code>fsp_err_t</code> (* <code>write</code> )( <code>spi_ctrl_t</code> * <code>const p_ctrl</code> , void const * <code>p_src</code> , <code>uint32_t</code> const <code>length</code> , <code>spi_bit_width_t</code> const <code>bit_width</code> )	
<code>fsp_err_t</code> (* <code>writeRead</code> )( <code>spi_ctrl_t</code> * <code>const p_ctrl</code> , void const * <code>p_src</code> , void * <code>p_dest</code> , <code>uint32_t</code> const <code>length</code> , <code>spi_bit_width_t</code> const <code>bit_width</code> )	
<code>fsp_err_t</code> (* <code>callbackSet</code> )( <code>spi_ctrl_t</code> * <code>const p_api_ctrl</code> , void(* <code>p_callback</code> )( <code>spi_callback_args_t</code> *), void const * <code>const p_context</code> , <code>spi_callback_args_t</code> * <code>const p_callback_memory</code> )	

`fsp_err_t(* close )(spi_ctrl_t *const p_ctrl)`

## Field Documentation

### ◆ open

`fsp_err_t(* spi_api_t::open) (spi_ctrl_t *p_ctrl, spi_cfg_t const *const p_cfg)`

Initialize a channel for SPI communication mode.

#### Implemented as

- `R_SPI_Open()`
- `R_SCI_SPI_Open()`

#### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to user-provided storage for the control block.
[in]	<code>p_cfg</code>	Pointer to SPI configuration structure.

### ◆ read

`fsp_err_t(* spi_api_t::read) (spi_ctrl_t *const p_ctrl, void *p_dest, uint32_t const length, spi_bit_width_t const bit_width)`

Receive data from a SPI device.

#### Implemented as

- `R_SPI_Read()`
- `R_SCI_SPI_Read()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to the control block for the channel.
[in]	<code>length</code>	Number of units of data to be transferred (unit size specified by the <code>bit_width</code> ).
[in]	<code>bit_width</code>	Data bit width to be transferred.
[out]	<code>p_dest</code>	Pointer to destination buffer into which data will be copied that is received from a SPI device. It is the responsibility of the caller to ensure that adequate space is available to hold the requested data count.

## ◆ write

```
fsp_err_t(* spi_api_t::write) (spi_ctrl_t *const p_ctrl, void const *p_src, uint32_t const length,
spi_bit_width_t const bit_width)
```

Transmit data to a SPI device.

**Implemented as**

- R\_SPI\_Write()
- R\_SCI\_SPI\_Write()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
[in]	p_src	Pointer to a source data buffer from which data will be transmitted to a SPI device. The argument must not be NULL.
[in]	length	Number of units of data to be transferred (unit size specified by the bit_width).
[in]	bit_width	Data bit width to be transferred.

◆ **writeRead**

```
fsp_err_t(* spi_api_t::writeRead) (spi_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t
const length, spi_bit_width_t const bit_width)
```

Simultaneously transmit data to a SPI device while receiving data from a SPI device (full duplex).

**Implemented as**

- R\_SPI\_WriteRead()
- R\_SCI\_SPI\_WriteRead()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
[in]	p_src	Pointer to a source data buffer from which data will be transmitted to a SPI device. The argument must not be NULL.
[out]	p_dest	Pointer to destination buffer into which data will be copied that is received from a SPI device. It is the responsibility of the caller to ensure that adequate space is available to hold the requested data count. The argument must not be NULL.
[in]	length	Number of units of data to be transferred (unit size specified by the bit_width).
[in]	bit_width	Data bit width to be transferred.

◆ **callbackSet**

```
fsp_err_t(* spi_api_t::callbackSet) (spi_ctrl_t *const p_api_ctrl, void(*p_callback)(spi_callback_args_t *), void const *const p_context, spi_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SCI\_SPI\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the SPI control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* spi_api_t::close) (spi_ctrl_t *const p_ctrl)
```

Remove power to the SPI channel designated by the handle and disable the associated interrupts.

**Implemented as**

- R\_SPI\_Close()
- R\_SCI\_SPI\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the control block for the channel.
------	--------	---

◆ **spi\_instance\_t**

```
struct spi_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

spi_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
spi_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
spi_api_t const *	p_api	Pointer to the API structure for

		this instance.
--	--	----------------

## Typedef Documentation

### ◆ spi\_ctrl\_t

```
typedef void spi_ctrl_t
```

SPI control block. Allocate an instance specific control block to pass into the SPI API calls.

#### Implemented as

- sci\_spi\_instance\_ctrl\_t
- spi\_instance\_ctrl\_t

## Enumeration Type Documentation

### ◆ spi\_bit\_width\_t

```
enum spi_bit_width_t
```

Data bit width

Enumerator

SPI_BIT_WIDTH_8_BITS	Data bit width is 8 bits byte.
SPI_BIT_WIDTH_9_BITS	Data bit width is 9 bits word.
SPI_BIT_WIDTH_10_BITS	Data bit width is 10 bits word.
SPI_BIT_WIDTH_11_BITS	Data bit width is 11 bits word.
SPI_BIT_WIDTH_12_BITS	Data bit width is 12 bits word.
SPI_BIT_WIDTH_13_BITS	Data bit width is 13 bits word.
SPI_BIT_WIDTH_14_BITS	Data bit width is 14 bits word.
SPI_BIT_WIDTH_15_BITS	Data bit width is 15 bits word.
SPI_BIT_WIDTH_16_BITS	Data bit width is 16 bits word.
SPI_BIT_WIDTH_20_BITS	Data bit width is 20 bits long word.
SPI_BIT_WIDTH_24_BITS	Data bit width is 24 bits long word.
SPI_BIT_WIDTH_32_BITS	Data bit width is 32 bits long word.

## ◆ spi\_mode\_t

enum spi_mode_t	
Master or slave operating mode	
Enumerator	
SPI_MODE_MASTER	Channel operates as SPI master.
SPI_MODE_SLAVE	Channel operates as SPI slave.

## ◆ spi\_clk\_phase\_t

enum spi_clk_phase_t	
Clock phase	
Enumerator	
SPI_CLK_PHASE_EDGE_ODD	0: Data sampling on odd edge, data variation on even edge
SPI_CLK_PHASE_EDGE_EVEN	1: Data variation on odd edge, data sampling on even edge

## ◆ spi\_clk\_polarity\_t

enum spi_clk_polarity_t	
Clock polarity	
Enumerator	
SPI_CLK_POLARITY_LOW	0: Clock polarity is low when idle
SPI_CLK_POLARITY_HIGH	1: Clock polarity is high when idle

◆ **spi\_mode\_fault\_t**

enum <a href="#">spi_mode_fault_t</a>	
Mode fault error flag. This error occurs when the device is setup as a master, but the SS/SA line does not seem to be controlled by the master. This usually happens when the connecting device is also acting as master. A similar situation can also happen when configured as a slave.	
Enumerator	
SPI_MODE_FAULT_ERROR_ENABLE	Mode fault error flag on.
SPI_MODE_FAULT_ERROR_DISABLE	Mode fault error flag off.

◆ **spi\_bit\_order\_t**

enum <a href="#">spi_bit_order_t</a>	
Bit order	
Enumerator	
SPI_BIT_ORDER_MSB_FIRST	Send MSB first in transmission.
SPI_BIT_ORDER_LSB_FIRST	Send LSB first in transmission.

◆ **spi\_event\_t**

enum <a href="#">spi_event_t</a>	
SPI events	
Enumerator	
SPI_EVENT_TRANSFER_COMPLETE	The data transfer was completed.
SPI_EVENT_TRANSFER_ABORTED	The data transfer was aborted.
SPI_EVENT_ERR_MODE_FAULT	Mode fault error.
SPI_EVENT_ERR_READ_OVERFLOW	Read overflow error.
SPI_EVENT_ERR_PARITY	Parity error.
SPI_EVENT_ERR_OVERRUN	Overrun error.
SPI_EVENT_ERR_FRAMING	Framing error.
SPI_EVENT_ERR_MODE_UNDERRUN	Underrun error.

## 4.3.34 SPI Flash Interface

### Interfaces

#### Detailed Description

---

Interface for accessing external SPI flash devices.

## Summary

The SPI flash API provides an interface that configures, writes, and erases sectors in SPI flash devices.

Implemented by:

- Octa Serial Peripheral Interface Flash (r\_ospfi)
- Quad Serial Peripheral Interface Flash (r\_qsfi)

#### Data Structures

---

struct spi\_flash\_erase\_command\_t

struct spi\_flash\_direct\_transfer\_t

struct spi\_flash\_cfg\_t

struct spi\_flash\_status\_t

struct spi\_flash\_api\_t

struct spi\_flash\_instance\_t

#### Typedefs

---

typedef void spi\_flash\_ctrl\_t

#### Enumerations

---

enum spi\_flash\_read\_mode\_t

enum spi\_flash\_protocol\_t

enum spi\_flash\_address\_bytes\_t

enum spi\_flash\_data\_lines\_t

enum spi\_flash\_dummy\_clocks\_t

enum `spi_flash_direct_transfer_dir_t`**Data Structure Documentation**◆ **spi\_flash\_erase\_command\_t**

struct spi_flash_erase_command_t		
Structure to define an erase command and associated erase size.		
Data Fields		
uint16_t	command	Erase command.
uint32_t	size	Size of erase for associated command, set to SPI_FLASH_ERASE_SIZE_CHIP_ERASE for chip erase.

◆ **spi\_flash\_direct\_transfer\_t**

struct spi_flash_direct_transfer_t		
Structure to define a direct transfer.		
Data Fields		
uint32_t	address	Starting address.
uint32_t	data	Data.
uint16_t	command	Transfer command.
uint8_t	dummy_cycles	Number of dummy cycles.
uint8_t	command_length	Command length.
uint8_t	address_length	Address length.
uint8_t	data_length	Data length.

◆ **spi\_flash\_cfg\_t**

struct spi_flash_cfg_t		
User configuration structure used by the open function		
Data Fields		
<a href="#">spi_flash_protocol_t</a>	spi_protocol	Initial SPI protocol. SPI protocol can be changed in <a href="#">spi_flash_api_t::spiProtocolSet</a> .
<a href="#">spi_flash_read_mode_t</a>	read_mode	Read mode.
<a href="#">spi_flash_address_bytes_t</a>	address_bytes	Number of bytes used to represent the address.
<a href="#">spi_flash_dummy_clocks_t</a>	dummy_clocks	Number of dummy clocks to use for fast read operations.
<a href="#">spi_flash_data_lines_t</a>	page_program_address_lines	Number of lines used to send

		address for page program command. This should either be 1 or match the number of lines used in the selected read mode.
uint8_t	write_status_bit	Which bit determines write status.
uint8_t	write_enable_bit	Which bit determines write status.
uint32_t	page_size_bytes	Page size in bytes (maximum number of bytes for page program)
uint8_t	page_program_command	Page program command.
uint8_t	write_enable_command	Command to enable write or erase, typically 0x06.
uint8_t	status_command	Command to read the write status.
uint8_t	read_command	Read command - OSPI SPI mode only.
uint8_t	xip_enter_command	Command to enter XIP mode.
uint8_t	xip_exit_command	Command to exit XIP mode.
uint8_t	erase_command_list_length	Length of erase command list.
<a href="#">spi_flash_erase_command_t</a> const *	p_erase_command_list	List of all erase commands and associated sizes.
void const *	p_extend	Pointer to implementation specific extended configurations.

#### ◆ spi\_flash\_status\_t

struct spi_flash_status_t		
Status.		
Data Fields		
bool	write_in_progress	Whether or not a write is in progress. This is determined by reading the <a href="#">spi_flash_cfg_t::write_status_bit</a> from the <a href="#">spi_flash_cfg_t::status_command</a> .

#### ◆ spi\_flash\_api\_t

struct spi_flash_api_t		
SPI flash implementations follow this API.		

Data Fields	
fsp_err_t(*)	open )(spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
fsp_err_t(*)	directWrite )(spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
fsp_err_t(*)	directRead )(spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t(*)	directTransfer )(spi_flash_ctrl_t *p_ctrl, spi_flash_direct_transfer_t *const p_transfer, spi_flash_direct_transfer_dir_t direction)
fsp_err_t(*)	spiProtocolSet )(spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
fsp_err_t(*)	write )(spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
fsp_err_t(*)	erase )(spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
fsp_err_t(*)	statusGet )(spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
fsp_err_t(*)	xipEnter )(spi_flash_ctrl_t *p_ctrl)
fsp_err_t(*)	xipExit )(spi_flash_ctrl_t *p_ctrl)
fsp_err_t(*)	bankSet )(spi_flash_ctrl_t *p_ctrl, uint32_t bank)
fsp_err_t(*)	close )(spi_flash_ctrl_t *p_ctrl)
Field Documentation	

◆ **open**

```
fsp_err_t(* spi_flash_api_t::open) (spi_flash_ctrl_t *p_ctrl, spi_flash_cfg_t const *const p_cfg)
```

Open the SPI flash driver module.

**Implemented as**

- R\_OSPI\_Open()
- R\_QSPI\_Open()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_cfg	Pointer to a configuration structure

◆ **directWrite**

```
fsp_err_t(* spi_flash_api_t::directWrite) (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint32_t const bytes, bool const read_after_write)
```

Write raw data to the SPI flash.

**Implemented as**

- R\_OSPI\_DirectWrite()
- R\_QSPI\_DirectWrite()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_src	Pointer to raw data to write, must include any required command/address
[in]	bytes	Number of bytes to write
[in]	read_after_write	If true, the slave select remains asserted and the peripheral does not return to direct communications mode. If false, the slave select is deasserted and memory mapped access is possible after this function returns if the device is not busy.

### ◆ directRead

```
fsp_err_t(* spi_flash_api_t::directRead) (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

Read raw data from the SPI flash. Must follow a call to `spi_flash_api_t::directWrite`.

#### Implemented as

- `R_OSPI_DirectRead()`
- `R_QSPI_DirectRead()`

#### Parameters

[in]	p_ctrl	Pointer to a driver handle
[out]	p_dest	Pointer to read raw data into
[in]	bytes	Number of bytes to read

### ◆ directTransfer

```
fsp_err_t(* spi_flash_api_t::directTransfer) (spi_flash_ctrl_t *p_ctrl, spi_flash_direct_transfer_t *const p_transfer, spi_flash_direct_transfer_dir_t direction)
```

Direct Read/Write raw data to the SPI flash.

#### Implemented as

- `R_OSPI_DirectTransfer()`

#### Parameters

[in]	p_ctrl	Pointer to a driver handle
[in]	p_data	Pointer to command, address and data values and lengths
[in]	direction	Direct Read/Write

### ◆ spiProtocolSet

```
fsp_err_t(* spi_flash_api_t::spiProtocolSet) (spi_flash_ctrl_t *p_ctrl, spi_flash_protocol_t spi_protocol)
```

Change the SPI protocol in the driver. The application must change the SPI protocol on the device.

#### Implemented as

- `R_OSPI_SpiProtocolSet()`
- `R_QSPI_SpiProtocolSet()`

#### Parameters

[in]	p_ctrl	Pointer to a driver handle
[in]	spi_protocol	Desired SPI protocol

## ◆ write

```
fsp_err_t(* spi_flash_api_t::write) (spi_flash_ctrl_t *p_ctrl, uint8_t const *const p_src, uint8_t *const p_dest, uint32_t byte_count)
```

Program a page of data to the flash.

**Implemented as**

- R\_OSPI\_Write()
- R\_QSPI\_Write()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_src	The memory address of the data to write to the flash device
[in]	p_dest	The location in the flash device address space to write the data to
[in]	byte_count	The number of bytes to write

## ◆ erase

```
fsp_err_t(* spi_flash_api_t::erase) (spi_flash_ctrl_t *p_ctrl, uint8_t *const p_device_address, uint32_t byte_count)
```

Erase a certain number of bytes of the flash.

**Implemented as**

- R\_OSPI\_Erase()
- R\_QSPI\_Erase()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	p_device_address	The location in the flash device address space to start the erase from
[in]	byte_count	The number of bytes to erase. Set to SPI_FLASH_ERASE_SIZE_CHIP_ERASE to erase entire chip.

◆ **statusGet**

```
fsp_err_t(* spi_flash_api_t::statusGet) (spi_flash_ctrl_t *p_ctrl, spi_flash_status_t *const p_status)
```

Get the write or erase status of the flash.

**Implemented as**

- R\_OSPI\_StatusGet()
- R\_QSPI\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[out]	p_status	Current status of the SPI flash device stored here.

◆ **xipEnter**

```
fsp_err_t(* spi_flash_api_t::xipEnter) (spi_flash_ctrl_t *p_ctrl)
```

Enter XIP mode.

**Implemented as**

- R\_OSPI\_XipEnter()
- R\_QSPI\_XipEnter()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

◆ **xipExit**

```
fsp_err_t(* spi_flash_api_t::xipExit) (spi_flash_ctrl_t *p_ctrl)
```

Exit XIP mode.

**Implemented as**

- R\_OSPI\_XipExit()
- R\_QSPI\_XipExit()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

◆ **bankSet**

```
fsp_err_t(* spi_flash_api_t::bankSet) (spi_flash_ctrl_t *p_ctrl, uint32_t bank)
```

Select the bank to access. See implementation for details.

**Implemented as**

- R\_OSPI\_BankSet()
- R\_QSPI\_BankSet()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
[in]	bank	The bank number

◆ **close**

```
fsp_err_t(* spi_flash_api_t::close) (spi_flash_ctrl_t *p_ctrl)
```

Close the SPI flash driver module.

**Implemented as**

- R\_OSPI\_Close()
- R\_QSPI\_Close()

**Parameters**

[in]	p_ctrl	Pointer to a driver handle
------	--------	----------------------------

◆ **spi\_flash\_instance\_t**

```
struct spi_flash_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

spi_flash_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
spi_flash_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
spi_flash_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **spi\_flash\_ctrl\_t**typedef void [spi\\_flash\\_ctrl\\_t](#)

SPI flash control block. Allocate an instance specific control block to pass into the SPI flash API calls.

**Implemented as**

- [qspi\\_instance\\_ctrl\\_t](#)
- [ospi\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **spi\_flash\_read\_mode\_t**enum [spi\\_flash\\_read\\_mode\\_t](#)

Read mode.

## Enumerator

<code>SPI_FLASH_READ_MODE_STANDARD</code>	Standard Read Mode (no dummy cycles)
<code>SPI_FLASH_READ_MODE_FAST_READ</code>	Fast Read Mode (dummy cycles between address and data)
<code>SPI_FLASH_READ_MODE_FAST_READ_DUAL_OUT PUT</code>	Fast Read Dual Output Mode (data on 2 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_DUAL_IO</code>	Fast Read Dual I/O Mode (address and data on 2 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_QUAD_OUT PUT</code>	Fast Read Quad Output Mode (data on 4 lines)
<code>SPI_FLASH_READ_MODE_FAST_READ_QUAD_IO</code>	Fast Read Quad I/O Mode (address and data on 4 lines)

◆ **spi\_flash\_protocol\_t**

enum <code>spi_flash_protocol_t</code>	
SPI protocol.	
Enumerator	
<code>SPI_FLASH_PROTOCOL_EXTENDED_SPI</code>	Extended SPI mode (commands on 1 line)
<code>SPI_FLASH_PROTOCOL_QPI</code>	QPI mode (commands on 4 lines). Note that the application must ensure the device is in QPI mode.
<code>SPI_FLASH_PROTOCOL_SOPI</code>	SOPI mode (command and data on 8 lines). Note that the application must ensure the device is in SOPI mode.
<code>SPI_FLASH_PROTOCOL_DOPI</code>	DOPI mode (command and data on 8 lines, dual data rate). Note that the application must ensure the device is in DOPI mode.

◆ **spi\_flash\_address\_bytes\_t**

enum <code>spi_flash_address_bytes_t</code>	
Number of bytes in the address.	
Enumerator	
<code>SPI_FLASH_ADDRESS_BYTES_3</code>	3 address bytes
<code>SPI_FLASH_ADDRESS_BYTES_4</code>	4 address bytes with standard commands. If this option is selected, the application must issue the EN4B command using <code>spi_flash_api_t::directWrite()</code> if required by the device.
<code>SPI_FLASH_ADDRESS_BYTES_4_4BYTE_READ_CODE</code>	4 address bytes using standard 4-byte command set.

◆ **spi\_flash\_data\_lines\_t**

enum <code>spi_flash_data_lines_t</code>	
Number of data lines used.	
Enumerator	
<code>SPI_FLASH_DATA_LINES_1</code>	1 data line
<code>SPI_FLASH_DATA_LINES_2</code>	2 data lines
<code>SPI_FLASH_DATA_LINES_4</code>	4 data lines

## ◆ spi\_flash\_dummy\_clocks\_t

enum spi_flash_dummy_clocks_t	
Number of dummy cycles for fast read operations.	
Enumerator	
SPI_FLASH_DUMMY_CLOCKS_DEFAULT	Default is 6 clocks for Fast Read Quad I/O, 4 clocks for Fast Read Dual I/O, and 8 clocks for other fast read instructions including Fast Read Quad Output, Fast Read Dual Output, and Fast Read.
SPI_FLASH_DUMMY_CLOCKS_3	3 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_4	4 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_5	5 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_6	6 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_7	7 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_8	8 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_9	9 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_10	10 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_11	11 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_12	12 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_13	13 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_14	14 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_15	15 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_16	16 dummy clocks
SPI_FLASH_DUMMY_CLOCKS_17	17 dummy clocks

### ◆ spi\_flash\_direct\_transfer\_dir\_t

```
enum spi_flash_direct_transfer_dir_t
```

```
Direct Read and Write direction
```

## 4.3.35 Three-Phase Interface

### Interfaces

#### Detailed Description

Interface for three-phase timer functions.

## Summary

The Three-Phase interface provides functionality for synchronous start/stop/reset control of three timer channels for use in 3-phase motor control applications.

Implemented by:

- General PWM Timer Three-Phase Motor Control Driver (`r_gpt_three_phase`)

#### Data Structures

```
struct three_phase_duty_cycle_t
```

```
struct three_phase_cfg_t
```

```
struct three_phase_api_t
```

```
struct three_phase_instance_t
```

#### Typedefs

```
typedef void three_phase_ctrl_t
```

#### Enumerations

```
enum three_phase_channel_t
```

```
enum three_phase_buffer_mode_t
```

#### Data Structure Documentation

### ◆ three\_phase\_duty\_cycle\_t

```
struct three_phase_duty_cycle_t
```

Struct for passing duty cycle values to <a href="#">three_phase_api_t::dutyCycleSet</a>		
Data Fields		
uint32_t	duty[3]	Duty cycle. Note: When the GPT instances are configured in <code>TIMER_MODE_TRIANGLE_WAVE_AS_YMMETRIC_PWM_MODE3</code> , this value sets the duty cycle count that is transferred to GTCCRA/B at the trough.
uint32_t	duty_buffer[3]	Double-buffer for duty cycle values. Note: When the GPT instances are configured in <code>TIMER_MODE_TRIANGLE_WAVE_AS_YMMETRIC_PWM_MODE3</code> , this value sets the duty cycle count that is transferred to GTCCRA/B at the crest.

#### ◆ [three\\_phase\\_cfg\\_t](#)

struct <a href="#">three_phase_cfg_t</a>		
User configuration structure, used in <code>open</code> function		
Data Fields		
<a href="#">three_phase_buffer_mode_t</a>	buffer_mode	Single or double-buffer mode.
<a href="#">timer_instance_t</a> const *	p_timer_instance[3]	Pointer to the timer instance structs.
<a href="#">three_phase_channel_t</a>	callback_ch	Channel to enable callback when using <a href="#">three_phase_api_t::callbackSet</a> .
uint32_t	channel_mask	Bitmask of timer channels used by this module.
void const *	p_context	Placeholder for user data. Passed to the user callback in <a href="#">timer_callback_args_t</a> .
void const *	p_extend	Extension parameter for hardware specific settings.

#### ◆ [three\\_phase\\_api\\_t](#)

struct <a href="#">three_phase_api_t</a>	
Three-Phase API structure.	
Data Fields	
<a href="#">fsp_err_t</a> (* <code>open</code> )( <a href="#">three_phase_ctrl_t</a> *const p_ctrl, <a href="#">three_phase_cfg_t</a> const *const p_cfg)	

<code>fsp_err_t(*</code>	<code>start )(three_phase_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>stop )(three_phase_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>reset )(three_phase_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>dutyCycleSet )(three_phase_ctrl_t *const p_ctrl, three_phase_duty_cycle_t *const p_duty_cycle)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(three_phase_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(three_phase_ctrl_t *const p_ctrl)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* three_phase_api_t::open) (three_phase_ctrl_t *const p_ctrl, three_phase_cfg_t const *const p_cfg)`

Initial configuration.

### Implemented as

- `R_GPT_THREE_PHASE_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control block. Must be declared by user. Elements set here.
[in]	<code>p_cfg</code>	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **start**

```
fsp_err_t(* three_phase_api_t::start) (three_phase_ctrl_t *const p_ctrl)
```

Start all three timers synchronously.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	---

◆ **stop**

```
fsp_err_t(* three_phase_api_t::stop) (three_phase_ctrl_t *const p_ctrl)
```

Stop all three timers synchronously.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Stop\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	---

◆ **reset**

```
fsp_err_t(* three_phase_api_t::reset) (three_phase_ctrl_t *const p_ctrl)
```

Reset all three timers synchronously.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	---

◆ **dutyCycleSet**

```
fsp_err_t(* three_phase_api_t::dutyCycleSet) (three_phase_ctrl_t *const p_ctrl,
three_phase_duty_cycle_t *const p_duty_cycle)
```

Sets the duty cycle match values. If the timer is counting, the updated duty cycle is reflected after the next timer expiration.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_DutyCycleSet\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
[in]	p_duty_cycle	Duty cycle values for all three timer channels.

◆ **callbackSet**

```
fsp_err_t(* three_phase_api_t::callbackSet) (three_phase_ctrl_t *const p_api_ctrl,
void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call.
[in]	p_callback	Callback function to register with GPT U-channel
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* three_phase_api_t::close) (three_phase_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

**Implemented as**

- [R\\_GPT\\_THREE\\_PHASE\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">three_phase_api_t::open</a> call for this timer.
------	--------	---

◆ **three\_phase\_instance\_t**

```
struct three_phase_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">three_phase_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">three_phase_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">three_phase_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **three\_phase\_ctrl\_t**

```
typedef void three_phase_ctrl_t
```

Three-Phase control block. Allocate an instance specific control block to pass into the timer API calls.

**Implemented as**

- [gpt\\_three\\_phase\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **three\_phase\_channel\_t**

enum <code>three_phase_channel_t</code>	
Timer channel indices	
Enumerator	
<code>THREE_PHASE_CHANNEL_U</code>	U-channel index.
<code>THREE_PHASE_CHANNEL_V</code>	V-channel index.
<code>THREE_PHASE_CHANNEL_W</code>	W-channel index.

◆ **three\_phase\_buffer\_mode\_t**

enum <code>three_phase_buffer_mode_t</code>	
Buffering mode	
Enumerator	
<code>THREE_PHASE_BUFFER_MODE_SINGLE</code>	Single-buffer mode.
<code>THREE_PHASE_BUFFER_MODE_DOUBLE</code>	Double-buffer mode.

## 4.3.36 Timer Interface

### Interfaces

#### Detailed Description

Interface for timer functions.

## Summary

The general timer interface provides standard timer functionality including periodic mode, one-shot mode, PWM output, and free-running timer mode. After each timer cycle (overflow or underflow), an interrupt can be triggered.

If an instance supports output compare mode, it is provided in the extension configuration `timer_on_<instance>_cfg_t` defined in `r_<instance>.h`.

Implemented by:

- [General PWM Timer \(r\\_gpt\)](#)
- [Asynchronous General Purpose Timer \(r\\_agt\)](#)

## Data Structures

struct [timer\\_callback\\_args\\_t](#)

struct [timer\\_info\\_t](#)

struct [timer\\_status\\_t](#)

struct [timer\\_cfg\\_t](#)

struct [timer\\_api\\_t](#)

struct [timer\\_instance\\_t](#)

## Typedefs

typedef void [timer\\_ctrl\\_t](#)

## Enumerations

enum [timer\\_event\\_t](#)

enum [timer\\_variant\\_t](#)

enum [timer\\_state\\_t](#)

enum [timer\\_mode\\_t](#)

enum [timer\\_direction\\_t](#)

enum [timer\\_source\\_div\\_t](#)

## Data Structure Documentation

### ◆ [timer\\_callback\\_args\\_t](#)

struct <a href="#">timer_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	<a href="#">p_context</a>	Placeholder for user data. Set in <a href="#">timer_api_t::open</a> function in <a href="#">timer_cfg_t</a> .
<a href="#">timer_event_t</a>	<a href="#">event</a>	The event can be used to identify what caused the callback.
uint32_t	<a href="#">capture</a>	Most recent capture, only valid if event is <a href="#">TIMER_EVENT_CAPTURE_A</a> or <a href="#">TIMER_EVENT_CAPTURE_B</a> .

◆ **timer\_info\_t**

struct timer_info_t		
Timer information structure to store various information for a timer resource		
Data Fields		
<a href="#">timer_direction_t</a>	count_direction	Clock counting direction of the timer.
uint32_t	clock_frequency	Clock frequency of the timer counter.
uint32_t	period_counts	Period in raw timer counts.  <i>Note</i> <i>For triangle wave PWM modes, the full period is double this value.</i>

◆ **timer\_status\_t**

struct timer_status_t		
Current timer status.		
Data Fields		
uint32_t	counter	Current counter value.
<a href="#">timer_state_t</a>	state	Current timer state (running or stopped)

◆ **timer\_cfg\_t**

struct timer_cfg_t		
User configuration structure, used in open function		
<b>Data Fields</b>		
<a href="#">timer_mode_t</a>	mode	
		Select enumerated value from <a href="#">timer_mode_t</a> .
uint32_t	<a href="#">period_counts</a>	
		Period in raw timer counts.
<a href="#">timer_source_div_t</a>	source_div	
		Source clock divider.
uint32_t	<a href="#">duty_cycle_counts</a>	

	Duty cycle in counts.
uint8_t	<a href="#">channel</a>
uint8_t	<a href="#">cycle_end_ipr</a>
	Cycle end interrupt priority.
IRQn_Type	<a href="#">cycle_end_irq</a>
	Cycle end interrupt.
void(*	<a href="#">p_callback</a> )( <a href="#">timer_callback_args_t</a> *p_args)
void const *	<a href="#">p_context</a>
void const *	<a href="#">p_extend</a>
	Extension parameter for hardware specific settings.

## Field Documentation

### ◆ channel

uint8\_t timer\_cfg\_t::channel

Select a channel corresponding to the channel number of the hardware.

### ◆ p\_callback

void(\* timer\_cfg\_t::p\_callback) ([timer\\_callback\\_args\\_t](#) \*p\_args)

Callback provided when a timer ISR occurs. Set to NULL for no CPU interrupt.

### ◆ p\_context

void const\* timer\_cfg\_t::p\_context

Placeholder for user data. Passed to the user callback in [timer\\_callback\\_args\\_t](#).

### ◆ timer\_api\_t

struct timer\_api\_t

Timer API structure. General timer functions implemented at the HAL layer follow this API.

### Data Fields

<code>fsp_err_t(*</code>	<code>open )(timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>start )(timer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>stop )(timer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>reset )(timer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>enable )(timer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>disable )(timer_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>periodSet )(timer_ctrl_t *const p_ctrl, uint32_t const period)</code>
<code>fsp_err_t(*</code>	<code>dutyCycleSet )(timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(timer_ctrl_t *const p_api_ctrl, void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(timer_ctrl_t *const p_ctrl)</code>

### Field Documentation

◆ **open**

```
fsp_err_t(* timer_api_t::open) (timer_ctrl_t *const p_ctrl, timer_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_GPT\_Open()
- R\_AGT\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **start**

```
fsp_err_t(* timer_api_t::start) (timer_ctrl_t *const p_ctrl)
```

Start the counter.

**Implemented as**

- R\_GPT\_Start()
- R\_AGT\_Start()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **stop**

```
fsp_err_t(* timer_api_t::stop) (timer_ctrl_t *const p_ctrl)
```

Stop the counter.

**Implemented as**

- R\_GPT\_Stop()
- R\_AGT\_Stop()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **reset**

```
fsp_err_t(* timer_api_t::reset) (timer_ctrl_t *const p_ctrl)
```

Reset the counter to the initial value.

**Implemented as**

- R\_GPT\_Reset()
- R\_AGT\_Reset()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **enable**

```
fsp_err_t(* timer_api_t::enable) (timer_ctrl_t *const p_ctrl)
```

Enables input capture.

**Implemented as**

- R\_GPT\_Enable()
- R\_AGT\_Enable()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **disable**

```
fsp_err_t(* timer_api_t::disable) (timer_ctrl_t *const p_ctrl)
```

Disables input capture.

**Implemented as**

- R\_GPT\_Disable()
- R\_AGT\_Disable()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **periodSet**

```
fsp_err_t(* timer_api_t::periodSet) (timer_ctrl_t *const p_ctrl, uint32_t const period)
```

Set the time until the timer expires. See implementation for details of period update timing.

**Implemented as**

- R\_GPT\_PeriodSet()
- R\_AGT\_PeriodSet()

**Note**

*Timer expiration may or may not generate a CPU interrupt based on how the timer is configured in `timer_api_t::open`.*

**Parameters**

[in]	p_ctrl	Control block set in <code>timer_api_t::open</code> call for this timer.
[in]	p_period	Time until timer should expire.

◆ **dutyCycleSet**

```
fsp_err_t(* timer_api_t::dutyCycleSet) (timer_ctrl_t *const p_ctrl, uint32_t const duty_cycle_counts, uint32_t const pin)
```

Sets the number of counts for the pin level to be high. If the timer is counting, the updated duty cycle is reflected after the next timer expiration.

**Implemented as**

- R\_GPT\_DutyCycleSet()
- R\_AGT\_DutyCycleSet()

**Parameters**

[in]	p_ctrl	Control block set in <code>timer_api_t::open</code> call for this timer.
[in]	duty_cycle_counts	Time until duty cycle should expire.
[in]	pin	Which output pin to update. See implementation for details.

## ◆ infoGet

```
fsp_err_t(* timer_api_t::infoGet) (timer_ctrl_t *const p_ctrl, timer_info_t *const p_info)
```

Stores timer information in p\_info.

**Implemented as**

- R\_GPT\_InfoGet()
- R\_AGT\_InfoGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[out]	p_info	Collection of information for this timer.

## ◆ statusGet

```
fsp_err_t(* timer_api_t::statusGet) (timer_ctrl_t *const p_ctrl, timer_status_t *const p_status)
```

Get the current counter value and timer state and store it in p\_status.

**Implemented as**

- R\_GPT\_StatusGet()
- R\_AGT\_StatusGet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[out]	p_status	Current status of this timer.

◆ **callbackSet**

```
fsp_err_t(* timer_api_t::callbackSet) (timer_ctrl_t *const p_api_ctrl,
void(*p_callback)(timer_callback_args_t *), void const *const p_context, timer_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_GPT\_CallbackSet()
- R\_AGT\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* timer_api_t::close) (timer_ctrl_t *const p_ctrl)
```

Allows driver to be reconfigured and may reduce power consumption.

**Implemented as**

- R\_GPT\_Close()
- R\_AGT\_Close()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">timer_api_t::open</a> call for this timer.
------	--------	---

◆ **timer\_instance\_t**

```
struct timer_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">timer_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
--------------------------------	--------	---

<code>timer_cfg_t</code> const *	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>timer_api_t</code> const *	<code>p_api</code>	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `timer_ctrl_t`

typedef void <code>timer_ctrl_t</code>
Timer control block. Allocate an instance specific control block to pass into the timer API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <code>gpt_instance_ctrl_t</code></li> <li>◦ <code>agt_instance_ctrl_t</code></li> </ul>

## Enumeration Type Documentation

### ◆ `timer_event_t`

enum <code>timer_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>TIMER_EVENT_CYCLE_END</code>	Requested timer delay has expired or timer has wrapped around.
<code>TIMER_EVENT_CREST</code>	Timer crest event (counter is at a maximum, triangle-wave PWM only)
<code>TIMER_EVENT_CAPTURE_A</code>	A capture has occurred on signal A.
<code>TIMER_EVENT_CAPTURE_B</code>	A capture has occurred on signal B.
<code>TIMER_EVENT_TROUGH</code>	Timer trough event (counter is 0, triangle-wave PWM only).

◆ **timer\_variant\_t**

enum <a href="#">timer_variant_t</a>	
Timer variant types.	
Enumerator	
TIMER_VARIANT_32_BIT	32-bit timer
TIMER_VARIANT_16_BIT	16-bit timer

◆ **timer\_state\_t**

enum <a href="#">timer_state_t</a>	
Possible status values returned by <a href="#">timer_api_t::statusGet</a> .	
Enumerator	
TIMER_STATE_STOPPED	Timer is stopped.
TIMER_STATE_COUNTING	Timer is running.

◆ **timer\_mode\_t**

enum <a href="#">timer_mode_t</a>	
Timer operational modes	
Enumerator	
TIMER_MODE_PERIODIC	Timer restarts after period elapses.
TIMER_MODE_ONE_SHOT	Timer stops after period elapses.
TIMER_MODE_PWM	Timer generates saw-wave PWM output.
TIMER_MODE_TRIANGLE_WAVE_SYMMETRIC_PWM	Timer generates symmetric triangle-wave PWM output.
TIMER_MODE_TRIANGLE_WAVE_ASYMMETRIC_PWM	Timer generates asymmetric triangle-wave PWM output.
TIMER_MODE_TRIANGLE_WAVE_ASYMMETRIC_PWM_MODE3	Timer generates Asymmetric Triangle-wave PWM output. In PWM mode 3, the duty cycle does not need to be updated at each trough/crest interrupt. Instead, the trough and crest duty cycle values can be set once and only need to be updated when the application needs to change the duty cycle.

◆ **timer\_direction\_t**

enum <a href="#">timer_direction_t</a>	
Direction of timer count	
Enumerator	
TIMER_DIRECTION_DOWN	Timer count goes up.
TIMER_DIRECTION_UP	Timer count goes down.

◆ **timer\_source\_div\_t**

enum <code>timer_source_div_t</code>	
PCLK divisors	
Enumerator	
<code>TIMER_SOURCE_DIV_1</code>	Timer clock source divided by 1.
<code>TIMER_SOURCE_DIV_2</code>	Timer clock source divided by 2.
<code>TIMER_SOURCE_DIV_4</code>	Timer clock source divided by 4.
<code>TIMER_SOURCE_DIV_8</code>	Timer clock source divided by 8.
<code>TIMER_SOURCE_DIV_16</code>	Timer clock source divided by 16.
<code>TIMER_SOURCE_DIV_32</code>	Timer clock source divided by 32.
<code>TIMER_SOURCE_DIV_64</code>	Timer clock source divided by 64.
<code>TIMER_SOURCE_DIV_128</code>	Timer clock source divided by 128.
<code>TIMER_SOURCE_DIV_256</code>	Timer clock source divided by 256.
<code>TIMER_SOURCE_DIV_1024</code>	Timer clock source divided by 1024.

### 4.3.37 Transfer Interface

#### Interfaces

#### Detailed Description

Interface for data transfer functions.

## Summary

The transfer interface supports background data transfer (no CPU intervention).

Implemented by:

- [Data Transfer Controller \(r\\_dtc\)](#)
- [Direct Memory Access Controller \(r\\_dmac\)](#)

#### Data Structures

struct [transfer\\_properties\\_t](#)

struct [transfer\\_info\\_t](#)

struct [transfer\\_cfg\\_t](#)

struct [transfer\\_api\\_t](#)

struct [transfer\\_instance\\_t](#)

## Typedefs

typedef void [transfer\\_ctrl\\_t](#)

## Enumerations

enum [transfer\\_mode\\_t](#)

enum [transfer\\_size\\_t](#)

enum [transfer\\_addr\\_mode\\_t](#)

enum [transfer\\_repeat\\_area\\_t](#)

enum [transfer\\_chain\\_mode\\_t](#)

enum [transfer\\_irq\\_t](#)

enum [transfer\\_start\\_mode\\_t](#)

## Data Structure Documentation

### ◆ [transfer\\_properties\\_t](#)

struct <a href="#">transfer_properties_t</a>		
Driver specific information.		
Data Fields		
uint32_t	block_count_max	Maximum number of blocks.
uint32_t	block_count_remaining	Number of blocks remaining.
uint32_t	transfer_length_max	Maximum number of transfers.
uint32_t	transfer_length_remaining	Number of transfers remaining.

### ◆ [transfer\\_info\\_t](#)

struct <a href="#">transfer_info_t</a>		
This structure specifies the properties of the transfer.		

**Warning**

When using DTC, this structure corresponds to the descriptor block registers required by the DTC. The following components may be modified by the driver: `p_src`, `p_dest`, `num_blocks`, and `length`.

When using DTC, do NOT reuse this structure to configure multiple transfers. Each transfer must have a unique [transfer\\_info\\_t](#).

When using DTC, this structure must not be allocated in a temporary location. Any instance of this structure must remain in scope until the transfer it is used for is closed.

**Note**

*When using DTC, consider placing instances of this structure in a protected section of memory.*

Data Fields		
union <a href="#">transfer_info_t</a>	<code>__unnamed__</code>	
void const *volatile	<code>p_src</code>	Source pointer.
void *volatile	<code>p_dest</code>	Destination pointer.
volatile uint16_t	<code>num_blocks</code>	Number of blocks to transfer when using <a href="#">TRANSFER_MODE_BLOCK</a> (both DTC and DMAC) or <a href="#">TRANSFER_MODE_REPEAT</a> (DMAC only) or <a href="#">TRANSFER_MODE_REPEAT_BLOCK</a> (DMAC only), unused in other modes.
volatile uint16_t	<code>length</code>	Length of each transfer. Range limited for <a href="#">TRANSFER_MODE_BLOCK</a> , <a href="#">TRANSFER_MODE_REPEAT</a> , and <a href="#">TRANSFER_MODE_REPEAT_BLOCK</a> see HAL driver for details.

**◆ transfer\_cfg\_t**

Data Fields		
<a href="#">transfer_info_t</a> *	<code>p_info</code>	Pointer to transfer configuration options. If using chain transfer (DTC only), this can be a pointer to an array of chained transfers that will be completed in order.
void const *	<code>p_extend</code>	Extension parameter for hardware specific settings.

**◆ transfer\_api\_t**

Data Fields		
<a href="#">transfer_info_t</a> *	<code>p_info</code>	Pointer to transfer configuration options. If using chain transfer (DTC only), this can be a pointer to an array of chained transfers that will be completed in order.
void const *	<code>p_extend</code>	Extension parameter for hardware specific settings.

Transfer functions implemented at the HAL layer will follow this API.

Data Fields	
fsp_err_t(*	open )(transfer_ctrl_t *const p_ctrl, transfer_cfg_t const *const p_cfg)
fsp_err_t(*	reconfigure )(transfer_ctrl_t *const p_ctrl, transfer_info_t *p_info)
fsp_err_t(*	reset )(transfer_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint16_t const num_transfers)
fsp_err_t(*	enable )(transfer_ctrl_t *const p_ctrl)
fsp_err_t(*	disable )(transfer_ctrl_t *const p_ctrl)
fsp_err_t(*	softwareStart )(transfer_ctrl_t *const p_ctrl, transfer_start_mode_t mode)
fsp_err_t(*	softwareStop )(transfer_ctrl_t *const p_ctrl)
fsp_err_t(*	infoGet )(transfer_ctrl_t *const p_ctrl, transfer_properties_t *const p_properties)
fsp_err_t(*	close )(transfer_ctrl_t *const p_ctrl)
Field Documentation	

◆ **open**

```
fsp_err_t(* transfer_api_t::open) (transfer_ctrl_t *const p_ctrl, transfer_cfg_t const *const p_cfg)
```

Initial configuration.

**Implemented as**

- R\_DTC\_Open()
- R\_DMACE\_Open()

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **reconfigure**

```
fsp_err_t(* transfer_api_t::reconfigure) (transfer_ctrl_t *const p_ctrl, transfer_info_t *p_info)
```

Reconfigure the transfer. Enable the transfer if p\_info is valid.

**Implemented as**

- R\_DTC\_Reconfigure()
- R\_DMACE\_Reconfigure()

**Parameters**

[in,out]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_info	Pointer to a new transfer info structure.

◆ **reset**

```
fsp_err_t(* transfer_api_t::reset) (transfer_ctrl_t *const p_ctrl, void const *p_src, void *p_dest,
uint16_t const num_transfers)
```

Reset source address pointer, destination address pointer, and/or length, keeping all other settings the same. Enable the transfer if p\_src, p\_dest, and length are valid.

**Implemented as**

- R\_DTC\_Reset()
- R\_DMACE\_Reset()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
[in]	p_src	Pointer to source. Set to NULL if source pointer should not change.
[in]	p_dest	Pointer to destination. Set to NULL if destination pointer should not change.
[in]	num_transfers	Transfer length in normal mode or number of blocks in block mode. In DMACE only, resets number of repeats (initially stored in <a href="#">transfer_info_t::num_blocks</a> ) in repeat mode. Not used in repeat mode for DTC.

◆ **enable**

```
fsp_err_t(* transfer_api_t::enable) (transfer_ctrl_t *const p_ctrl)
```

Enable transfer. Transfers occur after the activation source event (or when [transfer\\_api\\_t::softwareStart](#) is called if ELC\_EVENT\_ELC\_NONE is chosen as activation source).

**Implemented as**

- R\_DTC\_Enable()
- R\_DMACE\_Enable()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">transfer_api_t::open</a> call for this transfer.
------	--------	---

◆ **disable**

`fsp_err_t(* transfer_api_t::disable) (transfer_ctrl_t *const p_ctrl)`

Disable transfer. Transfers do not occur after the activation source event (or when `transfer_api_t::softwareStart` is called if `ELC_EVENT_ELC_NONE` is chosen as the DMAC activation source).

**Note**

*If a transfer is in progress, it will be completed. Subsequent transfer requests do not cause a transfer.*

**Implemented as**

- `R_DTC_Disable()`
- `R_DMAC_Disable()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
------	--------	--

◆ **softwareStart**

`fsp_err_t(* transfer_api_t::softwareStart) (transfer_ctrl_t *const p_ctrl, transfer_start_mode_t mode)`

Start transfer in software.

**Warning**

Only works if `ELC_EVENT_ELC_NONE` is chosen as the DMAC activation source.

**Note**

*Not supported for DTC.*

**Implemented as**

- `R_DMAC_SoftwareStart()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
[in]	mode	Select mode from <code>transfer_start_mode_t</code> .

## ◆ softwareStop

`fsp_err_t(* transfer_api_t::softwareStop) (transfer_ctrl_t *const p_ctrl)`

Stop transfer in software. The transfer will stop after completion of the current transfer.

*Note*

*Not supported for DTC.*

*Only applies for transfers started with TRANSFER\_START\_MODE\_REPEAT.*

**Warning**

Only works if ELC\_EVENT\_ELC\_NONE is chosen as the DMAC activation source.

**Implemented as**

- `R_DMAMAC_SoftwareStop()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
------	--------	--

## ◆ infoGet

`fsp_err_t(* transfer_api_t::infoGet) (transfer_ctrl_t *const p_ctrl, transfer_properties_t *const p_properties)`

Provides information about this transfer.

**Implemented as**

- `R_DTC_InfoGet()`
- `R_DMAMAC_InfoGet()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
[out]	p_properties	Driver specific information.

## ◆ close

`fsp_err_t(* transfer_api_t::close) (transfer_ctrl_t *const p_ctrl)`

Releases hardware lock. This allows a transfer to be reconfigured using `transfer_api_t::open`.

**Implemented as**

- `R_DTC_Close()`
- `R_DMAMAC_Close()`

**Parameters**

[in]	p_ctrl	Control block set in <code>transfer_api_t::open</code> call for this transfer.
------	--------	--

◆ **transfer\_instance\_t**

struct transfer_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
<a href="#">transfer_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">transfer_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">transfer_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **transfer\_ctrl\_t**

typedef void <a href="#">transfer_ctrl_t</a>
Transfer control block. Allocate an instance specific control block to pass into the transfer API calls.
<b>Implemented as</b>
<ul style="list-style-type: none"> <li>◦ <a href="#">dte_instance_ctrl_t</a></li> <li>◦ <a href="#">dmac_instance_ctrl_t</a></li> </ul>

**Enumeration Type Documentation**

◆ **transfer\_mode\_t**

enum <code>transfer_mode_t</code>	
Transfer mode describes what will happen when a transfer request occurs.	
Enumerator	
<code>TRANSFER_MODE_NORMAL</code>	In normal mode, each transfer request causes a transfer of <code>transfer_size_t</code> from the source pointer to the destination pointer. The transfer length is decremented and the source and address pointers are updated according to <code>transfer_addr_mode_t</code> . After the transfer length reaches 0, transfer requests will not cause any further transfers.
<code>TRANSFER_MODE_REPEAT</code>	Repeat mode is like normal mode, except that when the transfer length reaches 0, the pointer to the repeat area and the transfer length will be reset to their initial values. If DMAC is used, the transfer repeats only <code>transfer_info_t::num_blocks</code> times. After the transfer repeats <code>transfer_info_t::num_blocks</code> times, transfer requests will not cause any further transfers. If DTC is used, the transfer repeats continuously (no limit to the number of repeat transfers).
<code>TRANSFER_MODE_BLOCK</code>	In block mode, each transfer request causes <code>transfer_info_t::length</code> transfers of <code>transfer_size_t</code> . After each individual transfer, the source and destination pointers are updated according to <code>transfer_addr_mode_t</code> . After the block transfer is complete, <code>transfer_info_t::num_blocks</code> is decremented. After the <code>transfer_info_t::num_blocks</code> reaches 0, transfer requests will not cause any further transfers.
<code>TRANSFER_MODE_REPEAT_BLOCK</code>	In addition to block mode features, repeat-block mode supports a ring buffer of blocks and offsets within a block (to split blocks into arrays of their first data, second data, etc.)

◆ **transfer\_size\_t**

enum <a href="#">transfer_size_t</a>	
Transfer size specifies the size of each individual transfer. Total transfer length = <code>transfer_size_t * transfer_length_t</code>	
Enumerator	
TRANSFER_SIZE_1_BYTE	Each transfer transfers a 8-bit value.
TRANSFER_SIZE_2_BYTE	Each transfer transfers a 16-bit value.
TRANSFER_SIZE_4_BYTE	Each transfer transfers a 32-bit value.

◆ **transfer\_addr\_mode\_t**

enum <a href="#">transfer_addr_mode_t</a>	
Address mode specifies whether to modify (increment or decrement) pointer after each transfer.	
Enumerator	
TRANSFER_ADDR_MODE_FIXED	Address pointer remains fixed after each transfer.
TRANSFER_ADDR_MODE_OFFSET	Offset is added to the address pointer after each transfer.
TRANSFER_ADDR_MODE_INCREMENTED	Address pointer is incremented by associated <a href="#">transfer_size_t</a> after each transfer.
TRANSFER_ADDR_MODE_DECREMENTED	Address pointer is decremented by associated <a href="#">transfer_size_t</a> after each transfer.

◆ **transfer\_repeat\_area\_t**

enum <a href="#">transfer_repeat_area_t</a>	
Repeat area options (source or destination). In <a href="#">TRANSFER_MODE_REPEAT</a> , the selected pointer returns to its original value after <a href="#">transfer_info_t::length</a> transfers. In <a href="#">TRANSFER_MODE_BLOCK</a> and <a href="#">TRANSFER_MODE_REPEAT_BLOCK</a> , the selected pointer returns to its original value after each transfer.	
Enumerator	
<a href="#">TRANSFER_REPEAT_AREA_DESTINATION</a>	Destination area repeated in <a href="#">TRANSFER_MODE_REPEAT</a> or <a href="#">TRANSFER_MODE_BLOCK</a> or <a href="#">TRANSFER_MODE_REPEAT_BLOCK</a> .
<a href="#">TRANSFER_REPEAT_AREA_SOURCE</a>	Source area repeated in <a href="#">TRANSFER_MODE_REPEAT</a> or <a href="#">TRANSFER_MODE_BLOCK</a> or <a href="#">TRANSFER_MODE_REPEAT_BLOCK</a> .

◆ **transfer\_chain\_mode\_t**

enum <a href="#">transfer_chain_mode_t</a>	
Chain transfer mode options.	
<i>Note</i> <i>Only applies for DTC.</i>	
Enumerator	
<a href="#">TRANSFER_CHAIN_MODE_DISABLED</a>	Chain mode not used.
<a href="#">TRANSFER_CHAIN_MODE_EACH</a>	Switch to next transfer after a single transfer from this <a href="#">transfer_info_t</a> .
<a href="#">TRANSFER_CHAIN_MODE_END</a>	Complete the entire transfer defined in this <a href="#">transfer_info_t</a> before chaining to next transfer.

◆ **transfer\_irq\_t**

enum <code>transfer_irq_t</code>	
Interrupt options.	
Enumerator	
TRANSFER_IRQ_END	<p>Interrupt occurs only after last transfer. If this transfer is chained to a subsequent transfer, the interrupt will occur only after subsequent chained transfer(s) are complete.</p> <p><b>Warning</b> DTC triggers the interrupt of the activation source. Choosing TRANSFER_IRQ_END with DTC will prevent activation source interrupts until the transfer is complete.</p>
TRANSFER_IRQ_EACH	<p>Interrupt occurs after each transfer.</p> <p><i>Note</i> <i>Not available in all HAL drivers. See HAL driver for details.</i></p>

◆ **transfer\_start\_mode\_t**

enum <code>transfer_start_mode_t</code>	
Select whether to start single or repeated transfer with software start.	
Enumerator	
TRANSFER_START_MODE_SINGLE	Software start triggers single transfer.
TRANSFER_START_MODE_REPEAT	Software start transfer continues until transfer is complete.

## 4.3.38 UART Interface

### Interfaces

#### Detailed Description

Interface for UART communications.

## Summary

The UART interface provides common APIs for UART HAL drivers. The UART interface supports the following features:

- Full-duplex UART communication
- Interrupt driven transmit/receive processing
- Callback function with returned event code
- Runtime baud-rate change
- Hardware resource locking during a transaction
- CTS/RTS hardware flow control support (with an associated IOPORT pin)

Implemented by:

- [Serial Communications Interface \(SCI\) UART \(r\\_sci\\_uart\)](#)

### Data Structures

struct [uart\\_info\\_t](#)

struct [uart\\_callback\\_args\\_t](#)

struct [uart\\_cfg\\_t](#)

struct [uart\\_api\\_t](#)

struct [uart\\_instance\\_t](#)

### Typedefs

typedef void [uart\\_ctrl\\_t](#)

### Enumerations

enum [uart\\_event\\_t](#)

enum [uart\\_data\\_bits\\_t](#)

enum [uart\\_parity\\_t](#)

enum [uart\\_stop\\_bits\\_t](#)

enum [uart\\_dir\\_t](#)

### Data Structure Documentation

#### ◆ [uart\\_info\\_t](#)

struct [uart\\_info\\_t](#)

UART driver specific information

Data Fields

uint32_t	write_bytes_max	Maximum bytes that can be written at this time. Only applies if <a href="#">uart_cfg_t::p_transfer_tx</a> is not NULL.
uint32_t	read_bytes_max	Maximum bytes that are available to read at one time. Only applies if <a href="#">uart_cfg_t::p_transfer_rx</a> is not NULL.

◆ **uart\_callback\_args\_t**

struct uart_callback_args_t		
UART Callback parameter definition		
Data Fields		
uint32_t	channel	Device channel number.
<a href="#">uart_event_t</a>	event	Event code.
uint32_t	data	Contains the next character received for the events UART_EVENT_RX_CHAR, UART_EVENT_ERR_PARITY, UART_EVENT_ERR_FRAMING, or UART_EVENT_ERR_OVERFLOW. Otherwise unused.
void const *	p_context	Context provided to user during callback.

◆ **uart\_cfg\_t**

struct uart_cfg_t	
UART Configuration	
<b>Data Fields</b>	
uint8_t	<a href="#">channel</a>
	Select a channel corresponding to the channel number of the hardware.
<a href="#">uart_data_bits_t</a>	<a href="#">data_bits</a>
	Data bit length (8 or 7 or 9)
<a href="#">uart_parity_t</a>	<a href="#">parity</a>
	Parity type (none or odd or even)

<code>uart_stop_bits_t</code>	<code>stop_bits</code>
	Stop bit length (1 or 2)
<code>uint8_t</code>	<code>rx_ipl</code>
	Receive interrupt priority.
<code>IRQn_Type</code>	<code>rx_irq</code>
	Receive interrupt IRQ number.
<code>uint8_t</code>	<code>tx_ipl</code>
	Transmit interrupt priority.
<code>IRQn_Type</code>	<code>tx_irq</code>
	Transmit interrupt IRQ number.
<code>uint8_t</code>	<code>tei_ipl</code>
	Transmit end interrupt priority.
<code>IRQn_Type</code>	<code>tei_irq</code>
	Transmit end interrupt IRQ number.
<code>uint8_t</code>	<code>eri_ipl</code>
	Error interrupt priority.
<code>IRQn_Type</code>	<code>eri_irq</code>
	Error interrupt IRQ number.

<code>transfer_instance_t const *</code>	<code>p_transfer_rx</code>
<code>transfer_instance_t const *</code>	<code>p_transfer_tx</code>
<code>void(*</code>	<code>p_callback )(uart_callback_args_t *p_args)</code>
	Pointer to callback function.
<code>void const *</code>	<code>p_context</code>
	User defined context passed into callback function.
<code>void const *</code>	<code>p_extend</code>
	UART hardware dependent configuration.

## Field Documentation

### ◆ `p_transfer_rx`

`transfer_instance_t const* uart_cfg_t::p_transfer_rx`

Optional transfer instance used to receive multiple bytes without interrupts. Set to NULL if unused. If NULL, the number of bytes allowed in the read API is limited to one byte at a time.

### ◆ `p_transfer_tx`

`transfer_instance_t const* uart_cfg_t::p_transfer_tx`

Optional transfer instance used to send multiple bytes without interrupts. Set to NULL if unused. If NULL, the number of bytes allowed in the write APIs is limited to one byte at a time.

### ◆ `uart_api_t`

`struct uart_api_t`

Shared Interface definition for UART

#### Data Fields

<code>fsp_err_t(*</code>	<code>open )(uart_ctrl_t *const p_ctrl, uart_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>read )(uart_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)</code>
<code>fsp_err_t(*</code>	<code>write )(uart_ctrl_t *const p_ctrl, uint8_t const *const p_src, uint32_t</code>

	const bytes)
<code>fsp_err_t(*</code>	<code>baudSet )(uart_ctrl_t *const p_ctrl, void const *const p_baudrate_info)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(uart_ctrl_t *const p_ctrl, uart_info_t *const p_info)</code>
<code>fsp_err_t(*</code>	<code>communicationAbort )(uart_ctrl_t *const p_ctrl, uart_dir_t communication_to_abort)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(uart_ctrl_t *const p_api_ctrl, void(*p_callback)(uart_callback_args_t *), void const *const p_context, uart_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(uart_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>readStop )(uart_ctrl_t *const p_ctrl, uint32_t *remaining_bytes)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* uart_api_t::open) (uart_ctrl_t *const p_ctrl, uart_cfg_t const *const p_cfg)`

Open UART device.

### Implemented as

- `R_SCI_UART_Open()`

### Parameters

[in,out]	<code>p_ctrl</code>	Pointer to the UART control block. Must be declared by user. Value set here.
[in]	<code>uart_cfg_t</code>	Pointer to UART configuration structure. All elements of this structure must be set by user.

## ◆ read

`fsp_err_t(* uart_api_t::read) (uart_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)`

Read from UART device. The read buffer is used until the read is complete. When a transfer is complete, the callback is called with event `UART_EVENT_RX_COMPLETE`. Bytes received outside an active transfer are received in the callback function with event `UART_EVENT_RX_CHAR`. The maximum transfer size is reported by `infoGet()`.

**Implemented as**

- `R_SCI_UART_Read()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the UART control block for the channel.
[in]	<code>p_dest</code>	Destination address to read data from.
[in]	<code>bytes</code>	Read data length.

## ◆ write

`fsp_err_t(* uart_api_t::write) (uart_ctrl_t *const p_ctrl, uint8_t const *const p_src, uint32_t const bytes)`

Write to UART device. The write buffer is used until write is complete. Do not overwrite write buffer contents until the write is finished. When the write is complete (all bytes are fully transmitted on the wire), the callback called with event `UART_EVENT_TX_COMPLETE`. The maximum transfer size is reported by `infoGet()`.

**Implemented as**

- `R_SCI_UART_Write()`

**Parameters**

[in]	<code>p_ctrl</code>	Pointer to the UART control block.
[in]	<code>p_src</code>	Source address to write data to.
[in]	<code>bytes</code>	Write data length.

◆ **baudSet**

```
fsp_err_t(* uart_api_t::baudSet) (uart_ctrl_t *const p_ctrl, void const *const p_baudrate_info)
```

Change baud rate.

**Warning**

Calling this API aborts any in-progress transmission and disables reception until the new baud settings have been applied.

**Implemented as**

- R\_SCI\_UART\_BaudSet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	p_baudrate_info	Pointer to module specific information for configuring baud rate.

◆ **infoGet**

```
fsp_err_t(* uart_api_t::infoGet) (uart_ctrl_t *const p_ctrl, uart_info_t *const p_info)
```

Get the driver specific information.

**Implemented as**

- R\_SCI\_UART\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	baudrate	Baud rate in bps.

◆ **communicationAbort**

```
fsp_err_t(* uart_api_t::communicationAbort) (uart_ctrl_t *const p_ctrl, uart_dir_t communication_to_abort)
```

Abort ongoing transfer.

**Implemented as**

- R\_SCI\_UART\_Abort()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	communication_to_abort	Type of abort request.

◆ **callbackSet**

```
fsp_err_t(* uart_api_t::callbackSet) (uart_ctrl_t *const p_api_ctrl,
void(*p_callback)(uart_callback_args_t *), void const *const p_context, uart_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- R\_SCI\_Uart\_CallbackSet()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* uart_api_t::close) (uart_ctrl_t *const p_ctrl)
```

Close UART device.

**Implemented as**

- R\_SCI\_UART\_Close()

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
------	--------	------------------------------------

◆ **readStop**

```
fsp_err_t(* uart_api_t::readStop) (uart_ctrl_t *const p_ctrl, uint32_t *remaining_bytes)
```

Stop ongoing read and return the number of bytes remaining in the read.

**Implemented as**

- [R\\_SCI\\_UART\\_ReadStop\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the UART control block.
[in,out]	remaining_bytes	Pointer to location to store remaining bytes for read.

◆ **uart\_instance\_t**

```
struct uart_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">uart_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">uart_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">uart_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **uart\_ctrl\_t**

```
typedef void uart_ctrl_t
```

UART control block. Allocate an instance specific control block to pass into the UART API calls.

**Implemented as**

- [sci\\_uart\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

◆ **uart\_event\_t**

enum <code>uart_event_t</code>	
UART Event codes	
Enumerator	
<code>UART_EVENT_RX_COMPLETE</code>	Receive complete event.
<code>UART_EVENT_TX_COMPLETE</code>	Transmit complete event.
<code>UART_EVENT_RX_CHAR</code>	Character received.
<code>UART_EVENT_ERR_PARITY</code>	Parity error event.
<code>UART_EVENT_ERR_FRAMING</code>	Mode fault error event.
<code>UART_EVENT_ERR_OVERFLOW</code>	FIFO Overflow error event.
<code>UART_EVENT_BREAK_DETECT</code>	Break detect error event.
<code>UART_EVENT_TX_DATA_EMPTY</code>	Last byte is transmitting, ready for more data.

◆ **uart\_data\_bits\_t**

enum <code>uart_data_bits_t</code>	
UART Data bit length definition	
Enumerator	
<code>UART_DATA_BITS_8</code>	Data bits 8-bit.
<code>UART_DATA_BITS_7</code>	Data bits 7-bit.
<code>UART_DATA_BITS_9</code>	Data bits 9-bit.

◆ **uart\_parity\_t**

enum <a href="#">uart_parity_t</a>	
UART Parity definition	
Enumerator	
UART_PARITY_OFF	No parity.
UART_PARITY_EVEN	Even parity.
UART_PARITY_ODD	Odd parity.

◆ **uart\_stop\_bits\_t**

enum <a href="#">uart_stop_bits_t</a>	
UART Stop bits definition	
Enumerator	
UART_STOP_BITS_1	Stop bit 1-bit.
UART_STOP_BITS_2	Stop bits 2-bit.

◆ **uart\_dir\_t**

enum <a href="#">uart_dir_t</a>	
UART transaction definition	
Enumerator	
UART_DIR_RX_TX	Both RX and TX.
UART_DIR_RX	Only RX.
UART_DIR_TX	Only TX.

**4.3.39 USB Interface**[Interfaces](#)**Detailed Description**

Interface for USB functions.

## Summary

The USB interface provides USB functionality.

The USB interface can be implemented by:

- [USB \(r\\_usb\\_basic\)](#)

### Data Structures

struct [usb\\_cfg\\_t](#)

struct [usb\\_api\\_t](#)

struct [usb\\_instance\\_t](#)

### Macros

#define [USB\\_BREQUEST](#)  
b15-8

#define [USB\\_GET\\_STATUS](#)  
USB Standard request Get Status.

#define [USB\\_CLEAR\\_FEATURE](#)  
USB Standard request Clear Feature.

#define [USB\\_REQRESERVED](#)  
USB Standard request Reqreserved.

#define [USB\\_SET\\_FEATURE](#)  
USB Standard request Set Feature.

#define [USB\\_REQRESERVED1](#)  
USB Standard request Reqreserved1.

#define [USB\\_SET\\_ADDRESS](#)  
USB Standard request Set Address.

```
#define USB_GET_DESCRIPTOR
USB Standard request Get Descriptor.
```

```
#define USB_SET_DESCRIPTOR
USB Standard request Set Descriptor.
```

```
#define USB_GET_CONFIGURATION
USB Standard request Get Configuration.
```

```
#define USB_SET_CONFIGURATION
USB Standard request Set Configuration.
```

```
#define USB_GET_INTERFACE
USB Standard request Get Interface.
```

```
#define USB_SET_INTERFACE
USB Standard request Set Interface.
```

```
#define USB_SYNCH_FRAME
USB Standard request Synch Frame.
```

```
#define USB_HOST_TO_DEV
From host to device.
```

```
#define USB_DEV_TO_HOST
From device to host.
```

```
#define USB_STANDARD
Standard Request.
```

```
#define USB_CLASS
Class Request.
```

```
#define USB_VENDOR
```

Vendor Request.

```
#define USB_DEVICE  
Device.
```

```
#define USB_INTERFACE  
Interface.
```

```
#define USB_ENDPOINT  
End Point.
```

```
#define USB_OTHER  
Other.
```

```
#define USB_NULL  
NULL pointer.
```

```
#define USB_IP0  
USB0 module.
```

```
#define USB_IP1  
USB1 module.
```

```
#define USB_PIPE0  
Pipe Number0.
```

```
#define USB_PIPE1  
Pipe Number1.
```

```
#define USB_PIPE2  
Pipe Number2.
```

```
#define USB_PIPE3  
Pipe Number3.
```

```
#define USB_PIPE4  
    Pipe Number4.
```

```
#define USB_PIPE5  
    Pipe Number5.
```

```
#define USB_PIPE6  
    Pipe Number6.
```

```
#define USB_PIPE7  
    Pipe Number7.
```

```
#define USB_PIPE8  
    Pipe Number8.
```

```
#define USB_PIPE9  
    Pipe Number9.
```

```
#define USB_EP0  
    End Point Number0.
```

```
#define USB_EP1  
    End Point Number1.
```

```
#define USB_EP2  
    End Point Number2.
```

```
#define USB_EP3  
    End Point Number3.
```

```
#define USB_EP4  
    End Point Number4.
```

```
#define USB_EP5  
End Point Number5.
```

```
#define USB_EP6  
End Point Number6.
```

```
#define USB_EP7  
End Point Number7.
```

```
#define USB_EP8  
End Point Number8.
```

```
#define USB_EP9  
End Point Number9.
```

```
#define USB_EP10  
End Point Number10.
```

```
#define USB_EP11  
End Point Number11.
```

```
#define USB_EP12  
End Point Number12.
```

```
#define USB_EP13  
End Point Number13.
```

```
#define USB_EP14  
End Point Number14.
```

```
#define USB_EP15  
End Point Number15.
```

```
#define USB_EP_DIR
```

b7: Endpoint Direction

```
#define USB_EP_DIR_IN  
b7: Endpoint Direction In
```

```
#define USB_EP_DIR_OUT  
b7: Endpoint Direction Out
```

```
#define USB_DT_DEVICE  
Device Descriptor.
```

```
#define USB_DT_CONFIGURATION  
Configuration Descriptor.
```

```
#define USB_DT_STRING  
String Descriptor.
```

```
#define USB_DT_INTERFACE  
Interface Descriptor.
```

```
#define USB_DT_ENDPOINT  
Endpoint Descriptor.
```

```
#define USB_DT_DEVICE_QUALIFIER  
Device Qualifier Descriptor.
```

```
#define USB_DT_OTHER_SPEED_CONF  
Other Speed Configuration Descriptor.
```

```
#define USB_DT_INTERFACE_POWER  
Interface Power Descriptor.
```

```
#define USB_DT_OTGDESCRIPTOR  
OTG Descriptor.
```

```
#define USB_DT_HUBDESCRIPTOR  
HUB descriptor.
```

```
#define USB_IFCLS_NOT  
Un corresponding Class.
```

```
#define USB_IFCLS_AUD  
Audio Class.
```

```
#define USB_IFCLS_CDC  
CDC Class.
```

```
#define USB_IFCLS_CDCC  
CDC-Control Class.
```

```
#define USB_IFCLS_HID  
HID Class.
```

```
#define USB_IFCLS_PHY  
Physical Class.
```

```
#define USB_IFCLS_IMG  
Image Class.
```

```
#define USB_IFCLS_PRN  
Printer Class.
```

```
#define USB_IFCLS_MAS  
Mass Storage Class.
```

```
#define USB_IFCLS_HUB  
HUB Class.
```

```
#define USB_IFCLS_CDCD
```

CDC-Data Class.

```
#define USB_IFCLS_CHIP
```

Chip/Smart Card Class.

```
#define USB_IFCLS_CNT
```

Content-Security Class.

```
#define USB_IFCLS_VID
```

Video Class.

```
#define USB_IFCLS_DIAG
```

Diagnostic Device.

```
#define USB_IFCLS_WIRE
```

Wireless Controller.

```
#define USB_IFCLS_APL
```

Application-Specific.

```
#define USB_IFCLS_VEN
```

Vendor-Specific Class.

```
#define USB_EP_IN
```

In Endpoint.

```
#define USB_EP_OUT
```

Out Endpoint.

```
#define USB_EP_ISO
```

Isochronous Transfer.

```
#define USB_EP_BULK
```

Bulk Transfer.

```
#define USB_EP_INT  
Interrupt Transfer.
```

```
#define USB_CF_RESERVED  
Reserved(set to 1)
```

```
#define USB_CF_SELFP  
Self Powered.
```

```
#define USB_CF_BUSP  
Bus Powered.
```

```
#define USB_CF_RWUPON  
Remote Wake up ON.
```

```
#define USB_CF_RWUPOFF  
Remote Wake up OFF.
```

```
#define USB_DD_BLENGTH  
Device Descriptor Length.
```

```
#define USB_CD_BLENGTH  
Configuration Descriptor Length.
```

```
#define USB_ID_BLENGTH  
Interface Descriptor Length.
```

```
#define USB_ED_BLENGTH  
Endpoint Descriptor Length.
```

## Typedefs

```
typedef void usb_ctrl_t
```

## Enumerations

enum [usb\\_speed\\_t](#)enum [usb\\_setup\\_status\\_t](#)enum [usb\\_status\\_t](#)enum [usb\\_class\\_t](#)enum [usb\\_bcport\\_t](#)enum [usb\\_onoff\\_t](#)enum [usb\\_transfer\\_t](#)enum [usb\\_transfer\\_type\\_t](#)enum [usb\\_mode\\_t](#)enum [usb\\_compliancetest\\_status\\_t](#)

## Data Structure Documentation

### ◆ [usb\\_cfg\\_t](#)

struct <a href="#">usb_cfg_t</a>		
USB configuration.		
Data Fields		
<a href="#">usb_mode_t</a>	usb_mode	USB_MODE_HOST/USB_MODE_P ERI.
<a href="#">usb_speed_t</a>	usb_speed	USB speed (USB_HS/USB_FS/USB_LS)
uint8_t	module_number	USB module number (USB_IP0/USB_IP1)
<a href="#">usb_class_t</a>	type	USB device class etc.
usb_descriptor_t *	p_usb_reg	Pointer to the <a href="#">usb_descriptor_t</a> structure area.
usb_compliance_cb_t	usb_compliance_cb	
IRQn_Type	irq	USBI dedicated interrupt number storage variable.
IRQn_Type	irq_r	USBR dedicated interrupt number storage variable.
IRQn_Type	irq_d0	FS D0FIFO dedicated interrupt

		number storage variable.
IRQn_Type	irq_d1	FS D1FIFO dedicated interrupt number storage variable.
IRQn_Type	hsirq	USBIR dedicated interrupt number storage variable.
IRQn_Type	hsirq_d0	HS D0FIFO dedicated interrupt number storage variable.
IRQn_Type	hsirq_d1	HS D1FIFO dedicated interrupt number storage variable.
uint8_t	ipl	Variable to store the interrupt priority of USBI.
uint8_t	ipl_r	Variable to store the interrupt priority of USBR.
uint8_t	ipl_d0	Variable to store the interrupt priority of FS D0FIFO.
uint8_t	ipl_d1	Variable to store the interrupt priority of FS D1FIFO.
uint8_t	hsipl	Variable to store the interrupt priority of USBIR.
uint8_t	hsipl_d0	Variable to store the interrupt priority of HS D0FIFO.
uint8_t	hsipl_d1	Variable to store the interrupt priority of HS D1FIFO.
usb_callback_t *	p_usb_apl_callback	Application Callback.
void const *	p_context	Other Context.
const transfer_instance_t *	p_transfer_tx	Send context.
const transfer_instance_t *	p_transfer_rx	Receive context.

#### ◆ usb\_api\_t

struct usb_api_t	
Functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(usb_ctrl_t *const p_api_ctrl)
fsp_err_t(*)	read )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t destination)

<code>fsp_err_t(*</code>	<code>write )(usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size, uint8_t destination)</code>
<code>fsp_err_t(*</code>	<code>stop )(usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t destination)</code>
<code>fsp_err_t(*</code>	<code>suspend )(usb_ctrl_t *const p_api_ctrl)</code>
<code>fsp_err_t(*</code>	<code>resume )(usb_ctrl_t *const p_api_ctrl)</code>
<code>fsp_err_t(*</code>	<code>vbusSet )(usb_ctrl_t *const p_api_ctrl, uint16_t state)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(usb_ctrl_t *const p_api_ctrl, usb_info_t *p_info, uint8_t destination)</code>
<code>fsp_err_t(*</code>	<code>pipeRead )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)</code>
<code>fsp_err_t(*</code>	<code>pipeWrite )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)</code>
<code>fsp_err_t(*</code>	<code>pipeStop )(usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number)</code>
<code>fsp_err_t(*</code>	<code>usedPipesGet )(usb_ctrl_t *const p_api_ctrl, uint16_t *p_pipe, uint8_t destination)</code>
<code>fsp_err_t(*</code>	<code>pipeInfoGet )(usb_ctrl_t *const p_api_ctrl, usb_pipe_t *p_info, uint8_t pipe_number)</code>
<code>fsp_err_t(*</code>	<code>eventGet )(usb_ctrl_t *const p_api_ctrl, usb_status_t *event)</code>
<code>fsp_err_t(*</code>	<code>callback )(usb_callback_t *p_callback)</code>
<code>fsp_err_t(*</code>	<code>pullUp )(usb_ctrl_t *const p_api_ctrl, uint8_t state)</code>
<code>fsp_err_t(*</code>	<code>hostControlTransfer )(usb_ctrl_t *const p_api_ctrl, usb_setup_t *p_setup, uint8_t *p_buf, uint8_t device_address)</code>

<code>fsp_err_t(*</code>	<code>periControlDataGet )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)</code>
<code>fsp_err_t(*</code>	<code>periControlDataSet )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)</code>
<code>fsp_err_t(*</code>	<code>periControlStatusSet )(usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status)</code>
<code>fsp_err_t(*</code>	<code>remoteWakeup )(usb_ctrl_t *const p_api_ctrl)</code>
<code>fsp_err_t(*</code>	<code>moduleNumberGet )(usb_ctrl_t *const p_api_ctrl, uint8_t *module_number)</code>
<code>fsp_err_t(*</code>	<code>classTypeGet )(usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type)</code>
<code>fsp_err_t(*</code>	<code>deviceAddressGet )(usb_ctrl_t *const p_api_ctrl, uint8_t *device_address)</code>
<code>fsp_err_t(*</code>	<code>pipeNumberGet )(usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number)</code>
<code>fsp_err_t(*</code>	<code>deviceStateGet )(usb_ctrl_t *const p_api_ctrl, uint16_t *state)</code>
<code>fsp_err_t(*</code>	<code>dataSizeGet )(usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)</code>
<code>fsp_err_t(*</code>	<code>setupGet )(usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)</code>
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* usb_api_t::open) (usb_ctrl_t *const p_api_ctrl, usb_cfg_t const *const p_cfg)
```

Start the USB module

**Implemented as**

- R\_USB\_Open()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* usb_api_t::close) (usb_ctrl_t *const p_api_ctrl)
```

Stop the USB module

**Implemented as**

- R\_USB\_Close()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **read**

```
fsp_err_t(* usb_api_t::read) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t destination)
```

Request USB data read

**Implemented as**

- R\_USB\_Read()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores read data.
[in]	size	Read request size.
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

## ◆ write

```
fsp_err_t(* usb_api_t::write) (usb_ctrl_t *const p_api_ctrl, uint8_t const *const p_buf, uint32_t size,
uint8_t destination)
```

Request USB data write

**Implemented as**

- R\_USB\_Write()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores write data.
[in]	size	Read request size.
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

## ◆ stop

```
fsp_err_t(* usb_api_t::stop) (usb_ctrl_t *const p_api_ctrl, usb_transfer_t direction, uint8_t
destination)
```

Stop USB data read/write processing

**Implemented as**

- R\_USB\_Stop()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	direction	Receive (USB_TRANSFER_READ) or send (USB_TRANSFER_WRITE).
[in]	destination	In Host mode, it represents the device address, and in Peripheral mode, it represents the device class.

◆ **suspend**

```
fsp_err_t(* usb_api_t::suspend) (usb_ctrl_t *const p_api_ctrl)
```

Request suspend

**Implemented as**

- R\_USB\_Suspend()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **resume**

```
fsp_err_t(* usb_api_t::resume) (usb_ctrl_t *const p_api_ctrl)
```

Request resume

**Implemented as**

- R\_USB\_Resume()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **vbusSet**

```
fsp_err_t(* usb_api_t::vbusSet) (usb_ctrl_t *const p_api_ctrl, uint16_t state)
```

Sets VBUS supply start/stop.

**Implemented as**

- R\_USB\_VbusSet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	state	VBUS supply start/stop specification

## ◆ infoGet

```
fsp_err_t(* usb_api_t::infoGet) (usb_ctrl_t *const p_api_ctrl, usb_info_t *p_info, uint8_t destination)
```

Get information on USB device.

**Implemented as**

- R\_USB\_InfoGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_info	Pointer to usb_info_t structure area.
[in]	destination	Device address for Host.

## ◆ pipeRead

```
fsp_err_t(* usb_api_t::pipeRead) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
```

Request data read from specified pipe

**Implemented as**

- R\_USB\_PipeRead()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores read data.
[in]	size	Read request size.
[in]	pipe_number	Pipe Number.

## ◆ pipeWrite

```
fsp_err_t(* usb_api_t::pipeWrite) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size, uint8_t pipe_number)
```

Request data write to specified pipe

**Implemented as**

- R\_USB\_PipeWrite()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_buf	Pointer to area that stores write data.
[in]	size	Read request size.
[in]	pipe_number	Pipe Number.

## ◆ pipeStop

```
fsp_err_t(* usb_api_t::pipeStop) (usb_ctrl_t *const p_api_ctrl, uint8_t pipe_number)
```

Stop USB data read/write processing to specified pipe

**Implemented as**

- R\_USB\_PipeStop()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	pipe_number	Pipe Number.

## ◆ usedPipesGet

```
fsp_err_t(* usb_api_t::usedPipesGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *p_pipe, uint8_t destination)
```

Get pipe number

**Implemented as**

- R\_USB\_UsedPipesGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_pipe	Pointer to area that stores the selected pipe number (bit map information).
[in]	destination	Device address for Host.

◆ **pipeInfoGet**

```
fsp_err_t(* usb_api_t::pipeInfoGet) (usb_ctrl_t *const p_api_ctrl, usb_pipe_t *p_info, uint8_t pipe_number)
```

Get pipe information

**Implemented as**

- [R\\_USB\\_PipeInfoGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_info	Pointer to usb_pipe_t structure area.
[in]	pipe_number	Pipe Number.

◆ **eventGet**

```
fsp_err_t(* usb_api_t::eventGet) (usb_ctrl_t *const p_api_ctrl, usb_status_t *event)
```

Return USB-related completed events (OS less only)

**Implemented as**

- [R\\_USB\\_EventGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[out]	event	Pointer to event.

◆ **callback**

```
fsp_err_t(* usb_api_t::callback) (usb_callback_t *p_callback)
```

Register a callback function to be called upon completion of a USB related event. (RTOS only)

**Implemented as**

- [R\\_USB\\_Callback\(\)](#)

**Parameters**

[in]	p_callback	Pointer to Callback function.
------	------------	-------------------------------

## ◆ pullUp

```
fsp_err_t(* usb_api_t::pullUp) (usb_ctrl_t *const p_api_ctrl, uint8_t state)
```

Pull-up enable/disable setting of D+/D- line.

**Implemented as**

- R\_USB\_PullUp()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	state	Pull-up enable/disable setting.

## ◆ hostControlTransfer

```
fsp_err_t(* usb_api_t::hostControlTransfer) (usb_ctrl_t *const p_api_ctrl, usb_setup_t *p_setup, uint8_t *p_buf, uint8_t device_address)
```

Performs settings and transmission processing when transmitting a setup packet.

**Implemented as**

- R\_USB\_HostControlTransfer()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_setup	Setup packet information.
[in]	p_buf	Transfer area information.
[in]	device_address	Device address information.

## ◆ periControlDataGet

```
fsp_err_t(* usb_api_t::periControlDataGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)
```

Receives data sent by control transfer.

**Implemented as**

- R\_USB\_PeriControlDataGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_buf	Data reception area information.
[in]	size	Data reception size information.

◆ **periControlDataSet**

```
fsp_err_t(* usb_api_t::periControlDataSet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_buf, uint32_t size)
```

Performs transfer processing for control transfer.

**Implemented as**

- [R\\_USB\\_PeriControlDataSet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	p_buf	Area information for data transfer.
[in]	size	Transfer size information.

◆ **periControlStatusSet**

```
fsp_err_t(* usb_api_t::periControlStatusSet) (usb_ctrl_t *const p_api_ctrl, usb_setup_status_t status)
```

Set the response to the setup packet.

**Implemented as**

- [R\\_USB\\_PeriControlStatusSet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[in]	status	USB port startup information.

◆ **remoteWakeup**

```
fsp_err_t(* usb_api_t::remoteWakeup) (usb_ctrl_t *const p_api_ctrl)
```

Sends a remote wake-up signal to the connected Host.

**Implemented as**

- [R\\_USB\\_RemoteWakeup\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
------	------------	------------------------

◆ **moduleNumberGet**

```
fsp_err_t(* usb_api_t::moduleNumberGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *module_number)
```

This API gets the module number.

**Implemented as**

- [R\\_USB\\_ModuleNumberGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	module_number	Module number to get.

◆ **classTypeGet**

```
fsp_err_t(* usb_api_t::classTypeGet) (usb_ctrl_t *const p_api_ctrl, usb_class_t *class_type)
```

This API gets the module number.

**Implemented as**

- [R\\_USB\\_ClassTypeGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	class_type	Class type to get.

◆ **deviceAddressGet**

```
fsp_err_t(* usb_api_t::deviceAddressGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *device_address)
```

This API gets the device address.

**Implemented as**

- [R\\_USB\\_DeviceAddressGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	device_address	Device address to get.

◆ **pipeNumberGet**

```
fsp_err_t(* usb_api_t::pipeNumberGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *pipe_number)
```

This API gets the pipe number.

**Implemented as**

- [R\\_USB\\_PipeNumberGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	pipe_number	Pipe number to get.

◆ **deviceStateGet**

```
fsp_err_t(* usb_api_t::deviceStateGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *state)
```

This API gets the state of the device.

**Implemented as**

- [R\\_USB\\_DeviceStateGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	state	Device state to get.

◆ **dataSizeGet**

```
fsp_err_t(* usb_api_t::dataSizeGet) (usb_ctrl_t *const p_api_ctrl, uint32_t *data_size)
```

This API gets the data size.

**Implemented as**

- [R\\_USB\\_DataSizeGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	data_size	Data size to get.

◆ **setupGet**

```
fsp_err_t(* usb_api_t::setupGet) (usb_ctrl_t *const p_api_ctrl, usb_setup_t *setup)
```

This API gets the setup type.

**Implemented as**

- R\_USB\_SetupGet()

**Parameters**

[in]	p_api_ctrl	USB control structure.
[out]	setup	Setup type to get.

◆ **usb\_instance\_t**

```
struct usb_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

usb_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
usb_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
usb_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **usb\_ctrl\_t**

```
typedef void usb_ctrl_t
```

USB control block. Allocate an instance specific control block to pass into the USB API calls.

**Implemented as**

- usb\_instance\_ctrl\_t

**Enumeration Type Documentation**

◆ **usb\_speed\_t**

enum <code>usb_speed_t</code>	
USB speed type	
Enumerator	
<code>USB_SPEED_LS</code>	Low speed operation.
<code>USB_SPEED_FS</code>	Full speed operation.
<code>USB_SPEED_HS</code>	Hi speed operation.

◆ **usb\_setup\_status\_t**

enum <code>usb_setup_status_t</code>	
USB request result	
Enumerator	
<code>USB_SETUP_STATUS_ACK</code>	ACK response.
<code>USB_SETUP_STATUS_STALL</code>	STALL response.

◆ **usb\_status\_t**

enum <code>usb_status_t</code>	
USB driver status	
Enumerator	
<code>USB_STATUS_POWERED</code>	Powered State.
<code>USB_STATUS_DEFAULT</code>	Default State.
<code>USB_STATUS_ADDRESS</code>	Address State.
<code>USB_STATUS_CONFIGURED</code>	Configured State.
<code>USB_STATUS_SUSPEND</code>	Suspend State.
<code>USB_STATUS_RESUME</code>	Resume State.
<code>USB_STATUS_DETACH</code>	Detach State.
<code>USB_STATUS_REQUEST</code>	Request State.
<code>USB_STATUS_REQUEST_COMPLETE</code>	Request Complete State.
<code>USB_STATUS_READ_COMPLETE</code>	Read Complete State.
<code>USB_STATUS_WRITE_COMPLETE</code>	Write Complete State.
<code>USB_STATUS_BC</code>	battery Charge State
<code>USB_STATUS_OVERCURRENT</code>	Over Current state.
<code>USB_STATUS_NOT_SUPPORT</code>	Device Not Support.
<code>USB_STATUS_NONE</code>	None Status.
<code>USB_STATUS_MSC_CMD_COMPLETE</code>	MSC_CMD Complete.

◆ **usb\_class\_t**

enum <code>usb_class_t</code>	
USB class type	
Enumerator	
<code>USB_CLASS_PCDC</code>	PCDC Class.
<code>USB_CLASS_PCDCC</code>	PCDCC Class.
<code>USB_CLASS_PCDC2</code>	PCDC2 Class.
<code>USB_CLASS_PCDCC2</code>	PCDCC2 Class.
<code>USB_CLASS_PHID</code>	PHID Class.
<code>USB_CLASS_PVND</code>	PVND Class.
<code>USB_CLASS_HCDC</code>	HCDC Class.
<code>USB_CLASS_HCDCC</code>	HCDCC Class.
<code>USB_CLASS_HHID</code>	HHID Class.
<code>USB_CLASS_HVND</code>	HVND Class.
<code>USB_CLASS_HMSC</code>	HMSC Class.
<code>USB_CLASS_PMSC</code>	PMSC Class.
<code>USB_CLASS_REQUEST</code>	USB Class Request.
<code>USB_CLASS_END</code>	USB Class End Code.

◆ **usb\_bcport\_t**

enum <a href="#">usb_bcport_t</a>	
USB battery charging type	
Enumerator	
USB_BCPORT_SDP	SDP port settings.
USB_BCPORT_CDP	CDP port settings.
USB_BCPORT_DCP	DCP port settings.

◆ **usb\_onoff\_t**

enum <a href="#">usb_onoff_t</a>	
USB status	
Enumerator	
USB_OFF	USB Off State.
USB_ON	USB On State.

◆ **usb\_transfer\_t**

enum <a href="#">usb_transfer_t</a>	
USB read/write type	
Enumerator	
USB_TRANSFER_READ	Data Receive communication.
USB_TRANSFER_WRITE	Data transmission communication.

◆ **usb\_transfer\_type\_t**

enum <code>usb_transfer_type_t</code>	
USB transfer type	
Enumerator	
<code>USB_TRANSFER_TYPE_BULK</code>	Bulk communication.
<code>USB_TRANSFER_TYPE_INT</code>	Interrupt communication.
<code>USB_TRANSFER_TYPE_ISO</code>	Isochronous communication.

◆ **usb\_mode\_t**

enum <code>usb_mode_t</code>	
Enumerator	
<code>USB_MODE_HOST</code>	Host mode.
<code>USB_MODE_PERI</code>	Peripheral mode.

◆ **usb\_compliancetest\_status\_t**

enum <code>usb_compliancetest_status_t</code>	
Enumerator	
<code>USB_COMPLIANCETEST_ATTACH</code>	Device Attach Detection.
<code>USB_COMPLIANCETEST_DETACH</code>	Device Detach Detection.
<code>USB_COMPLIANCETEST_TPL</code>	TPL device connect.
<code>USB_COMPLIANCETEST_NOTTPL</code>	Not TPL device connect.
<code>USB_COMPLIANCETEST_HUB</code>	USB Hub connect.
<code>USB_COMPLIANCETEST_OVRC</code>	Over current.
<code>USB_COMPLIANCETEST_NORES</code>	Response Time out for Control Read Transfer.
<code>USB_COMPLIANCETEST_SETUP_ERR</code>	Setup Transaction Error.

## 4.3.40 USB HCDC Interface

### Interfaces

#### Detailed Description

Interface for USB HCDC functions.

## Summary

The USB HCDC interface provides USB HCDC functionality.

The USB HCDC interface can be implemented by:

- [USB Host Communications Device Class Driver \(r\\_usb\\_hcdc\)](#)

#### Data Structures

struct [usb\\_hcdc\\_encapsulated\\_t](#)

struct [usb\\_hcdc\\_abstractstate\\_t](#)

struct [usb\\_hcdc\\_countrysetting\\_t](#)

union [usb\\_hcdc\\_commfeature\\_t](#)

struct [usb\\_hcdc\\_linecoding\\_t](#)

struct [usb\\_hcdc\\_controllinestate\\_t](#)

struct [usb\\_hcdc\\_serialstate\\_t](#)

struct [usb\\_hcdc\\_breakduration\\_t](#)

#### Enumerations

enum [usb\\_hcdc\\_data\\_bit\\_t](#)

enum [usb\\_hcdc\\_stop\\_bit\\_t](#)

enum [usb\\_hcdc\\_parity\\_bit\\_t](#)

enum [usb\\_hcdc\\_line\\_speed\\_t](#)

enum [usb\\_hcdc\\_feature\\_selector\\_t](#)

#### Data Structure Documentation

◆ **usb\_hcdc\_encapsulated\_t**

struct usb_hcdc_encapsulated_t		
Encapsulated data		
Data Fields		
uint8_t *	p_data	Protocol dependent data.
uint16_t	wlength	Data length in bytes.

◆ **usb\_hcdc\_abstractstate\_t**

struct usb_hcdc_abstractstate_t		
Abstract Control Model (ACM) settings bitmap		
Data Fields		
uint16_t	bis: 1	Idle enable.
uint16_t	bdms: 1	Data multiplexing enable.
uint16_t	rsv: 14	Reserved.

◆ **usb\_hcdc\_countrysetting\_t**

struct usb_hcdc_countrysetting_t		
Country code data		
Data Fields		
uint16_t	country_code	Country code.

◆ **usb\_hcdc\_commfeature\_t**

union usb_hcdc_commfeature_t		
Feature setting data		
Data Fields		
<a href="#">usb_hcdc_abstractstate_t</a>	abstract_state	ACM settings bitmap.
<a href="#">usb_hcdc_countrysetting_t</a>	country_setting	Country code.

◆ **usb\_hcdc\_linecoding\_t**

struct usb_hcdc_linecoding_t		
Virtual UART configuration (line coding)		
Data Fields		
<a href="#">usb_hcdc_line_speed_t</a>	dwkte_rate	Data terminal rate in bits per second.
<a href="#">usb_hcdc_stop_bit_t</a>	bchar_format	Stop bits.
<a href="#">usb_hcdc_parity_bit_t</a>	bparity_type	Parity.
<a href="#">usb_hcdc_data_bit_t</a>	bdata_bits	Data bits.

uint8_t	rsv	Reserved.
---------	-----	-----------

#### ◆ usb\_hcdc\_controllinestate\_t

struct usb_hcdc_controllinestate_t		
Virtual UART control signal bitmap		
Data Fields		
uint16_t	bdtr: 1	DTR.
uint16_t	brts: 1	RTS.
uint16_t	rsv: 14	Reserved.

#### ◆ usb\_hcdc\_serialstate\_t

struct usb_hcdc_serialstate_t		
Virtual UART state bitmap		
Data Fields		
uint16_t	brx_carrier: 1	DCD signal.
uint16_t	btx_carrier: 1	DSR signal.
uint16_t	bbreak: 1	Break detection status.
uint16_t	bring_signal: 1	Ring signal.
uint16_t	bframing: 1	Framing error.
uint16_t	bparity: 1	Parity error.
uint16_t	bover_run: 1	Over Run error.
uint16_t	rsv: 9	Reserved.

#### ◆ usb\_hcdc\_breakduration\_t

struct usb_hcdc_breakduration_t		
Break duration data		
Data Fields		
uint16_t	wtime_ms	Duration of Break.

## Enumeration Type Documentation

◆ **usb\_hcdc\_data\_bit\_t**

enum <a href="#">usb_hcdc_data_bit_t</a>	
Virtual UART data length	
Enumerator	
USB_HCDC_DATA_BIT_7	7 bits
USB_HCDC_DATA_BIT_8	8 bits

◆ **usb\_hcdc\_stop\_bit\_t**

enum <a href="#">usb_hcdc_stop_bit_t</a>	
Virtual UART stop bit length	
Enumerator	
USB_HCDC_STOP_BIT_1	1 bit
USB_HCDC_STOP_BIT_15	1.5 bits
USB_HCDC_STOP_BIT_2	2 bits

◆ **usb\_hcdc\_parity\_bit\_t**

enum <a href="#">usb_hcdc_parity_bit_t</a>	
Virtual UART parity bit setting	
Enumerator	
USB_HCDC_PARITY_BIT_NONE	No parity bit.
USB_HCDC_PARITY_BIT_ODD	Odd parity.
USB_HCDC_PARITY_BIT_EVEN	Even parity.

◆ **usb\_hcdc\_line\_speed\_t**

enum <a href="#">usb_hcdc_line_speed_t</a>	
Virtual UART bitrate	

### ◆ usb\_hcdc\_feature\_selector\_t

```
enum usb_hcdc_feature_selector_t
```

```
Feature Selector
```

## 4.3.41 USB HHID Interface

### Interfaces

#### Detailed Description

Interface for USB HHID functions.

## Summary

The USB HHID interface provides USB HHID functionality.

The USB HHID interface can be implemented by:

- USB Host Human Interface Device Class Driver (r\_usb\_hhid)

#### Data Structures

```
struct usb_hhid_api_t
```

```
struct usb_hhid_instance_t
```

#### Macros

```
#define USB_HID_OTHER  
Other.
```

```
#define USB_HID_KEYBOARD  
Keyboard.
```

```
#define USB_HID_MOUSE  
Mouse.
```

```
#define USB_HID_IN  
In Transfer.
```

```
#define USB_HID_OUT
Out Transfer.
```

## Data Structure Documentation

### ◆ usb\_hhid\_api\_t

struct usb\_hhid\_api\_t

USB HHID functions implemented at the HAL layer will follow this API.

#### Data Fields

fsp_err_t(*)	typeGet )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_type, uint8_t device_address)
--------------	--

fsp_err_t(*)	maxPacketSizeGet )(usb_ctrl_t *const p_api_ctrl, uint16_t *p_size, uint8_t direction, uint8_t device_address)
--------------	---

## Field Documentation

### ◆ typeGet

fsp\_err\_t(\* usb\_hhid\_api\_t::typeGet) (usb\_ctrl\_t \*const p\_api\_ctrl, uint8\_t \*p\_type, uint8\_t device\_address)

Get HID protocol.(USB Mouse/USB Keyboard/Other Type.)

#### Implemented as

- R\_USB\_HHID\_TypeGet()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_type	Pointer to store HID protocol value.
[in]	device_address	Device Address.

◆ **maxPacketSizeGet**

```
fsp_err_t(* usb_hhid_api_t::maxPacketSizeGet) (usb_ctrl_t *const p_api_ctrl, uint16_t *p_size,
uint8_t direction, uint8_t device_address)
```

Obtains max packet size for the connected HID device. The max packet size is set to the area. Set the direction (USB\_HID\_IN/USB\_HID\_OUT).

**Implemented as**

- [R\\_USB\\_HHID\\_MaxPacketSizeGet\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_size	Pointer to the area to store the max package size.
[in]	direction	Transfer direction.
[in]	device_address	Device Address.

◆ **usb\_hhid\_instance\_t**

```
struct usb_hhid_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

usb_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
usb_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
usb_hhid_api_t const *	p_api	Pointer to the API structure for this instance.

**4.3.42 USB HMSC Interface**[Interfaces](#)**Detailed Description**

Interface for USB HMSC functions.

**Summary**

The USB HMSC interface provides USB HMSC functionality.

The USB HMSC interface can be implemented by:

- [USB Host Mass Storage Class Driver \(r\\_usb\\_hmsc\)](#)

## Data Structures

struct [usb\\_hmsc\\_api\\_t](#)

## Enumerations

enum [usb\\_atapi\\_t](#)

enum [usb\\_csw\\_result\\_t](#)

## Data Structure Documentation

### ◆ [usb\\_hmsc\\_api\\_t](#)

struct [usb\\_hmsc\\_api\\_t](#)

USB HMSC functions implemented at the HAL layer will follow this API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">storageCommand</a> )(usb_ctrl_t *const p_api_ctrl, uint8_t *buf, uint8_t command, uint8_t destination)
------------------------------	--

<a href="#">fsp_err_t</a> (*	<a href="#">driveNumberGet</a> )(usb_ctrl_t *const p_api_ctrl, uint8_t *p_drive, uint8_t destination)
------------------------------	---

<a href="#">fsp_err_t</a> (*	<a href="#">storageReadSector</a> )(uint16_t drive_number, uint8_t *const buff, uint32_t sector_number, uint16_t sector_count)
------------------------------	--

<a href="#">fsp_err_t</a> (*	<a href="#">storageWriteSector</a> )(uint16_t drive_number, uint8_t const *const buff, uint32_t sector_number, uint16_t sector_count)
------------------------------	---

<a href="#">fsp_err_t</a> (*	<a href="#">semaphoreGet</a> )(void)
------------------------------	--------------------------------------

<a href="#">fsp_err_t</a> (*	<a href="#">semaphoreRelease</a> )(void)
------------------------------	--

## Field Documentation

◆ **storageCommand**

```
fsp_err_t(* usb_hmsc_api_t::storageCommand) (usb_ctrl_t *const p_api_ctrl, uint8_t *buf, uint8_t command, uint8_t destination)
```

Processing for MassStorage(ATAPI) command.

**Implemented as**

- R\_USB\_HMSC\_StorageCommand()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	*buf	Pointer to the buffer area to store the transfer data.
[in]	command	ATAPI command.
[in]	destination	Represents a device address.

◆ **driveNumberGet**

```
fsp_err_t(* usb_hmsc_api_t::driveNumberGet) (usb_ctrl_t *const p_api_ctrl, uint8_t *p_drive, uint8_t destination)
```

Get number of Storage drive.

**Implemented as**

- R\_USB\_HMSC\_DriveNumberGet()

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[out]	p_drive	Store address for Drive No.
[in]	destination	Represents a device address.

### ◆ storageReadSector

`fsp_err_t(*usb_hmsc_api_t::storageReadSector)(uint16_t drive_number, uint8_t *const buff, uint32_t sector_number, uint16_t sector_count)`

Read sector information.

#### Implemented as

- [R\\_USB\\_HMSC\\_StorageReadSector\(\)](#)

#### Parameters

[in]	drive_number	Drive number.
[out]	*buff	Pointer to the buffer area to store the transfer data.
[in]	sector_number	The sector number to start with.
[in]	sector_count	Transmit with the sector size of the number of times.

### ◆ storageWriteSector

`fsp_err_t(*usb_hmsc_api_t::storageWriteSector)(uint16_t drive_number, uint8_t const *const buff, uint32_t sector_number, uint16_t sector_count)`

Write sector information.

#### Implemented as

- [R\\_USB\\_HMSC\\_StorageWriteSector\(\)](#)

#### Parameters

[in]	drive_number	Drive number.
[in]	*buff	Pointer to the buffer area to store the transfer data.
[in]	sector_number	The sector number to start with.
[in]	sector_count	Transmit with the sector size of the number of times.

### ◆ semaphoreGet

`fsp_err_t(*usb_hmsc_api_t::semaphoreGet)(void)`

Get Semaphore.

#### Implemented as

- [R\\_USB\\_HMSC\\_SemaphoreGet\(\)](#)

**◆ semaphoreRelease**`fsp_err_t(* usb_hmsc_api_t::semaphoreRelease) (void)`

Release Semaphore.

**Implemented as**

- `R_USB_HMSC_SemaphoreRelease()`

**Enumeration Type Documentation**

◆ **usb\_atapi\_t**

enum <code>usb_atapi_t</code>	
ATAPI commands	
Enumerator	
<code>USB_ATAPI_TEST_UNIT_READY</code>	Test Unit Ready.
<code>USB_ATAPI_REQUEST_SENSE</code>	Request Sense.
<code>USB_ATAPI_FORMAT_UNIT</code>	Format Unit.
<code>USB_ATAPI_INQUIRY</code>	Inquiry.
<code>USB_ATAPI_MODE_SELECT6</code>	Mode Select6.
<code>USB_ATAPI_MODE_SENSE6</code>	Mode Sense6.
<code>USB_ATAPI_START_STOP_UNIT</code>	Start Stop Unit.
<code>USB_ATAPI_PREVENT_ALLOW</code>	Prevent Allow.
<code>USB_ATAPI_READ_FORMAT_CAPACITY</code>	Read Format Capacity.
<code>USB_ATAPI_READ_CAPACITY</code>	Read Capacity.
<code>USB_ATAPI_READ10</code>	Read10.
<code>USB_ATAPI_WRITE10</code>	Write10.
<code>USB_ATAPI_SEEK</code>	Seek.
<code>USB_ATAPI_WRITE_AND_VERIFY</code>	Write and Verify.
<code>USB_ATAPI_VERIFY10</code>	Verify10.
<code>USB_ATAPI_MODE_SELECT10</code>	Mode Select10.
<code>USB_ATAPI_MODE_SENSE10</code>	Mode Sense10.

◆ **usb\_csw\_result\_t**

enum usb_csw_result_t	
Command Status Wrapper (CSW)	
Enumerator	
USB_CSW_RESULT_SUCCESS	CSW was successful.
USB_CSW_RESULT_FAIL	CSW failed.
USB_CSW_RESULT_PHASE	CSW has phase error.

**4.3.43 USB PCDC Interface**[Interfaces](#)**Detailed Description**

Interface for USB PCDC functions.

**Summary**

The USB PCDC interface provides USB PCDC functionality.

The USB PCDC interface can be implemented by:

- [USB Peripheral Communications Device Class \(r\\_usb\\_pcdc\)](#)

**Data Structures**

```
struct usb_serial_state_bitmap_t
```

```
union usb_sci_serialstate_t
```

```
struct usb_pcdc_linecoding_t
```

```
struct usb_pcdc_ctrllinestate_t
```

**Macros**

```
#define USB_PCDC_SET_LINE_CODING
Set Line Coding.
```

```
#define USB_PCDC_GET_LINE_CODING
```

Get Line Coding.

```
#define USB_PCDC_SET_CONTROL_LINE_STATE
```

Control Line State.

```
#define USB_PCDC_SERIAL_STATE
```

Serial State Code.

```
#define USB_PCDC_SETUP_TBL_BSIZE
```

Setup packet table size (uint16\_t \* 5)

## Data Structure Documentation

### ◆ usb\_serial\_state\_bitmap\_t

struct usb_serial_state_bitmap_t		
Virtual UART signal state		
Data Fields		
uint16_t	b_rx_carrier: 1	DCD signal.
uint16_t	b_tx_carrier: 1	DSR signal.
uint16_t	b_break: 1	Break signal.
uint16_t	b_ring_signal: 1	Ring signal.
uint16_t	b_framing: 1	Framing error.
uint16_t	b_parity: 1	Parity error.
uint16_t	b_over_run: 1	Overrun error.
uint16_t	rsv: 9	Reserved.

### ◆ usb\_sci\_serialstate\_t

union usb_sci_serialstate_t		
Class Notification Serial State		
Data Fields		
uint32_t	word	Word Access.
<a href="#">usb_serial_state_bitmap_t</a>	bit	Bit Access.

### ◆ usb\_pcdc\_linecoding\_t

struct usb_pcdc_linecoding_t		

Virtual UART communication settings		
Data Fields		
uint32_t	dw_dte_rate	Bitrate.
uint8_t	b_char_format	Stop bits.
uint8_t	b_parity_type	Parity.
uint8_t	b_data_bits	Data bits.
uint8_t	rsv	Reserved.

#### ◆ usb\_pcdc\_ctrllinestate\_t

struct usb_pcdc_ctrllinestate_t		
Virtual UART control line state		
Data Fields		
uint16_t	bdtr: 1	DTR.
uint16_t	brts: 1	RTS.
uint16_t	rsv: 14	Reserved.

### 4.3.44 USB PHID Interface

#### Interfaces

#### Detailed Description

Interface for USB PHID functions.

### Summary

The USB interface provides USB functionality.

The USB PHID interface can be implemented by:

- [USB Peripheral Human Interface Device Class \(r\\_usb\\_phid\)](#)

### 4.3.45 USB PMSC Interface

#### Interfaces

#### Detailed Description

Interface for USB PMSC functions.

## Summary

The USB PMSC interface provides USB PMSC functionality.

The USB PMSC interface can be implemented by:

- [USB Peripheral Mass Storage Class \(r\\_usb\\_pmsc\)](#)

### Macros

```
#define USB_MASS_STORAGE_RESET
    Mass storage reset request code.
```

```
#define USB_GET_MAX_LUN
    Get max logical unit number request code.
```

## 4.3.46 WDT Interface

[Interfaces](#)

### Detailed Description

Interface for watch dog timer functions.

## Summary

The WDT interface for the Watchdog Timer (WDT) peripheral provides watchdog functionality including resetting the device or generating an interrupt.

The watchdog timer interface can be implemented by:

- [Watchdog Timer \(r\\_wdt\)](#)
- [Independent Watchdog Timer \(r\\_iwdt\)](#)

### Data Structures

```
struct wdt_callback_args_t
```

```
struct wdt_timeout_values_t
```

```
struct wdt_cfg_t
```

```
struct wdt_api_t
```

```
struct wdt_instance_t
```

## Typedefs

```
typedef void wdt_ctrl_t
```

## Enumerations

```
enum wdt_timeout_t
```

```
enum wdt_clock_division_t
```

```
enum wdt_window_start_t
```

```
enum wdt_window_end_t
```

```
enum wdt_reset_control_t
```

```
enum wdt_stop_control_t
```

```
enum wdt_status_t
```

## Data Structure Documentation

### ◆ wdt\_callback\_args\_t

struct wdt_callback_args_t		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data. Set in <a href="#">wdt_api_t::open</a> function in <a href="#">wdt_cfg_t</a> .

### ◆ wdt\_timeout\_values\_t

struct wdt_timeout_values_t		
WDT timeout data. Used to return frequency of WDT clock and timeout period		
Data Fields		
uint32_t	clock_frequency_hz	Frequency of watchdog clock after divider.
uint32_t	timeout_ticks	Timeout period in units of watchdog clock ticks.

### ◆ wdt\_cfg\_t

struct wdt_cfg_t		
WDT configuration parameters.		

Data Fields	
<code>wdt_timeout_t</code>	<code>timeout</code>
	Timeout period.
<code>wdt_clock_division_t</code>	<code>clock_division</code>
	Clock divider.
<code>wdt_window_start_t</code>	<code>window_start</code>
	Refresh permitted window start position.
<code>wdt_window_end_t</code>	<code>window_end</code>
	Refresh permitted window end position.
<code>wdt_reset_control_t</code>	<code>reset_control</code>
	Select NMI or reset generated on underflow.
<code>wdt_stop_control_t</code>	<code>stop_control</code>
	Select whether counter operates in sleep mode.
<code>void(*</code>	<code>p_callback</code> )( <code>wdt_callback_args_t</code> * <code>p_args</code> )
	Callback provided when a WDT NMI ISR occurs.
<code>void const *</code>	<code>p_context</code>
<code>void const *</code>	<code>p_extend</code>
	Placeholder for user extension.
Field Documentation	

◆ **p\_context**

```
void const* wdt_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in [wdt\\_callback\\_args\\_t](#).

◆ **wdt\_api\_t**

```
struct wdt_api_t
```

WDT functions implemented at the HAL layer will follow this API.

**Data Fields**

fsp_err_t(*)	<a href="#">open</a> )(wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg)
--------------	--

fsp_err_t(*)	<a href="#">refresh</a> )(wdt_ctrl_t *const p_ctrl)
--------------	---

fsp_err_t(*)	<a href="#">statusGet</a> )(wdt_ctrl_t *const p_ctrl, wdt_status_t *const p_status)
--------------	---

fsp_err_t(*)	<a href="#">statusClear</a> )(wdt_ctrl_t *const p_ctrl, const wdt_status_t status)
--------------	--

fsp_err_t(*)	<a href="#">counterGet</a> )(wdt_ctrl_t *const p_ctrl, uint32_t *const p_count)
--------------	---

fsp_err_t(*)	<a href="#">timeoutGet</a> )(wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout)
--------------	---

fsp_err_t(*)	<a href="#">callbackSet</a> )(wdt_ctrl_t *const p_api_ctrl, void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const p_callback_memory)
--------------	--

**Field Documentation**

◆ **open**

```
fsp_err_t(* wdt_api_t::open) (wdt_ctrl_t *const p_ctrl, wdt_cfg_t const *const p_cfg)
```

Initialize the WDT in register start mode. In auto-start mode with NMI output it registers the NMI callback.

**Implemented as**

- R\_WDT\_Open()
- R\_IWDT\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **refresh**

```
fsp_err_t(* wdt_api_t::refresh) (wdt_ctrl_t *const p_ctrl)
```

Refresh the watchdog timer.

**Implemented as**

- R\_WDT\_Refresh()
- R\_IWDT\_Refresh()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **statusGet**

```
fsp_err_t(* wdt_api_t::statusGet) (wdt_ctrl_t *const p_ctrl, wdt_status_t *const p_status)
```

Read the status of the WDT.

**Implemented as**

- R\_WDT\_StatusGet()
- R\_IWDT\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_status	Pointer to variable to return status information through.

◆ **statusClear**

```
fsp_err_t(* wdt_api_t::statusClear) (wdt_ctrl_t *const p_ctrl, const wdt_status_t status)
```

Clear the status flags of the WDT.

**Implemented as**

- R\_WDT\_StatusClear()
- R\_IWDT\_StatusClear()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	status	Status condition(s) to clear.

◆ **counterGet**

```
fsp_err_t(* wdt_api_t::counterGet) (wdt_ctrl_t *const p_ctrl, uint32_t *const p_count)
```

Read the current WDT counter value.

**Implemented as**

- R\_WDT\_CounterGet()
- R\_IWDT\_CounterGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_count	Pointer to variable to return current WDT counter value.

◆ **timeoutGet**

```
fsp_err_t(* wdt_api_t::timeoutGet) (wdt_ctrl_t *const p_ctrl, wdt_timeout_values_t *const p_timeout)
```

Read the watchdog timeout values.

**Implemented as**

- R\_WDT\_TimeoutGet()
- R\_IWDT\_TimeoutGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_timeout	Pointer to structure to return timeout values.

◆ **callbackSet**

```
fsp_err_t(* wdt_api_t::callbackSet) (wdt_ctrl_t *const p_api_ctrl,
void(*p_callback)(wdt_callback_args_t *), void const *const p_context, wdt_callback_args_t *const
p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [R\\_WDT\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the WDT control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **wdt\_instance\_t**

```
struct wdt_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">wdt_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">wdt_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">wdt_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **wdt\_ctrl\_t**

```
typedef void wdt_ctrl_t
```

WDT control block. Allocate an instance specific control block to pass into the WDT API calls.

**Implemented as**

- [wdt\\_instance\\_ctrl\\_t](#)
- [iwdt\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ wdt\_timeout\_t

enum wdt_timeout_t	
WDT time-out periods.	
Enumerator	
WDT_TIMEOUT_128	128 clock cycles
WDT_TIMEOUT_512	512 clock cycles
WDT_TIMEOUT_1024	1024 clock cycles
WDT_TIMEOUT_2048	2048 clock cycles
WDT_TIMEOUT_4096	4096 clock cycles
WDT_TIMEOUT_8192	8192 clock cycles
WDT_TIMEOUT_16384	16384 clock cycles

◆ **wdt\_clock\_division\_t**

enum <code>wdt_clock_division_t</code>	
WDT clock division ratio.	
Enumerator	
<code>WDT_CLOCK_DIVISION_1</code>	CLK/1.
<code>WDT_CLOCK_DIVISION_4</code>	CLK/4.
<code>WDT_CLOCK_DIVISION_16</code>	CLK/16.
<code>WDT_CLOCK_DIVISION_32</code>	CLK/32.
<code>WDT_CLOCK_DIVISION_64</code>	CLK/64.
<code>WDT_CLOCK_DIVISION_128</code>	CLK/128.
<code>WDT_CLOCK_DIVISION_256</code>	CLK/256.
<code>WDT_CLOCK_DIVISION_512</code>	CLK/512.
<code>WDT_CLOCK_DIVISION_2048</code>	CLK/2048.
<code>WDT_CLOCK_DIVISION_8192</code>	CLK/8192.

◆ **wdt\_window\_start\_t**

enum <code>wdt_window_start_t</code>	
WDT refresh permitted period window start position.	
Enumerator	
<code>WDT_WINDOW_START_25</code>	Start position = 25%.
<code>WDT_WINDOW_START_50</code>	Start position = 50%.
<code>WDT_WINDOW_START_75</code>	Start position = 75%.
<code>WDT_WINDOW_START_100</code>	Start position = 100%.

◆ **wdt\_window\_end\_t**

enum <a href="#">wdt_window_end_t</a>	
WDT refresh permitted period window end position.	
Enumerator	
WDT_WINDOW_END_75	End position = 75%.
WDT_WINDOW_END_50	End position = 50%.
WDT_WINDOW_END_25	End position = 25%.
WDT_WINDOW_END_0	End position = 0%.

◆ **wdt\_reset\_control\_t**

enum <a href="#">wdt_reset_control_t</a>	
WDT Counter underflow and refresh error control.	
Enumerator	
WDT_RESET_CONTROL_NMI	NMI request when counter underflows.
WDT_RESET_CONTROL_RESET	Reset request when counter underflows.

◆ **wdt\_stop\_control\_t**

enum <a href="#">wdt_stop_control_t</a>	
WDT Counter operation in sleep mode.	
Enumerator	
WDT_STOP_CONTROL_DISABLE	Count will not stop when device enters sleep mode.
WDT_STOP_CONTROL_ENABLE	Count will automatically stop when device enters sleep mode.

◆ **wdt\_status\_t**

enum <code>wdt_status_t</code>	
WDT status	
Enumerator	
<code>WDT_STATUS_NO_ERROR</code>	No status flags set.
<code>WDT_STATUS_UNDERFLOW_ERROR</code>	Underflow flag set.
<code>WDT_STATUS_REFRESH_ERROR</code>	Refresh error flag set. Refresh outside of permitted window.
<code>WDT_STATUS_UNDERFLOW_AND_REFRESH_ERROR</code>	Underflow and refresh error flags set.

**4.3.47 ADPCM Decoder Interface**[Interfaces](#)**Detailed Description**

Interface for ADPCM decoder.

**Summary**

The ADPCM decoder interface provides functionality to decode the 4bit ADPCM data to 16bit PCM output.

Implemented by: [ADPCM Decoder \(rm\\_adpcm\\_decoder\)](#)

**Data Structures**

struct [adpcm\\_decoder\\_cfg\\_t](#)

struct [adpcm\\_decoder\\_api\\_t](#)

struct [adpcm\\_decoder\\_instance\\_t](#)

**Typedefs**

typedef void [adpcm\\_decoder\\_ctrl\\_t](#)

**Data Structure Documentation**◆ **adpcm\_decoder\_cfg\_t**

```
struct adpcm_decoder_cfg_t
```

Audio Decoder general configuration

### ◆ adpcm\_decoder\_api\_t

```
struct adpcm_decoder_api_t
```

Audio Decoder interface API.

#### Data Fields

<code>fsp_err_t(*</code>	<code>open</code> )( <code>adpcm_decoder_ctrl_t *const p_ctrl, adpcm_decoder_cfg_t const *const p_cfg</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>decode</code> )( <code>adpcm_decoder_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t src_len_bytes</code> )
--------------------------	---

<code>fsp_err_t(*</code>	<code>reset</code> )( <code>adpcm_decoder_ctrl_t *const p_ctrl</code> )
--------------------------	---

<code>fsp_err_t(*</code>	<code>close</code> )( <code>adpcm_decoder_ctrl_t *const p_ctrl</code> )
--------------------------	---

#### Field Documentation

##### ◆ open

```
fsp_err_t(* adpcm_decoder_api_t::open) (adpcm_decoder_ctrl_t *const p_ctrl, adpcm_decoder_cfg_t const *const p_cfg)
```

Initialize Audio Decoder device.

#### Implemented as

- `RM_ADPCM_DECODER_Open()`

#### Note

To reconfigure after calling this function, call `adpcm_decoder_api_t::close` first.

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control handle structure
[in]	<code>p_cfg</code>	Pointer to configuration structure

◆ **decode**

```
fsp_err_t(* adpcm_decoder_api_t::decode) (adpcm_decoder_ctrl_t *const p_ctrl, void const *p_src, void *p_dest, uint32_t src_len_bytes)
```

Decodes the compressed data and stores it in output buffer.

**Implemented as**

- [RM\\_ADPCM\\_DECODER\\_Decode\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
[in]	p_src	Pointer to a source data buffer from which data will be picked up for decode operation. The argument must not be NULL.
[out]	p_dest	Pointer to the location to store the decoded data.
[in]	p_dest	Number of bytes to be decoded.

◆ **reset**

```
fsp_err_t(* adpcm_decoder_api_t::reset) (adpcm_decoder_ctrl_t *const p_ctrl)
```

Resets the ADPCM driver.

**Implemented as**

- [RM\\_ADPCM\\_DECODER\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **close**

```
fsp_err_t(* adpcm_decoder_api_t::close) (adpcm_decoder_ctrl_t *const p_ctrl)
```

Close the specified Audio decoder modules.

**Implemented as**

- [RM\\_ADPCM\\_DECODER\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control handle structure
------	--------	-------------------------------------

◆ **adpcm\_decoder\_instance\_t**

struct adpcm_decoder_instance_t		
This structure encompasses everything that is needed to use an instance of this interface.		
Data Fields		
adpcm_decoder_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
adpcm_decoder_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
adpcm_decoder_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **adpcm\_decoder\_ctrl\_t**

typedef void adpcm_decoder_ctrl_t
Audio Decoder control block. Allocate an instance specific control block to pass into the Audio Decoder API calls.
<b>Implemented as</b>
◦ <a href="#">adpcm_decoder_instance_ctrl_t</a>

**4.3.48 AUDIO PLAYBACK Interface**[Interfaces](#)**Detailed Description**

Interface for the Audio Playback.

Defines the API and data structures for the Audio Playback implementation.

**Summary**

This module provides common interface for Audio Playback.

Implemented by: [Audio Playback with PWM \(rm\\_audio\\_playback\\_pwm\)](#)

**Data Structures**

struct [audio\\_playback\\_callback\\_args\\_t](#)

struct [audio\\_playback\\_cfg\\_t](#)

```
struct audio_playback_api_t
```

```
struct audio_playback_instance_t
```

## Typedefs

```
typedef void audio_playback_ctrl_t
```

## Enumerations

```
enum audio_playback_event_t
```

## Data Structure Documentation

### ◆ audio\_playback\_callback\_args\_t

struct audio_playback_callback_args_t		
Callback function parameter data		
Data Fields		
void *	p_context	Placeholder for user data.
audio_playback_event_t	event	Event that triggered the callback.

### ◆ audio\_playback\_cfg\_t

struct audio_playback_cfg_t		
Audio Playback configuration parameters.		
<b>Data Fields</b>		
void const *	p_extend	Hardware dependent configuration.
void(*	p_callback	(audio_playback_callback_args_t *p_args)
void *	p_context	

## Field Documentation

### ◆ p\_callback

```
void(* audio_playback_cfg_t::p_callback) (audio_playback_callback_args_t *p_args)
```

Callback called when play is complete.

◆ **p\_context**

```
void* audio_playback_cfg_t::p_context
```

Placeholder for user data. Passed to the user callback in [audio\\_playback\\_callback\\_args\\_t](#).

◆ **audio\_playback\_api\_t**

```
struct audio_playback_api_t
```

Audio Playback functions implemented by the Audio Playback drivers will follow this API.

**Data Fields**

<code>fsp_err_t(*</code>	<code>open</code> )( <code>audio_playback_ctrl_t *const p_ctrl, audio_playback_cfg_t const *const p_cfg</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>start</code> )( <code>audio_playback_ctrl_t *const p_ctrl</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>stop</code> )( <code>audio_playback_ctrl_t *const p_ctrl</code> )
--------------------------	---

<code>fsp_err_t(*</code>	<code>play</code> )( <code>audio_playback_ctrl_t *const p_ctrl, void const *const p_buffer, uint32_t length</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>close</code> )( <code>audio_playback_ctrl_t *const p_ctrl</code> )
--------------------------	--

**Field Documentation**◆ **open**

```
fsp_err_t(* audio_playback_api_t::open) (audio_playback_ctrl_t *const p_ctrl, audio_playback_cfg_t const *const p_cfg)
```

Open a audio playback module.

**Implemented as**

- [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Open\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to memory allocated for control block.
[in]	p_cfg	Pointer to the hardware configurations.

◆ **start**

```
fsp_err_t(* audio_playback_api_t::start) (audio_playback_ctrl_t *const p_ctrl)
```

Start audio playback hardware.

**Implemented as**

- [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Start\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
------	--------	---------------------------

◆ **stop**

```
fsp_err_t(* audio_playback_api_t::stop) (audio_playback_ctrl_t *const p_ctrl)
```

Stop audio playback hardware.

**Implemented as**

- [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Stop\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
------	--------	---------------------------

◆ **play**

```
fsp_err_t(* audio_playback_api_t::play) (audio_playback_ctrl_t *const p_ctrl, void const *const p_buffer, uint32_t length)
```

Play audio buffer.

**Implemented as**

- [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Play\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_buffer	Pointer to buffer with PCM samples to play. Data must be scaled for audio playback hardware.
[in]	length	Length of data in p_buffer.

◆ **close**

```
fsp_err_t(* audio_playback_api_t::close) (audio_playback_ctrl_t *const p_ctrl)
```

Close the audio driver.

**Implemented as**

- [RM\\_AUDIO\\_PLAYBACK\\_PWM\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control block initialized in <a href="#">audio_playback_api_t::open</a> .
------	--------	--

◆ **audio\_playback\_instance\_t**

```
struct audio_playback_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">audio_playback_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">audio_playback_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">audio_playback_api_t</a> const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **audio\_playback\_ctrl\_t**

```
typedef void audio_playback_ctrl_t
```

Audio Playback control block. Allocate an instance specific control block to pass into the AUDIO\_PLAYBACK API calls.

**Implemented as**

- [audio\\_playback\\_pwm\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**

### ◆ audio\_playback\_event\_t

enum <code>audio_playback_event_t</code>	
Callback event types.	
Enumerator	
<code>AUDIO_PLAYBACK_EVENT_PLAYBACK_COMPLETE</code>	Audio playback complete event.

## 4.3.50 Block Media Interface

### Interfaces

#### Detailed Description

Interface for block media memory access.

## Summary

The block media interface supports reading, writing, and erasing media devices. All functions are non-blocking if possible. The callback is used to determine when an operation completes.

Implemented by:

- SD/MMC Block Media Implementation (`rm_block_media_sdmmc`)
- SPI Block Media Implementation (`rm_block_media_spi`)
- USB HMSC Block Media Implementation (`rm_block_media_usb`)

#### Data Structures

struct `rm_block_media_info_t`

struct `rm_block_media_callback_args_t`

struct `rm_block_media_cfg_t`

struct `rm_block_media_status_t`

struct `rm_block_media_api_t`

struct `rm_block_media_instance_t`

#### Typedefs

typedef void `rm_block_media_ctrl_t`

#### Enumerations

enum `rm_block_media_event_t`**Data Structure Documentation**◆ **rm\_block\_media\_info\_t**

struct <code>rm_block_media_info_t</code>		
Block media device information supported by the instance		
Data Fields		
<code>uint32_t</code>	<code>sector_size_bytes</code>	Sector size in bytes.
<code>uint32_t</code>	<code>num_sectors</code>	Total number of sectors.
<code>bool</code>	<code>reentrant</code>	True if connected block media driver is reentrant.
<code>bool</code>	<code>write_protected</code>	True if connected block media device is write protected.

◆ **rm\_block\_media\_callback\_args\_t**

struct <code>rm_block_media_callback_args_t</code>		
Callback function parameter data		
Data Fields		
<code>rm_block_media_event_t</code>	<code>event</code>	The event can be used to identify what caused the callback.
<code>void const *</code>	<code>p_context</code>	Placeholder for user data.

◆ **rm\_block\_media\_cfg\_t**

struct <code>rm_block_media_cfg_t</code>		
User configuration structure, used in open function		
<b>Data Fields</b>		
<code>void(*</code>	<code>p_callback</code> )( <code>rm_block_media_callback_args_t</code> * <code>p_args</code> )	
		DEPRECATED - Block size, must be a power of 2 multiple of <code>sector_size_bytes</code> . <a href="#">More...</a>
<code>void const *</code>	<code>p_context</code>	User defined context passed into callback function.
<code>void const *</code>	<code>p_extend</code>	Extension parameter for hardware specific settings.

## Field Documentation

### ◆ p\_callback

```
void(* rm_block_media_cfg_t::p_callback) (rm_block_media_callback_args_t *p_args)
```

DEPRECATED - Block size, must be a power of 2 multiple of sector\_size\_bytes.

Pointer to callback function

### ◆ rm\_block\_media\_status\_t

```
struct rm_block_media_status_t
```

Current status

#### Data Fields

bool	initialized	False if <a href="#">rm_block_media_api_t::mediaInit</a> has not been called since media was inserted, true otherwise.
bool	busy	True if media is busy with a previous write/erase operation.
bool	media_inserted	Media insertion status, true if media is not removable.

### ◆ rm\_block\_media\_api\_t

```
struct rm_block_media_api_t
```

Block media interface API.

#### Data Fields

<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )(rm_block_media_ctrl_t *const p_ctrl, rm_block_media_cfg_t const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">mediaInit</a> )(rm_block_media_ctrl_t *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">read</a> )(rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address, uint32_t const num_blocks)
<a href="#">fsp_err_t</a> (*	<a href="#">write</a> )(rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const p_src_address, uint32_t const block_address, uint32_t const num_blocks)
<a href="#">fsp_err_t</a> (*	<a href="#">erase</a> )(rm_block_media_ctrl_t *const p_ctrl, uint32_t const

	block_address, uint32_t const num_blocks)
fsp_err_t(*	callbackSet )(rm_block_media_ctrl_t *const p_ctrl, void(*p_callback)(rm_block_media_callback_args_t *), void const *const p_context, rm_block_media_callback_args_t *const p_callback_memory)
fsp_err_t(*	statusGet )(rm_block_media_ctrl_t *const p_ctrl, rm_block_media_status_t *const p_status)
fsp_err_t(*	infoGet )(rm_block_media_ctrl_t *const p_ctrl, rm_block_media_info_t *const p_info)
fsp_err_t(*	close )(rm_block_media_ctrl_t *const p_ctrl)

## Field Documentation

### ◆ open

fsp\_err\_t(\* rm\_block\_media\_api\_t::open) (rm\_block\_media\_ctrl\_t \*const p\_ctrl, rm\_block\_media\_cfg\_t const \*const p\_cfg)

Initialize block media device. `rm_block_media_api_t::mediaInit` must be called to complete the initialization procedure.

### Implemented as

- RM\_BLOCK\_MEDIA\_SDMMC\_Open
- RM\_BLOCK\_MEDIA\_SPI\_Open
- RM\_BLOCK\_MEDIA\_USB\_Open

### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **medialnit**

```
fsp_err_t(* rm_block_media_api_t::medialnit) (rm_block_media_ctrl_t *const p_ctrl)
```

Initializes a media device. If the device is removable, it must be plugged in prior to calling this API. This function blocks until media initialization is complete.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Medialnit
- RM\_BLOCK\_MEDIA\_SPI\_Medialnit
- RM\_BLOCK\_MEDIA\_USB\_Medialnit

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
------	--------	---

◆ **read**

```
fsp_err_t(* rm_block_media_api_t::read) (rm_block_media_ctrl_t *const p_ctrl, uint8_t *const p_dest_address, uint32_t const block_address, uint32_t const num_blocks)
```

Reads blocks of data from the specified memory device address to the location specified by the caller.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Read
- RM\_BLOCK\_MEDIA\_SPI\_Read
- RM\_BLOCK\_MEDIA\_USB\_Read

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_dest_address	Destination to read the data into.
[in]	block_address	Block address to read the data from.
[in]	num_blocks	Number of blocks of data to read.

◆ **write**

```
fsp_err_t(* rm_block_media_api_t::write) (rm_block_media_ctrl_t *const p_ctrl, uint8_t const *const p_src_address, uint32_t const block_address, uint32_t const num_blocks)
```

Writes blocks of data to the specified device memory address.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Write
- RM\_BLOCK\_MEDIA\_SPI\_Write
- RM\_BLOCK\_MEDIA\_USB\_Write

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	p_src_address	Address to read the data to be written.
[in]	block_address	Block address to write the data to.
[in]	num_blocks	Number of blocks of data to write.

◆ **erase**

```
fsp_err_t(* rm_block_media_api_t::erase) (rm_block_media_ctrl_t *const p_ctrl, uint32_t const block_address, uint32_t const num_blocks)
```

Erases blocks of data from the memory device.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Erase
- RM\_BLOCK\_MEDIA\_SPI\_Erase
- RM\_BLOCK\_MEDIA\_USB\_Erase

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	block_address	Block address to start the erase process at.
[in]	num_blocks	Number of blocks of data to erase.

### ◆ callbackSet

```
fsp_err_t(* rm_block_media_api_t::callbackSet) (rm_block_media_ctrl_t *const p_ctrl, void(
*p_callback)(rm_block_media_callback_args_t *), void const *const p_context,
rm_block_media_callback_args_t *const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

#### Implemented as

- RM\_BLOCK\_MEDIA\_SDMMC\_CallbackSet()

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

### ◆ statusGet

```
fsp_err_t(* rm_block_media_api_t::statusGet) (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_status_t *const p_status)
```

Get status of connected device.

#### Implemented as

- RM\_BLOCK\_MEDIA\_SDMMC\_StatusGet
- RM\_BLOCK\_MEDIA\_SPI\_StatusGet
- RM\_BLOCK\_MEDIA\_USB\_StatusGet

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_status	Pointer to store current status.

## ◆ infoGet

```
fsp_err_t(* rm_block_media_api_t::infoGet) (rm_block_media_ctrl_t *const p_ctrl,
rm_block_media_info_t *const p_info)
```

Returns information about the block media device.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_InfoGet
- RM\_BLOCK\_MEDIA\_SPI\_InfoGet
- RM\_BLOCK\_MEDIA\_USB\_InfoGet

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
[out]	p_info	Pointer to information structure. All elements of this structure will be set by the function.

## ◆ close

```
fsp_err_t(* rm_block_media_api_t::close) (rm_block_media_ctrl_t *const p_ctrl)
```

Closes the module.

**Implemented as**

- RM\_BLOCK\_MEDIA\_SDMMC\_Close
- RM\_BLOCK\_MEDIA\_SPI\_Close
- RM\_BLOCK\_MEDIA\_USB\_Close

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_block_media_api_t::open</a> call.
------	--------	---

## ◆ rm\_block\_media\_instance\_t

```
struct rm_block_media_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">rm_block_media_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rm_block_media_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rm_block_media_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `rm_block_media_ctrl_t`

```
typedef void rm\_block\_media\_ctrl\_t
```

Block media API control block. Allocate an instance specific control block to pass into the block media API calls.

#### Implemented as

- [rm\\_block\\_media\\_sdmmc\\_instance\\_ctrl\\_t](#)
- [rm\\_block\\_media\\_spi\\_instance\\_ctrl\\_t](#)
- [rm\\_block\\_media\\_usb\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ `rm_block_media_event_t`

```
enum rm\_block\_media\_event\_t
```

Events that can trigger a callback function

#### Enumerator

<code>RM_BLOCK_MEDIA_EVENT_MEDIA_REMOVED</code>	Media removed event.
<code>RM_BLOCK_MEDIA_EVENT_MEDIA_INSERTED</code>	Media inserted event.
<code>RM_BLOCK_MEDIA_EVENT_OPERATION_COMPLETE</code>	Read, write, or erase completed.
<code>RM_BLOCK_MEDIA_EVENT_ERROR</code>	Error on media operation.
<code>RM_BLOCK_MEDIA_EVENT_POLL_STATUS</code>	Poll <a href="#">rm_block_media_api_t::statusGet</a> for write/erase completion.
<code>RM_BLOCK_MEDIA_EVENT_MEDIA_SUSPEND</code>	Media suspended event.
<code>RM_BLOCK_MEDIA_EVENT_MEDIA_RESUME</code>	Media resumed event.
<code>RM_BLOCK_MEDIA_EVENT_WAIT</code>	Indication to user that they should wait for an interrupt on a pending operation.
<code>RM_BLOCK_MEDIA_EVENT_WAIT_END</code>	Indication to user that interrupt has been received and waiting can end.

## 4.3.51 Communications Middleware Interface

### Interfaces

#### Detailed Description

Interface for Communications Middleware functions.

## Summary

The Communications interface provides multiple communications functionality.

The Communications interface can be implemented by:

- I2C Communications Middleware (rm\_comms\_i2c)

#### Data Structures

struct [rm\\_comms\\_write\\_read\\_params\\_t](#)

struct [rm\\_comms\\_callback\\_args\\_t](#)

struct [rm\\_comms\\_cfg\\_t](#)

struct [rm\\_comms\\_api\\_t](#)

struct [rm\\_comms\\_instance\\_t](#)

#### Typedefs

typedef void [rm\\_comms\\_ctrl\\_t](#)

#### Enumerations

enum [rm\\_comms\\_event\\_t](#)

#### Data Structure Documentation

##### ◆ [rm\\_comms\\_write\\_read\\_params\\_t](#)

struct [rm\\_comms\\_write\\_read\\_params\\_t](#)

Struct to pack params for writeRead

##### ◆ [rm\\_comms\\_callback\\_args\\_t](#)

struct [rm\\_comms\\_callback\\_args\\_t](#)

Communications middleware callback parameter definition

##### ◆ [rm\\_comms\\_cfg\\_t](#)

struct rm_comms_cfg_t	
Communications middleware configuration block	
Data Fields	
uint32_t	<a href="#">semaphore_timeout</a>
	timeout for callback.
void(*	<a href="#">p_callback</a> )(rm_comms_callback_args_t *p_args)
	Pointer to callback function, mostly used if using non-blocking functionality.
void const *	<a href="#">p_lower_level_cfg</a>
	Pointer to lower level driver configuration structure.
void const *	<a href="#">p_extend</a>
	Pointer to extended configuration by instance of interface.
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.

◆ **rm\_comms\_api\_t**

struct rm_comms_api_t	
COMM APIs	
Data Fields	
fsp_err_t(*	<a href="#">open</a> )(rm_comms_ctrl_t *const p_ctrl, rm_comms_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">close</a> )(rm_comms_ctrl_t *const p_ctrl)
fsp_err_t(*	<a href="#">read</a> )(rm_comms_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
fsp_err_t(*	<a href="#">write</a> )(rm_comms_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t

	const bytes)
--	--------------

<code>fsp_err_t(*</code>	<code>writeRead )(rm_comms_ctrl_t *const p_ctrl, rm_comms_write_read_params_t write_read_params)</code>
--------------------------	---

## Field Documentation

### ◆ open

`fsp_err_t(* rm_comms_api_t::open) (rm_comms_ctrl_t *const p_ctrl, rm_comms_cfg_t const *const p_cfg)`

Open driver.

#### Implemented as

- `RM_COMMS_I2C_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* rm_comms_api_t::close) (rm_comms_ctrl_t *const p_ctrl)`

Close driver.

#### Implemented as

- `RM_COMMS_I2C_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
------	---------------------	-------------------------------

## ◆ read

```
fsp_err_t(* rm_comms_api_t::read) (rm_comms_ctrl_t *const p_ctrl, uint8_t *const p_dest, uint32_t const bytes)
```

Read data.

**Implemented as**

- RM\_COMMS\_I2C\_Read()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_dest	Pointer to the location to store read data.
[in]	bytes	Number of bytes to read.

## ◆ write

```
fsp_err_t(* rm_comms_api_t::write) (rm_comms_ctrl_t *const p_ctrl, uint8_t *const p_src, uint32_t const bytes)
```

Write data.

**Implemented as**

- RM\_COMMS\_I2C\_Write()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_src	Pointer to the location to get write data from.
[in]	bytes	Number of bytes to write.

## ◆ writeRead

```
fsp_err_t(* rm_comms_api_t::writeRead) (rm_comms_ctrl_t *const p_ctrl, rm_comms_write_read_params_t write_read_params)
```

Write bytes over comms followed by a read, will have a struct for params.

**Implemented as**

- RM\_COMMS\_I2C\_WriteRead()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	write_read_params	Parameters structure.

## ◆ rm\_comms\_instance\_t

```
struct rm_comms_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Typedef Documentation

### ◆ rm\_comms\_ctrl\_t

```
typedef void rm_comms_ctrl_t
```

Communications control block. Allocate an instance specific control block to pass into the Communications API calls.

#### Implemented as

- [rm\\_comms\\_i2c\\_instance\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ rm\_comms\_event\_t

```
enum rm_comms_event_t
```

Event in the callback function

## 4.3.52 FileX Block Media Port Interface

### Interfaces

#### Detailed Description

Interface for FileX Block Media port.

## Summary

The FileX block media port provides notifications for insertion and removal of removable media and provides initialization functions required by FileX.

The FileX Block media interface can be implemented by: [Azure RTOS FileX Block Media I/O Driver \(rm\\_filex\\_block\\_media\)](#)

#### Data Structures

```
struct rm_filex_block_media_callback_args_t
```

```
struct rm_filex_block_media_cfg_t
```

```
struct  rm_filex_block_media_api_t
```

```
struct  rm_filex_block_media_instance_t
```

## Typedefs

```
typedef void  rm_filex_block_media_ctrl_t
```

## Enumerations

```
enum  rm_filex_block_media_partition_t
```

## Data Structure Documentation

### ◆ rm\_filex\_block\_media\_callback\_args\_t

struct rm_filex_block_media_callback_args_t		
Callback function parameter data		
Data Fields		
rm_block_media_event_t	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

### ◆ rm\_filex\_block\_media\_cfg\_t

struct rm_filex_block_media_cfg_t		
Block media configuration structure		
<b>Data Fields</b>		
rm_block_media_instance_t *	p_lower_lvl_block_media	
		Lower level block media pointer.
rm_filex_block_media_partition_t	partition	
		Partition to use for partitioned media.
void(*	p_callback )(rm_filex_block_media_callback_args_t *p_args)	
		Pointer to callback function.

### ◆ rm\_filex\_block\_media\_api\_t

```
struct rm_filex_block_media_api_t
```

FileX block media functions implemented at the HAL layer will follow this API.

### Data Fields

<code>fsp_err_t(*</code>	<code>open</code> )( <code>rm_filex_block_media_ctrl_t *const p_ctrl,</code> <code>rm_filex_block_media_cfg_t const *const p_cfg</code> )
--------------------------	--

<code>fsp_err_t(*</code>	<code>close</code> )( <code>rm_filex_block_media_ctrl_t *const p_ctrl</code> )
--------------------------	--

## Field Documentation

### ◆ open

```
fsp_err_t(* rm_filex_block_media_api_t::open) (rm_filex_block_media_ctrl_t *const p_ctrl,
rm_filex_block_media_cfg_t const *const p_cfg)
```

Open media device.

### Implemented as

- `RM_FILEX_BLOCK_MEDIA_Open()`

### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

### ◆ close

```
fsp_err_t(* rm_filex_block_media_api_t::close) (rm_filex_block_media_ctrl_t *const p_ctrl)
```

Close media device.

### Implemented as

- `RM_FILEX_BLOCK_MEDIA_Close()`

### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ rm\_filex\_block\_media\_instance\_t

```
struct rm_filex_block_media_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

<code>rm_filex_block_media_ctrl_t *</code>	p_ctrl	Pointer to the control structure for this instance.
<code>rm_filex_block_media_cfg_t</code>	p_cfg	Pointer to the configuration

const *const		structure for this instance.
<a href="#">rm_filex_block_media_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [rm\\_filex\\_block\\_media\\_ctrl\\_t](#)

typedef void <a href="#">rm_filex_block_media_ctrl_t</a>
Block media control structure

## Enumeration Type Documentation

### ◆ [rm\\_filex\\_block\\_media\\_partition\\_t](#)

enum <a href="#">rm_filex_block_media_partition_t</a>	
Partitions that can be selected to use FileX with	
Enumerator	
RM_FILEX_BLOCK_MEDIA_PARTITION0	Partition 0 (0x01BE) in Master Boot Record Partition Table.
RM_FILEX_BLOCK_MEDIA_PARTITION1	Partition 1 (0x01CE) in Master Boot Record Partition Table.
RM_FILEX_BLOCK_MEDIA_PARTITION2	Partition 2 (0x01DE) in Master Boot Record Partition Table.
RM_FILEX_BLOCK_MEDIA_PARTITION3	Partition 3 (0x01EE) in Master Boot Record Partition Table.

## 4.3.53 FreeRTOS+FAT Port Interface

### Interfaces

#### Detailed Description

Interface for FreeRTOS+FAT port.

## Summary

The FreeRTOS+FAT port provides notifications for insertion and removal of removable media and provides initialization functions required by FreeRTOS+FAT.

The FreeRTOS+FAT interface can be implemented by: [FreeRTOS+FAT Port \(rm\\_freertos\\_plus\\_fat\)](#)

## Data Structures

struct [rm\\_freertos\\_plus\\_fat\\_callback\\_args\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_device\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_api\\_t](#)

struct [rm\\_freertos\\_plus\\_fat\\_instance\\_t](#)

## Enumerations

enum [rm\\_freertos\\_plus\\_fat\\_event\\_t](#)

enum [rm\\_freertos\\_plus\\_fat\\_type\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_freertos\\_plus\\_fat\\_callback\\_args\\_t](#)

struct <a href="#">rm_freertos_plus_fat_callback_args_t</a>		
Callback function parameter data		
Data Fields		
<a href="#">rm_freertos_plus_fat_event_t</a>	event	The event can be used to identify what caused the callback.
void const *	p_context	Placeholder for user data.

### ◆ [rm\\_freertos\\_plus\\_fat\\_device\\_t](#)

struct <a href="#">rm_freertos_plus_fat_device_t</a>		
Information obtained from the media device.		
Data Fields		
uint32_t	sector_count	Sector count.
uint32_t	sector_size_bytes	Sector size in bytes.

### ◆ [rm\\_freertos\\_plus\\_fat\\_api\\_t](#)

struct <a href="#">rm_freertos_plus_fat_api_t</a>		
FreeRTOS plus Fat functions implemented at the HAL layer will follow this API.		
<b>Data Fields</b>		
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">rm_freertos_plus_fat_ctrl_t</a> *const p_ctrl, <a href="#">rm_freertos_plus_fat_cfg_t</a> const *const p_cfg)	

<code>fsp_err_t(*</code>	<code>mediaInit</code> )( <code>rm_freertos_plus_fat_ctrl_t *const p_ctrl</code> , <code>rm_freertos_plus_fat_device_t *const p_device</code> )
<code>fsp_err_t(*</code>	<code>diskInit</code> )( <code>rm_freertos_plus_fat_ctrl_t *const p_ctrl</code> , <code>rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg</code> , <code>FF_Disk_t *const p_disk</code> )
<code>fsp_err_t(*</code>	<code>diskDeinit</code> )( <code>rm_freertos_plus_fat_ctrl_t *const p_ctrl</code> , <code>FF_Disk_t *const p_disk</code> )
<code>fsp_err_t(*</code>	<code>infoGet</code> )( <code>rm_freertos_plus_fat_ctrl_t *const p_ctrl</code> , <code>FF_Disk_t *const p_disk</code> , <code>rm_freertos_plus_fat_info_t *const p_info</code> )
<code>fsp_err_t(*</code>	<code>close</code> )( <code>rm_freertos_plus_fat_ctrl_t *const p_ctrl</code> )

## Field Documentation

### ◆ open

`fsp_err_t(* rm_freertos_plus_fat_api_t::open)` (`rm_freertos_plus_fat_ctrl_t *const p_ctrl`,  
`rm_freertos_plus_fat_cfg_t const *const p_cfg`)

Open media device.

### Implemented as

- `RM_FREERTOS_PLUS_FAT_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

◆ **medialnit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::medialnit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_device_t *const p_device)
```

Initializes a media device. If the device is removable, it must be plugged in prior to calling this API. This function blocks until media initialization is complete.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Medialnit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_device	Pointer to store device information.

◆ **disklnit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::disklnit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
rm_freertos_plus_fat_disk_cfg_t const *const p_disk_cfg, FF_Disk_t *const p_disk)
```

Initializes a FreeRTOS+FAT FF\_Disk\_t structure.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Disklnit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_disk_cfg	Pointer to disk configurations
[out]	p_disk	Pointer to store FreeRTOS+FAT disk structure.

◆ **diskDeinit**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::diskDeinit) (rm_freertos_plus_fat_ctrl_t *const p_ctrl,
FF_Disk_t *const p_disk)
```

Deinitializes a FreeRTOS+FAT FF\_Disk\_t structure.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_DiskDeinit](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_disk_cfg	Pointer to disk configurations
[out]	p_disk	Pointer to store FreeRTOS+FAT disk structure.

◆ **infoGet**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::infoGet) (rm_freertos_plus_fat_ctrl_t *const p_ctrl, FF_Disk_t
*const p_disk, rm_freertos_plus_fat_info_t *const p_info)
```

Returns information about the media device.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_InfoGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_info	Pointer to information structure. All elements of this structure will be set by the function.

◆ **close**

```
fsp_err_t(* rm_freertos_plus_fat_api_t::close) (rm_freertos_plus_fat_ctrl_t *const p_ctrl)
```

Close media device.

**Implemented as**

- [RM\\_FREERTOS\\_PLUS\\_FAT\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **rm\_freertos\_plus\_fat\_instance\_t**

```
struct rm_freertos_plus_fat_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

Data Fields		
<code>rm_freertos_plus_fat_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance.
<code>rm_freertos_plus_fat_cfg_t const *const</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance.
<code>rm_freertos_plus_fat_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance.

## Enumeration Type Documentation

### ◆ `rm_freertos_plus_fat_event_t`

enum <code>rm_freertos_plus_fat_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_REMOVED</code>	Media removed event.
<code>RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_INSERTED</code>	Media inserted event.
<code>RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_SUSPENDED</code>	Media suspended event.
<code>RM_FREERTOS_PLUS_FAT_EVENT_MEDIA_RESUMED</code>	Media resumed event.

### ◆ `rm_freertos_plus_fat_type_t`

enum <code>rm_freertos_plus_fat_type_t</code>	
Enumerator	
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT32</code>	FAT32 disk.
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT16</code>	FAT16 disk.
<code>RM_FREERTOS_PLUS_FAT_TYPE_FAT12</code>	FAT12 disk.

## 4.3.54 HS300X Middleware Interface

### Interfaces

## Detailed Description

Interface for HS300X Middleware functions.

## Summary

The HS300X interface provides HS300X functionality.

The HS300X interface can be implemented by:

- [HS300X Sensor Middleware \(rm\\_hs300x\)](#)

## Data Structures

```
struct rm_hs300x_callback_args_t
```

```
struct rm_hs300x_raw_data_t
```

```
struct rm_hs300x_sensor_data_t
```

```
struct rm_hs300x_data_t
```

```
struct rm_hs300x_cfg_t
```

```
struct rm_hs300x_api_t
```

```
struct rm_hs300x_instance_t
```

## Typedefs

```
typedef void rm_hs300x_ctrl_t
```

## Enumerations

```
enum rm_hs300x_event_t
```

## Data Structure Documentation

### ◆ rm\_hs300x\_callback\_args\_t

```
struct rm_hs300x_callback_args_t
```

HS300X callback parameter definition

### ◆ rm\_hs300x\_raw\_data\_t

```
struct rm_hs300x_raw_data_t
```

HS300X raw data

Data Fields

```
uint8_t
```

```
humidity[2]
```

Upper 2 bits of 0th element are

		data status.
uint8_t	temperature[2]	Lower 2 bits of 1st element are mask.

#### ◆ rm\_hs300x\_sensor\_data\_t

struct rm_hs300x_sensor_data_t		
HS300X sensor data block		
Data Fields		
int16_t	integer_part	
int16_t	decimal_part	To two decimal places.

#### ◆ rm\_hs300x\_data\_t

struct rm_hs300x_data_t		
HS300X data block		

#### ◆ rm\_hs300x\_cfg\_t

struct rm_hs300x_cfg_t		
HS300X Configuration		
<b>Data Fields</b>		
rm_comms_instance_t const *	p_instance	
		Pointer to Communications Middleware instance.
void const *	p_context	
		Pointer to the user-provided context.
void const *	p_extend	
		Pointer to extended configuration by instance of interface.
void(*	p_callback)(rm_hs300x_callback_args_t *p_args)	
		Pointer to callback function.

#### ◆ rm\_hs300x\_api\_t

--	--	--

struct rm\_hs300x\_api\_t

HS300X APIs

**Data Fields**

fsp_err_t(*	open )(rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_cfg_t const *const p_cfg)
-------------	--

fsp_err_t(*	measurementStart )(rm_hs300x_ctrl_t *const p_ctrl)
-------------	--

fsp_err_t(*	read )(rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_raw_data_t *const p_raw_data)
-------------	--

fsp_err_t(*	dataCalculate )(rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_raw_data_t *const p_raw_data, rm_hs300x_data_t *const p_hs300x_data)
-------------	--

fsp_err_t(*	close )(rm_hs300x_ctrl_t *const p_ctrl)
-------------	---

**Field Documentation****◆ open**

fsp_err_t(* rm_hs300x_api_t::open)	(rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_cfg_t const *const p_cfg)
------------------------------------	--

Open sensor.

**Implemented as**

- RM\_HS300X\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **measurementStart**

```
fsp_err_t(* rm_hs300x_api_t::measurementStart) (rm_hs300x_ctrl_t *const p_ctrl)
```

Start a measurement.

**Implemented as**

- [RM\\_HS300X\\_MeasurementStart\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **read**

```
fsp_err_t(* rm_hs300x_api_t::read) (rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_raw_data_t *const p_raw_data)
```

Read ADC data from HS300X.

**Implemented as**

- [RM\\_HS300X\\_Read\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data structure.

◆ **dataCalculate**

```
fsp_err_t(* rm_hs300x_api_t::dataCalculate) (rm_hs300x_ctrl_t *const p_ctrl, rm_hs300x_raw_data_t *const p_raw_data, rm_hs300x_data_t *const p_hs300x_data)
```

Calculate humidity and temperature values from ADC data.

**Implemented as**

- [RM\\_HS300X\\_DataCalculate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_hs300x_data	Pointer to HS300X data structure.

◆ **close**

```
fsp_err_t(* rm_hs300x_api_t::close) (rm_hs300x_ctrl_t *const p_ctrl)
```

Close HS300X.

**Implemented as**

- [RM\\_HS300X\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **rm\_hs300x\_instance\_t**

```
struct rm_hs300x_instance_t
```

HS300X instance

## Data Fields

<a href="#">rm_hs300x_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance
<a href="#">rm_hs300x_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance
<a href="#">rm_hs300x_api_t</a> const *	p_api	Pointer to the API structure for this instance

**Typedef Documentation**◆ **rm\_hs300x\_ctrl\_t**

```
typedef void rm_hs300x_ctrl_t
```

HS300X control block. Allocate an instance specific control block to pass into the HS300X API calls.

**Implemented as**

- [rm\\_hs300x\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **rm\_hs300x\_event\_t**

```
enum rm_hs300x_event_t
```

Event in the callback function

**4.3.55 LittleFS Interface**

## Interfaces

### Detailed Description

Interface for LittleFS access.

### Summary

The LittleFS Port configures a fail-safe filesystem designed for microcontrollers on top of a lower level storage device.

Implemented by: [LittleFS Flash Port \(rm\\_littlefs\\_flash\)](#)

### Data Structures

struct [rm\\_littlefs\\_cfg\\_t](#)

struct [rm\\_littlefs\\_api\\_t](#)

struct [rm\\_littlefs\\_instance\\_t](#)

### Typedefs

typedef void [rm\\_littlefs\\_ctrl\\_t](#)

### Data Structure Documentation

#### ◆ [rm\\_littlefs\\_cfg\\_t](#)

struct <a href="#">rm_littlefs_cfg_t</a>		
User configuration structure, used in open function		
Data Fields		
struct <a href="#">lfs_config</a> const *	<a href="#">p_lfs_cfg</a>	Pointer LittleFS configuration structure.
void const *	<a href="#">p_extend</a>	Pointer to hardware dependent configuration.

#### ◆ [rm\\_littlefs\\_api\\_t](#)

struct <a href="#">rm_littlefs_api_t</a>		
LittleFS Port interface API.		
<b>Data Fields</b>		
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">rm_littlefs_ctrl_t</a> *const p_ctrl, <a href="#">rm_littlefs_cfg_t</a> const *const p_cfg)	
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )( <a href="#">rm_littlefs_ctrl_t</a> *const p_ctrl)	

## Field Documentation

### ◆ open

```
fsp_err_t(* rm_littlefs_api_t::open) (rm_littlefs_ctrl_t *const p_ctrl, rm_littlefs_cfg_t const *const p_cfg)
```

Initialize The lower level storage device.

#### Implemented as

- [RM\\_LITTLEFS\\_FLASH\\_Open](#)

#### Parameters

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

### ◆ close

```
fsp_err_t(* rm_littlefs_api_t::close) (rm_littlefs_ctrl_t *const p_ctrl)
```

Closes the module and lower level storage device.

#### Implemented as

- [RM\\_LITTLEFS\\_FLASH\\_Close](#)

#### Parameters

[in]	p_ctrl	Control block set in <a href="#">rm_littlefs_api_t::open</a> call.
------	--------	--

### ◆ rm\_littlefs\_instance\_t

```
struct rm_littlefs_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

<a href="#">rm_littlefs_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rm_littlefs_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rm_littlefs_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ `rm_littlefs_ctrl_t`

```
typedef void rm_littlefs_ctrl_t
```

LittleFS Port API control block. Allocate an instance specific control block to pass into the LittleFS Port API calls.

#### Implemented as

- `rm_littlefs_flash_instance_ctrl_t`

## 4.3.56 Motor angle Interface

### Interfaces

#### Detailed Description

Interface for motor angle and speed calculation functions.

## Summary

The Motor angle interface calculates the rotor angle and rotational speed from other data.

The motor angle interface can be implemented by:

- [Motor Angle and Speed Estimation \(rm\\_motor\\_estimate\)](#)
- [Motor Angle and Speed Calculation with an Encoder \(rm\\_motor\\_sense\\_encoder\)](#)

#### Data Structures

struct `motor_angle_cfg_t`

struct `motor_angle_current_t`

struct `motor_angle_voltage_reference_t`

struct `motor_angle_encoder_info_t`

struct `motor_angle_api_t`

struct `motor_angle_instance_t`

#### Typedefs

```
typedef void motor_angle_ctrl_t
```

#### Enumerations

enum `motor_sense_encoder_angle_adjust_t`**Data Structure Documentation**◆ **motor\_angle\_cfg\_t**struct `motor_angle_cfg_t`

Configuration parameters.

◆ **motor\_angle\_current\_t**struct `motor_angle_current_t`

Interface structure

## Data Fields

float	id	d-axis current
float	iq	q-axis current

◆ **motor\_angle\_voltage\_reference\_t**struct `motor_angle_voltage_reference_t`

Motor angle voltage reference

## Data Fields

float	vd	d-axis voltage reference
float	vq	q-axis voltage reference

◆ **motor\_angle\_encoder\_info\_t**struct `motor_angle_encoder_info_t`

Motor angle encoder adjustment info

## Data Fields

<code>motor_sense_encoder_angle_adjust_t</code>	e_adjust_status	Encoder Adjustment Status.
uint8_t	u1_adjust_count_full	Adjustment count became full.

◆ **motor\_angle\_api\_t**struct `motor_angle_api_t`

Functions implemented as application interface will follow these APIs.

**Data Fields**

<code>fsp_err_t</code> (*	<code>open</code> )( <code>motor_angle_ctrl_t</code> *const p_ctrl, <code>motor_angle_cfg_t</code> const *const p_cfg)
---------------------------	--

<code>fsp_err_t</code> (*	<code>close</code> )( <code>motor_angle_ctrl_t</code> *const p_ctrl)
---------------------------	--

<code>fsp_err_t(*</code>	<code>reset )(motor_angle_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>currentSet )(motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)</code>
<code>fsp_err_t(*</code>	<code>speedSet )(motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)</code>
<code>fsp_err_t(*</code>	<code>flagPiCtrlSet )(motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)</code>
<code>fsp_err_t(*</code>	<code>internalCalculate )(motor_angle_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>angleSpeedGet )(motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)</code>
<code>fsp_err_t(*</code>	<code>angleAdjust )(motor_angle_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>encoderCyclic )(motor_angle_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>estimatedComponentGet )(motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq)</code>
<code>fsp_err_t(*</code>	<code>infoGet )(motor_angle_ctrl_t *const p_ctrl, motor_angle_encoder_info_t *const p_info)</code>
<code>fsp_err_t(*</code>	<code>parameterUpdate )(motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *p_cfg)</code>

## Field Documentation

◆ **open**

```
fsp_err_t(* motor_angle_api_t::open) (motor_angle_ctrl_t *const p_ctrl, motor_angle_cfg_t const *const p_cfg)
```

Initialize the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_Open()
- RM\_MOTOR\_SENSE\_ENCODER\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* motor_angle_api_t::close) (motor_angle_ctrl_t *const p_ctrl)
```

Close (Finish) the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_Close()
- RM\_MOTOR\_SENSE\_ENCODER\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_angle_api_t::reset) (motor_angle_ctrl_t *const p_ctrl)
```

Reset the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_Reset()
- RM\_MOTOR\_SENSE\_ENCODER\_Reset()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ currentSet

```
fsp_err_t(* motor_angle_api_t::currentSet) (motor_angle_ctrl_t *const p_ctrl, motor_angle_current_t *const p_st_current, motor_angle_voltage_reference_t *const p_st_voltage)
```

Set (Input) Current & Voltage Reference data into the Motor\_Angle.

#### Implemented as

- RM\_MOTOR\_ESTIMATE\_CurrentSet()
- RM\_MOTOR\_SENSE\_ENCODER\_CurrentSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_current	Pointer to current structure
[in]	p_st_voltage	Pointer to voltage Reference structure

### ◆ speedSet

```
fsp_err_t(* motor_angle_api_t::speedSet) (motor_angle_ctrl_t *const p_ctrl, float const speed_ctrl, float const damp_speed)
```

Set (Input) Speed Information into the Motor\_Angle.

#### Implemented as

- RM\_MOTOR\_ESTIMATE\_SpeedSet()
- RM\_MOTOR\_SENSE\_ENCODER\_SpeedSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	speed_ctrl	Control reference of rotational speed [rad/s]
[in]	damp_speed	Damping rotational speed [rad/s]

◆ **flagPiCtrlSet**

```
fsp_err_t(* motor_angle_api_t::flagPiCtrlSet) (motor_angle_ctrl_t *const p_ctrl, uint32_t const flag_pi)
```

Set the flag of PI Control runs.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_FlagPiCtrlSet()
- RM\_MOTOR\_SENSE\_ENCODER\_FlagPiCtrlSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	flag_pi	The flag of PI control runs

◆ **internalCalculate**

```
fsp_err_t(* motor_angle_api_t::internalCalculate) (motor_angle_ctrl_t *const p_ctrl)
```

Calculate internal parameters of encoder process.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_InternalCalculate()
- RM\_MOTOR\_SENSE\_ENCODER\_InternalCalculate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **angleSpeedGet**

```
fsp_err_t(* motor_angle_api_t::angleSpeedGet) (motor_angle_ctrl_t *const p_ctrl, float *const p_angle, float *const p_speed, float *const p_phase_err)
```

Get rotor angle and rotational speed from the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_AngleSpeedGet()
- RM\_MOTOR\_SENSE\_ENCODER\_AngleSpeedGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_angl	Memory address to get rotor angle data
[out]	p_speed	Memory address to get rotational speed data
[out]	p_phase_err	Memory address to get phase(angle) error data

◆ **angleAdjust**

```
fsp_err_t(* motor_angle_api_t::angleAdjust) (motor_angle_ctrl_t *const p_ctrl)
```

Angle Adjustment Process.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_AngleAdjust()
- RM\_MOTOR\_SENSE\_ENCODER\_AngleAdjust()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **encoderCyclic**

```
fsp_err_t(* motor_angle_api_t::encoderCyclic) (motor_angle_ctrl_t *const p_ctrl)
```

Encoder Cyclic Process.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_EncoderCyclic()
- RM\_MOTOR\_SENSE\_ENCODER\_EncoderCyclic()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **estimatedComponentGet**

```
fsp_err_t(* motor_angle_api_t::estimatedComponentGet) (motor_angle_ctrl_t *const p_ctrl, float *const p_ed, float *const p_eq)
```

Get estimated d/q-axis component from the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_EstimatedComponentGet()
- RM\_MOTOR\_SENSE\_ENCODER\_EstimatedComponentGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_ed	Memory address to get estimated d-axis component
[out]	p_eq	Memory address to get estimated q-axis component

◆ **infoGet**

```
fsp_err_t(* motor_angle_api_t::infoGet) (motor_angle_ctrl_t *const p_ctrl,
motor_angle_encoder_info_t *const p_info)
```

Get Encoder Calculate Information.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_InfoGet()
- RM\_MOTOR\_SENSE\_ENCODER\_InfoGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_info	Memory address to get encoder calculate information

◆ **parameterUpdate**

```
fsp_err_t(* motor_angle_api_t::parameterUpdate) (motor_angle_ctrl_t *const p_ctrl,
motor_angle_cfg_t const *p_cfg)
```

Update Parameters for the calculation in the Motor\_Angle.

**Implemented as**

- RM\_MOTOR\_ESTIMATE\_ParameterUpdate()
- RM\_MOTOR\_SENSE\_ENCODER\_ParameterUpdate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **motor\_angle\_instance\_t**

```
struct motor_angle_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_angle_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_angle_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_angle_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **motor\_angle\_ctrl\_t**typedef void [motor\\_angle\\_ctrl\\_t](#)

Motor Angle Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [motor\\_angle\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **motor\_sense\_encoder\_angle\_adjust\_t**enum [motor\\_sense\\_encoder\\_angle\\_adjust\\_t](#)

Enumerator

MOTOR_SENSE_ENCODER_ANGLE_ADJUST_90_DEGREE	Roter Angle Adjustment to pull in 90degree.
MOTOR_SENSE_ENCODER_ANGLE_ADJUST_0_DEGREE	Roter Angle Adjustment to pull in 0degree.
MOTOR_SENSE_ENCODER_ANGLE_ADJUST_FINISH	Roter Angle Adjustment Finish.

**4.3.57 Motor Interface**[Interfaces](#)**Detailed Description**

Interface for Motor functions.

**Summary**

The Motor interface provides Motor functionality.

Implemented by:

- [Motor Sensorless Vector Control \(rm\\_motor\\_sensorless\)](#)
- [Motor encoder vector control \(rm\\_motor\\_encoder\)](#)

**Data Structures**struct [motor\\_cfg\\_t](#)struct [motor\\_api\\_t](#)

```
struct motor_instance_t
```

## Typedefs

```
typedef void motor_ctrl_t
```

## Enumerations

```
enum motor_error_t
```

## Data Structure Documentation

### ◆ motor\_cfg\_t

struct motor_cfg_t		
Configuration parameters.		
Data Fields		
<a href="#">motor_speed_instance_t</a> const *	p_motor_speed_instance	Speed Instance.
<a href="#">motor_current_instance_t</a> const *	p_motor_current_instance	Current Instance.
void const *	p_context	Placeholder for user data. Passed to the user callback in <a href="#">motor_callback_args_t</a> .
void const *	p_extend	Placeholder for user extension.

### ◆ motor\_api\_t

struct motor_api_t	
Functions implemented at the HAL layer will follow this API.	
Data Fields	
<a href="#">fsp_err_t</a> (*	<a href="#">open</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl, <a href="#">motor_cfg_t</a> const *const p_cfg)
<a href="#">fsp_err_t</a> (*	<a href="#">close</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">run</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">stop</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">reset</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl)
<a href="#">fsp_err_t</a> (*	<a href="#">errorSet</a> )( <a href="#">motor_ctrl_t</a> *const p_ctrl, <a href="#">motor_error_t</a> const error)

<code>fsp_err_t(*</code>	<code>speedSet )(motor_ctrl_t *const p_ctrl, float const speed_rpm)</code>
<code>fsp_err_t(*</code>	<code>positionSet )(motor_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(motor_ctrl_t *const p_ctrl, uint8_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>angleGet )(motor_ctrl_t *const p_ctrl, float *const p_angle_rad)</code>
<code>fsp_err_t(*</code>	<code>speedGet )(motor_ctrl_t *const p_ctrl, float *const p_speed_rpm)</code>
<code>fsp_err_t(*</code>	<code>errorCheck )(motor_ctrl_t *const p_ctrl, uint16_t *const p_error)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* motor_api_t::open) (motor_ctrl_t *const p_ctrl, motor_cfg_t const *const p_cfg)`

Open driver.

#### Implemented as

- `RM_MOTOR_SENSORLESS_Open()`
- `RM_MOTOR_ENCODER_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* motor_api_t::close) (motor_ctrl_t *const p_ctrl)`

Close driver.

#### Implemented as

- `RM_MOTOR_SENSORLESS_Close()`
- `RM_MOTOR_ENCODER_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
------	---------------------	-------------------------------

◆ **run**

```
fsp_err_t(* motor_api_t::run) (motor_ctrl_t *const p_ctrl)
```

Run the motor. (Start the motor rotation.)

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_Run()
- RM\_MOTOR\_ENCODER\_Run()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **stop**

```
fsp_err_t(* motor_api_t::stop) (motor_ctrl_t *const p_ctrl)
```

Stop the motor. (Stop the motor rotation.)

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_Stop()
- RM\_MOTOR\_ENCODER\_Stop()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_api_t::reset) (motor_ctrl_t *const p_ctrl)
```

Reset the motor control. (Recover from the error status.)

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_Reset()
- RM\_MOTOR\_ENCODER\_Reset()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **errorSet**

```
fsp_err_t(* motor_api_t::errorSet) (motor_ctrl_t *const p_ctrl, motor_error_t const error)
```

Set Error Information.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_ErrorSet()
- RM\_MOTOR\_ENCODER\_ErrorSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	error	Happend error code

◆ **speedSet**

```
fsp_err_t(* motor_api_t::speedSet) (motor_ctrl_t *const p_ctrl, float const speed_rpm)
```

Set rotation speed.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_SpeedSet()
- RM\_MOTOR\_ENCODER\_SpeedSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	speed_rpm	Required rotation speed [rpm]

◆ **positionSet**

```
fsp_err_t(* motor_api_t::positionSet) (motor_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position)
```

Set reference position.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_PositionSet()
- RM\_MOTOR\_ENCODER\_PositionSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_position	Pointer to set required data

◆ **statusGet**

```
fsp_err_t(* motor_api_t::statusGet) (motor_ctrl_t *const p_ctrl, uint8_t *const p_status)
```

Get the motor control status.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_StatusGet()
- RM\_MOTOR\_ENCODER\_StatusGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_status	Pointer to get the motor control status

◆ **angleGet**

```
fsp_err_t(* motor_api_t::angleGet) (motor_ctrl_t *const p_ctrl, float *const p_angle_rad)
```

Get the rotor angle.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_AngleGet()
- RM\_MOTOR\_ENCODER\_AngleGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_angle_rad	Pointer to get the rotor angle [rad]

◆ **speedGet**

```
fsp_err_t(* motor_api_t::speedGet) (motor_ctrl_t *const p_ctrl, float *const p_speed_rpm)
```

Get the rotation speed.

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_SpeedGet()
- RM\_MOTOR\_ENCODER\_SpeedGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_speed_rpm	Pointer to get the rotation speed [rpm]

◆ **errorCheck**

```
fsp_err_t(* motor_api_t::errorCheck) (motor_ctrl_t *const p_ctrl, uint16_t *const p_error)
```

Check the error occurrence

**Implemented as**

- RM\_MOTOR\_SENSORLESS\_ErrorCheck()
- RM\_MOTOR\_ENCODER\_ErrorCheck()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_error	Pointer to get occurred error

◆ **motor\_instance\_t**

```
struct motor_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **motor\_ctrl\_t**

```
typedef void motor_ctrl_t
```

Motor Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_instance\_ctrl\_t

**Enumeration Type Documentation**◆ **motor\_error\_t**

```
enum motor_error_t
```

Error information

## 4.3.58 Motor current Interface

### Interfaces

#### Detailed Description

Interface for motor current functions.

## Summary

The Motor current interface for getting the PWM modulation duty from electric current and speed

The motor current control interface can be implemented by:

- Motor Current (rm\_motor\_current)

#### Data Structures

struct [motor\\_current\\_output\\_t](#)

struct [motor\\_current\\_input\\_current\\_t](#)

struct [motor\\_current\\_input\\_voltage\\_t](#)

struct [motor\\_current\\_get\\_voltage\\_t](#)

struct [motor\\_current\\_cfg\\_t](#)

struct [motor\\_current\\_api\\_t](#)

struct [motor\\_current\\_instance\\_t](#)

#### Typedefs

typedef void [motor\\_current\\_ctrl\\_t](#)

#### Enumerations

enum [motor\\_current\\_event\\_t](#)

#### Data Structure Documentation

##### ◆ motor\_current\_output\_t

struct <a href="#">motor_current_output_t</a>		
Structure of interface to speed control Output parameters		
Data Fields		
float	f_id	D-axis current [A].

float	f_iq	Q-axis current [A].
float	f_vamax	
float	f_speed_rad	Speed value [rad/s].
float	f_speed_rpm	Speed value [rpm].
float	f_rotor_angle	Motor rotor angle [rad].
float	f_position_rad	Motor rotor position [rad].
float	f_ed	Estimated d-axis component[V] of flux due to the permanent magnet.
float	f_eq	Estimated q-axis component[V] of flux due to the permanent magnet.
float	f_phase_err_rad	Phase error [rad].
uint8_t	u1_flag_get_iref	Flag to set d/q-axis current reference.
uint8_t	u1_adjust_status	Angle adjustment satatus.
uint8_t	u1_adjust_count_full	Angle adjustment count full.

#### ◆ motor\_current\_input\_current\_t

struct motor_current_input_current_t		
Three-phase input current		
Data Fields		
float	iu	U phase current[A].
float	iv	V phase current[A].
float	iw	W phase current[A].

#### ◆ motor\_current\_input\_voltage\_t

struct motor_current_input_voltage_t		
Input voltage		
Data Fields		
float	vdc	Main line voltage[V].
float	va_max	Maximum magnitude of voltage vector[V].

#### ◆ motor\_current\_get\_voltage\_t

struct motor_current_get_voltage_t		
Struct to get motor current		
Data Fields		

float	u_voltage	U phase voltage[V].
float	v_voltage	V phase voltage[V].
float	w_voltage	W phase voltage[V].
float	vd_reference	d-axis voltage reference
float	vq_reference	q-axis voltage reference

#### ◆ motor\_current\_cfg\_t

struct motor_current_cfg_t
Configuration parameters.

#### ◆ motor\_current\_api\_t

struct motor_current_api_t	
Functions implemented at the Motor Current Module will follow these APIs.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	reset )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	run )(motor_current_ctrl_t *const p_ctrl)
fsp_err_t(*)	parameterSet )(motor_current_ctrl_t *const p_ctrl, motor_current_input_t const *const p_st_input)
fsp_err_t(*)	currentReferenceSet )(motor_current_ctrl_t *const p_ctrl, float const id_reference, float const iq_reference)
fsp_err_t(*)	speedPhaseSet )(motor_current_ctrl_t *const p_ctrl, float const speed_rad, float const phase_rad)
fsp_err_t(*)	currentSet )(motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage)
fsp_err_t(*)	parameterGet )(motor_current_ctrl_t *const p_ctrl,

	<code>motor_current_output_t *const p_st_output)</code>
<code>fsp_err_t(*</code>	<code>currentGet )(motor_current_ctrl_t *const p_ctrl, float *const p_id, float *const p_iq)</code>
<code>fsp_err_t(*</code>	<code>phaseVoltageGet )(motor_current_ctrl_t *const p_ctrl, motor_current_get_voltage_t *const p_voltage)</code>
<code>fsp_err_t(*</code>	<code>parameterUpdate )(motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* motor_current_api_t::open) (motor_current_ctrl_t *const p_ctrl, motor_current_cfg_t const *const p_cfg)`

Initialize the motor current module.

#### Implemented as

- `RM_MOTOR_CURRENT_Open()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* motor_current_api_t::close) (motor_current_ctrl_t *const p_ctrl)`

Close (Finish) the motor current module.

#### Implemented as

- `RM_MOTOR_CURRENT_Close()`

#### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
------	---------------------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_current_api_t::reset) (motor_current_ctrl_t *const p_ctrl)
```

Reset variables for the motor current module.

**Implemented as**

- RM\_MOTOR\_CURRENT\_Reset()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **run**

```
fsp_err_t(* motor_current_api_t::run) (motor_current_ctrl_t *const p_ctrl)
```

Activate the motor current control.

**Implemented as**

- RM\_MOTOR\_CURRENT\_Run()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterSet**

```
fsp_err_t(* motor_current_api_t::parameterSet) (motor_current_ctrl_t *const p_ctrl,  
motor_current_input_t const *const p_st_input)
```

Set (Input) parameters into the motor current module.

**Implemented as**

- RM\_MOTOR\_CURRENT\_ParameterSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_input	Pointer to input data structure(speed control output data)

### ◆ currentReferenceSet

`fsp_err_t(* motor_current_api_t::currentReferenceSet) (motor_current_ctrl_t *const p_ctrl, float const id_reference, float const iq_reference)`

Set (Input) Current reference into the motor current module.

#### Implemented as

- `RM_MOTOR_CURRENT_CurrentReferenceSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	id_reference	D-axis current reference [A]
[in]	iq_reference	Q-axis current reference [A]

### ◆ speedPhaseSet

`fsp_err_t(* motor_current_api_t::speedPhaseSet) (motor_current_ctrl_t *const p_ctrl, float const speed_rad, float const phase_rad)`

Set (Input) Speed & Phase data into the motor current module.

#### Implemented as

- `RM_MOTOR_CURRENT_SpeedPhaseSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	speed_rad	Rotational speed [rad/s]
[in]	phase_rad	Rotor phase [rad]

### ◆ currentSet

`fsp_err_t(* motor_current_api_t::currentSet) (motor_current_ctrl_t *const p_ctrl, motor_current_input_current_t const *const p_st_current, motor_current_input_voltage_t const *const p_st_voltage)`

Set (Input) Current data into the motor current module.

#### Implemented as

- `RM_MOTOR_CURRENT_CurrentSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_current	Pointer to input current structure
[in]	p_st_voltage	Pointer to input voltage structure

◆ **parameterGet**

```
fsp_err_t(* motor_current_api_t::parameterGet) (motor_current_ctrl_t *const p_ctrl,
motor_current_output_t *const p_st_output)
```

Get (output) parameters from the motor current module

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_ParameterGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_st_output	Pointer to output data structure(speed control input data)

◆ **currentGet**

```
fsp_err_t(* motor_current_api_t::currentGet) (motor_current_ctrl_t *const p_ctrl, float *const p_id,
float *const p_iq)
```

Get d/q-axis current

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_CurrentGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_id	Pointer to get d-axis current [A]
[out]	p_iq	Pointer to get q-axis current [A]

◆ **phaseVoltageGet**

```
fsp_err_t(* motor_current_api_t::phaseVoltageGet) (motor_current_ctrl_t *const p_ctrl,
motor_current_get_voltage_t *const p_voltage)
```

Get phase output voltage

**Implemented as**

- [RM\\_MOTOR\\_CURRENT\\_PhaseVoltageGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_voltage	Pointer to get voltages

◆ **parameterUpdate**

```
fsp_err_t(* motor_current_api_t::parameterUpdate) (motor_current_ctrl_t *const p_ctrl,
motor_current_cfg_t const *const p_cfg)
```

Update parameters for the calculation in the motor current control.

**Implemented as**

- RM\_MOTOR\_CURRENT\_ParameterUpdate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **motor\_current\_instance\_t**

```
struct motor_current_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_current_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_current_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_current_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **motor\_current\_ctrl\_t**

```
typedef void motor_current_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_current\_ctrl\_t

**Enumeration Type Documentation**

◆ **motor\_current\_event\_t**

enum <code>motor_current_event_t</code>	
Events that can trigger a callback function	
Enumerator	
<code>MOTOR_CURRENT_EVENT_FORWARD</code>	Event forward current control.
<code>MOTOR_CURRENT_EVENT_DATA_SET</code>	Event set speed control output data.
<code>MOTOR_CURRENT_EVENT_BACKWARD</code>	Event backward current control.

**4.3.59 Motor driver Interface**[Interfaces](#)**Detailed Description**

Interface for motor driver functions.

**Summary**

The Motor driver interface for setting the PWM modulation duty

The motor current control interface can be implemented by:

- [Motor Driver \(rm\\_motor\\_driver\)](#)

**Data Structures**

struct [motor\\_driver\\_callback\\_args\\_t](#)

struct [motor\\_driver\\_current\\_get\\_t](#)

struct [motor\\_driver\\_cfg\\_t](#)

struct [motor\\_driver\\_api\\_t](#)

struct [motor\\_driver\\_instance\\_t](#)

**Typedefs**

typedef void [motor\\_driver\\_ctrl\\_t](#)

**Enumerations**

enum [motor\\_driver\\_event\\_t](#)

## Data Structure Documentation

### ◆ motor\_driver\_callback\_args\_t

struct motor_driver_callback_args_t		
Callback function parameter data		
Data Fields		
<a href="#">motor_driver_event_t</a>	event	Event trigger.
void const *	p_context	Placeholder for user data.

### ◆ motor\_driver\_current\_get\_t

struct motor_driver_current_get_t		
Current Data Get Structure		
Data Fields		
float	iu	U phase current [A].
float	iw	W phase current [A].
float	vdc	Main Line Voltage [V].
float	va_max	maximum magnitude of voltage vector

### ◆ motor\_driver\_cfg\_t

struct motor_driver_cfg_t		
Configuration parameters.		
<b>Data Fields</b>		
<a href="#">adc_channel_t</a>	<a href="#">iu_ad_ch</a>	
		A/D Channel for U Phase Current.
<a href="#">adc_channel_t</a>	<a href="#">iw_ad_ch</a>	
		A/D Channel for W Phase Current.
<a href="#">adc_channel_t</a>	<a href="#">vdc_ad_ch</a>	
		A/D Channel for Main Line Voltage.
void const *	<a href="#">p_context</a>	
		Placeholder for user data.

--

### ◆ motor\_driver\_api\_t

struct motor\_driver\_api\_t

Functions implemented at the HAL layer will follow these APIs.

#### Data Fields

fsp_err_t(*)	open )(motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)
fsp_err_t(*)	close )(motor_driver_ctrl_t *const p_ctrl)
fsp_err_t(*)	reset )(motor_driver_ctrl_t *const p_ctrl)
fsp_err_t(*)	phaseVoltageSet )(motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage)
fsp_err_t(*)	currentGet )(motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get)
fsp_err_t(*)	flagCurrentOffsetGet )(motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset)
fsp_err_t(*)	currentOffsetRestart )(motor_driver_ctrl_t *const p_ctrl)
fsp_err_t(*)	parameterUpdate )(motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)

#### Field Documentation

--

◆ **open**

```
fsp_err_t(* motor_driver_api_t::open) (motor_driver_ctrl_t *const p_ctrl, motor_driver_cfg_t const *const p_cfg)
```

Initialize the Motor Driver Module.

**Implemented as**

- [RM\\_MOTOR\\_DRIVER\\_Open\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* motor_driver_api_t::close) (motor_driver_ctrl_t *const p_ctrl)
```

Close the Motor Driver Module

**Implemented as**

- [RM\\_MOTOR\\_DRIVER\\_Close\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_driver_api_t::reset) (motor_driver_ctrl_t *const p_ctrl)
```

Reset variables of the Motor Driver Module

**Implemented as**

- [RM\\_MOTOR\\_DRIVER\\_Reset\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ phaseVoltageSet

`fsp_err_t(* motor_driver_api_t::phaseVoltageSet) (motor_driver_ctrl_t *const p_ctrl, float const u_voltage, float const v_voltage, float const w_voltage)`

Set (Input) Phase Voltage data into the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_PhaseVoltageSet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	u_voltage	U phase voltage [V]
[in]	v_voltage	V phase voltage [V]
[in]	w_voltage	W phase voltage [V]

### ◆ currentGet

`fsp_err_t(* motor_driver_api_t::currentGet) (motor_driver_ctrl_t *const p_ctrl, motor_driver_current_get_t *const p_current_get)`

Get Phase current, Vdc and Va\_max data from the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_CurrentGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_current_get	Pointer to get data structure.

### ◆ flagCurrentOffsetGet

`fsp_err_t(* motor_driver_api_t::flagCurrentOffsetGet) (motor_driver_ctrl_t *const p_ctrl, uint8_t *const p_flag_offset)`

Get the flag of finish current offset detection from the Motor Driver Module

#### Implemented as

- `RM_MOTOR_DRIVER_FlagCurrentOffsetGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_flag_offset	Flag of finish current offset detection

◆ **currentOffsetRestart**

```
fsp_err_t(* motor_driver_api_t::currentOffsetRestart) (motor_driver_ctrl_t *const p_ctrl)
```

Restart current offset detection

**Implemented as**

- RM\_MOTOR\_DRIVER\_CurrentOffsetRestart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterUpdate**

```
fsp_err_t(* motor_driver_api_t::parameterUpdate) (motor_driver_ctrl_t *const p_ctrl,  
motor_driver_cfg_t const *const p_cfg)
```

Update Configuration Parameters for the calculation in the Motor Driver Module

**Implemented as**

- RM\_MOTOR\_DRIVER\_ParameterUpdate()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **motor\_driver\_instance\_t**

```
struct motor_driver_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_driver_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_driver_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_driver_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **motor\_driver\_ctrl\_t**

```
typedef void motor_driver_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- motor\_driver\_ctrl\_t

**Enumeration Type Documentation**◆ **motor\_driver\_event\_t**

```
enum motor_driver_event_t
```

Events that can trigger a callback function

Enumerator

MOTOR_DRIVER_EVENT_FORWARD	Event before Motor Driver Process (before Current Control timing)
MOTOR_DRIVER_EVENT_CURRENT	Event Current Control timing.
MOTOR_DRIVER_EVENT_BACKWARD	Event after Motor Driver Process (after PWM duty setting)

**4.3.60 Motor position Interface****Interfaces****Detailed Description**

Interface for motor position functions.

**Summary**

The Motor position interface for getting the speed references from Encoder Sensor

The motor position interface can be implemented by:

- [Motor Position \(rm\\_motor\\_position\)](#)

**Data Structures**

```
struct motor_position_cfg_t
```

```
struct motor_position_api_t
```

```
struct motor_position_instance_t
```

## Typedefs

```
typedef void motor_position_ctrl_t
```

## Enumerations

```
enum motor_position_ctrl_mode_t
```

## Data Structure Documentation

### ◆ motor\_position\_cfg\_t

struct motor_position_cfg_t		
Configuration parameters.		
Data Fields		
void const *	p_context	Placeholder for user data.
void const *	p_extend	

### ◆ motor\_position\_api\_t

struct motor_position_api_t		
Functions implemented at the HAL layer will follow these APIs.		
<b>Data Fields</b>		
fsp_err_t(*)	open	(motor_position_ctrl_t *const p_ctrl, motor_position_cfg_t const *const p_cfg)
fsp_err_t(*)	close	(motor_position_ctrl_t *const p_ctrl)
fsp_err_t(*)	reset	(motor_position_ctrl_t *const p_ctrl)
fsp_err_t(*)	positionGet	(motor_position_ctrl_t *const p_ctrl, int16_t *const p_position)
fsp_err_t(*)	positionSet	(motor_position_ctrl_t *const p_ctrl, float const position_rad)
fsp_err_t(*)	positionReferenceSet	(motor_position_ctrl_t *const p_ctrl, int16_t const position_reference_deg)

<code>fsp_err_t(*</code>	<code>controlModeSet )(motor_position_ctrl_t *const p_ctrl, motor_position_ctrl_mode_t const mode)</code>
<code>fsp_err_t(*</code>	<code>positionControl )(motor_position_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>ipdSpeedPControl )(motor_position_ctrl_t *const p_ctrl, float const ref_speed_rad, float const speed_rad, float *const p_iq_ref)</code>
<code>fsp_err_t(*</code>	<code>speedReferencePControlGet )(motor_position_ctrl_t *const p_ctrl, float *const p_speed_ref)</code>
<code>fsp_err_t(*</code>	<code>speedReferenceIpdcControlGet )(motor_position_ctrl_t *const p_ctrl, float const max_speed_rad, float *const p_speed_ref)</code>
<code>fsp_err_t(*</code>	<code>speedReferenceFeedforwardGet )(motor_position_ctrl_t *const p_ctrl, float *const p_speed_ref)</code>
<code>fsp_err_t(*</code>	<code>parameterUpdate )(motor_position_ctrl_t *const p_ctrl, motor_position_cfg_t const *const p_cfg)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* motor_position_api_t::open) (motor_position_ctrl_t *const p_ctrl, motor_position_cfg_t const *const p_cfg)`

Initialize the Motor Position Module.

### Implemented as

- `RM_MOTOR_POSITION_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

◆ **close**

```
fsp_err_t(* motor_position_api_t::close) (motor_position_ctrl_t *const p_ctrl)
```

Close (Finish) the Motor Position Module.

**Implemented as**

- RM\_MOTOR\_POSITION\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_position_api_t::reset) (motor_position_ctrl_t *const p_ctrl)
```

Reset(Stop) the Motor Position Module.

**Implemented as**

- RM\_MOTOR\_POSITION\_Reset()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **positionGet**

```
fsp_err_t(* motor_position_api_t::positionGet) (motor_position_ctrl_t *const p_ctrl, int16_t *const p_position)
```

Get Position data.

**Implemented as**

- RM\_MOTOR\_POSITION\_PositionGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_position	Pointer to get position data

◆ **positionSet**

```
fsp_err_t(* motor_position_api_t::positionSet) (motor_position_ctrl_t *const p_ctrl, float const position_rad)
```

Set Position data from Encoder.

**Implemented as**

- [RM\\_MOTOR\\_POSITION\\_PositionSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	position_rad	Position data [radian]

◆ **positionReferenceSet**

```
fsp_err_t(* motor_position_api_t::positionReferenceSet) (motor_position_ctrl_t *const p_ctrl, int16_t const position_reference_deg)
```

Set (Input) Position reference into the Motor Position Module.

**Implemented as**

- [RM\\_MOTOR\\_POSITION\\_PositionReferenceSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	position_refernce_deg	Position reference [degree]

◆ **controlModeSet**

```
fsp_err_t(* motor_position_api_t::controlModeSet) (motor_position_ctrl_t *const p_ctrl, motor_position_ctrl_mode_t const mode)
```

Set (Input) Position Control Mode.

**Implemented as**

- [RM\\_MOTOR\\_POSITION\\_ControlModeSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	mode	Position Control Mode

### ◆ positionControl

`fsp_err_t(* motor_position_api_t::positionControl) (motor_position_ctrl_t *const p_ctrl)`

Calculate internal position reference

#### Implemented as

- `RM_MOTOR_POSITION_PositionControl()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

### ◆ ipdSpeedPControl

`fsp_err_t(* motor_position_api_t::ipdSpeedPControl) (motor_position_ctrl_t *const p_ctrl, float const ref_speed_rad, float const speed_rad, float *const p_iq_ref)`

Calculate iq reference

#### Implemented as

- `RM_MOTOR_POSITION_IpdSpeedPControl()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	ref_speed_rad	Speed Reference [rad/sec]
[in]	speed_rad	Current Speed [rad/sec]
[out]	p_iq_ref	Pointer to get iq reference

### ◆ speedReferencePControlGet

`fsp_err_t(* motor_position_api_t::speedReferencePControlGet) (motor_position_ctrl_t *const p_ctrl, float *const p_speed_ref)`

Get Speed Reference by P Control

#### Implemented as

- `RM_MOTOR_POSITION_SpeedReferencePControlGet()`

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_speed_ref	Pointer to get speed reference

### ◆ speedReferenceIpdControlGet

`fsp_err_t(* motor_position_api_t::speedReferenceIpdControlGet) (motor_position_ctrl_t *const p_ctrl, float const max_speed_rad, float *const p_speed_ref)`

Get Speed Reference by IPD Control

#### Implemented as

- [RM\\_MOTOR\\_POSITION\\_SpeedReferenceIpdControlGet\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_speed_ref	Pointer to get speed reference

### ◆ speedReferenceFeedforwardGet

`fsp_err_t(* motor_position_api_t::speedReferenceFeedforwardGet) (motor_position_ctrl_t *const p_ctrl, float *const p_speed_ref)`

Get Speed Reference by Speed Feedforward

#### Implemented as

- [RM\\_MOTOR\\_POSITION\\_SpeedReferenceFeedforwardGet\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[out]	p_speed_ref	Pointer to get speed reference

### ◆ parameterUpdate

`fsp_err_t(* motor_position_api_t::parameterUpdate) (motor_position_ctrl_t *const p_ctrl, motor_position_cfg_t const *const p_cfg)`

Update Parameters for the calculation in the Motor Position Module.

#### Implemented as

- [RM\\_MOTOR\\_POSITION\\_ParameterUpdate\(\)](#)

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

### ◆ motor\_position\_instance\_t

`struct motor_position_instance_t`

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

<a href="#">motor_position_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">motor_position_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">motor_position_api_t</a> const *	p_api	Pointer to the API structure for this instance.

## Typedef Documentation

### ◆ [motor\\_position\\_ctrl\\_t](#)

```
typedef void motor\_position\_ctrl\_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

#### Implemented as

- [motor\\_position\\_ctrl\\_t](#)

## Enumeration Type Documentation

### ◆ [motor\\_position\\_ctrl\\_mode\\_t](#)

```
enum motor\_position\_ctrl\_mode\_t
```

Position Control Mode

## 4.3.61 Motor speed Interface

### Interfaces

#### Detailed Description

Interface for motor speed functions.

## Summary

The Motor speed interface for getting the current references from electric current and rotational speed

The motor speed interface can be implemented by:

- [Motor Speed \(rm\\_motor\\_speed\)](#)

## Data Structures

struct [motor\\_speed\\_callback\\_args\\_t](#)

struct [motor\\_speed\\_position\\_data\\_t](#)

struct [motor\\_speed\\_cfg\\_t](#)

struct [motor\\_speed\\_api\\_t](#)

struct [motor\\_speed\\_instance\\_t](#)

## Typedefs

typedef void [motor\\_speed\\_ctrl\\_t](#)

## Enumerations

enum [motor\\_speed\\_event\\_t](#)

enum [motor\\_speed\\_loop\\_mode\\_t](#)

enum [motor\\_speed\\_step\\_t](#)

## Data Structure Documentation

### ◆ [motor\\_speed\\_callback\\_args\\_t](#)

struct <a href="#">motor_speed_callback_args_t</a>		
Callback function parameter data		
Data Fields		
void const *	p_context	Placeholder for user data.
<a href="#">motor_speed_event_t</a>	event	

### ◆ [motor\\_speed\\_position\\_data\\_t](#)

struct <a href="#">motor_speed_position_data_t</a>		
Motor speed and position structure		
Data Fields		
<a href="#">motor_speed_step_t</a>	e_step_mode	Select step mode.
<a href="#">motor_speed_loop_mode_t</a>	e_loop_mode	Select control mode.
int16_t	position_reference_degree	Position reference [degree].

### ◆ [motor\\_speed\\_cfg\\_t](#)

struct <a href="#">motor_speed_cfg_t</a>		
Configuration parameters.		

Data Fields	
motor_speed_input_t *	st_input
	Input data structure for automatic set.
motor_speed_output_t *	st_output
	Output data structure for automatic receive.
motor_position_instance_t const *	p_position_instance
	Position module instance.
void const *	p_context
	Placeholder for user data.

#### ◆ motor\_speed\_api\_t

struct motor_speed_api_t	
Functions implemented at the HAL layer will follow these APIs.	
Data Fields	
fsp_err_t(*	open )(motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)
fsp_err_t(*	close )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*	reset )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*	run )(motor_speed_ctrl_t *const p_ctrl)
fsp_err_t(*	speedReferenceSet )(motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm)
fsp_err_t(*	positionReferenceSet )(motor_speed_ctrl_t *const p_ctrl, motor_speed_position_data_t const *const p_position_data)

<code>fsp_err_t(*</code>	<code>parameterSet )(motor_speed_ctrl_t *const p_ctrl, motor_speed_input_t const *const p_st_input)</code>
<code>fsp_err_t(*</code>	<code>speedControl )(motor_speed_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>parameterGet )(motor_speed_ctrl_t *const p_ctrl, motor_speed_output_t *const p_st_output)</code>
<code>fsp_err_t(*</code>	<code>parameterUpdate )(motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)</code>

## Field Documentation

### ◆ open

`fsp_err_t(* motor_speed_api_t::open) (motor_speed_ctrl_t *const p_ctrl, motor_speed_cfg_t const *const p_cfg)`

Initialize the motor speed module.

### Implemented as

- `RM_MOTOR_SPEED_Open()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
[in]	<code>p_cfg</code>	Pointer to configuration structure.

### ◆ close

`fsp_err_t(* motor_speed_api_t::close) (motor_speed_ctrl_t *const p_ctrl)`

Close (Finish) the motor speed module.

### Implemented as

- `RM_MOTOR_SPEED_Close()`

### Parameters

[in]	<code>p_ctrl</code>	Pointer to control structure.
------	---------------------	-------------------------------

◆ **reset**

```
fsp_err_t(* motor_speed_api_t::reset) (motor_speed_ctrl_t *const p_ctrl)
```

Reset(Stop) the motor speed module.

**Implemented as**

- RM\_MOTOR\_SPEED\_Reset()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **run**

```
fsp_err_t(* motor_speed_api_t::run) (motor_speed_ctrl_t *const p_ctrl)
```

Activate the motor speed control.

**Implemented as**

- RM\_MOTOR\_SPEED\_Run()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **speedReferenceSet**

```
fsp_err_t(* motor_speed_api_t::speedReferenceSet) (motor_speed_ctrl_t *const p_ctrl, float const speed_reference_rpm)
```

Set (Input) speed reference into the motor speed module.

**Implemented as**

- RM\_MOTOR\_SPEED\_SpeedReferenceSet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	speed_refernce_rpm	Speed reference [rpm]

### ◆ positionReferenceSet

```
fsp_err_t(* motor_speed_api_t::positionReferenceSet) (motor_speed_ctrl_t *const p_ctrl,
motor_speed_position_data_t const *const p_position_data)
```

Set (Input) position reference and control mode

#### Implemented as

- RM\_MOTOR\_SPEED\_PositionReferenceSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_position_data	Pointer to structure position data

### ◆ parameterSet

```
fsp_err_t(* motor_speed_api_t::parameterSet) (motor_speed_ctrl_t *const p_ctrl,
motor_speed_input_t const *const p_st_input)
```

Set (Input) speed parameters into the motor speed module.

#### Implemented as

- RM\_MOTOR\_SPEED\_ParameterSet()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
[in]	p_st_input	Pointer to structure to input parameters.

### ◆ speedControl

```
fsp_err_t(* motor_speed_api_t::speedControl) (motor_speed_ctrl_t *const p_ctrl)
```

Calculate current reference

#### Implemented as

- RM\_MOTOR\_SPEED\_SpeedControl()

#### Parameters

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **parameterGet**

```
fsp_err_t(* motor_speed_api_t::parameterGet) (motor_speed_ctrl_t *const p_ctrl,
motor_speed_output_t *const p_st_output)
```

Get speed control output parameters

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_ParameterGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_st_output	Pointer to get speed control parameters

◆ **parameterUpdate**

```
fsp_err_t(* motor_speed_api_t::parameterUpdate) (motor_speed_ctrl_t *const p_ctrl,
motor_speed_cfg_t const *const p_cfg)
```

Update Parameters for the calculation in the motor speed module.

**Implemented as**

- [RM\\_MOTOR\\_SPEED\\_ParameterUpdate\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure include update parameters.

◆ **motor\_speed\_instance\_t**

```
struct motor_speed_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

motor_speed_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
motor_speed_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
motor_speed_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**

◆ **motor\_speed\_ctrl\_t**typedef void [motor\\_speed\\_ctrl\\_t](#)

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [motor\\_speed\\_ctrl\\_t](#)

**Enumeration Type Documentation**◆ **motor\_speed\_event\_t**enum [motor\\_speed\\_event\\_t](#)

Events that can trigger a callback function

## Enumerator

MOTOR_SPEED_EVENT_FORWARD	Event forward speed control.
MOTOR_SPEED_EVENT_BACKWARD	Event backward speed control.
MOTOR_SPEED_EVENT_ENCODER_CYCLIC	Event encoder cyclic.
MOTOR_SPEED_EVENT_ENCODER_ADJUST	Event encoder adjust.

◆ **motor\_speed\_loop\_mode\_t**enum [motor\\_speed\\_loop\\_mode\\_t](#)

## Enumerator

MOTOR_SPEED_LOOP_MODE_SPEED	Speed control mode.
MOTOR_SPEED_LOOP_MODE_POSITION	Position control mode.

◆ **motor\_speed\_step\_t**enum [motor\\_speed\\_step\\_t](#)

## Enumerator

MOTOR_SPEED_STEP_DISABLE	Position control works without step mode.
MOTOR_SPEED_STEP_ENABLE	Position control works with step mode.

## 4.3.62 Touch Middleware Interface

### Interfaces

#### Detailed Description

Interface for Touch Middleware functions.

## Summary

The TOUCH interface provides TOUCH functionality.

The TOUCH interface can be implemented by:

- [Capacitive Touch Middleware \(rm\\_touch\)](#)

#### Data Structures

struct [touch\\_button\\_cfg\\_t](#)

struct [touch\\_slider\\_cfg\\_t](#)

struct [touch\\_wheel\\_cfg\\_t](#)

struct [touch\\_pad\\_cfg\\_t](#)

struct [touch\\_cfg\\_t](#)

struct [touch\\_api\\_t](#)

struct [touch\\_instance\\_t](#)

#### Macros

#define [TOUCH\\_COUNT\\_MAX](#)  
Value of Maximum count.

#define [TOUCH\\_OFF\\_VALUE](#)  
Value of Non-touch.

#### Typedefs

typedef void [touch\\_ctrl\\_t](#)

typedef struct [touch\\_callback\\_args\\_t](#)  
st\_ctsu\_callback\_args

## Data Structure Documentation

### ◆ touch\_button\_cfg\_t

struct touch_button_cfg_t		
Configuration of each button		
Data Fields		
uint8_t	elem_index	Element number used by this button.
uint16_t	threshold	Touch/non-touch judgment threshold.
uint16_t	hysteresis	Threshold hysteresis for chattering prevention.

### ◆ touch\_slider\_cfg\_t

struct touch_slider_cfg_t		
Configuration of each slider		
Data Fields		
uint8_t const *	p_elem_index	Element number array used by this slider.
uint8_t	num_elements	Number of elements used by this slider.
uint16_t	threshold	Position calculation start threshold value.

### ◆ touch\_wheel\_cfg\_t

struct touch_wheel_cfg_t		
Configuration of each wheel		
Data Fields		
uint8_t const *	p_elem_index	Element number array used by this wheel.
uint8_t	num_elements	Number of elements used by this wheel.
uint16_t	threshold	Position calculation start threshold value.

### ◆ touch\_pad\_cfg\_t

struct touch_pad_cfg_t		
Configuration of each pads		
Data Fields		

uint8_t const *	p_elem_index_rx	RX of element number arrays used by this pad.
uint8_t const *	p_elem_index_tx	TX of element number arrays used by this pad.
uint8_t	num_elements	Number of elements used by this pad.
uint16_t	threshold	Coordinate calculation threshold value.
uint16_t	rx_pixel	rx coordinate resolution
uint16_t	tx_pixel	tx coordinate resolution
uint8_t	max_touch	Maximum number of touch judgments used by the pad.
uint8_t	num_drift	Number of pad drift.

#### ◆ touch\_cfg\_t

struct touch_cfg_t		
User configuration structure, used in open function		
Data Fields		
touch_button_cfg_t const *	p_buttons	Pointer to array of button configuration.
touch_slider_cfg_t const *	p_sliders	Pointer to array of slider configuration.
touch_wheel_cfg_t const *	p_wheels	Pointer to array of wheel configuration.
touch_pad_cfg_t const *	p_pad	Pointer of pad configuration.
uint8_t	num_buttons	Number of buttons.
uint8_t	num_sliders	Number of sliders.
uint8_t	num_wheels	Number of wheels.
uint8_t	on_freq	The cumulative number of determinations of ON.
uint8_t	off_freq	The cumulative number of determinations of OFF.
uint16_t	drift_freq	Base value drift frequency. [0 : no use].
uint16_t	cancel_freq	Maximum continuous ON. [0 : no use].
uint8_t	number	Configuration number for QE monitor.
ctsu_instance_t const *	p_ctsu_instance	Pointer to CTSU instance.
uart_instance_t const *	p_uart_instance	Pointer to UART instance.

void const *	p_context	User defined context passed into callback function.
void const *	p_extend	Pointer to extended configuration by instance of interface.

### ◆ touch\_api\_t

struct touch_api_t	
Functions implemented at the HAL layer will follow this API.	
<b>Data Fields</b>	
fsp_err_t(*)	open )(touch_ctrl_t *const p_ctrl, touch_cfg_t const *const p_cfg)
fsp_err_t(*)	scanStart )(touch_ctrl_t *const p_ctrl)
fsp_err_t(*)	dataGet )(touch_ctrl_t *const p_ctrl, uint64_t *p_button_status, uint16_t *p_slider_position, uint16_t *p_wheel_position)
fsp_err_t(*)	padDataGet )(touch_ctrl_t *const p_ctrl, uint16_t *p_pad_rx_coordinate, uint16_t *p_pad_tx_coordinate, uint8_t *p_pad_num_touch)
fsp_err_t(*)	callbackSet )(touch_ctrl_t *const p_api_ctrl, void(*p_callback)(touch_callback_args_t *), void const *const p_context, touch_callback_args_t *const p_callback_memory)
fsp_err_t(*)	close )(touch_ctrl_t *const p_ctrl)
<b>Field Documentation</b>	

◆ **open**

```
fsp_err_t(* touch_api_t::open) (touch_ctrl_t *const p_ctrl, touch_cfg_t const *const p_cfg)
```

Open driver.

**Implemented as**

- RM\_TOUCH\_Open()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **scanStart**

```
fsp_err_t(* touch_api_t::scanStart) (touch_ctrl_t *const p_ctrl)
```

Scan start.

**Implemented as**

- RM\_TOUCH\_ScanStart()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **dataGet**

```
fsp_err_t(* touch_api_t::dataGet) (touch_ctrl_t *const p_ctrl, uint64_t *p_button_status, uint16_t *p_slider_position, uint16_t *p_wheel_position)
```

Data get.

**Implemented as**

- RM\_TOUCH\_DataGet()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_button_status	Pointer to get data bitmap.
[out]	p_slider_position	Pointer to get data array.
[out]	p_wheel_position	Pointer to get data array.

◆ **padDataGet**

```
fsp_err_t(* touch_api_t::padDataGet) (touch_ctrl_t *const p_ctrl, uint16_t *p_pad_rx_coordinate,
uint16_t *p_pad_tx_coordinate, uint8_t *p_pad_num_touch)
```

pad data get.

**Implemented as**

- [RM\\_TOUCH\\_PadDataGet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[out]	p_pad_rx_coordinate	Pointer to get coordinate of receiver side.
[out]	p_pad_tx_coordinate	Pointer to get coordinate of transmitter side.
[out]	p_pad_num_touch	Pointer to get touch count.

◆ **callbackSet**

```
fsp_err_t(* touch_api_t::callbackSet) (touch_ctrl_t *const p_api_ctrl,
void(*p_callback)(touch_callback_args_t *), void const *const p_context, touch_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- [RM\\_TOUCH\\_CallbackSet\(\)](#)

**Parameters**

[in]	p_ctrl	Pointer to the CTSU control block.
[in]	p_callback	Callback function
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* touch_api_t::close) (touch_ctrl_t *const p_ctrl)
```

Close driver.

**Implemented as**

- RM\_TOUCH\_Close()

**Parameters**

[in]	p_ctrl	Pointer to control structure.
------	--------	-------------------------------

◆ **touch\_instance\_t**

```
struct touch_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

touch_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
touch_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
touch_api_t const *	p_api	Pointer to the API structure for this instance.

**Typedef Documentation**◆ **touch\_ctrl\_t**

```
typedef void touch_ctrl_t
```

Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- touch\_instance\_ctrl\_t

◆ **touch\_callback\_args\_t**

```
typedef struct st_ctsu_callback_args touch_callback_args_t
```

Callback function parameter data

**4.3.63 Virtual EEPROM Interface**

## Interfaces

## Detailed Description

Interface for Virtual EEPROM access.

## Summary

The Virtual EEPROM Port configures a fail-safe key value store designed for microcontrollers on top of a lower level storage device.

Implemented by: [Virtual EEPROM \(rm\\_vee\\_flash\)](#)

### Data Structures

struct [rm\\_vee\\_callback\\_args\\_t](#)

struct [rm\\_vee\\_cfg\\_t](#)

struct [rm\\_vee\\_api\\_t](#)

struct [rm\\_vee\\_instance\\_t](#)

### Typedefs

typedef void [rm\\_vee\\_ctrl\\_t](#)

### Enumerations

enum [rm\\_vee\\_state\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_vee\\_callback\\_args\\_t](#)

struct <a href="#">rm_vee_callback_args_t</a>		
User configuration structure, used in open function		
Data Fields		
<a href="#">rm_vee_state_t</a>	state	State of the Virtual EEPROM.
void const *	p_context	Placeholder for user data. Set in <a href="#">rm_vee_api_t::open</a> function in:: <a href="#">rm_vee_cfg_t</a> .

### ◆ [rm\\_vee\\_cfg\\_t](#)

struct <a href="#">rm_vee_cfg_t</a>	
User configuration structure, used in open function	
<b>Data Fields</b>	
uint32_t	<a href="#">start_addr</a>

	Start address to be used for Virtual EEPROM memory.
uint32_t	<a href="#">num_segments</a>
	Number of segments to divide the volume into.
uint32_t	<a href="#">total_size</a>
	Total size of the volume.
uint32_t	<a href="#">ref_data_size</a>
	Size of the reference data stored at the end of the segment.
uint32_t	<a href="#">record_max_id</a>
	Maximum record ID that can be used.
uint16_t *	<a href="#">rec_offset</a>
	Pointer to buffer used for record offset caching.
void(*	<a href="#">p_callback</a> )(rm_vee_callback_args_t *p_args)
	Callback provided when a Virtual EEPROM event occurs.
void const *	<a href="#">p_context</a>
	Placeholder for user data.
void const *	<a href="#">p_extend</a>
	Pointer to hardware dependent configuration.

◆ **rm\_vee\_api\_t**

```
struct rm_vee_api_t
```

Virtual EEPROM interface API.

### Data Fields

<code>fsp_err_t(*</code>	<code>open )(rm_vee_ctrl_t *const p_ctrl, rm_vee_cfg_t const *const p_cfg)</code>
<code>fsp_err_t(*</code>	<code>recordWrite )(rm_vee_ctrl_t *const p_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t num_bytes)</code>
<code>fsp_err_t(*</code>	<code>recordPtrGet )(rm_vee_ctrl_t *const p_ctrl, uint32_t rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)</code>
<code>fsp_err_t(*</code>	<code>refDataWrite )(rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)</code>
<code>fsp_err_t(*</code>	<code>refDataPtrGet )(rm_vee_ctrl_t *const p_ctrl, uint8_t **const pp_ref_data)</code>
<code>fsp_err_t(*</code>	<code>statusGet )(rm_vee_ctrl_t *const p_ctrl, rm_vee_status_t *const p_status)</code>
<code>fsp_err_t(*</code>	<code>refresh )(rm_vee_ctrl_t *const p_ctrl)</code>
<code>fsp_err_t(*</code>	<code>format )(rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)</code>
<code>fsp_err_t(*</code>	<code>callbackSet )(rm_vee_ctrl_t *const p_api_ctrl, void(*p_callback)(rm_vee_callback_args_t *), void const *const p_context, rm_vee_callback_args_t *const p_callback_memory)</code>
<code>fsp_err_t(*</code>	<code>close )(rm_vee_ctrl_t *const p_ctrl)</code>

### Field Documentation

◆ **open**

```
fsp_err_t(* rm_vee_api_t::open) (rm_vee_ctrl_t *const p_ctrl, rm_vee_cfg_t const *const p_cfg)
```

Initializes the driver's internal structures and opens the Flash driver.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_Open](#)

**Parameters**

[in]	p_ctrl	Pointer to control block. Must be declared by user. Elements set here.
[in]	p_cfg	Pointer to configuration structure. All elements of this structure must be set by user.

◆ **recordWrite**

```
fsp_err_t(* rm_vee_api_t::recordWrite) (rm_vee_ctrl_t *const p_ctrl, uint32_t const rec_id, uint8_t const *const p_rec_data, uint32_t num_bytes)
```

Writes a record to data flash.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RecordWrite](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	rec_id	ID of record to write.
[in]	p_rec_data	Pointer to record data to write.
[in]	num_bytes	Length of data to write.

## ◆ recordPtrGet

```
fsp_err_t(* rm_vee_api_t::recordPtrGet) (rm_vee_ctrl_t *const p_ctrl, uint32_t rec_id, uint8_t **const pp_rec_data, uint32_t *const p_num_bytes)
```

This function gets the pointer to the most recent version of a record specified by ID.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RecordPtrGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	rec_id	ID of record to locate.
[in]	pp_rec_data	Pointer to set to the most recent version of the record.
[in]	p_num_bytes	Variable to load with record length.

## ◆ refDataWrite

```
fsp_err_t(* rm_vee_api_t::refDataWrite) (rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)
```

Writes new Reference data to the reference update area.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RefDataWrite](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_ref_data	Pointer to data to write to the reference data update area.

## ◆ refDataPtrGet

```
fsp_err_t(* rm_vee_api_t::refDataPtrGet) (rm_vee_ctrl_t *const p_ctrl, uint8_t **const pp_ref_data)
```

Gets a pointer to the most recent reference data.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_RefDataPtrGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	pp_ref_data	Pointer to set to the most recent valid reference data.

◆ **statusGet**

```
fsp_err_t(* rm_vee_api_t::statusGet) (rm_vee_ctrl_t *const p_ctrl, rm_vee_status_t *const p_status)
```

Get the current status of the VEE driver.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_StatusGet](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_status	Pointer to store the current status of the VEE driver.

◆ **refresh**

```
fsp_err_t(* rm_vee_api_t::refresh) (rm_vee_ctrl_t *const p_ctrl)
```

Manually start a refresh operation.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_Refresh](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
------	--------	---------------------------

◆ **format**

```
fsp_err_t(* rm_vee_api_t::format) (rm_vee_ctrl_t *const p_ctrl, uint8_t const *const p_ref_data)
```

Format the Virtual EEPROM.

**Implemented as**

- [RM\\_VEE\\_FLASH\\_Format](#)

**Parameters**

[in]	p_ctrl	Pointer to control block.
[in]	p_ref_data	Optional pointer to reference data to write during format.

◆ **callbackSet**

```
fsp_err_t(* rm_vee_api_t::callbackSet) (rm_vee_ctrl_t *const p_api_ctrl,
void(*p_callback)(rm_vee_callback_args_t*), void const *const p_context, rm_vee_callback_args_t
*const p_callback_memory)
```

Specify callback function and optional context pointer and working memory pointer.

**Implemented as**

- RM\_VEE\_FLASH\_CallbackSet()

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_vee_api_t::open</a> call.
[in]	p_callback	Callback function to register
[in]	p_context	Pointer to send to callback function
[in]	p_working_memory	Pointer to volatile memory where callback structure can be allocated. Callback arguments allocated here are only valid during the callback.

◆ **close**

```
fsp_err_t(* rm_vee_api_t::close) (rm_vee_ctrl_t *const p_ctrl)
```

Closes the module and lower level storage device.

**Implemented as**

- RM\_VEE\_FLASH\_Close

**Parameters**

[in]	p_ctrl	Control block set in <a href="#">rm_vee_api_t::open</a> call.
------	--------	---

◆ **rm\_vee\_instance\_t**

```
struct rm_vee_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

## Data Fields

<a href="#">rm_vee_ctrl_t</a> *	p_ctrl	Pointer to the control structure for this instance.
<a href="#">rm_vee_cfg_t</a> const *	p_cfg	Pointer to the configuration structure for this instance.
<a href="#">rm_vee_api_t</a> const *	p_api	Pointer to the API structure for

		this instance.
--	--	----------------

## Typedef Documentation

### ◆ `rm_vee_ctrl_t`

```
typedef void rm_vee_ctrl_t
```

Virtual EEPROM API control block. Allocate an instance specific control block to pass into the VEE API calls.

#### Implemented as

- `rm_vee_flash_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `rm_vee_state_t`

```
enum rm_vee_state_t
```

#### Enumerator

<code>RM_VEE_STATE_READY</code>	Ready.
<code>RM_VEE_STATE_BUSY</code>	Operation in progress.
<code>RM_VEE_STATE_REFRESH</code>	Refresh operation in progress.
<code>RM_VEE_STATE_OVERFLOW</code>	The amount of data written exceeds the space available.
<code>RM_VEE_STATE_HARDWARE_FAIL</code>	Lower level hardware failure.

## 4.3.64 ZMOD4XXX Middleware Interface

### Interfaces

#### Detailed Description

Interface for ZMOD4XXX Middleware functions.

## Summary

The ZMOD4XXX interface provides ZMOD4XXX functionality.

The ZMOD4XXX interface can be implemented by:

- ZMOD4XXX Sensor Middleware (rm\_zmod4xxx)

## Data Structures

struct [rm\\_zmod4xxx\\_callback\\_args\\_t](#)

struct [rm\\_zmod4xxx\\_raw\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_iaq\\_1st\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_iaq\\_2nd\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_odor\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_sulfur\\_odor\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_oaq\\_1st\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_oaq\\_2nd\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_cfg\\_t](#)

struct [rm\\_zmod4xxx\\_api\\_t](#)

struct [rm\\_zmod4xxx\\_instance\\_t](#)

## Typedefs

typedef void [rm\\_zmod4xxx\\_ctrl\\_t](#)

## Enumerations

enum [rm\\_zmod4xxx\\_event\\_t](#)

enum [rm\\_zmod4xxx\\_sulfur\\_odor\\_t](#)

## Data Structure Documentation

### ◆ [rm\\_zmod4xxx\\_callback\\_args\\_t](#)

struct [rm\\_zmod4xxx\\_callback\\_args\\_t](#)

ZMOD4XXX sensor API callback parameter definition

### ◆ [rm\\_zmod4xxx\\_raw\\_data\\_t](#)

struct [rm\\_zmod4xxx\\_raw\\_data\\_t](#)

ZMOD4XXX raw data structure

### ◆ [rm\\_zmod4xxx\\_iaq\\_1st\\_data\\_t](#)

struct rm_zmod4xxx_iaq_1st_data_t		
ZMOD4XXX IAQ 1st gen data structure		
Data Fields		
float	rmox	MOx resistance.
float	rcda	CDA resistance.
float	iaq	IAQ index.
float	tvoc	TVOC concentration (mg/m <sup>3</sup> ).
float	etoh	EtOH concentration (ppm).
float	eco2	eCO2 concentration (ppm).

◆ **rm\_zmod4xxx\_iaq\_2nd\_data\_t**

struct rm_zmod4xxx_iaq_2nd_data_t		
ZMOD4XXX IAQ 2nd gen data structure		
Data Fields		
float	rmox[13]	MOx resistance.
float	log_rcda	log10 of CDA resistance.
float	iaq	IAQ index.
float	tvoc	TVOC concentration (mg/m <sup>3</sup> ).
float	etoh	EtOH concentration (ppm).
float	eco2	eCO2 concentration (ppm).

◆ **rm\_zmod4xxx\_odor\_data\_t**

struct rm_zmod4xxx_odor_data_t		
ZMOD4XXX Odor structure		
Data Fields		
bool	control_signal	Control signal input for odor lib.
float	odor	Concentration ratio for odor lib.

◆ **rm\_zmod4xxx\_sulfur\_odor\_data\_t**

struct rm_zmod4xxx_sulfur_odor_data_t		
ZMOD4XXX Sulfur-Odor structure		
Data Fields		
float	rmox[9]	MOx resistance.
float	intensity	odor intensity rating ranges from 0.0 to 5.0 for sulfur lib
<a href="#">rm_zmod4xxx_sulfur_odor_t</a>	odor	sulfur_odor classification for lib

◆ **rm\_zmod4xxx\_oaq\_1st\_data\_t**

struct rm_zmod4xxx_oaq_1st_data_t		
ZMOD4XXX OAQ 1st gen data structure		
Data Fields		
float	rmox[15]	MOx resistance.
float	aiq	Air Quality.

◆ **rm\_zmod4xxx\_oaq\_2nd\_data\_t**

struct rm_zmod4xxx_oaq_2nd_data_t		
ZMOD4XXX OAQ 2nd gen data structure		
Data Fields		
float	rmox[8]	MOx resistance.
float	ozone_concentration	The ozone concentration in part-per-billion.
uint16_t	fast_aqi	1-minute average of the Air Quality Index according to the EPA standard based on ozone
uint16_t	epa_aqi	The Air Quality Index according to the EPA standard based on ozone.

◆ **rm\_zmod4xxx\_cfg\_t**

struct rm_zmod4xxx_cfg_t	
ZMOD4XXX configuration block	
<b>Data Fields</b>	
rm_comms_instance_t const *	p_comms_instance
	Pointer to Communications Middleware instance.
void const *	p_timer_instance
	Pointer to Timer driver instance.
void const *	p_irq_instance
	Pointer to IRQ instance.
void const *	p_zmod4xxx_device

	Pointer to ZMOD4XXX device structure.
void const *	<a href="#">p_zmod4xxx_handle</a>
	Pointer to ZMOD4XXX library handler.
void const *	<a href="#">p_zmod4xxx_results</a>
	Pointer to ZMOD4XXX library results.
void const *	<a href="#">p_context</a>
	Pointer to the user-provided context.
void const *	<a href="#">p_extend</a>
	Pointer to extended configuration by instance of interface.
void(*	<a href="#">p_comms_callback</a> )(rm_zmod4xxx_callback_args_t *p_args)
	I2C Communications callback.
void(*	<a href="#">p_irq_callback</a> )(rm_zmod4xxx_callback_args_t *p_args)
	IRQ callback.

#### ◆ rm\_zmod4xxx\_api\_t

struct rm_zmod4xxx_api_t	
ZMOD4XXX APIs	
<b>Data Fields</b>	
fsp_err_t(*	<a href="#">open</a> )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_cfg_t const *const p_cfg)
fsp_err_t(*	<a href="#">measurementStart</a> )(rm_zmod4xxx_ctrl_t *const p_api_ctrl)

fsp_err_t(*)	measurementStop )(rm_zmod4xxx_ctrl_t *const p_api_ctrl)
fsp_err_t(*)	statusCheck )(rm_zmod4xxx_ctrl_t *const p_api_ctrl)
fsp_err_t(*)	read )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data)
fsp_err_t(*)	iaq1stGenDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_1st_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	iaq2ndGenDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_2nd_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	odorDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_odor_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	sulfurOdorDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_sulfur_odor_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	oaq1stGenDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_1st_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	oaq2ndGenDataCalculate )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_2nd_data_t *const p_zmod4xxx_data)
fsp_err_t(*)	temperatureAndHumiditySet )(rm_zmod4xxx_ctrl_t *const p_api_ctrl, float temperature, float humidity)
fsp_err_t(*)	close )(rm_zmod4xxx_ctrl_t *const p_api_ctrl)

## Field Documentation

◆ **open**

```
fsp_err_t(* rm_zmod4xxx_api_t::open) (rm_zmod4xxx_ctrl_t *const p_api_ctrl, rm_zmod4xxx_cfg_t
const *const p_cfg)
```

Open sensor.

**Implemented as**

- [RM\\_ZMOD4XXX\\_Open\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to configuration structure.

◆ **measurementStart**

```
fsp_err_t(* rm_zmod4xxx_api_t::measurementStart) (rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

Start measurement

**Implemented as**

- [RM\\_ZMOD4XXX\\_MeasurementStart\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **measurementStop**

```
fsp_err_t(* rm_zmod4xxx_api_t::measurementStop) (rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

Stop measurement

**Implemented as**

- [RM\\_ZMOD4XXX\\_MeasurementStop\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **statusCheck**

```
fsp_err_t(* rm_zmod4xxx_api_t::statusCheck) (rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

Read status of the sensor

**Implemented as**

- [RM\\_ZMOD4XXX\\_StatusCheck\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

◆ **read**

```
fsp_err_t(* rm_zmod4xxx_api_t::read) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,  
rm_zmod4xxx_raw_data_t *const p_raw_data)
```

Read ADC data.

**Implemented as**

- [RM\\_ZMOD4XXX\\_Read\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data structure.

◆ **iaq1stGenDataCalculate**

```
fsp_err_t(* rm_zmod4xxx_api_t::iaq1stGenDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,  
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_1st_data_t *const  
p_zmod4xxx_data)
```

Calculate IAQ 1st Gen. values from ADC data.

**Implemented as**

- [RM\\_ZMOD4XXX\\_Iaq1stGenDataCalculate\(\)](#)

**Parameters**

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXXX data structure.

### ◆ iaq2ndGenDataCalculate

```
fsp_err_t(* rm_zmod4xxx_api_t::iaq2ndGenDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_iaq_2nd_data_t *const
p_zmod4xxx_data)
```

Calculate IAQ 2nd Gen. values from ADC data.

#### Implemented as

- RM\_ZMOD4XXX\_Iaq2ndGenDataCalculate()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXX data structure.

### ◆ odorDataCalculate

```
fsp_err_t(* rm_zmod4xxx_api_t::odorDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_odor_data_t *const p_zmod4xxx_data)
```

Calculate Odor values from ADC data.

#### Implemented as

- RM\_ZMOD4XXX\_OdorDataCalculate()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXX data structure.

### ◆ sulfurOdorDataCalculate

```
fsp_err_t(* rm_zmod4xxx_api_t::sulfurOdorDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_sulfur_odor_data_t *const
p_zmod4xxx_data)
```

Calculate Sulfur Odor values from ADC data.

#### Implemented as

- RM\_ZMOD4XXX\_SulfurOdorDataCalculate()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXX data structure.

### ◆ oaq1stGenDataCalculate

```
fsp_err_t(* rm_zmod4xxx_api_t::oaq1stGenDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_1st_data_t *const
p_zmod4xxx_data)
```

Calculate OAQ 1st Gen. values from ADC data.

#### Implemented as

- RM\_ZMOD4XXX\_Oaq1stGenDataCalculate()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXX data structure.

### ◆ oaq2ndGenDataCalculate

```
fsp_err_t(* rm_zmod4xxx_api_t::oaq2ndGenDataCalculate) (rm_zmod4xxx_ctrl_t *const p_api_ctrl,
rm_zmod4xxx_raw_data_t *const p_raw_data, rm_zmod4xxx_oaq_2nd_data_t *const
p_zmod4xxx_data)
```

Calculate OAQ 2nd Gen. values from ADC data.

#### Implemented as

- RM\_ZMOD4XXX\_Oaq2ndGenDataCalculate()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	p_raw_data	Pointer to raw data.
[in]	p_zmod4xxx_data	Pointer to ZMOD4XXX data structure.

### ◆ temperatureAndHumiditySet

```
fsp_err_t(* rm_zmod4xxx_api_t::temperatureAndHumiditySet) (rm_zmod4xxx_ctrl_t *const
p_api_ctrl, float temperature, float humidity)
```

Set temperature and humidity.

#### Implemented as

- RM\_ZMOD4XXX\_TemperatureAndHumiditySet()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
[in]	temperature	Temperature (deg C).
[in]	humidity	Humidity (percent).

### ◆ close

```
fsp_err_t(* rm_zmod4xxx_api_t::close) (rm_zmod4xxx_ctrl_t *const p_api_ctrl)
```

Close the sensor

#### Implemented as

- RM\_ZMOD4XXX\_Close()

#### Parameters

[in]	p_api_ctrl	Pointer to control structure.
------	------------	-------------------------------

### ◆ rm\_zmod4xxx\_instance\_t

```
struct rm_zmod4xxx_instance_t
```

ZMOD4XXX instance

Data Fields		
<code>rm_zmod4xxx_ctrl_t *</code>	<code>p_ctrl</code>	Pointer to the control structure for this instance
<code>rm_zmod4xxx_cfg_t const *</code>	<code>p_cfg</code>	Pointer to the configuration structure for this instance
<code>rm_zmod4xxx_api_t const *</code>	<code>p_api</code>	Pointer to the API structure for this instance

## Typedef Documentation

### ◆ `rm_zmod4xxx_ctrl_t`

```
typedef void rm_zmod4xxx_ctrl_t
```

ZMOD4xxx Control block. Allocate an instance specific control block to pass into the API calls.

#### Implemented as

- `rm_zmod4xxx_instance_ctrl_t`

## Enumeration Type Documentation

### ◆ `rm_zmod4xxx_event_t`

```
enum rm_zmod4xxx_event_t
```

Event in the callback function

### ◆ `rm_zmod4xxx_sulfur_odor_t`

```
enum rm_zmod4xxx_sulfur_odor_t
```

Sulfur-Odor status

## 4.3.65 SCE Interface

### Interfaces

#### Detailed Description

Interface for Secure Crypto Engine (SCE) functions.

## Summary

The SCE interface provides SCE functionality.

The SCE interface can be implemented by:

- [Secure Crypto Engine \(r\\_sce\\_protected\)](#)

## Data Structures

struct [sce\\_byte\\_data\\_t](#)

struct [sce\\_aes\\_wrapped\\_key\\_t](#)

struct [sce\\_hmac\\_sha\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa1024\\_public\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa1024\\_private\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa2048\\_public\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa2048\\_private\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa3072\\_public\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa4096\\_public\\_wrapped\\_key\\_t](#)

struct [sce\\_rsa1024\\_wrapped\\_pair\\_key\\_t](#)

struct [sce\\_rsa2048\\_wrapped\\_pair\\_key\\_t](#)

struct [sce\\_ecc\\_public\\_wrapped\\_key\\_t](#)

struct [sce\\_ecc\\_private\\_wrapped\\_key\\_t](#)

struct [sce\\_ecc\\_wrapped\\_pair\\_key\\_t](#)

struct [sce\\_ecdh\\_wrapped\\_key\\_t](#)

struct [sce\\_key\\_update\\_key\\_t](#)

struct [sce\\_aes\\_handle\\_t](#)

struct [sce\\_gcm\\_handle\\_t](#)

struct [sce\\_ccm\\_handle\\_t](#)

struct [sce\\_cmac\\_handle\\_t](#)

struct [sce\\_sha\\_md5\\_handle\\_t](#)

struct [sce\\_hmac\\_sha\\_handle\\_t](#)

struct [sce\\_ecdh\\_handle\\_t](#)

struct [sce\\_cfg\\_t](#)

struct [sce\\_api\\_t](#)

struct [sce\\_instance\\_t](#)

## Typedefs

typedef [sce\\_byte\\_data\\_t](#) [sce\\_rsa\\_byte\\_data\\_t](#)  
byte data [More...](#)

typedef [sce\\_byte\\_data\\_t](#) [sce\\_ecdsa\\_byte\\_data\\_t](#)  
byte data [More...](#)

typedef void [sce\\_ctrl\\_t](#)

## Enumerations

enum [lifecycle\\_t](#)

## Data Structure Documentation

### ◆ [sce\\_byte\\_data\\_t](#)

struct <a href="#">sce_byte_data_t</a>		
Byte data structure		
Data Fields		
<a href="#">uint8_t</a> *	<a href="#">pdata</a>	pointer
<a href="#">uint32_t</a>	<a href="#">data_length</a>	<a href="#">data_length</a>
<a href="#">uint32_t</a>	<a href="#">data_type</a>	data type

### ◆ [sce\\_aes\\_wrapped\\_key\\_t](#)

struct <a href="#">sce_aes_wrapped_key_t</a>		
AES wrapped key data structure. DO NOT MODIFY.		
Data Fields		
<a href="#">uint32_t</a>	<a href="#">type</a>	key type
<a href="#">uint32_t</a>	<a href="#">value[HW_SCE_AES256_KEY_IN_DEX_WORD_SIZE]</a>	wrapped key value

◆ **sce\_hmac\_sha\_wrapped\_key\_t**

struct sce_hmac_sha_wrapped_key_t		
HMAC-SHA wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	key type
uint32_t	value[HW_SCE_HMAC_KEY_INDE X_WORD_SIZE]	wrapped key value

◆ **sce\_rsa1024\_public\_wrapped\_key\_t**

struct sce_rsa1024_public_wrapped_key_t		
RSA 1024bit public wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	key type
struct sce_rsa1024_public_wrapped_k ey_t	value	

◆ **sce\_rsa1024\_private\_wrapped\_key\_t**

struct sce_rsa1024_private_wrapped_key_t		
RSA 1024bit private wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	key type
struct sce_rsa1024_private_wrapped_ key_t	value	

◆ **sce\_rsa2048\_public\_wrapped\_key\_t**

struct sce_rsa2048_public_wrapped_key_t		
RSA 2048bit public wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	Key type.
struct sce_rsa2048_public_wrapped_k ey_t	value	

◆ **sce\_rsa2048\_private\_wrapped\_key\_t**

struct sce_rsa2048_private_wrapped_key_t		
RSA 2048bit private wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	key type

struct sce_rsa2048_private_wrapped_key_t	value	
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#### ◆ sce\_rsa3072\_public\_wrapped\_key\_t

struct sce_rsa3072_public_wrapped_key_t		
RSA 3072bit public wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	Key type.
struct sce_rsa3072_public_wrapped_key_t	value	

#### ◆ sce\_rsa4096\_public\_wrapped\_key\_t

struct sce_rsa4096_public_wrapped_key_t		
RSA 4096bit public wrapped key data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	Key type.
struct sce_rsa4096_public_wrapped_key_t	value	

#### ◆ sce\_rsa1024\_wrapped\_pair\_key\_t

struct sce_rsa1024_wrapped_pair_key_t		
RSA 1024bit wrapped key pair structure. DO NOT MODIFY.		
Data Fields		
sce_rsa1024_private_wrapped_key_t	private	RSA 1024-bit private wrapped key.
sce_rsa1024_public_wrapped_key_t	public	RSA 1024-bit public wrapped key.

#### ◆ sce\_rsa2048\_wrapped\_pair\_key\_t

struct sce_rsa2048_wrapped_pair_key_t		
RSA 2048bit wrapped key pair structure. DO NOT MODIFY.		
Data Fields		
sce_rsa2048_private_wrapped_key_t	private	RSA 2048-bit private wrapped key.
sce_rsa2048_public_wrapped_key_t	public	RSA 2048-bit public wrapped key.

#### ◆ sce\_ecc\_public\_wrapped\_key\_t

--	--	--

struct sce_ecc_public_wrapped_key_t		
ECC P-192/224/256 public wrapped key data structure		
Data Fields		
uint32_t	type	key type
struct sce_ecc_public_wrapped_key_t	value	

◆ **sce\_ecc\_private\_wrapped\_key\_t**

struct sce_ecc_private_wrapped_key_t		
ECC P-192/224/256 private wrapped key data structure		
Data Fields		
uint32_t	type	key type
uint32_t	value[HW_SCE_ECC_PRIVATE_KEY_MANAGEMENT_INFO_WORD_SIZE]	wrapped key value

◆ **sce\_ecc\_wrapped\_pair\_key\_t**

struct sce_ecc_wrapped_pair_key_t		
ECC P-192/224/256 wrapped key pair structure		
Data Fields		
sce_ecc_private_wrapped_key_t	private	ECC private wrapped key.
sce_ecc_public_wrapped_key_t	public	ECC public wrapped key.

◆ **sce\_ecdh\_wrapped\_key\_t**

struct sce_ecdh_wrapped_key_t		
ECDH wrapped key data structure		
Data Fields		
uint32_t	type	key type
uint32_t	value[HW_SCE_SHARED_SECRET_KEY_INDEX_WORD_SIZE]	wrapped key value

◆ **sce\_key\_update\_key\_t**

struct sce_key_update_key_t		
Update key ring index data structure. DO NOT MODIFY.		
Data Fields		
uint32_t	type	key type
uint32_t	value[HW_SCE_UPDATE_KEY_RING_INDEX_WORD_SIZE]	wrapped key value

◆ **sce\_aes\_handle\_t**

struct sce_aes_handle_t		
The work area for AES. DO NOT MODIFY.		
Data Fields		
uint32_t	id	serial number of this handle
sce_aes_wrapped_key_t	wrapped_key	wrapped key
uint32_t	current_input_data_size	text size under encryption / decryption
uint8_t	last_1_block_as_fraction[HW_SCE_AES_BLOCK_BYTE_SIZE]	text array less than the block long
uint8_t	last_2_block_as_fraction[HW_SCE_AES_BLOCK_BYTE_SIZE *2]	reserved
uint8_t	current_initial_vector[HW_SCE_AES_CBC_IV_BYTE_SIZE]	current initialization vector used in CBC mode
uint8_t	flag_call_init	control flag of calling function

## ◆ sce\_gcm\_handle\_t

struct sce_gcm_handle_t		
The work area for GCM. DO NOT MODIFY.		
Data Fields		
uint32_t	id	serial number of this handle
sce_aes_wrapped_key_t	wrapped_key	wrapped key
uint8_t	gcm_buffer[HW_SCE_AES_BLOCK_BYTE_SIZE]	text array less than the block long
uint8_t	gcm_aad_buffer[HW_SCE_AES_GCM_AAD_BLOCK_BYTE_SIZE]	AAD array less than the block long.
uint32_t	all_received_length	entire length of text
uint32_t	all_received_aad_length	entire length of text
uint32_t	buffering_length	text array length less than the block long
uint32_t	buffering_aad_length	AAD array length less than the block long.
uint8_t	flag_call_init	control flag of calling function
uint8_t	flag_update_input_data	control flag of next input data

## ◆ sce\_ccm\_handle\_t

struct sce_ccm_handle_t		
The work area for CCM. DO NOT MODIFY.		
Data Fields		

uint32_t	id	serial number of this handle
<a href="#">sce_aes_wrapped_key_t</a>	wrapped_key	wrapped key
uint8_t	formatted_data[HW_SCE_AES_CCM_B_FORMAT_BYTE_SIZE]	formatted data area
uint8_t	counter[HW_SCE_AES_CCM_COUNTER_BYTE_SIZE]	counter of CTR mode
uint8_t	ccm_buffer[HW_SCE_AES_BLOCK_BYTE_SIZE]	text array less than the block long
uint32_t	all_received_length	entire length of text
uint32_t	buffering_length	text array length less than the block long
uint8_t	flag_call_init	control flag of calling function

◆ **sce\_cmac\_handle\_t**

struct sce_cmac_handle_t		
The work area for CMAC. DO NOT MODIFY.		
Data Fields		
uint32_t	id	serial number of this handle
<a href="#">sce_aes_wrapped_key_t</a>	wrapped_key	wrapped key
uint8_t	cmac_buffer[HW_SCE_AES_BLOCK_BYTE_SIZE]	message array less than the block long
uint32_t	all_received_length	entire length of message
uint32_t	buffering_length	message array length less than the block long
uint8_t	flag_call_init	control flag of calling function

◆ **sce\_sha\_md5\_handle\_t**

struct sce_sha_md5_handle_t		
The work area for SHA. DO NOT MODIFY.		
Data Fields		
uint32_t	id	serial number of this handle
uint8_t	sha_buffer[HW_SCE_SHA256_HASH_LENGTH_BYTE_SIZE * 4]	message array length less than the block long
uint32_t	all_received_length	entire length of message
uint32_t	buffering_length	message array length less than the block long
uint8_t	current_hash[HW_SCE_SHA256_HASH_LENGTH_BYTE_SIZE]	last hash value
uint8_t	flag_call_init	control flag of calling function

◆ **sce\_hmac\_sha\_handle\_t**

struct sce_hmac_sha_handle_t		
The work area for HMAC-SHA. DO NOT MODIFY.		
Data Fields		
uint32_t	id	serial number of this handle
<a href="#">sce_hmac_sha_wrapped_key_t</a>	wrapped_key	wrapped key
uint8_t	hmac_buffer[HW_SCE_SHA256_HASH_LENGTH_BYTE_SIZE *4]	message array length less than the block long
uint32_t	all_received_length	entire length of message
uint32_t	buffering_length	message array length less than the block long
uint8_t	flag_call_init	control flag of calling function

◆ **sce\_ecdh\_handle\_t**

struct sce_ecdh_handle_t		
The work area for ECDH		
Data Fields		
uint32_t	id	serial number of this handle
uint32_t	flag_use_key_id	control frag that the key_id has already used or not
uint32_t	key_id	serial number of the wrapped key
uint32_t	key_type	key type
uint8_t	flag_call_init	control flag of calling function
uint8_t	flag_call_make_public	control flag of calling function
uint8_t	flag_call_read_public	control flag of calling function
uint8_t	flag_call_shared_secret	control flag of calling function

◆ **sce\_cfg\_t**

struct sce_cfg_t		
User configuration structure, used in open function		
Data Fields		
<a href="#">lifecycle_t</a>	lifecycle	Data lifecycle.

◆ **sce\_api\_t**

struct sce_api_t		
Functions implemented at the HAL layer will follow this API.		

Data Fields	
fsp_err_t(*	open )(sce_ctrl_t *const p_ctrl, sce_cfg_t const *const p_cfg)
fsp_err_t(*	close )(sce_ctrl_t *const p_ctrl)
fsp_err_t(*	softwareReset )(void)
fsp_err_t(*	randomNumberGenerate )(uint32_t *random)
fsp_err_t(*	AES128_WrappedKeyGenerate )(sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES256_WrappedKeyGenerate )(sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES128_EncryptedKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES256_EncryptedKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES128ECB_EncryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES128ECB_EncryptUpdate )(sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t(*	AES128ECB_EncryptFinal )(sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)
fsp_err_t(*	AES128ECB_DecryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES128ECB_DecryptUpdate )(sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)

fsp_err_t(*)	AES128ECB_DecryptFinal )(sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)
fsp_err_t(*)	AES256ECB_EncryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*)	AES256ECB_EncryptUpdate )(sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t(*)	AES256ECB_EncryptFinal )(sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)
fsp_err_t(*)	AES256ECB_DecryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*)	AES256ECB_DecryptUpdate )(sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t(*)	AES256ECB_DecryptFinal )(sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)
fsp_err_t(*)	AES128CBC_EncryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)
fsp_err_t(*)	AES128CBC_EncryptUpdate )(sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
fsp_err_t(*)	AES128CBC_EncryptFinal )(sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)
fsp_err_t(*)	AES128CBC_DecryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)
fsp_err_t(*)	AES128CBC_DecryptUpdate )(sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)
fsp_err_t(*)	AES128CBC_DecryptFinal )(sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)

<code>fsp_err_t(*</code>	<code>AES256CBC_EncryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)</code>
<code>fsp_err_t(*</code>	<code>AES256CBC_EncryptUpdate )(sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CBC_EncryptFinal )(sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CBC_DecryptInit )(sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)</code>
<code>fsp_err_t(*</code>	<code>AES256CBC_DecryptUpdate )(sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CBC_DecryptFinal )(sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_EncryptInit )(sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_EncryptUpdate )(sce_gcm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_data_length, uint8_t *aad, uint32_t aad_length)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_EncryptFinal )(sce_gcm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_data_length, uint8_t *atag)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_DecryptInit )(sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_DecryptUpdate )(sce_gcm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_data_length, uint8_t *aad, uint32_t aad_length)</code>
<code>fsp_err_t(*</code>	<code>AES128GCM_DecryptFinal )(sce_gcm_handle_t *handle, uint8_t *plain, uint32_t *plain_data_length, uint8_t *atag, uint32_t atag_length)</code>

<code>fsp_err_t(*</code>	<code>AES256GCM_EncryptInit</code> )(sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)
<code>fsp_err_t(*</code>	<code>AES256GCM_EncryptUpdate</code> )(sce_gcm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_data_length, uint8_t *aad, uint32_t aad_length)
<code>fsp_err_t(*</code>	<code>AES256GCM_EncryptFinal</code> )(sce_gcm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_data_length, uint8_t *atag)
<code>fsp_err_t(*</code>	<code>AES256GCM_DecryptInit</code> )(sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)
<code>fsp_err_t(*</code>	<code>AES256GCM_DecryptUpdate</code> )(sce_gcm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_data_length, uint8_t *aad, uint32_t aad_length)
<code>fsp_err_t(*</code>	<code>AES256GCM_DecryptFinal</code> )(sce_gcm_handle_t *handle, uint8_t *plain, uint32_t *plain_data_length, uint8_t *atag, uint32_t atag_length)
<code>fsp_err_t(*</code>	<code>AES128CCM_EncryptInit</code> )(sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)
<code>fsp_err_t(*</code>	<code>AES128CCM_EncryptUpdate</code> )(sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)
<code>fsp_err_t(*</code>	<code>AES128CCM_EncryptFinal</code> )(sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)
<code>fsp_err_t(*</code>	<code>AES128CCM_DecryptInit</code> )(sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)
<code>fsp_err_t(*</code>	<code>AES128CCM_DecryptUpdate</code> )(sce_ccm_handle_t *handle, uint8_t

	<code>*cipher, uint8_t *plain, uint32_t cipher_length)</code>
<code>fsp_err_t(*</code>	<code>AES128CCM_DecryptFinal )(sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_EncryptInit )(sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_EncryptUpdate )(sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_EncryptFinal )(sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_DecryptInit )(sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_DecryptUpdate )(sce_ccm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)</code>
<code>fsp_err_t(*</code>	<code>AES256CCM_DecryptFinal )(sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)</code>
<code>fsp_err_t(*</code>	<code>AES128CMAC_GenerateInit )(sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>AES128CMAC_GenerateUpdate )(sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)</code>
<code>fsp_err_t(*</code>	<code>AES128CMAC_GenerateFinal )(sce_cmac_handle_t *handle, uint8_t *mac)</code>
<code>fsp_err_t(*</code>	<code>AES128CMAC_VerifyInit )(sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>AES128CMAC_VerifyUpdate )(sce_cmac_handle_t *handle, uint8_t</code>

	*message, uint32_t message_length)
fsp_err_t(*	AES128CMAC_VerifyFinal )(sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t(*	AES256CMAC_GenerateInit )(sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES256CMAC_GenerateUpdate )(sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t(*	AES256CMAC_GenerateFinal )(sce_cmac_handle_t *handle, uint8_t *mac)
fsp_err_t(*	AES256CMAC_VerifyInit )(sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)
fsp_err_t(*	AES256CMAC_VerifyUpdate )(sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t(*	AES256CMAC_VerifyFinal )(sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t(*	SHA256_Init )(sce_sha_md5_handle_t *handle)
fsp_err_t(*	SHA256_Update )(sce_sha_md5_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t(*	SHA256_Final )(sce_sha_md5_handle_t *handle, uint8_t *digest, uint32_t *digest_length)
fsp_err_t(*	RSA1024_WrappedKeyPairGenerate )(sce_rsa1024_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	RSA2048_WrappedKeyPairGenerate )(sce_rsa2048_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	RSA1024_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t

	<code>*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_public_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSA1024_EncryptedPrivateKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_private_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSA2048_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa2048_public_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSA2048_EncryptedPrivateKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa2048_private_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSA3072_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa3072_public_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSA4096_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa4096_public_wrapped_key_t *wrapped_key)</code>
<code>fsp_err_t(*</code>	<code>RSASSA_PKCS1024_SignatureGenerate )(sce_rsa_byte_data_t *message_hash, sce_rsa_byte_data_t *signature, sce_rsa1024_private_wrapped_key_t *wrapped_key, uint8_t hash_type)</code>
<code>fsp_err_t(*</code>	<code>RSASSA_PKCS2048_SignatureGenerate )(sce_rsa_byte_data_t *message_hash, sce_rsa_byte_data_t *signature, sce_rsa2048_private_wrapped_key_t *wrapped_key, uint8_t hash_type)</code>
<code>fsp_err_t(*</code>	<code>RSASSA_PKCS1024_SignatureVerify )(sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa1024_public_wrapped_key_t *wrapped_key, uint8_t hash_type)</code>
<code>fsp_err_t(*</code>	<code>RSASSA_PKCS2048_SignatureVerify )(sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa2048_public_wrapped_key_t *wrapped_key, uint8_t hash_type)</code>

fsp_err_t(*)	RSASSA_PKCS3072_SignatureVerify )(sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa3072_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t(*)	RSASSA_PKCS4096_SignatureVerify )(sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa4096_public_wrapped_key_t *wrapped_key, uint8_t hash_type)
fsp_err_t(*)	RSAES_PKCS1024_Encrypt )(sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa1024_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	RSAES_PKCS2048_Encrypt )(sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa2048_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	RSAES_PKCS3072_Encrypt )(sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa3072_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	RSAES_PKCS4096_Encrypt )(sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa4096_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	RSAES_PKCS1024_Decrypt )(sce_rsa_byte_data_t *cipher, sce_rsa_byte_data_t *plain, sce_rsa1024_private_wrapped_key_t *wrapped_key)
fsp_err_t(*)	RSAES_PKCS2048_Decrypt )(sce_rsa_byte_data_t *cipher, sce_rsa_byte_data_t *plain, sce_rsa2048_private_wrapped_key_t *wrapped_key)
fsp_err_t(*)	SHA256HMAC_EncryptedKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t(*)	SHA256HMAC_GenerateInit )(sce_hmac_sha_handle_t *handle, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t(*)	SHA256HMAC_GenerateUpdate )(sce_hmac_sha_handle_t *handle,

	uint8_t *message, uint32_t message_length)
fsp_err_t(*	SHA256HMAC_GenerateFinal )(sce_hmac_sha_handle_t *handle, uint8_t *mac)
fsp_err_t(*	SHA256HMAC_VerifyInit )(sce_hmac_sha_handle_t *handle, sce_hmac_sha_wrapped_key_t *wrapped_key)
fsp_err_t(*	SHA256HMAC_VerifyUpdate )(sce_hmac_sha_handle_t *handle, uint8_t *message, uint32_t message_length)
fsp_err_t(*	SHA256HMAC_VerifyFinal )(sce_hmac_sha_handle_t *handle, uint8_t *mac, uint32_t mac_length)
fsp_err_t(*	ECC_secp192r1_WrappedKeyPairGenerate )(sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	ECC_secp224r1_WrappedKeyPairGenerate )(sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	ECC_secp256r1_WrappedKeyPairGenerate )(sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	ECC_secp384r1_WrappedKeyPairGenerate )(sce_ecc_wrapped_pair_key_t *wrapped_pair_key)
fsp_err_t(*	ECC_secp192r1_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*	ECC_secp224r1_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*	ECC_secp256r1_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*	ECC_secp384r1_EncryptedPublicKeyWrap )(uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key,

	<code>sce_ecc_public_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECC_secp192r1_EncryptedPrivateKeyWrap</code> )( <code>uint8_t *initial_vector</code> , <code>uint8_t *encrypted_key</code> , <code>sce_key_update_key_t *key_update_key</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECC_secp224r1_EncryptedPrivateKeyWrap</code> )( <code>uint8_t *initial_vector</code> , <code>uint8_t *encrypted_key</code> , <code>sce_key_update_key_t *key_update_key</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECC_secp256r1_EncryptedPrivateKeyWrap</code> )( <code>uint8_t *initial_vector</code> , <code>uint8_t *encrypted_key</code> , <code>sce_key_update_key_t *key_update_key</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECC_secp384r1_EncryptedPrivateKeyWrap</code> )( <code>uint8_t *initial_vector</code> , <code>uint8_t *encrypted_key</code> , <code>sce_key_update_key_t *key_update_key</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp192r1_SignatureGenerate</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*message_hash</code> , <code>sce_ecdsa_byte_data_t *signature</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp224r1_SignatureGenerate</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*message_hash</code> , <code>sce_ecdsa_byte_data_t *signature</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp256r1_SignatureGenerate</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*message_hash</code> , <code>sce_ecdsa_byte_data_t *signature</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp384r1_SignatureGenerate</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*message_hash</code> , <code>sce_ecdsa_byte_data_t *signature</code> , <code>sce_ecc_private_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp192r1_SignatureVerify</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*signature</code> , <code>sce_ecdsa_byte_data_t *message_hash</code> , <code>sce_ecc_public_wrapped_key_t *wrapped_key</code> )
<code>fsp_err_t(*</code>	<code>ECDSA_secp224r1_SignatureVerify</code> )( <code>sce_ecdsa_byte_data_t</code> <code>*signature</code> , <code>sce_ecdsa_byte_data_t *message_hash</code> , <code>sce_ecc_public_wrapped_key_t *wrapped_key</code> )

fsp_err_t(*)	ECDSA_secp256r1_SignatureVerify )(sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	ECDSA_secp384r1_SignatureVerify )(sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	ECDH_secp256r1_Init )(sce_ecdh_handle_t *handle, uint32_t key_type, uint32_t use_key_id)
fsp_err_t(*)	ECDH_secp256r1_PublicKeySign )(sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key, uint8_t *public_key, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)
fsp_err_t(*)	ECDH_secp256r1_PublicKeyVerify )(sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, uint8_t *public_key_data, sce_ecdsa_byte_data_t *signature, sce_ecc_public_wrapped_key_t *wrapped_key)
fsp_err_t(*)	ECDH_secp256r1_SharedSecretCalculate )(sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key, sce_ecdh_wrapped_key_t *shared_secret_wrapped_key)
fsp_err_t(*)	ECDH_secp256r1_KeyDerivation )(sce_ecdh_handle_t *handle, sce_ecdh_wrapped_key_t *shared_secret_wrapped_key, uint32_t key_type, uint32_t kdf_type, uint8_t *other_info, uint32_t other_info_length, sce_hmac_sha_wrapped_key_t *salt_wrapped_key, sce_aes_wrapped_key_t *wrapped_key)

## Field Documentation

◆ **open**

`fsp_err_t(* sce_api_t::open) (sce_ctrl_t *const p_ctrl, sce_cfg_t const *const p_cfg)`

Enables use of SCE functionality.

**Implemented as**

- `R_SCE_Open()`

**Parameters**

[in]	p_ctrl	Pointer to control structure.
[in]	p_cfg	Pointer to pin configuration structure.

◆ **close**

`fsp_err_t(* sce_api_t::close) (sce_ctrl_t *const p_ctrl)`

Stops supply of power to the SCE.

**Implemented as**

- `R_SCE_Close()`

**Parameters**

[in]	p_ctrl	Pointer to control structure.
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◆ **softwareReset**

`fsp_err_t(* sce_api_t::softwareReset) (void)`

Software reset to SCE.

**Implemented as**

- `R_SCE_SoftwareReset()`

◆ **randomNumberGenerate**

`fsp_err_t(* sce_api_t::randomNumberGenerate) (uint32_t *random)`

Generates 4 words random number.

**Implemented as**

- `R_SCE_RandomNumberGenerate()`

**Parameters**

[in,out]	random	Stores 4 words (16 bytes) random data.
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### ◆ AES128\_WrappedKeyGenerate

`fsp_err_t(* sce_api_t::AES128_WrappedKeyGenerate) (sce_aes_wrapped_key_t *wrapped_key)`

This API outputs 128-bit AES wrapped key.

#### Implemented as

- `R_SCE_AES128_WrappedKeyGenerate()`

#### Parameters

[in,out]	wrapped_key	128-bit AES wrapped key
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### ◆ AES256\_WrappedKeyGenerate

`fsp_err_t(* sce_api_t::AES256_WrappedKeyGenerate) (sce_aes_wrapped_key_t *wrapped_key)`

This API outputs 256-bit AES wrapped key.

#### Implemented as

- `R_SCE_AES256_WrappedKeyGenerate()`

#### Parameters

[in,out]	wrapped_key	256-bit AES wrapped key
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### ◆ AES128\_EncryptedKeyWrap

`fsp_err_t(* sce_api_t::AES128_EncryptedKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)`

This API outputs 128-bit AES wrapped key.

#### Implemented as

- `R_SCE_AES128_EncryptedKeyWrap()`

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	128-bit AES wrapped key

### ◆ AES256\_EncryptedKeyWrap

`fsp_err_t(* sce_api_t::AES256_EncryptedKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_aes_wrapped_key_t *wrapped_key)`

This API outputs 256-bit AES wrapped key.

#### Implemented as

- `R_SCE_AES256_EncryptedKeyWrap()`

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	256-bit AES wrapped key

### ◆ AES128ECB\_EncryptInit

`fsp_err_t(* sce_api_t::AES128ECB_EncryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES128ECB encryption.

#### Implemented as

- `R_SCE_AES128ECB_EncryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key

### ◆ AES128ECB\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES128ECB_EncryptUpdate) (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES128ECB encryption.

#### Implemented as

- `R_SCE_AES128ECB_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in,out]	plain_length	plaintext data length (must be a multiple of 16)

### ◆ AES128ECB\_EncryptFinal

`fsp_err_t(* sce_api_t::AES128ECB_EncryptFinal) (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)`

Finalize AES128ECB encryption.

#### Implemented as

- `R_SCE_AES128ECB_EncryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

### ◆ AES128ECB\_DecryptInit

`fsp_err_t(* sce_api_t::AES128ECB_DecryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES128ECB decryption.

#### Implemented as

- `R_SCE_AES128ECB_DecryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key

### ◆ AES128ECB\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES128ECB_DecryptUpdate) (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES128ECB decryption.

#### Implemented as

- `R_SCE_AES128ECB_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

### ◆ AES128ECB\_DecryptFinal

`fsp_err_t(* sce_api_t::AES128ECB_DecryptFinal) (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)`

Finalize AES128ECB decryption.

#### Implemented as

- `R_SCE_AES128ECB_DecryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

### ◆ AES256ECB\_EncryptInit

`fsp_err_t(* sce_api_t::AES256ECB_EncryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES256ECB encryption.

#### Implemented as

- `R_SCE_AES256ECB_EncryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key

### ◆ AES256ECB\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES256ECB_EncryptUpdate) (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES256ECB encryption.

#### Implemented as

- [R\\_SCE\\_AES256ECB\\_EncryptUpdate\(\)](#)

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in,out]	plain_length	plaintext data length (must be a multiple of 16)

### ◆ AES256ECB\_EncryptFinal

`fsp_err_t(* sce_api_t::AES256ECB_EncryptFinal) (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)`

Finalize AES256ECB encryption.

#### Implemented as

- [R\\_SCE\\_AES256ECB\\_EncryptFinal\(\)](#)

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

### ◆ AES256ECB\_DecryptInit

`fsp_err_t(* sce_api_t::AES256ECB_DecryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES256ECB decryption.

#### Implemented as

- [R\\_SCE\\_AES256ECB\\_DecryptInit\(\)](#)

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key

### ◆ AES256ECB\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES256ECB_DecryptUpdate) (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES256ECB decryption.

#### Implemented as

- `R_SCE_AES256ECB_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

### ◆ AES256ECB\_DecryptFinal

`fsp_err_t(* sce_api_t::AES256ECB_DecryptFinal) (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)`

Finalize AES256ECB decryption.

#### Implemented as

- `R_SCE_AES256ECB_DecryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

### ◆ AES128CBC\_EncryptInit

`fsp_err_t(* sce_api_t::AES128CBC_EncryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)`

Initialize AES128CBC encryption.

#### Implemented as

- `R_SCE_AES128CBC_EncryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initial vector area (16byte)

### ◆ AES128CBC\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES128CBC_EncryptUpdate) (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES128CBC encryption.

#### Implemented as

- `R_SCE_AES128CBC_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in,out]	plain_length	plaintext data length (must be a multiple of 16)

### ◆ AES128CBC\_EncryptFinal

`fsp_err_t(* sce_api_t::AES128CBC_EncryptFinal) (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)`

Finalize AES128CBC encryption.

#### Implemented as

- `R_SCE_AES128CBC_EncryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

### ◆ AES128CBC\_DecryptInit

`fsp_err_t(* sce_api_t::AES128CBC_DecryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)`

Initialize AES128CBC decryption.

#### Implemented as

- `R_SCE_AES128CBC_DecryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initial vector area (16byte)

### ◆ AES128CBC\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES128CBC_DecryptUpdate) (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES128CBC decryption.

#### Implemented as

- `R_SCE_AES128CBC_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

### ◆ AES128CBC\_DecryptFinal

`fsp_err_t(* sce_api_t::AES128CBC_DecryptFinal) (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)`

Finalize AES128CBC decryption.

#### Implemented as

- `R_SCE_AES128CBC_DecryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

### ◆ AES256CBC\_EncryptInit

`fsp_err_t(* sce_api_t::AES256CBC_EncryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)`

Initialize AES256CBC encryption.

#### Implemented as

- `R_SCE_AES256CBC_EncryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initial vector area (16byte)

### ◆ AES256CBC\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES256CBC_EncryptUpdate) (sce_aes_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES256CBC encryption.

#### Implemented as

- `R_SCE_AES256CBC_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in,out]	plain_length	plaintext data length (must be a multiple of 16)

### ◆ AES256CBC\_EncryptFinal

`fsp_err_t(* sce_api_t::AES256CBC_EncryptFinal) (sce_aes_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length)`

Finalize AES256CBC encryption.

#### Implemented as

- `R_SCE_AES256CBC_EncryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	cipher	ciphertext data area (nothing ever written here)
[in,out]	cipher_length	ciphertext data length (0 always written here)

### ◆ AES256CBC\_DecryptInit

`fsp_err_t(* sce_api_t::AES256CBC_DecryptInit) (sce_aes_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector)`

Initialize AES256CBC decryption.

#### Implemented as

- `R_SCE_AES256CBC_DecryptInit()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initial vector area (16byte)

### ◆ AES256CBC\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES256CBC_DecryptUpdate) (sce_aes_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES256CBC decryption.

#### Implemented as

- `R_SCE_AES256CBC_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in,out]	cipher_length	ciphertext data length (must be a multiple of 16)

### ◆ AES256CBC\_DecryptFinal

`fsp_err_t(* sce_api_t::AES256CBC_DecryptFinal) (sce_aes_handle_t *handle, uint8_t *plain, uint32_t *plain_length)`

Finalize AES256CBC decryption.

#### Implemented as

- `R_SCE_AES256CBC_DecryptFinal()`

#### Parameters

[in,out]	handle	AES handler (work area)
[in,out]	plain	plaintext data area (nothing ever written here)
[in,out]	plain_length	plaintext data length (0 always written here)

### ◆ AES128GCM\_EncryptInit

`fsp_err_t(*sce_api_t::AES128GCM_EncryptInit)(sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)`

Initialize AES128GCM encryption.

#### Implemented as

- `R_SCE_AES128GCM_EncryptInit()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initialization vector area (initial_vector_length byte)
[in]	initial_vector_length	initialization vector length (1 or more bytes)

### ◆ AES128GCM\_EncryptUpdate

`fsp_err_t(*sce_api_t::AES128GCM_EncryptUpdate)(sce_gcm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_data_length, uint8_t *aad, uint32_t aad_length)`

Update AES128GCM encryption.

#### Implemented as

- `R_SCE_AES128GCM_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_data_length	plaintext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

### ◆ AES128GCM\_EncryptFinal

`fsp_err_t(* sce_api_t::AES128GCM_EncryptFinal) (sce_gcm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_data_length, uint8_t *atag)`

Finalize AES128GCM encryption.

#### Implemented as

- `R_SCE_AES128GCM_EncryptFinal()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area (cipher_data_length byte)
[in,out]	cipher_data_length	ciphertext data length (0 always written here)
[in,out]	atag	authentication tag area

### ◆ AES128GCM\_DecryptInit

`fsp_err_t(* sce_api_t::AES128GCM_DecryptInit) (sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)`

Initialize AES128GCM decryption.

#### Implemented as

- `R_SCE_AES128GCM_DecryptInit()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	initial_vector	initialization vector area (initial_vector_length byte)
[in]	initial_vector_length	initialization vector length (1 ore more bytes)

### ◆ AES128GCM\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES128GCM_DecryptUpdate) (sce_gcm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_data_length, uint8_t *aad, uint32_t aad_length)`

Update AES128GCM decryption.

#### Implemented as

- `R_SCE_AES128GCM_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area
[in]	plain	plaintext data area
[in]	cipher_data_length	ciphertext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

### ◆ AES128GCM\_DecryptFinal

`fsp_err_t(* sce_api_t::AES128GCM_DecryptFinal) (sce_gcm_handle_t *handle, uint8_t *plain, uint32_t *plain_data_length, uint8_t *atag, uint32_t atag_length)`

Finalize AES128GCM decryption.

#### Implemented as

- `R_SCE_AES128GCM_DecryptFinal()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	plain	plaintext data area (cipher_data_length byte)
[in,out]	plain_data_length	plaintext data length (0 always written here)
[in,out]	atag	authentication tag area (atag_length byte)
[in]	atag_length	authentication tag length (4,8,12,13,14,15,16 bytes)

### ◆ AES256GCM\_EncryptInit

`fsp_err_t(* sce_api_t::AES256GCM_EncryptInit) (sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)`

Initialize AES256GCM encryption.

#### Implemented as

- `R_SCE_AES256GCM_EncryptInit()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initialization vector area (initial_vector_length byte)
[in]	initial_vector_length	initialization vector length (1 or more bytes)

### ◆ AES256GCM\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES256GCM_EncryptUpdate) (sce_gcm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_data_length, uint8_t *aad, uint32_t aad_length)`

Update AES256GCM encryption.

#### Implemented as

- `R_SCE_AES256GCM_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_data_length	plaintext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

### ◆ AES256GCM\_EncryptFinal

`fsp_err_t(* sce_api_t::AES256GCM_EncryptFinal) (sce_gcm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_data_length, uint8_t *atag)`

Finalize AES256GCM encryption.

#### Implemented as

- `R_SCE_AES256GCM_EncryptFinal()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area (cipher_data_length byte)
[in,out]	cipher_data_length	ciphertext data length (0 always written here)
[in,out]	atag	authentication tag area

### ◆ AES256GCM\_DecryptInit

`fsp_err_t(* sce_api_t::AES256GCM_DecryptInit) (sce_gcm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *initial_vector, uint32_t initial_vector_length)`

Initialize AES256GCM decryption.

#### Implemented as

- `R_SCE_AES256GCM_DecryptInit()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	initial_vector	initialization vector area (initial_vector_length byte)
[in]	initial_vector_length	initialization vector length (1 ore more bytes)

### ◆ AES256GCM\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES256GCM_DecryptUpdate) (sce_gcm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_data_length, uint8_t *aad, uint32_t aad_length)`

Update AES256GCM decryption.

#### Implemented as

- `R_SCE_AES256GCM_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	cipher	ciphertext data area
[in]	plain	plaintext data area
[in]	cipher_data_length	ciphertext data length (0 or more bytes)
[in]	aad	additional authentication data (aad_length byte)
[in]	aad_length	additional authentication data length (0 or more bytes)

### ◆ AES256GCM\_DecryptFinal

`fsp_err_t(* sce_api_t::AES256GCM_DecryptFinal) (sce_gcm_handle_t *handle, uint8_t *plain, uint32_t *plain_data_length, uint8_t *atag, uint32_t atag_length)`

Finalize AES256GCM decryption.

#### Implemented as

- `R_SCE_AES256GCM_DecryptFinal()`

#### Parameters

[in,out]	handle	AES-GCM handler (work area)
[in,out]	plain	plaintext data area (cipher_data_length byte)
[in,out]	plain_data_length	plaintext data length (0 always written here)
[in,out]	atag	authentication tag area (atag_length byte)
[in]	atag_length	authentication tag length (4,8,12,13,14,15,16 bytes)

### ◆ AES128CCM\_EncryptInit

`fsp_err_t(* sce_api_t::AES128CCM_EncryptInit) (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)`

Initialize AES128CCM encryption.

#### Implemented as

- `R_SCE_AES128CCM_EncryptInit()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES128CCM\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES128CCM_EncryptUpdate) (sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES128CCM encryption.

#### Implemented as

- `R_SCE_AES128CCM_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_length	plaintext data length

### ◆ AES128CCM\_EncryptFinal

`fsp_err_t(* sce_api_t::AES128CCM_EncryptFinal) (sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)`

Finalize AES128CCM encryption.

#### Implemented as

- [R\\_SCE\\_AES128CCM\\_EncryptFinal\(\)](#)

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	cipher	ciphertext data area
[in,out]	cipher_length	ciphertext data length
[in,out]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES128CCM\_DecryptInit

`fsp_err_t(* sce_api_t::AES128CCM_DecryptInit) (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)`

Initialize AES128CCM decryption.

#### Implemented as

- [R\\_SCE\\_AES128CCM\\_DecryptInit\(\)](#)

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	128-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES128CCM\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES128CCM_DecryptUpdate) (sce_ccm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES128CCM decryption.

#### Implemented as

- `R_SCE_AES128CCM_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in]	cipher_length	ciphertext data length

### ◆ AES128CCM\_DecryptFinal

`fsp_err_t(* sce_api_t::AES128CCM_DecryptFinal) (sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)`

Finalize AES128CCM decryption.

#### Implemented as

- `R_SCE_AES128CCM_DecryptFinal()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	plain	plaintext data area
[in,out]	plain_length	plaintext data length
[in]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES256CCM\_EncryptInit

`fsp_err_t(* sce_api_t::AES256CCM_EncryptInit) (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)`

Initialize AES256CCM encryption.

#### Implemented as

- `R_SCE_AES256CCM_EncryptInit()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES256CCM\_EncryptUpdate

`fsp_err_t(* sce_api_t::AES256CCM_EncryptUpdate) (sce_ccm_handle_t *handle, uint8_t *plain, uint8_t *cipher, uint32_t plain_length)`

Update AES256CCM encryption.

#### Implemented as

- `R_SCE_AES256CCM_EncryptUpdate()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	plain	plaintext data area
[in,out]	cipher	ciphertext data area
[in]	plain_length	plaintext data length

### ◆ AES256CCM\_EncryptFinal

`fsp_err_t(* sce_api_t::AES256CCM_EncryptFinal) (sce_ccm_handle_t *handle, uint8_t *cipher, uint32_t *cipher_length, uint8_t *mac, uint32_t mac_length)`

Finalize AES256CCM encryption.

#### Implemented as

- [R\\_SCE\\_AES256CCM\\_EncryptFinal\(\)](#)

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	cipher	ciphertext data area
[in,out]	cipher_length	ciphertext data length
[in,out]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES256CCM\_DecryptInit

`fsp_err_t(* sce_api_t::AES256CCM_DecryptInit) (sce_ccm_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key, uint8_t *nonce, uint32_t nonce_length, uint8_t *adata, uint8_t a_length, uint32_t payload_length, uint32_t mac_length)`

Initialize AES256CCM decryption.

#### Implemented as

- [R\\_SCE\\_AES256CCM\\_DecryptInit\(\)](#)

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	wrapped_key	256-bit AES wrapped key
[in]	nonce	Nonce
[in]	nonce_length	Nonce data length (7 to 13 bytes)
[in]	adata	additional authentication data
[in]	a_length	additional authentication data length (0 to 110 bytes)
[in]	payload_length	Payload length (any number of bytes)
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES256CCM\_DecryptUpdate

`fsp_err_t(* sce_api_t::AES256CCM_DecryptUpdate) (sce_ccm_handle_t *handle, uint8_t *cipher, uint8_t *plain, uint32_t cipher_length)`

Update AES256CCM decryption.

#### Implemented as

- `R_SCE_AES256CCM_DecryptUpdate()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in]	cipher	ciphertext data area
[in,out]	plain	plaintext data area
[in]	cipher_length	ciphertext data length

### ◆ AES256CCM\_DecryptFinal

`fsp_err_t(* sce_api_t::AES256CCM_DecryptFinal) (sce_ccm_handle_t *handle, uint8_t *plain, uint32_t *plain_length, uint8_t *mac, uint32_t mac_length)`

Finalize AES256CCM decryption.

#### Implemented as

- `R_SCE_AES256CCM_DecryptFinal()`

#### Parameters

[in,out]	handle	AES-CCM handler (work area)
[in,out]	plain	plaintext data area
[in,out]	plain_length	plaintext data length
[in]	mac	MAC area
[in]	mac_length	MAC length (4, 6, 8, 10, 12, 14, or 16 bytes)

### ◆ AES128CMAC\_GenerateInit

`fsp_err_t(* sce_api_t::AES128CMAC_GenerateInit) (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES128CMAC generation.

#### Implemented as

- `R_SCE_AES128CMAC_GenerateInit()`

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	128-bit AES wrapped key

### ◆ AES128CMAC\_GenerateUpdate

`fsp_err_t(* sce_api_t::AES128CMAC_GenerateUpdate) (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update AES128CMAC generation.

#### Implemented as

- `R_SCE_AES128CMAC_GenerateUpdate()`

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

### ◆ AES128CMAC\_GenerateFinal

`fsp_err_t(* sce_api_t::AES128CMAC_GenerateFinal) (sce_cmac_handle_t *handle, uint8_t *mac)`

Finalize AES128CMAC generation.

#### Implemented as

- `R_SCE_AES128CMAC_GenerateFinal()`

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (16byte)

### ◆ AES128CMAC\_VerifyInit

```
fsp_err_t(* sce_api_t::AES128CMAC_VerifyInit) (sce_cmac_handle_t *handle,
sce_aes_wrapped_key_t *wrapped_key)
```

Initialize AES128CMAC verification.

#### Implemented as

- R\_SCE\_AES128CMAC\_VerifyInit()

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	128-bit AES wrapped key

### ◆ AES128CMAC\_VerifyUpdate

```
fsp_err_t(* sce_api_t::AES128CMAC_VerifyUpdate) (sce_cmac_handle_t *handle, uint8_t *message,
uint32_t message_length)
```

Update AES128CMAC verification.

#### Implemented as

- R\_SCE\_AES128CMAC\_VerifyUpdate()

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

### ◆ AES128CMAC\_VerifyFinal

`fsp_err_t(* sce_api_t::AES128CMAC_VerifyFinal) (sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)`

Finalize AES128CMAC verification.

#### Implemented as

- `R_SCE_AES128CMAC_VerifyFinal()`

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (mac_length byte)
[in,out]	mac_length	MAC data length (2 to 16 bytes)

### ◆ AES256CMAC\_GenerateInit

`fsp_err_t(* sce_api_t::AES256CMAC_GenerateInit) (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES256CMAC generation.

#### Implemented as

- `R_SCE_AES256CMAC_GenerateInit()`

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	256-bit AES wrapped key

### ◆ AES256CMAC\_GenerateUpdate

`fsp_err_t(* sce_api_t::AES256CMAC_GenerateUpdate) (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update AES256CMAC generation.

#### Implemented as

- [R\\_SCE\\_AES256CMAC\\_GenerateUpdate\(\)](#)

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

### ◆ AES256CMAC\_GenerateFinal

`fsp_err_t(* sce_api_t::AES256CMAC_GenerateFinal) (sce_cmac_handle_t *handle, uint8_t *mac)`

Finalize AES256CMAC generation.

#### Implemented as

- [R\\_SCE\\_AES256CMAC\\_GenerateFinal\(\)](#)

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (16byte)

### ◆ AES256CMAC\_VerifyInit

`fsp_err_t(* sce_api_t::AES256CMAC_VerifyInit) (sce_cmac_handle_t *handle, sce_aes_wrapped_key_t *wrapped_key)`

Initialize AES256CMAC verification.

#### Implemented as

- [R\\_SCE\\_AES256CMAC\\_VerifyInit\(\)](#)

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	wrapped_key	256-bit AES wrapped key

### ◆ AES256CMAC\_VerifyUpdate

`fsp_err_t(* sce_api_t::AES256CMAC_VerifyUpdate) (sce_cmac_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update AES256CMAC verification.

#### Implemented as

- [R\\_SCE\\_AES256CMAC\\_VerifyUpdate\(\)](#)

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in]	message	message data area (message_length byte)
[in]	message_length	message data length (0 or more bytes)

### ◆ AES256CMAC\_VerifyFinal

`fsp_err_t(* sce_api_t::AES256CMAC_VerifyFinal) (sce_cmac_handle_t *handle, uint8_t *mac, uint32_t mac_length)`

Finalize AES256CMAC verification.

#### Implemented as

- [R\\_SCE\\_AES256CMAC\\_VerifyFinal\(\)](#)

#### Parameters

[in,out]	handle	AES-CMAC handler (work area)
[in,out]	mac	MAC data area (mac_length byte)
[in,out]	mac_length	MAC data length (2 to 16 bytes)

### ◆ SHA256\_Init

`fsp_err_t(* sce_api_t::SHA256_Init) (sce_sha_md5_handle_t *handle)`

Initialize SHA-256 Calculation.

#### Implemented as

- [R\\_SCE\\_SHA256\\_Init\(\)](#)

#### Parameters

[in,out]	handle	SHA handler (work area)
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### ◆ SHA256\_Update

`fsp_err_t(* sce_api_t::SHA256_Update) (sce_sha_md5_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update SHA-256 Calculation.

#### Implemented as

- `R_SCE_SHA256_Update()`

#### Parameters

[in,out]	handle	SHA handler (work area)
[in]	message	message data area
[in]	message_length	message data length

### ◆ SHA256\_Final

`fsp_err_t(* sce_api_t::SHA256_Final) (sce_sha_md5_handle_t *handle, uint8_t *digest, uint32_t *digest_length)`

Finalize SHA-256 Calculation.

#### Implemented as

- `R_SCE_SHA256_Final()`

#### Parameters

[in,out]	handle	SHA handler (work area)
[in,out]	digest	hasha data area
[in,out]	digest_length	hash data length (32bytes)

### ◆ RSA1024\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::RSA1024_WrappedKeyPairGenerate) (sce_rsa1024_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs 1024-bit RSA wrapped pair key.

#### Implemented as

- `R_SCE_RSA1024_WrappedKeyPairGenerate()`

#### Parameters

[in,out]	wrapped_key	128-bit AES wrapped key
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### ◆ RSA2048\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::RSA2048_WrappedKeyPairGenerate) (sce_rsa2048_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs 2048-bit RSA wrapped pair key.

#### Implemented as

- `R_SCE_RSA2048_WrappedKeyPairGenerate()`

#### Parameters

[in,out]	wrapped_key	128-bit AES wrapped key
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### ◆ RSA1024\_EncryptedPublicKeyWrap

`fsp_err_t(* sce_api_t::RSA1024_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_public_wrapped_key_t *wrapped_key)`

This API outputs 1024-bit RSA public wrapped key.

#### Implemented as

- `R_SCE_RSA1024_EncryptedPublicKeyWrap()`

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA public wrapped key

### ◆ RSA1024\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::RSA1024_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa1024_private_wrapped_key_t
*wrapped_key)
```

This API outputs 1024-bit RSA private wrapped key.

#### Implemented as

- R\_SCE\_RSA1024\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	1024-bit RSA private wrapped key

### ◆ RSA2048\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::RSA2048_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa2048_public_wrapped_key_t
*wrapped_key)
```

This API outputs 2048-bit RSA public wrapped key.

#### Implemented as

- R\_SCE\_RSA2048\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	2048-bit RSA public wrapped key

### ◆ RSA2048\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::RSA2048_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa2048_private_wrapped_key_t
*wrapped_key)
```

This API outputs 2048-bit RSA private wrapped key.

#### Implemented as

- R\_SCE\_RSA2048\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	2048-bit RSA private wrapped key

### ◆ RSA3072\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::RSA3072_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa3072_public_wrapped_key_t
*wrapped_key)
```

This API outputs 3072-bit RSA public wrapped key.

#### Implemented as

- R\_SCE\_RSA3072\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	3072-bit RSA public wrapped key

### ◆ RSA4096\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::RSA4096_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_rsa4096_public_wrapped_key_t
*wrapped_key)
```

This API outputs 4096-bit RSA public wrapped key.

#### Implemented as

- R\_SCE\_RSA4096\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	4096-bit RSA public wrapped key

### ◆ RSASSA\_PKCS1024\_SignatureGenerate

```
fsp_err_t(* sce_api_t::RSASSA_PKCS1024_SignatureGenerate) (sce_rsa_byte_data_t *message_hash,
sce_rsa_byte_data_t *signature, sce_rsa1024_private_wrapped_key_t *wrapped_key, uint8_t
hash_type)
```

RSASSA-PKCS1-V1\_5 signature generation.

#### Implemented as

- R\_SCE\_RSASSA\_PKCS1024\_SignatureGenerate()

#### Parameters

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Inputs the 1024-bit RSA private wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSASSA\_PKCS2048\_SignatureGenerate

`fsp_err_t(* sce_api_t::RSASSA_PKCS2048_SignatureGenerate) (sce_rsa_byte_data_t *message_hash, sce_rsa_byte_data_t *signature, sce_rsa2048_private_wrapped_key_t *wrapped_key, uint8_t hash_type)`

RSASSA-PKCS1-V1\_5 signature generation.

#### Implemented as

- `R_SCE_RSASSA_PKCS2048_SignatureGenerate()`

#### Parameters

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Inputs the 2048-bit RSA private wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSASSA\_PKCS1024\_SignatureVerify

`fsp_err_t(* sce_api_t::RSASSA_PKCS1024_SignatureVerify) (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa1024_public_wrapped_key_t *wrapped_key, uint8_t hash_type)`

RSASSA-PKCS1-V1\_5 signature verification.

#### Implemented as

- `R_SCE_RSASSA_PKCS1024_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to verify
[in]	message_hash	Message text or hash value to verify
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSASSA\_PKCS2048\_SignatureVerify

`fsp_err_t(* sce_api_t::RSASSA_PKCS2048_SignatureVerify) (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa2048_public_wrapped_key_t *wrapped_key, uint8_t hash_type)`

RSASSA-PKCS1-V1\_5 signature verification.

#### Implemented as

- `R_SCE_RSASSA_PKCS2048_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to verify
[in]	message_hash	Message text or hash value to verify
[in]	wrapped_key	Inputs the 2048-bit RSA public wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSASSA\_PKCS3072\_SignatureVerify

`fsp_err_t(* sce_api_t::RSASSA_PKCS3072_SignatureVerify) (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa3072_public_wrapped_key_t *wrapped_key, uint8_t hash_type)`

RSASSA-PKCS1-V1\_5 signature verification.

#### Implemented as

- `R_SCE_RSASSA_PKCS3072_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to verify
[in]	message_hash	Message text or hash value to verify
[in]	wrapped_key	Inputs the 3072-bit RSA public wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSASSA\_PKCS4096\_SignatureVerify

`fsp_err_t(* sce_api_t::RSASSA_PKCS4096_SignatureVerify) (sce_rsa_byte_data_t *signature, sce_rsa_byte_data_t *message_hash, sce_rsa4096_public_wrapped_key_t *wrapped_key, uint8_t hash_type)`

RSASSA-PKCS1-V1\_5 signature verification.

#### Implemented as

- `R_SCE_RSASSA_PKCS4096_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to verify
[in]	message_hash	Message text or hash value to verify
[in]	wrapped_key	Inputs the 4096-bit RSA public wrapped key.
[in]	hash_type	Only HW_SCE_RSA_HASH_SHA256 is supported

### ◆ RSAES\_PKCS1024\_Encrypt

`fsp_err_t(* sce_api_t::RSAES_PKCS1024_Encrypt) (sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa1024_public_wrapped_key_t *wrapped_key)`

RSAES-PKCS1-V1\_5 encryption.

#### Implemented as

- `R_SCE_RSAES_PKCS1024_Encrypt()`

#### Parameters

[in]	plain	plaintext
[in,out]	cipher	ciphertext
[in]	wrapped_key	Inputs the 1024-bit RSA public wrapped key.

**◆ RSAES\_PKCS2048\_Encrypt**

`fsp_err_t(* sce_api_t::RSAES_PKCS2048_Encrypt) (sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa2048_public_wrapped_key_t *wrapped_key)`

RSAES-PKCS1-V1\_5 encryption.

**Implemented as**

- `R_SCE_RSAES_PKCS2048_Encrypt()`

**Parameters**

[in]	plain	plaintext
[in,out]	cipher	ciphertext
[in]	wrapped_key	Inputs the 2048-bit RSA public wrapped key.

**◆ RSAES\_PKCS3072\_Encrypt**

`fsp_err_t(* sce_api_t::RSAES_PKCS3072_Encrypt) (sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa3072_public_wrapped_key_t *wrapped_key)`

RSAES-PKCS1-V1\_5 encryption.

**Implemented as**

- `R_SCE_RSAES_PKCS3072_Encrypt()`

**Parameters**

[in]	plain	plaintext
[in,out]	cipher	ciphertext
[in]	wrapped_key	Inputs the 3072-bit RSA public wrapped key.

**◆ RSAES\_PKCS4096\_Encrypt**

`fsp_err_t(* sce_api_t::RSAES_PKCS4096_Encrypt) (sce_rsa_byte_data_t *plain, sce_rsa_byte_data_t *cipher, sce_rsa4096_public_wrapped_key_t *wrapped_key)`

RSAES-PKCS1-V1\_5 encryption.

**Implemented as**

- `R_SCE_RSAES_PKCS4096_Encrypt()`

**Parameters**

[in]	plain	plaintext
[in,out]	cipher	ciphertext
[in]	wrapped_key	Inputs the 4096-bit RSA public wrapped key.

**◆ RSAES\_PKCS1024\_Decrypt**

```
fsp_err_t(* sce_api_t::RSAES_PKCS1024_Decrypt) (sce_rsa_byte_data_t *cipher, sce_rsa_byte_data_t *plain, sce_rsa1024_private_wrapped_key_t *wrapped_key)
```

RSAES-PKCS1-V1\_5 decryption.

**Implemented as**

- R\_SCE\_RSAES\_PKCS1024\_Decrypt()

**Parameters**

[in]	cipher	ciphertext
[in,out]	plain	plaintext
[in]	wrapped_key	Inputs the 1024-bit RSA private wrapped key.

**◆ RSAES\_PKCS2048\_Decrypt**

```
fsp_err_t(* sce_api_t::RSAES_PKCS2048_Decrypt) (sce_rsa_byte_data_t *cipher, sce_rsa_byte_data_t *plain, sce_rsa2048_private_wrapped_key_t *wrapped_key)
```

RSAES-PKCS1-V1\_5 decryption.

**Implemented as**

- R\_SCE\_RSAES\_PKCS2048\_Decrypt()

**Parameters**

[in]	cipher	ciphertext
[in,out]	plain	plaintext
[in]	wrapped_key	Inputs the 2048-bit RSA private wrapped key.

### ◆ SHA256HMAC\_EncryptedKeyWrap

```
fsp_err_t(* sce_api_t::SHA256HMAC_EncryptedKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_hmac_sha_wrapped_key_t
*wrapped_key)
```

This API outputs HMAC-SHA256 wrapped key.

#### Implemented as

- R\_SCE\_SHA256HMAC\_EncryptedKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	HMAC-SHA256 wrapped key

### ◆ SHA256HMAC\_GenerateInit

```
fsp_err_t(* sce_api_t::SHA256HMAC_GenerateInit) (sce_hmac_sha_handle_t *handle,
sce_hmac_sha_wrapped_key_t *wrapped_key)
```

Initialize HMAC-SHA256 generation.

#### Implemented as

- R\_SCE\_SHA256HMAC\_GenerateInit()

#### Parameters

[in,out]	handle	SHA-HMAC handler (work area)
[in]	wrapped_key	MAC wrapped key

### ◆ SHA256HMAC\_GenerateUpdate

`fsp_err_t(* sce_api_t::SHA256HMAC_GenerateUpdate) (sce_hmac_sha_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update HMAC-SHA256 generation.

#### Implemented as

- `R_SCE_SHA256HMAC_GenerateUpdate()`

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in]	message	Message area
[in]	message_length	Message length

### ◆ SHA256HMAC\_GenerateFinal

`fsp_err_t(* sce_api_t::SHA256HMAC_GenerateFinal) (sce_hmac_sha_handle_t *handle, uint8_t *mac)`

Finalize HMAC-SHA256 generation.

#### Implemented as

- `R_SCE_SHA256HMAC_GenerateFinal()`

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in,out]	mac	HMAC area (32 bytes)

### ◆ SHA256HMAC\_VerifyInit

`fsp_err_t(* sce_api_t::SHA256HMAC_VerifyInit) (sce_hmac_sha_handle_t *handle, sce_hmac_sha_wrapped_key_t *wrapped_key)`

Initialize HMAC-SHA256 verification.

#### Implemented as

- `R_SCE_SHA256HMAC_VerifyInit()`

#### Parameters

[in,out]	handle	SHA-HMAC handler (work area)
[in]	wrapped_key	MAC wrapped key

### ◆ SHA256HMAC\_VerifyUpdate

`fsp_err_t(* sce_api_t::SHA256HMAC_VerifyUpdate) (sce_hmac_sha_handle_t *handle, uint8_t *message, uint32_t message_length)`

Update HMAC-SHA256 verification.

#### Implemented as

- `R_SCE_SHA256HMAC_VerifyUpdate()`

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in]	message	Message area
[in]	message_length	Message length

### ◆ SHA256HMAC\_VerifyFinal

`fsp_err_t(* sce_api_t::SHA256HMAC_VerifyFinal) (sce_hmac_sha_handle_t *handle, uint8_t *mac, uint32_t mac_length)`

Finalize HMAC-SHA256 verification.

#### Implemented as

- `R_SCE_SHA256HMAC_VerifyFinal()`

#### Parameters

[in,out]	handle	SHA-HMAC handle (work area)
[in]	mac	HMAC area
[in]	mac_length	HMAC length

### ◆ ECC\_secp192r1\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::ECC_secp192r1_WrappedKeyPairGenerate) (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs secp192r1 wrapped pair key.

#### Implemented as

- `R_SCE_ECC_secp192r1_WrappedKeyPairGenerate()`

#### Parameters

[in,out]	wrapped_pair_key	Wrapped pair key for secp192r1 public key and private key pair
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### ◆ ECC\_secp224r1\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::ECC_secp224r1_WrappedKeyPairGenerate) (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs secp224r1 wrapped pair key.

#### Implemented as

- [R\\_SCE\\_ECC\\_secp224r1\\_WrappedKeyPairGenerate\(\)](#)

#### Parameters

[in,out]	wrapped_pair_key	Wrapped pair key for secp224r1 public key and private key pair
----------	------------------	--

### ◆ ECC\_secp256r1\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::ECC_secp256r1_WrappedKeyPairGenerate) (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs secp256r1 wrapped pair key.

#### Implemented as

- [R\\_SCE\\_ECC\\_secp256r1\\_WrappedKeyPairGenerate\(\)](#)

#### Parameters

[in,out]	wrapped_pair_key	Wrapped pair key for secp256r1 public key and private key pair
----------	------------------	--

### ◆ ECC\_secp384r1\_WrappedKeyPairGenerate

`fsp_err_t(* sce_api_t::ECC_secp384r1_WrappedKeyPairGenerate) (sce_ecc_wrapped_pair_key_t *wrapped_pair_key)`

This API outputs secp384r1 wrapped pair key.

#### Implemented as

- [R\\_SCE\\_ECC\\_secp384r1\\_WrappedKeyPairGenerate\(\)](#)

#### Parameters

[in,out]	wrapped_pair_key	Wrapped pair key for secp384r1 public key and private key pair
----------	------------------	--

### ◆ ECC\_secp192r1\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp192r1_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

This API outputs secp192r1 public wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp192r1\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp192r1 public wrapped key

### ◆ ECC\_secp224r1\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp224r1_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t *wrapped_key)
```

This API outputs secp224r1 public wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp224r1\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp224r1 public wrapped key

### ◆ ECC\_secp256r1\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp256r1_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t
*wrapped_key)
```

This API outputs secp256r1 public wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp256r1\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp256r1 public wrapped key

### ◆ ECC\_secp384r1\_EncryptedPublicKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp384r1_EncryptedPublicKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_public_wrapped_key_t
*wrapped_key)
```

This API outputs secp384r1 public wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp384r1\_EncryptedPublicKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp384r1 public wrapped key

### ◆ ECC\_secp192r1\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp192r1_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

This API outputs secp192r1 private wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp192r1\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp192r1 private wrapped key

### ◆ ECC\_secp224r1\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp224r1_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t *encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_private_wrapped_key_t *wrapped_key)
```

This API outputs secp224r1 private wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp224r1\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp224r1 private wrapped key

### ◆ ECC\_secp256r1\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp256r1_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_private_wrapped_key_t
*wrapped_key)
```

This API outputs secp256r1 private wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp256r1\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp256r1 private wrapped key

### ◆ ECC\_secp384r1\_EncryptedPrivateKeyWrap

```
fsp_err_t(* sce_api_t::ECC_secp384r1_EncryptedPrivateKeyWrap) (uint8_t *initial_vector, uint8_t
*encrypted_key, sce_key_update_key_t *key_update_key, sce_ecc_private_wrapped_key_t
*wrapped_key)
```

This API outputs secp384r1 private wrapped key.

#### Implemented as

- R\_SCE\_ECC\_secp384r1\_EncryptedPrivateKeyWrap()

#### Parameters

[in]	initial_vector	Initialization vector when generating encrypted_key
[in]	encrypted_key	User key encrypted and MAC appended
[in]	key_update_key	Key update keyring
[in,out]	wrapped_key	secp384r1 private wrapped key

**◆ ECDSA\_secp192r1\_SignatureGenerate**

```
fsp_err_t(* sce_api_t::ECDSA_secp192r1_SignatureGenerate) (sce_ecdsa_byte_data_t
*message_hash, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)
```

ECDSA signature generation.

**Implemented as**

◦ R\_SCE\_ECDSA\_secp192r1\_SignatureGenerate()

**Parameters**

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Input wrapped key of secp192r1 private key.

**◆ ECDSA\_secp224r1\_SignatureGenerate**

```
fsp_err_t(* sce_api_t::ECDSA_secp224r1_SignatureGenerate) (sce_ecdsa_byte_data_t
*message_hash, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)
```

ECDSA signature generation.

**Implemented as**

◦ R\_SCE\_ECDSA\_secp224r1\_SignatureGenerate()

**Parameters**

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Input wrapped key of secp224r1 private key.

### ◆ ECDSA\_secp256r1\_SignatureGenerate

`fsp_err_t(* sce_api_t::ECDSA_secp256r1_SignatureGenerate) (sce_ecdsa_byte_data_t *message_hash, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)`

ECDSA signature generation.

#### Implemented as

- `R_SCE_ECDSA_secp256r1_SignatureGenerate()`

#### Parameters

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Input wrapped key of secp256r1 private key.

### ◆ ECDSA\_secp384r1\_SignatureGenerate

`fsp_err_t(* sce_api_t::ECDSA_secp384r1_SignatureGenerate) (sce_ecdsa_byte_data_t *message_hash, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)`

ECDSA signature generation.

#### Implemented as

- `R_SCE_ECDSA_secp384r1_SignatureGenerate()`

#### Parameters

[in]	message_hash	Message or hash value to which to attach signature
[in,out]	signature	Signature text storage destination information
[in]	wrapped_key	Input wrapped key of secp384r1 private key.

### ◆ ECDSA\_secp192r1\_SignatureVerify

`fsp_err_t(* sce_api_t::ECDSA_secp192r1_SignatureVerify) (sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)`

ECDSA signature verification.

#### Implemented as

- `R_SCE_ECDSA_secp192r1_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to be verified
[in,out]	message_hash	Message or hash value to be verified
[in]	wrapped_key	Input wrapped key of secp192r1 public key.

### ◆ ECDSA\_secp224r1\_SignatureVerify

`fsp_err_t(* sce_api_t::ECDSA_secp224r1_SignatureVerify) (sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)`

ECDSA signature verification.

#### Implemented as

- `R_SCE_ECDSA_secp224r1_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to be verified
[in,out]	message_hash	Message or hash value to be verified
[in]	wrapped_key	Input wrapped key of secp224r1 public key.

### ◆ ECDSA\_secp256r1\_SignatureVerify

`fsp_err_t(* sce_api_t::ECDSA_secp256r1_SignatureVerify) (sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)`

ECDSA signature verification.

#### Implemented as

- `R_SCE_ECDSA_secp256r1_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to be verified
[in,out]	message_hash	Message or hash value to be verified
[in]	wrapped_key	Input wrapped key of secp256r1 public key.

### ◆ ECDSA\_secp384r1\_SignatureVerify

`fsp_err_t(* sce_api_t::ECDSA_secp384r1_SignatureVerify) (sce_ecdsa_byte_data_t *signature, sce_ecdsa_byte_data_t *message_hash, sce_ecc_public_wrapped_key_t *wrapped_key)`

ECDSA signature verification.

#### Implemented as

- `R_SCE_ECDSA_secp384r1_SignatureVerify()`

#### Parameters

[in]	signature	Signature text information to be verified
[in,out]	message_hash	Message or hash value to be verified
[in]	wrapped_key	Input wrapped key of secp384r1 public key.

### ◆ ECDH\_secp256r1\_Init

`fsp_err_t(* sce_api_t::ECDH_secp256r1_Init) (sce_ecdh_handle_t *handle, uint32_t key_type, uint32_t use_key_id)`

secp256r1 ECDH Initialization.

#### Implemented as

- `R_SCE_ECDH_secp256r1_Init()`

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	key_type	Key exchange type
[in]	use_key_id	use key_id or not

### ◆ ECDH\_secp256r1\_PublicKeySign

`fsp_err_t(* sce_api_t::ECDH_secp256r1_PublicKeySign) (sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key, uint8_t *public_key, sce_ecdsa_byte_data_t *signature, sce_ecc_private_wrapped_key_t *wrapped_key)`

secp256r1 ECDH public key Signature.

#### Implemented as

- `R_SCE_ECDH_secp256r1_PublicKeySign()`

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	ecc_public_wrapped_key	For ECDHE, input a null pointer. For ECDH, input the wrapped key of a secp256r1 public key.
[in]	ecc_private_wrapped_key	secp256r1 private key for signature generation
[in,out]	public_key	User secp256r1 public key (512-bit) for key exchange.
[in,out]	signature	Signature text storage destination information
[in,out]	wrapped_key	For ECDHE, a private wrapped key generated from a random number. Not output for ECDH.

### ◆ ECDH\_secp256r1\_PublicKeyVerify

`fsp_err_t(* sce_api_t::ECDH_secp256r1_PublicKeyVerify) (sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, uint8_t *public_key_data, sce_ecdsa_byte_data_t *signature, sce_ecc_public_wrapped_key_t *wrapped_key)`

secp256r1 ECDH public key verification.

#### Implemented as

- `R_SCE_ECDH_secp256r1_PublicKeyVerify()`

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	ecc_public_wrapped_key	Public wrapped key area for signature verification
[in]	public_key_data	secp256r1 public key (512-bit)
[in]	signature	ECDSA secp256r1 signature of ecc_public_wrapped_key
[in,out]	wrapped_key	wrapped key of ecc_public_wrapped_key

### ◆ ECDH\_secp256r1\_SharedSecretCalculate

`fsp_err_t(* sce_api_t::ECDH_secp256r1_SharedSecretCalculate) (sce_ecdh_handle_t *handle, sce_ecc_public_wrapped_key_t *ecc_public_wrapped_key, sce_ecc_private_wrapped_key_t *ecc_private_wrapped_key, sce_ecdh_wrapped_key_t *shared_secret_wrapped_key)`

secp256r1 ECDH shared secret calculation.

#### Implemented as

- `R_SCE_ECDH_secp256r1_SharedSecretCalculate()`

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	ecc_public_wrapped_key	Public wrapped key
[in]	ecc_private_wrapped_key	Private wrapped key
[in,out]	shared_secret_wrapped_key	Wrapped key of shared secret Z calculated by ECDH key exchange

### ◆ ECDH\_secp256r1\_KeyDerivation

```
fsp_err_t(* sce_api_t::ECDH_secp256r1_KeyDerivation) (sce_ecdh_handle_t *handle,
sce_ecdh_wrapped_key_t *shared_secret_wrapped_key, uint32_t key_type, uint32_t kdf_type,
uint8_t *other_info, uint32_t other_info_length, sce_hmac_sha_wrapped_key_t *salt_wrapped_key,
sce_aes_wrapped_key_t *wrapped_key)
```

secp256r1 ECDH key derivation.

#### Implemented as

- R\_SCE\_ECDH\_secp256r1\_KeyDerivation()

#### Parameters

[in,out]	handle	ECDH handler (work area)
[in]	shared_secret_wrapped_key	Z wrapped key calculated by R_SCE_ECDH_secp256r1_SharedSecretCalculate
[in]	key_type	Derived key type
[in]	kdf_type	Algorithm used for key derivation calculation
[in]	other_info	Additional data used for key derivation calculation
[in]	other_info_length	Data length of other_info
[in]	salt_wrapped_key	Salt wrapped key
[in,out]	wrapped_key	Wrapped key corresponding to key_type.

### ◆ sce\_instance\_t

```
struct sce_instance_t
```

This structure encompasses everything that is needed to use an instance of this interface.

#### Data Fields

sce_ctrl_t *	p_ctrl	Pointer to the control structure for this instance.
sce_cfg_t const *	p_cfg	Pointer to the configuration structure for this instance.
sce_api_t const *	p_api	Pointer to the API structure for this instance.

### Typedef Documentation

**◆ sce\_rsa\_byte\_data\_t**

```
typedef sce_byte_data_t sce_rsa_byte_data_t
```

byte data

RSA byte data structure

**◆ sce\_ecdsa\_byte\_data\_t**

```
typedef sce_byte_data_t sce_ecdsa_byte_data_t
```

byte data

ECDSA byte data structure

**◆ sce\_ctrl\_t**

```
typedef void sce_ctrl_t
```

SCE Control block. Allocate an instance specific control block to pass into the API calls.

**Implemented as**

- [sce\\_instance\\_ctrl\\_t](#)

**Enumeration Type Documentation****◆ lifecycle\_t**

```
enum lifecycle_t
```

Data lifecycle

# Chapter 5 Copyright

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