# RENESAS

## **USER'S MANUAL**

ISL1561IRZ-EVALZ Evaluation Board

AN1812 Rev 0.00 May 8, 2014

### **General Description**

The ISL1561IRZ-EVALZ is a fixed gain dual port class-G differential amplifier designed for driving ADSL2+ and VDSL2 signals at very low power dissipation. The current feedback amplifiers operate on a single +14V power supply and internally generates higher supply voltages when needed to enable efficient power operation.

A USB micro-controller is integrated into the board to program the registers in the ISL1561 through a 3-pin serial protocol interface (SPI). Evaluation software is included in the evaluation kit to program the registers and set the quiescent current for each port at 0.5mA steps.

### **Detailed Description**

#### **SPI Control**

The micro-controller uses 4 logic signals (SCLK, SDI, SDO and CS) to communicate with ISL1561's 3-pin SPI: SCLK, SDATA and CS. Since SDATA for the ISL1561 is used for both data in and data out, a series of  $10k\Omega$  resistors are placed between SDI and SDO with SDI connected directly to SDATA in order for the micro-controller to read the registers in ISL1561.

### **Evaluation Software**

The GUI software is available to program the ISL1561IRZ-EVALZ evaluation board. Running the "ISL1561\_Installer\_V1.0.exe" will install the needed drivers for the program. The program files will be installed in "C:\Program Files\Intersil\ISL1561" and the file to run is "ISL1561.exe". When running the program, be sure the micro-controller is connected to the computer's USB port.

The ISL1561 starts up in disable mode. Clicking "Read All" will make both registers display "80". The two register boxes allow users to write and read. For example, when a user clicks in the box and types "0F", the program also enters in the same box the read register value, which is also "0F". If a different value is displayed, the register is not programmed correctly.

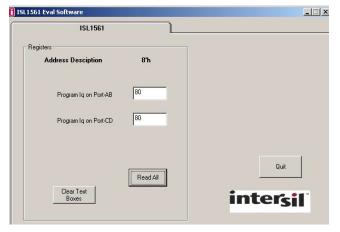


FIGURE 1. WINDOW'S GUI

#### **Programming Quiescent Current**

Table 1 lists quiescent current given the values entered in the register boxes. The register boxes in the GUI accept hexadecimal. Entering "OF" in the box will change the quiescent current to 7.2mA for that port. To change to a different value, users can click in the box to highlight the previous value and enter a new value.

| TABLE 1. | REGISTER     | VALUES | vs lo | q |
|----------|--------------|--------|-------|---|
|          | ILCOIO I EIL | TALOLO | 10 11 | 1 |

| VALUES IN EITHER PORTAB OR<br>PORTCD BOX | lq PER PORT<br>(mA) |  |
|--|---------------------|--|
| 80                                       | 2.5                 |  |
| OF                                       | 7.2                 |  |
| 10                                       | 10.3                |  |
| 7F                                       | 19.5                |  |

When the previous value is highlighted, users can also use the up and down arrow keys on the keyboard to change the value. If the current value is "OF", pressing the arrow key down will change the value to "OE" and pressing the key up will change the value to "10". Each step changes quiescent current by 500µA for the selected port.

The range of quiescent current for each port with the most significant bit (MSB) low is 8'h00 to 8'h7F and with the most significant bit (MSB) high is 8'h80 to 8h'FF. To change the quiescent current to 10.3mA/port, entering "1C" is the same as entering "9C" in the registers. The later sets the MSB high. Be careful when setting the MSB high for both ports because this will over-ride the boost operation as shown in Table 2 of the <u>ISL1561</u> datasheet.

When verifying reading and writing to the registers on an oscilloscope, note that the least significant bit (LSB) is loaded first and the most significant bit (MSB) is loaded last. The scope will display a "FO" instead of a "OF" because the micro-controller reads MSB first. Bit swapping was implemented on the software to load LSB first.

Figure 2 is a scope capture of SDATA in yellow, SCLK in red and CS in blue. From left to right, SDATA shows the first bit is low, which defines read. The next 3 bits, 110, defines reg3 as being read. The following 8 bits, 11110000, defines reg3 as the value of "F0". Reading and writing to the register only occurs when CS is held low.



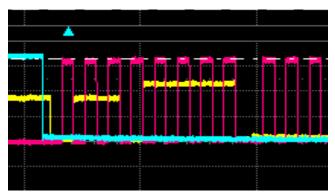


FIGURE 2. SDATA = "F0" IN PORTAB (reg3)

#### **Board Design Recommendation**

The ISL1561 is recommended to operate with less than 45pF of common mode parasitic on any of the four outputs. To minimize parasitic capacitance in the ISL1561 design, consider laying out short output traces and choosing low capacitance protection devices and line transformers with low interwinding capacitance in the signal path.

Close placement of the boost capacitors to the boost pins is necessary to minimize parasitic inductance in the boost supply path. On the ISL1561IRZ-EVALZ evaluation board, 1µF and 2.2µF capacitors are used instead of one in order to place the smaller footprint, a 1µF capacitor, close to the boost pins. An increase in ringing at the outputs caused by the rising edge of each boost event is observed if the boost capacitors are moved away from the package pins. Adding 5Ω in series to the boost capacitors will help reduce this common mode ringing.

The supply decoupling capacitors are also placed close to the supply pins to minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors, so close placement of the  $0.1\mu$ F capacitors on the supply pin will improve dynamic performance. The higher  $2.2\mu$ F value capacitors can be placed further from the supply pins as they provide low frequency decoupling.

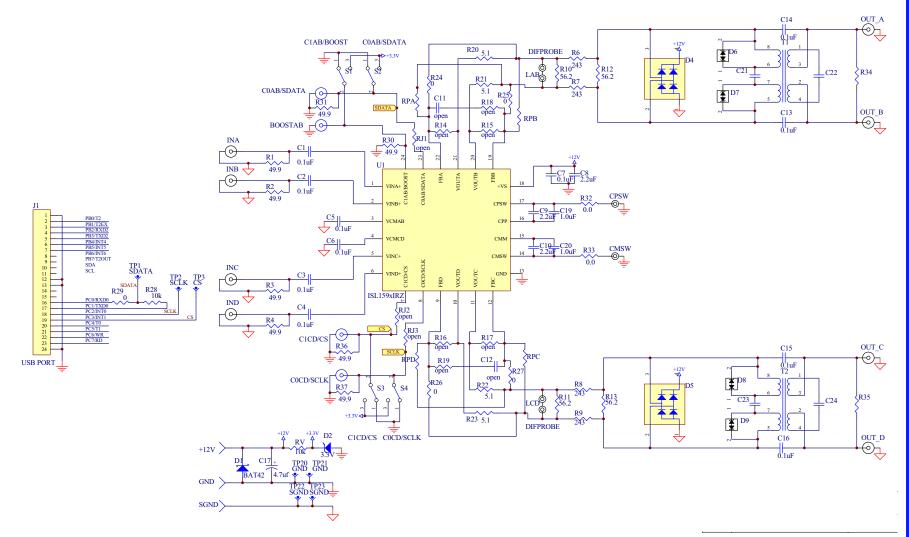
The thermal pad for the ISL1561 should be connected to ground. For good thermal control, running vias to a bottom pad helps dissipate heat away from the package.

#### **Output Resistor Loading**

In DSL applications, a line transformer is placed between the line driver and 100 $\Omega$  line. When the transformer is not available, an equivalent resistor load can be used. On PortAB, R6, R7, R10 and R12 allow for 100 $\Omega$  connected across OUTA-OUTB while keeping the load seen by the line driver 51 $\Omega$  (51 $\Omega$  is calculated from using a 1:1.4 transformer with 100 $\Omega$  on the line). When 100 $\Omega$  is connected across OUTA-OUTB, the resistor divider network attenuates the signal by -23.2dB.



### ISL1561IRZ-EVALZ Evaluation Board Schematic



ISL1561IRZ-EVALZ

### **Bill of Materials**

| DESIGNATION  | QTY | DESCRIPTION                              | MANUFACTURER           | MFG. PART NUMBER      |
|--|-----|--|------------------------|-----------------------|
| IC   | 1   | ISL1561IRZ                               | INTERSIL               | ISL1561IRZ            |
| None   | 1   | Printed Circuit Board                    |                        | ISL1561IRZ Eval Board |
| C1-C7  | 7   | 0.1µF, Ceramic Capacitors                | ANY                    | 0603                  |
| C8   | 1   | 2.2µF, Ceramic Capacitors                | ANY                    | 0603                  |
| C9, C10  | 2   | 2.2µF, Ceramic Capacitor                 | ANY                    | 0805                  |
| C13-C16  | 4   | 0.1µF, Ceramic Capacitor                 | ANY                    | 0805                  |
| C17  | 1   | 4.7µF, 25V, Ceramic Capacitor            | ANY                    | 3528                  |
| C19, C20   | 2   | 1.0µF, Ceramic Capacitor                 | ANY                    | 0402                  |
| C21, C23   | 2   | Open                                     | ANY                    | 1812                  |
| C22, C24   | 2   | Open                                     | ANY                    | -                     |
| R1-R4, R30, R31,<br>R36, R37                               | 8   | 49.9Ω, 1% Ceramic Resistor               | ANY                    | 0603                  |
| R6-R9  | 4   | 243Ω, 1% Ceramic Resistors               | ANY                    | 0805                  |
| R10-R13  | 4   | 56.2Ω, 1% Ceramic Resistor               | ANY                    | 0805                  |
| R20-R23  | 4   | 5.1Ω, 1% Ceramic Resistor                | ANY                    | 0805                  |
| R24-R27, R29   | 5   | 0.0Ω, 1% Ceramic Resistor                | ANY                    | 0603                  |
| R28  | 1   | 10kΩ, 1% Ceramic Resistor                | ANY                    | 0603                  |
| R32, R33   | 2   | 0.0Ω, 1% Ceramic Resistor                | ANY                    | 0402                  |
| RV   | 1   | Open                                     | ANY                    | 0805                  |
| C11, C12, R14-R19,<br>RJ1, RJ2, RJ3, RPA,<br>RPB, RPC, RPD | 15  | Open                                     | ANY                    | 0603                  |
| R34, R35   | 2   | Open                                     | ANY                    | -                     |
| D1   | 1   | Schottky Diode                           | ANY                    | SOD-123               |
| D2   | 1   | 3.3V Zener Diode                         | ANY                    | SOD-123               |
| D4, D5   | 2   | Open                                     | ANY                    | S0T-143               |
| D6-D9  | 4   | Open                                     | ANY                    | SOD-323               |
| S1-S4  | 4   | Open                                     | Toggle Switch GT11MCKE | -                     |
| T1, T2   | 2   | Open                                     | ANY                    | -                     |
| 14V, SGND, GND   | 4   | Banana Jack                              | ANY                    | 4-Pin                 |
| INA-IND, OUTA-<br>OUTD, CS, SDATA,<br>SCLK                 | 10  | BNC                                      | ANY                    | -                     |
|  | 4   | 6-32x.375"Lg., Phillips Pan Head         | OLANDER                | 6C37PPMS              |
|  | 4   | 6-32x.50"Lg., Hex Standoff, 1/4" Hex Dia | OLANDER                | 6C50HF4U              |

### **Evaluation Board Layout**

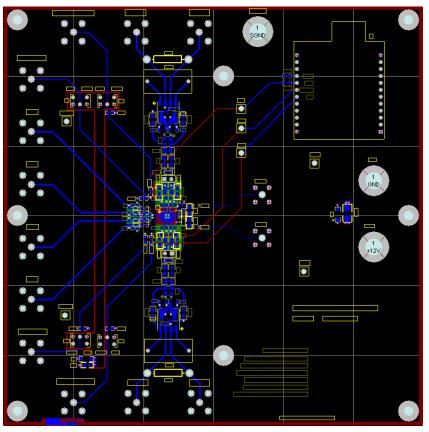


FIGURE 3. TOP VIEW



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