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User's Manual

μPD780232 Subseries

8-Bit Single-Chip Microcontrollers

μPD780232
μPD780233
μPD78F0233

Document No. U13364EJ2V0UD00 (2nd edition)
Date Published March 2003 N CP(K)
Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Major Revision in This Edition (1/2)

Page	Description
Throughout	Addition of product μPD780233GC-×××-8BT
	Change of description from FIP™ controller/driver to VFD controller/driver
	Addition of description of expanded supply voltage range version (V_{DD} = 2.7 to 5.5 V and V_{DD} = 3.0 to 5.5 V)
p.30	Addition of **Caution** to **1.8 Mask Option**
p.32	Addition of description on pull-down resistor to FIP0 to FIP23, FIP24 to FIP31, FIP32 to FIP39, FIP40 to FIP47, and FIP48 to FIP52 in **2.1 Pin Function List (2) Non-port pins**
p.35	Addition of description on pull-down resistor to **2.2.7 FIP0 to FIP23**
p.37	Change of **Table 2-1 Types of Pin I/O Circuits**
p.69 p.70 p.71 p.72	Modification of block diagrams **Figure 4-2 Block Diagram of P00 to P02** **Figure 4-3 Block Diagram of P20 and P27** **Figure 4-4 Block Diagram of P21, P24 to P26** **Figure 4-5 Block Diagram of P22 and P23**
pp.73 to 76	Addition of **Caution** to **4.2.3 Port 3** to **4.2.6 Port 6**
p.78	Change of description of **(2) Pull-up resistor option registers (PU0, PU2)** in **4.3 Port Function Control Registers**
p.80	Modification of **Table 4-4 Comparison Between Mask Options of Mask ROM Models and μPD78F0233**
pp.89, 90	Change of configuration in **6.2 Configuration of 8-Bit Remote Control Timer 9** and **6.3 Registers Controlling 8-Bit Remote Control Timer 9**
pp.97, 98	Change of **Figure 7-5 Timing of Interval Timer Operation**
p.99	Change of **Figure 7-6 Start Timing of 8-Bit Timer Register 8n (TM8n)**
p.100	Modification of cautions in **CHAPTER 8 WATCHDOG TIMER**
p.116	Addition of **9.5 How to Read A/D Converter Characteristics Table**
p.118 p.120 p.121 p.121	Addition of the following items to **9.6 Cautions for A/D Converter** (6) Input impedance of ANI0 to ANI3 pins (12) Timing at which A/D conversion result is undefined (13) Notes on board design (14) Internal equivalent circuit of ANI0 to ANI3 pins and permissible signal source impedance
pp.144 to 161	Modification of description in **(3) Communication operation**, **(4) Synchronization control**, and **(5) Timing of interrupt request signal generation** in **10.4.3 3-wire serial mode with automatic transmit/receive function**
p.163	Change of **Figure 11-1 Block Diagram of Serial Interface SIO3**
p.168	Change of description of **(6)** in **12.1 Function of VFD Controller/Driver** and addition of **Note**
p.171	Change of **Figure 12-2 Format of Display Mode Register 0** (change of set value of FOUT5 to FOUT0 and the number of VFD output pins) and addition of **Caution 4**
p.176	Addition of **Figure 12-7 Relationship Between Address Location of Display Data Memory and VFD Output (with 42 VFD Output Pins and 14 Patterns)**
p.185	Addition of **Remark** to **Table 13-1 Interrupt Sources**
p.187	Change of **Figure 13-1 Basic Configuration of Interrupt Function (D) Software interrupt**
p.189	Addition of **Cautions 3** and **4** to **Figure 13-2 Format of Interrupt Request Flag Register**
p.192	Change of **Figure 13-5 Format of External Interrupt Rising Edge Enable Register (EGP), External Interrupt Falling Edge Enable Register (EGN)** (The two registers were separately explained in the previous edition. In this version, they are combined and explained in one figure.)

Major Revision in This Edition (2/2)

Page	Description
p.216	Modification of **Table 16-1 Differences Between μPD78F0233 and Mask ROM Models**
p.218	Addition of **16.2 Flash Memory Features**
p.241	Addition of **CHAPTER 18 ELECTRICAL SPECIFICATIONS**
p.308	Addition of **CHAPTER 19 PACKAGE DRAWINGS**
p.309	Addition of **CHAPTER 20 RECOMMENDED SOLDERING CONDITIONS**
p.310	Change of **Table A-1 Major Differences Between μPD780232 and 780208 Subseries**
p.312	Modification of **APPENDIX B DEVELOPMENT TOOLS**
p.324	Addition of **APPENDIX C CAUTIONS ON DESIGNING TARGET SYSTEM**
p.328	Addition of **APPENDIX E REVISION HISTORY**

The mark ★ shows major revised points.

PREFACE

Target Readers This manual is intended for users who wish to understand the functions of the μPD780232 Subseries and to design and develop application systems and programs using these microcontrollers.

Purpose This manual is intended for the users to understand the functions described in the Organization below.

Organization The μPD780232 Subseries manual is divided into two parts: this manual and instructions (common to the 78K/0 Series)

μPD780232 Subseries User's Manual (This manual)	78K/0 Series Instructions User's Manual
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU function • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

☐ To understand the functions in general:
→ Read this manual in the order of the contents.

☐ How to interpret the register format:
→ For the circled bit number, the bit name is defined as a reserved word in RA78K0, and in CC78K0, already defined in the header file named sfrbit.h.

☐ When you know a register name and want to confirm its details:
→ Read **APPENDIX D REGISTER INDEX**.

☐ When you want to know the differences between the μPD780208 Subseries:
→ Read **APPENDIX A DIFFERENCES BETWEEN μPD780232 AND 780208 SUBSERIES**.

☐ When you want to know the details of the μPD780232 Subseries instruction function:
→ Read **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	High digits on the left and low digits on the right
Active low representation:	$\overline{xxx}$ (overscore pin or signal name)
Note:	Footnote for item marked with **Note** in the text.
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representations:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

★ **Related Documents**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780232 Subseries User's Manual	This manual
78K/0 Series Instructions User's Manual	U12326E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembler Preprocessor	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K Series Ver. 2.30 or Later System Simulator	Operation (Windows® Based)	U15373E
	External Part User Open Interface Specification	U15802E
ID78K Series Integrated Debugger Ver. 2.30 or Later	Operation (Windows Based)	U15185E
RX78K0 Real-time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver 3.12 or Later (Windows Based)		U14610E

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Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-780233-NS-EM4 Emulation Board	U14666E
IE-78001-R-A In-Circuit Emulator	U14142E
IE-78K0-R-EX1 In-Circuit Emulator	To be prepered

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the "Semiconductor Device Mount Manual" webpage (http://www.necel.com/pkg/en/mount/index.html)

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CHAPTER 1 GENERAL

1.1 Features

- Internal memory

Item / Part Number	Program Memory		Data Memory		
	Mask ROM	Flash Memory	High-Speed RAM	Buffer RAM	VFD Display RAM
μPD780232	16KB	—	768 bytes	32 bytes	112 bytes
★ μPD780233Note 1	24KB	—			
μPD78F0233	—	24KBNote 2			

Notes 1. Under development

2. 16 or 24KB can be selected by the memory size select register (IMS).

- Minimum instruction execution time changeable from high speed (0.4 μs) to low speed (6.4 μs)
- I/O port: 40 pins
- VFD controller/driver: Total display output pins: 53 (universal grid compatible)
  - Display current 15 mA: 20 pins
  - Display current 5 mA: 33 pins
- 8-bit resolution A/D converter: 4 channels
  - Supply voltage (AV_{DD} = 4.5 to 5.5 V)
- Serial interface: 2 channels
  - 3-wire serial mode (with automatic transmit/receive function): 1 channel
  - 2-wire serial mode (transmission only): 1 channel
- Timer: 4 channels
  - 8-bit remote control timer: 1 channel
  - 8-bit timer: 2 channels
  - Watchdog timer: 1 channel
- Vectored interrupt source: 14
- Supply voltage: V_{DD} = 4.5 to 5.5 VNote

★ **Note** Versions with an expanded supply voltage range (V_{DD} = 2.7 to 5.5 V and V_{DD} = 3.0 to 5.5 V) are also available. Since the electrical specifications vary depending on the product, refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS** for details.

1.2 Application Fields

Combined mini-component audio systems, separate mini-component audio systems, tuners, cassette decks, CD/MD players, and audio amplifiers

1.3 Ordering Information

Part Number	Package	Internal ROM
μPD780232GC-×××-8BT	80-pin plastic QFP (14 x 14)	Mask ROM
★ μPD780233GC-×××-8BT[Note]	80-pin plastic QFP (14 x 14)	Mask ROM
μPD78F0233GC-8BT	80-pin plastic QFP (14 x 14)	Flash memory

Note Under development

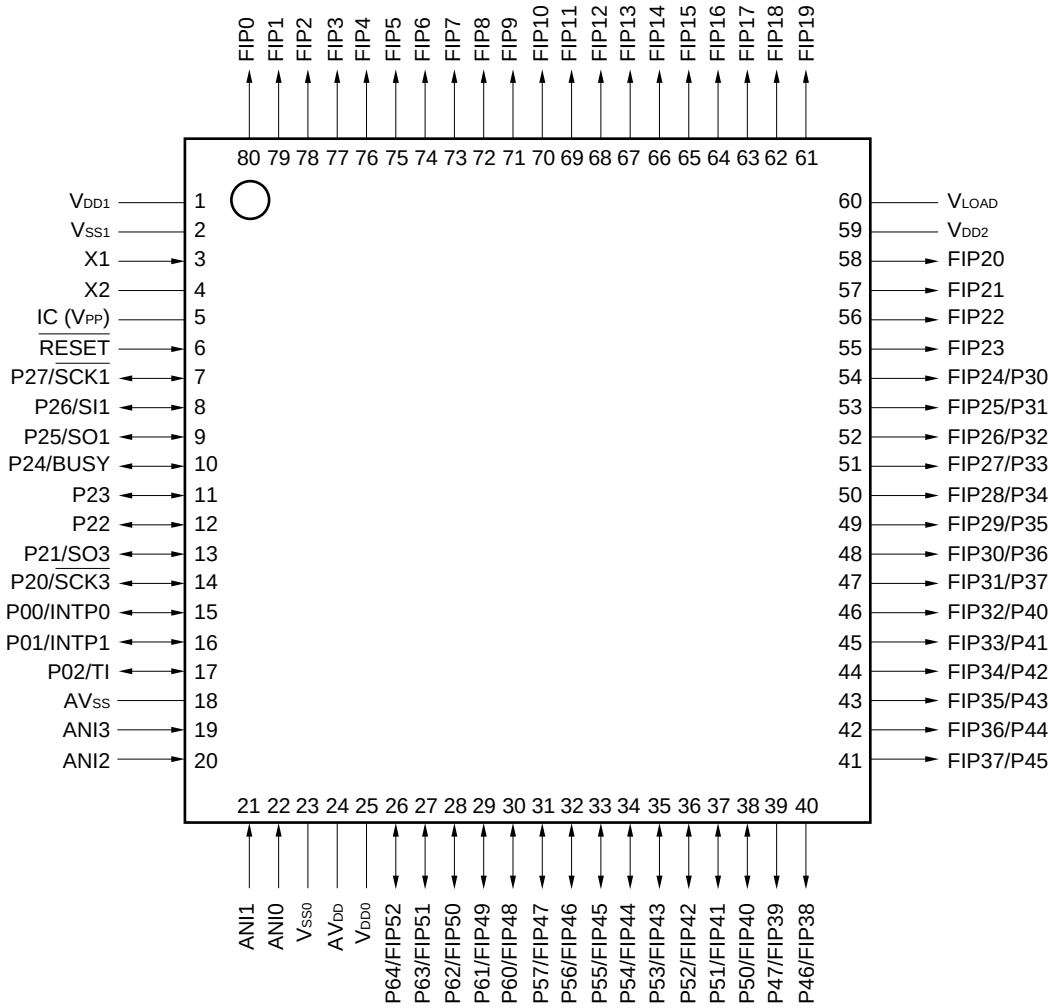
★ **Caution The ROM code number differs between the expanded supply voltage range versions and conventional products. Contact an NEC Electronics sales representative when ordering the product.**

Remark ××× indicates ROM code suffix.

1.4 Pin Configuration (Top View)

- **80-pin plastic QFP (14 x 14)**

★ **μPD780232GC-×××-8BT, 780233GC-×××-8BT[Note], 78F0233GC-8BT**



Note Under development

Cautions 1. Directly connect the IC (Internally Connected) pin to V_{SS1} in the normal operation mode.

2. Connect the AV_{DD} pin to V_{DD1}.

3. Connect the AV_{SS} pin to V_{SS1}.

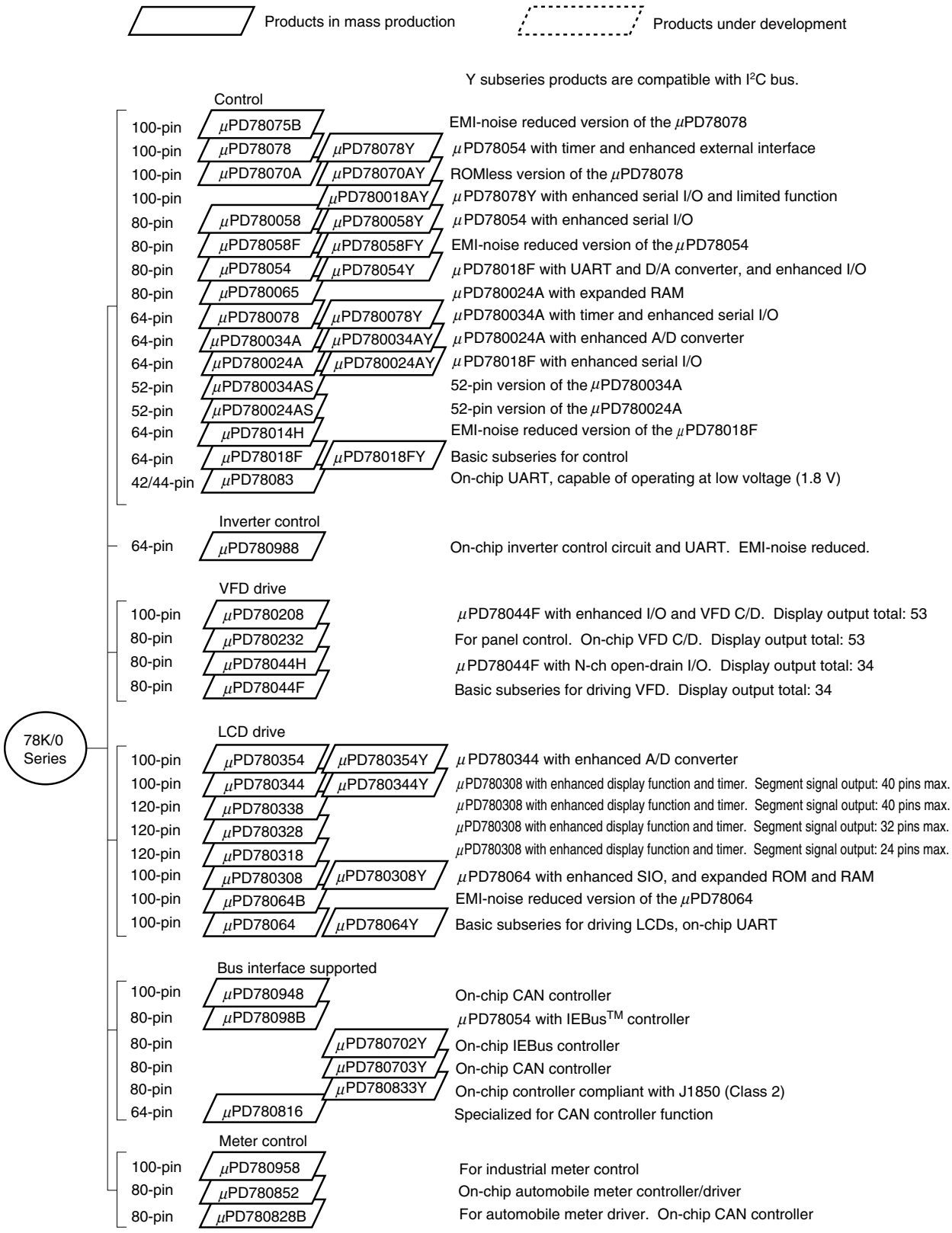
Remarks 1. When using the microcontroller in an application where the noise generated from the microcontroller must be suppressed, it is recommended that power be supplied to V_{DD0} and V_{DD1} from separate sources, and that V_{SS0} and V_{SS1} be connected to separate ground lines, to improve the noise immunity.

2. ( ): μPD78F0233

ANI0 to ANI3: Analog input
AV_{DD}: Analog power supply
AV_{SS}: Analog ground
BUSY: Busy
FIP0 to FIP52: Fluorescent indicator panel
IC: Internally connected
INTP0, INTP1: External interrupt input
P00 to P02: Port 0
P20 to P27: Port 2
P30 to P37: Port 3
P40 to P47: Port 4
P50 to P57: Port 5
P60 to P64: Port 6
$\overline{\text{RESET}}$: Reset
$\overline{\text{SCK1}}$, $\overline{\text{SCK3}}$: Serial clock
SI1: Serial input
SO1, SO3: Serial output
TI: Timer input
V_{DD0} to V_{DD2}: Power supply
V_{LOAD}: Negative power supply
V_{PP}: Programming power supply
V_{SS0}, V_{SS1}: Ground
X1, X2: Crystal

★ 1.5 78K/0 Series Lineup

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries name.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

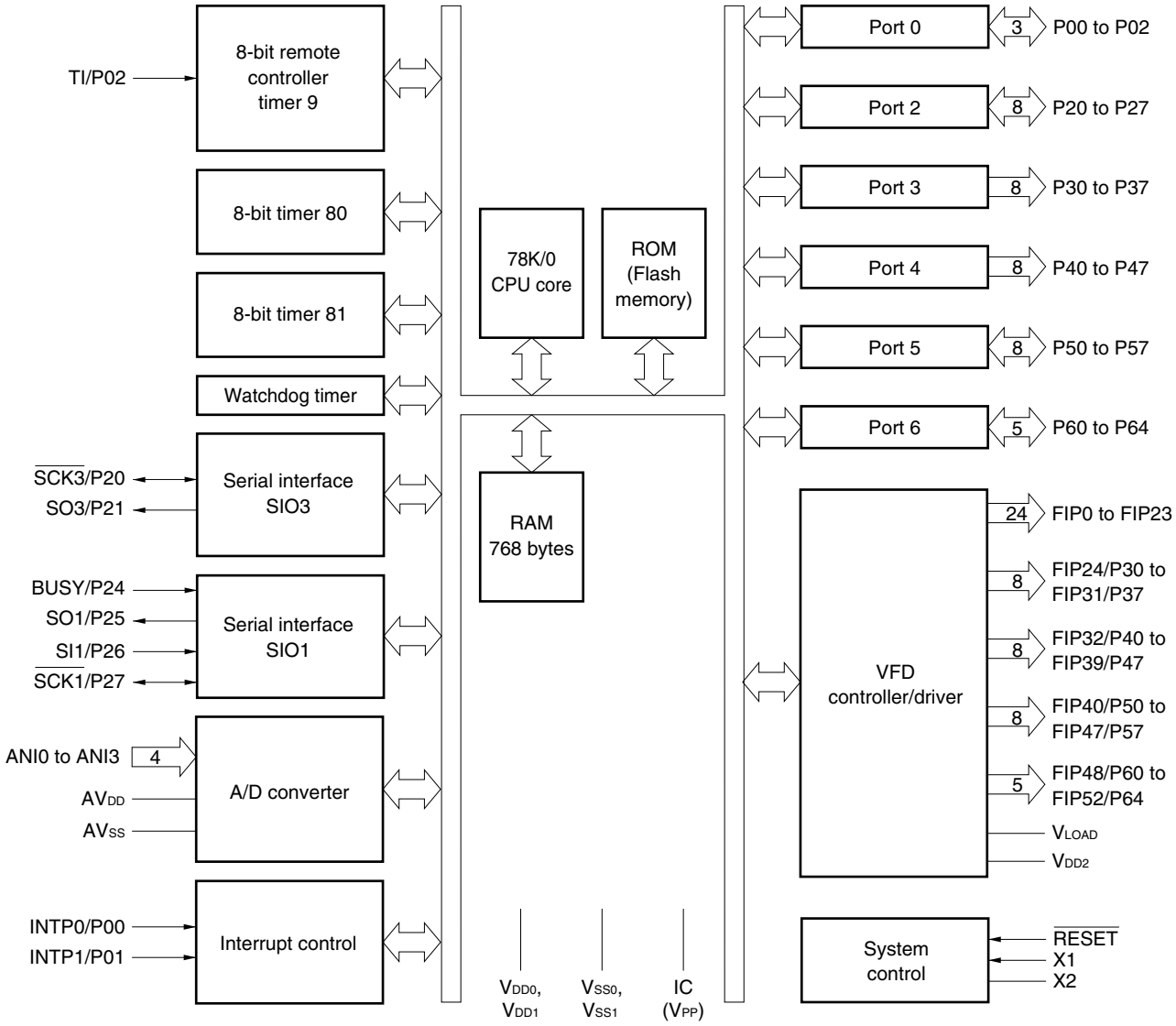
The major functional differences among the subseries are listed below.

- Non-Y subseries

Subseries Name \ Function		ROM Capacity (Bytes)	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD780034AS						–	4 ch			39		–
	μPD780024AS						4 ch	–					
	μPD78014H						8 ch			2 ch	53		√
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780354	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	3 ch (UART: 1 ch)	66	1.8 V	–
	μPD780344						8 ch	–					
	μPD780338	48 K to 60 K	3 ch	2 ch			–	10 ch	1 ch	2 ch (UART: 1 ch)	54		
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

1.6 Block Diagram



Remarks 1. The internal ROM capacity varies depending on the model.

2. ( ): μPD78F0233

1.7 Functional Outline

★

Item \ Part Number		μPD780232	μPD780233Note 1	μPD78F0233
Internal memory	ROM	Mask ROM		Flash memory
		16 KB	24 KB	24 KBNote 2
	High-speed RAM	768 bytes		
	Buffer RAM	32 bytes		
	VFD display RAM	112 bytes		
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Minimum instruction execution time		0.4/0.8/1.6/3.2/6.4 μs (main system clock: 5.0 MHz)		
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.		
I/O port (including VFD-multiplexed pins)		Total: 40 pins • CMOS I/O: 11 pins • P-ch open-drain I/O: 13 pins • P-ch open-drain output: 16 pins		
VFD controller/driver		Total display output: 53 pins • Display current 15 mA: 20 pins • Display current: 5 mA: 33 pins		
A/D converter		• 8-bit resolution × 4 channels • Supply voltage: AV_{DD} = 4.5 to 5.5 V		
Serial interface		• 3-wire serial mode (with automatic transmit/receive function): 1 channel • 2-wire serial mode (transmission only): 1 channel		
Timer		• 8-bit remote control timer: 1 channel • 8-bit timer: 2 channels • Watchdog timer: 1 channel		
Vectored interrupt source	Maskable	Internal: 10, external: 2		
	Non-maskable	Internal: 1		
	Software	1		
Supply voltage		V_{DD} = 4.5 to 5.5 VNote 3		
Package		80-pin plastic QFP (14 x 14)		

Notes 1. Under development

2. 16 or 24 KB can be selected by the memory size select register (IMS)

★ **3.** Versions with an expanded supply voltage range (V_{DD} = 2.7 to 5.5 V and V_{DD} = 3.0 to 5.5 V) are also available. Since the electrical specifications vary depending on the product, refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS** for details.

1.8 Mask Option

The mask ROM models (μPD780232, 780233) have mask options. By specifying the mask options when placing an order for these models, the pull-down resistor shown in Table 1-1 can be connected. If these mask options are used when pull-down resistor is necessary, the number of components can be decreased and the mounting area can be reduced.

Table 1-1 shows the mask options available for the μPD780232 Subseries.

Table 1-1. Mask Options of Mask ROM Models

Pin Name	Mask Option
FIP0 to FIP23 P30/FIP24 to P37/FIP31 P40/FIP32 to P47/FIP39	Pull-down resistors to V_{LOAD} can be connected in 1-bit units.
P50/FIP40 to P57/FIP47 P60/FIP48 to P64/FIP52	Pull-down resistors to V_{LOAD} or V_{SS0} can be connected in 1-bit units.

★ **Caution Adjust the number of pull-down resistors so that the total dissipation is not exceeded. (Refer to 12.7 Calculation of Total Power Dissipation.)**

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

(1) Port pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 3-bit I/O port Input/output mode can be specified in 1-bit units. An on-chip pull-up resistor can be used by software settings when this port is used as input port.	Input	INTP0
P01				INTP1
P02				TI
P20	I/O	Port 2 8-bit I/O port Input/output mode can be specified in 1-bit units. An on-chip pull-up resistor can be used by software settings when this port is used as input port.	Input	$\overline{\text{SCK3}}$
P21				SO3
P22				—
P23				—
P24				BUSY
P25				SO1
P26				SI1
P27				$\overline{\text{SCK1}}$
P30 to P37	Output	Port 3 P-ch open-drain 8-bit high-withstanding-voltage output port Pull-down resistor for V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-down resistors, however.	Output	FIP24 to FIP31
P40 to P47	Output	Port 4 P-ch open-drain 8-bit high-withstanding-voltage output port Pull-down resistor for V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-down resistors, however.	Output	FIP32 to FIP39
P50 to P57	I/O	Port 5 P-ch open-drain 8-bit high-withstanding-voltage I/O port Input/output mode can be specified in 1-bit units. Pull-down resistor for V_{LOAD} or V_{SS0} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-up resistors, however.	Output	FIP40 to FIP47
P60 to P64	I/O	Port 6 P-ch open-drain 5-bit high-withstanding-voltage I/O port Input/output mode can be specified in 1-bit units. Pull-down resistor for V_{LOAD} or V_{SS0} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-down resistors, however.	Output	FIP48 to FIP52

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00
INTP1		External interrupt request input.		P01
TI	Input	Timer input of 8-bit remote control timer 9.	Input	P02
$\overline{SCK3}$	I/O	Serial clock I/O of serial interface.	Input	P20
SO3	Output	Serial data output of serial interface.	Input	P21
BUSY	Input	Busy signal input to serial interface automatic transmission/reception.	Input	P24
SO1	Output	Serial data output of serial interface.	Input	P25
SI1	Input	Serial data input of serial interface.	Input	P26
$\overline{SCK1}$	I/O	Serial clock I/O of serial interface.	Input	P27
★ FIP0 to FIP23	Output	High-voltage high-current output of VFD controller/driver. Pull-down resistor for V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 have pull-down resistors.	Output	—
★ FIP24 to FIP31		High-voltage high-current output of VFD controller/driver. Pull-down resistor for V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-down resistors, however.		P30 to P37
★ FIP32 to FIP39				P40 to P47
★ FIP40 to FIP47		High-voltage high-current output of VFD controller/driver. Pull-down resistor for V_{LOAD} or V_{SS0} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-up resistors, however.	Input	P50 to P57
★ FIP48 to FIP52				P60 to P64
V_{LOAD}	—	Pull-down resistor connection of VFD controller/driver.	—	—
★ $\overline{RESET}$	Input	System reset input.	Input	—
X1	Input	Crystal connection for main system clock oscillation.	—	—
X2	—		—	—
ANI0 to ANI3	Input	Analog input for A/D converter.	Input	—
AV_{DD}	—	Analog power/reference voltage input to A/D converter. Set the same potential as V_{DD1}.	—	—
AV_{SS}	—	Ground potential for A/D converter. Set the same potential as V_{SS1}.	—	—
V_{DD0}	—	Positive power supply to ports.	—	—
V_{DD1}	—	Positive power supply (except ports, analog block, and VFD controller/driver)	—	—
V_{DD2}	—	Positive power supply to VFD controller/driver.	—	—
V_{SS0}	—	Ground potential for ports.	—	—
V_{SS1}	—	Ground potential (except ports and analog block).	—	—
V_{PP}	—	High voltage is applied to this pin when program is written/verified. In normal operation mode, directly connect to V_{SS1}.	—	—
IC	—	Internally connected. Directly connect to V_{SS1}.	—	—

2.2 Pin Functions

2.2.1 P00 to P02 (Port 0)

P00 to P02 are used as a 3-bit I/O port. These pins also have external interrupt request input and timer input functions in addition to the I/O port function.

Port 0 can be set to the following operation modes in 1-bit units.

(1) Port mode

P00 to P02 function as a 3-bit I/O port.

This 2-bit port can be set to the input or output mode in 1-bit units by port mode register 0 (PM0). When used as an input port, the internal pull-up resistor can be connected using pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P02 functions as external interrupt request input and timer input pins.

(a) INTP0, INTP1

INTP0 and INTP1 input external interrupt requests whose valid edge can be specified (to be the rising edge, falling edge, or both the rising and falling edges).

(b) TI

TI input timer of the 8-bit remote control timer.

2.2.2 P20 to P27 (Port 2)

P20 to P27 constitute an 8-bit I/O port, port 2. These pins also have functions to I/O data of the serial interface, clock, and automatic transmit/receive busy input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an 8-bit I/O port. This port can be set to the input or output mode in 1-bit units using port mode register 2 (PM2). When the port is used as an input port, the internal pull-up resistor can be used if so specified by pull-up resistor option register 2 (PU2).

(2) Control mode

P20 to P27 are used to input/output serial interface data, clock, and input automatic transmit/receive busy signals.

(a) SI1, SO1, SO3

These are I/O pins of the serial data of the serial interface.

(b) $\overline{\text{SCK1}}$, $\overline{\text{SCK3}}$

These are I/O pins of the serial clock of the serial interface.

(c) BUSY

This is an I/O pin of the serial data of the serial interface.

2.2.3 P30 to P37 (Port 3)

P30 to P37 constitute an 8-bit output port. These pins are also used as VFD controller/driver output pins.
The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P37 function as an 8-bit output port.
These pins are P-ch open-drain pins. Pull-down resistors can be connected to these pins of the mask ROM models by mask option in 1-bit units. The μPD78F0233 does not have pull-down resistors.

(2) Control mode

P30 to P37 function as the output pins of the VFD controller/driver (FIP24 to FIP31).

2.2.4 P40 to P47 (Port 4)

P40 to P47 constitute an 8-bit output port. These pins are also used as VFD controller/driver output pins.
The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P47 function as an 8-bit output port.
These pins are P-ch open-drain pins. Pull-down resistors can be connected to these pins of the mask ROM models by mask option in 1-bit units. The μPD78F0233 does not have pull-down resistors.

(2) Control mode

P40 to P47 function as the output pins of the VFD controller/driver (FIP32 to FIP39).

2.2.5 P50 to P57 (Port 5)

P50 to P57 constitute an 8-bit I/O port. These pins are also used as VFD controller/driver output pins.
The following operation modes can be specified in 1-bit units.

(1) Port mode

P50 to P57 function as an 8-bit I/O port in this mode.
These pins are P-ch open-drain pins. Pull-down resistors can be connected to these pins of the mask ROM models by mask option. Pull-down resistor to V_{LOAD} or V_{SS0} can be selected in 1-bit units. The μPD78F0233 does not have pull-down resistors.

(2) Control mode

P50 to P57 function as the output pins of the VFD controller/driver (FIP40 to FIP47).

2.2.6 P60 to P64 (Port 6)

P60 to P64 constitute a 5-bit I/O port. These pins are also used as VFD controller/driver output pins.
The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 to P64 function as a 5-bit I/O port.
These pins are P-ch open-drain pins. Pull-down resistors can be connected to these pins of the mask ROM models by mask option. Pull-down resistor to V_{LOAD} or V_{SS0} can be selected in 1-bit units. The μPD78F0233 does not have pull-down resistors.

(2) Control mode

P60 to P64 function as the output pins of the VFD controller/driver (FIP48 to FIP52).

2.2.7 FIP0 to FIP23

These are the output pins of the VFD controller/driver.

★ Pull-down resistors can be connected to these pins of the mask ROM models by mask option in 1-bit units.

2.2.8 V_{LOAD}

This pin connects a pull-down resistor to the VFD controller/driver.

2.2.9 AV_{DD}

This pin supply an analog voltage to the A/D converter.

Always keep this pin at the same potential as the V_{DD1} pin even when the A/D converter is not used.

2.2.10 AV_{SS}

This is the ground pin of the A/D converter.

Always keep this pin at the same potential as the V_{SS1} pin even when the A/D converter is not used.

2.2.11 $\overline{\text{RESET}}$

This pin inputs an active-low system reset signal.

2.2.12 X1 and X2

These pins connect a crystal resonator for main system clock oscillation.

To supply an external clock, input it to X1, and input a signal reverse to that input to X1, to X2.

2.2.13 ANI0 to ANI3

These are the input pins of the A/D converter.

2.2.14 V_{DD0} to V_{DD2}

V_{DD0} supplies a positive voltage to the ports.

V_{DD1} supplies a positive voltage to the internal function blocks other than the ports, analog block, and VFD controller/driver.

V_{DD2} supplies a positive voltage to the VFD controller/driver.

2.2.15 V_{SS0} and V_{SS1}

V_{SS0} is the ground pin for the ports.

V_{SS1} is the ground pin for the internal function blocks other than the ports and analog block.

2.2.16 V_{PP} (μPD78F0233 only)

A high voltage is applied to this pin when the flash memory programming mode is used and when a program is written or verified.

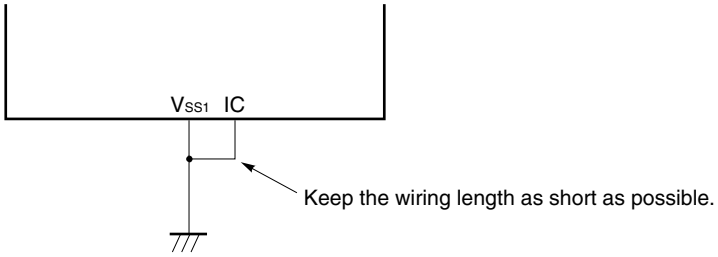
Directly connect this pin to V_{SS1} in normal operation mode.

★ 2.2.17 IC (Mask ROM models)

The IC (Internally Connected) pin sets a test mode in which the μPD780232 Subseries is tested before shipment. Usually, connect the IC pin directly to V_{SS1} with as short a wiring length as possible.

If there is a potential difference between the IC and V_{SS1} pins because the wiring length between the IC and V_{SS1} pin is too long, or external noise is superimposed on the IC pin, your program may not run correctly.

○ Directly connect IC pin to V_{SS1}.



2.3 I/O Circuits of Pins and Connections of Unused Pins

The I/O circuit types of each pin and recommended connection of unused pins are shown in Table 2-1. For the I/O configuration of each circuit type, refer to Figure 2-1.

★ **Table 2-1. Types of Pin I/O Circuits**

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pin
P00/INTP0	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P01/INTP1			
P02/TI			
P20/$\overline{SCK3}$			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/SO3			
P22, P23			
P24/BUSY			
P25/SO1			
P26/SI1			
P27/$\overline{SCK1}$			
Mask ROM models (μPD780232, 780233)			
FIP0 to FIP23	14-F	Output	Leave open.
P30/FIP24 to P37/FIP31			
P40/FIP32 to P47/FIP39			
P50/FIP40 to P57/FIP47	15-D	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor[Note]. Output: Leave open.
P60/FIP48 to P64/FIP52			
IC	—	—	Directly connect to V_{SS1}.
Flasyh memory model (μPD78F0233)			
FIP0 to FIP23	14-C	Output	Leave open.
P30/FIP24 to P37/FIP31	14-E		
P40/FIP32 to P47/FIP39			
P50/FIP40 to P57/FIP47	15-E	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P60/FIP48 to P64/FIP52			
V_{PP}	—	—	Directly connect to V_{SS1}.
$\overline{RESET}$	2	Input	—
ANI0 to ANI3	7	Input	Independently connect to V_{DD0} or V_{SS0}.
AV_{DD}	—	—	Connect to V_{DD1}.
AV_{SS}			Connect to V_{SS1}.
V_{LOAD}			

Note Leave open when a pull-down resistor is connected by the mask option.

Figure 2-1. Pin I/O Circuits (1/2)

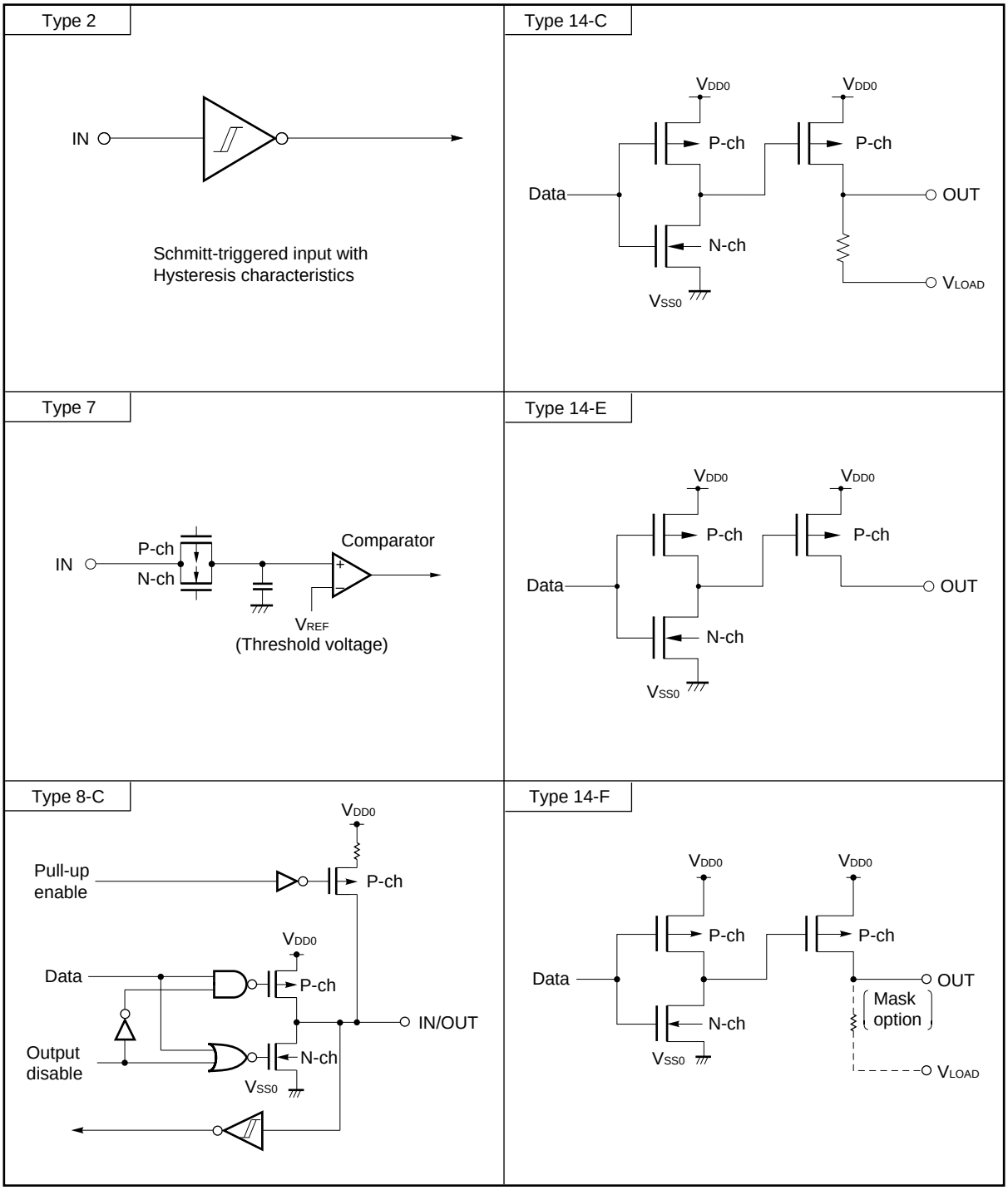
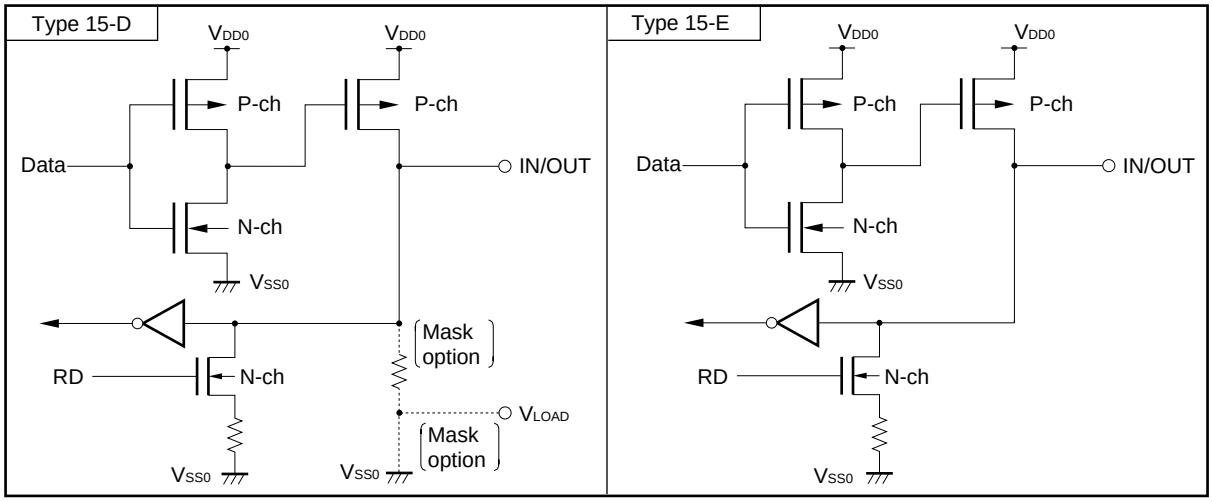


Figure 2-1. Pin I/O Circuits (2/2)

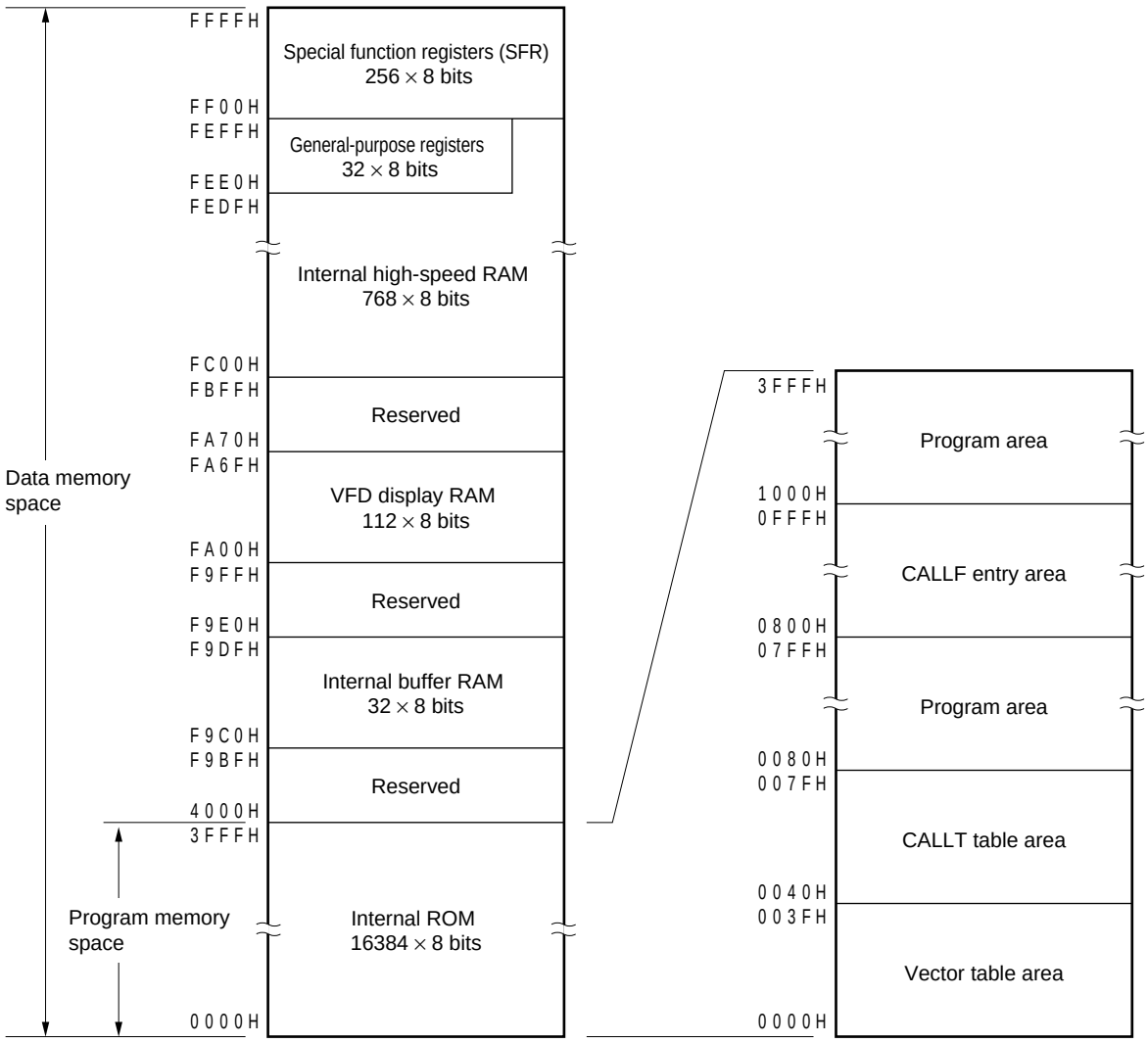


CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

Each model in the μPD780232 Subseries can access a memory space of 64KB. Figures 3-1 to 3-3 show the memory map.

Figure 3-1. Memory Map (μPD780232)



★ **Figure 3-2. Memory Map (μPD780233)**

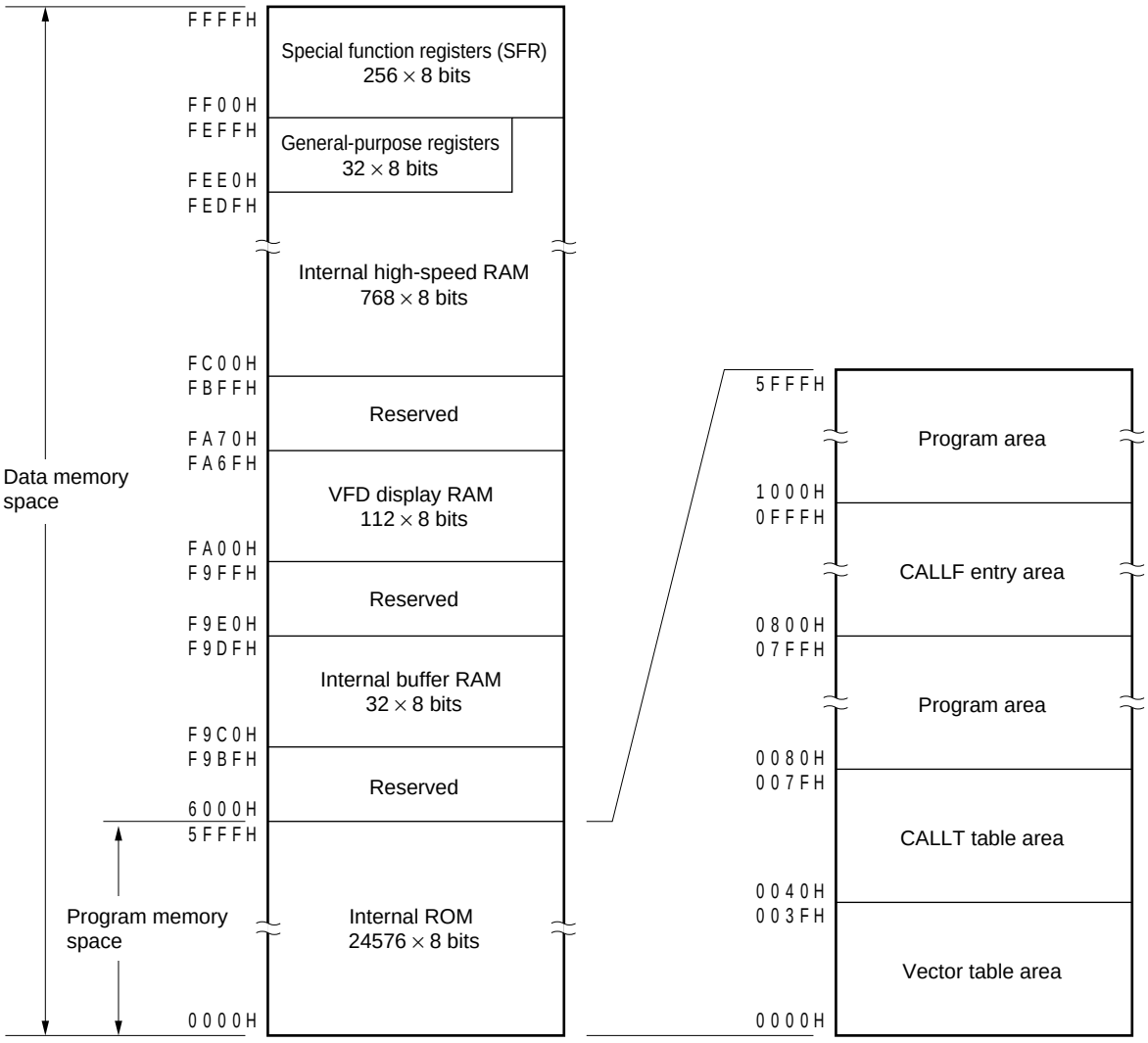
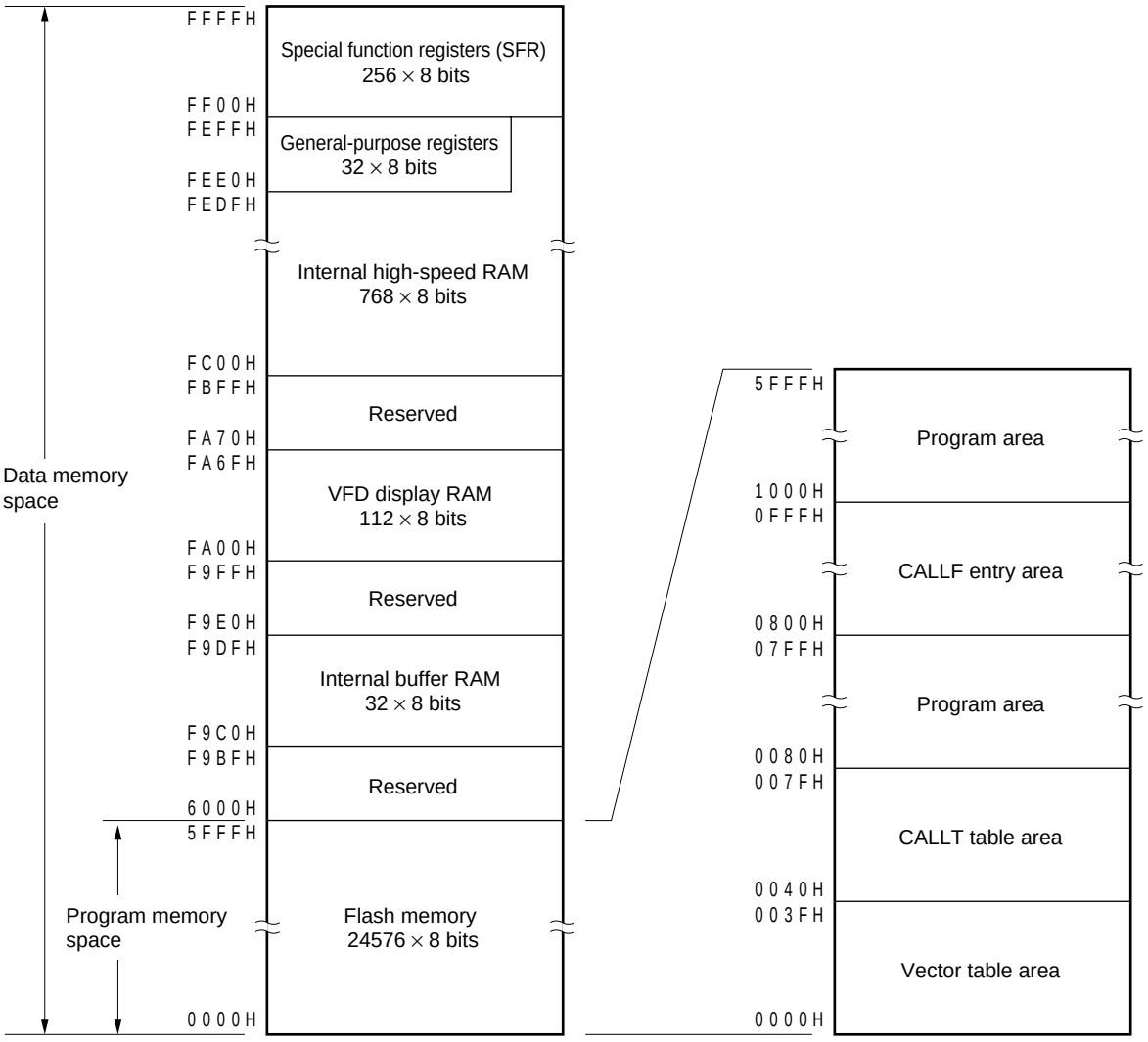


Figure 3-3. Memory Map (μPD78F0233)



3.1.1 Internal program memory space

The internal program memory space stores programs and table data. Usually, this space is accessed by program counter (PC).

Each model in the μPD780232 Subseries has an internal ROM (or flash memory) of the following capacity.

Table 3-1. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD780232	Mask ROM	16384 × 8 bits (0000H to 3FFFH)
★ μPD780233		24576 × 8 bits (0000H to 5FFFH)
μPD78F0233	Flash memory	24576 × 8 bits (0000H to 5FFFH)

The following areas are allocated to the internal program memory space.

(1) Vector table area

A 64-byte area of addresses 0000H to 003FH is reserved as a vector table area. Program start addresses to which execution is to branch when the $\overline{\text{RESET}}$ signal is input or when an interrupt request is generated are stored in this area. Of a 16-bit address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

Table 3-2. Vector Table

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	$\overline{\text{RESET}}$ input	0010H	INTKS
0004H	INTWDT	0012H	INTCSI1
0006H	INTP0	0014H	INTCSI3
0008H	INTP1	0016H	INTTM80
000AH	INTTM90	0018H	INTTM81
000CH	INTTM91	001AH	INTAD
000EH	INTTM92	003EH	BRK

(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can be used to store the subroutine entry addresses of the 1-byte call instruction (CALLT).

(3) CALLF instruction entry area

From an area of 0800H to 0FFFH, a subroutine can be directly called by using the 2-byte call instruction (CALLF).

3.1.2 Internal data memory space

The μPD780232 Subseries has the following RAM.

(1) Internal high-speed RAM

The internal high-speed RAM is assigned to 768-byte area FC00H to FEFFH.

Of these addresses, FEE0H to FEFFH constitute a 32-byte area to which four banks of general-purpose registers, with each bank consisting of eight 8-bit registers, are allocated.

★ This area cannot be used as a program area in which instructions are written and executed.

The internal high-speed RAM can also be used as a stack memory.

★ (2) Internal buffer RAM

The internal buffer RAM is allocated to the 32-byte area F9C0H to F9DFH. The internal buffer RAM is used to store the transmit/receive data in 3-wire serial mode (with automatic transmit/receive function). When 3-wire serial mode with automatic transmit/receive function is not used, the internal buffer RAM can be used as ordinary RAM.

(3) VFD display RAM

The VFD display RAM is allocated to the 112-byte area FA00H to FA6FH. This RAM can also be used as a normal RAM.

3.1.3 Special function register (SFR) area

Special function registers (SFR) are allocated to the area FF00H to FFFFH as on-chip peripheral hardware (refer to **Table 3-3 Special Function Registers** in **3.2.3 Special function register (SFR))**.

Caution Do not access an address to which no SFR is allocated.

3.1.4 Data memory addressing

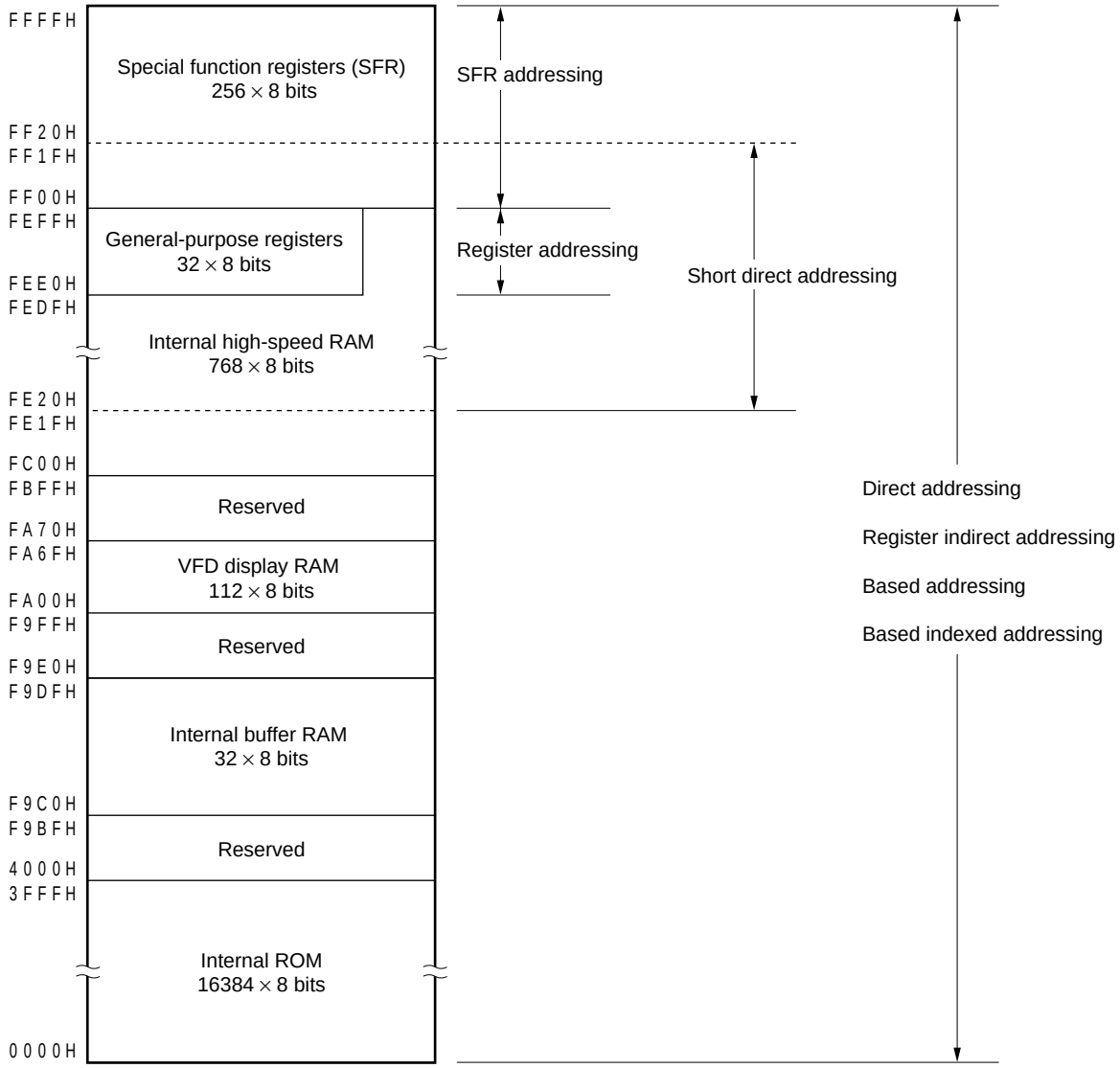
Specifying the address of the instruction to be executed next, or specifying an address of the register or memory to be manipulated when an instruction is executed is called addressing.

The address of the instruction to be executed next is addressed by the program counter (PC) (for details, refer to **3.3 Instruction Address Addressing**).

The μPD780232 Subseries has many addressing modes to improve the operability when a memory area to be manipulated during instruction execution is addressed. Particularly in the areas to which the data memory is assigned, the special function registers (SFR) and general-purpose registers can be addressed in accordance with their functions. All the 64KB data memory, 0000H to FFFFH, can also be addressed. Figures 3-4 to 3-6 illustrate how the data memory is addressed.

For details on each addressing mode, refer to **3.4 Operand Address Addressing**.

Figure 3-4. Data Memory Addressing (μPD780232)



★ **Figure 3-5. Data Memory Addressing (μPD780233)**

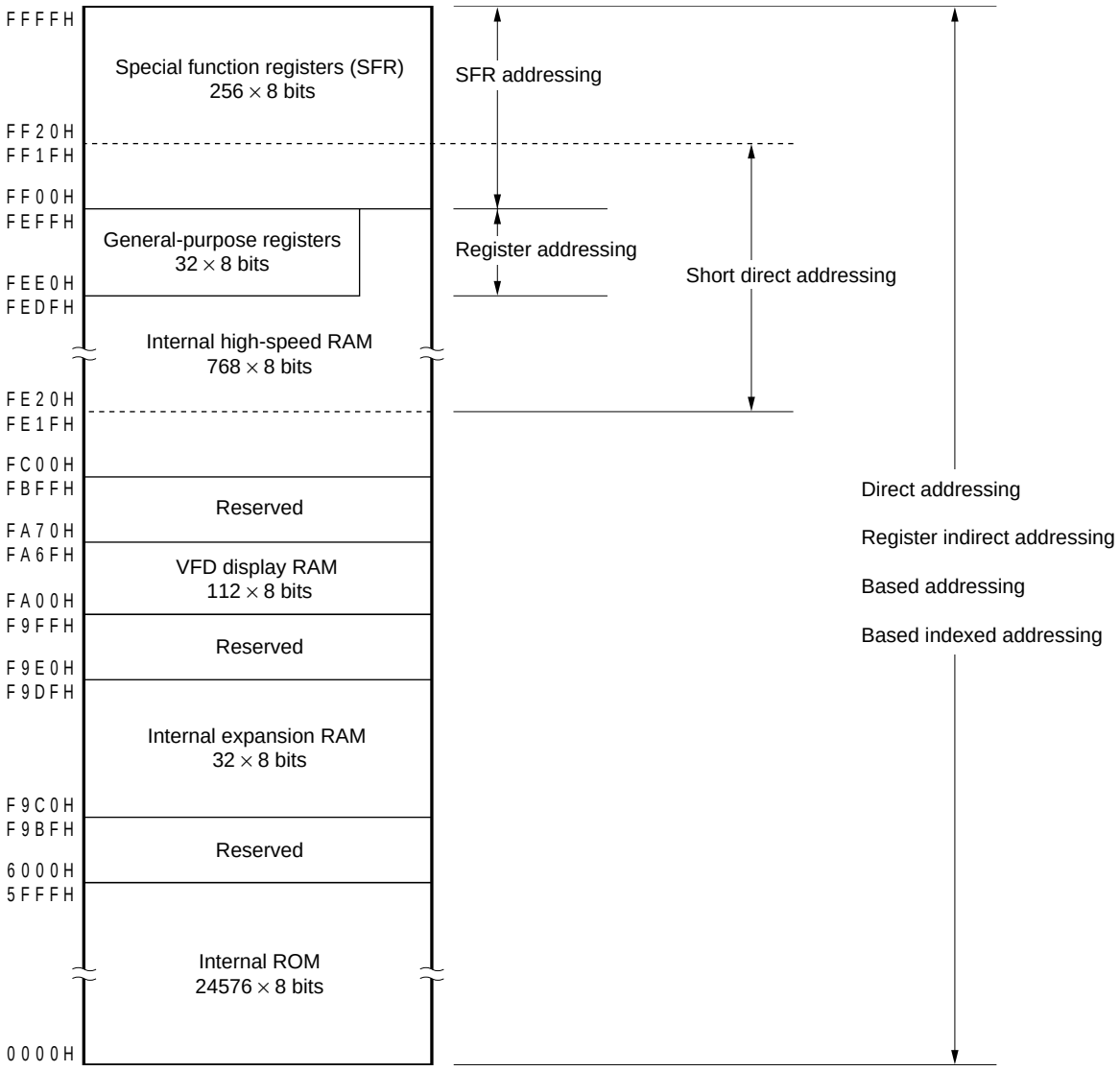
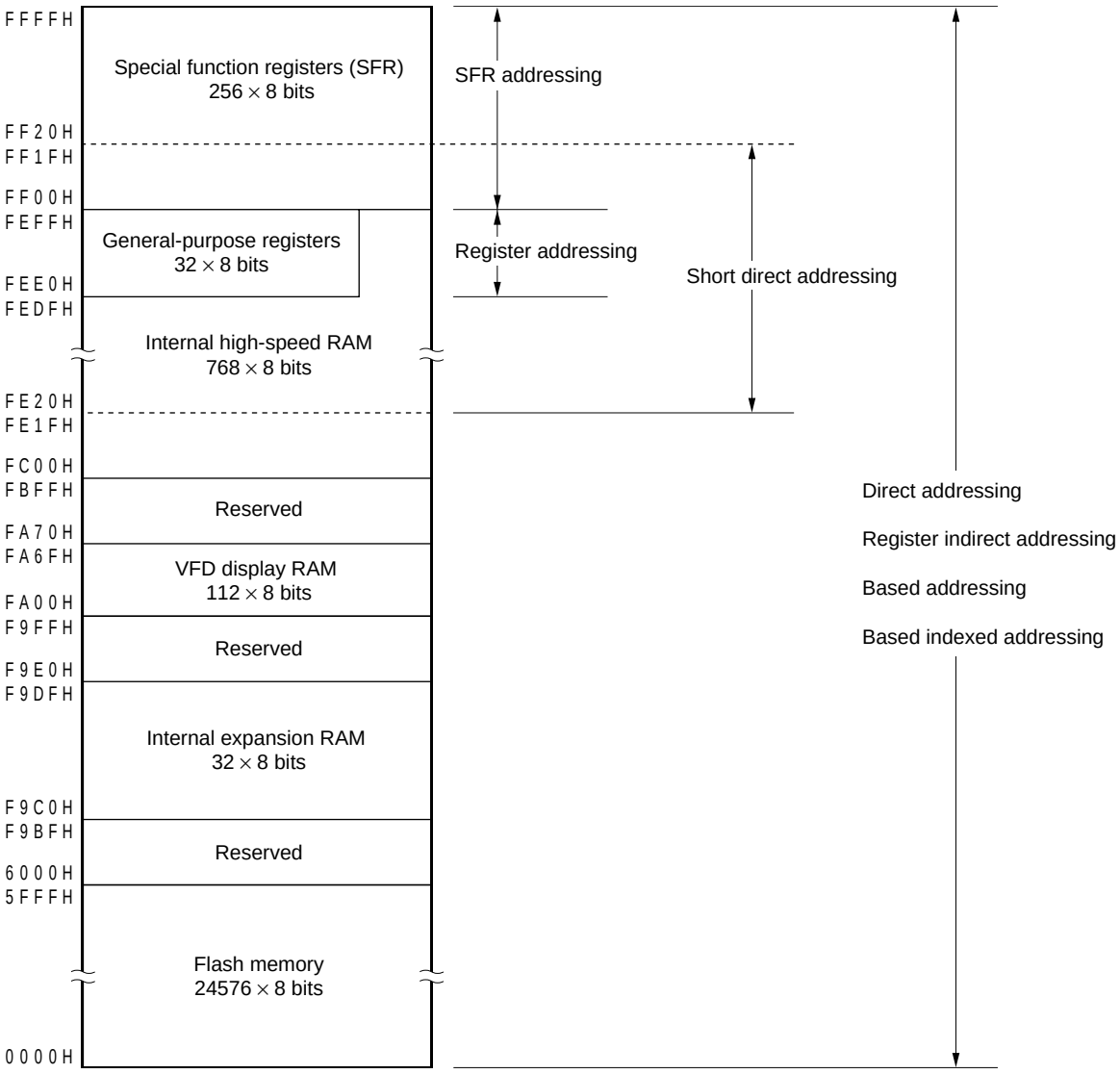


Figure 3-6. Data Memory Addressing (μPD78F0233)



3.2 Processor Registers

The μPD780232 Subseries units incorporate the following processor registers.

3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. A program counter (PC), a program status word (PSW) and a stack pointer (SP) are control registers.

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed. In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data and register contents are set.

$\overline{\text{RESET}}$ input sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-7. Configuration of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register including various flags to be set/reset by instruction execution. Program status word contents are automatically stacked upon interrupt request generation or PUSH PSW instruction execution and are automatically reset upon execution of the RETB, RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 3-8. Configuration of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

(a) Interrupt enable flag (IE)

This flag controls acknowledgement of an interrupt request by the CPU.

When IE = 0, all interrupts except the non-maskable interrupt are disabled (DI status).

When IE = 1, the interrupts are enabled (EI status). At this time, acknowledgement of interrupt requests is controlled with an in-service priority flag (ISP) and an interrupt mask flag for various interrupt sources and a priority specification flag.

The interrupt enable flag is also reset to 0 when the DI instruction or an interrupt request has been acknowledged and is set to 1 when the EI instruction has been executed.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0 and RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information which indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flag (ISP)

This flag manages the priority of acknowledgeable maskable vectored interrupts.

When ISP = 0, the vectored interrupt request specified by the priority specification flag registers (PR0L and PR0H) (refer to **13.3 (3) Priority specification flag registers (PR0L and PR0H)**) to have a low priority is disabled. Whether an interrupt request is actually acknowledged is controlled by the status of the interrupt enable flag (IE).

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shifted out value upon rotate instruction execution and functions as a bit accumulator during bit manipulation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area (FC00H to FEFFH) can be set as the stack area.

Figure 3-9. Configuration of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (saved) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-10 and 3-11.

Caution Since $\overline{\text{RESET}}$ input makes SP contents undefined, be sure to initialize the SP before instruction execution.

Figure 3-10. Data Saved to Stack Memory

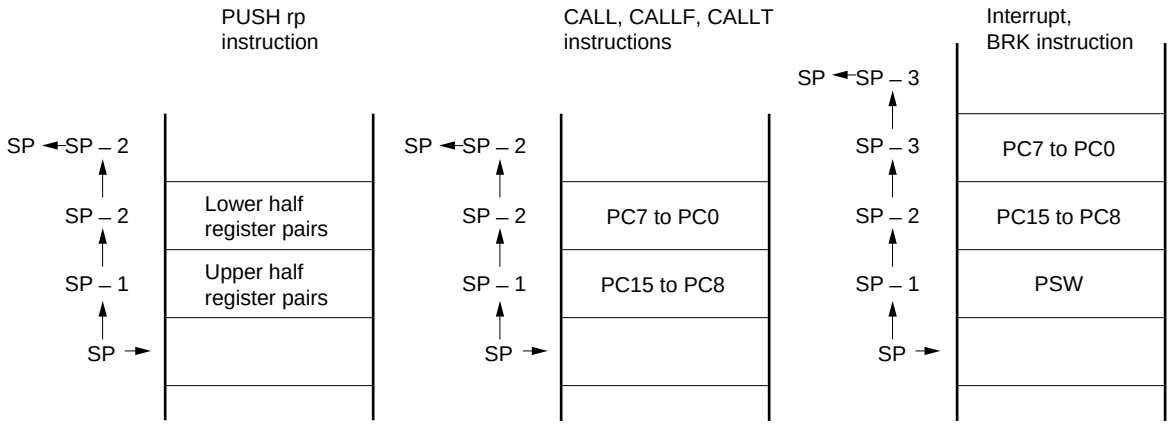
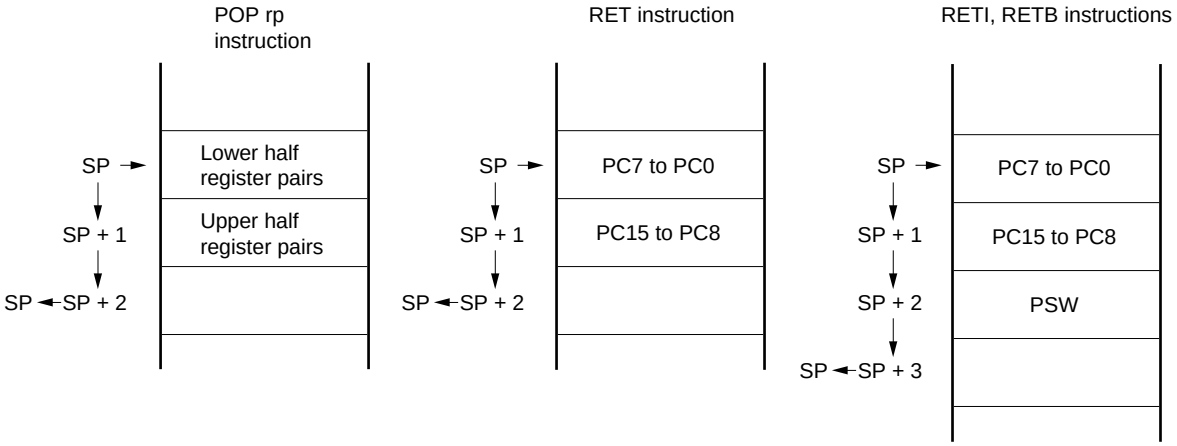


Figure 3-11. Data Restored from Stack Memory



3.2.2 General-purpose registers

A general-purpose register is mapped at particular addresses (FEE0H to FEFFH) of the data memory. It consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

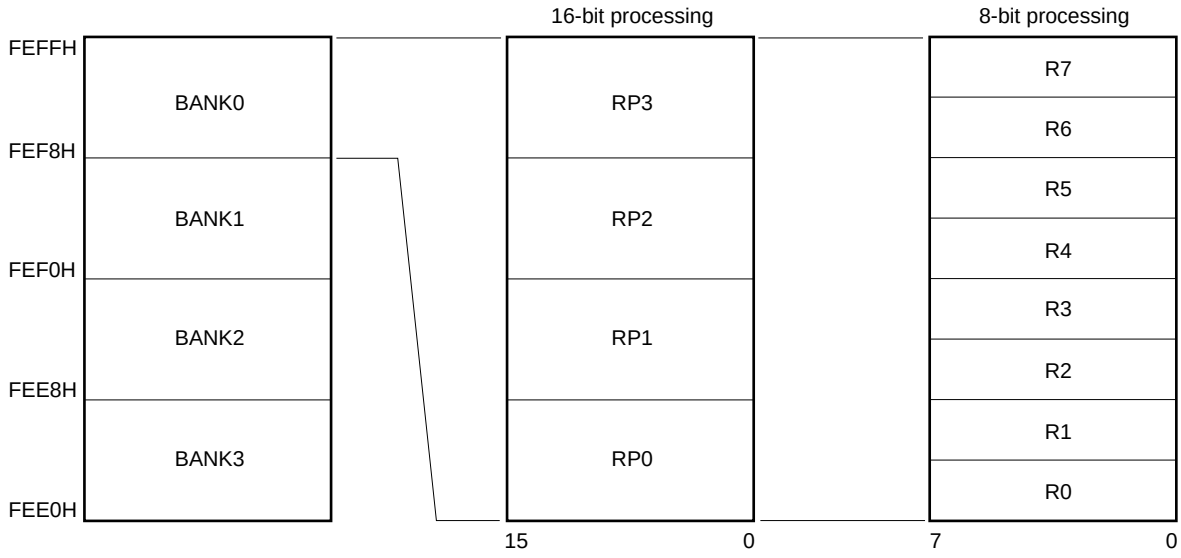
Each register can also be used as an 8-bit register. Two 8-bit registers can be used in pairs as a 16-bit register (AX, BC, DE, and HL).

They can be written in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

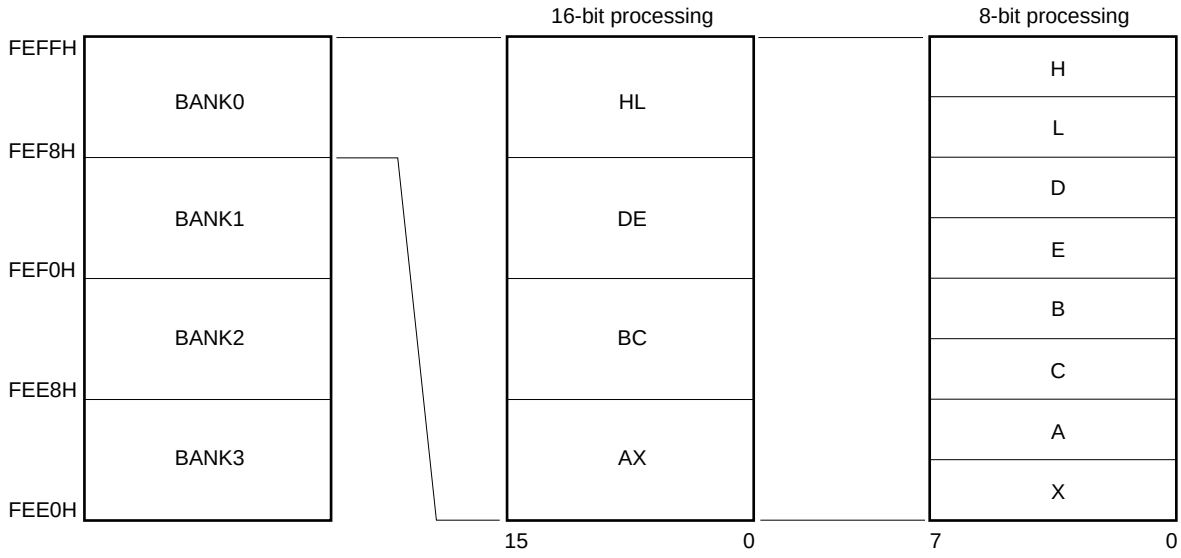
Register banks to be used for instruction execution are set with the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interruption for each bank.

Figure 3-12. Configuration of General-Purpose Register

(a) Absolute Name



(b) Function Name



3.2.3 Special function registers (SFR: Special Function Register)

Unlike a general-purpose register, each special function register has special functions. It is allocated in the FF00H to FFFFH area.

The special function register can be manipulated, like the general-purpose register, with the operation, transfer and bit manipulation instructions. Manipulatable bit units, 1, 8, and 16, depend on the special function register type.

Each manipulation bit unit can be specified as follows.

- **1-bit manipulation**
  Write the symbol reserved with assembler for the 1-bit manipulation instruction operand (sfr.bit).
  This manipulation can also be specified with an address.
- **8-bit manipulation**
  Write the symbol reserved with assembler for the 8-bit manipulation instruction operand (sfr).
  This manipulation can also be specified with an address.
- **16-bit manipulation**
  Write the symbol reserved with assembler for the 16-bit manipulation instruction operand (sfrp).
  When addressing an address, write an even address.

Table 3-3 gives a list of special function registers. The meaning of items in the table is as follows.

- **Symbol**
  This is a symbol to indicate an address of the special function register.
  The symbols shown in this column are reserved words of the RA78K0, and have already been defined in the header file called “sfrbit.h” of the CC78K0. These can be written as instruction operands if the RA78K0, ID78K0-NS, ID78K0, or SM78K0 is used.
- **R/W**
  Indicates whether the corresponding special function register can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- **Manipulatable bit units**
  √ indicates the bit unit (1, 8, or 16 bits) in which the register can be manipulated. – indicates that the register cannot be manipulated in the indicated bit unit.
- **After reset**
  Indicates each register status upon $\overline{\text{RESET}}$ input.

Table 3-3. Special Function Registers (1/2)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Units			After Reset
					1 bit	8 bits	16 bits	
FF00H	Port 0	P0		R/W	√	√	—	00H
FF02H	Port 2	P2			√	√	—	
FF03H	Port 3	P3			√	√	—	
FF04H	Port 4	P4			√	√	—	
FF05H	Port 5	P5			√	√	—	
FF06H	Port 6	P6			√	√	—	
FF07H	Port level read register 5	PT5		R	√	√	—	Undefined
FF08H	8-bit compare register 80	CR80		R/W	—	√	—	00H
FF09H	8-bit compare register 81	CR81			—	√	—	
FF0AH	Remote control timer capture register 90	CP90		R	—	√	—	
FF0BH	Remote control timer capture register 91	CP91			—	√	—	
FF0CH	Serial shift register 1	SIO1		R/W	—	√	—	
FF0DH	Automatic data transmit/receive address pointer	ADTP			—	√	—	Undefined
FF0EH	Serial shift register 3	SIO3			—	√	—	
FF0FH	Port level read register 6	PT6		R	√	√	—	
FF10H	A/D conversion result register 0	ADCR0			—	√	—	
FF20H	Port mode register 0	PM0		R/W	√	√	—	FFH
FF22H	Port mode register 2	PM2			√	√	—	
FF30H	Pull-up resistor option register 0	PU0			√	√	—	00H
FF32H	Pull-up resistor option register 2	PU2			√	√	—	
FF42H	Watchdog timer clock select register	WDCS			—	√	—	
FF48H	External interrupt rising edge enable register	EGP			√	√	—	
FF49H	External interrupt falling edge enable register	EGN			√	√	—	
FF60H	8-bit timer control register 80	TMC80			√	√	—	
FF61H	8-bit timer control register 81	TMC81			√	√	—	
FF62H	Remote control timer control register 9	TMC9			√	√	—	
FF63H	Serial operation mode register 1	CSIM1			√	√	—	
FF64H	Automatic data transmit/receive control register	ADTC			√	√	—	
FF65H	Automatic data transmit/receive interval specification register	ADTI			√	√	—	
FF66H	Serial operation mode register 3	CSIM3			√	√	—	
FF67H	A/D converter mode register 0	ADM0			√	√	—	
FF68H	Analog input channel specification register 0	ADS0			—	√	—	
FF69H	Display mode register 0	DSPM0			√	√	—	10H
FF6AH	Display mode register 1	DSPM1			√	√	—	01H
FF6BH	Display mode register 2	DSPM2			√	√	—	00H
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE4H	Interrupt mask flag register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt mask flag register 0H		MK0H		√	√		
FFE8H	Priority specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority specification flag register 0H		PR0H		√	√		

Table 3-3. Special Function Registers (2/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Units			After Reset
				1 bit	8 bits	16 bits	
FFF0H	Memory size switching register	IMS	R/W	—	√	—	CFH[Note]
FFF9H	Watchdog timer mode register	WDTM		√	√	—	00H
FFFAH	Oscillation stabilization time select register	OSTS		—	√	—	04H
FFFBH	Processor clock control register	PCC		√	√	—	

Note The initial value is CFH, but set and use each microcontroller with the values shown below.

μPD780232: 04H

★ μPD780233: 06H

μPD78F0233: Value corresponding to mask ROM versions

3.3 Instruction Address Addressing

An instruction address is determined by program counter (PC) contents. Program counter (PC) contents are normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to the PC and branched by the following addressing (For details of instructions, refer to **78K/0 Series Instructions User's Manual (U12326E)**.

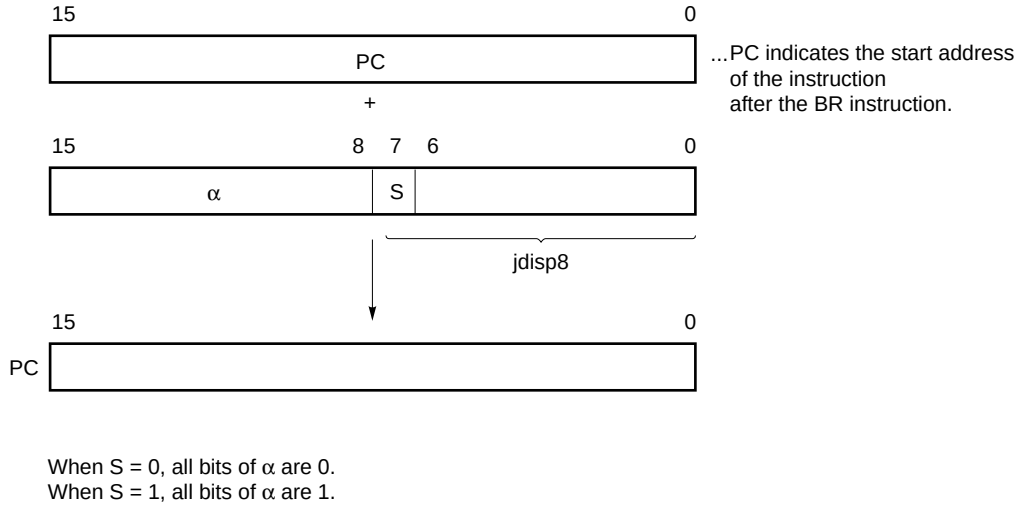
3.3.1 Relative addressing

[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (–128 to +127) and bit 7 becomes a sign bit. In the relative addressing modes, execution branches in a relative range of –128 to +127 from the first address of the next instruction.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

3.3.2 Immediate addressing

[Function]

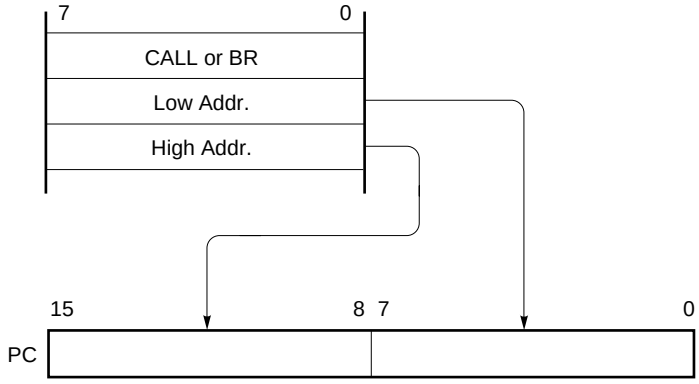
Immediate data in the instruction word is transferred to the program counter (PC) and branched.

This function is carried out when the CALL !addr16 or BR !addr16 or CALLF !addr11 instruction is executed.

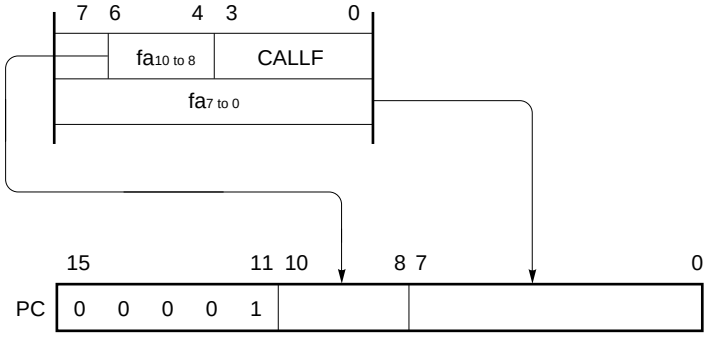
The CALL !addr16 and BR !addr16 instructions can branch in the entire memory space. The CALLF !addr11 instruction branches to an area of addresses 0800H to 0FFFH.

[Illustration]

When the CALL !addr16 or BR !addr16 instruction is executed



When the CALLF !addr11 instruction is executed



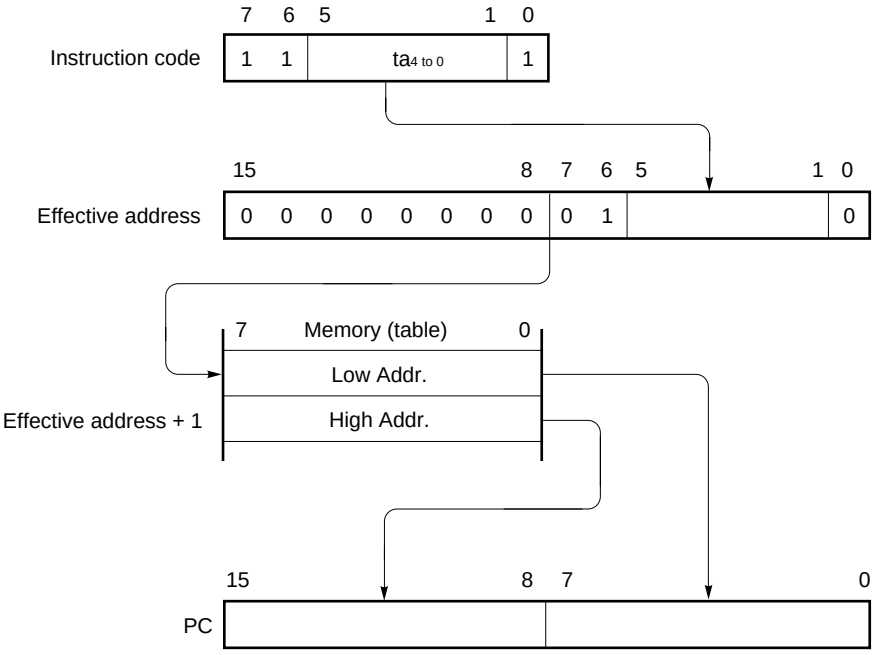
3.3.3 Table indirect addressing

[Function]

Table contents (branch destination address) of the particular location to be addressed by bits 1 to 5 of the immediate data of an operation code are transferred to the program counter (PC) and branched.

Before the CALLT [addr5] instruction is executed, table indirect addressing is performed. This instruction references an address stored in the memory table at addresses 40H to 7FH, and can branch in the entire memory space.

[Illustration]



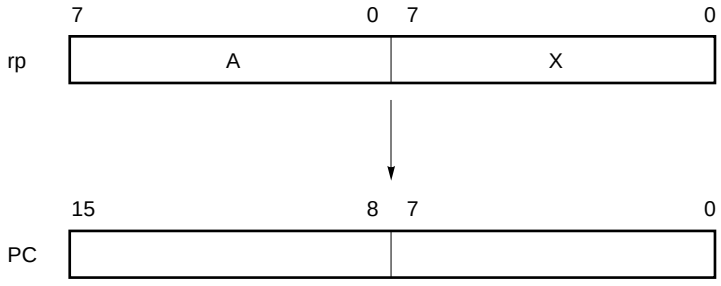
3.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



3.4 Operand Address Addressing

The following various methods are available to specify the register and memory (addressing) which undergo manipulation during instruction execution.

3.4.1 Implied addressing

[Function]

The register which functions as an accumulator (A and AX) in the general-purpose register is automatically (implicitly) addressed.

Of the μPD780232 Subseries instruction words, the following instructions employs implied addressing.

Instruction	Register Specified by Implied Addressing
MULU	A register for multiplicand and AX register for product storage
DIVUW	AX register for dividend and quotient storage
ADJBA/ADJBS	A register for storage of numeric values subject to decimal adjustment
ROR4/ROL4	A register for storage of digit data which undergoes digit rotation

[Operand format]

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

[Example]

In the case of MULU X

With an 8-bit x 8-bit multiply instruction, the product of A register and X register is stored in AX. In this example, the A and AX registers are specified by implied addressing.

3.4.2 Register addressing

[Function]

This addressing accesses a general-purpose register as an operand. The general-purpose register accessed is specified by the register bank select flags (RBS0 and RBS1) and register specification code (Rn or RPn) in an instruction code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

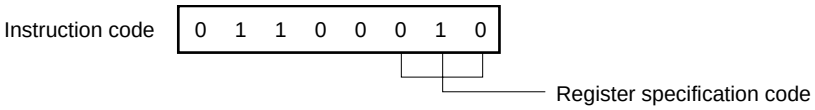
[Operand format]

Identifier	Explanation
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

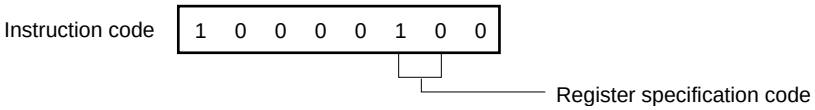
'r' and 'rp' can be written with function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) as well as absolute names (R0 to R7 and RP0 to RP3).

[Example]

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp



3.4.3 Direct addressing

[Function]

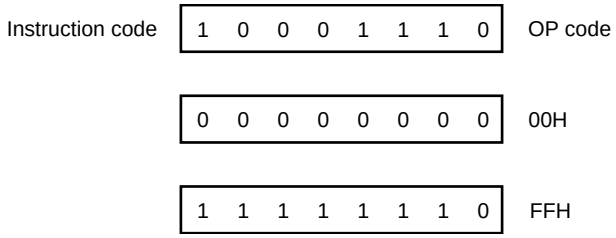
This addressing directly addresses the memory indicated by the immediate data in an instruction word.

[Operand format]

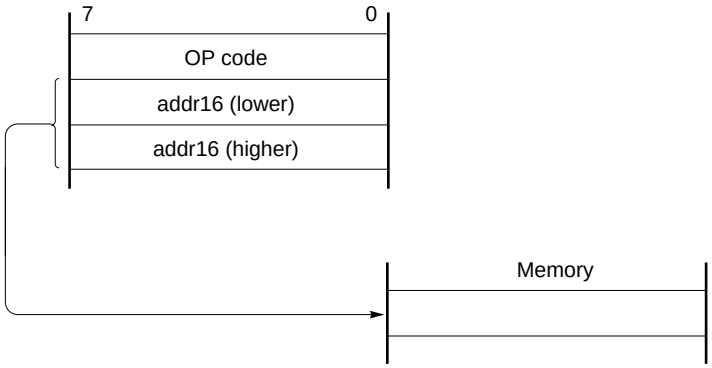
Identifier	Explanation
addr16	Label or 16-bit immediate data

[Example]

MOV A, !0FE00H; when setting !addr16 to FE00H



[Illustration]



3.4.4 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word. The fixed space to which this addressing is applied is the 256-byte space of addresses FE20H to FF1FH. Addresses FE20H to FEFFH constitute a part of the SFR area, and the internal high-speed RAM is mapped to this area. The special function registers (SFRs) are mapped to the area from addresses FF00H to FF1FH. If the SFR area (FF00H to FF1FH) where short direct addressing is applied, ports which are frequently accessed in a program and a compare register of the timer/event counter and a capture register of the timer/event counter are mapped and these SFRs can be manipulated with a small number of bytes and clocks.

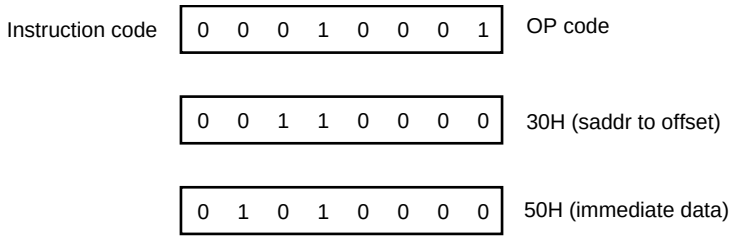
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. Refer to **[Illustration]**.

[Operand format]

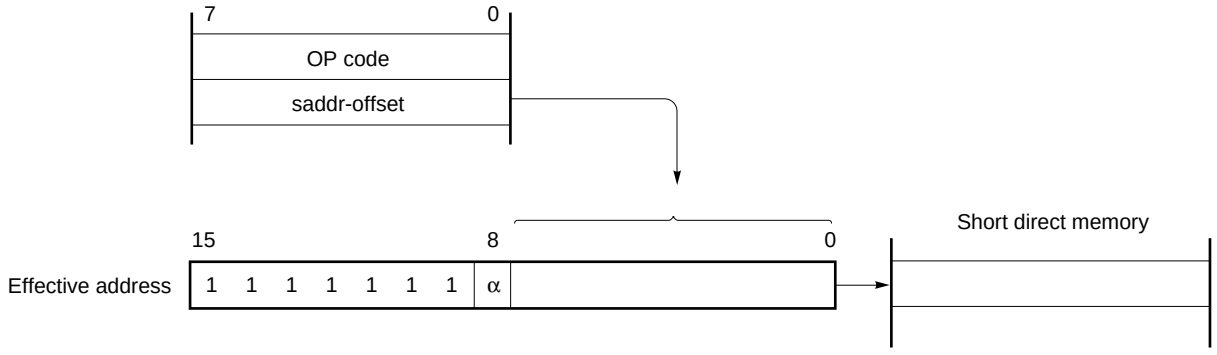
Identifier	Explanation
saddr	Label or FE20H to indicate FF1FH immediate data
saddrp	Label of FE20H to indicate FF1FH immediate data (even address only)

[Example]

MOV 0FE30H, #50H; when setting saddr to FE30H and immediate data to 50H



[Illustration]



When 8-bit immediate data is 20H to FFH, α = 0

When 8-bit immediate data is 00H to 1FH, α = 1

3.4.5 Special function register (SFR) addressing

[Function]

The memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word.

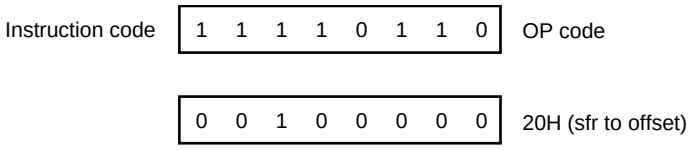
This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, the SFR mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

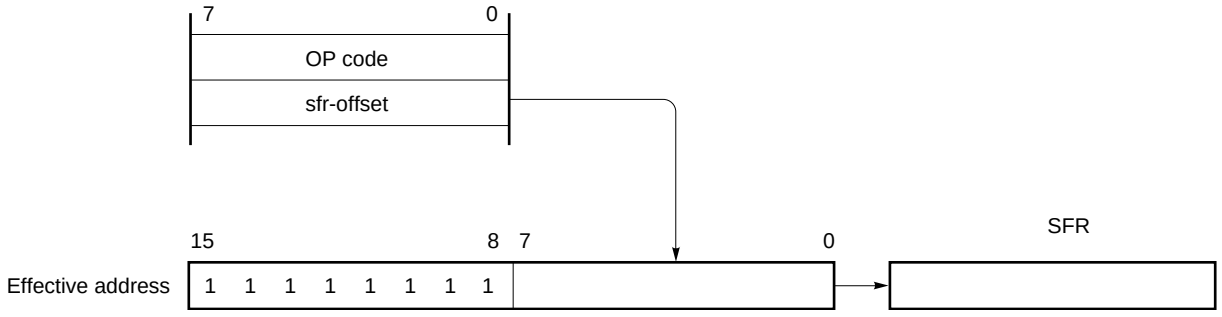
Identifier	Explanation
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

[Example]

MOV PM0, A; when selecting PM0 (FF20H) as sfr



[Illustration]



3.4.6 Register indirect addressing

[Function]

The addressing addresses the memory with the contents of a register pair specified as an operand. The register pair to be accessed is specified by the register bank select flags (RBS0 and RBS1) and register pair specification code in an instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

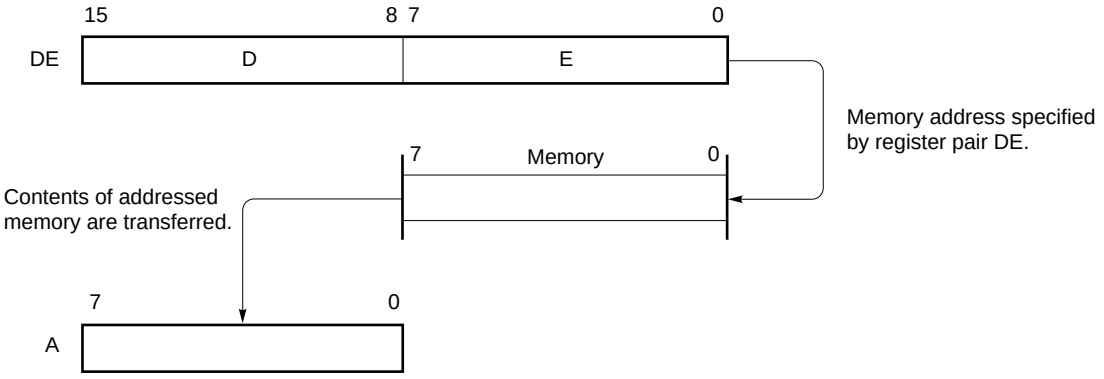
Identifier	Explanation
–	[DE], [HL]

[Example]

MOV A, [DE]; when selecting [DE] as register pair

Instruction code	1	0	0	0	0	1	0	1

[Illustration]



3.4.7 Based addressing

[Function]

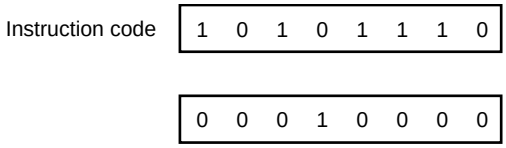
This addressing addresses the memory by adding 8-bit immediate data to the contents of the HL register pair which is used as a base register and by using the result of the addition. The HL register pair to be accessed is in the register bank specified by the register bank select flags (RBS0 and RBS1). Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Explanation
—	[HL+byte]

[Example]

MOV A, [HL+10H]; When setting byte to 10H



3.4.8 Based indexed addressing

[Function]

This addressing addresses the memory by adding the contents of the HL register pair, which is used as a base register, to the contents of the B or C register specified in the instruction word, and by using the result of the addition. The HL, B, and C registers to be accessed are registers in the register bank specified by the register bank select flags (RBS0 and RBS1). The addition is performed by extending the contents of the B or C register to 16 bits as a positive number. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Explanation
—	[HL+B], [HL+C]

[Example]

In the case of MOV A, [HL+B] (selects the B register)

Instruction code	1	0	1	0	1	0	1	1

3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and RETURN instructions are executed or the register is saved/reset upon generation of an interrupt request.

Stack addressing enables to address the internal high-speed RAM area only.

[Example]

In the case of PUSH DE (saves the DE register)

Instruction code	1	0	1	1	0	1	0	1

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

The μPD780232 Subseries incorporates 16 output ports and 24 I/O ports. Figure 4-1 shows the port configuration. Every port is capable of 1-bit and 8-bit manipulations and can carry out considerably varied control operations. Besides port functions, the ports can also serve as on-chip hardware I/O pins.

Figure 4-1. Port Types

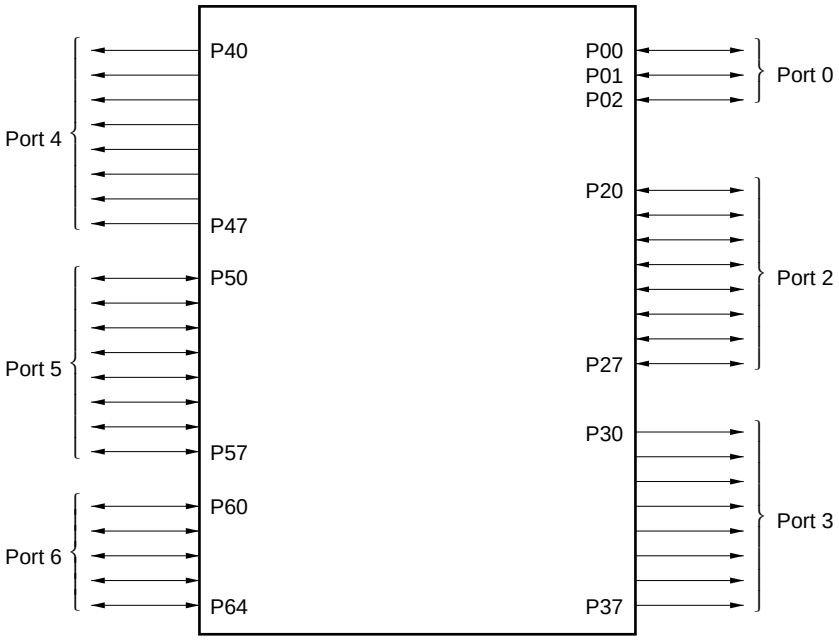


Table 4-1. Port Function

Pin Name	Function	Alternate Function
P00	Port 0 3-bit I/O port Input/output mode can be specified in 1-bit units. An on-chip pull-up resistor can be used by software settings when this port is used as input port.	INTP0
P01		INTP1
P02		TI
P20	Port 2 8-bit I/O port Input/output mode can be specified in 1-bit units. An on-chip pull-up resistor can be used by software settings when this port is used as input port.	$\overline{\text{SCK3}}$
P21		SO3
P22		—
P23		—
P24		BUSY
P25		SO1
P26		SI1
P27		$\overline{\text{SCK1}}$
P30 to P37	Port 3 P-ch open-drain 8-bit high-withstanding-voltage output port Pull-down resistor to V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-up resistors, however.	FIP24 to FIP31
P40 to P47	Port 4 P-ch open-drain 8-bit high-withstanding-voltage output port Pull-down resistor to V_{LOAD} can be used by mask option in 1-bit units (mask ROM models only). μPD78F0233 does not have pull-down resistors, however.	FIP32 to FIP39
P50 to P57	Port 5 P-ch open-drain 8-bit high-withstanding-voltage I/O port Input/output mode can be specified in 1-bit units. Pull-down resistor can be used by mask option in 1-bit units (mask ROM models only) (Connection to V_{LOAD} or V_{SS0} specifiable in 1-bit units). μPD78F0233 does not have pull-down resistors, however.	FIP40 to FIP47
P60 to P64	Port 6 P-ch open-drain 5-bit high-withstanding-voltage I/O port Input/output mode can be specified in 1-bit units. Pull-down resistor can be used by mask option in 1-bit units (mask ROM models only) (Connection to V_{LOAD} or V_{SS0} specifiable in 1-bit units). μPD78F0233 does not have pull-down resistors, however.	FIP48 to FIP52

4.2 Port Configuration

A port includes the following hardware.

Table 4-2. Port Configuration

Item	Configuration
Control register	Port mode register (PMn: n = 0, 2) Pull-up resistor option register (PUn: n = 0, 2) Output latch (Pm: m = 0, 2, 5, 6)
Port	Total: 40 (16 outputs, 24 inputs/outputs)
Pull-up resistor	Total: 11 (software control)
Pull-down resistor	• Mask ROM model Total: 29 (mask option specification: 29) • μPD78F0233 None

4.2.1 Port 0

Port 0 is a 3-bit I/O port with output latch. P00 to P02 pins can specify the input or output mode in 1-bit units using ★ port mode register 0 (PM0). P00 to P02 pins can be connected to an on-chip pull-up resistor in 1-bit units using pull-up resistor option register 0 (PU0).

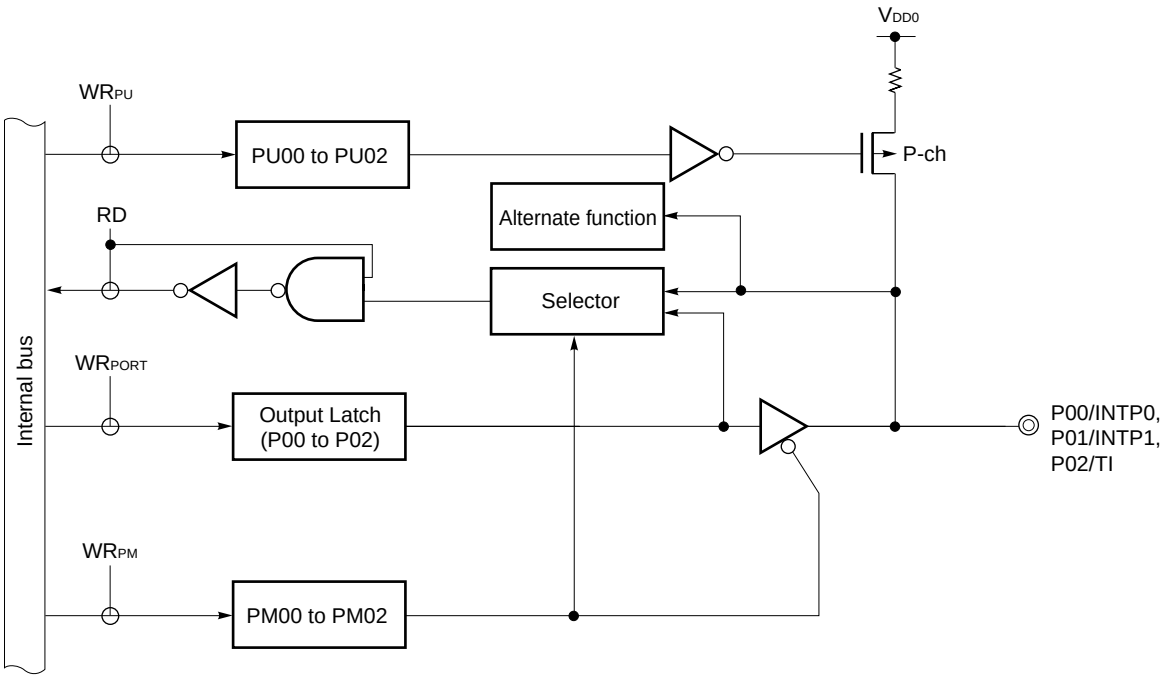
Alternate functions include external interrupt request input and timer input.

$\overline{\text{RESET}}$ input sets port 0 to input mode.

Figure 4-2 shows a block diagram of port 0.

Caution Because P00 and P01 pins also serve for external interrupt request input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. Thus, when the output mode is used, set the interrupt mask flag to 1.

★ **Figure 4-2. Block Diagram of P00 to P02**



PU: Pull-up resistor option register
PM: Port mode register
RD: Port 0 read signal
WR: Port 0 write signal

4.2.2 Port 2

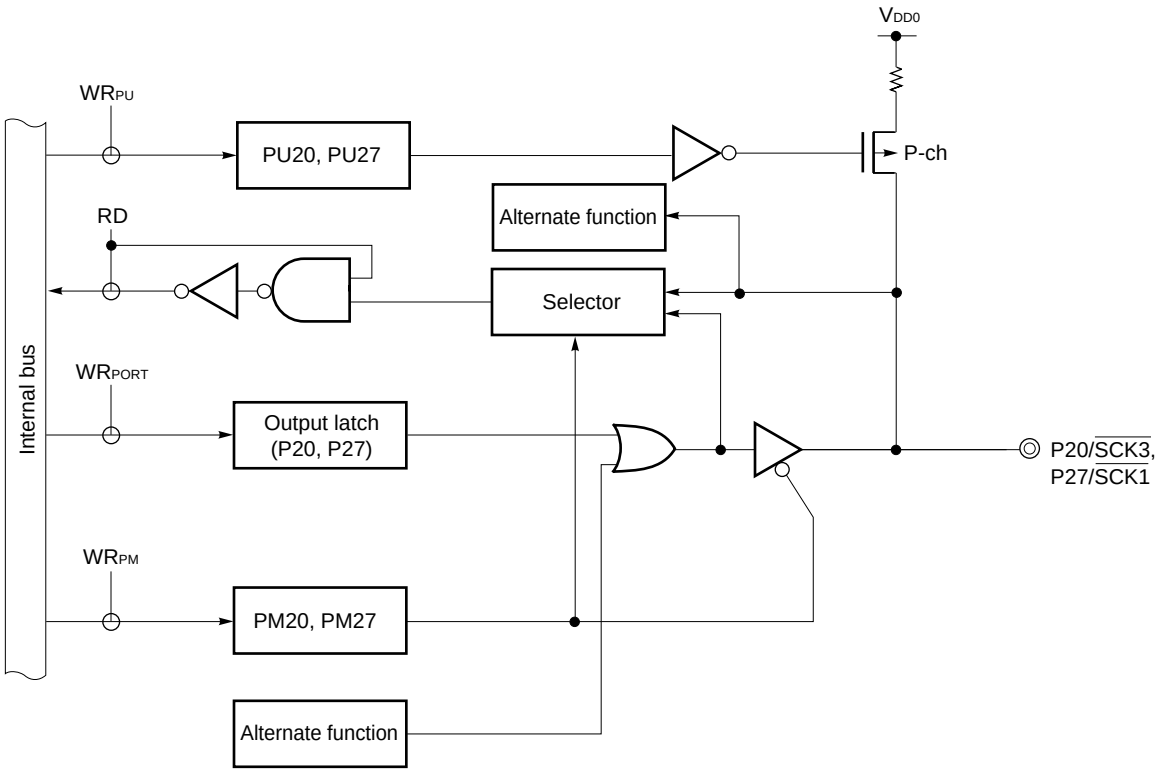
Port 2 is an 8-bit I/O port with output latch. P20 to P27 pins can specify the input or output mode in 1-bit units using ★ the port mode register 2 (PM2). P20 to P27 pins can be connected to an on-chip pull-up resistor in 1-bit units using pull-up resistor option register 2 (PU2).

Alternate functions include serial interface data I/O, clock I/O, and automatic transmit/receive busy input.

$\overline{\text{RESET}}$ input sets port 2 to input mode.

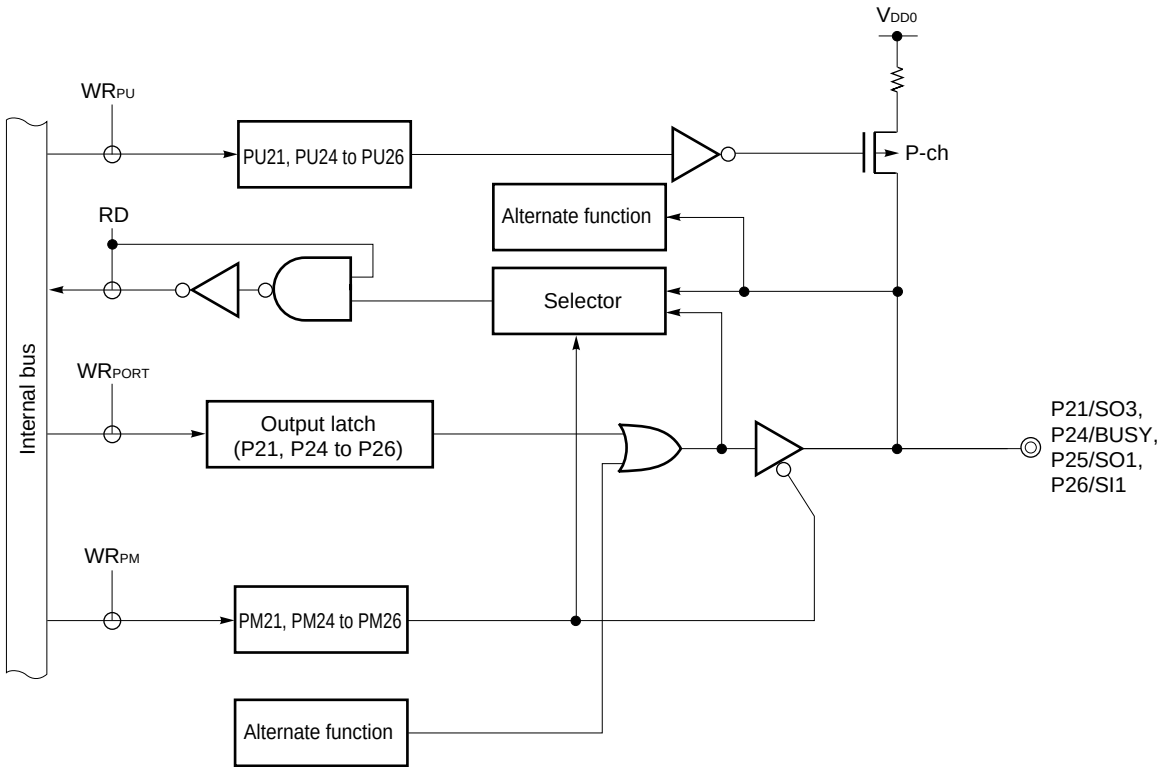
Figures 4-3 to 4-5 show block diagrams of port 2.

★ **Figure 4-3. Block Diagram of P20 and P27**



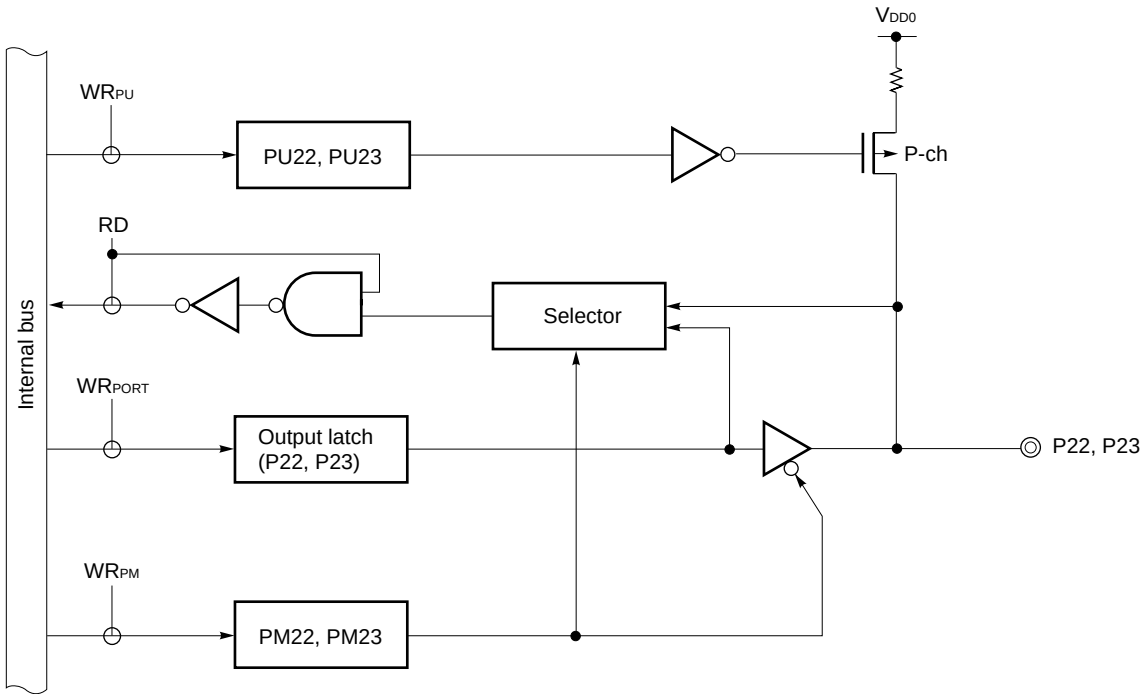
PU: Pull-up resistor option register
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

★ **Figure 4-4. Block Diagram of P21, P24 to P26**



PU: Pull-up resistor option register
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

★ **Figure 4-5. Block Diagram of P22 and P23**



PU: Pull-up resistor option register
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

4.2.3 Port 3

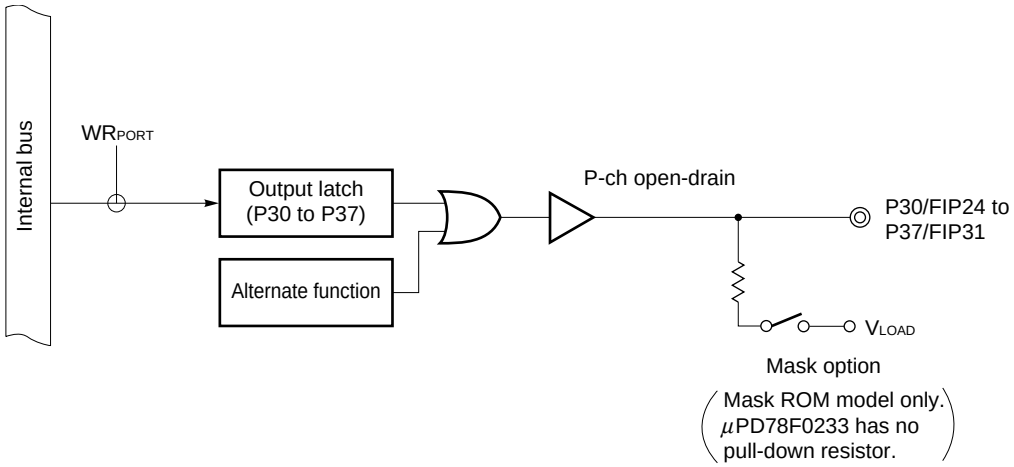
Port 3 is an 8-bit output only port. On-chip pull-down resistors can be connected in 1-bit units with the mask option in case of mask ROM model. The μPD78F0233 has no pull-down resistor.

In addition, VFD controller/driver segment/digit output is provided as an alternate function.

Figure 4-6 shows a block diagram of port 3.

★ **Caution Adjust the number of pull-down resistors so that the total dissipation is not exceeded. (Refer to 12.7 Calculation of Total Power Dissipation.)**

Figure 4-6. Block Diagram of P30 to P37



WR: Port 3 write signal

4.2.4 Port 4

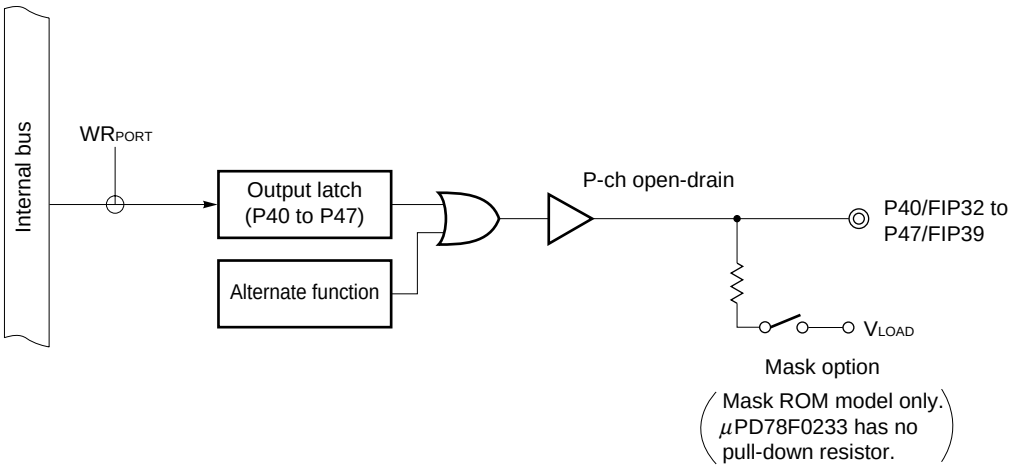
Port 4 is an 8-bit output only port. On-chip pull-down resistors can be connected in 1-bit units with the mask option in case of mask ROM model. The μPD78F0233 has no pull-down resistor.

In addition, VFD controller/driver segment/digit output is provided as an alternate function.

Figure 4-7 shows a block diagram of port 4.

★ **Caution Adjust the number of pull-down resistors so that the total dissipation is not exceeded. (Refer to 12.7 Calculation of Total Power Dissipation.)**

Figure 4-7. Block Diagram of P40 to P47



WR: Port 4 write signal

4.2.5 Port 5

Port 5 is an 8-bit I/O port with output latch. When using this port as an output port, the value assigned to the output latch (P50 to P57) is output. When it is used as an input port, set the output latch (P50 to P57) to "0", and read the port level read (PT50 to PT57). On-chip pull-down resistors can be connected in 1-bit units with the mask option. Pull-down resistor to V_{LOAD} or V_{SS0} can be selected in 1-bit units. The μPD78F0233 has no pull-down resistor.

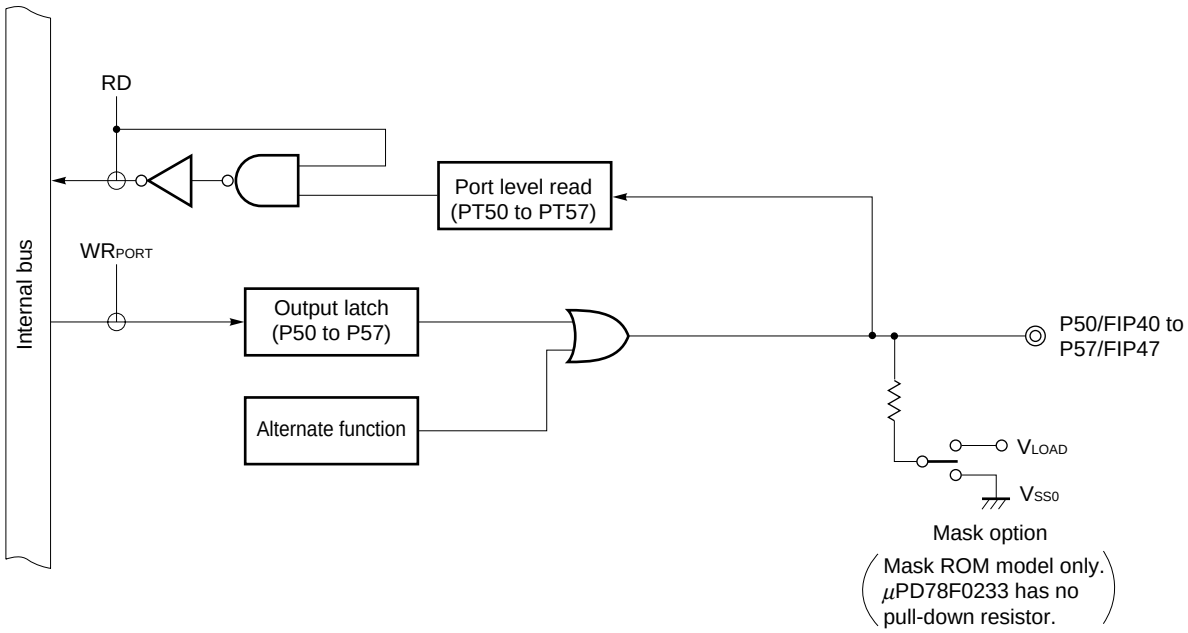
In addition, VFD controller/driver output is provided as an alternate function.

$\overline{\text{RESET}}$ input sets port 5 to input mode.

Figure 4-8 shows a block diagram of port 5.

★ **Caution Adjust the number of pull-down resistors so that the total dissipation is not exceeded. (Refer to 12.7 Calculation of Total Power Dissipation.)**

Figure 4-8. Block Diagram of P50 to P57



RD: Port 5 read signal

WR: Port 5 write signal

4.2.6 Port 6

Port 6 is a 5-bit I/O port with output latch. When using this port as an output port, the value assigned to the output latch (P60 to P64) is output. When it is used as an input port, set the output latch (P60 to P64) to "0", and read the port level read (PT60 to PT64). On-chip pull-down resistors can be connected in 1-bit units with the mask option. Pull-down resistor to V_{LOAD} or V_{SS0} can be selected in 1-bit units. The μPD78F0233 has no pull-down resistor.

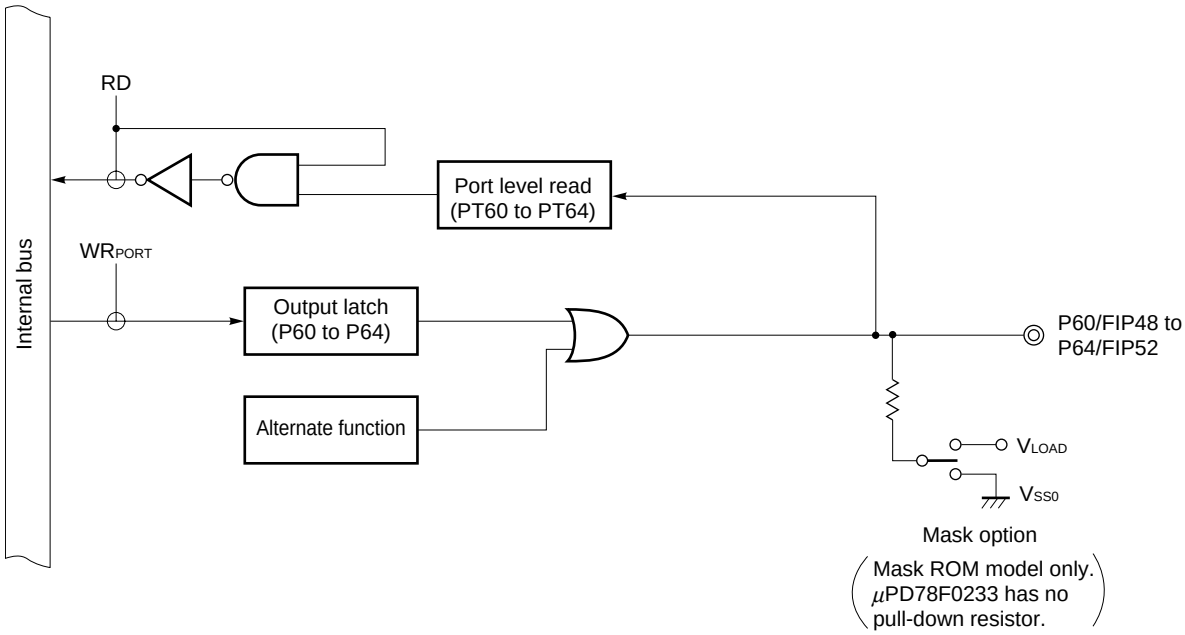
In addition, VFD controller/driver output is provided as an alternate function.

$\overline{\text{RESET}}$ input sets port 6 to input mode.

Figure 4-9 shows a block diagram of port 6.

★ **Caution Adjust the number of pull-down resistors so that the total dissipation is not exceeded. (Refer to 12.7 Calculation of Total Power Dissipation.)**

Figure 4-9. Block Diagram of P60 to P64



RD: Port 6 read signal

WR: Port 6 write signal

4.3 Port Function Control Registers

The following two types of registers control the ports.

- Port mode registers (PM0, PM2)
- Pull-up resistor option register (PU0, PU2)

(1) Port mode registers (PM0, PM2)

These registers are used to set port I/O in 1-bit units.

PM0 and PM2 are independently set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

When a port pin is used as its alternate function pin, set the port mode register and the output latch according to Table 4-3.

Cautions 1. Pins P30 to P37 and P40 to P47 are output-only pins.

2. As port 0 has an alternate function as external interrupt request input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

Table 4-3. Port Mode Register and Output Latch Setting When Alternate Function Is Used

Pin Name	Alternate Function		PMxx	Pxx
	Function Name	I/O		
P00	INTP0	Input	1	×
P01	INTP1	Input	1	×
P02	TI	Input	1	×

3. When using port 2 as the serial interface pin, setting of the I/O and output latch is necessary depending on the function used. For details of the setting, refer to 10.3 (1) Serial operation mode register 1 (CSIM1) and 11.3 (1) Serial operation mode register 3 (CSIM3).

Remark ×: Don't care
PMxx: Port mode register
Pxx: Port output latch

Figure 4-10. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	1	PM02	PM01	PM00	FF20H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PMmn	Pmn pin I/O mode slection (m = 0: n = 0 to 2) (m = 2: n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(2) Pull-up resistor option registers (PU0, PU2)

★ This register is used to set whether or not to use an internal pull-up resistor of pins at ports 0 and 2. By setting PU0 and PU2, on-chip pull-up resistors corresponding to bits in PU0 and PU2 can be used.

PU0 and PU2 are set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears these registers to 00H.

★ **Caution When PUmn is set to 1, an on-chip pull-up resistor is connected regardless of whether the current mode is input or output. Accordingly, when using the port in output mode, set the corresponding bit of PUmn to 0 (m = 0: n = 0 to 2, m = 2: n = 0 to 7).**

Figure 4-11. Format of Pull-Up Resistor Option Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	0	0	0	0	PU02	PU01	PU00	F F 3 0 H	0 0 H	R/W
PU2	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	F F 3 2 H	0 0 H	R/W

PUmn	Pmn internal pull-up resistor selection (m = 0: n = 0 to 2) (m = 2: n = 0 to 7)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

4.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

4.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.

Once data is written to the output latch, it is retained until data is written to the output latch again.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.

Once data is written to the output latch, it is retained until data is written to the output latch again.

Cautions 1. Ports 3 and 4 are output-only ports.

2. When using ports 5 and 6 as input ports, set output latch to 0.

4.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction in ports 0 and 2. The output latch contents do not change.

It is possible to read the pin status of ports 5 and 6 by reading the port level read (PT5, PT6).

Cautions 1. Ports 3 and 4 are output-only ports.

2. When using ports 5 and 6 as input ports, set output latch to 0.

4.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.

Once data is written to the output latch, it is retained until data is written to the output latch again.

(2) Input mode

The output latch contents are undefined, but since the output buffer is off, the pin status does not change.

Cautions 1. Ports 3 and 4 are output-only ports.

2. When using ports 5 and 6 as input ports, set output latch to 0.

3. In the case of 1-bit memory manipulation instruction, although a single bit is manipulated the port is accessed as an 8-bit unit. Therefore, on a port with a mixture of input and output pins, the output latch contents for pins specified as input are undefined except for the manipulated bit.

4.5 Selecting Mask Option

The mask ROM models have the following mask options. The μPD78F0233 does not have mask options.

★ **Table 4-4. Comparison Between Mask Options of Mask ROM Models and μPD78F0233**

Pin Name	Mask Option of Mask ROM Model	μPD78F0233
FIP0 to FIP23	Pull-down resistor to V_{LOAD} can be connected in 1-bit units.	Pull-down resistor is provided.
P30/FIP24 to P37/FIP31, P40/FIP32 to P47/FIP39	Pull-down resistor to V_{LOAD} can be connected in 1-bit units.	Pull-down resistor is not provided.
P50/FIP40 to P57/FIP47, P60/FIP48 to P64/FIP52	Pull-down resistor can be connected in 1-bit units. Connection to V_{LOAD} or V_{SS0} can be selected.	Pull-down resistor is not provided.

CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates clock to be supplied to the CPU and peripheral hardware. The following type of system clock oscillators is available.

- **Main system clock oscillator**
  This circuit oscillates at frequencies of 5.0 MHz. Oscillation can be stopped by executing the STOP instruction.

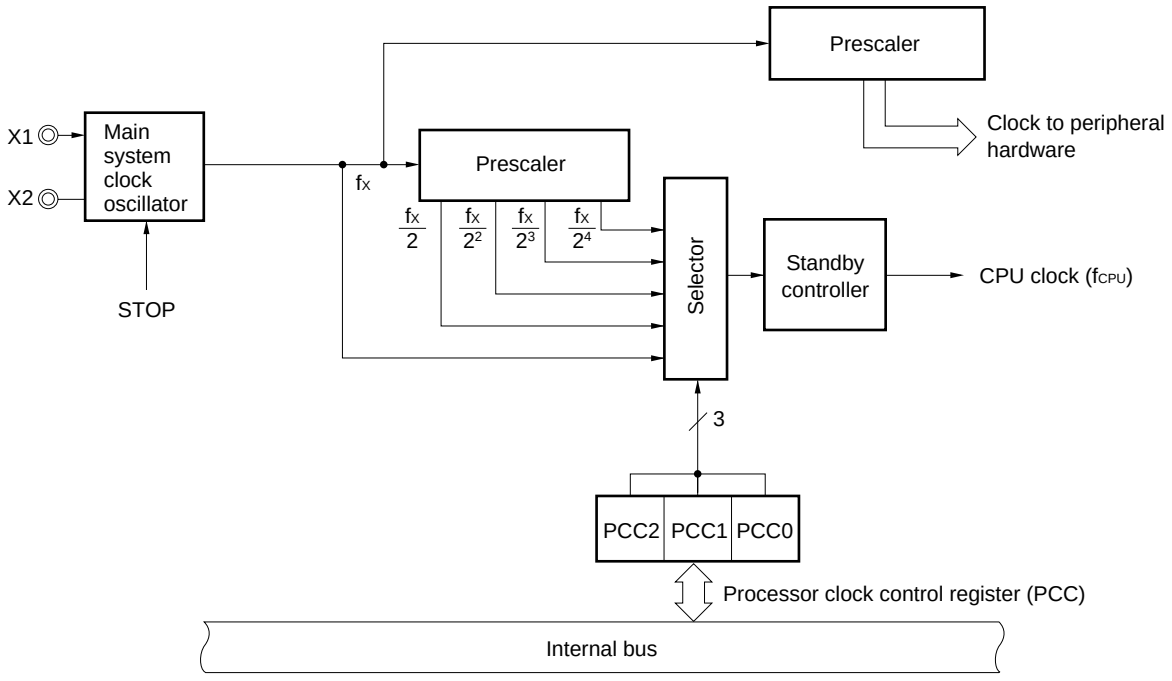
5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control register	Processor clock control register (PCC)
Oscillator	Main system clock oscillator

★ **Figure 5-1. Block Diagram of Clock Generator**



5.3 Register Controlling Clock Generator

The clock generator is controlled by the processor clock control register (PCC).

- **Processor clock control register (PCC)**
  This register selects a CPU clock and selects a division ratio.
  PCC is set by a 1-bit or 8-bit memory manipulation instruction.
  $\overline{\text{RESET}}$ sets PCC to 04H.

Figure 5-2. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	0	0	0	0	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W

PCC2	PCC1	PCC0	Selection of CPU clock (f_{CPU})
0	0	0	f_X
0	0	1	$f_X/2$
0	1	0	$f_X/2^2$
0	1	1	$f_X/2^3$
1	0	0	$f_X/2^4$
Other			Setting prohibited

Caution Be sure to clear bits 3 to 7 to “0”.

Remark f_X: Oscillation frequency of main system clock

The shortest instruction of the μPD780232 Subseries is executed in two CPU clocks. Therefore, the relation between the CPU clock (f_{CPU}) and minimum instruction execution time is as shown in Table 5-2.

Table 5-2. Relation Between CPU Clock and Minimum Instruction Execution Time

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$
f_X	0.4 μs
$f_X/2$	0.8 μs
$f_X/2^2$	1.6 μs
$f_X/2^3$	3.2 μs
$f_X/2^4$	6.4 μs

f_X = 5.0 MHz

f_X: Main system clock oscillation frequency

5.4 System Clock Oscillator

5.4.1 Main system clock oscillator

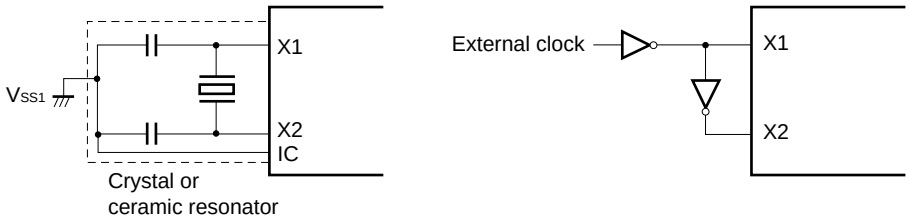
The main system clock oscillator oscillates with a crystal or ceramic resonator (5.0 MHz TYP.) connected to the X1 and X2 pins.

External clocks can be input to the main system clock oscillator. In this case, input a clock signal to the X1 pin and an antiphase clock signal to the X2 pin.

Figure 5-3 shows an external circuit of the main system clock oscillator.

Figure 5-3. External Circuit of Main System Clock Oscillator

(a) Crystal or ceramic oscillation **(b) External clock**



Cautions 1. The STOP mode cannot be set when the external clock is input. This is because the X2 pin is pulled up by V_{DD1}.

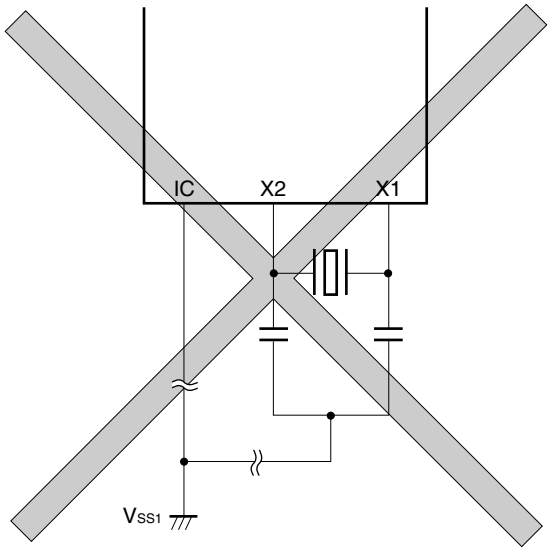
2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

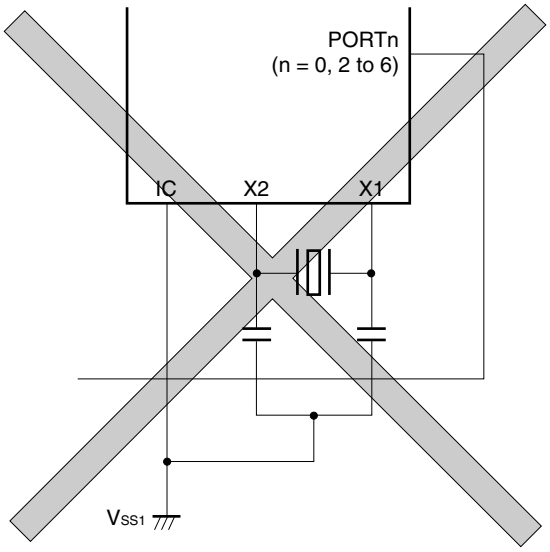
Figure 5-4 shows examples of incorrect resonator connection.

Figure 5-4. Examples of Incorrect Resonator Connection (1/2)

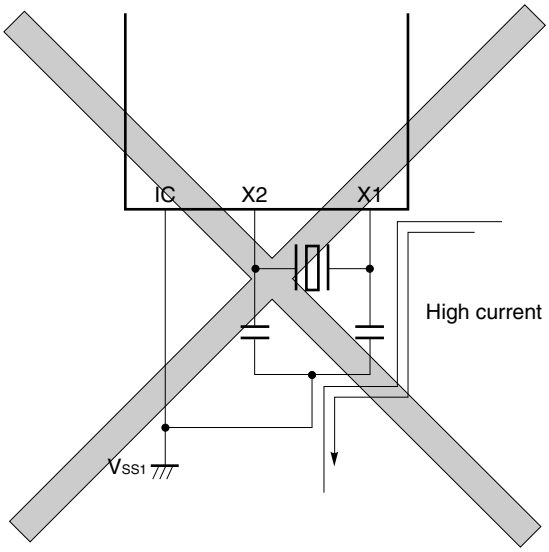
(a) Too long wiring



(b) Crossed signal line



(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)

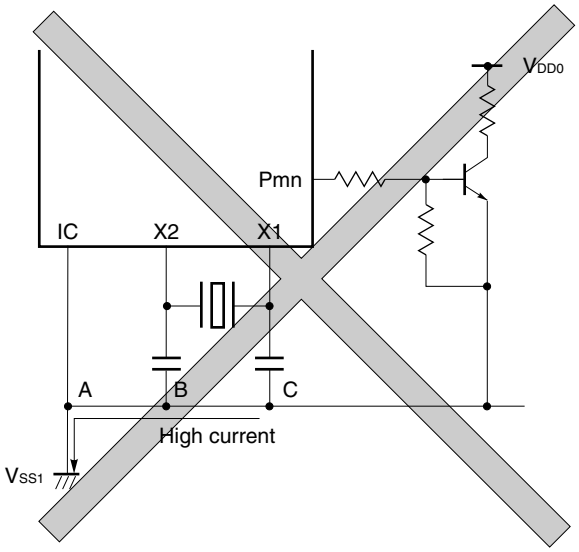
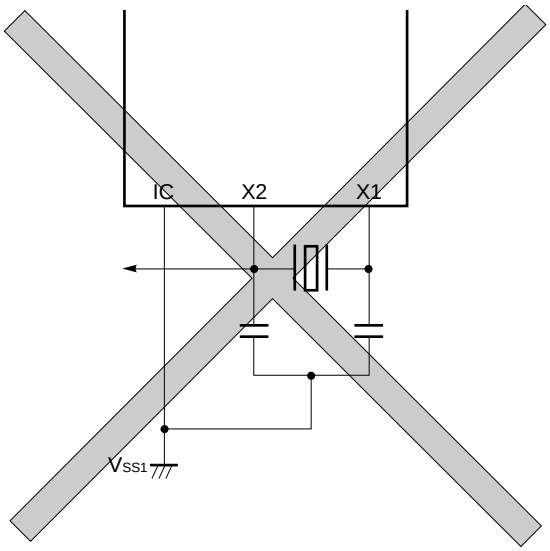


Figure 5-4. Examples of Incorrect Resonator Connection (2/2)

(e) Signals are fetched



5.5 Operations of Clock Generator

The clock generator generates the following various types of clocks and controls the CPU operating mode including the standby mode.

- Main system clock f_X
- CPU clock f_{CPU}
- Clock to peripheral hardware

The function and operation of the clock generator are determined by the processor clock control register (PCC) as follows.

(a) Upon generation of $\overline{\text{RESET}}$ signal, the lowest speed mode of the main system clock (6.4 μs when operated at 5.0 MHz) is selected (PCC = 04H). Main system clock oscillation stops while low level is applied to $\overline{\text{RESET}}$ pin.

(b) Five types of minimum instruction execution time (0.4 μs, 0.8 μs, 1.6 μs, 3.2 μs, and 6.4 μs: when operated at 5.0 MHz) can be selected by the PCC setting.

(c) Two standby modes, STOP and HALT, are available.

(d) The main system clock is divided and supplied to the peripheral hardware. Therefore, the peripheral hardware also stops if the main system clock is stopped. (Except external input clock operation)

5.6 Changing CPU Clock

5.6.1 Time required to change CPU clock

The CPU clock can be changed by using bits 0 to 2 (PCC0 to PCC2) of the processor clock control register (PCC).

Actually, the clock is not changed immediately after PCC has been rewritten, and the CPU operates with the old clock until the specified number of instructions (refer to **Table 5-3**) has been executed after PCC was changed.

Table 5-3. Maximum Time Required for Changing CPU Clock

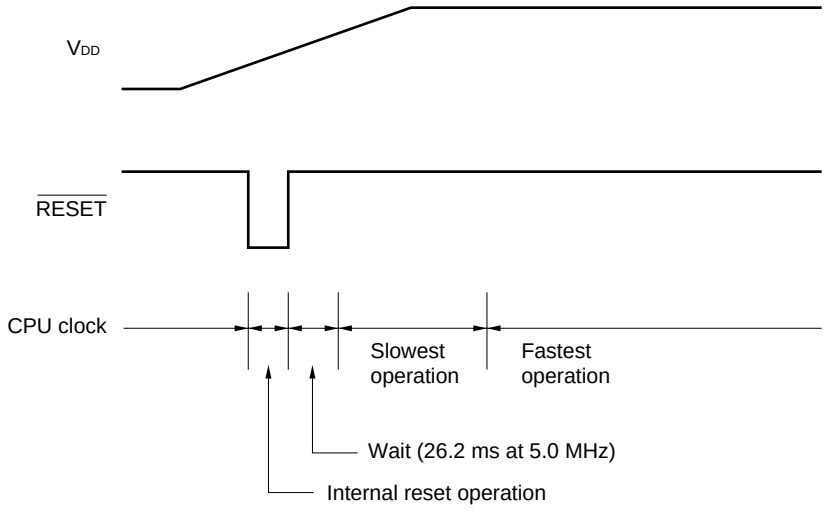
Set Value before Change			Set Value After Change														
PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0
			0	0	0	0	0	1	0	1	0	0	1	1	1	0	0
0	0	0				16 instructions			16 instructions			16 instructions			16 instructions		
0	0	1	8 instructions						8 instructions			8 instructions			8 instructions		
0	1	0	4 instructions			4 instructions						4 instructions			4 instructions		
0	1	1	2 instructions			2 instructions			2 instructions						2 instructions		
1	0	0	1 instruction			1 instruction			1 instruction			1 instruction					

Remark The time required to execute one instruction is equal to the minimum instruction execution time with the CPU clock before change.

5.6.2 CPU clock changing procedure

The CPU clock is changed in the following procedure.

Figure 5-5. Changing CPU Clock



(1) The CPU is reset if the $\overline{\text{RESET}}$ pin is made low after power application. The reset is cleared and the main system clock starts oscillating if the $\overline{\text{RESET}}$ pin is later made high. At this time, it is automatically ensured that oscillation stabilization time ($2^{17}/f_X$) elapses.
After that, the CPU starts executing instructions at the slowest speed of the main system clock (6.4 μs at 5.0 MHz).

(2) After sufficient time has elapsed during which the V_{DD} voltage rises to the level at which the CPU can operate at the highest speed, the contents of the processor clock control register (PCC) are rewritten, and the CPU operates at the highest speed.

CHAPTER 6 8-BIT REMOTE CONTROL TIMER 9

6.1 Function of 8-Bit Remote Control Timer 9

The 8-bit remote control timer has a pulse width measurement function with a resolution of 8 bits.

Pulse width is measured from a difference in count value when the valid edge has been detected while the timer operates in the free-running mode.

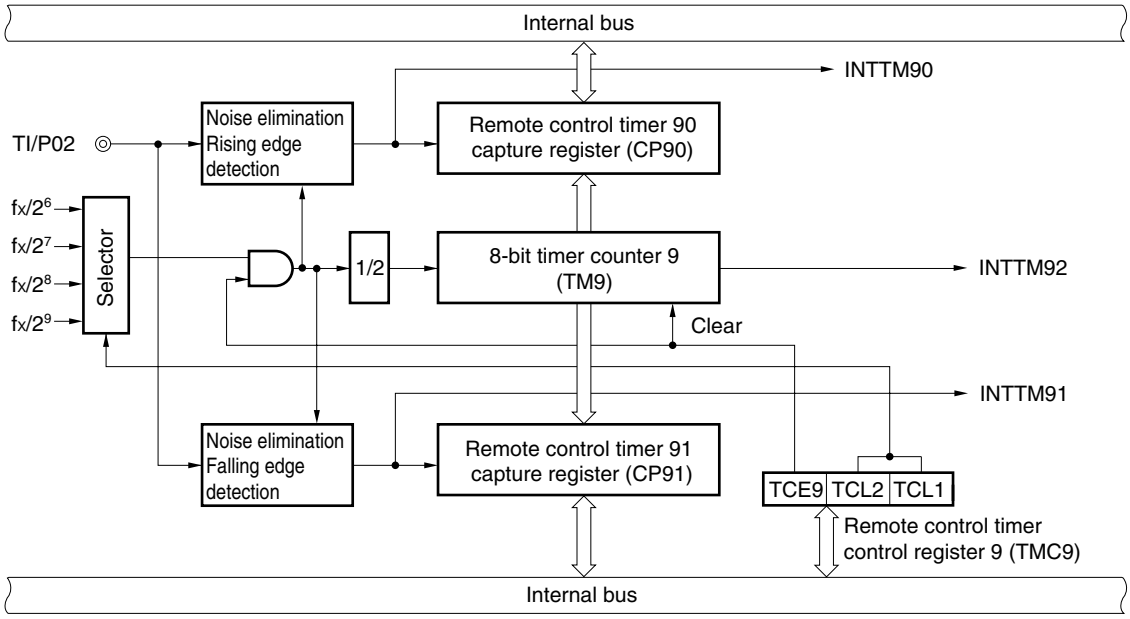
★ 6.2 Configuration of 8-Bit Remote Control Timer 9

8-bit remote control timer 9 includes the following hardware.

Table 6-1. Configuration of 8-Bit Remote Control Timer 9

Item	Configuration
Timer/counter	8-bit timer counter 9 (TM9)
Register	Remote control timer capture register: 2 (CP90 and CP91)
Control register	Remote control timer control register 9 (TMC9)

Figure 6-1. Block Diagram of 8-Bit Remote Control Timer 9



(1) 8-bit timer counter 9 (TM9)

This 8-bit register counts the count pulse.

The value of this register is initialized to 00H by $\overline{\text{RESET}}$ input or by clearing the TCE9 bit.

(2) Remote control timer capture registers 90, 91 (CP90 and CP91)

These 8-bit registers capture the contents of the 8-bit timer counter 9 (TM9).

The capture operation is performed in synchronization with the valid edge input to the TI pin (capture trigger).

The contents of CP90 are retained until the next rising edge of the TI pin is detected. The contents of CP91 are retained until the next falling edge of the TI pin is detected.

CP90 and CP91 can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears these registers to 00H.

★ 6.3 Registers Controlling 8-Bit Remote Control Timer 9

8-bit remote control timer 9 is controlled by 8-bit remote control register 9 (TMC9).

(1) Remote control timer control register 9 (TMC9)

This register enables or disables the operation of 8-bit timer counter 9 (TM9), and sets the count clock.

TMC9 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC9 to 00H.

Figure 6-2. Format of Remote Control Timer Control Register 9

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
TMC9	TCE9	0	0	0	0	0	TCL2	TCL1	FF62H	00H	R/W

TCE9	Controls count operation of TM9
0	Clears counter to 0 and stops operation
1	Starts count operation

TCL2	TCL1	Selects count clock
0	0	$f_X/2^{10}$ (4.9 kHz)
0	1	$f_X/2^9$ (9.8 kHz)
1	0	$f_X/2^8$ (19.5 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

Caution Be sure to clear bits 2 to 6 to "0".

Remarks 1. fx: Main system clock oscillation frequency

2. ( ): fx = 5.0 MHz

6.4 Operation of 8-Bit Remote Control Timer 9

8-bit remote control timer 9 operates as a pulse width measuring circuit.

The width of a high-level or low-level external pulse input to the TI pin is measured by operating 8-bit timer counter 9 (TM9) in the free-running mode.

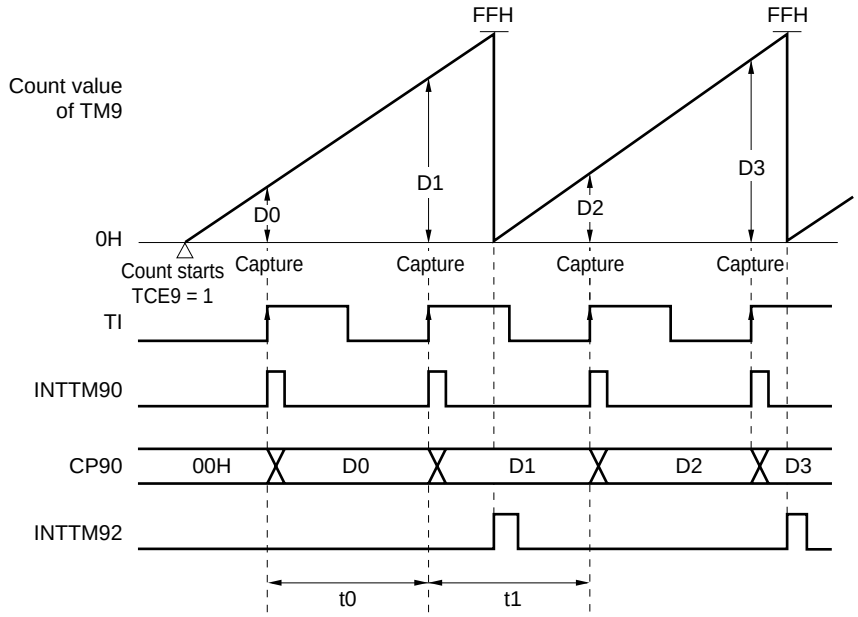
Detection of the valid edge is sampled every 2 cycles of the count clock selected by TCL1 and TCL2, and the capture operation is not performed until the valid level has been detected two times. Therefore, the pulse width input to the TI pin must be 5 or more of the count clock set by TCL1 and TCL2, regardless of whether the level is high or low. If the pulse width is less than 5 clocks, it cannot be detected, and the capture operation is not performed.

The value of 8-bit timer counter 9 (TM9) is loaded to and retained in the capture registers (CP90 and CP91) in synchronization with the valid edge of the pulse input to the TI pin, as shown in Figure 6-3.

Figure 6-3 shows the timing of pulse width measurement.

Figure 6-3. Timing of Pulse Width Measurement (1/2)

(1) To measure pulse width in synchronization with rising edge



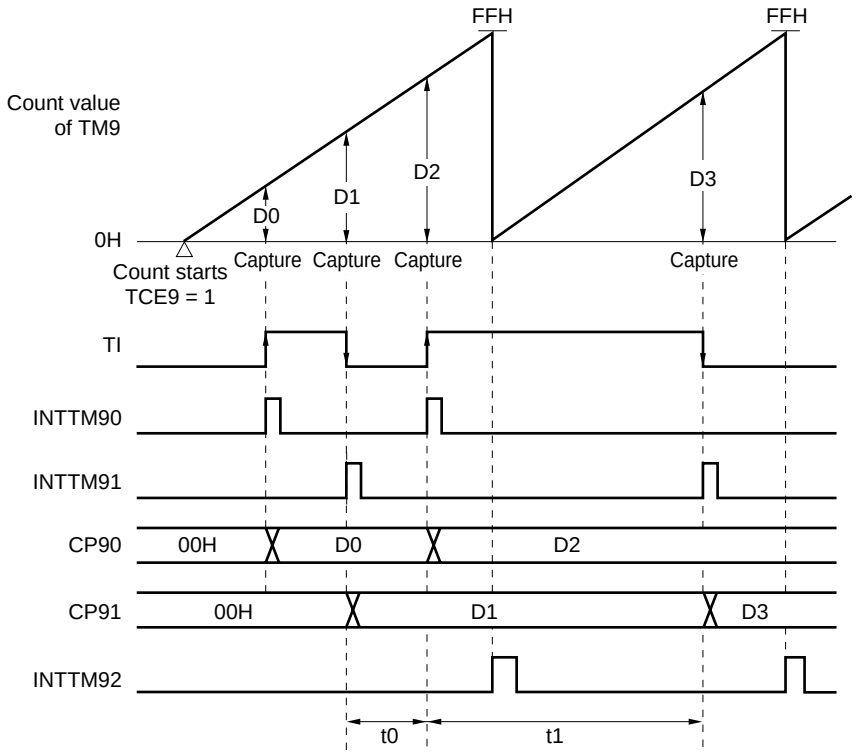
Remark $t0 = (D1 - D0) \times 1/f_{COUNT}$

$t1 = (100H - D1 + D2) \times 1/f_{COUNT}$

f_{COUNT}: Count clock frequency set by TCL1 and TCL2

Figure 6-3. Timing of Pulse Width Measurement (2/2)

(2) Measure pulse width in synchronization with both rising and falling edges



Remark $t0 = (D1 - D0) \times 1/f_{COUNT}$

$t1 = (100H - D2 + D3) \times 1/f_{COUNT}$

f_{COUNT}: Count clock frequency set by TCL1 and TCL2

CHAPTER 7 8-BIT TIMERS 80, 81

7.1 Function of 8-Bit Timers 80, 81

8-bit timers 80 and 81 have an interval timer function. The interval timer repeatedly generates interrupt requests at intervals specified by the preset count value.

7.2 Configuration of 8-Bit Timers 80, 81

8-bit timers 80 and 81 includes the following hardware.

Table 7-1. Configuration of 8-Bit Timers 80, 81

Item	Configuration
Timer/counter	8-bit timer counter 8n (TM80, TM81)
Register	8-bit compare register 8n (CR80, CR81)
Control register	8-bit timer control register 8n (TMC80, TMC81)

n = 0, 1

Figure 7-1. Block Diagram of 8-Bit Timer 80

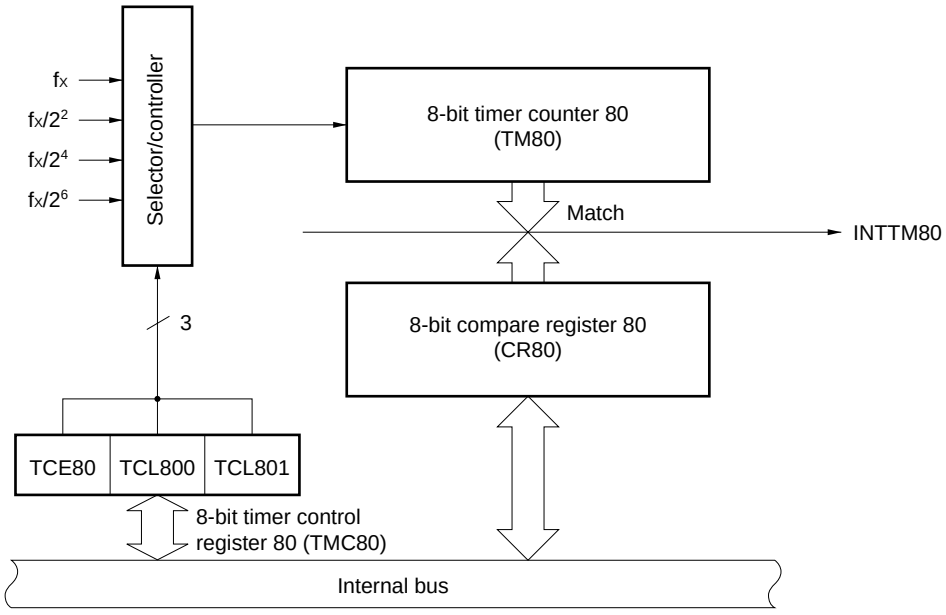
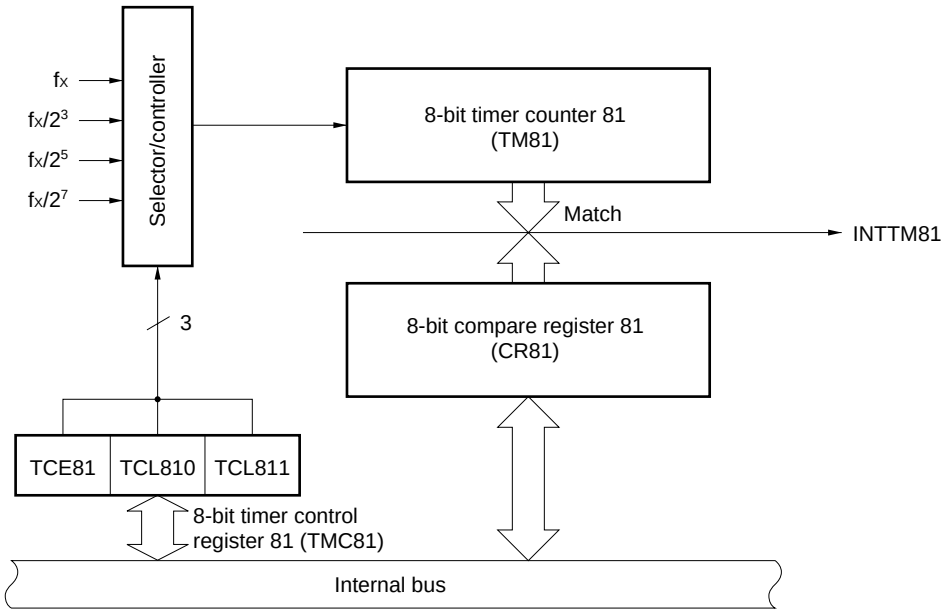


Figure 7-2. Block Diagram of 8-Bit Timer 81



(1) 8-bit timer counters 80, 81 (TM80, TM81)

These registers count the count pulses.

$\overline{\text{RESET}}$ input clears these registers to 00H.

(2) 8-bit compare registers 80, 81 (CR80, CR81)

These 8-bit registers constantly compare the value set in CR80 and the count value of 8-bit timer counter 80 (TM80), or the value set in the CR81 and the count value of 8-bit timer counter 81 (TM81). When these values match, an interrupt request is generated for the corresponding register (INTTM80 and INTTM81).

CR80 and CR81 can be set to 00H to FFH by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears these registers to 00H.

Caution Do not change the value of CR80 and CR81 during the timer count operation. However, the same value can be set.

7.3 Registers Controlling 8-Bit Timers 80, 81

8-bit timers 80 and 81 are controlled by 8-bit timer control register 8n (TMC8n).

(1) 8-bit timer control register 8n (TMC8n)

This register enables/stops the operation of 8-bit timer counter 8n and sets the count clock.

TMC8n is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC8n to 00H.

Remark n = 0,1

Figure 7-3. Format of 8-Bit Timer Control Register 80

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
TMC80	TCE80	0	0	0	0	0	TCL800	TCL801	FF60H	00H	R/W

TCE80	Controls count operation of TM80
0	Stops operation (Clears TM80 to 00H.)
1	Enables operation

TCL800	TCL801	Selects count clock of TM80
0	0	f_X (5.0 MHz)
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^4$ (313 kHz)
1	1	$f_X/2^6$ (78.1 kHz)

Cautions 1. Set TCL800 and TCL801 after stopping (TCE80 = 0) the timer operation.

2. Be sure to set bits 2 to 6 to “0”.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

Figure 7-4. Format of 8-Bit Timer Control Register 81

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
TMC81	TCE81	0	0	0	0	0	TCL810	TCL811	FF61H	00H	R/W

TCE81	Controls count operation of TM81
0	Stops operation (Clears TM81 to 00H.)
1	Enables operation

TCL810	TCL811	Selects count clock of TM81
0	0	$f_X/2$ (2.5 MHz)
0	1	$f_X/2^3$ (625 kHz)
1	0	$f_X/2^5$ (156 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

Cautions 1. Set TCL810 and TCL811 after stopping (TCE81 = 0) the timer operation.

2. Be sure to set bits 2 to 6 to “0”.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

7.4 Operation of 8-Bit Timers 80, 81

8-bit timers 80 and 81 operate as an interval timer that repeatedly generates interrupt requests at intervals specified by the count value preset in 8-bit compare register 8n (CR8n).

It generates an interrupt request signal (INTTM8n) at the same time as it clears the value of TM8n to “0” and continues counting when the count value of 8-bit timer counter 8n (TM8n) matches the value preset in CR8n.

The count clock of 8-bit timer control register 8n (TMC8n) can be selected by bits 0 and 1 of TM8n (TCL8n0 and TMC8n1).

[Setting]

<1> Set the registers after stopping the timer count operation (TCE8n = 0).
- CR8n: Compare value
- TMC8n: Count clock selection

<2> Starts timer count operation after setting TCE8n to 1.

<3> When the values of TM8n and CR8n match, INTTM8n is generated. (TM8n is cleared to 00H.)

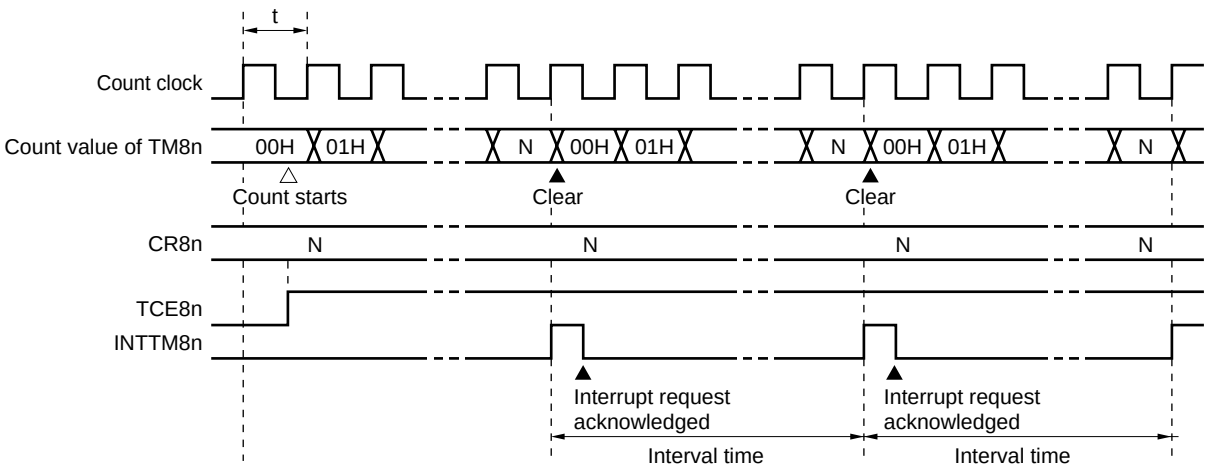
<4> Afterwards, INTTM8n is repeatedly generated at the same interval. Set TCE8n to 0 when stopping the timer count operation.

Caution Do not change the value of CR8n during the timer count operation. However, the same value can be set.

Remark n = 0,1

★ **Figure 7-5. Timing of Interval Timer Operation (1/2)**

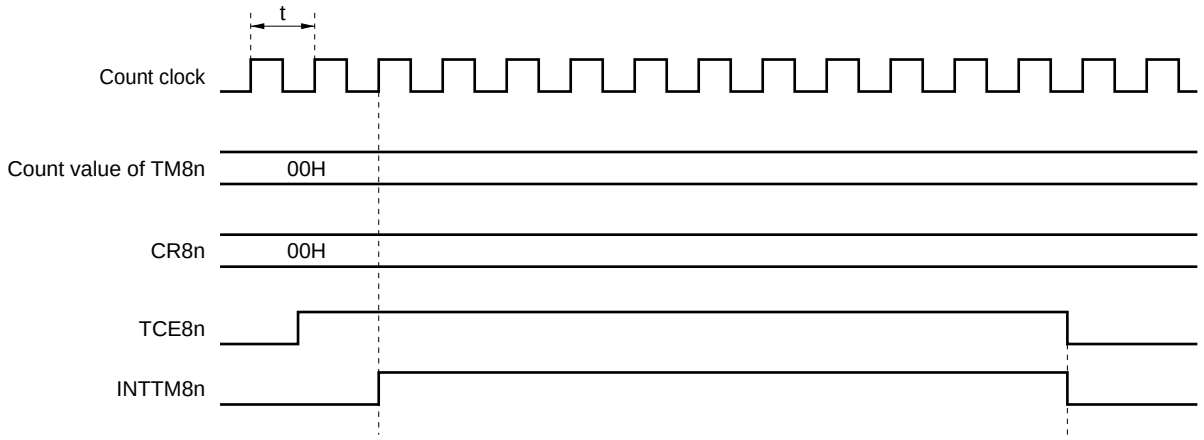
(a) Basic operation



Remark n = 0, 1

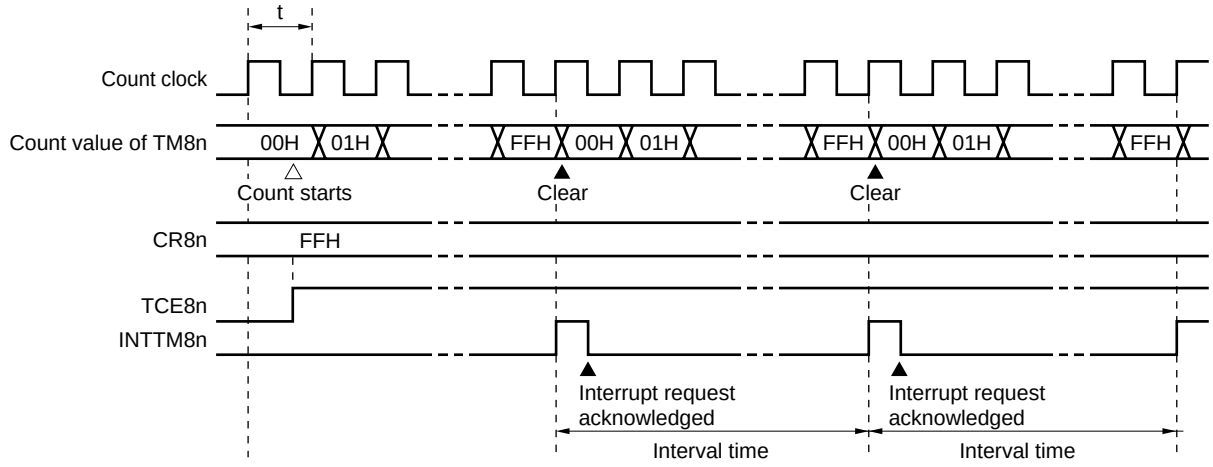
★ **Figure 7-5. Timing of Interval Timer Operation (2/2)**

(b) When CR8n = 00H



Caution When 00H is assigned to the CR8n, INTTM8n is fixed to high and a valid edge is output only at the first time.

(c) When CR8n = FFH



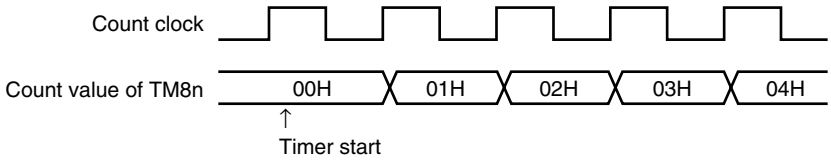
Remark n = 0,1

7.5 Caution When Using 8-Bit Timers 80, 81

(1) Time difference when the timer starts

There is a time difference of 1 clock at the maximum from the timer start to the generation of the match signal. This is because 8-bit timer counter 8n (TM8n) starts asynchronously with the count clock.

★ **Figure 7-6. Start Timing of 8-Bit Timer Counter 8n (TM8n)**



(2) Caution during the timer count operation

(a) 8-bit compare register 8n (CR8n)

Do not change the value of 8-bit compare register 8n (CR8n) during the timer count operation. However, the same value can be set.

Change the value of CR8n after stopping the timer count operation (TCE8n = 0).

(b) Bits 0, 1 (TCL8n0, TCL8n1) of 8-bit timer control register 8n (TMC8n)

Do not set to bits 0 and 1 (TCL8n0, TCL8n1) of 8-bit timer control register 8n during the timer count operation.

Set TCL8n0 and TCL8n1 after stopping the timer count operation (TCE = 0).

Remark n = 0, 1

CHAPTER 8 WATCHDOG TIMER

8.1 Function of Watchdog Timer

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer
- Selection of oscillation stabilization time

Caution Select whether the watchdog timer is used in the watchdog timer mode or interval timer mode, by using the watchdog timer mode register (WDTM) (The watchdog timer and internal timer cannot be used simultaneously). ★

(1) Watchdog timer mode

In this mode, the watchdog timer detects an inadvertent program loop. On detection of program loop, the non-maskable interrupt or $\overline{\text{RESET}}$ signal can be generated.

Table 8-1. Program Loop Detection Time of Watchdog Timer

Program Loop Detection Time	f_X = 5.0 MHz	Program Loop Detection Time	f_X = 5.0 MHz
$2^{12}/f_X$	819 μs	$2^{16}/f_X$	13.1 ms
$2^{13}/f_X$	1.64 ms	$2^{17}/f_X$	26.2 ms
$2^{14}/f_X$	3.28 ms	$2^{18}/f_X$	52.4 ms
$2^{15}/f_X$	6.55 ms	$2^{20}/f_X$	210 ms

f_X: Main system clock oscillation frequency

(2) Interval timer mode

In this mode, the watchdog timer generates an interrupt request at fixed time intervals.

Table 8-2. Interval Time

Interval Time	f_X = 5.0 MHz	Interval Time	f_X = 5.0 MHz
$2^{12}/f_X$	819 μs	$2^{16}/f_X$	13.1 ms
$2^{13}/f_X$	1.64 ms	$2^{17}/f_X$	26.2 ms
$2^{14}/f_X$	3.28 ms	$2^{18}/f_X$	52.4 ms
$2^{15}/f_X$	6.55 ms	$2^{20}/f_X$	210 ms

f_X: Main system clock oscillation frequency

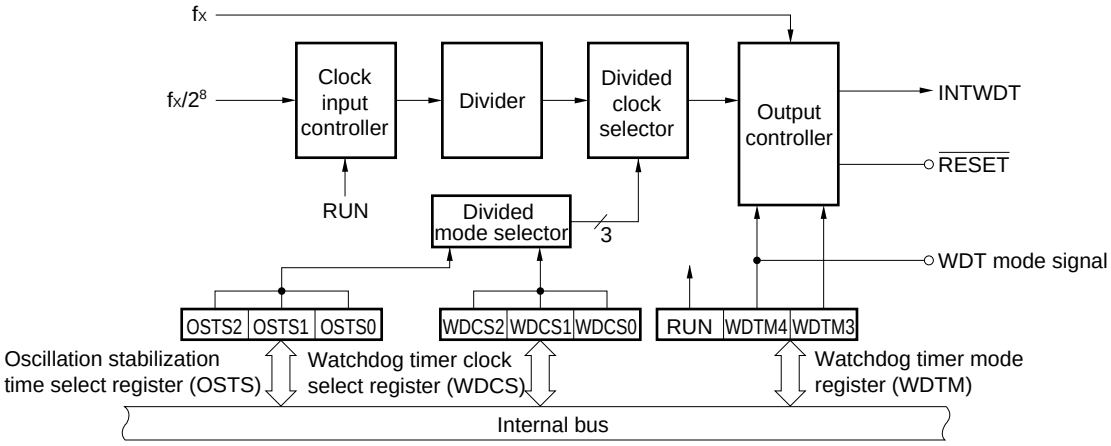
8.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 8-3. Configuration of Watchdog Timer

Item	Configuration
Control register	Oscillation stabilization time select register (OSTS) Watchdog timer clock select register (WDCS) Watchdog timer mode register (WDTM)

Figure 8-1. Block Diagram of Watchdog Timer



8.3 Registers Controlling Watchdog Timer

The following three types of registers control the watchdog timer.

- Oscillation stabilization time select register (OSTS)
- Watchdog timer clock select register (WDCS)
- Watchdog timer mode register (WDTM)

(1) Oscillation stabilization time select register (OSTS)

This register selects the oscillation stabilization time during which oscillation is stabilized after the $\overline{\text{RESET}}$ signal has been deasserted or the STOP mode has been released.

OSTS is set by an 8-bit memory manipulation instruction.

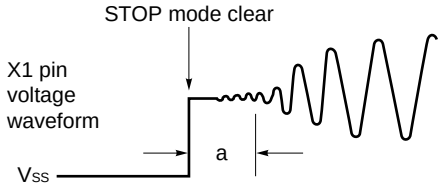
$\overline{\text{RESET}}$ input sets OSTS to 04H. Therefore, when clearing STOP mode by $\overline{\text{RESET}}$ input, it takes $2^{17}/f_X$ until cleared.

Figure 8-2. Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selects oscillation stabilization time at STOP mode release
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{14}/f_X$ (3.28 ms)
0	1	0	$2^{15}/f_X$ (6.55 ms)
0	1	1	$2^{16}/f_X$ (13.1 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Other			Setting prohibited

Caution The wait time after STOP mode clear does not include the time (see "a" below) from STOP mode clear to clock oscillation start, regardless of clearance by $\overline{\text{RESET}}$ input or by interrupt request generation.



Remarks 1. f_X: Main system clock frequency

2. ( ): f_X = 5.0 MHz

(2) Watchdog timer clock select register (WDCS)

This register selects the overflow time of the watchdog timer or interval timer.

WDCS is set by an 8-bit manipulation instruction.

$\overline{\text{RESET}}$ input clears WDCS to 00H.

Figure 8-3. Format of Watchdog Timer Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
WDCS	0	0	0	0	0	WDCS2	WDCS1	WDCS0	FF42H	00H	R/W

WDCS2	WDCS1	WDCS0	Overflow time of watchdog timer/interval timer
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{13}/f_X$ (1.64 ms)
0	1	0	$2^{14}/f_X$ (3.28 ms)
0	1	1	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{16}/f_X$ (13.1 ms)
1	0	1	$2^{17}/f_X$ (26.2 ms)
1	1	0	$2^{18}/f_X$ (52.4 ms)
1	1	1	$2^{20}/f_X$ (210 ms)

★ **Caution Be sure to set bits 3 to 7 to “0”.**

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

(3) Watchdog timer mode register (WDTM)

This register selects the operation mode of the watchdog timer, and enables or disables the counting operation.

WDTM is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears WDTM to 00H.

Figure 8-4. Format of Watchdog Timer Mode Register

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Selects operation of watchdog timer[Note 1]
0	Stops counting
1	Clears counter and starts counting

WDTM4	WDTM3	Selects operation mode of watchdog timer[Note 2]
0	×	Interval timer mode[Note 3] (Maskable interrupt request occurs when overflow occurs.)
1	0	Watchdog timer mode 1 (Non-maskable interrupt request occurs when overflow occurs.)
1	1	Watchdog timer mode 2 (Reset operation is started when overflow occurs.)

Notes 1. The RUN bit cannot be cleared to 0 by software once it has been set. Therefore, counting cannot be stopped, after it has been started, by any means other than $\overline{\text{RESET}}$ input.

2. The WDTM3 and WDTM4 bits cannot be cleared to 0 by software once they have been set.

3. The register starts interval timer operation when RUN is set to 1.

★ **Caution When the RUN bit is set to 1 and the watchdog timer is cleared, the actual overflow time is up to $2^8/f_X$ seconds shorter than the time set in the watchdog timer clock select register (WDCS).**

Remark ×: don't care

8.4 Operation of Watchdog Timer

8.4.1 Operation as watchdog timer

The watchdog timer operates to detect a program loop when bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is set to 1.

The program loop detection time interval of the watchdog timer can be selected by bits 0 to 2 (WDCS0 to WDCS2) of the watchdog timer clock select register (WDCS). By setting bit 7 (RUN) of WDTM, the watchdog timer starts the count operation. If RUN is set to 1 again within the specified program loop detection time interval after the counting operation has been started, the watchdog timer is cleared and starts the count operation again.

If RUN is not set to 1 and the program loop detection time is exceeded, the system is reset or a non-maskable interrupt request is generated depending on the value of bit 3 (WDTM3) of WDTM.

The watchdog timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 and clear the watchdog timer before executing the STOP instruction to set the STOP mode.

★ **Caution The actual program loop detection time may be up to $2^8/f_X$ seconds shorter than the set time.**

Table 8-4. Program Loop Detection Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Program Loop Detection Time of Watchdog Timer
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{13}/f_X$ (1.64 ms)
0	1	0	$2^{14}/f_X$ (3.28 ms)
0	1	1	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{16}/f_X$ (13.1 ms)
1	0	1	$2^{17}/f_X$ (26.2 ms)
1	1	0	$2^{18}/f_X$ (52.4 ms)
1	1	1	$2^{20}/f_X$ (210 ms)

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

8.4.2 Operation as interval timer

The watchdog timer operates as an interval timer that repeatedly generates an interrupt request at intervals specified by the preset count value if bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is cleared to 0.

The interval time of the interval timer can be selected by bits 0 to 2 (WDCS0 to WDCS2) of the watchdog timer clock select register (WDCS). By setting bit 7 (RUN) of WDTM to 1, the watchdog timer starts interval timer operation.

★ While the watchdog timer is operating as an interval timer, the interrupt mask flag (WDTMK) and priority specification flag (WDTPR) are valid, and a maskable interrupt (INTWDT) can be generated. The default priority of INTWDT is the highest of all the maskable interrupts.

The interval timer continues operating in the HALT mode, but stops in the STOP mode. Therefore, set RUN and clear the interval timer before executing the STOP instruction to set the STOP mode.

Cautions 1. If bit 4 (WDTM4) of WDTM has been set to 1 (to select the watchdog timer mode), the interval timer mode cannot be set unless the $\overline{\text{RESET}}$ signal is input.

★ **2. The interval time immediately after WDTM has been set may be up to $2^8/f_X$ seconds shorter than the set time.**

Table 8-5. Interval Time of Interval Timer

WDCS2	WDCS1	WDCS0	Interval Time
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{13}/f_X$ (1.64 ms)
0	1	0	$2^{14}/f_X$ (3.28 ms)
0	1	1	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{16}/f_X$ (13.1 ms)
1	0	1	$2^{17}/f_X$ (26.2 ms)
1	1	0	$2^{18}/f_X$ (52.4 ms)
1	1	1	$2^{20}/f_X$ (210 ms)

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

CHAPTER 9 A/D CONVERTER

9.1 Function of A/D Converter

The A/D converter converts analog input signals into digital values with a resolution of 8 bits. Up to four analog input channels (ANI0 to ANI3) can be controlled.

The A/D conversion operation can be started only by software.

One of the analog input channels, ANI0 to ANI3, is selected for A/D conversion. The A/D conversion operation is repeatedly performed, and an interrupt request (INTAD) is generated each time the A/D conversion has been completed.

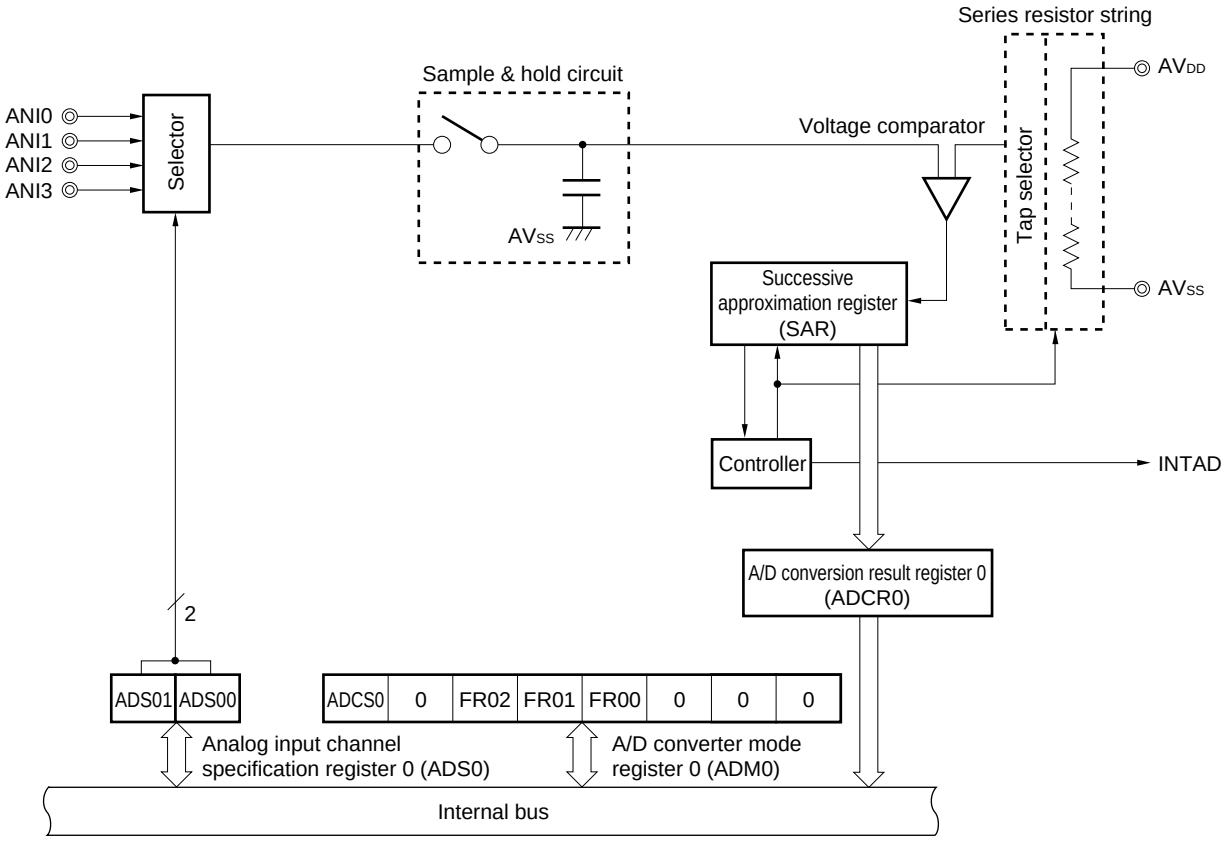
9.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

Table 9-1. Configuration of A/D Converter

Item	Configuration
Analog input	4 channels (ANI0 to ANI7)
Register	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control register	A/D converter mode register 0 (ADM0) Analog input channel specification register 0 (ADS0)

Figure 9-1. Block Diagram of A/D Converter



(1) Successive approximation register (SAR)

This register compares the voltage value of the input analog signal with the value of the voltage tap (compare voltage) from the series resistor string, and holds the result of the comparison, starting from the most significant bit (MSB).

When the comparison result is held down to the least significant bit (LSB) (i.e., when the A/D conversion is complete), the contents of this register are transferred to A/D conversion result register 0 (ADCR0).

(2) A/D conversion result register 0 (ADCR0)

This register holds the result of the A/D conversion. Each time an A/D conversion is complete, the conversion result is loaded to this register from the successive approximation register (SAR).

ADCR0 is read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes ADCR0 undefined.

Caution When writing to A/D converter mode register 0 (ADM0) and analog input channel specification register 0 (ADS0), the contents of ADCR0 may be undefined. Read the conversion results before writing to ADM0 or ADS0 after the conversion; otherwise an incorrect conversion result may be read.

(3) Sample & hold circuit

★ The sample & hold circuit samples the input signal of the analog input pin selected with the selector at the start of A/D conversion, and maintains this sampled analog input voltage value while A/D conversion is performed.

(4) Voltage comparator

★ The voltage comparator compares the sampled analog input voltage and the output voltage of the series resistor string.

(5) Series resistor string

The series resistor string is connected between the AV_{DD} and AV_{SS} pins, and generates a voltage to be compared with the input analog signal.

(6) ANI0 to ANI3 pins

These are four channels of analog input pins of the A/D converter, and input analog signals to be converted.

Cautions 1. Make sure that the input voltages of ANI0 to ANI3 are within the rated range. If a voltage greater than AV_{DD} or less than AV_{SS} is input a channel (even if it is within the absolute maximum rating range), the converted value of the channel is undefined, and, in the worst case, the converted values of the other channels are affected.

★ **2. When a digital pulse is applied to a pin adjacent to the analog input pins during A/D conversion, the expected A/D conversion value may not be obtained because of coupling noise. Therefore, do not apply a pulse to the pins adjacent to the analog input pins during A/D conversion.**

(7) AV_{SS} pin

★ This is the ground potential pin of the A/D converter. Make sure this pin is always at the same potential as the V_{SS0} or V_{SS1} pin even when the A/D converter is not used.

(8) AV_{DD} pin

★ This is the analog power supply pin of the A/D converter. Make sure that this pin is always at the same potential as the V_{DD0} or V_{DD1} pin even when the A/D converter is not used.

In the standby mode, the current flowing to the series resistor string can be lowered by stopping the conversion operation (by clearing bit 7 (ADCS0) of A/D converter mode register 0 (ADM0)).

Caution A series resistor string of several 10 kΩ is connected between the AV_{DD} and AV_{SS} pins. If the output impedance of the reference voltage source is high, therefore, the error of the reference voltage increases by connecting the impedance in series with the series resistor string between the AV_{DD} and AV_{SS} pins.

9.3 Registers Controlling A/D Converter

The following two types of registers control the A/D converter.

- A/D converter mode register 0 (ADM0)
- Analog input channel specification register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

This register specifies the conversion time of the input analog signal to be converted, and starts or stops the conversion operation.

ADM0 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADM0 to 00H.

Figure 9-2. Format of A/D Converter Mode Register 0

	Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
★	ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF67H	00H	R/W

ADCS0	Control A/D conversion operation
0	Stops conversion
1	Enables conversion

FR02	FR01	FR00	Selects A/D conversion time[Note 1]	
			f_X = 5.0 MHz	f_X = 4.19 MHz
0	0	0	144/f_X (28.8 μs)	144/f_X (34.4 μs)
0	0	1	120/f_X (24 μs)	120/f_X (28.6 μs)
0	1	0	96/f_X (19.2 μs)	96/f_X (22.9 μs)
1	0	0	72/f_X (14.4 μs)	72/f_X (17.2 μs)
1	0	1	60/f_X (setting prohibited[Note 2])	60/f_X (14.3 μs)
1	1	0	48/f_X (setting prohibited[Note 2])	48/f_X (setting prohibited[Note 2])
Other			Setting prohibited	

Notes 1. Make sure that the A/D conversion time is 14 μs or longer.

2. These settings are prohibited because the A/D conversion time is less than 14 μs.

Cautions 1. The conversion result is undefined immediately after bit 7 (ADCS0) has been set.

2. Stop A/D conversion before rewriting FR00 to FR02.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz operation.

(2) Analog input channel specification register 0 (ADS0)

This register specifies a port that inputs the analog voltage to be converted.

★ ADS0 is set by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADS0 to 00H.

Figure 9-3. Format of Analog Input Channel Specification Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
★ ADS0	0	0	0	0	0	0	ADS01	ADS00	FF68H	00H	R/W

ADS01	ADS00	Specifies analog input channel
0	0	ANI0
0	1	ANI1
1	0	ANI2
1	1	ANI3
Other		Setting prohibited

Caution Be sure to set bits 2 to 7 to “0”.

9.4 Operation of A/D Converter

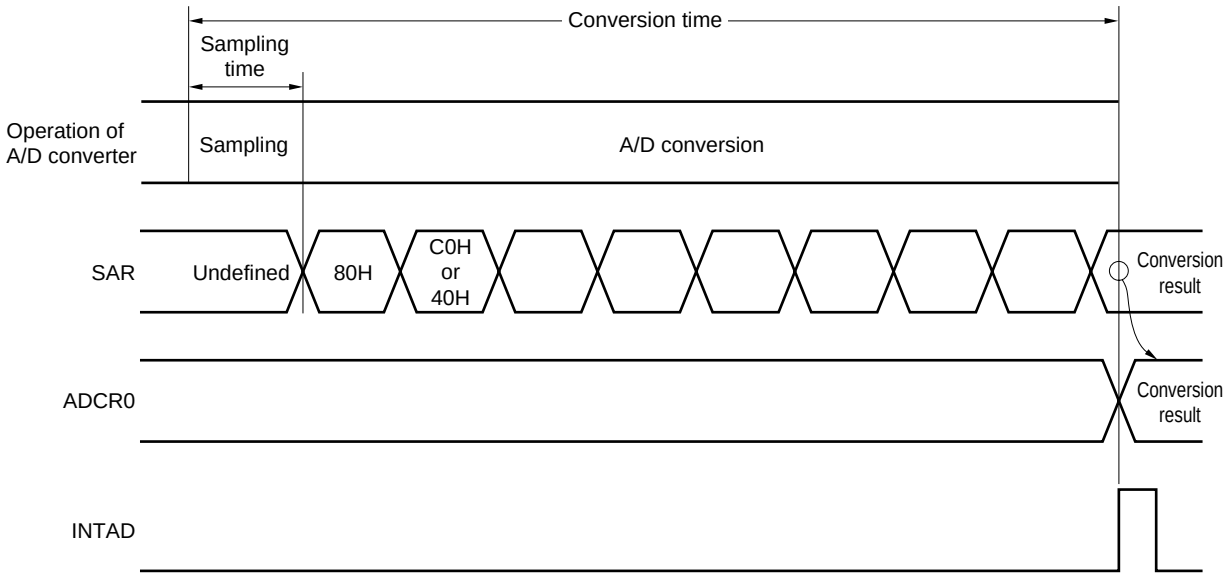
9.4.1 Basic operation of A/D converter

(1) Select one channel for A/D conversion using analog input channel specification register 0 (ADS0).
(2) The sample & hold circuit samples the voltage input to the selected analog input channel.
(3) The sample & hold circuit enters the hold status after it has performed sampling for fixed time, and holds the input analog voltage until the A/D conversion is complete.
(4) Bit 7 of the successive approximation register (SAR) is set. The tap selector sets the voltage tap of the series resistor string to (1/2) AV_{DD}.
(5) The voltage comparator compares the voltage difference between the voltage of the series resistor string and voltage tap. If the input analog voltage is greater than (1/2) AV_{DD}, the MSB of SAR remains set. If it is less than (1/2) AV_{DD}, MSB is reset.
(6) Bit 6 of SAR is automatically set, and the next comparison is performed. The voltage tap of the series resistor string is selected as follows, depending on the value of bit 7 to which the result has been already set.
   - Bit 7 = 1: (3/4) AV_{DD}
   - Bit 7 = 0: (1/4) AV_{DD}

   This voltage tap is compared with the input analog voltage. Depending on this result, bit 6 of SAR is manipulated as follows.
   - If input analog voltage ≥ voltage tap: Bit 6 = 1
   - If input analog voltage < voltage tap: Bit 6 = 0
(7) Comparison continues like this up to bit 0 of SAR.
(8) When comparison of 8 bits has been completed, the valid digital result remains in SAR, and its value is transferred and latched to A/D conversion result register 0 (ADCR0).
   At the same time, an A/D conversion end interrupt request (INTAD) is generated.

Caution The first A/D conversion value immediately after the A/D conversion is started may not satisfy the ratings.

Figure 9-4. Basic Operation of A/D Converter



A/D conversion is performed continuously until bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is reset to 0 by software.

If an attempt is made to write data to ADM0 or analog input channel specification register 0 (ADS0) during A/D conversion, the conversion is initialized and started from the beginning if ADCS0 is set to 1.

The value of A/D conversion result register 0 (ADCR0) is undefined when the $\overline{\text{RESET}}$ signal is input.

★ Check A/D conversion end with the A/D conversion end interrupt request flag (ADIF).

9.4.2 Input voltage and conversion result

★ The analog voltage input to an analog input pin (ANI0 to ANI3) and the theoretical result of A/D conversion (A/D conversion result register 0 (ADCR0)) have the following relationship.

$$ADCR0 = INT\left(\frac{V_{IN}}{AV_{DD}} \times 256 + 0.5\right)$$

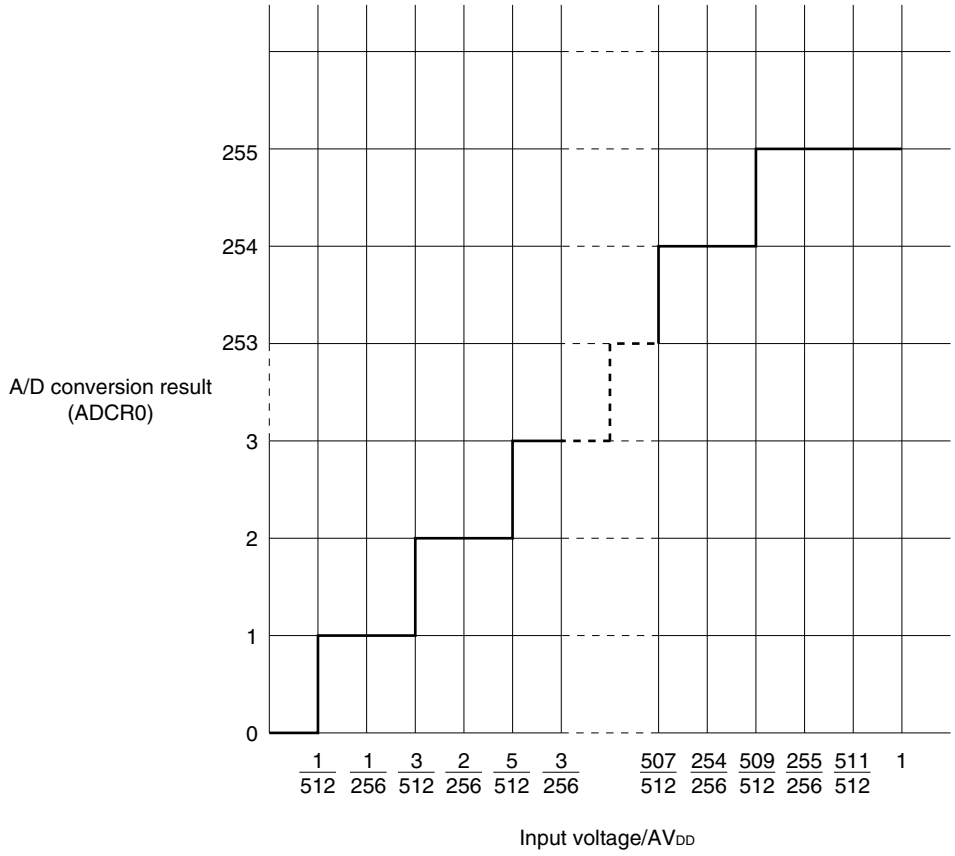
or,

$$(ADCR0 - 0.5) \times \frac{AV_{DD}}{256} \leq V_{IN} < (ADCR0 + 0.5) \times \frac{AV_{DD}}{256}$$

INT( ): Function that returns integer of value in ( )
V_{IN}: Analog input voltage
AV_{DD}: Supply voltage to A/D converter
ADCR0: Value of A/D conversion result register 0 (ADCR0)

Figure 9-5 shows the relationship between the analog input voltage and A/D conversion result.

Figure 9-5. Relationship Between Analog Input Voltage and A/D Conversion Result



9.4.3 Operation mode of A/D converter

Select one analog input channel from ANI0 to ANI3 using analog input channel specification register 0 (ADS0) to start A/D conversion.

★ The A/D conversion operation can be started only by software (by setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 1).

The A/D conversion result is stored in A/D conversion result register 0 (ADCR0), and an interrupt request signal (INTAD) is generated.

- A/D conversion by software start

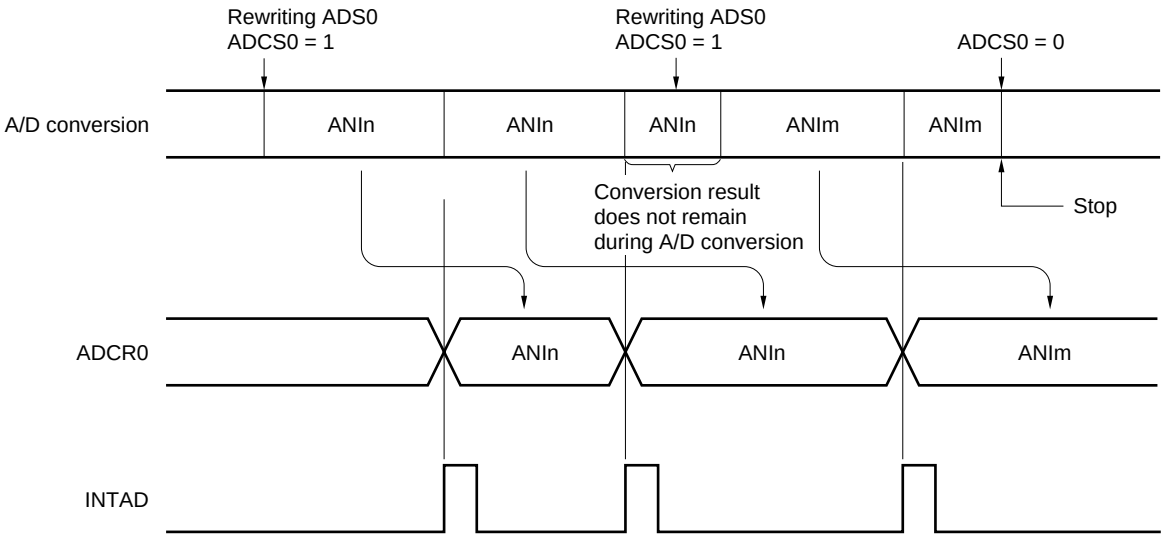
  Converting the voltage applied to the analog input pin specified by analog input channel specification register 0 (ADS0) is started when bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is set to 1.

  When A/D conversion is complete, the conversion result is stored in A/D conversion result register 0 (ADCR0), and an interrupt request (INTAD) is generated. When A/D conversion is started and completed, the next conversion is immediately started. This is repeated until new data is written to ADS0.

  If ADS0 is rewritten during A/D conversion, the conversion under execution is stopped, and conversion of the selected analog input channel is started.

  If data with ADCS0 being 0 is written to ADM0 during A/D conversion, the conversion is immediately stopped.

Figure 9-6. A/D Conversion by Software Start



Remark n = 0 to 3
m = 0 to 3

★ 9.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 8 bits.

$1LSB = 1/2^8 = 1/256$
$= 0.4\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a (1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of (1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the overall error is not included in the characteristics table.

Figure 9-7. Overall Error

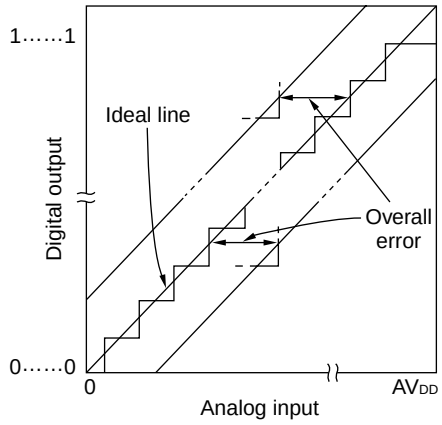
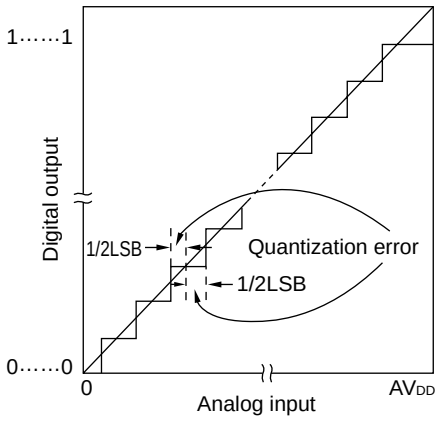


Figure 9-8. Quantization Error



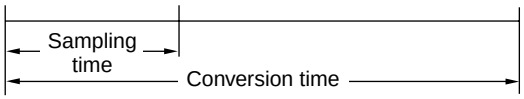
(4) Conversion time

This expresses the time since sampling has been started until digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(5) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



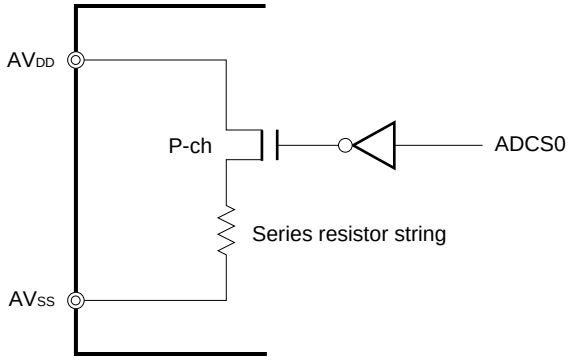
9.6 Cautions for A/D Converter

(1) Power consumption in standby mode

The A/D converter stops operating in the standby mode. At this time, the power consumption can be reduced by stopping the conversion operation by clearing bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 0.

Figure 9-9 shows the circuit configuration of series resistor string.

Figure 9-9. Circuit Configuration of Series Resistor String



(2) Input range of ANI0 to ANI3

Observe the rated range of the ANI0 to ANI3 input voltage. If a voltage of AV_{DD} or higher and AV_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operation

<1> Conflict between writing and reading A/D conversion result register 0 (ADCR0) on completion of conversion

Reading ADRC0 takes precedence. After ADCR0 has been read, a new conversion result is written to ADCR0.

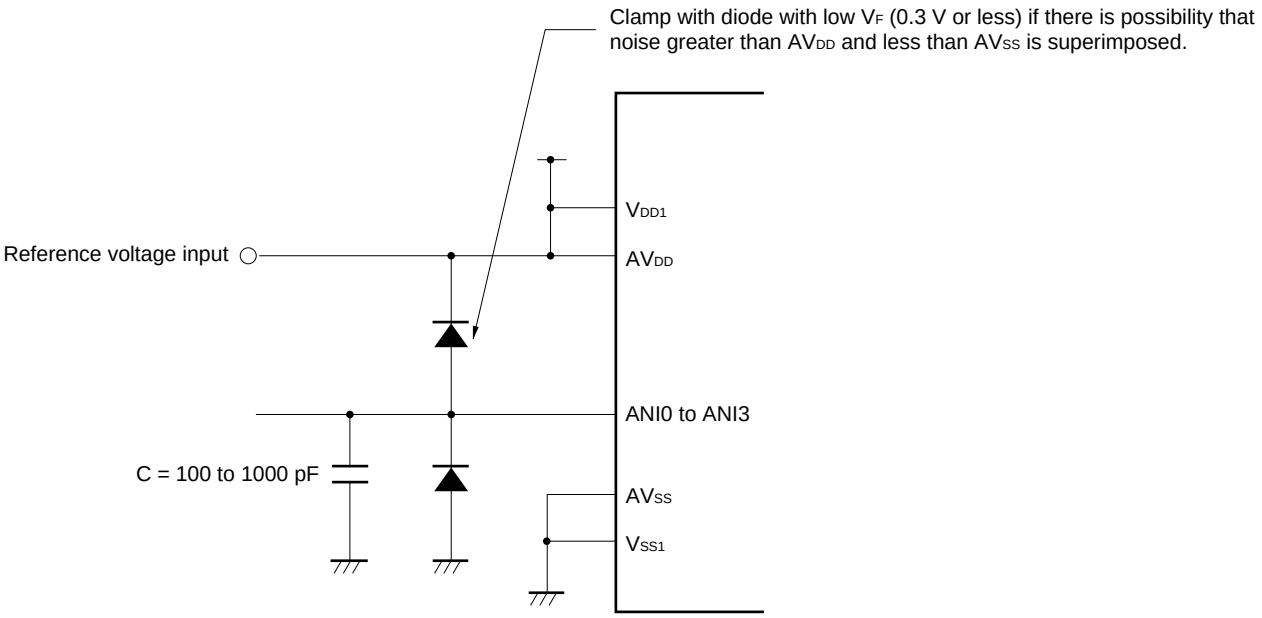
<2> Conflict between writing ADCR0 and writing A/D converter mode register 0 (ADM0) or writing analog input channel specification register 0 (ADS0) on completion of conversion

Writing ADM0 or ADS0 takes precedence. ADCR0 is not written. Nor is the conversion end interrupt request signal (INTAD) generated.

(4) Noise measures

To maintain the 8-bit resolution, care must be exercised that no noise is superimposed on the AV_{DD} and ANI0 to ANI3 pins. The higher the output impedance of the analog input source, the heavier the influence of noise. To suppress noise, connecting external C as shown in Figure 9-10 is recommended.

Figure 9-10. Processing of Analog Input Pin



(5) ANI0 to ANI3

When a digital pulse is applied to a pin adjacent to the analog input pins during A/D conversion, the expected A/D conversion value may not be obtained because of coupling noise. Therefore, do not apply a pulse to the pins adjacent to the analog input pins during A/D conversion.

★ **(6) Input impedance of ANI0 to ANI3 pins**

In this A/D converter, the internal sampling capacitor is charged and sampling is performed for approx. one tenth of the conversion time.

Since only the leakage current flows other than during sampling and the current for charging the capacitor also flows during sampling, the input impedance fluctuates and has no meaning.

To perform sufficient sampling, however, it is recommended to make the output impedance of the analog input source 10 kΩ or lower, or attach a capacitor of around 100 pF to the ANI0 to ANI3 pins (see **Figure 9-10**).

(7) Input impedance of AV_{DD} pin

A series resistor string of several 10 kΩ is connected between the AV_{DD} and AV_{SS} pins. If the output impedance of the reference voltage source is high, therefore, the error of the reference voltage increases by connecting the impedance in series with the series resistor string between the AV_{DD} and AV_{SS} pins.

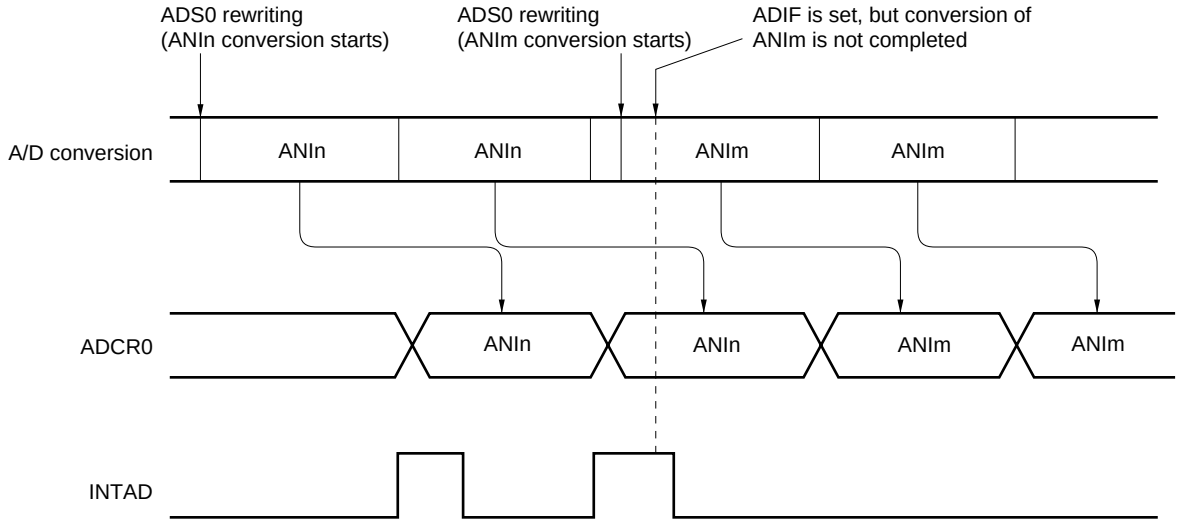
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the contents of analog input channel specification register 0 (ADS0) are changed.

If the analog input pin is changed during A/D conversion, therefore, the A/D conversion result of the previous analog input may be written to ADS0 immediately before ADS0 is rewritten, and consequently, the conversion end interrupt flag may be set. If ADIF is read immediately after ADS0 has been rewritten, ADIF may be set despite that the A/D conversion of the new analog input has not been completed.

Clear ADIF before resuming A/D conversion that has been stopped.

Figure 9-11. A/D Conversion End Interrupt Request Generation Timing

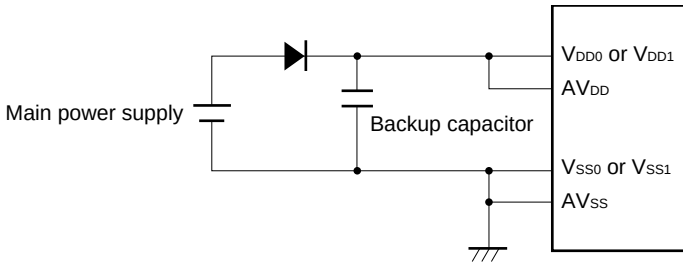


Remark n = 0 to 3
m = 0 to 3

(9) AV_{DD} pin

The AV_{DD} pin supplies power to the analog circuit. It also supplies power to the input circuit of ANI0 to ANI3. ★ Therefore, apply the same potential as that of the V_{DD0} or V_{DD1} pin to this pin, as shown in Figure 9-12, in an application where a backup power supply is used.

Figure 9-12. Processing of AV_{DD} Pin



(10) Conversion result immediately after starting A/D conversion

The first A/D conversion result value is undefined immediately after the A/D conversion operation has been started. Poll the A/D conversion completion interrupt request (INTAD) to discard the first conversion result.

(11) Reading A/D conversion result register 0 (ADCR0)

When writing in A/D converter mode register 0 (ADM0) and analog input channel specification register 0 (ADS0), the contents of ADCR0 may be undefined. Read the result of the conversion before writing in ADM0 or ADS0 after the conversion. Otherwise, an incorrect conversion result may read.

★ **(12) Timing at which A/D conversion result is undefined**

The A/D conversion value may be undefined if the timing of completion of A/D conversion and the timing of stopping the A/D conversion conflict with each other. Therefore, read the the A/D conversion result during the A/D conversion operation. To read the conversion result after stopping the A/D conversion operation, be sure to stop the A/D conversion before the next conversion ends.

Figures 9-13 and 9-14 show the timing of reading the conversion result.

Figure 9-13. Timing of Reading Conversion Result (When Conversion Result Is Undefined)

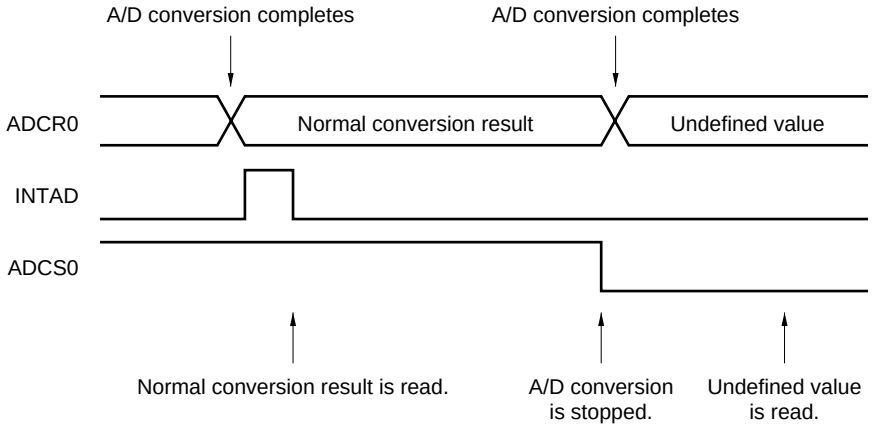
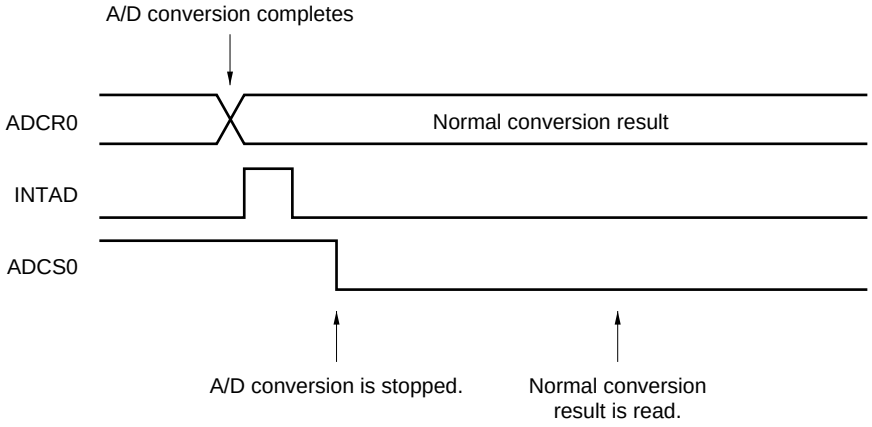


Figure 9-14. Timing of Reading Conversion Result (When Conversion Result Is Normal)



★ **(13) Notes on board design**

Locate analog circuits as far away from digital circuits as possible on the board because the analog circuits may be affected by the noise of the digital circuits. In particular, do not cross an analog signal line with a digital signal line, or wire an analog signal line in the vicinity of a digital signal line. Otherwise, the A/D conversion characteristics may be affected by the noise of the digital line.

Connect AV_{SS} and V_{SS0} or V_{SS1} at one location on the board where the voltages are stable.

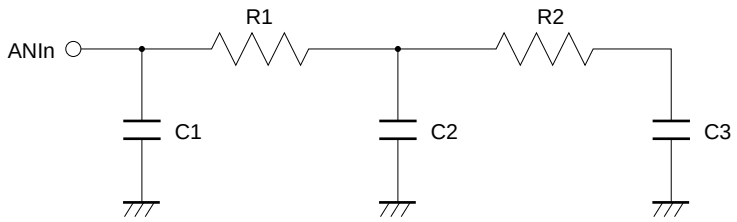
★ **(14) Internal equivalent circuit of ANI0 to ANI3 pins and permissible signal source impedance**

To complete sampling within the sampling time with sufficient A/D conversion accuracy, the impedance of the signal source such as a sensor must be sufficiently low. Figure 9-15 shows the internal equivalent circuit of the ANI0 to ANI3 pins.

If the impedance of the signal source is high, connect capacitors with a high capacitance to the pins ANI0 to ANI3. An example of this is shown in Figure 9-16. In this case, however, the microcontroller cannot follow an analog signal with a high differential coefficient because a lowpass filter is created.

To convert a high-speed analog signal or to convert an analog signal in the scan mode, insert a low-impedance buffer.

Figure 9-15. Internal Equivalent Circuit of Pins ANI0 to ANI3



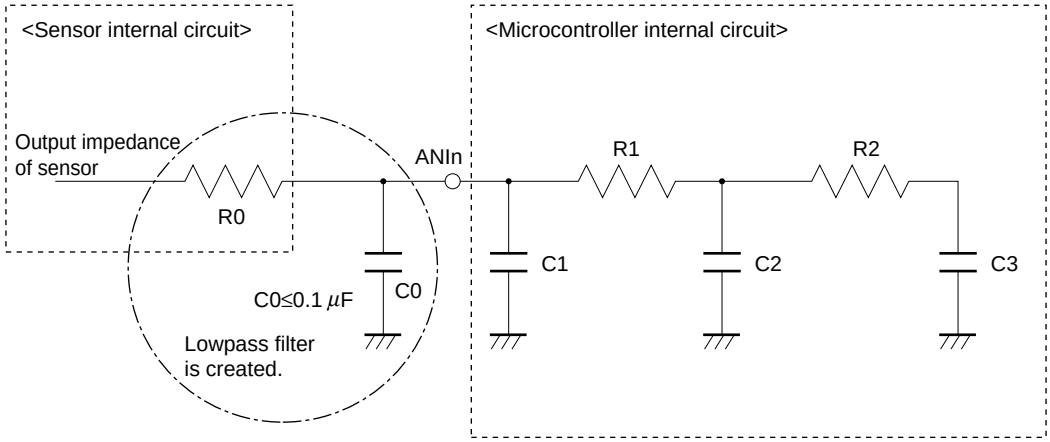
Remark n = 0 to 3

Table 9-2. Resistances and Capacitances of Equivalent Circuit (Reference Values)

AV_{DD}	R1	R2	C1	C2	C3
4.5 V	4 kΩ	2.7 kΩ	8 pF	1.4 pF	2 pF

Caution The resistances and capacitances in Table 9-2 are not guaranteed values.

Figure 9-16. Example of Connection If Signal Source Impedance Is High



Remark n = 0 to 3

CHAPTER 10 SERIAL INTERFACE SIO1

10.1 Functions of Serial Interface SIO1

Serial interface SIO1 employs the following three modes.

- Operation stop mode
- 3-wire serial mode
- 3-wire serial mode with automatic transmit/receive function

(1) Operation stop mode

This mode is used when serial transfer is not carried out to reduce power consumption. For details, refer to **10.4.1 Operation stop mode**.

(2) 3-wire serial mode (MSB/LSB first switchable)

This mode is used for 8-bit data transfer using three lines, each for serial clock ($\overline{\text{SCK1}}$), serial output (SO1) and serial input (SI1).

The 3-wire serial mode enables simultaneous transmission/reception and so decreases the data transfer processing time.

Since the start bit of 8-bit data to undergo serial transfer is switchable between MSB and LSB, connection is enabled with either start bit device.

The 3-wire serial mode is valid for connection of peripheral IC units and display controllers which incorporate a conventional synchronous serial interface. For details, refer to **10.4.2 3-wire serial mode**.

(3) 3-wire serial mode with automatic transmit/receive function (MSB/LSB first switchable)

This mode has an automatic transmit/receive function in addition to the functions in **(2)** above.

The automatic transmit/receive function is used to transmit/receive data with a maximum of 32 bytes. This function enables the hardware to transmit/receive data to/from the OSD (On Screen Display) device and a device with built-in display controller/driver independently of the CPU, thus the software load can be alleviated. For details, refer to **10.4.3 3-wire serial mode with automatic transmit/receive function**.

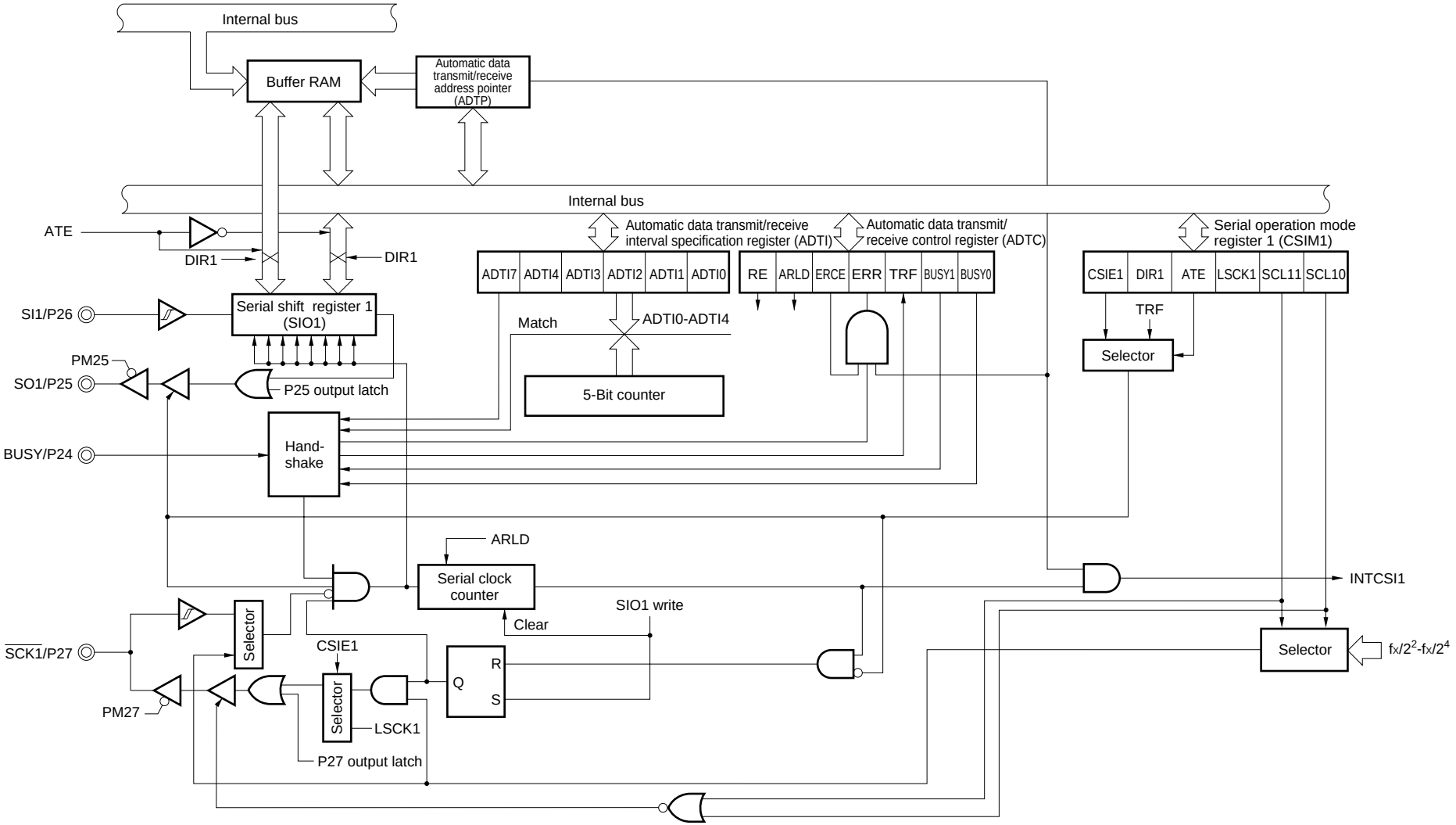
10.2 Configuration of Serial Interface SIO1

Serial interface SIO1 includes the following hardware.

Table 10-1. Configuration of Serial Interface SIO1

Item	Configuration
Register	Serial shift register 1 (SIO1) Automatic data transmit/receive address pointer (ADTP)
Control register	Serial operation mode register 1 (CSIM1) Automatic data transmit/receive control register (ADTC) Automatic data transmit/receive interval specification register (ADTI)

Figure 10-1. Block Diagram of Serial Interface SIO1



(1) Serial shift register 1 (SIO1)

This is an 8-bit register to carry out parallel/serial conversion and to carry out serial transmission/reception (shift operation) in synchronization with the serial clock.

SIO1 is set by an 8-bit memory manipulation instruction.

When the value in bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is 1, writing data to SIO1 starts serial operation.

In transmission, data written to SIO1 is output to the serial output (SO1). In reception, data is read from the serial input (SI1) to SIO1.

$\overline{\text{RESET}}$ input clears SIO1 to 00H.

Caution Do not write data to SIO1 while the automatic transmit/receive function is activated.

(2) Automatic data transmit/receive address pointer (ADTP)

This register stores value of (transmit data byte – 1) while the automatic transmit/receive function is activated. As data is transferred/received, it is automatically decremented.

ADTP is set by an 8-bit memory manipulation instruction. The higher 3 bits must be set to 0.

$\overline{\text{RESET}}$ input makes ADTP undefined.

Caution Do not write data to ADTP while the automatic transmit/receive function is activated.

(3) Serial clock counter

This counter counts the serial clocks to be output and input during transmission/reception to check whether 8-bit data has been transmitted/received.

10.3 Registers Controlling Serial Interface SIO1

The following three types of registers are used to control serial interface SIO1.

- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive interval specification register (ADTI)

(1) Serial operation mode register 1 (CSIM1)

This register sets serial interface SIO1 serial clock, operating mode, operation enable/stop and automatic transmit/receive operation enable/stop, $\overline{\text{SCK1}}$ pin chip enable control.

CSIM1 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM1 to 00H.

Caution Set the port mode register (PMxx) in the 3-wire serial mode as follows. Set the output latch to 0.

<Serial clock setting>

- **In the case of serial clock output (master transmission or master reception):**
  Set P27 ($\overline{\text{SCK1}}$) to the output mode (PM27 = 0).
- **In the case of serial clock input (slave transmission or slave reception):**
  Set P27 to input mode (PM27 = 1).

<Operation mode setting>

- **In transmission or transmission/reception mode:**
  Set P25 (SO1) to output mode (PM25 = 0).
  Set P26 (SI1) to input mode (PM26 = 1). ★
- **In reception mode**
  Set P26 (SI1) in input mode (PM26 = 1).

Figure 10-2. Format of Serial Operation Mode Register 1 (CSIM1)

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM1	CSIE1	DIR1	ATE	LSCK1	0	0	SCL11	SCL10	FF63H	00H	R/W

CSIE1	Enables/disables operation of serial interface SIO1		
	Shift register operation	Serial counter	Port[Note 1]
0	Stops operation	Cleared	Port function
1	Enables operation	Enables count operation	Serial function + port function

DIR1	Specifies first bit of serial transfer data
0	MSB
1	LSB

ATE	Selects operating mode of serial interface SIO1
0	3-wire serial mode
1	3-wire serial mode with automatic transmit/receive function

LSCK1	Chip enable control of $\overline{\text{SCK1}}$ pin
0	$\overline{\text{SCK1}}$ is used as port (P27) when CSIE1 = 0. $\overline{\text{SCK1}}$ is used for clock output when CSIE1 = 1.
1	$\overline{\text{SCK1}}$ is fixed to high level when CSIE1 = 0. $\overline{\text{SCK1}}$ is used for clock output when CSIE1 = 1.

SCL11	SCL10	Selects serial clock of serial interface SIO1
0	0	External clock input to $\overline{\text{SCK1}}$ pin[Note 2]
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^3$ (625 kHz)
1	1	$f_X/2^4$ (313 kHz)

Notes 1. When CSIE1 = 0 (SIO1 operation stop status), SI1, SO1, $\overline{\text{SCK1}}$, and BUSY pins can be used as port pins.

2. When external clock input is selected by clearing SCL11 and SCL10 to 0, 0, clear bit 1 (BUSY1) of the automatic data transmit/receive control register (ADTC) to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

(2) Automatic data transmit/receive control register (ADTC)

This register sets automatic receive enable/disable, the operating mode, busy input enable/disable and displays automatic transmit/receive execution.

ADTC is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADTC to 00H.

Figure 10-3. Format of Automatic Data Transmit/Receive Control Register (ADTC)

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>	Address	After reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	0	BUSY1	BUSY0	FF64H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Busy input control
0	×	Not using busy input Note 2
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R

TRF	Status of automatic transmit/receive function Note 3
0	Detection of termination of automatic transmission/ reception (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection of automatic transmit/receive function
0	No error (This bit is set to 0 when data is written to SIO1)
1	Error occurred

R/W

ERCE	Error check control of automatic transmit/ receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode selection of automatic transmit/ receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive control of automatic transmit/receive function
0	Receive disable Note 4
1	Receive enable

Notes 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. When BUSY1 is reset to 0, P24 (CMOS I/O) is used even when bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is set to 1.

3. When an interrupt is acknowledged, interrupt request flag CSIIF1 is cleared. Therefore, use TRF, instead of CSIIF1, to identify the completion of automatic transmission/reception.

4. When RE is reset to 0, P26 (CMOS I/O) is used even if bit 7 (CSIE1) of CSIM1 is set to 1.

★ **Caution When bits 1 and 0 (SCL11, SCL10) of CSIM1 are set to 0 to select external clock input, set bit 1 (BUSY1) of ADTC to "0". (Handshake control cannot be performed when the external clock is input.)**

Remark ×: Don't care

(3) Automatic data transmit/receive interval specification register (ADTI)

This register sets the automatic data transmit/receive function data transfer interval.

ADTI is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADTI to 00H.

Figure 10-4. Format of Automatic Data Transmit/Receive Interval Specification Register (ADTI) (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF65H	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0 MHz, f_{SCK} = 1.25 MHz)Note 2	n
0	0	0	0	0	1.60 μs + 0.5/f_{SCK}	0
0	0	0	0	1		1
0	0	0	1	0	2.40 μs + 0.5/f_{SCK}	2
0	0	0	1	1	3.20 μs + 0.5/f_{SCK}	3
0	0	1	0	0	4.00 μs + 0.5/f_{SCK}	4
0	0	1	0	1	4.80 μs + 0.5/f_{SCK}	5
0	0	1	1	0	5.60 μs + 0.5/f_{SCK}	6
0	0	1	1	1	6.40 μs + 0.5/f_{SCK}	7
0	1	0	0	0	7.20 μs + 0.5/f_{SCK}	8
0	1	0	0	1	8.00 μs + 0.5/f_{SCK}	9
0	1	0	1	0	8.80 μs + 0.5/f_{SCK}	10
0	1	0	1	1	9.60 μs + 0.5/f_{SCK}	11
0	1	1	0	0	10.4 μs + 0.5/f_{SCK}	12
0	1	1	0	1	11.2 μs + 0.5/f_{SCK}	13
0	1	1	1	0	12.0 μs + 0.5/f_{SCK}	14
0	1	1	1	1	12.8 μs + 0.5/f_{SCK}	15

Notes 1. The interval time is $2/f_{SCK}$.

2. The data transfer interval time is found from the following expressions (n: Value set to ADTI0 to ADTI4).

<1> n = 0

$$\text{Interval time} = \frac{2}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

<2> n = 1 to 31

$$\text{Interval time} = \frac{n+1}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

Cautions 1. Do not write ADTI during operation of automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. When controlling the interval time of automatic transmit/receive data transfer by using ADTI, busy control is invalid. (Refer to 10.4.3 (4) (a) Busy control option.)

Remark f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Figure 10-4. Format of Automatic Data Transmit/Receive Interval Specification Register (ADTI) (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF65H	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0 MHz, f_{SCK} = 1.25 MHz)[Note]	n
1	0	0	0	0	13.6 μs + 0.5/f_{SCK}	16
1	0	0	0	1	14.4 μs + 0.5/f_{SCK}	17
1	0	0	1	0	15.2 μs + 0.5/f_{SCK}	18
1	0	0	1	1	16.0 μs + 0.5/f_{SCK}	19
1	0	1	0	0	16.8 μs + 0.5/f_{SCK}	20
1	0	1	0	1	17.6 μs + 0.5/f_{SCK}	21
1	0	1	1	0	18.4 μs + 0.5/f_{SCK}	22
1	0	1	1	1	19.2 μs + 0.5/f_{SCK}	23
1	1	0	0	0	20.0 μs + 0.5/f_{SCK}	24
1	1	0	0	1	20.8 μs + 0.5/f_{SCK}	25
1	1	0	1	0	21.6 μs + 0.5/f_{SCK}	26
1	1	0	1	1	22.4 μs + 0.5/f_{SCK}	27
1	1	1	0	0	23.2 μs + 0.5/f_{SCK}	28
1	1	1	0	1	24.0 μs + 0.5/f_{SCK}	29
1	1	1	1	0	24.8 μs + 0.5/f_{SCK}	30
1	1	1	1	1	25.6 μs + 0.5/f_{SCK}	31

Note The data transfer interval time is found from the following expressions (n: Value set to ADTI0 to ADTI4).

<1> n = 0

$$\text{Interval time} = \frac{2}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

<2> n = 1 to 31

$$\text{Interval time} = \frac{n+1}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

Cautions 1. Do not write ADTI during operation of automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. When controlling the interval time of automatic transmit/receive data transfer by using ADTI, busy control is invalid. (Refer to 10.4.3 (4) (a) Busy control option.)

Remark f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

10.4 Operations of Serial Interface SIO1

The following three operating modes are available to serial interface SIO1.

- Operation stop mode
- 3-wire serial mode
- 3-wire serial mode with automatic transmit/receive function

10.4.1 Operation stop mode

Serial transfer is not carried out in the operation stop mode. Serial shift register 1 (SIO1) does not carry out shift operation either, and thus it can be used as an ordinary 8-bit register.

In the operation stop mode, the SI1, SO1, $\overline{SCK1}$, and BUSY pins can be used as ordinary ports.

(1) Register setting

The operation stop mode is set by serial operation mode register 1 (CSIM1).

CSIM1 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM1 to 00H.

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM1	CSIE1	DIR1	ATE	LSCK1	0	0	SCL11	SCL10	FF63H	00H	R/W

CSIE1	Enables/Disables Operation of Serial Interface SIO1		
	Shift register operation	Serial counter	Port[Note]
0	Stops operation	Cleared	Port function

Note When CSIE1 = 0 (SIO1 operation stop status), SI1, SO1, $\overline{SCK1}$, and BUSY pins can be used as port pins.

10.4.2 3-wire serial mode operation

The 3-wire serial mode is valid for connection of peripheral IC units and display controllers which incorporate a conventional synchronous serial interface.

Communication is carried out with three lines of serial clock ($\overline{SCK1}$), serial output (SO1) and serial input (SI1).

(1) Register setting

The 3-wire serial mode is set by serial operation mode register 1 (CSIM1).

CSIM1 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM1 to 00H.

Caution Set the port mode register (PMxx) in the 3-wire serial mode as follows. Set the output latch to 0.

<Serial clock setting>

- **In the case of serial clock output (master transmission or master reception):**
  Set P27 ($\overline{SCK1}$) to the output mode (PM27 = 0).
- **In the case of serial clock input (slave transmission or slave reception):**
  Set P27 to input mode (PM27 = 1).

<Operation mode setting>

- **In transmission or transmission/reception mode:**
  Set P25 (SO1) to output mode (PM25 = 0).
  Set P26 (SI1) to input mode (PM26 = 1). ★
- **In reception mode**
  Set P26 (SI1) in input mode (PM26 = 1).

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM1	CSIE1	DIR1	ATE	LSCK1	0	0	SCL11	SCL10	FF63H	00H	R/W

CSIE1	Enables/disables operation of serial interface SIO1		
	Shift register operation	Serial counter	Port[Note 1]
0	Stops operation	Cleared	Port function
1	Enables operation	Enables count operation	Serial function + port function

DIR1	Specifies first bit of serial transfer data
0	MSB
1	LSB

ATE	Selects operating mode of serial interface SIO1
0	3-wire serial mode
1	3-wire serial mode with automatic transmit/receive function

LSCK1	Chip enable control of $\overline{\text{SCK1}}$ pin
0	$\overline{\text{SCK1}}$ is used as port (P27) when CSIE1 = 0. $\overline{\text{SCK1}}$ is used for clock output when CSIE1 = 1.
1	$\overline{\text{SCK1}}$ is fixed to high level when CSIE1 = 0. $\overline{\text{SCK1}}$ is used for clock output when CSIE1 = 1.

SCL11	SCL10	Selects serial clock of serial interface SIO1
0	0	External clock input to $\overline{\text{SCK1}}$ pin[Note 2]
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^3$ (625 kHz)
1	1	$f_X/2^4$ (313 kHz)

Notes 1. When CSIE1 = 0 (SIO1 operation stop status), SI1, SO1, $\overline{\text{SCK1}}$, and BUSY pins can be used as port pins.

2. When external clock input is selected by clearing SCL11 and SCL10 to 0, 0, clear bit 1 (BUSY1) of the automatic data transmit/receive control register (ADTC) to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

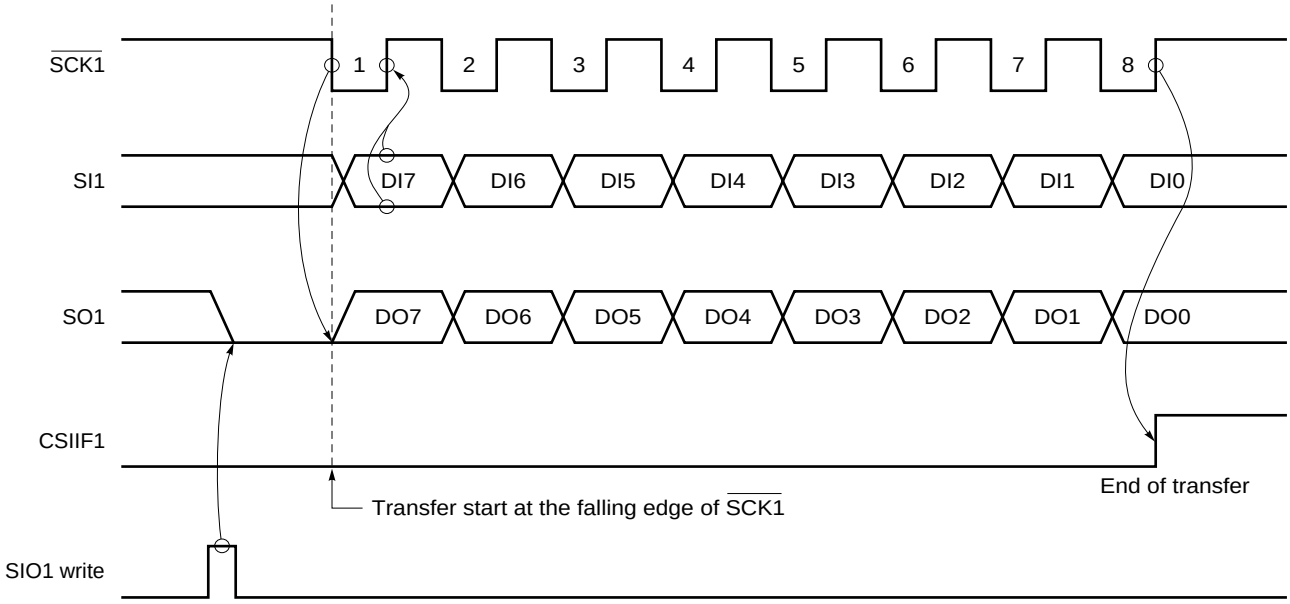
(2) Communication operation

The 3-wire serial mode is used for data transmission/reception in 8-bit units. Bit-wise data transmission/reception is carried out in synchronization with the serial clock.

Shift operation of serial shift register 1 (SIO1) is carried out at the falling edge of the serial clock ($\overline{SCK1}$). The transmit data is held in the SO1 latch and is output from the SO1 pin. The receive data input to the SI1 pin is latched into SIO1 at the rising edge of $\overline{SCK1}$.

Upon termination of 8-bit transfer, the SIO1 operation stops automatically and the interrupt request flag (CSIIF1) is set.

Figure 10-5. 3-Wire Serial Mode Timings



Caution SO1 pin becomes low level by SIO1 write.

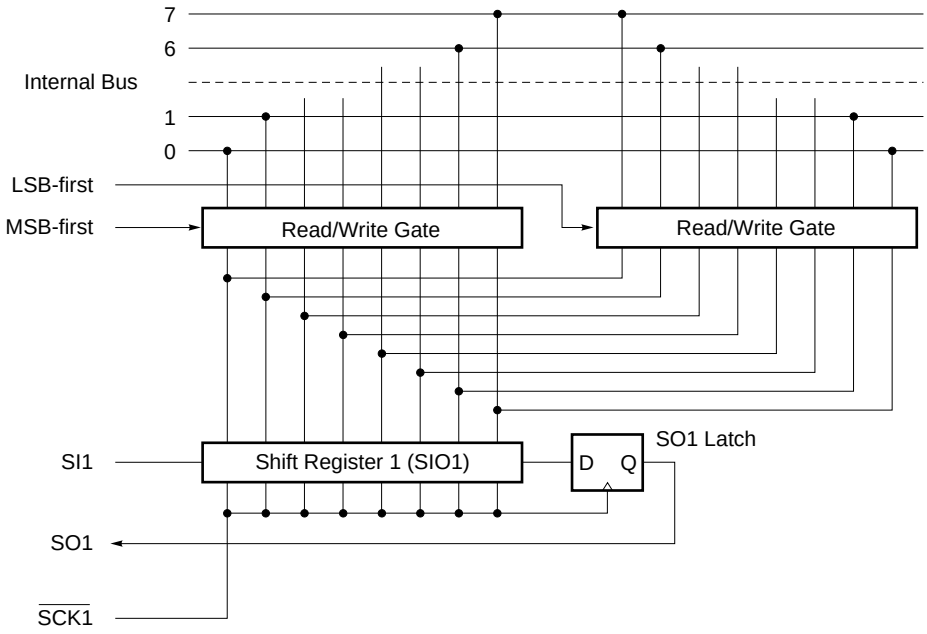
(3) MSB/LSB switching as the start bit

The 3-wire serial mode enables to select transfer to start from MSB or LSB.

Figure 10-6 shows the configuration of serial shift register 1 (SIO1) and internal bus. As shown in the figure, MSB/LSB can be read/written in reverse form.

MSB/LSB switching as the start bit can be specified with bit 6 (DIR1) of serial operation mode register 1 (CSIM1).

Figure 10-6. Circuit of Switching in Transfer Bit Order



Start bit switching is realized by switching the bit order for data write to SIO1. The SIO1 shift order remains unchanged.

Thus, switching between MSB-first and LSB-first must be performed before writing data to the shift register.

(4) Transfer start

Serial transfer is started by setting transfer data to serial shift register 1 (SIO1) when the following two conditions are satisfied.

- Serial interface SIO1 operation control bit (bit 7 (CSIE1) of serial operation mode register 1 (CSIM1)) = 1
- Internal serial clock is stopped or $\overline{\text{SCK1}}$ is a high level after 8-bit serial transfer.

Caution Transfer does not start if CSIE1 is set to "1" after data write to SIO1.

Upon termination of 8-bit transfer, serial transfer automatically stops and the interrupt request flag (CSIIF1) is set.

10.4.3 3-wire serial mode with automatic transmit/receive function

This 3-wire serial mode is used for transmission/reception of a maximum of 32-byte data without the use of software. Once transfer is started, the data prestored in the RAM can be transmitted by the set number of bytes, and data can be received and stored in the RAM by the set number of bytes.

Handshake signal (BUSY) are supported by hardware to transmit/receive data continuously. OSD (On Screen Display) LSI and peripheral LSI including LCD controller/driver can be connected without difficulty.

(1) Register setting

The 3-wire serial mode with automatic transmit/receive function is set with serial operation mode register 1 (CSIM1), the automatic data transmit/receive control register (ADTC) and the automatic data transmit/receive interval specification register (ADTI).

(a) Serial operation mode register 1 (CSIM1)

CSIM1 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM1 to 00H.

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After reset	R/W
CSIM1	CSIE1	DIR1	ATE	LSCK1	0	0	SCL11	SCL10	FF63H	00H	R/W

CSIE1	Enables/disables operation of serial interface SIO1		
	Shift register operation	Serial counter	Port[Note 1]
0	Stops operation	Cleared	Port function
1	Enables operation	Enables count operation	Serial function + port function

DIR1	Specifies first bit of serial transfer data
0	MSB
1	LSB

ATE	Selects operating mode of serial interface SIO1
0	3-wire serial mode
1	3-wire serial mode with automatic transmit/receive function

LSCK1	Chip enable control of $\overline{SCK1}$ pin
0	$\overline{SCK1}$ is used as port (P27) when CSIE1 = 0. $\overline{SCK1}$ is used for clock output when CSIE1 = 1.
1	$\overline{SCK1}$ is fixed to high level when CSIE1 = 0. $\overline{SCK1}$ is used for clock output when CSIE1 = 1.

SCL11	SCL10	Selects serial clock of serial interface SIO1
0	0	External clock input to $\overline{SCK1}$ pin[Note 2]
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^3$ (625 kHz)
1	1	$f_X/2^4$ (313 kHz)

Notes 1. When CSIE1 = 0 (SIO1 operation stop status), SI1, SO1, $\overline{SCK1}$, and BUSY pins can be used as port pins.

2. When external clock input is selected by clearing SCL11 and SCL10 to 0, 0, clear bit 1 (BUSY1) of the automatic data transmit/receive control register (ADTC) to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. ( ): f_X = 5.0 MHz

(b) Automatic data transmit/receive control register (ADTC)

ADTC is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears ADTC to 00H.

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>	Address	After reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	0	BUSY1	BUSY0	FF64H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Busy input control
0	×	Not using busy input Note 2
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R

TRF	Status of automatic transmit/receive function Note 3
0	Detection of termination of automatic transmission/ reception (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection of automatic transmit/receive function
0	No error (This bit is set to 0 when data is written to SIO1)
1	Error occurred

R/W

ERCE	Error check control of automatic transmit/ receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode selection of automatic transmit/ receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive control of automatic transmit/receive function
0	Receive disable Note 4
1	Receive enable

Notes 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. When BUSY1 is reset to 0, P24 (CMOS I/O) is used even when bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is set to 1.

3. When an interrupt is acknowledged, interrupt request flag CSIIF1 is cleared. Therefore, use TRF, instead of CSIIF1, to identify the completion of automatic transmission/reception.

4. When RE is reset to 0, P26 (CMOS I/O) is used even when bit 7 (CSIE1) of CSIM1 is set to 1.

Caution When bits 1 and 0 (SCL11, SCL10) of CSIM1 are set to 0 to select external clock input, set bit 1 (BUSY1) of ADTC to "0". (Handshake control cannot be performed when the external clock is input.)

Remark ×: Don't care

(c) Automatic data transmit/receive interval specification register (ADTI)

This register sets the automatic data transmit/receive function data transfer interval.

ADTI is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADTI to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF65H	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0 MHz, f_{SCK} = 1.25 MHz)Note 2	n
0	0	0	0	0	1.60 μs + 0.5/f_{SCK}	0
0	0	0	0	1		1
0	0	0	1	0	2.40 μs + 0.5/f_{SCK}	2
0	0	0	1	1	3.20 μs + 0.5/f_{SCK}	3
0	0	1	0	0	4.00 μs + 0.5/f_{SCK}	4
0	0	1	0	1	4.80 μs + 0.5/f_{SCK}	5
0	0	1	1	0	5.60 μs + 0.5/f_{SCK}	6
0	0	1	1	1	6.40 μs + 0.5/f_{SCK}	7
0	1	0	0	0	7.20 μs + 0.5/f_{SCK}	8
0	1	0	0	1	8.00 μs + 0.5/f_{SCK}	9
0	1	0	1	0	8.80 μs + 0.5/f_{SCK}	10
0	1	0	1	1	9.60 μs + 0.5/f_{SCK}	11
0	1	1	0	0	10.4 μs + 0.5/f_{SCK}	12
0	1	1	0	1	11.2 μs + 0.5/f_{SCK}	13
0	1	1	1	0	12.0 μs + 0.5/f_{SCK}	14
0	1	1	1	1	12.8 μs + 0.5/f_{SCK}	15

Notes 1. The interval time is 2/f_{SCK}.

2. The data transfer interval time is found from the following expressions (n: Value set to ADTI0 to ADTI4).

<1> n = 0

$$\text{Interval time} = \frac{2}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

<2> n = 1 to 31

$$\text{Interval time} = \frac{n+1}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

Cautions 1. Do not write ADTI during operation of automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. When controlling the interval time of automatic transmit/receive data transfer by using ADTI, busy control is invalid. (Refer to 10.4.3 (4) (a) Busy control option.)

Remark f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF65H	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0 MHz, f_{SCK} = 1.25 MHz)Note	n
1	0	0	0	0	13.6 μs + 0.5/f_{SCK}	16
1	0	0	0	1	14.4 μs + 0.5/f_{SCK}	17
1	0	0	1	0	15.2 μs + 0.5/f_{SCK}	18
1	0	0	1	1	16.0 μs + 0.5/f_{SCK}	19
1	0	1	0	0	16.8 μs + 0.5/f_{SCK}	20
1	0	1	0	1	17.6 μs + 0.5/f_{SCK}	21
1	0	1	1	0	18.4 μs + 0.5/f_{SCK}	22
1	0	1	1	1	19.2 μs + 0.5/f_{SCK}	23
1	1	0	0	0	20.0 μs + 0.5/f_{SCK}	24
1	1	0	0	1	20.8 μs + 0.5/f_{SCK}	25
1	1	0	1	0	21.6 μs + 0.5/f_{SCK}	26
1	1	0	1	1	22.4 μs + 0.5/f_{SCK}	27
1	1	1	0	0	23.2 μs + 0.5/f_{SCK}	28
1	1	1	0	1	24.0 μs + 0.5/f_{SCK}	29
1	1	1	1	0	24.8 μs + 0.5/f_{SCK}	30
1	1	1	1	1	25.6 μs + 0.5/f_{SCK}	31

Note The data transfer interval time is found from the following expressions (n: Value set to ADTI0 to ADTI4).

<1> n = 0

$$\text{Interval time} = \frac{2}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

<2> n = 1 to 31

$$\text{Interval time} = \frac{n+1}{f_{SCK}} + \frac{0.5}{f_{SCK}}$$

Cautions 1. Do not write ADTI during operation of automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. When controlling the interval time of automatic transmit/receive data transfer by using ADTI, busy control is invalid. (Refer to 10.4.3 (4) (a) Busy control option.)

Remark f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

(2) Automatic transmit/receive data setting

(a) Transmit data setting

★ <1> Write transmit data from the least significant address F9C0H of buffer RAM (up to F9DFH at maximum). The transmit data should be in the order from higher address to lower address.
<2> Set to the automatic data transmit/receive address pointer (ADTP) the value obtained by subtracting 1 from the number of transmit data bytes.

(b) Automatic transmit/receive mode setting

<1> Set bit 7 (CSIE1) and bit 5 (ATE) of serial operation mode register 1 (CSIM1) to 1.
<2> Set bit 7 (RE) of the automatic data transmit/receive control register (ADTC) to 1.
<3> Set a data transmit/receive interval in the automatic data transmit/receive interval specification register (ADTI).
<4> Write any value to serial I/O shift register 1 (SIO1) (transfer start trigger).

Caution Writing any value to SIO1 orders the start of automatic transmit/receive operation and the written value has no meaning.

The following operations are automatically carried out when (a) and (b) are carried out.

- After the buffer RAM data specified with ADTP is transferred to SIO1, transmission is carried out (start of automatic transmission/reception).
- The received data is written to the buffer RAM address specified with ADTP.
- ADTP is decremented and the next data transmission/reception is carried out. Data transmission/ ★ reception continues until the ADTP decremental output becomes 00H and address F9C0H data is output (end of automatic transmission/reception).
- When automatic transmission/reception is terminated, bit 3 (TRF) of ADTC is cleared to 0.

(3) Communication operation

(a) Basic transmit/receive mode

This transmit/receive mode is the same as the 3-wire serial mode in which specified number of data are transmitted/received in 8-bit units.

Serial transfer is started when any data is written to serial shift register 1 (SIO1) while bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is set to 1.

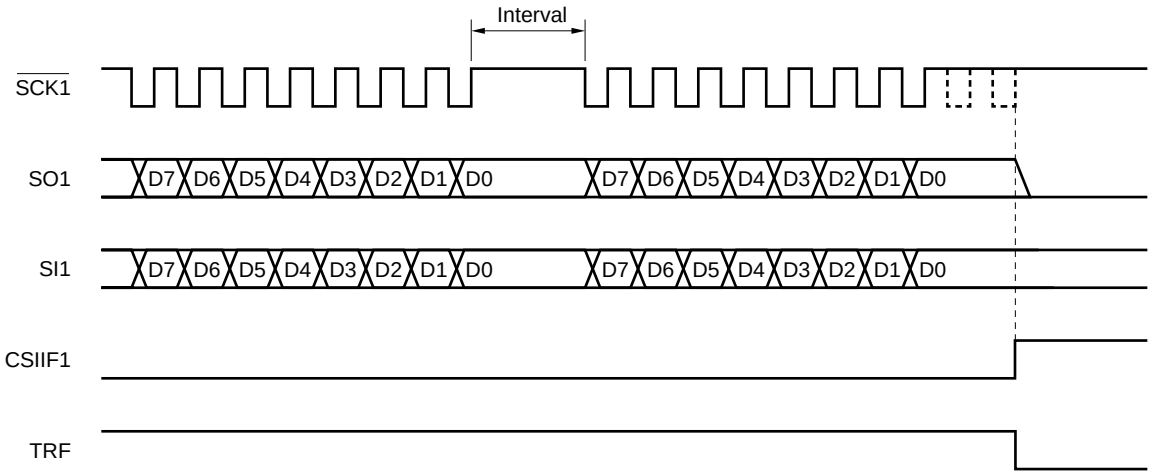
★ In the master mode, the interrupt request flag (CSIIF1) is set to “1” and bit 3 (TRF) of the automatic data transmit/receive control register (ADTC) is cleared to “0” in synchronization with the rising edge of the serial clock two clocks after the last byte has been transmitted. In the slave mode, CSIIF1 is set to “1” and TRF is cleared to “0” in synchronization with the rising clock of the serial clock after the last byte has been transmitted. Upon interrupt acknowledgment, CSIIF1 is cleared, so check for the end of automatic transmission/reception using TRF instead of CSIIF1.

If busy control is not executed, the P24/BUSY pin can be used as normal I/O port.

Figure 10-7 shows the basic transmit/receive mode operation timings, and Figure 10-8 shows the operation flowchart.

Figure 10-9 shows buffer RAM operation at 6-byte transmission.

★ **Figure 10-7. Basic Transmit/Receive Mode Operation Timings (Master Mode)**



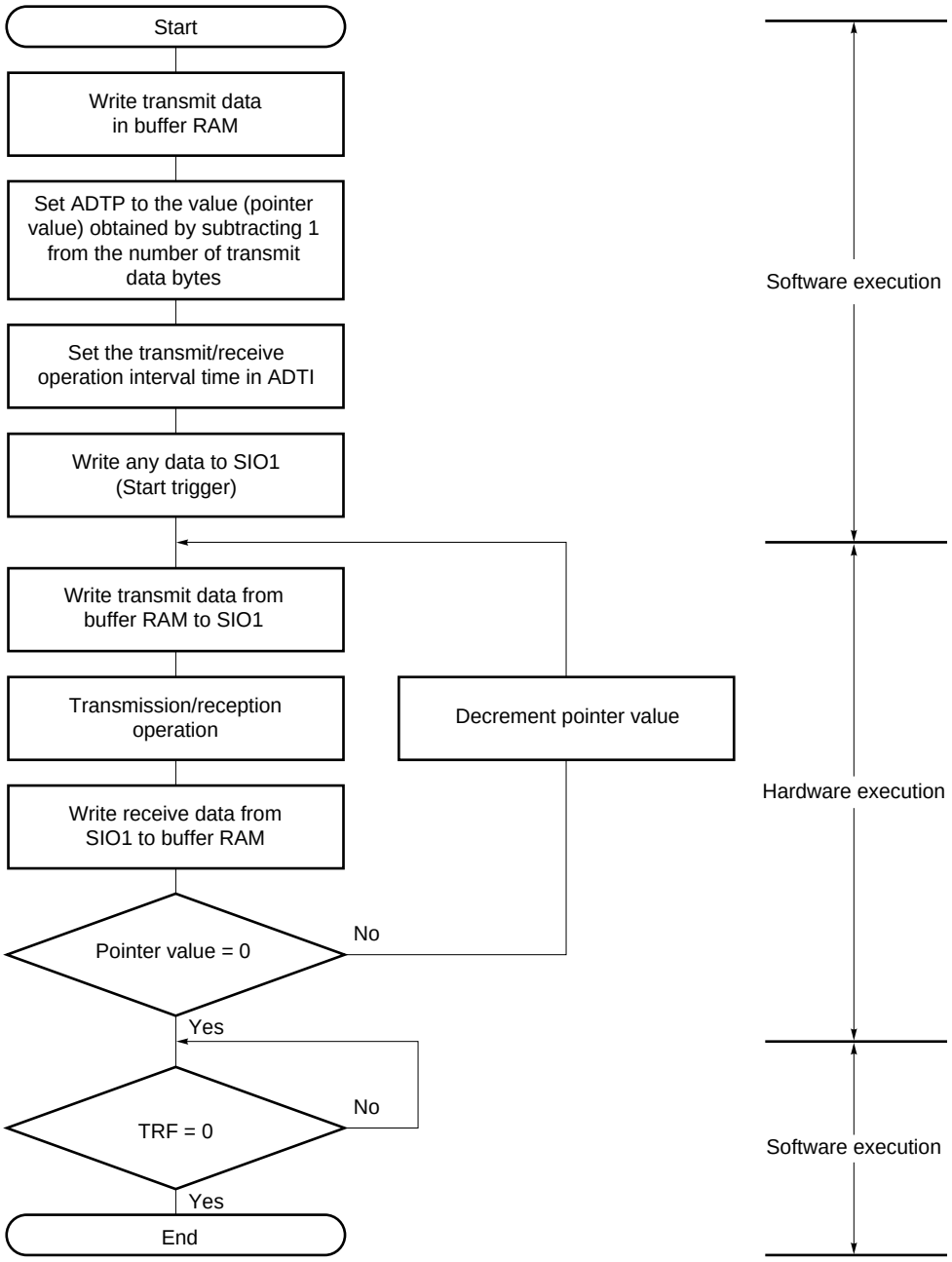
Cautions 1. Because, in the basic transmit/receive mode, the automatic transmit/receive function writes/reads data to/from the buffer RAM after 1-byte transmission/reception, an interval is inserted till the next transmission/reception. As the buffer RAM write/read is performed at the same time as CPU processing, the maximum interval is dependent upon CPU processing and the value of the automatic data transmit/receive interval specification register (ADTI) (refer to (6) Automatic data transmit/receive interval).

2. When TRF is cleared, the SO1 pin becomes low level.

Remark CSIIF1: Interrupt request flag

TRF: Bit 3 of automatic data transmit/receive control register (ADTC)

Figure 10-8. Basic Transmit/Receive Mode Flowchart



ADTP: Automatic data transmit/receive address pointer
ADTI: Automatic data transmit/receive interval specification register
SIO1: Serial shift register 1
TRF: Bit 3 of automatic data transmit/receive control register (ADTC)

In 6-byte transmission/reception (bit 6 (ARLD) and bit 7 (RE) of the automatic data transmit/receive control register (ADTC) = 0, and 1, respectively) in basic transmit/receive mode, buffer RAM operates as follows.

(i) Before transmission/reception (refer to Figure 10-9 (a))

After any data has been written to SIO1 (start trigger: this data is not transferred), transmit data 1 (T1) is transferred from the buffer RAM to SIO1. When transmission of the first byte is complete, receive data 1 (R1) is transferred from SIO1 to the buffer RAM, and automatic data transmit/receive address pointer (ADTP) is decremented. Then transmit data 2 (T2) is transferred from the buffer RAM to SIO1.

(ii) 4th byte transmit/receive point (refer to Figure 10-9 (b))

Transmission/reception of the third byte is complete, and transmit data 4 (T4) is transferred from the buffer RAM to SIO1. When transmission of the fourth byte is completed, receive data 4 (R4) is transferred from SIO1 to the buffer RAM, and ADTP is decremented.

(iii) Completion of transmission/reception (refer to Figure 10-9 (c))

When transmission of the sixth byte is complete, receive data 6 (R6) is transferred from SIO1 to the buffer RAM, and the interrupt request flag (CSIIF1) is set (INTCSI1 generation).

Figure 10-9. Buffer RAM Operation in 6-Byte Transmission/Reception (in Basic Transmit/Receive Mode) (1/2)

(a) Before transmission/reception

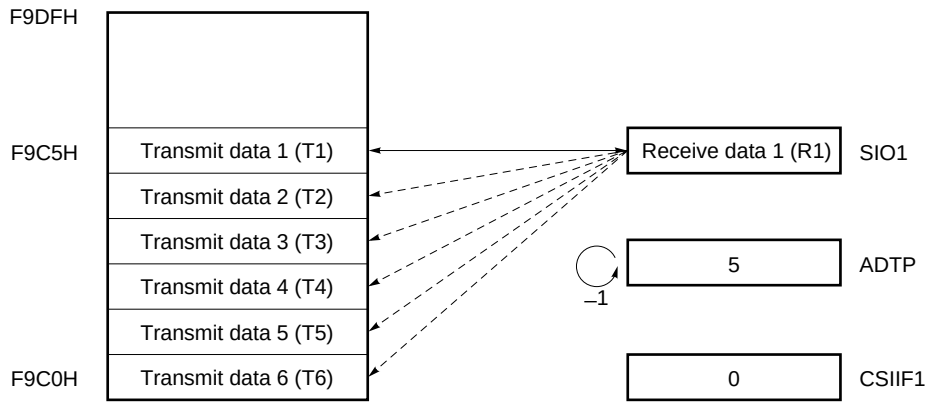
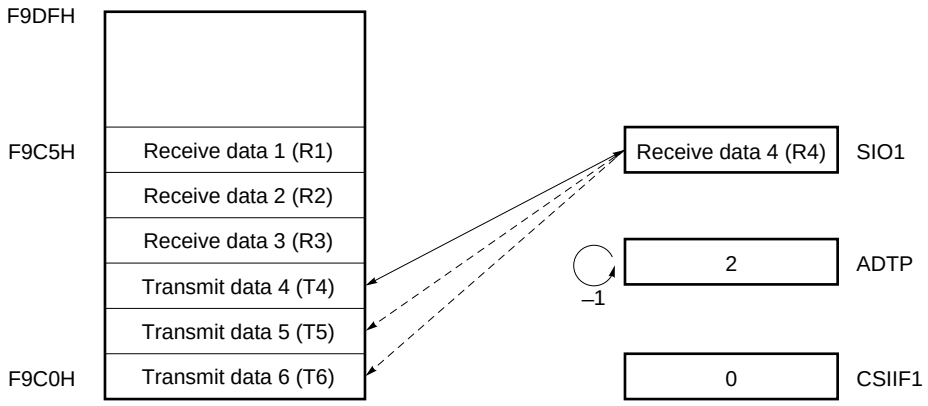
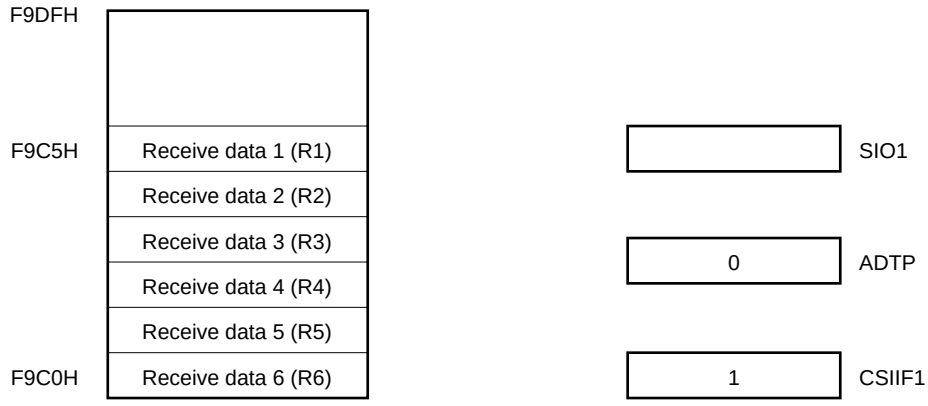


Figure 10-9. Buffer RAM Operation in 6-Byte Transmission/Reception (in Basic Transmit/Receive Mode) (2/2)

(b) 4th byte transmission/reception



(c) Completion of transmission/reception



(b) Basic transmit mode

In this mode, the specified number of 8-bit unit data are transmitted.

Serial transfer is started when any data is written to serial shift register 1 (SIO1) while bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is set to 1, and bit 7 (RE) of the automatic data transmit/receive control register (ADTC) is set to 0.

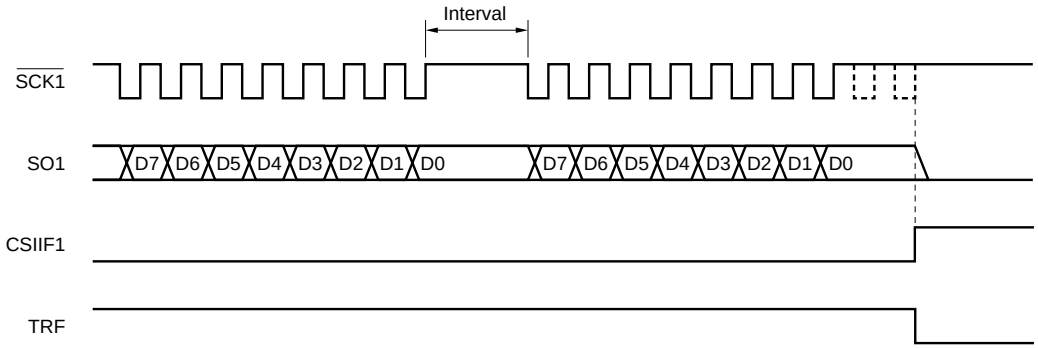
★ In the master mode, the interrupt request flag (CSIIF1) is set to “1” and bit 3 (TRF) of the automatic data transmit/receive control register (ADTC) is cleared to “0” in synchronization with the rising edge of the serial clock two clocks after the last byte has been transmitted. In the slave mode, CSIIF1 is set to “1” and TRF is cleared to “0” in synchronization with the rising clock of the serial clock after the last byte has been transmitted. Upon interrupt acknowledgment, CSIIF1 is cleared, so check for the end of automatic transmission/reception using TRF instead of CSIIF1.

If receive operation, busy control is not executed, the P26/SI1 and P24/BUSY pins can be used as normal I/O ports.

Figure 10-10 shows the basic transmit mode operation timings, and Figure 10-11 shows the operation flowchart.

Figure 10-12 shows buffer RAM operation when repeatedly transmit 6 bytes.

★ **Figure 10-10. Basic Transmit Mode Operation Timings (Master Mode)**



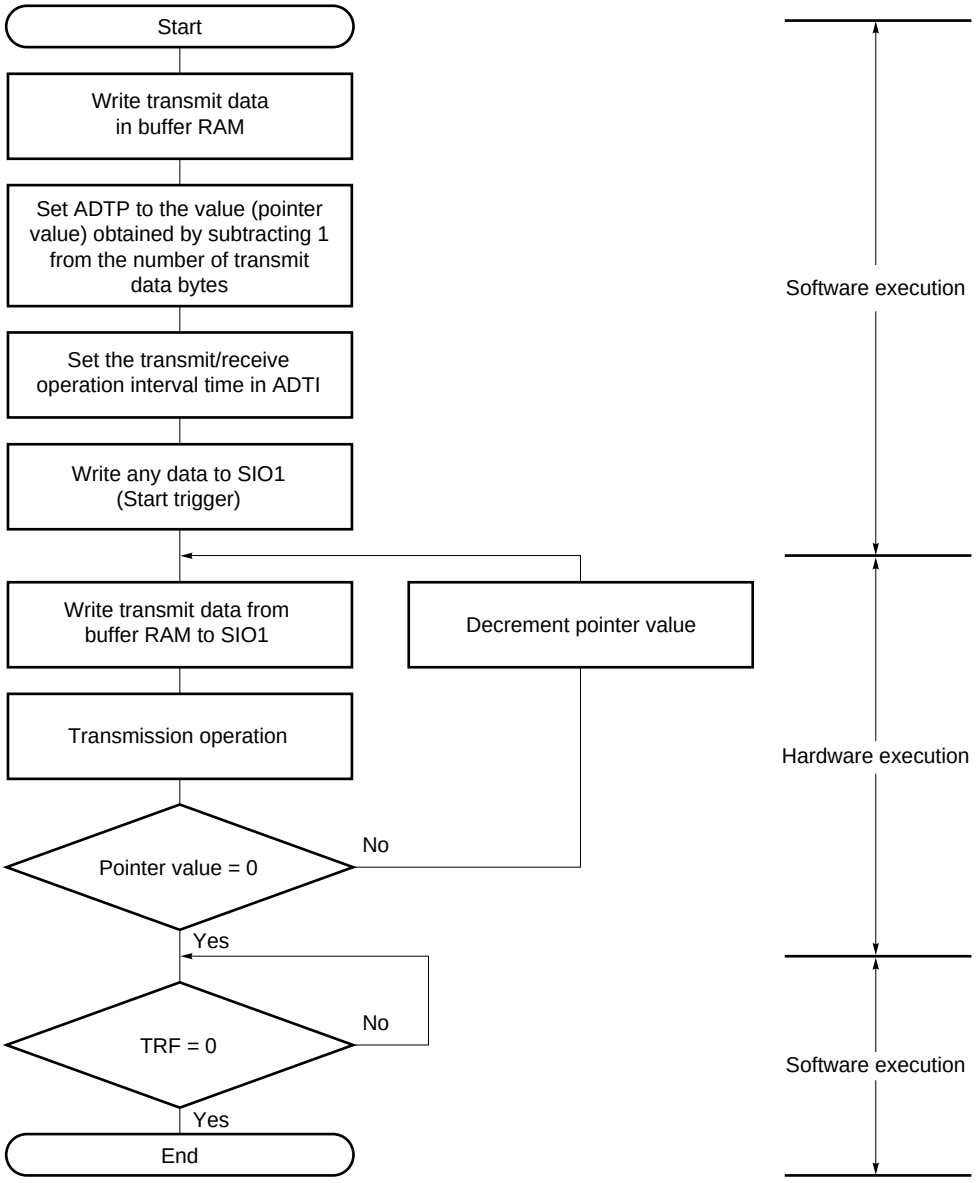
Cautions 1. Because, in the basic transmit mode, the automatic transmit/receive function reads data from the buffer RAM after 1-byte transmission, an interval is inserted till the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the maximum interval is dependent upon CPU processing and the value of the automatic data transmit/receive interval specification register (ADTI) (refer to (6) Automatic data transmit/receive interval).

2. When TRF is cleared, the SO1 pin becomes low level.

Remark CSIIF1: Interrupt request flag

TRF: Bit 3 of automatic data transmit/receive control register (ADTC)

Figure 10-11. Basic Transmit Mode Flowchart



ADTP: Automatic data transmit/receive address pointer
ADTI: Automatic data transmit/receive interval specification register
SIO1: Serial shift register 1
TRF: Bit 3 of automatic data transmit/receive control register (ADTC)

In 6-byte transmission (bit 6 (ARLD) and bit 7 (RE) of the automatic data transmit/receive control register (ADTC) are 0) in basic transmit mode, buffer RAM operates as follows.

(i) Before transmission (refer to Figure 10-12 (a))

After any data has been written to SIO1 (start trigger: this data is not transferred), transmit data 1 (T1) is transferred from the buffer RAM to SIO1. When transmission of the first byte is complete, ADTP is decremented. Then transmit data 2 (T2) is transferred from the buffer RAM to SIO1.

(ii) 4th byte transmission point (refer to Figure 10-12 (b))

Transmission of the third byte is complete, and transmit data 4 (T4) is transferred from the buffer RAM to SIO1. When transmission of the fourth byte is complete, ADTP is decremented.

(iii) Completion of transmission/reception (refer to Figure 10-12 (c))

When transmission of the sixth byte is complete, the interrupt request flag (CSIIF1) is set (INTCSI1 generation).

Figure 10-12. Buffer RAM Operation in 6-Byte Transmission (in Basic Transmit Mode) (1/2)

(a) Before transmission

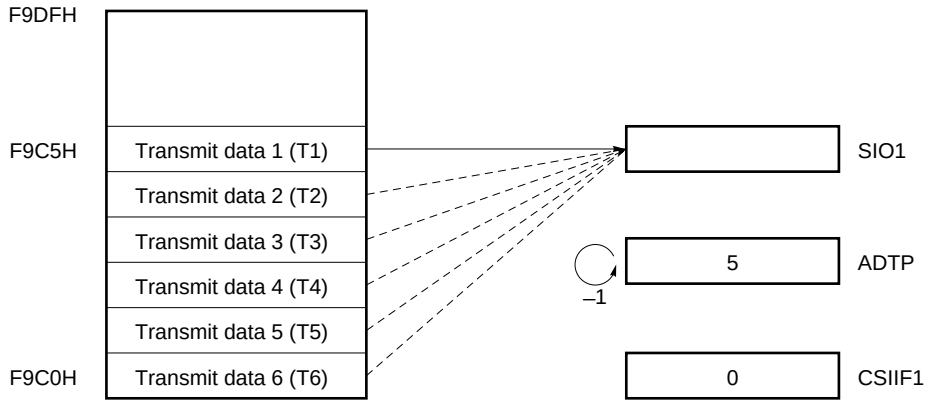
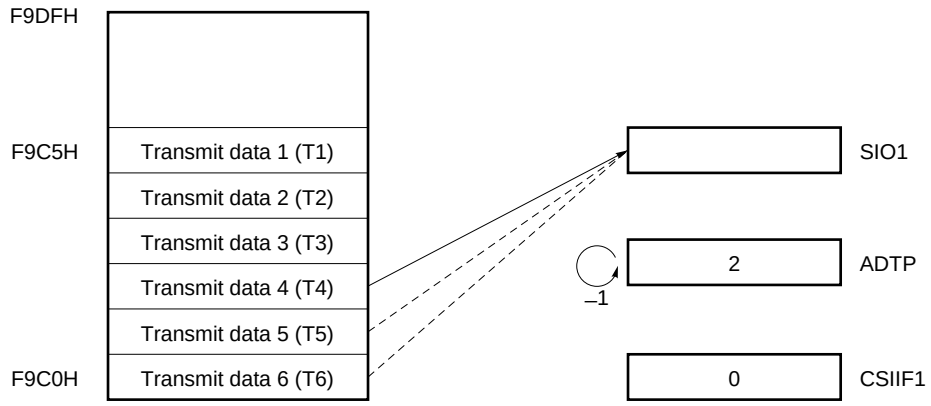
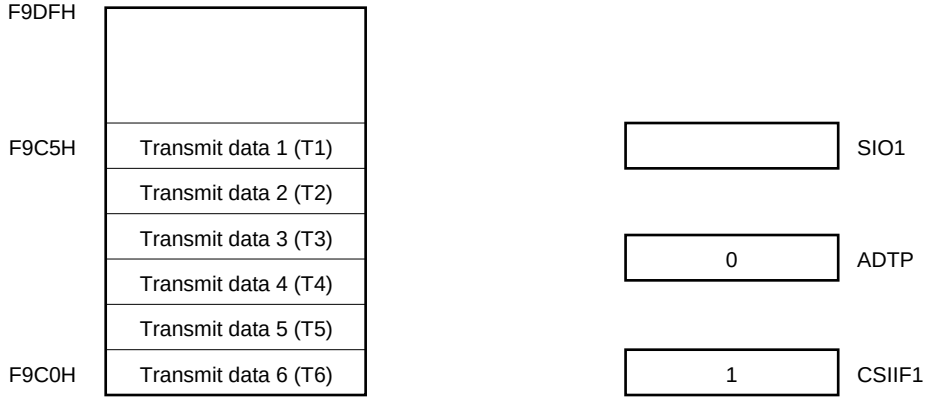


Figure 10-12. Buffer RAM Operation in 6-Byte Transmission (in Basic Transmit Mode) (2/2)

(b) 4th byte transmission point



(c) Completion of transmission/reception



(c) Repeat transmit mode

In this mode, data stored in the buffer RAM is transmitted repeatedly.

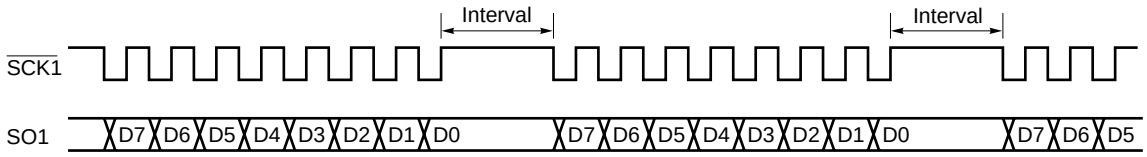
Serial transfer is started by writing any data to serial shift register 1 (SIO1) when bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is set 1, and bit 7 (RE) of the automatic data transmit/receive control register (ADTC) is set to 0.

Unlike the basic transmission mode, after the last byte (data in address F9C0H) has been transmitted, the interrupt request flag (CSIIF1) is not set, the value at the time when the transmission was started is set in the automatic data transmit/receive address pointer (ADTP) again, and the buffer RAM contents are transmitted again.

When a reception operation, busy control is not performed, the P26/SI1 and P24/BUSY pins can be used as ordinary I/O ports.

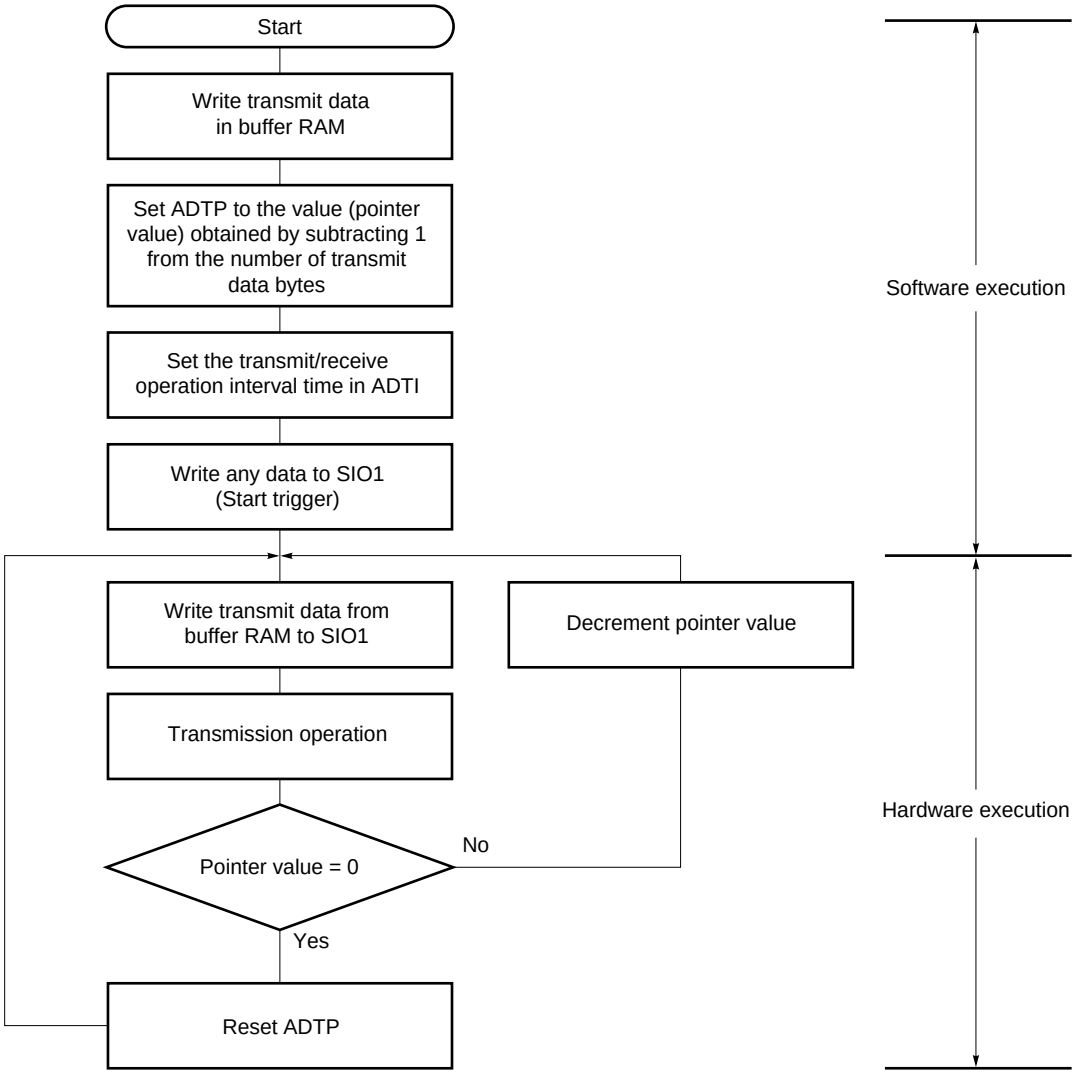
The repeat transmit mode operation timing is shown in Figure 10-13, and the operation flowchart in Figure 10-14.

Figure 10-13. Repeat Transmit Mode Operation Timing



Caution Since, in the repeat transmit mode, a read is performed on the buffer RAM after the transmission of one byte, the interval is included in the period up to the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the maximum interval is dependent upon the CPU operation and the value of the automatic data transmit/receive interval specification register (ADTI) (refer to (6) Automatic data transmit/receive interval).

Figure 10-14. Repeat Transmit Mode Flowchart



ADTP: Automatic data transmit/receive address pointer
ADTI: Automatic data transmit/receive interval specification register
SIO1: Serial shift register 1

In 6-byte transmission (bit 6 (ARLD) and bit 7 (RE) of the automatic data transmit/receive control register (ADTC) are 1 and 0, respectively) in repeat transmit mode, buffer RAM operates as follows.

(i) Before transmission (refer to Figure 10-15 (a))

After any data has been written to SIO1 (start trigger: this data is not transferred), transmit data 1 (T1) is transferred from the buffer RAM to SIO1. When transmission of the first byte is complete, ADTP is decremented. Then transmit data 2 (T2) is transferred from the buffer RAM to SIO1.

(ii) Upon completion of transmission of 6 bytes (refer to Figure 10-15 (b))

When transmission of the sixth byte is complete, the interrupt request flag (CSIIF1) is not set. The previous pointer value is assigned to the ADTP.

(iii) 7th byte transmission point (refer to Figure 10-15 (c))

Transmit data 1 (T1) is transferred from the buffer RAM to SIO1 again. When transmission of the first byte is complete, ADTP is decremented. Then transmit data 2 (T2) is transferred from the buffer RAM to SIO1.

Figure 10-15. Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmit Mode) (1/2)

(a) Before transmission

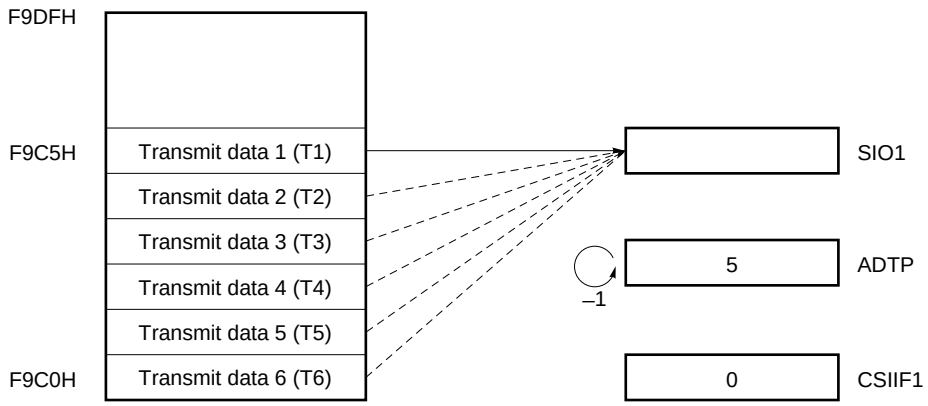
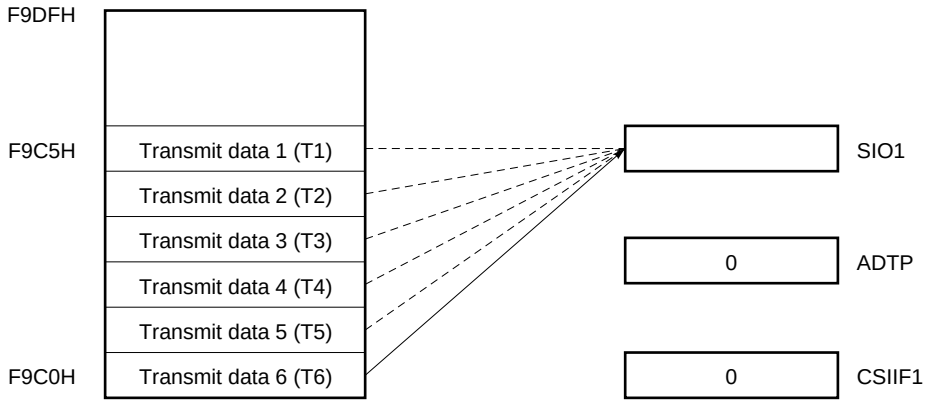
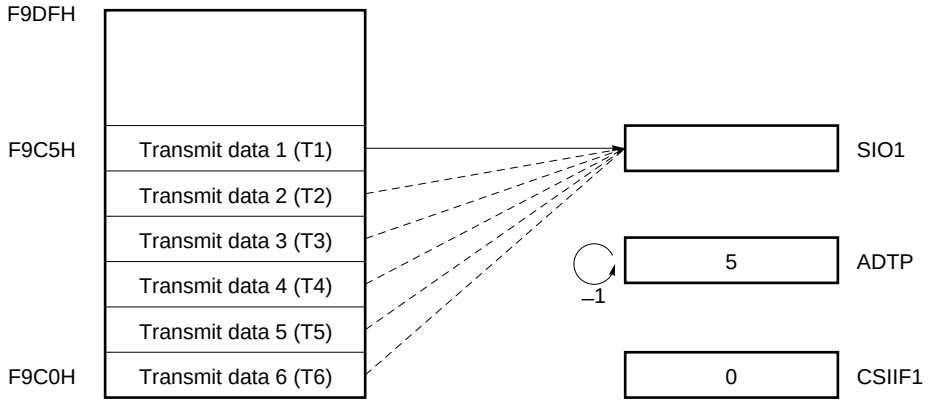


Figure 10-15. Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmit Mode) (2/2)

(b) Upon completion of transmission of 6 bytes



(c) 7th byte transmission point



(d) Automatic transmission/reception suspension and restart

Automatic transmission/reception can be temporarily suspended by setting bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) to 0.

If during 8-bit data transfer, the transmission/reception is not suspended if bit 7 (CSIE1) is set to 0. It is suspended upon completion of 8-bit data transfer.

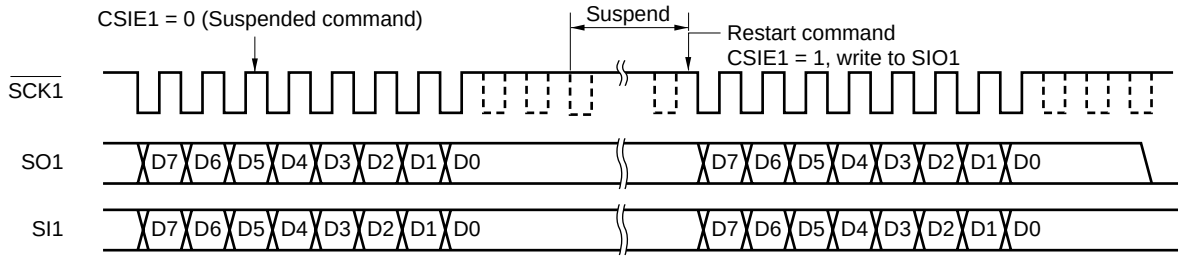
When suspended, bit 3 (TRF) of the automatic data transmit/receive control register (ADTC) is set to 0 after transfer of the 8th bit, and all the port pins used with the serial interface pins for dual function (P24/BUSY, P25/SO1, P26/SI1, P27/$\overline{\text{SCK1}}$) are set to the port mode.

During restart of transmission/reception, remaining data can be transferred by setting CSIE1 to 1 and writing any data to serial shift register 1 (SIO1).

Cautions 1. If the HALT instruction is executed during automatic transmission/reception, transfer is suspended and the HALT mode is set if during 8-bit data transfer.

2. When suspending automatic transmission/reception, do not change the operating mode to 3-wire serial mode while TRF = 1.

Figure 10-16. Automatic Transmission/Reception Suspension and Restart



CSIE1: Bit 7 of serial operation mode register 1 (CSIM1)

(4) Synchronization control

Busy control is a function to synchronize transmission/reception between the master device and a slave device. By using these functions, a shift in bits being transmitted or received can be detected.

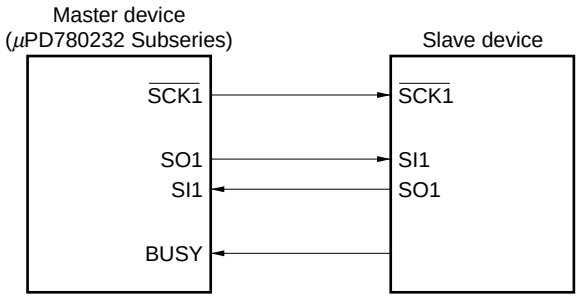
(a) Busy control option

Busy control is a function to keep the serial transmission/reception by the master device waiting while the busy signal output by a slave device to the master is active.
When using this busy control option, the following conditions must be satisfied.

- Bit 5 (ATE) of serial operation mode register 1 (CSIM1) is set to 1.
- Bit 1 (BUSY1) of the automatic data transmit/receive control register (ADTC) is set to 1.

Figure 10-17 shows the system configuration of the master device and a slave device when the busy control option is used.

★ **Figure 10-17. System Configuration When Busy Control Option Is Used**



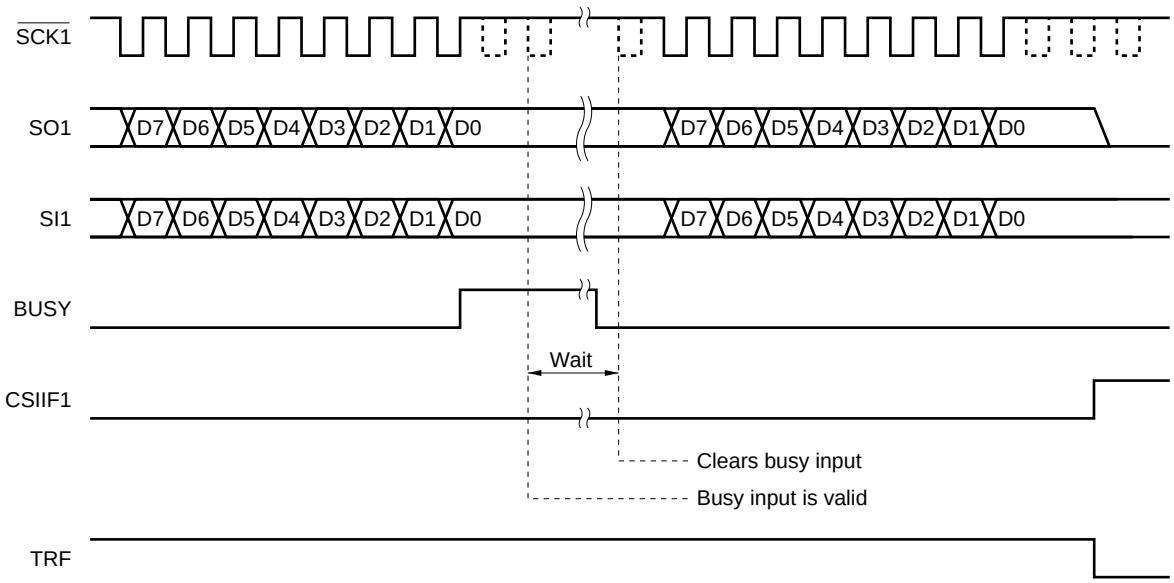
The master device inputs the busy signal output by the slave device to the BUSY/P24 pin. The master device samples the input busy signal in synchronization with the falling of the serial clock. Even if the busy signal becomes active while 8-bit data is being transmitted or received, transmission/reception by
★ the master is not kept waiting. If the busy signal is active at the falling edge of the serial clock two clocks after completion of transmission/reception of the 8-bit data, the busy input becomes valid. After that, the master transmission/reception is kept waiting while the busy signal is active.
The active level of the busy signal is set by bit 0 (BUSY0) of ADTC.

BUSY0 = 0: Active high
BUSY1 = 1: Active low

When using the busy control option, select the internal clock as the serial clock. Control with the busy signal cannot be implemented with the external clock.
Figure 10-18 shows the operation timing when the busy control option is used.

Caution Busy control cannot be used simultaneously with the interval time control function of the automatic data transmit/receive interval specification register (ADTI). If used, busy control is invalid.

★ **Figure 10-18. Operation Timing When Busy Control Option Is Used (When BUSY0 = 0)**

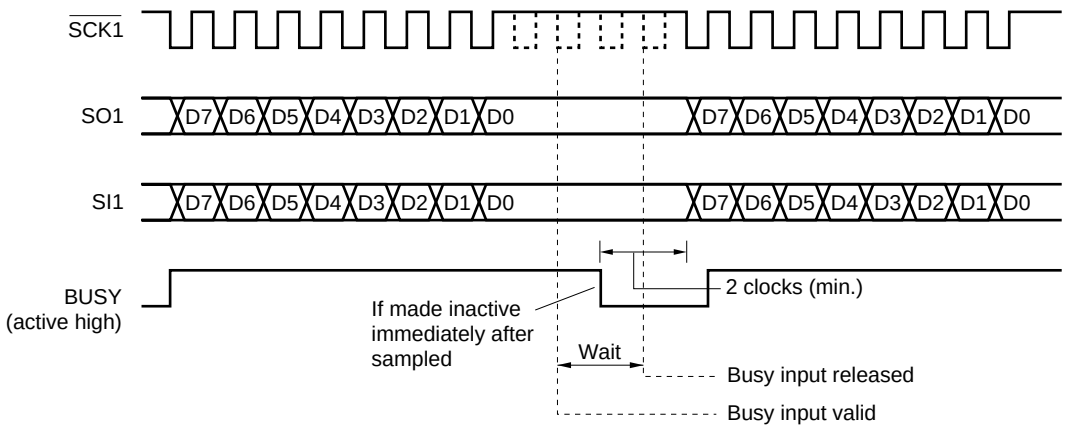


Caution If the TRF is cleared, the SO1 pin goes low.

Remark CSIIF1: Interrupt request flag
TRF: Bit 3 of automatic data transmit/receive control register (ADTC)

When the busy signal becomes inactive, waiting is released. If the sampled busy signal is inactive, transmission/reception of the next 8-bit data is started at the falling edge of the next clock.
Because the busy signal is asynchronous with the serial clock, it takes up to 1 clock until the busy signal
★ is sampled by the master, even if made inactive by the slave. It takes 1 clock until data transfer is started after the busy input was cleared.
To accurately release waiting, the slave must keep the busy signal inactive at least for the duration of
★ 2 clocks.
Figure 10-19 shows the timing of the busy signal and releasing the waiting. This figure shows an example where the busy signal is active as soon as transmission/reception has been started.

★ **Figure 10-19. Busy Signal and Wait Release (When BUSY0 = 0)**



(b) Bit shift detection by busy signal

During automatic transmission/reception, a bit shift of the serial clock of the slave device may occur because noise is superimposed on the serial clock signal output by the master device. In this case, the master can detect the bit shift by checking the busy signal during transmission by using the busy control option.

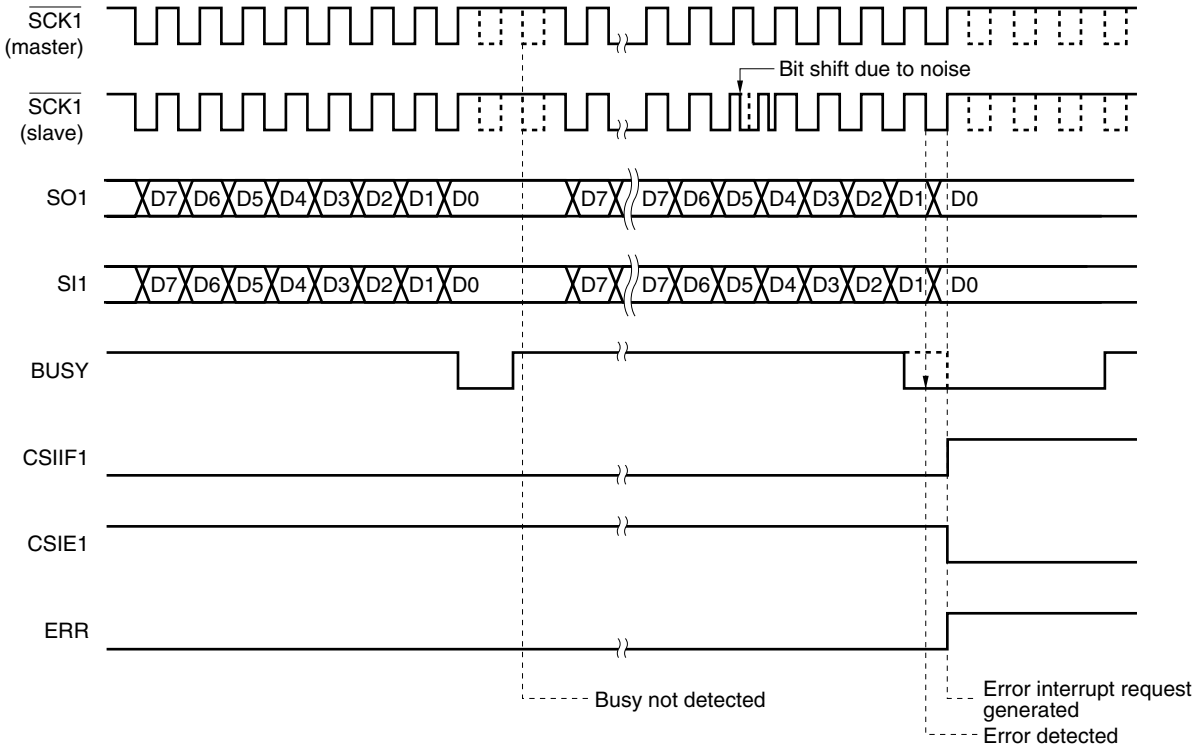
A bit shift is detected by using the busy signal as follows.

On the slave side, set so that a busy signal is output after the 8th rising edge of the serial clock for data transmission/reception. (If not wishing for a wait to be inserted due to the busy signal at this time, make the busy signal inactive within 2 clocks.)

★ On the master side, the busy signal is detected at the falling edge of the 8th clock of the serial clock by setting bit 5 (ERCE) of the automatic data transmit/receive control register (ADTC) to “1”. If bit 5 is active at this time, error processing (bit 4 (ERR) of the automatic data send/receive control register (ADT) is set to “1” and bit 7 (CSIE1) of serial operation mode register 1 (CSIM1) is cleared to “0”) is performed in synchronization with the rising edge of the 8th clock, and an interrupt request signal is generated.

Figure 10-20 shows the operation timing of the bit shift detection function by the busy signal.

★ **Figure 10-20. Operation Timing of Bit Shift Detection Function by Busy Signal (When BUSY0 = 1)**



CSIIF1: Interrupt request flag

CSIE1: Bit 7 of serial operation mode register1 (CSIM1)

ERR: Bit 4 of automatic data transmit/receive control register (ADTC)

(5) Timing of interrupt request signal generation

The interrupt signal is generated in synchronization with the timing shown in Table 10-2.

★ **Table 10-2. Timing of Interrupt Request Signal Generation**

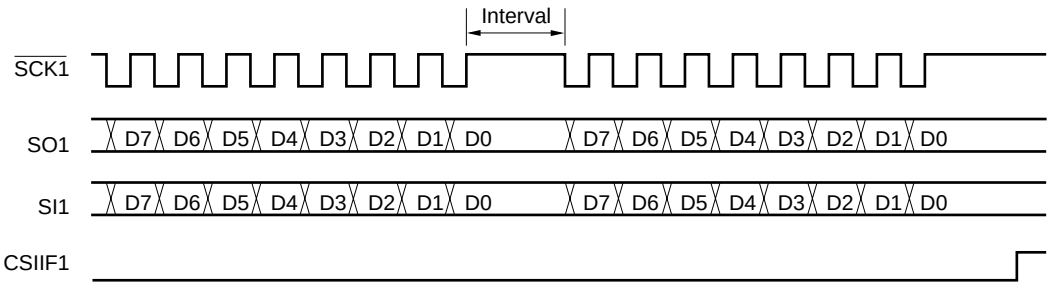
Operating Mode		Timing of Interrupt Request Signal
Single mode	Master mode	Rising of 10th serial clock at end of transfer
	Slave mode	Rising of 8th serial clock at end of transfer
Repetitive transmit mode		Not generated
If bit shift occurs during transmission/reception		Rising of 8th serial clock

(6) Interval time of automatic transmission/reception

Because read/write to/from the buffer RAM using the automatic transmit/receive function is performed asynchronously with the CPU processing, the interval time is dependent on the CPU processing of the timing of the eighth rising of the serial clock and the set value of the automatic data transmit/receive interval specification register (ADTI). Whether the interval time is dependent on ADIT is selected by setting of bit 7 (ADTI7) of ADTI. If ADTI7 is reset to 0, the interval time is $2/f_{SCK}$. If ADTI7 is set to 1, the interval time determined by the set contents of ADTI or interval time ($2/f_{SCK}$) by the CPU processing is selected whichever greater. Figure 10-21 shows the interval time of automatic transmission/reception

Remark f_{SCK}: Serial clock frequency

★ **Figure 10-21. Interval Time of Automatic Transmission/Reception**



The following expression must be satisfied to access the buffer RAM.

1 transfer cycle + interval time ≥ Read access + Write access + CPU buffer RAM access time

In the case of a “high-speed CPU & low-speed SCK”, the interval time is not necessary. In the case of a “low-speed CPU & high-speed SCK”, the interval time is necessary.
In this case, make sure that a sufficient interval time elapses, by using the automatic data transmit/receive interval specification register (ADTI), so that the above expression is satisfied.

CHAPTER 11 SERIAL INTERFACE SIO3

11.1 Function of Serial Interface SIO3

Serial interface SIO3 has the following two modes.

- Operation stop mode
- 2-wire serial mode (transmission only)

(1) Operation stop mode

This mode is used when serial transfer is not performed. For details, refer to **11.4.1 Operation stop mode**.

(2) 2-wire serial mode (transmission only) (with MSB first)

In this mode, 8-bit data is transferred by using three lines: serial clock ($\overline{\text{SCK3}}$) and serial output (SO3). Receive operation cannot be performed.

The first bit of the 8-bit data to be transferred is fixed to the MSB.

The 2-wire serial mode is useful when connecting peripheral ICs or display controller having a clocked serial interface. For details, refer to **11.4.2 2-wire serial mode (transmission only)**.

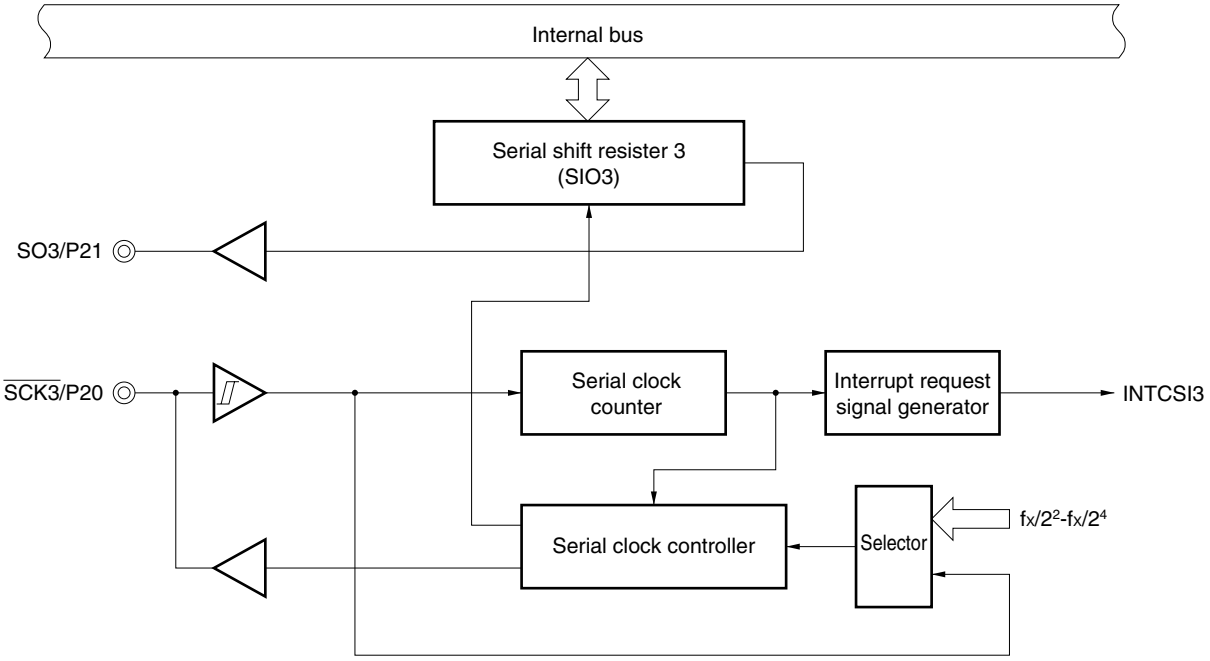
11.2 Configuration of Serial Interface SIO3

Serial interface SIO3 includes the following hardware.

Table 11-1. Configuration of Serial Interface SIO3

Item	Configuration
Register	Serial shift register 3 (SIO3)
Control register	Serial operation mode register 3 (CSIM3)

★ **Figure 11-1. Block Diagram of Serial Interface SIO3**



(1) Serial shift register 3 (SIO3)

This 8-bit register converts parallel data to serial data to perform serial transmission (shift operation) in synchronization with the serial clock.

SIO3 is set by an 8-bit memory manipulation instruction.

The serial operation is started by writing data to SIO3 when bit 7 (CSIE3) of serial operation mode register 3 (CSIM3) is 1.

The data written to SIO3 is output to the serial output line (SO3).

$\overline{\text{RESET}}$ input makes this register undefined.

Caution Do not read SIO3 during transmission.

(2) Serial clock counter

This counter counts the serial clock output or input during transmission to check that 8-bit data has been transmitted.

11.3 Registers Controlling Serial Interface SIO3

Serial interface SIO3 is controlled by serial operation mode register 3 (CSIM3).

(1) Serial operation mode register 3 (CSIM3)

This register selects the serial clock of the serial interface SIO3, and enables or disables the operation.

CSIM3 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM3 to 00H.

Caution Set the port mode register (PM××) in the 2-wire serial mode as follows. Set the output latch to 0.

<Serial clock setting>

- **In the case of serial clock output (master transmission)**
  Set P20 ($\overline{\text{SCK3}}$) to the output mode (PM20 = 0).
- **In the case of serial clock input (slave transmission)**
  Set P20 to input mode (PM20 = 1).

<Operation mode setting>

- **In transmission mode**
  Set P21 (SO3) to output mode (PM21 = 0).

Figure 11-2. Format of Serial Operation Mode Register 3

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM3	CSIE3	0	0	0	0	0	SCL31	SCL30	FF66H	00H	R/W

CSIE3	Enables or disables operation of serial interface SIO3		
	Shift register operation	Serial counter	Port
0	Disabled	Cleared	Port function[Note]
1	Enabled	Count operation enabled	Serial function + port function

SCL31	SCL30	Selects clock
0	0	External clock input to $\overline{\text{SCK3}}$ pin
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^3$ (625 kHz)
1	1	$f_X/2^4$ (313 kHz)

Note The SO3 and $\overline{\text{SCK3}}$ pins can be used as port pins when CSIE3 = 0 (when the SIO3 operation is stopped).

★ **Caution Be sure to set bits 2 to 6 to "0".**

Remarks 1. fx: Main system clock oscillation frequency

2. ( ): fx = 5.0 MHz

11.4 Operation of Serial Interface SIO3

Serial interface SIO3 operates in the following two modes.

- Operation stop mode
- 2-wire serial mode (transmission only)

11.4.1 Operation stop mode

In the operation stop mode, the power consumption can be reduced because serial transfer is not executed.

Because serial shift register 3 (SIO3) does not perform the shift operation, this register can be used as a normal 8-bit register.

In this mode, the SO3 and $\overline{\text{SCK3}}$ pins can be used as normal I/O port pins.

(1) Register setting

The operation stop mode is set by serial operation mode register 3 (CSIM3).

CSIM3 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM3 to 00H.

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM3	CSIE3	0	0	0	0	0	SCL31	SCL30	FF66H	00H	R/W

CSIE3	Enables or disables operation of serial interface SIO3		
	Shift register operation	Serial counter	Port
0	Disabled	Cleared	Port function[Note]

Note The SO3 and $\overline{\text{SCK3}}$ pins can be used as port pins when CSIE3 = 0 (when the SIO3 operation is stopped).

★ **Caution Be sure to set bits 2 to 6 to “0”.**

11.4.2 2-wire serial mode (transmission only)

The 2-wire serial mode is useful for connecting a peripheral IC or display controller having a clocked serial interface. Communication is established by using three lines: serial clock ($\overline{SCK3}$) and serial output (SO).

(1) Register setting

The 2-wire serial mode is set by the serial operation mode register 3 (CSIM3).

CSIM3 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM3 to 00H.

Caution Set the port mode register (PM××) in the 2-wire serial mode as follows. Set the output latch to 0.

<Serial clock setting>

- **In the case of serial clock output (master transmission)**
  Set P20 ($\overline{SCK3}$) to the output mode (PM20 = 0).
- **In the case of serial clock input (slave transmission)**
  Set P20 to input mode (PM20 = 1).

<Operation mode setting>

- **In transmission mode**
  Set P21 (SO3) to output mode (PM21 = 0).

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM3	CSIE3	0	0	0	0	0	SCL31	SCL30	FF66H	00H	R/W

CSIE3	Enables or disables operation of serial interface SIO3		
	Shift register operation	Serial counter	Port
0	Disabled	Cleared	Port function[Note]
1	Enabled	Count operation enabled	Serial function + port function

SCL31	SCL30	Selects clock
0	0	External clock input to $\overline{SCK3}$ pin
0	1	$f_X/2^2$ (1.25 MHz)
1	0	$f_X/2^3$ (625 kHz)
1	1	$f_X/2^4$ (313 kHz)

Note The SO3 and $\overline{SCK3}$ pins can be used as port pins when CSIE3 = 0 (when the SIO3 operation is stopped).

★ **Caution Be sure to set bits 2 to 6 to "0".**

Remarks 1. fx: Main system clock oscillation frequency

2. ( ): fx = 5.0 MHz

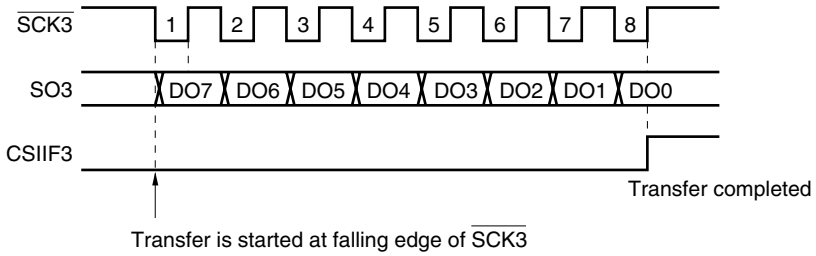
(2) Communication operation

In the 2-wire serial mode, data is transmitted in 8-bit units. Each bit of the data is transmitted in synchronization with the serial clock.

The shift operation of serial shift register 3 (SIO3) is performed in synchronization with the falling of the serial clock ($\overline{SCK3}$). The transmit data is retained by the SO3 latch and output from the SO3 pin.

When transfer of 8-bit data has been completed, SIO3 automatically stops its operation, and an interrupt request flag (CSIIF3) is set.

Figure 11-3. Timing in 2-Wire Serial Mode



(3) Transfer start

Serial transfer is started when data is assigned to serial shift register 3 (SIO3) if the following two conditions are satisfied.

- Set the operation control bit of serial interface SIO3 (bit 7 (CSIE3) of serial operation mode register 3 (CSIM3)) to 1
- If the internal serial clock is stopped or $\overline{SCK3}$ is high after 8-bit serial transfer

Caution Transfer is not started even if CSIE3 is set to "1" after data has been written to serial shift register 3 (SIO3).

Serial transfer is automatically stopped and an interrupt request flag (CSIIF3) is set when 8-bit transfer has been completed.

CHAPTER 12 VFD CONTROLLER/DRIVER

12.1 Function of VFD Controller/Driver

The VFD controller/driver of the μPD780232 Subseries has the following functions.

(1) Can output display signals (DMA operation) by automatically reading display data.
(2) The pins not used for VFD display can be used as I/O port or output port pins (FIP24 to FIP52 pins only).
(3) Luminance can be adjusted in 8 steps by display mode register 1 (DSPM1).
(4) Hardware for key scan application
- Generates an interrupt signal (INTKS) indicating key scan timing
- Timing in which key scan data is output can be detected by key scan flag (KSF).
- Whether key scan timing is inserted or not can be selected.

(5) High-voltage output buffer that can directly drive VFD
(6) FIP0 to FIP52 pins can be connected to pull-down resistors by mask option (mask ROM model only)[Note]. (The μPD78F0233 incorporates pull-down resistors for FIP0 to FIP23. The FIP24 to FIP52 pins do not have an internal pull-down resistor.)

★ **Note** When connecting a pull-down resistor is V_{LOAD} or V_{SS0} by mask option, adjust the number of pull-down resistors so that the total loss is not exceeded. (Refer to **12.7 Calculation of Total Power Dissipation**.)

Of the 53 VFD output pins of the μPD780232 Subseries, FIP24 to FIP52 are multiplexed with port pins. FIP0 to FIP23 are dedicated output pins.

FIP24 to FIP52 can be used as port pins when VFD display is disabled by bit 7 (DSPEN) of display mode register 0 (DSPM0). Even when VFD display is enabled, the VFD output pins not used for display signal output can be used as port pins.

Table 12-1. VFD Output Pins and Multiplexed Port Pins

VFD Pin Name	Multiplexed Port Name	I/O
FIP24 to FIP31	P30 to P37	Output-only port
FIP32 to FIP39	P40 to P47	Output-only port
FIP40 to FIP47	P50 to P57	I/O port
FIP48 to FIP52	P60 to P64	I/O port

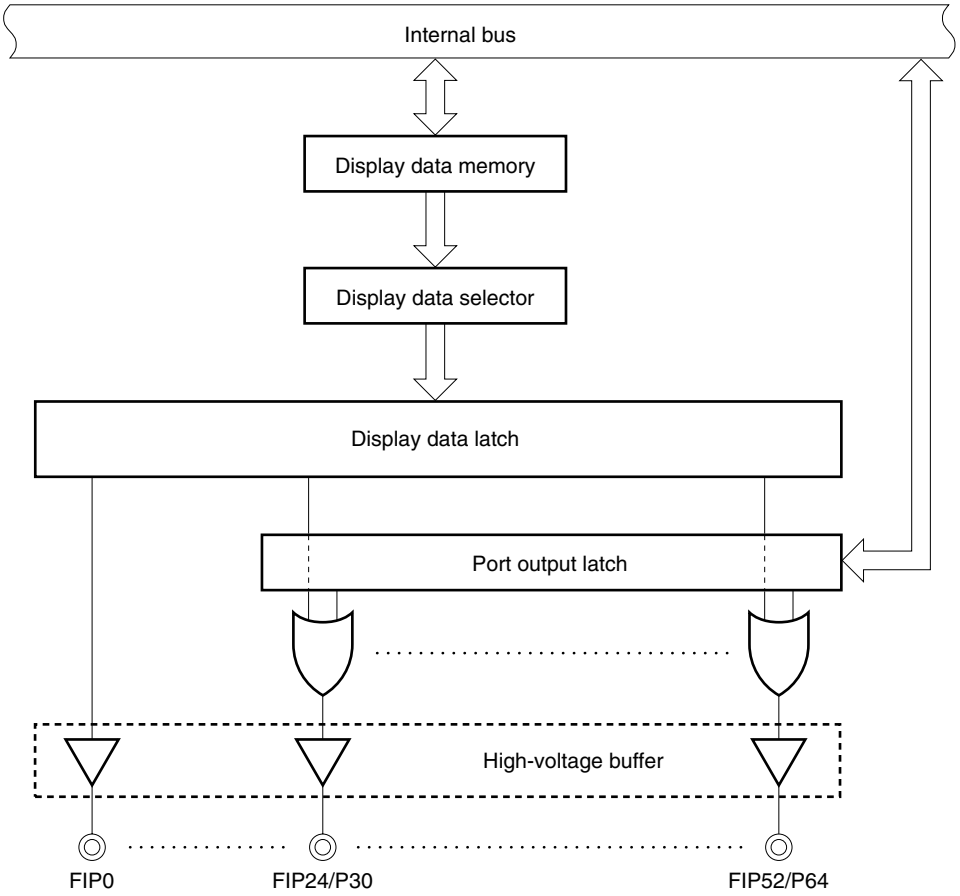
12.2 Configuration of VFD Controller/Driver

The VFD controller/driver includes the following hardware.

Table 12-2. Configuration of VFD Controller/Driver

Item	Configuration
Display	53
Control register	Display mode register 0 (DSPM0) Display mode register 1 (DSPM1) Display mode register 2 (DSPM2)

Figure 12-1. Block Diagram of VFD Controller/Driver



12.3 Registers Controlling VFD Controller/Driver

12.3.1 Control registers

The following three types of registers control the VFD controller/driver.

- Display mode register 0 (DSPM0)
- Display mode register 1 (DSPM1)
- Display mode register 2 (DSPM2)

(1) Display mode register 0 (DSPM0)

DSPM0 performs the following setting.

- Enables or disables display
- Number of VFD output pins

DSPM0 is set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets DSPM0 to 10H.

★ **Figure 12-2. Format of Display Mode Register 0**

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
DSPM0	DSPEN	0	FOUT5	FOUT4	FOUT3	FOUT2	FOUT1	FOUT0	FF69H	10H	R/W

DSPEN	Enables or disables VFD
0	Disables
1	Enables

FOUT5	FOUT4	FOUT3	FOUT2	FOUT1	FOUT0	Number of VFD output pins
0	1	0	0	0	0	17
0	1	0	0	0	1	18
0	1	0	0	1	0	19
0	1	0	0	1	1	20
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	32
1	0	0	0	0	0	33
1	0	0	0	0	1	34
1	0	0	0	1	0	35
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	0	0	0	1	50
1	1	0	0	1	0	51
1	1	0	0	1	1	52
1	1	0	1	0	0	53
Other						Setting prohibited

Cautions 1. Be sure to set bit 6 to “0”.

2. Do not write data to the bits other than DSPEN when bit 7 (DSPEN) = 1.

3. Be sure to set the output latch of the multiplexed port of a pin used for VFD output to “0”.

4. Segment and grids can be freely assigned among the VFD output signals set by DSPM0. However, when performing this setting, be careful about the pin assignment and the amplitude of the respective load currents.

(2) Display mode register 1 (DSPM1)

DSPM1 performs the following setting.

- Blanking width of VFD output signal
- Number of display patterns

DSPM1 is set by a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets DSPM1 to 01H.

Figure 12-3. Format of Display Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
DSPM1	FBLK2	FBLK1	FBLK0	FPAT4	FPAT3	FPAT2	FPAT1	FPAT0	FF6AH	01H	R/W

FBLK2	FBLK1	FBLK0	Blanking width of VFD output signal
0	0	0	1/16
0	0	1	2/16
0	1	0	4/16
0	1	1	6/16
1	0	0	8/16
1	0	1	10/16
1	1	0	12/16
1	1	1	14/16

FPAT4	FPAT3	FPAT2	FPAT1	FPAT0	Number of display patterns
0	0	0	0	1	2
0	0	0	1	0	3
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16
Other					Setting prohibited

Caution Do not write data to display mode register 1 (DSPM1) when bit 7 (DSPEN) of display mode register 0 (DSPM0) is 1.

(3) Display mode register 2 (DSPM2)

DSPM2 performs the following setting. It also indicates the status of the display timing/key scan.

- Insertion of key scan timing
- Display cycle (TDSP)

DSPM2 is set by a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears DSPM2 to 00H.

Figure 12-4. Format of Display Mode Register 2

Symbol	< 7 >	6	5	4	3	2	1	0	Address	After reset	R/W
DSPM2	KSF	KSM	0	0	0	0	FCYC1	FCYC0	FF92H	00H	R/W[Note]

KSF	Status of key scan cycle
0	Other than key scan cycle
1	Key scan cycle

KSM	Selects insertion of key scan cycle
0	Not inserted
1	Inserted

FCYC1	FCYC0	Display cycle
0	0	$2^{12}/f_X$ (819 μs)
0	1	$2^{11}/f_X$ (410 μs)
1	0	$2^{10}/f_X$ (205 μs)
1	1	Setting prohibited

Note Bit 7 is read-only bit.

Cautions 1. Be sure to set bits 2 to 5 to "0".

2. Do not write data to display mode register 2 (DSPM2) when bit 7 (DSPEN) of display mode register 0 (DSPM0) is 1.

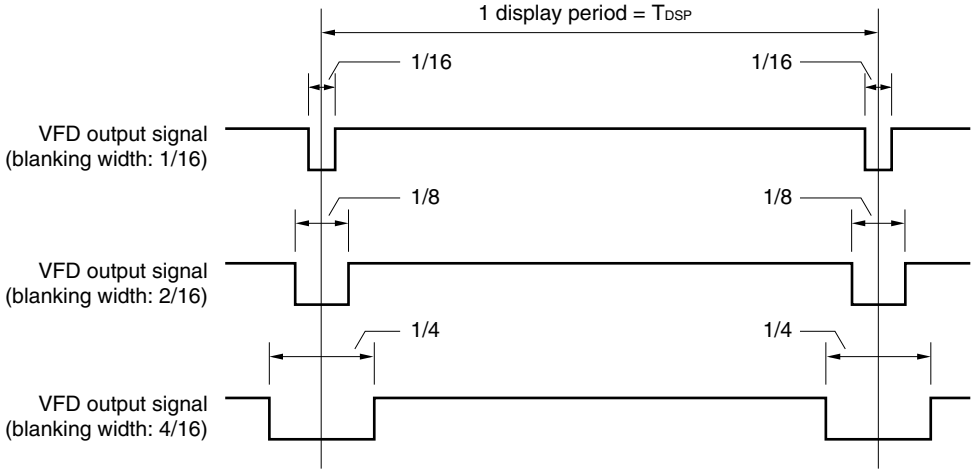
Remarks 1. fx: Main system clock oscillation frequency

2. ( ): fx = 5.0 MHz

12.3.2 One display period and blanking width

The VFD output signals are blanked equally at the beginning and end of the display period by the blanking width set by bits 0 to 2 (FBLK0 to FBLK2) of display mode register 1 (DSPM1).

Figure 12-5. Blanking Width of VFD Output Signal



12.4 Display Data Memory

The display data memory is a 112-byte RAM area that stores data to be displayed, and is mapped to addresses FA00H to FA6FH.

The VFD controller reads the data stored in the display data memory independently of the CPU operation for VFD display (DMA operation).

The area of the display data memory not used for display can be used as a normal RAM area.

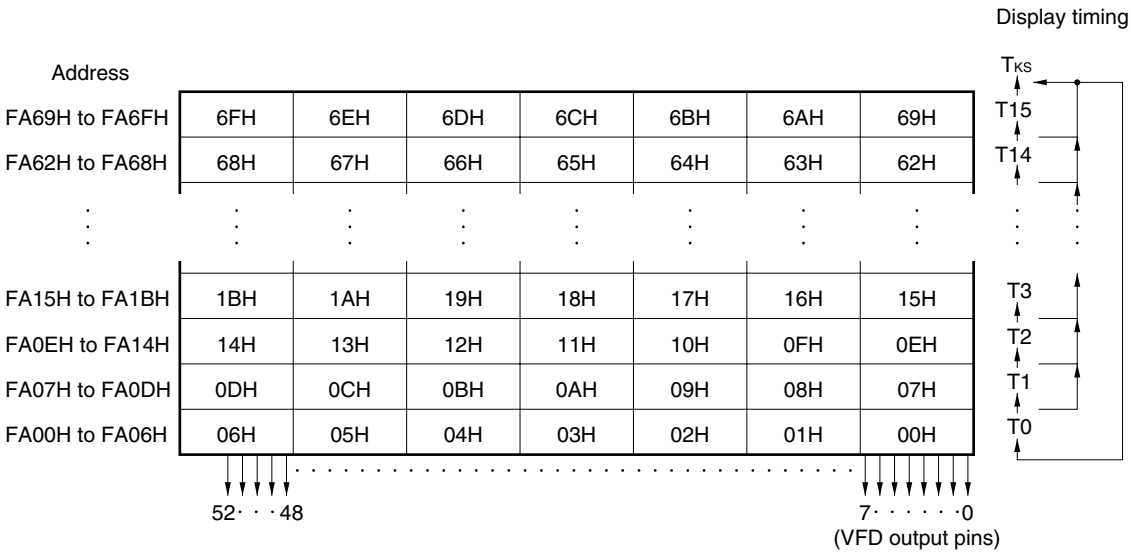
At key scan timing (T_{KS}), all the VFD output pins are cleared to “0”, and the data of the output latches of ports 3 to 6 are output to FIP24/P30 to FIP52/P64.

The address location of the display data memory is as follows:

- **With 53 VFD output pins and 16 patterns**

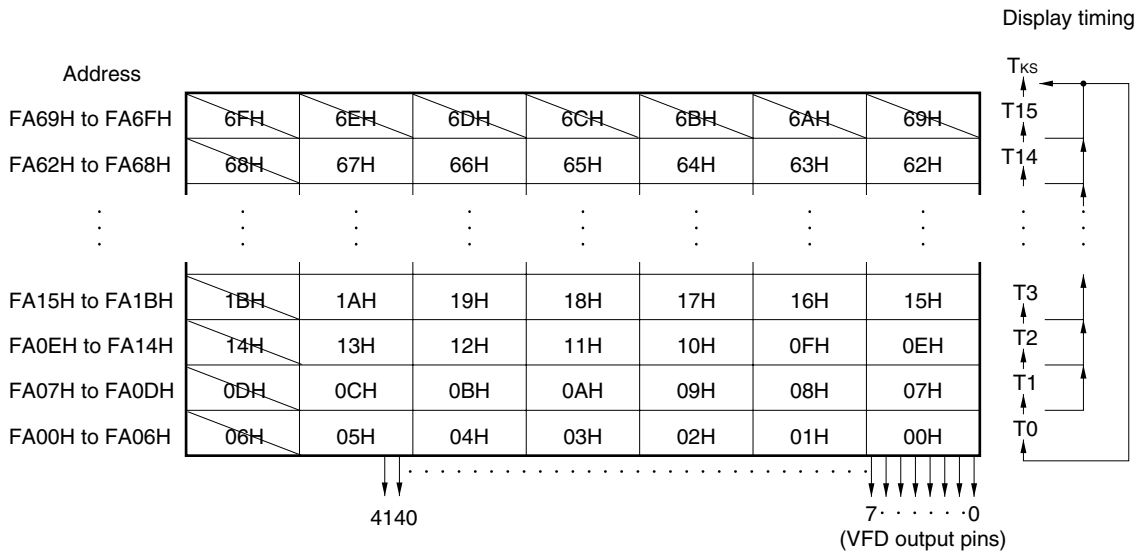
  The addresses of the display data memory corresponding to the data output at each display timing (T0 to T15) are as shown in Figure 12-6 (for example, T0 = FA00H to FA06H, and T1 = FA07H to FA0DH). When 53 VFD output pins (FIP0 to FIP52) are used, one block of display data consists of 7 bytes. VFD output pins 0 (FIP0) to 52 (FIP52) correspond to one block of display data sequentially, starting from the least significant bit toward the most significant bit.

Figure 12-6. Relationship Between Address Location of Display Data Memory and VFD Output (with 53 VFD Output Pins and 16 Patterns)



★ Regarding the display data memory, if 48 pins are used to display 1 pattern, the area that can be used as normal RAM is 1 byte, which increases by 1 byte for every 8-pin reduction. Moreover when the number of display patterns is 16 or less, whenever the number of patterns decreases, the area that can be used as normal RAM increases by 7 bytes each time.

★ **Figure 12-7. Relationship Between Address Location of Display Data Memory and VFD Output (with 42 VFD Output Pins and 14 Patterns)**



12.5 Key Scan Flag and Key Scan Data

12.5.1 Key scan flag

The key scan flag (KSF) is set to 1 during key scan timing, and is automatically reset to 0 at display timing.

KSF is mapped to bit 7 of display mode register 2 (DSPM2) and can be tested in 1-bit units. It cannot be written, however.

By testing KSF, it can be determined whether key scan timing is in progress, and whether key input data is correct can be checked.

Whether key scan timing is inserted or not can be selected by using the key scan timing insertion specification flag (KSM) (bit 6 of display mode register 2 (DSPM2)).

12.5.2 Key scan data

Data stored in ports 3 to 6 are output from the FIP24 to FIP52 pins during key scan timing.

Caution If scanning is performed in such a manner that both a segment and a digit turn ON during key scan timing, the display may flicker.

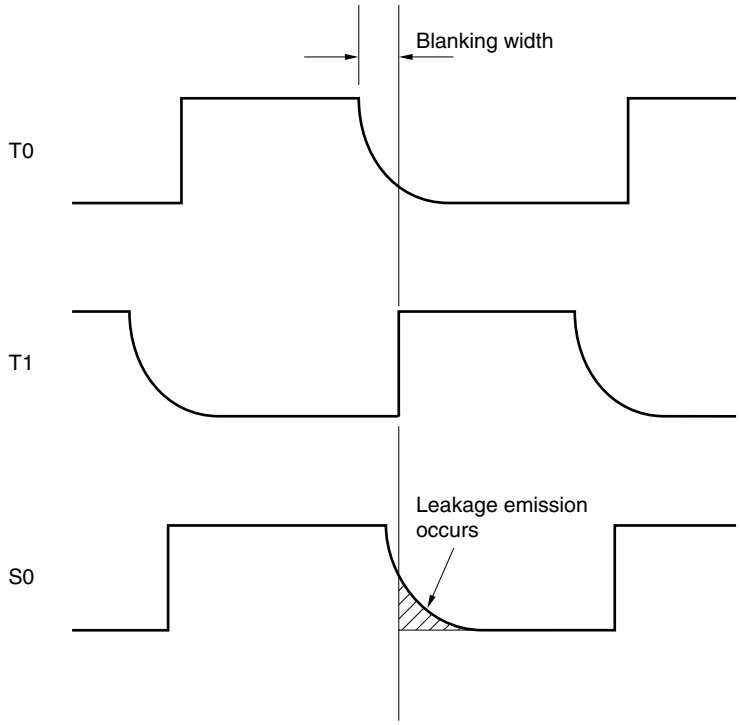
12.6 Leakage Emission of Fluorescent Indicator Panel

Leakage emission may take place when a fluorescent indicator panel is driven by the μPD780232 Subseries. The possible causes of this leakage emission are as follows.

(1) Short blanking time

Figure 12-8 shows the signal waveforms of a 2-digit display where the first digit T0 lights and the second digit remains dark. If the blanking time is too short as shown in this figure, the T1 signal rises before the segment signal is deasserted, causing leakage emission. Generally, the blanking time must be about 20 μs. Determine the set value of display mode register 1 (DSPM1), taking this into consideration.

Figure 12-8. Leakage Emission Because of Short Blanking Time



(2) Segment-grid capacitance of fluorescent indicator panel

Even if a sufficiently long blanking time is ensured as shown in Figure 12-10, leakage emission may still occur. This is because the fluorescent indicator panel has a capacitance between the grid and segment, as indicated by C_{SG} in the Figure 12-9, and the timing signal pin is raised via C_{SG}. If the voltage of the timing signal rises beyond the cutoff voltage (E_K) as shown in Figure 12-10, leakage emission occurs.

This whisker-like voltage changes with the values of C_{SG} and internal pull-down resistor (R_L). The greater the value of C_{SG}, and the greater the value of R_L, the higher this voltage, increasing the possibility of the occurrence of leakage emission.

The value of C_{SG} differs depending on the display area of the fluorescent indicator panel. The larger the area, the higher the C_{SG}.

Therefore, the value of the pull-down resistor differs depending on the size of the fluorescent indicator panel, in order to prevent leakage emission.

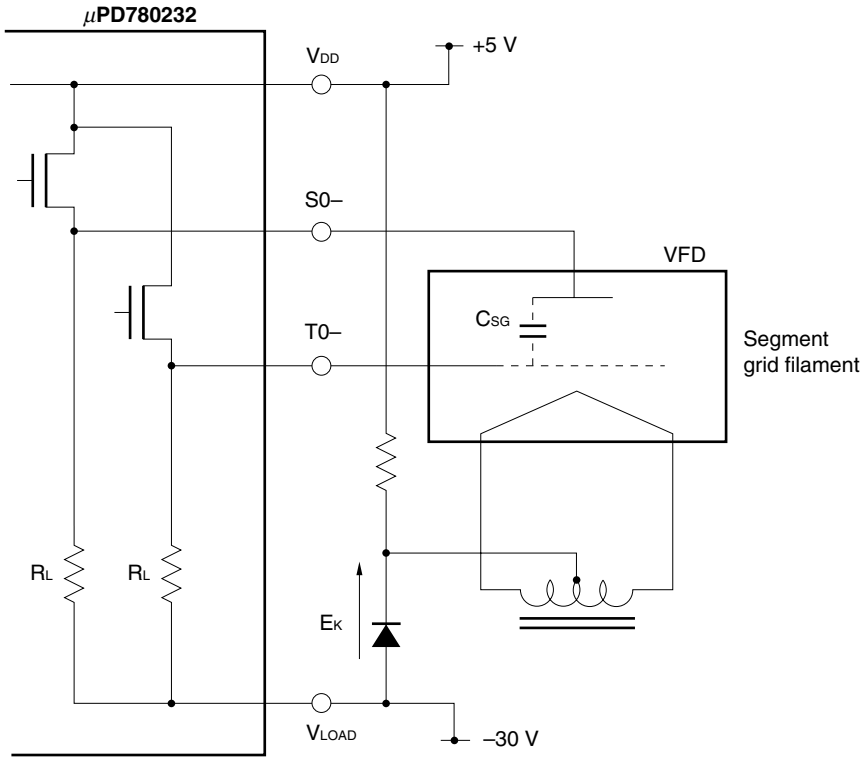
Because the value of the pull-down resistor that can be connected by mask option is relatively high, the leakage emission may not be suppressed by the internal pull-down resistor alone.

In case sufficient display quality cannot be obtained, deepen the back bias (increase E_K), attach a filter to the fluorescent indicator panel, or connect an external pull-down resistor of several 10 kΩ to the timing signal pin.

The likelihood of leakage emission caused by C_{SG} occurrence changes depending on the duty cycle of the whisker voltage vis-a-vis the total display cycle. The fewer the number of display digits, the less likelihood of occurrence of leakage emission.

Lowering the display luminance also has an effect of suppressing the leakage emission.

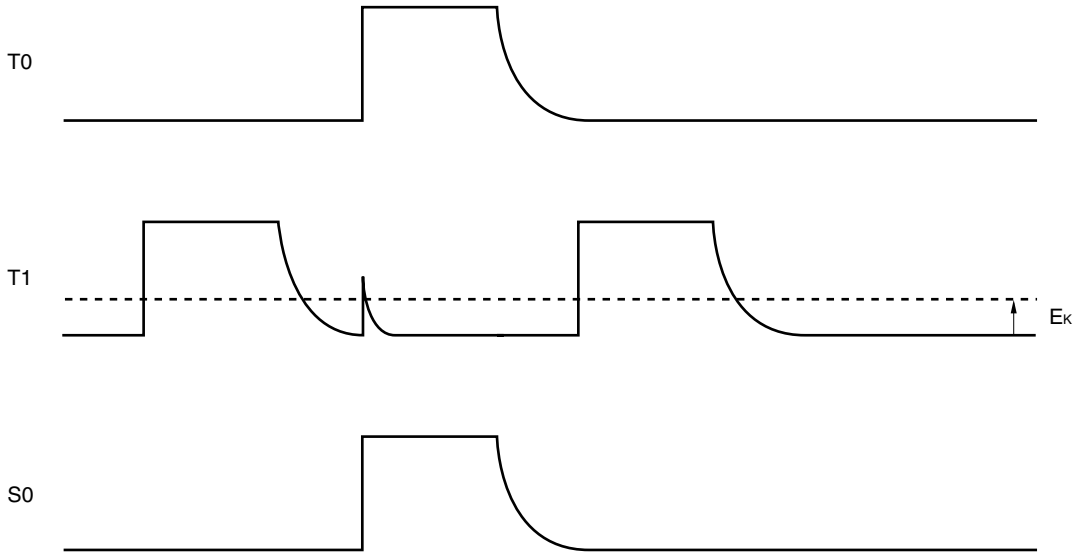
Figure 12-9. Leakage Emission Caused by C_{SG}



E_K: Cutoff voltage

R_L: Internal pull-down resistor

Figure 12-10. Leakage Emission Caused by C_{SG}

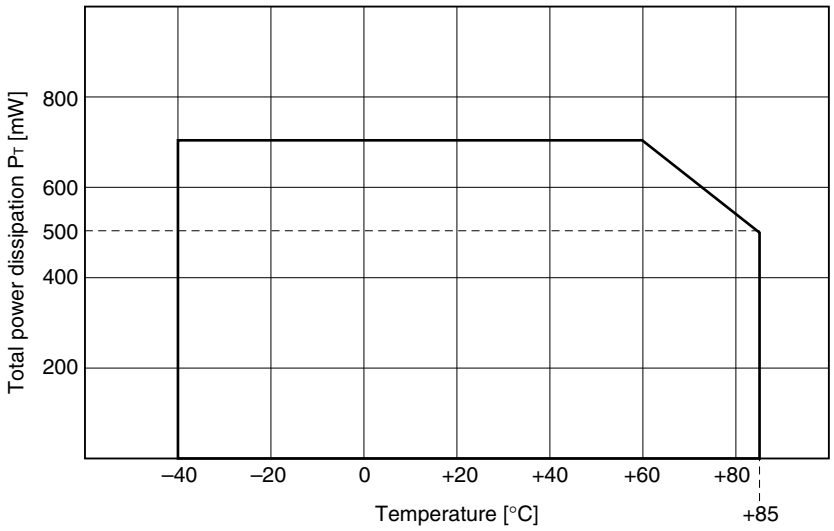


12.7 Calculation of Total Power Dissipation

The following three power dissipation are available for the μPD780232 Subseries. The sum of the three power dissipation should be less than the total power dissipation P_T (refer to **Figure 12-11**) (80% or less of ratings is recommended).

<1> CPU power dissipation: Calculate V_{DD} (MAX.) × I_{DD} (MAX.).
<2> Output pin power dissipation: Power dissipation when maximum current flows into each VFD output pin.
<3> Pull-down resistor power dissipation: Power dissipation by pull-down resistor incorporated in VFD output pin.

Figure 12-11. Total Power Dissipation P_T (T_A = –40 to +85°C)



The following is how to calculate total power dissipation for the example in Figure 12-12.

Example Assume the following conditions:
V_{DD} = 5.5 V, 5.0 MHz oscillation
Supply current (I_{DD}) = 21.0 mA
VFD output: 11 grids × 10 segments (Blanking width = 1/16: when FBLK0 to FBLK2 = 000B)
Maximum current at the grid pin is 15 mA.
Maximum current at the segment pin is 5 mA.
At the key scan timing, VFD output pin is off.
VFD output voltage: Grid $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)
Fluorescent display control voltage (V_{LOAD}) = –35 V
Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculation <1> to <3>, the total dissipation can be worked out.

<1> CPU power dissipation: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power dissipation:

Grid $(V_{DD} - V_{OD}) \times \dfrac{\text{Total current value of each grid}}{\text{The no. of grids} + 1} \times (1 - \text{Blanking width}) =$

$$2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{Grids}}{11\ \text{Grids} + 1} \times \left(1 - \frac{1}{16}\right) = 25.8\ \text{mW}$$

Segment $(V_{DD} - V_{OD}) \times \dfrac{\text{Total segment current value of illuminated dots}}{\text{The no. of grids} + 1} \times (1 - \text{Blanking width}) =$

$$0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{Dots}}{11\ \text{Grids} + 1} \times \left(1 - \frac{1}{16}\right) = 6.1\ \text{mW}$$

<3> Pull-down resistor power dissipation:

Grid $\dfrac{(V_{DD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \dfrac{\text{The no. of grids}}{\text{The no. grids} + 1} \times (1 - \text{Blanking width}) =$

$$\frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{Grids}}{11\ \text{Grids} + 1} \times \left(1 - \frac{1}{16}\right) = 36.4\ \text{mW}$$

Segment $\dfrac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \dfrac{\text{The no. of illuminated dots}}{\text{The no. of grids} + 1} \times (1 - \text{Blanking width}) =$

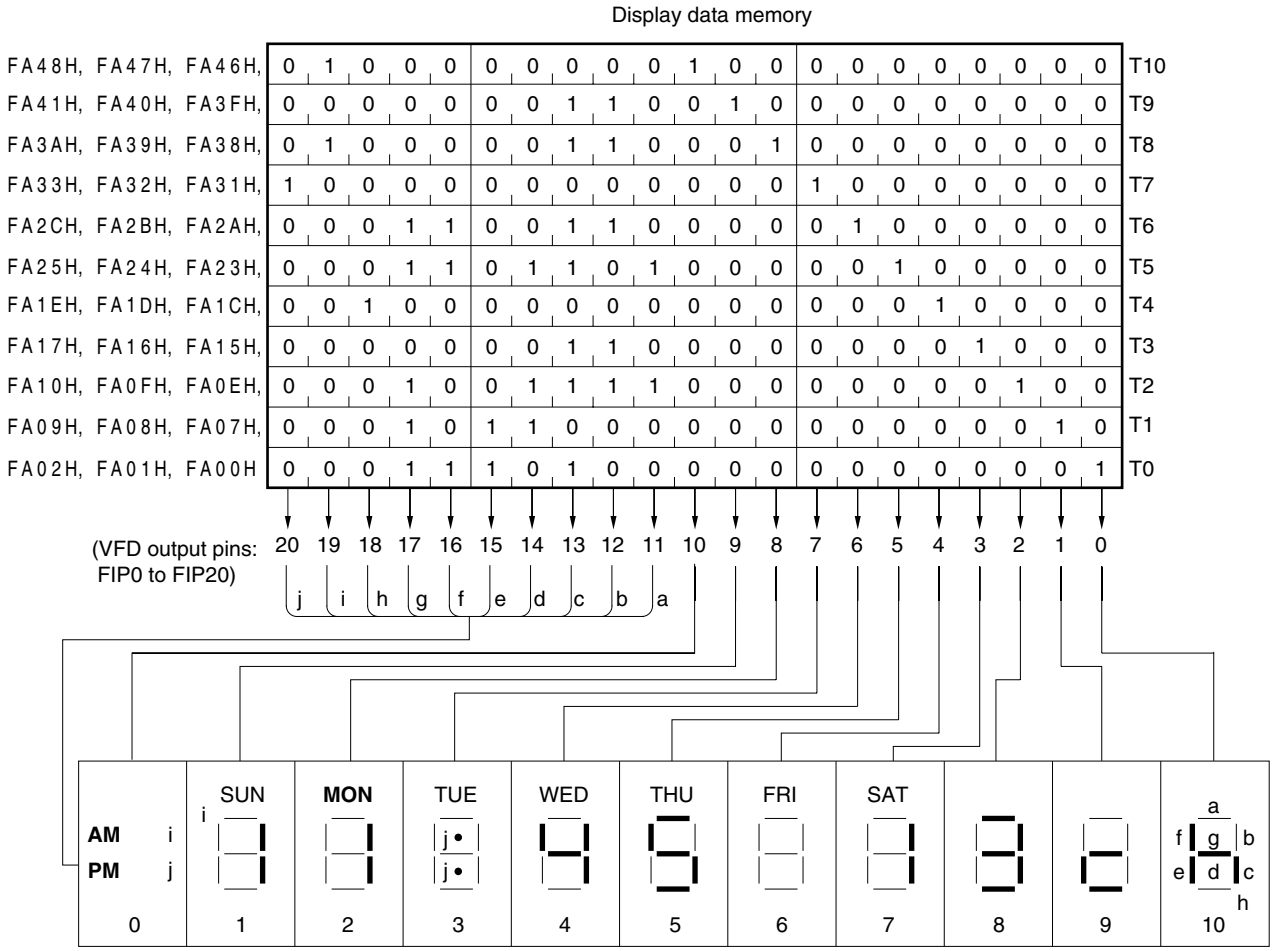
$$\frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{Grids} + 1} \times \left(1 - \frac{1}{16}\right) = 110.7\ \text{mW}$$

Total power dissipation = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power dissipation do not exceed the rating of the total power dissipation shown in Figure 12-11, so there is no problem in power dissipation.

However, when the total power dissipation exceeds the rating of the total power dissipation, it is necessary to lower the power dissipation. To reduce power dissipation, reduce the number of pull-down resistor.

Figure 12-12. Relationship Between Display Data Memory and VFD Output with 10 Segments-11 Digits Displayed



CHAPTER 13 INTERRUPT FUNCTIONS

13.1 Interrupt Function Types

The following three types of interrupt functions are used.

★ **(1) Non-maskable interrupt**

This interrupt is acknowledged even in a disabled state. It does not undergo interrupt priority control and is given top priority over all other interrupt requests. While non-maskable interrupts are being serviced, all other interrupts are held pending.

It generates a standby release signal.

Only one interrupt request source from the watchdog timer is incorporated as a non-maskable interrupt.

(2) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into a high interrupt priority group and a low interrupt priority group by setting the priority specification flag register (PR0L and PR0H).

Multiple high priority interrupts can be applied to low priority interrupts. If multiple interrupts with the same priority are simultaneously generated, each interrupt has a predetermined priority (refer to **Table 13-1**).

★ The standby release signal is generated and STOP or HALT mode is released.

Two external interrupt request sources and 10 internal interrupt request sources are incorporated as maskable interrupts.

(3) Software interrupt

This is a vectored interrupt to be generated by executing the BRK instruction. It is acknowledged even in a disabled state. The software interrupt does not undergo interrupt priority control.

13.2 Interrupt Sources and Configuration

A total of 14 non-maskable, maskable and software interrupts are incorporated in the interrupt sources (refer to **Table 13-1**).

Table 13-1. Interrupt Sources

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (with internal timer mode selected)			(B)
	1	INTP0	Detection of pin input edge	External	0006H	(C)
	2	INTP1			0008H	
	3	INTTM90	Detection of remote control timer input rising edge	Internal	000AH	(B)
	4	INTTM91	Detection of remote control timer input falling edge		000CH	
	5	INTTM92	Overflow of remote control timer		000EH	
	6	INTKS	Key scan timing from VFD controller/driver		0010H	
	7	INTCSI1	End of transfer of serial interface SIO1		0012H	
	8	INTCSI3	End of transfer of serial interface SIO3		0014H	
	9	INTTM80	Match between TM80 and CR80		0016H	
	10	INTTM81	Match between TM81 and CR81		0018H	
	11	INTAD	End of A/D conversion		001AH	
Software	—	BRK	Execution of BRK instruction	—	003EH	(D)

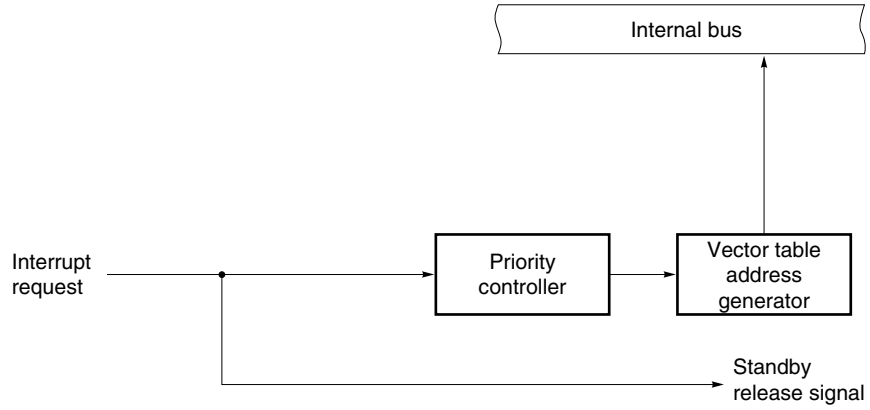
Notes 1. The default priority is the priority applicable when two or more maskable interrupts are generated simultaneously. 0 is the highest priority, and 11 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 13-1.

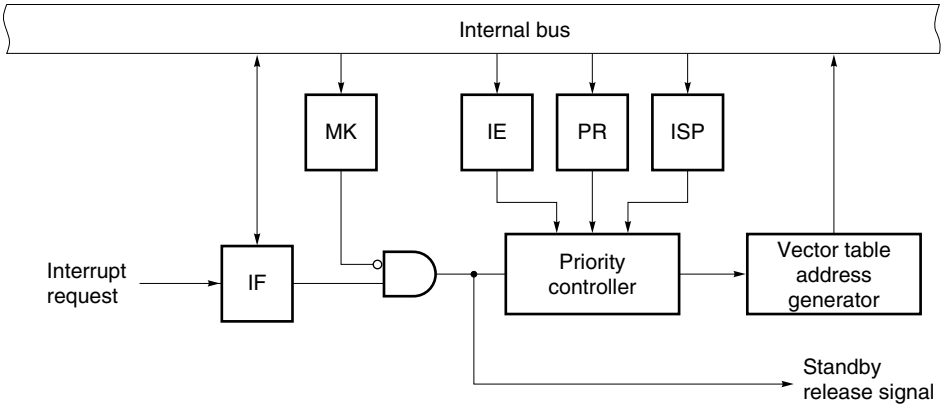
★ **Remark** The watchdog timer interrupt (INTWDT) can be selected from a non-maskable interrupt or a maskable interrupt (internal).

Figure 13-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0, INTP1)

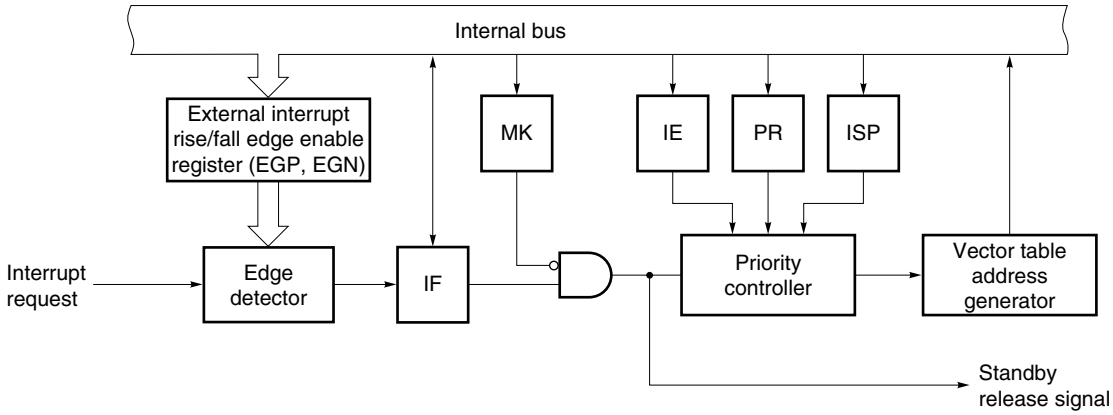
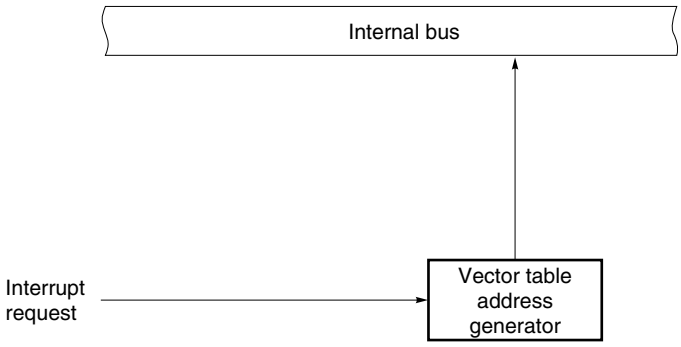


Figure 13-1. Basic Configuration of Interrupt Function (2/2)

★ **(D) Software interrupt**



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

13.3 Registers Controlling Interrupt Function

The following six types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L and IF0H)
- Interrupt mask flag register (MK0L and MK0H)
- Priority specification flag register (PR0L and PR0H)
- External interrupt rising edge enable register (EGP)
- External interrupt falling edge enable register (EGN)
- Program status word (PSW)

Table 13-2 gives a listing of interrupt request flags, interrupt mask flags and priority specification flag names corresponding to interrupt request sources.

Table 13-2. Various Flags Corresponding to Interrupt Request Sources

Interrupt Request Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	WDTIF[Note]	IF0L	WDTMK[Note]	MK0L	WDTPR[Note]	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTTM90	TMIF90		TMMK90		TMPR90	
INTTM91	TMIF91		TMMK91		TMPR91	
INTTM92	TMIF92		TMMK92		TMPR92	
INTKS	KSIF		KSMK		KSPR	
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTCSI3	CSIIF3	IF0H	CSIMK3	MK0H	CSIPR3	PR0H
INTTM80	TMIF80		TMMK80		TMPR80	
INTTM81	TMIF81		TMMK81		TMPR81	
INTAD	ADIF		ADMK		ADPR	

Note The WDTIF, WDTMK, and WDTPR flags are interrupt control flags used when the watchdog timer is used as an interval timer.

(1) Interrupt request flag registers (IF0L and IF0H)

The interrupt request flag is set to (1) when the corresponding interrupt request occurred or an instruction is executed. It is cleared to (0) when an instruction is executed upon acknowledgment of an interrupt request or upon application of $\overline{\text{RESET}}$ input.

IF0L and IF0H are set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H are used in combination as a 16-bit register IF0, they are set by a 16-bit memory operation instruction.

$\overline{\text{RESET}}$ input sets these registers to 00H.

Figure 13-2. Format of Interrupt Request Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0L	CSIIF1	KSIF	TMIF92	TMIF91	TMIF90	PIF1	PIF0	WDTIF	FFE0H	00H	R/W

	7	6	5	4	<3>	<2>	<1>	<0>			
IF0H	0	0	0	0	ADIF	TMIF81	TMIF80	CSIIF3	FFE1H	00H	R/W

xxIF	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated: Interrupt request state

Cautions 1. The WDTIF flag is R/W enabled only when a watchdog timer is used as an interval timer. If the watchdog timer is used in watchdog timer mode 1, set the WDTIF flag to 0.

2. Be sure to set bits 4 to 7 of IF0H to 0.

★ **3. Be sure to clear an interrupt request flag when operating a timer, serial interface, or A/D converter after standby mode is released; otherwise an interrupt request flag may be set by noise.**

★ **4. If an interrupt is acknowledged, the interrupt request flag is automatically cleared before the interrupt routine is entered.**

(2) Interrupt mask flag registers (MK0L and MK0H)

The interrupt mask flag is used to enable/disable the corresponding maskable interrupt service and to set standby clear enable/disable.

MK0L and MK0H are set by a 1-bit or 8-bit memory manipulation instruction. When MK0L and MK0H are used in combination as a 16-bit register MK0, they are set by a 16-bit memory operation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

Figure 13-3. Format of Interrupt Mask Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0L	CSIMK1	KSMK	TMMK92	TMMK91	TMMK90	PMK1	PMK0	WDTMK	FFE4H	FFH	R/W

	7	6	5	4	<3>	<2>	<1>	<0>			
MK0H	1	1	1	1	ADMK	TMMK81	TMMK80	CSIMK3	FFE5H	FFH	R/W

xxMK	Interrupt servicing and standby mode control
0	Interrupt servicing enabled, standby mode release enabled
1	Interrupt servicing disabled, standby mode release disabled

Cautions 1. If the WDTMK flag is read when the watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as an external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

3. Be sure to set bits 4 to 7 of MK0H to 1.

(3) Priority specification flag registers (PR0L and PR0H)

The priority specification flag is used to set the corresponding maskable interrupt priority orders.

PR0L and PR0H are set by a 1-bit or 8-bit memory manipulation instruction. When PR0L and PR0H are used in combination as a 16-bit register PR0, they are set by a 16-bit memory operation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

Figure 13-4. Format of Priority Specification Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
PR0L	CSIPR1	KSPR	TMPR92	TMPR91	TMPR90	PPR1	PPR0	WDTPR	FFE8H	FFH	R/W

	7	6	5	4	3	2	<1>	<0>			
PR0H	1	1	1	1	ADPR	TMPR81	TMPR80	CSIPR3	FFE9H	FFH	R/W

xxPR	Priority level selection
0	High priority level
1	Low priority level

Cautions 1. When the watchdog timer is used in watchdog timer mode 1, set the WDTPR flag to 1.

2. Be sure to set bits 4 to 7 of PR0H to 1.

(4) External interrupt rising edge enable register (EGP), external interrupt falling edge enable register (EGN)

These registers specify the valid edge for INTP0 and INTP1.

EGP and EGN are set by a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears these registers to 00H.

★ **Figure 13-5. Format of External Interrupt Rising Edge Enable Register (EGP), External Interrupt Falling Edge Enable Register (EGN)**

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	0	0	0	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	0	0	0	0	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 or 1)
0	0	Interrupt disable
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

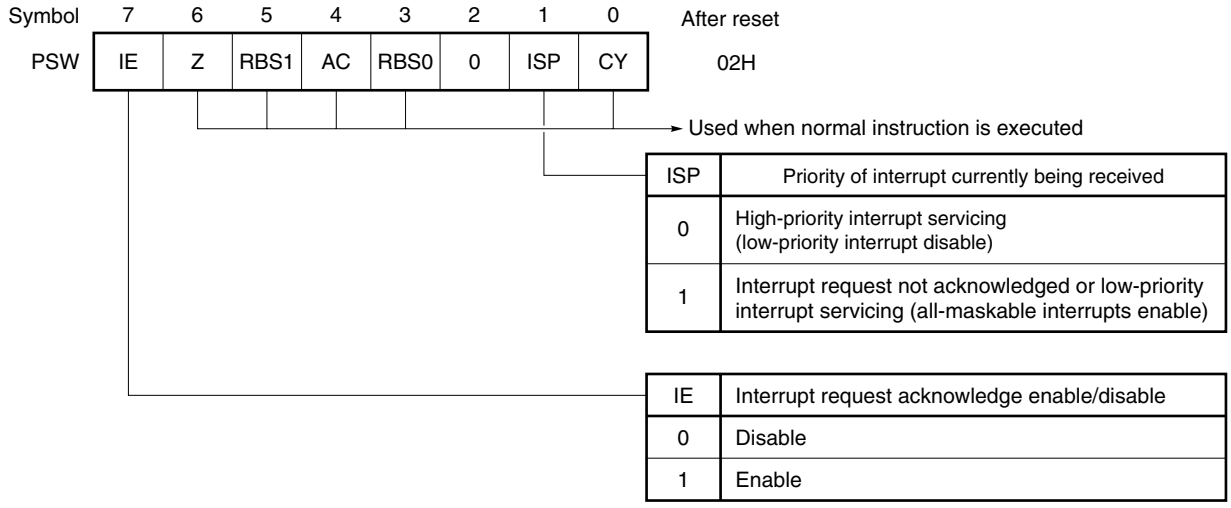
(5) Program status word (PSW)

The program status word is a register to hold the instruction execution result and the current status for interrupt request. The IE flag to set maskable interrupt enable/disable and the ISP flag to control nesting processing are mapped.

Besides 8-bit unit read/write, this register can carry out operations with a bit manipulation instruction and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged and the BRK instruction is executed, the contents of the PSW is automatically saved into a stack and the IE flag is reset to (0). If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The contents of the PSW is also saved into the stack with the PUSH PSW instruction. It is reset from the stack with the RETI, RETB, and POP PSW instructions.

$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 13-6. Configuration of Program Status Word



ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt request not acknowledged or low-priority interrupt servicing (all-maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

13.4 Interrupt Servicing Operations

13.4.1 Non-maskable interrupt request acknowledge operation

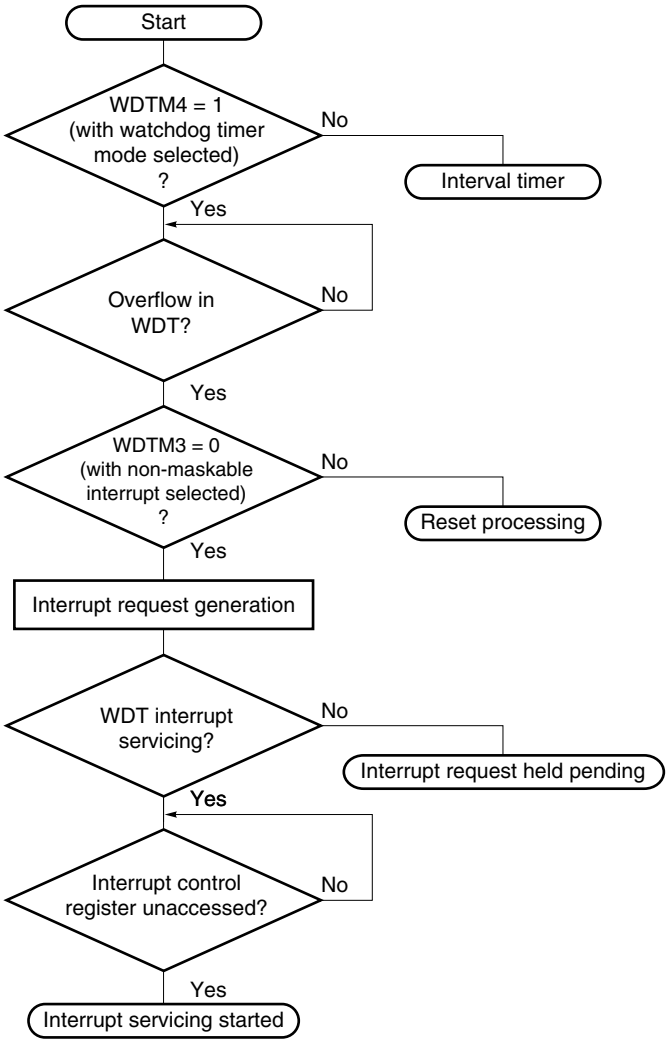
A non-maskable interrupt request is unconditionally acknowledged even if in an interrupt acknowledge disable state. It does not undergo interrupt priority control and has highest priority over all other interrupts.

If a non-maskable interrupt request is acknowledged, the contents are saved in the stacks, PSW and PC, in that order, the IE and ISP flags are reset to 0, and the vector table contents are loaded into PC and branched.

A new non-maskable interrupt request occurred during execution of a non-maskable interrupt servicing program is acknowledged after the current execution of the non-maskable interrupt servicing program is terminated (following RETI instruction execution) and one main routine instruction is executed. If a new non-maskable interrupt request occurred twice or more during non-maskable interrupt service program execution, only one non-maskable interrupt request is acknowledged after termination of the non-maskable interrupt service program execution.

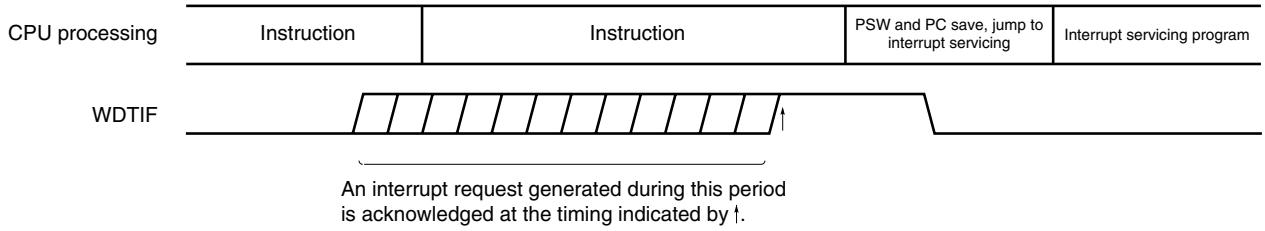
Figure 13-7 shows the flowchart illustrating how the non-maskable interrupt request occurs and is acknowledged. Figure 13-8 shows the acknowledge timing of the non-maskable interrupt. Figure 13-9 shows acknowledge operation of multiple non-maskable interrupts.

Figure 13-7. Flowchart from Non-Maskable Interrupt Request Generation to Acknowledgement



WDTM: Watchdog timer mode register
WDT: Watchdog timer

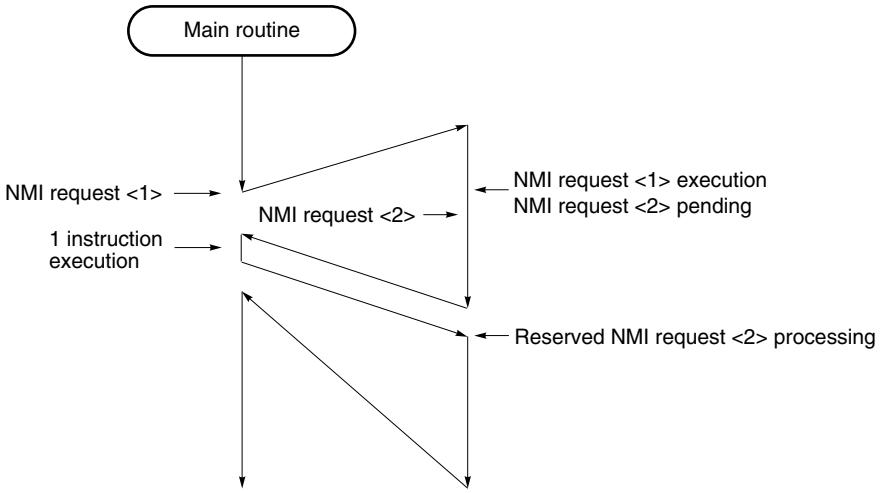
Figure 13-8. Timing of Non-Maskable Interrupt Request Acknowledgement



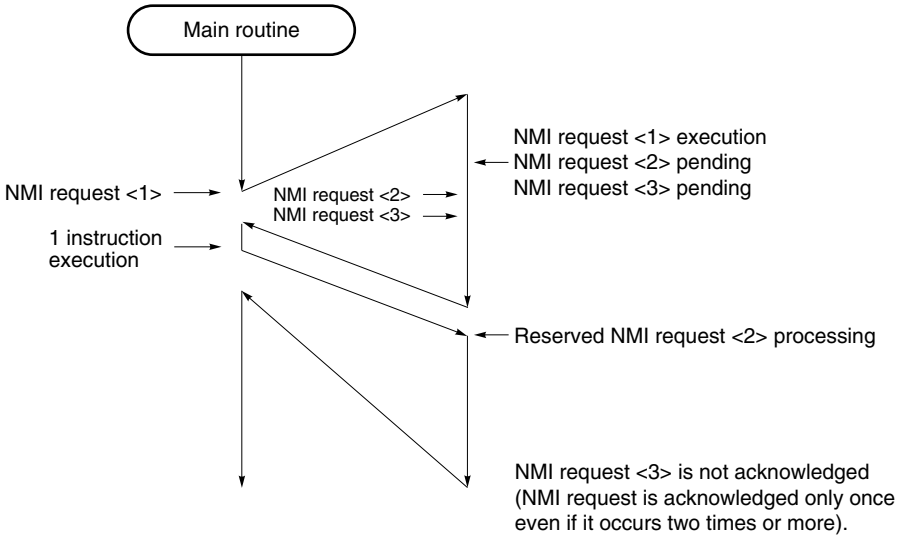
WDTIF: Watchdog timer interrupt request flag

Figure 13-9. Non-Maskable Interrupt Request Acknowledgement Operation

(a) If a new non-maskable interrupt request occurs during non-maskable interrupt servicing program execution



(b) If two non-maskable interrupt requests occur during non-maskable interrupt servicing program execution



13.4.2 Maskable interrupt request acknowledgement operation

A maskable interrupt request becomes acknowledgeable when an interrupt request flag is set to 1 and the interrupt mask (MK) flag is cleared to 0. A vectored interrupt request is acknowledged in an interrupt enable state (with the IE flag set to 1). However, a low-priority interrupt request is not acknowledged during high-priority interrupt servicing (with the ISP flag reset to 0).

Wait times from maskable interrupt request generation to interrupt servicing are shown in Table 13-3.

For the timing to acknowledge an interrupt request, refer to **Figures 13-11** and **13-12**.

Table 13-3. Times from Maskable Interrupt Request Generation to Interrupt Servicing

	Minimum Time	Maximum Time[Note]
When xxPR = 0	7 clocks	32 clocks
When xxPR = 1	8 clocks	33 clocks

Note If an interrupt request occurs just before a divide instruction, the wait time is maximized.

Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request specified for higher priority with the priority specification flag is acknowledged first. If two or more requests are assigned the same priority by the interrupt priority specification flag, the one with the higher default priority is acknowledged first.

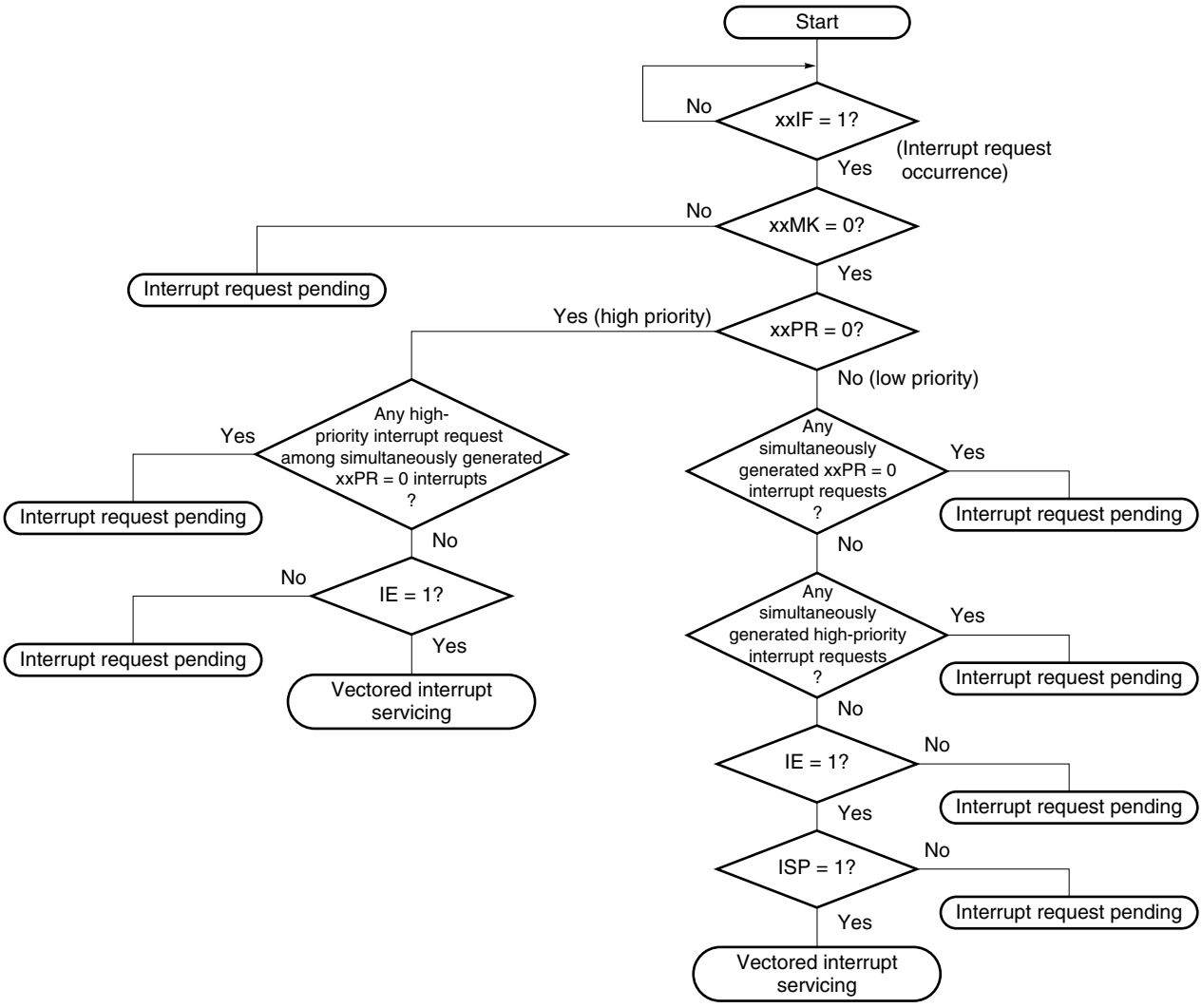
A pending interrupt request is acknowledged when it become acknowledgeable.

Figure 13-10 shows the algorithm of acknowledging interrupt requests.

If a maskable interrupt request is acknowledged, the contents are saved in the stacks, in the order of program status word (PSW), program counter (PC), the IE flag is reset to 0, and the acknowledged interrupt request priority specification flag contents are transferred to the ISP flag. In addition, the vector table data determined for each interrupt request is loaded into PC and branched.

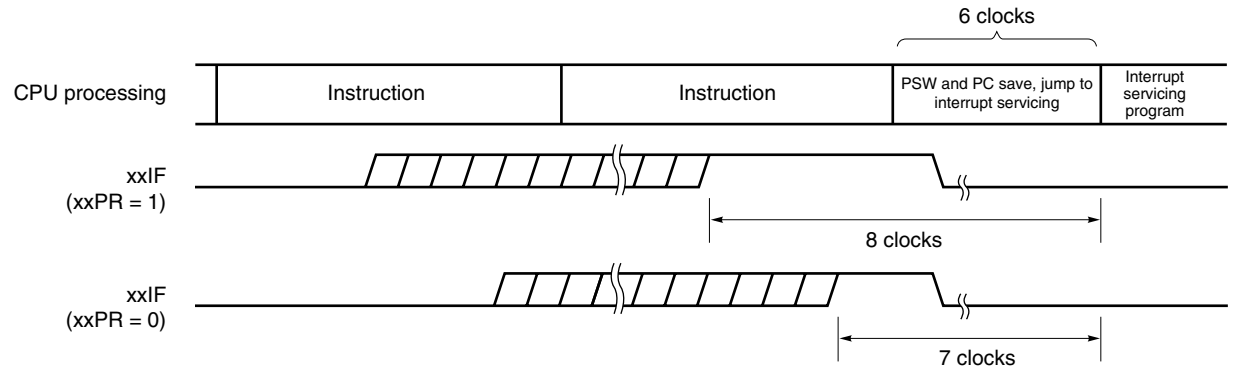
Restore from the interrupt is possible with the RETI instruction.

Figure 13-10. Interrupt Request Acknowledgement Processing Algorithm



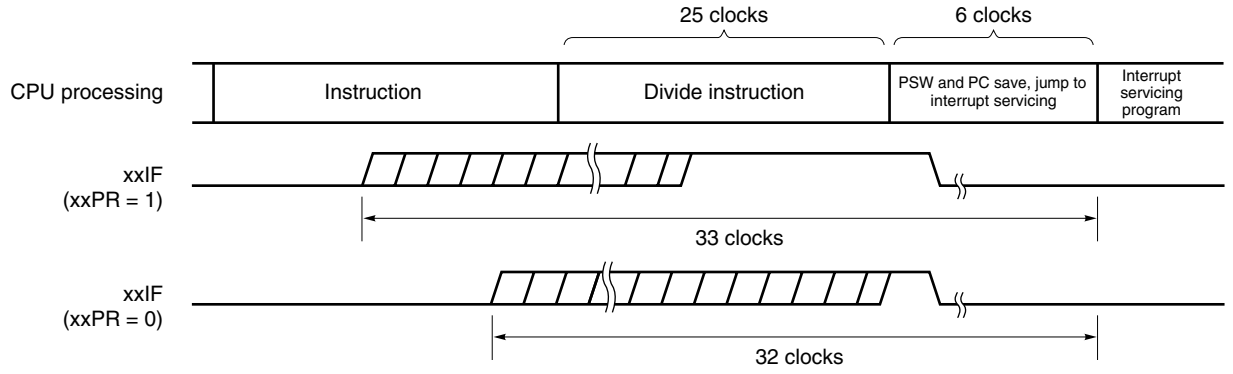
xxIF: Interrupt request flag
xxMK: Interrupt mask flag
xxPR: Priority specification flag
IE: Flag that controls maskable interrupt request acknowledge (1 = enable, 0 = disable)
ISP: Flag that indicates the priority level of the interrupt currently being serviced (0 = Higher priority interrupt servicing, 1 = No interrupt request acknowledged, or lower priority interrupt servicing)

Figure 13-11. Interrupt Request Acknowledgement Timing (Minimum Time)



Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

Figure 13-12. Interrupt Request Acknowledgement Timing (Maximum Time)



Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

13.4.3 Software interrupt request acknowledgement operation

A software interrupt request is acknowledged by BRK instruction execution. Software interrupt cannot be disabled.

If a software interrupt request is acknowledged, it is saved in the stacks, program status word (PSW), program counter (PC), in that order, the IE flag is reset to 0 and the contents of the vector tables (003EH and 003FH) are loaded to PC and branched.

Return from the software interrupt is possible with the RETB instruction.

Caution Do not use the RETI instruction for returning from the software interrupt.

13.4.4 Nesting

Acknowledging another interrupt while one interrupt is being serviced is called nesting.

A nesting does not occur unless acknowledgement of the interrupt request is enabled (IE = 1) (except the non-maskable interrupt). When an interrupt request is acknowledged, the other interrupt requests are disabled (IE = 0). To enable a nesting, therefore, the IE flag must be set to 1 by executing the EI instruction during interrupt servicing and the interrupt must be enabled. Even in the EI status, a nesting may not be enabled. In such a case, it is controlled according to the priority of the interrupt. An interrupt has two types of priorities: default priority and programmable priority. The nesting is controlled by the programmable priority.

In the EI status, if an interrupt request having the same as or higher priority than that of the interrupt currently being serviced is generated, and it is acknowledged as the nesting. If an interrupt request with a priority lower than that of the interrupt currently being serviced is generated, the nesting is not acknowledged.

If an interrupt is disabled, or if a nesting is not acknowledged because it has a low priority, the interrupt is held pending. After the servicing of the current interrupt is complete, and after one or more instruction executions of the main servicing has been executed, the pending interrupt is acknowledged.

Nesting is not acknowledged while the non-maskable interrupt is being serviced.

Table 13-4 shows interrupt requests enabled for nesting. Figure 13-13 shows nesting examples.

Table 13-4. Interrupt Request Enabled for Nesting During Interrupt Servicing

Nesting Request / Interrupt Being Serviced		Non-Maskable Interrupt Request	Maskable Interrupt Request			
			××PR = 0		××PR = 1	
			IE = 1	IE = 0	IE = 1	IE = 0
Non-maskable interrupt		×	×	×	×	×
Maskable interrupt	ISP = 0	√	√	×	×	×
	ISP = 1	√	√	×	√	×
Software interrupt		√	√	×	√	×

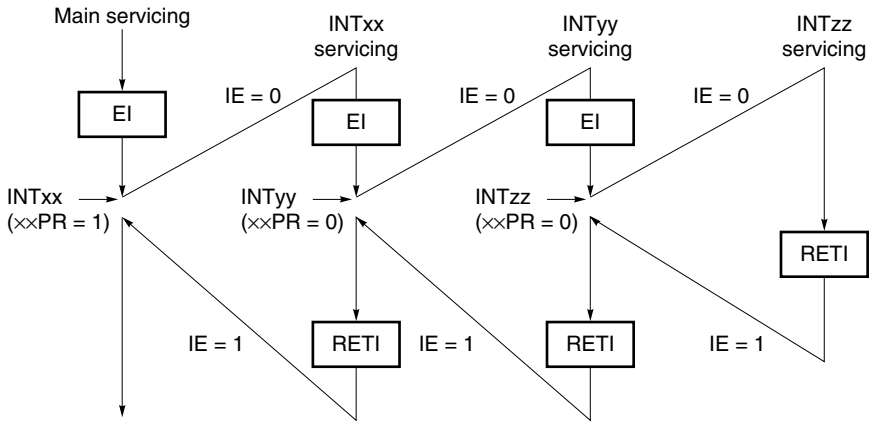
Remarks 1. √: Nesting enable
×: Nesting disable

2. ISP and IE are flags included in PSW.
ISP = 0: High-priority interrupt servicing
ISP = 1: Interrupt request is not acknowledged or low-priority interrupt servicing
IE = 0: Interrupt request acknowledge disabled
IE = 1: Interrupt request acknowledge enabled

3. ××PR is a flag included in PR0L and PR0H.
××PR = 0: High-priority level
××PR = 1: Low-priority level

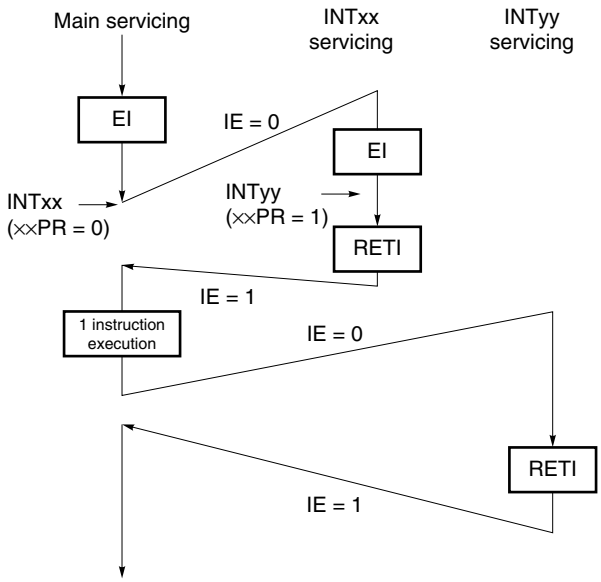
Figure 13-13. Nesting Example (1/2)

Example 1. Nesting is generated twice



Two interrupt requests INTyy and INTzz are acknowledged and nesting is generated when interrupt INTxx request is being serviced. Before each interrupt request is acknowledged, the EI instruction is always issued and the interrupt request is enabled.

Example 2. Nesting is not generated because of its priority

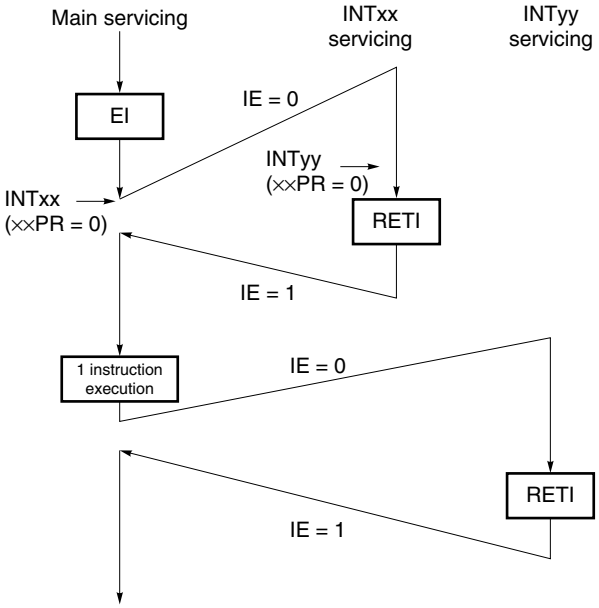


INTyy which is generated while INTxx is being serviced is not acknowledged and a nesting is not generaeted, because the priority of INTyy is lower than that of INTxx. INTyy is held pending and is acknowledged after one instruction of the main servicing has been executed.

××PR = 0: High-priority interrupt
××PR = 1: Low-priority interrupt
IE = 0: Acknowledgement of interrupt request is disabled

Figure 13-13. Nesting Example (2/2)

Example 3. Nesting is not generated because interrupts are not enabled



Because interrupts are not enabled (the EI instruction is not issued) in interrupt servicing INTxx, interrupt request INTyy is not acknowledged, and therefore, the interrupt is not nested. INTyy request is held pending, and is acknowledged after main processing one instruction has been executed.

××PR = 0: High priority level
IE = 0: Acknowledgement of interrupt request is enabled

13.4.5 Pending interrupt request

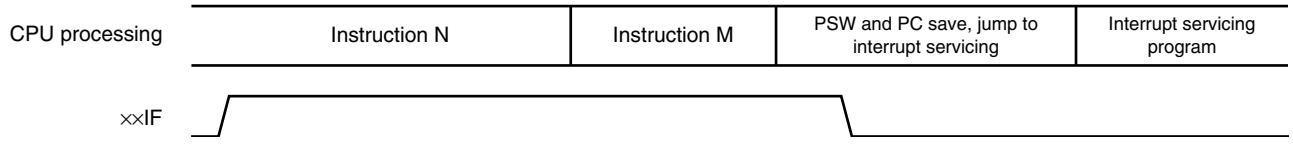
Some instructions may hold the acknowledgement of an interrupt request pending until the completion of the execution of the next instruction even if the interrupt request is generated during the execution of that instruction. These instructions (interrupt request hold instructions) are shown below.

- MOV PSW, #byte
- MOV A, PSW
- MOV PSW, A
- MOV1 PSW.bit, CY
- MOV1 CY, PSW.bit
- AND1 CY, PSW.bit
- OR1 CY, PSW.bit
- XOR1 CY, PSW.bit
- SET1 PSW.bit
- CLR1 PSW.bit
- RETB
- RETI
- PUSH PSW
- POP PSW
- BT PSW.bit, $addr16
- BF PSW.bit, $addr16
- BTCLR PSW.bit, $addr16
- EI
- DI
- Manipulation instructions for IF0L, IF0H, MK0L, MK0H, PR0L, PR0H, and INTM0 registers

Caution The BRK instruction is not one of the above-listed instructions that have interrupt requests held pending. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared to 0. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged. However, the non-maskable interrupt request is acknowledged.

Figure 13-14 shows the timing at which an interrupt request is held pending.

Figure 13-14. Pending Interrupt Request



Remarks 1. Instruction N: Interrupt request hold instruction

2. Instruction M: Instruction except interrupt request hold instructions

3. Operation of ××IF (interrupt request) is not effected by ××PR (priority level) value.

CHAPTER 14 STANDBY FUNCTION

14.1 Standby Function and Configuration

14.1.1 Standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. The HALT mode is intended to stop the CPU operation clock. The system clock oscillator continues oscillating. In this mode, the power consumption cannot be decreased as in the STOP mode. The HALT mode is valid to restart immediately upon interrupt request and to carry out intermittent operations like clock operations.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the main system clock oscillator stops and the whole system stops. The CPU power consumption can be considerably decreased.

Data memory low-voltage hold (down to V_{DD} = 2 V) is possible. Thus, the STOP mode is effective to hold data memory contents with ultra-low power consumption. Because this mode can be cleared upon interrupt request, it enables intermittent operations to be carried out.

However, because a wait time is necessary to secure the oscillation stabilization time after the STOP mode is cleared, select the HALT mode if it is necessary to start processing immediately upon interrupt request.

In any mode, all the contents of the register, flag and data memory just before standby mode setting are held. The I/O port output latch and output buffer statuses are also held.

★ **Cautions 1. When proceeding to the STOP mode, be sure to stop the peripheral hardware operating on the main system clock and then execute the STOP instruction.**

2. In order to reduce the power consumption in the A/D converter, clear bit 7 (CS0) of A/D converter mode register 0 (ADM0) to 0 and stop A/D conversion before executing a HALT or STOP instruction.

14.1.2 Standby function control register

The wait time after the STOP mode is cleared upon interrupt request until the oscillation stabilizes is controlled with the oscillation stabilization time select register (OSTS).

OSTS is set by an 8-bit memory manipulation instruction.

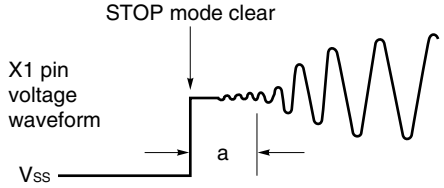
$\overline{\text{RESET}}$ input sets OSTS to 04H. Therefore, when the STOP mode is cleared with $\overline{\text{RESET}}$ input, the time until it is cleared is 2^{17}/fx.

Figure 14-1. Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selects oscillation stabilization time at STOP mode release
0	0	0	2^{12}/fx (819 μs)
0	0	1	2^{14}/fx (3.28 ms)
0	1	0	2^{15}/fx (6.55 ms)
0	1	1	2^{16}/fx (13.1 ms)
1	0	0	2^{17}/fx (26.2 ms)
Other			Setting prohibited

Caution The wait time after STOP mode clear does not include the time (see "a" below) from STOP mode clear to clock oscillation start, regardless of clearance by $\overline{\text{RESET}}$ input or by interrupt request generation.



Remarks 1. fx: Main system clock frequency

2. ( ): fx = 5.0 MHz

14.2 Standby Function Operations

14.2.1 HALT mode

(1) HALT mode set and operating status

The HALT mode is set by executing the HALT instruction.

The operating status in the HALT mode is described below.

Table 14-1. HALT Mode Operating Status

Item	Operating Status
Clock generator	Oscillation enabled. Clock supply to the CPU stops.
CPU	Operation stop.
Port (output latch)	Status before HALT instruction execution is held.
8-bit remote control timer 9	Operation enabled.
8-bit timers 80, 81	
Watchdog timer	
A/D converter	
Serial interface SIO1, SIO3	
VFD controller/driver	Operation disabled.
External interrupt request	Operation enabled.

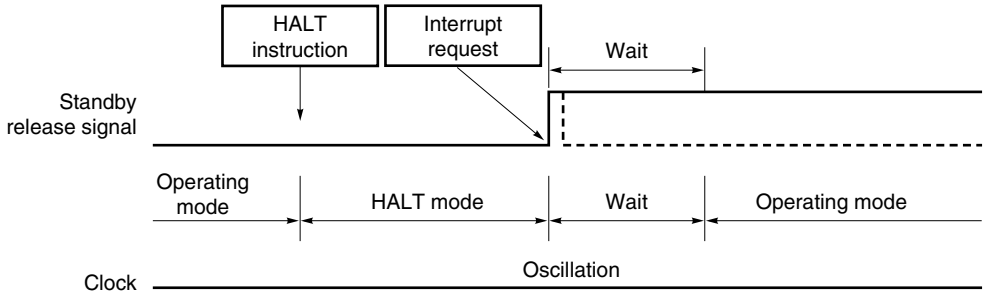
(2) Releasing HALT mode

The HALT mode can be released with the following three types of sources.

(a) Releasing by unmasked interrupt request

The HALT mode is released by an unmasked interrupt request. In this case, if the interrupt request is enabled to be acknowledged, vectored interrupt servicing is performed. If interrupt acknowledgement is disabled, the instruction at the next address is executed.

Figure 14-2. HALT Mode Release by Interrupt Request Generation



Remarks 1. The broken line indicates the case when the interrupt request which has released the standby status is acknowledged.

2. Wait time will be as follows.

- When vectored interrupt servicing is performed: 8 to 9 clocks
- When vectored interrupt servicing is not performed: 2 to 3 clocks

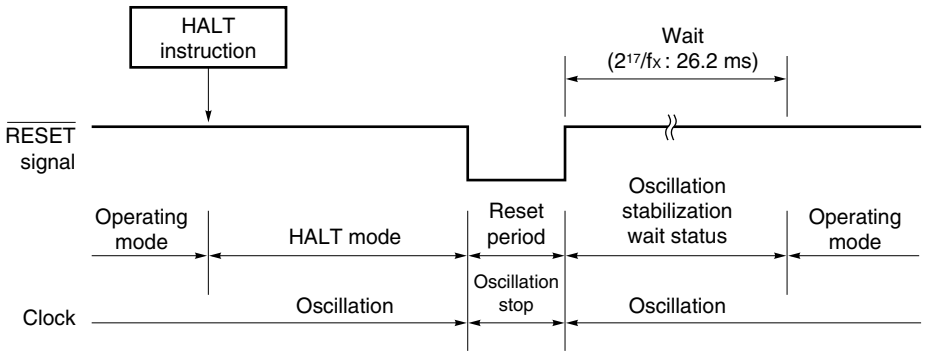
(b) Releasing by non-maskable interrupt request

The HALT mode is released regardless of whether interrupts are enabled or disabled, and vectored interrupt servicing is performed.

(c) Releasing by $\overline{\text{RESET}}$ input

When the HALT mode is released by the $\overline{\text{RESET}}$ signal, execution branches to the reset vector address in the same manner as the ordinary reset operation, and program execution is started.

Figure 14-3. HALT Mode Release by $\overline{\text{RESET}}$ Input



Remarks 1. fx: Main system clock oscillation frequency

2. Figures in parentheses apply to operation with fx = 5.0 MHz.

Table 14-2. Operation After HALT Mode Release

Release Source	××MK	××PR	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode hold
Non-maskable interrupt request	—	—	×	×	Interrupt servicing execution
$\overline{\text{RESET}}$ input	—	—	×	×	Reset processing

×: Don't care

14.2.2 STOP mode

(1) STOP mode set and operating status

The STOP mode is set by executing the STOP instruction.

Cautions 1. When the STOP mode is set, the X2 pin is internally pulled up to V_{DD1} to suppress the leakage at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

The operating status in the STOP mode is described below.

Table 14-3. STOP Mode Operating Status

Item	Operating Status
Clock generator	Oscillation stop.
CPU	Operation stop.
Output port (output latch)	Status before STOP mode setting is held.
8-bit remote control timer 9	Operation stop.
8-bit timers 80, 81	
Watchdog timer	
A/D converter	
Serial interface SIO1, SIO3	Operation enabled only when external input clock is selected as serial clock.
VFD controller/driver	Operation disabled.
External interrupt request	Operation enabled.

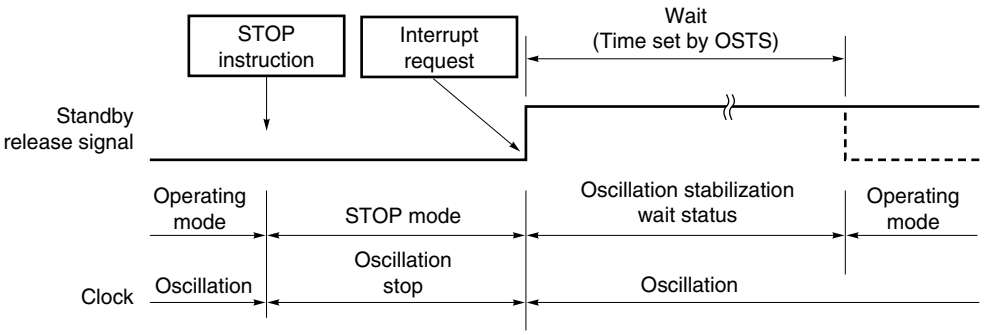
(2) Releasing STOP mode

The STOP mode can be cleared with the following two types of sources.

(a) Releasing by unmasked interrupt request

The STOP mode can be released by an unmasked interrupt request. In this case, if the interrupt is enabled to be acknowledged, vectored interrupt servicing is performed, after the oscillation stabilization time has elapsed. If interrupt acknowledgement is disabled, the instruction at the next address is executed.

Figure 14-4. STOP Mode Release by Interrupt Request Generation

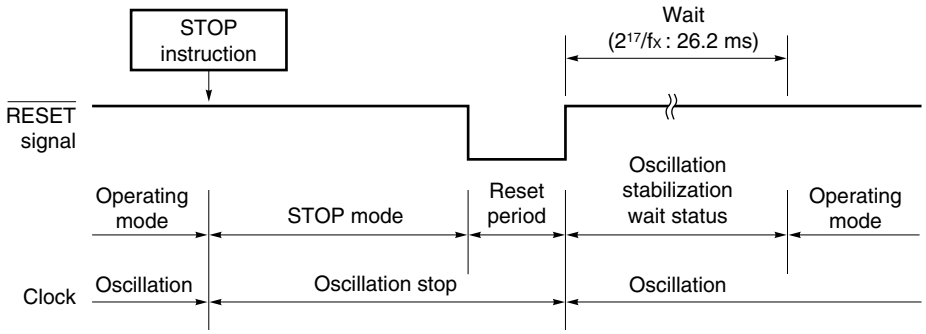


Remark The broken line indicates the case when the interrupt request which has cleared the standby status is acknowledged.

(b) Releasing by $\overline{\text{RESET}}$ input

When the STOP mode is released by the $\overline{\text{RESET}}$ signal, the reset operation is performed after the oscillation stabilization time has elapsed.

Figure 14-5. STOP Mode Release by $\overline{\text{RESET}}$ Input



Remarks 1. fx: Main system clock oscillation frequency

2. Figures in parentheses apply to operation with fx = 5.0 MHz.

Table 14-4. Operation After STOP Mode Release

Release Source	××MK	××PR	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	STOP mode hold
$\overline{\text{RESET}}$ input	—	—	×	×	Reset processing

×: Don't care

CHAPTER 15 RESET FUNCTION

15.1 Reset Function

The following two operations are available to generate the reset signal.

(1) External reset input with $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer overrun time detection

External reset and internal reset have no functional differences. In both cases, program execution starts at address 0000H or 0001H by $\overline{\text{RESET}}$ input.

When a low level is input to the $\overline{\text{RESET}}$ pin or the watchdog timer overflows, a reset is applied and each hardware is set to the status as shown in Table 15-1. Each pin has high impedance during reset input or during oscillation stabilization time just after reset clear.

When a high level is input to the $\overline{\text{RESET}}$ pin, the reset is cleared and program execution starts after the lapse of oscillation stabilization time (2^{17}/fx). The reset applied by watchdog timer overflow is automatically cleared after a reset and program execution starts after the lapse of oscillation stabilization time (2^{17}/fx) (refer to **Figures 15-2** to **15-4**).

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.
2. When the STOP mode is cleared by reset, the STOP mode contents are held during reset input. However, the port pin becomes high-impedance.

Figure 15-1. Block Diagram of Reset Function

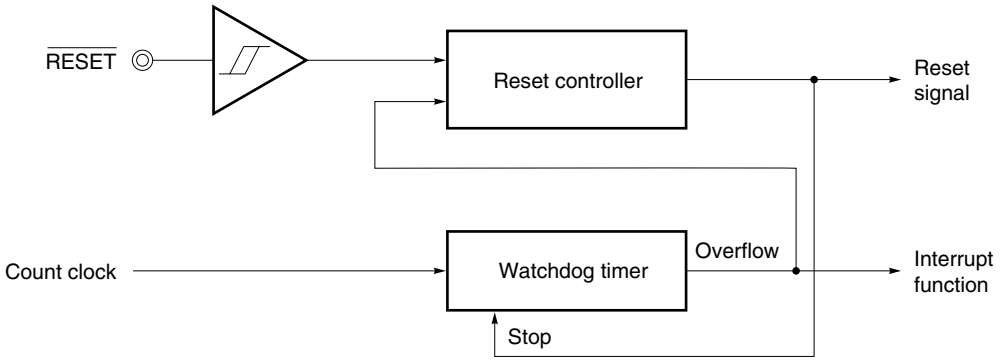


Figure 15-2. Timing of Reset Input by $\overline{\text{RESET}}$ Input

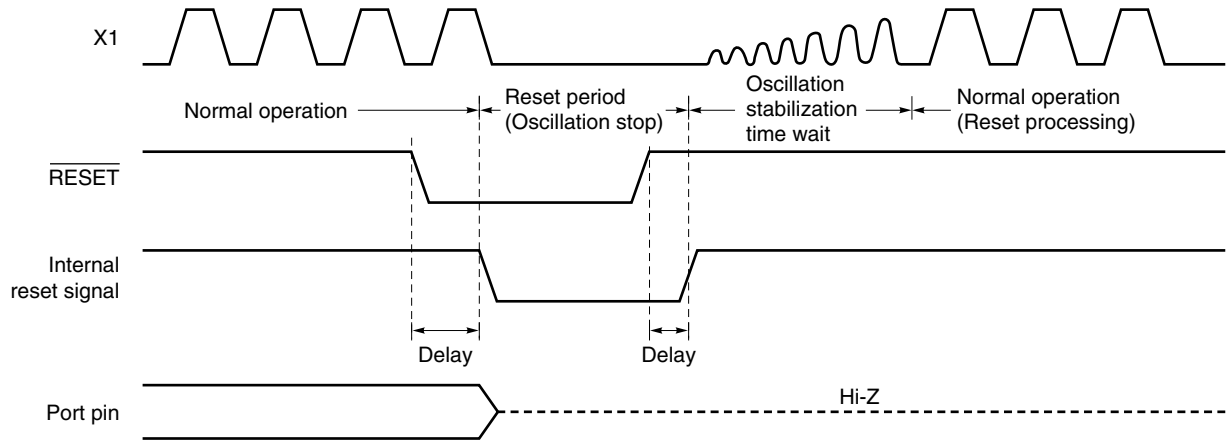


Figure 15-3. Timing of Reset Due to Watchdog Timer Overflow

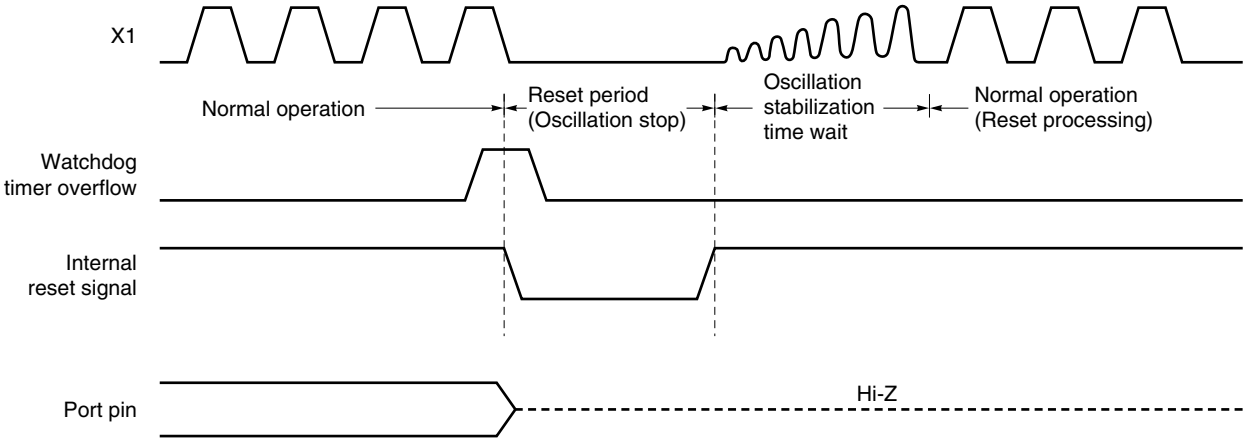


Figure 15-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input

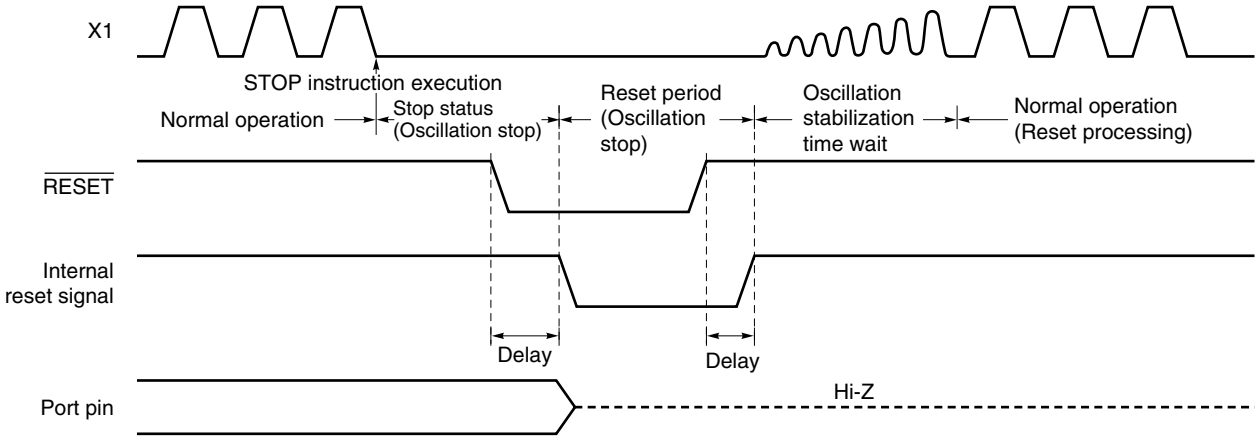


Table 15-1. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC)[Note 1]		Contents of reset vector table (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose register	Undefined[Note 2]
Port (output latch)	Ports 0, ports 2 to 6 (P0, P2 to P6)	00H
Port level read register (PT5, PT6)		Undefined
Port mode register (PM0, PM2)		FFH
Pull-up resistor option register (PU0, PU2)		00H
Processor clock control register (PCC)		04H
Memory size select register (IMS)		CFH[Note 3]
Oscillation stabilization time select register (OSTS)		04H
8-bit remote control timer	Capture registers 90, 91 (CP90, CP91)	00H
	Mode control register 9 (TMC9)	00H
8-bit timer	Compare registers 80, 81 (CR80, CR81)	00H
	Mode control registers 80, 81 (TMC80, TMC81)	00H
Watchdog timer	Clock select register (WDCS)	00H
	Mode register (WDTM)	00H
A/D converter	Conversion result register 0 (ADCR0)	Undefined
	Mode register 0 (ADM0)	00H
	Analog input channel specification register 0 (ADS0)	00H
Serial interface SIO3	Shift register 3 (SIO3)	Undefined
	Mode register 3 (CSIM3)	00H
Serial interface SIO1	Shift register 1 (SIO1)	00H
	Mode register 1 (CSIM1)	00H
	Automatic data transmit/receive address pointer (ADTP)	Undefined
	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive interval specification register (ADTI)	00H

Notes 1. Of the hardware units, only the contents of the PC are undefined during reset input or oscillation stabilization time wait. The statuses of the other hardware units are the same as those after reset.

2. The status after reset is retained in the standby mode.

3. After reset, be sure to set this bit as follows.

- μPD780232: 04H
- ★ μPD780233: 06H
- μPD78F0233: The value corresponding to the mask ROM model

Table 15-1. Hardware Status After Reset (2/2)

Hardware		Status After Reset
VFD controller/driver	Display mode register 0 (DSPM0)	10H
	Display mode register 1 (DSPM1)	01H
	Display mode register 2 (DSPM2)	00H
Interrupt	External interrupt rising edge enable register (EGP)	00H
	External interrupt falling edge enable register (EGN)	00H
	Request flag registers (IF0L, IF0H)	00H
	Mask flag registers (MK0L, MK0H)	FFH
	Priority specification flag registers (PR0L, PR0H)	FFH

CHAPTER 16 μPD78F0233

The μPD78F0233 has a flash memory to which a program can be written or whose contents can be erased with the device mounted on the PC board of the target system. Table 16-1 shows the differences between the flash memory model (μPD78F0233) and mask ROM models (μPD780232, 780233).

★ **Table 16-1. Differences Between μPD78F0233 and Mask ROM Models**

Item	μPD78F0233	μPD780232	μPD780233
Internal ROM structure	Flash memory	Mask ROM	
Internal ROM capacity	24 KB[Note]	16 KB	24 KB
Changing internal ROM capacity by memory size select register (IMS)	Possible	Impossible	
IC pin	Not provided	Provided	
V_{PP} pin	Provided	Not provided	
Pull-down resistor of FIP0 to FIP23 pins	Provided	Selected by mask option	
Pull-down resistor of P30/FIP24 to P37/FIP31, P40/FIP32 to P47/FIP39, P50/FIP40 to P57/FIP47, P60/FIP48 to P64/FIP52 pins	Not provided		
Electrical specifications and recommended soldering conditions	Refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS** and **CHAPTER 20 RECOMMENDED SOLDERING CONDITIONS**.		

Note The same capacity as the mask ROM versions can be specified by means of the memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

16.1 Memory Size Select Register

The μPD78F0233 can select the internal memory capacities by using the memory size select register (IMS). By setting IMS, the memory mapping of the μPD78F0233 can be made the same as that of a mask ROM model with different internal memory capacities.

IMS is set by using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input set IMS to CFH.

Caution As an initial value of the program, be sure to set IMS to a value shown in Figure 16-1. After reset, IMS becomes CFH, therefore, be sure to set IMS to a value of the target mask ROM model after reset.

Figure 16-1. Format of Memory Size Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	0	0	768 bytes
Other			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	1	0	0	16 KB
0	1	1	0	24 KB
Other				Setting prohibited

The IMS settings to obtain the same memory map as mask ROM models are shown in Table 16-2.

Table 16-2. Set Value of Memory Size Select Register

Target Mask ROM Model	Set Value of IMS
μPD780232	04H
★ μPD780233	06H

Caution When using the mask ROM versions, be sure to set the value indicated in Table 16-2 to IMS.

★ 16.2 Flash Memory Features

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV (part no. FL-PR4, PG-FP4)) to the target system with the flash memory mounted on the target system (on-board). A flash memory writing adapter (program adapter), which is a target board used exclusively for programming, is also provided.

Remark FL-PR3, FL-PR4, and the program adapter are the products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities low-quantity, varied model production
- Easy data adjustment when starting mass production

16.2.1 Programming environment

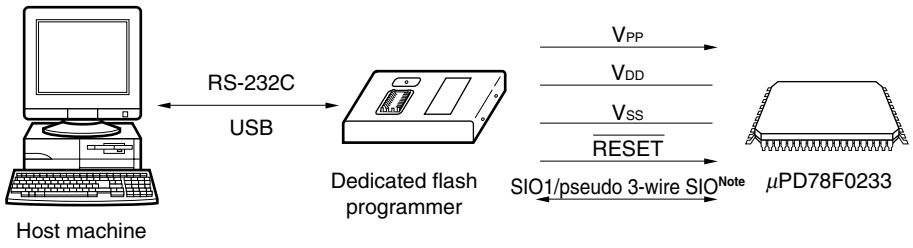
The following shows the environment required for μPD78F0233 flash memory programming.

When Flashpro III or Flashpro IV is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev. 1.1).

For details, refer to the manuals for Flashpro III/Flashpro IV.

Remark USB is supported by Flashpro IV only.

Figure 16-2. Environment for Writing Program to Flash Memory



Note Serial transfer is performed by controlling the port with software.

16.2.2 Communication mode

Use the communication mode shown in Table 16-3 to perform communication between the dedicated flash programmer and μPD78F0233.

Table 16-3. Communication Mode List

Communication Mode	Standard (TYPE) Setting[Note 1]					Pins Used	Number of V_{PP} Pulses
	Port (COMM PORT)	Speed (SIO CLOCK)	On Target (CPU CLOCK)	Frequency (Flashpro Clock)	Multiply Rate (Multiple Rate)		
3-wire serial I/O (SIO1)	SIO-ch0 (SIO ch-0)	2.4 to 625 kHz[Note 2] (100 Hz to 1.25 MHz)[Note 2]	Setting	1 to 5 MHz [Note 2]	1.0	SI1/P26 SO1/P25 $\overline{SCK1}$/P27	0
Pseudo 3-wire serial I/O	Port-ch0 (Port A)	100 to 1000 Hz[Note 2]	Setting	1 to 5 MHz [Note 2]	1.0	P22 (SI) P21 (SO) P20 ($\overline{SCK}$)	12

Notes 1. Selection items for Standard settings on the Flashpro IV TYPE settings on Flashpro III.

2. The possible setting range differs depending on the voltage. For details, refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS**.

Remark The items in parentheses indicate the set values and items of Flashpro III when they differ from the settings of Flashpro IV.

Figure 16-3. Communication Mode Selection Format

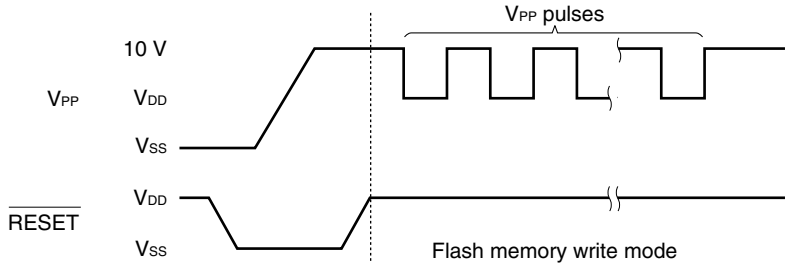
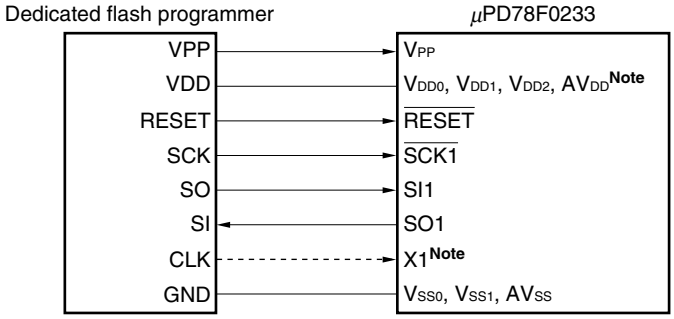
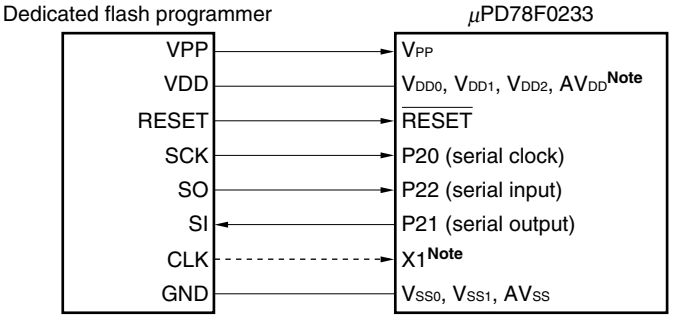


Figure 16-4. Example of Connection with Dedicated Flash Programmer

(a) 3-wire serial I/O (SIO1)



(b) Pseudo 3-wire serial I/O



Note The power can be supplied to the V_{DD0}, V_{DD1}, V_{DD2}, AV_{DD}, and X1 pins on the board. In this case, although it is not required to connect the dedicated flash programmer, VDD voltage must be supplied before programming is started.

If Flashpro III or Flashpro IV is used as a dedicated flash programmer, the following signals are generated for the μPD78F0233. For details, refer to the manual of Flashpro III/Flashpro IV.

Table 16-4. Pin Connection List

Signal Name	I/O	Pin Function	Pin Name	SIO1	Pseudo 3-Wire
VPP	Output	Write voltage	V_{PP}	◎	◎
VDD	I/O	V_{DD} voltage generation/ voltage monitoring	V_{DD0}, V_{DD1}, V_{DD2}, AV_{DD}	○**Note**	○**Note**
GND	–	Ground	V_{SS0}, V_{SS1}, AV_{SS}	◎	◎
CLK	Output	Clock output	X1	○	○
RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎	◎
SI	Input	Reception signal	SO1, P21	◎	◎
SO	Output	Transmit signal	SI1, P22	◎	◎
SCK	Output	Transfer clock	$\overline{\text{SCK1}}$, P20	◎	◎

Note V_{DD} voltage must be supplied before programming is started.

Remark ◎: Pin must be connected.
○: If the signal is supplied on the target board, pin need not be connected.

16.2.3 On-board pin processing

When performing programming on the target system, provide a connector on the target system to connect the dedicated flash programmer.

An on-board function that allows switching between normal operation mode and flash memory programming mode may be required in some cases.

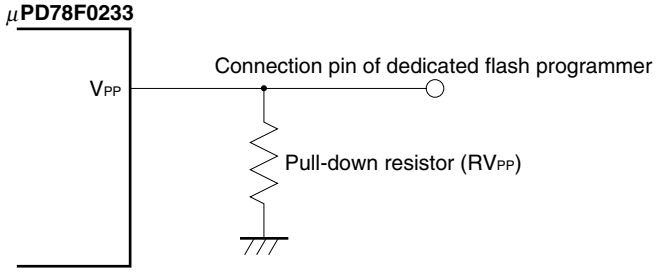
<V_{PP} pin>

In normal operation mode, input 0 V to the V_{PP} pin. In flash memory programming mode, a write voltage of 10.0 V (TYP.) is supplied to the V_{PP} pin, so perform the following.

(1) Connect a pull-down resistor (RV_{PP} = 10 kΩ) to the V_{PP} pin.
(2) Use the jumper on the board to switch the V_{PP} pin input to either the writer or directly to GND.

A V_{PP} pin connection example is shown below.

Figure 16-5. V_{PP} Pin Connection Example



<Serial interface pin>

The following shows the pins used by the serial interface.

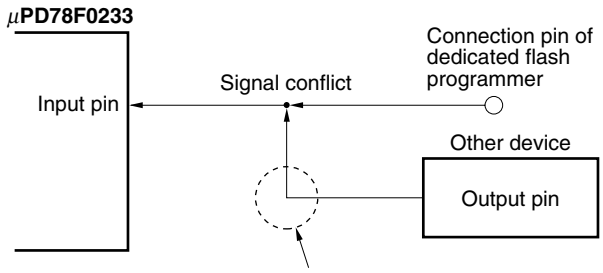
Serial Interface	Pins Used
3-wire serial I/O (SIO1)	SI1, SO1, $\overline{SCK1}$
pseudo 3-wire serial I/O	P20, P21, P22

When connecting the dedicated flash programmer to a serial interface pin that is connected to another device on-board, signal conflict or abnormal operation of the other devices may occur. Care must therefore be taken with such connections.

(1) Signal conflict

If the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a signal conflict occurs. To prevent this, isolate the connection with the other device or set the other device to the output high impedance status.

Figure 16-6. Signal Conflict (Input Pin of Serial Interface)

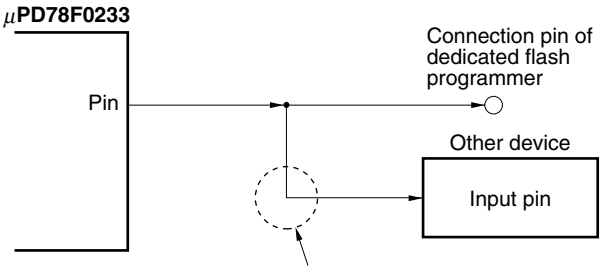


In the flash memory programming mode, the signal output by another device and the signal sent by the dedicated flash programmer conflict, therefore, isolate the signal of the other device.

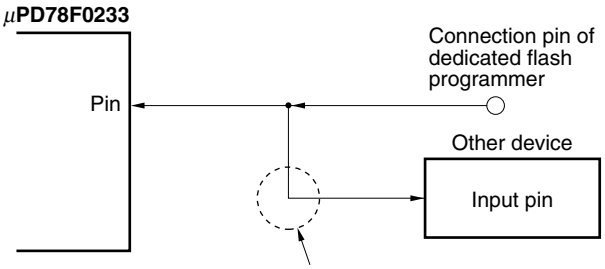
(2) Abnormal operation of other device

If the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), a signal is output to the device, and this may cause an abnormal operation. To prevent this abnormal operation, isolate the connection with the other device or set so that the input signals to the other device are ignored.

Figure 16-7. Abnormal Operation of Other Device



If the signal output by the μPD78F0233 affects another device in the flash memory programming mode, isolate the signals of the other device.

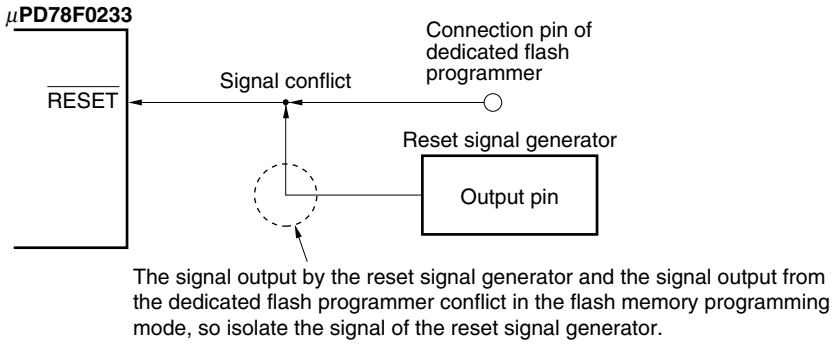


If the signal output by the dedicated flash programmer affects another device in the flash memory programming mode, isolate the signals of the other device.

<$\overline{\text{RESET}}$ pin>

If the reset signal of the dedicated flash programmer is connected to the $\overline{\text{RESET}}$ pin connected to the reset signal generator on-board, a signal conflict occurs. To prevent this, isolate the connection with the reset signal generator. If the reset signal is input from the user system in the flash memory programming mode, a normal programming operation cannot be performed. Therefore, do not input reset signals from other than the dedicated flash programmer.

Figure 16-8. Signal Conflict ($\overline{\text{RESET}}$ Pin)



<Port pins>

When the μPD78F0233 enters the flash memory programming mode, all the pins other than those that communicate in flash memory programming are in the same status as immediately after reset.

If the external device does not recognize initial statuses such as the output high impedance status, therefore, connect the external device to V_{DD0} or V_{SS0} via a resistor.

<Oscillator>

When using the on-board clock, connect X1 and X2 as required in the normal operation mode.

When using the clock output of the flash programmer, connect it directly to X1, disconnecting the main oscillator on-board, and leave the X2 pin open.

<Power supply>

To use the power output from the flash programmer, connect the V_{DD0}, V_{DD1}, and V_{DD2} pins to VDD of the flash programmer, and the V_{SS0} and V_{SS1} pins to GND of the flash programmer.

To use the on-board power supply, make connections that accord with the normal operation mode. However, because the voltage is monitored by the flash programmer, be sure to connect VDD of the flash programmer.

Supply the same power as in the normal operation mode to the other power supply pins (AV_{DD} and AV_{SS}).

<Other pins>

Process the other pins (FIP0 to FIP23 and ANI0 to ANI3) in the same manner as in the normal operation mode.

16.2.4 Connection of adapter for flash writing

The following figures show the examples of recommended connection when the adapter for flash writing is used.

Figure 16-9. Wiring Example for Flash Writing Adapter with 3-Wire Serial I/O (SIO1)

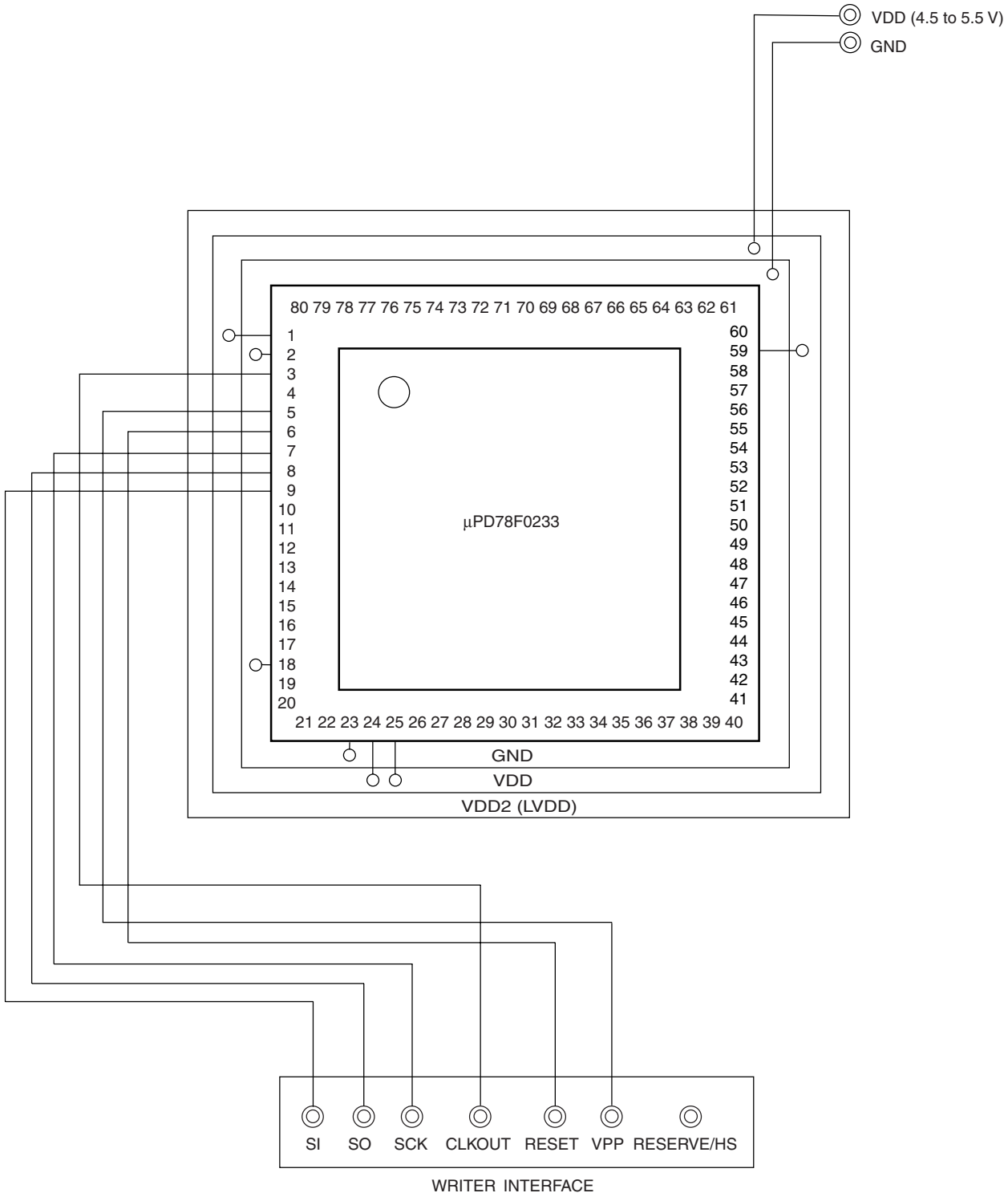
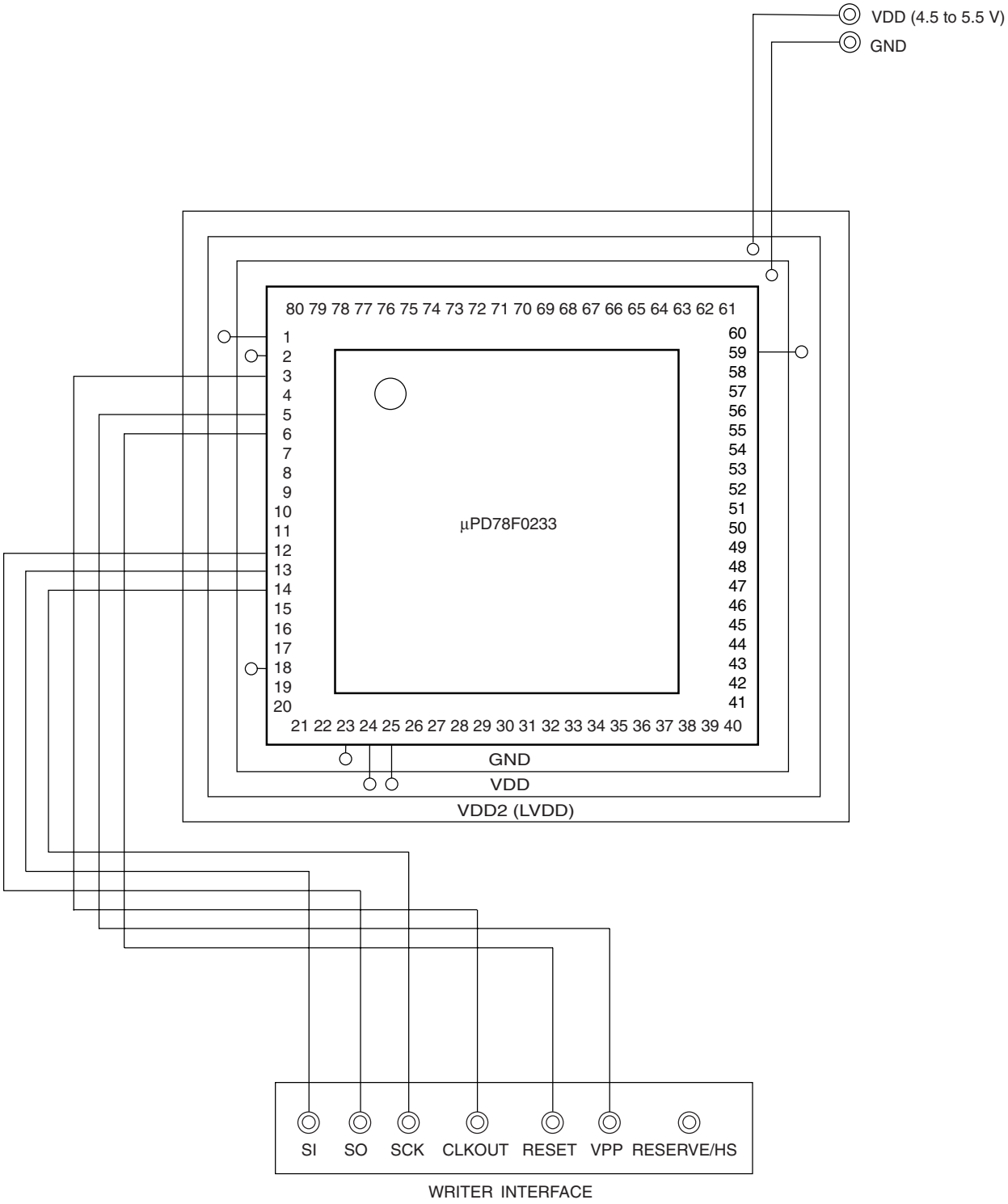


Figure 16-10. Wiring Example for Flash Writing Adapter with Pseudo 3-Wire Serial I/O



CHAPTER 17 INSTRUCTION SET

The instruction set for the μPD780232 Subseries is described in the following pages. For the details of operations and mnemonics (instruction codes) of each instruction, refer to **78K/0 Series Instructions User's Manual (U12326E)**.

17.1 Legend

17.1.1 Operand identifiers and methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more specification methods, select one of them. Alphabetic letters in capitals and symbols, #, !, $ and [ ] are key words and are written as they are. Symbols have the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, write an appropriate numeric value or a label. When using a label, be sure to write the #, !, $ and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 17-1. Operand Identifiers and Explanation

Identifier	Explanation
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbols (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even addresses only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note FFD0H to FFDFH are not addressable.

Remark For special function register symbols, refer to **Table 3-3 Special Function Registers**.

17.1.2 Description of “operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
RBS:	Register bank select flag
IE:	Interrupt request enable flag
NMIS:	Non-maskable interrupt servicing flag
( ):	Memory contents indicated by address or register contents in parentheses
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$:	Logical product (AND)
$\vee$:	Logical sum (OR)
$\veebar$:	Exclusive logical sum (exclusive OR)
$\overline{\quad}$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

17.1.3 Description of “flag operation” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
x:	Set/cleared according to the result
R:	Previously saved value is restored

17.2 Operation List

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	r, #byte	2	4	—	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	—	7	sfr ← byte	
		A, r Note 3	1	2	—	A ← r	
		r, A Note 3	1	2	—	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	—	5	A ← sfr	
		sfr, A	2	—	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	—	7	PSW ← byte	× × ×
		A, PSW	2	—	5	A ← PSW	
		PSW, A	2	—	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL+byte]	2	8	9	A ← (HL + byte)	
		[HL+byte], A	2	8	9	(HL + byte) ← A	
		A, [HL+B]	1	6	7	A ← (HL + B)	
		[HL+B], A	1	6	7	(HL + B) ← A	
		A, [HL+C]	1	6	7	A ← (HL + C)	
		[HL+C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	—	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	—	6	A ↔ sfr	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL+byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL+B]	2	8	10	A ↔ (HL + B)	
		A, [HL+C]	2	8	10	A ↔ (HL + C)	

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except r = A

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	MOVW	rp, #word	3	6	—	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	—	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	—	8	AX ← sfrp	
		sfrp, AX	2	—	8	sfrp ← AX	
		AX, rp Note 3	1	4	—	AX ← rp	
		rp, AX Note 3	1	4	—	rp ← AX	
		AX, !addr16	3	10	12	AX ← (addr16)	
		!addr16, AX	3	10	12	(addr16) ← AX	
	XCHW	AX, rp Note 3	1	4	—	AX ↔ rp	
8-bit operation	ADD	A, #byte	2	4	—	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r Note 4	2	4	—	A, CY ← A + r	× × ×
		r, A	2	4	—	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL)	× × ×
		A, [HL+byte]	2	8	9	A, CY ← A + (HL + byte)	× × ×
		A, [HL+B]	2	8	9	A, CY ← A + (HL + B)	× × ×
		A, [HL+C]	2	8	9	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	—	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r Note 4	2	4	—	A, CY ← A + r + CY	× × ×
		r, A	2	4	—	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + CY	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	× × ×
		A, [HL+byte]	2	8	9	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL+B]	2	8	9	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL+C]	2	8	9	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE or HL

4. Except r = A

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	SUB	A, #byte	2	4	—	A, CY ← A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	×	×	×
		A, r Note 3	2	4	—	A, CY ← A – r	×	×	×
		r, A	2	4	—	r, CY ← r – A	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr)	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL)	×	×	×
		A, [HL+byte]	2	8	9	A, CY ← A – (HL + byte)	×	×	×
		A, [HL+B]	2	8	9	A, CY ← A – (HL + B)	×	×	×
		A, [HL+C]	2	8	9	A, CY ← A – (HL + C)	×	×	×
	SUBC	A, #byte	2	4	—	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	4	—	A, CY ← A – r – CY	×	×	×
		r, A	2	4	—	r, CY ← r – A – CY	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	×	×	×
		A, [HL+byte]	2	8	9	A, CY ← A – (HL + byte) – CY	×	×	×
		A, [HL+B]	2	8	9	A, CY ← A – (HL + B) – CY	×	×	×
		A, [HL+C]	2	8	9	A, CY ← A – (HL + C) – CY	×	×	×
	AND	A, #byte	2	4	—	A ← A ∧ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	4	—	A ← A ∧ r	×		
		r, A	2	4	—	r ← r ∧ A	×		
		A, saddr	2	4	5	A ← A ∧ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∧ (HL)	×		
		A, [HL+byte]	2	8	9	A ← A ∧ (HL + byte)	×		
		A, [HL+B]	2	8	9	A ← A ∧ (HL + B)	×		
		A, [HL+C]	2	8	9	A ← A ∧ (HL + C)	×		

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except r = A

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	OR	A, #byte	2	4	—	A ← A ∨ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	4	—	A ← A ∨ r	×		
		r, A	2	4	—	r ← r ∨ A	×		
		A, saddr	2	4	5	A ← A ∨ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∨ (HL)	×		
		A, [HL+byte]	2	8	9	A ← A ∨ (HL + byte)	×		
		A, [HL+B]	2	8	9	A ← A ∨ (HL + B)	×		
		A, [HL+C]	2	8	9	A ← A ∨ (HL + C)	×		
	XOR	A, #byte	2	4	—	A ← A ∨̄ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	4	—	A ← A ∨̄ r	×		
		r, A	2	4	—	r ← r ∨̄ A	×		
		A, saddr	2	4	5	A ← A ∨̄ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∨̄ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∨̄ (HL)	×		
		A, [HL+byte]	2	8	9	A ← A ∨̄ (HL + byte)	×		
		A, [HL+B]	2	8	9	A ← A ∨̄ (HL + B)	×		
		A, [HL+C]	2	8	9	A ← A ∨̄ (HL + C)	×		
	CMP	A, #byte	2	4	—	A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr) – byte	×	×	×
		A, r Note 3	2	4	—	A – r	×	×	×
		r, A	2	4	—	r – A	×	×	×
		A, saddr	2	4	5	A – (saddr)	×	×	×
		A, !addr16	3	8	9	A – (addr16)	×	×	×
		A, [HL]	1	4	5	A – (HL)	×	×	×
		A, [HL+byte]	2	8	9	A – (HL + byte)	×	×	×
		A, [HL+B]	2	8	9	A – (HL + B)	×	×	×
		A, [HL+C]	2	8	9	A – (HL + C)	×	×	×

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except r = A

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	**ADDW**	AX, #word	3	6	—	AX, CY ← AX + word	×	×	×
	SUBW	AX, #word	3	6	—	AX, CY ← AX – word	×	×	×
	CMPW	AX, #word	3	6	—	AX – word	×	×	×
Multiply/ divide	**MULU**	X	2	16	—	AX ← A × X			
	DIVUW	C	2	25	—	AX (Quotient), C (Remainder) ← AX ÷ C			
Increase/ decrease	**INC**	r	1	2	—	r ← r + 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) + 1	×	×	
	DEC	r	1	2	—	r ← r – 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) – 1	×	×	
	INCW	rp	1	4	—	rp ← rp + 1			
	DECW	rp	1	4	—	rp ← rp – 1			
Rotation	**ROR**	A, 1	1	2	—	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
	ROL	A, 1	1	2	—	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
	RORC	A, 1	1	2	—	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
	ROLC	A, 1	1	2	—	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
	ROR4	[HL}	2	10	12	A_{3-0} ← $(HL)_{3-0}$, ← $(HL)_{7-4}$ ← A_{3-0}, $(HL)_{3-0}$ ← $(HL)_{7-4}$			
	ROL4	[HL]	2	10	12	A_{3-0} ← $(HL)_{7-4}$, ← $(HL)_{3-0}$ ← A_{3-0}, $(HL)_{7-4}$ ← $(HL)_{3-0}$			
BCD correction	**ADJBA**		2	4	—	Decimal Adjust Accumulator after Addition	×	×	×
	ADJBS		2	4	—	Decimal Adjust Accumulator after Subtract	×	×	×
Bit manipulation	**MOV1**	CY, saddr.bit	3	6	7	CY ← (saddr.bit)			×
		CY, sfr.bit	3	—	7	CY ← sfr.bit			×
		CY, A.bit	2	4	—	CY ← A.bit			×
		CY, PSW.bit	3	—	7	CY ← PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← (HL).bit			×
		saddr.bit, CY	3	6	8	(saddr.bit) ← CY			
		sfr.bit, CY	3	—	8	sfr.bit ← CY			
		A.bit, CY	2	4	—	A.bit ← CY			
		PSW.bit, CY	3	—	8	PSW.bit ← CY	×	×	
		[HL].bit, CY	2	6	8	(HL).bit ← CY			

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulation	**AND1**	CY, saddr.bit	3	6	7	CY ← CY ∧ (saddr.bit)			×
		CY, sfr.bit	3	—	7	CY ← CY ∧ sfr.bit			×
		CY, A.bit	2	4	—	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	—	7	CY ← CY ∧ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∧ (HL).bit			×
	OR1	CY, saddr.bit	3	6	7	CY ← CY ∨ (saddr.bit)			×
		CY, sfr.bit	3	—	7	CY ← CY ∨ sfr.bit			×
		CY, A.bit	2	4	—	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	—	7	CY ← CY ∨ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∨ (HL).bit			×
	XOR1	CY, saddr.bit	3	6	7	CY ← CY ⩛ (saddr.bit)			×
		CY, sfr.bit	3	—	7	CY ← CY ⩛ sfr.bit			×
		CY, A.bit	2	4	—	CY ← CY ⩛ A.bit			×
		CY, PSW.bit	3	—	7	CY ← CY ⩛ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ⩛ (HL).bit			×
	SET1	saddr.bit	2	4	6	(saddr.bit) ← 1			
		sfr.bit	3	—	8	sfr.bit ← 1			
		A.bit	2	4	—	A.bit ← 1			
		PSW.bit	2	—	6	PSW.bit ← 1	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 1			
	CLR1	saddr.bit	2	4	6	(saddr.bit) ← 0			
		sfr.bit	3	—	8	sfr.bit ← 0			
		A.bit	2	4	—	A.bit ← 0			
		PSW.bit	2	—	6	PSW.bit ← 0	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 0			
	SET1	CY	1	2	—	CY ← 1			1
	CLR1	CY	1	2	—	CY ← 0			0
	NOT1	CY	1	2	—	CY ← $\overline{CY}$			×

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
Call return	**CALL**	!addr16	3	7	—	(SP – 1) ← (PC + 3)H, (SP – 2) ← (PC + 3)L, PC ← addr16, SP ← SP – 2	
	CALLF	!addr11	2	5	—	(SP – 1) ← (PC + 2)H, (SP – 2) ← (PC + 2)L, PC15–11 ← 00001, PC10–0 ← addr11, SP ← SP – 2	
	CALLT	[addr5]	1	6	—	(SP – 1) ← (PC + 1)H, (SP – 2) ← (PC +1)L, PCH ← (00000000, addr5 + 1), PCL ← (00000000, addr5) SP ← SP – 2	
	BRK		1	6	—	(SP – 1) ← PSW, (SP – 2) ← (PC + 1)H, (SP – 3) ← (PC + 1)L, PCH ← (003FH), PCL ← (003EH), SP ← SP – 3, IE ← 0	
	RET		1	6	—	PCH ← (SP + 1), PCL ← (SP), SP ← SP + 2	
	RETI		1	6	—	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R R R
Stack manipulation	**RETB**		1	6	—	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
	PUSH	PSW	1	2	—	(SP – 1) ← PSW, SP ← SP – 1	
		rp	1	4	—	(SP – 1) ← rpH, (SP – 2) ← rpL, SP ← SP – 2	
	POP	PSW	1	2	—	PSW ← (SP), SP ← SP + 1	R R R
		rp	1	4	—	rpH ← (SP + 1), rpL ← (SP), SP ← SP + 2	
	MOVW	SP, #word	4	—	10	SP ← word	
		SP, AX	2	—	8	SP ← AX	
		AX, SP	2	—	8	AX ← SP	
Unconditional branch	**BR**	!addr16	3	6	—	PC ← addr16	
		$addr16	2	6	—	PC ← PC + 2 jdisp8	
		AX	2	8	—	PCH ← A, PCL ← X	
Conditional branch	**BC**	$addr16	2	6	—	PC ← PC + 2 jdisp8 if CY = 1	
	BNC	$addr16	2	6	—	PC ← PC + 2 jdisp8 if CY = 0	
	BZ	$addr16	2	6	—	PC ← PC + 2 jdisp8 if Z = 1	
	BNZ	$addr16	2	6	—	PC ← PC + 2 jdisp8 if Z = 0	

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
Conditional branch	**BT**	saddr.bit, $addr16	3	8	9	PC ← PC + 3 + jdisp8 if(saddr.bit) = 1	
		sfr.bit, $addr16	4	—	11	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
		A.bit, $addr16	3	8	—	PC ← PC + 3 + jdisp8 if A.bit = 1	
		PSW.bit, $addr16	3	—	9	PC ← PC + 3 + jdisp8 if PSW.bit = 1	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 1	
	BF	saddr.bit, $addr16	4	10	11	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
		sfr.bit, $addr16	4	—	11	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
		A.bit, $addr16	3	8	—	PC ← PC + 3 + jdisp8 if A.bit = 0	
		PSW.bit, $addr16	4	—	11	PC ← PC + 4 + jdisp8 if PSW.bit = 0	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 0	
	BTCLR	saddr.bit, $addr16	4	10	12	PC ← PC + 4 + jdisp8 if(saddr.bit) = 1 then reset (saddr.bit)	
		sfr.bit, $addr16	4	—	12	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit	
		A.bit, $addr16	3	8	—	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit	
		PSW.bit, $addr16	4	—	12	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	× × ×
		[HL].bit.$addr16	3	10	12	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit	
	DBNZ	B, $addr16	2	6	—	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
		C, $addr16	2	6	—	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
		saddr, $addr16	3	8	10	(saddr) ← (saddr) –1 , then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
CPU control	**SEL**	RBn	2	4	—	RBS1, 0 ← n	
	NOP		1	2	—	No Operation	
	EI		2	—	6	IE ← 1 (Enable Interrupt)	
	DI		2	—	6	IE ← 0 (Disable Interrupt)	
	HALT		2	6	—	Set HALT Mode	
	STOP		2	6	—	Set STOP Mode	

Notes 1. When the internal high-speed RAM area is accessed or instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

17.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruciton					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

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CHAPTER 18 ELECTRICAL SPECIFICATIONS

18.1 Electrical Specifications of μPD780232, 78F0233

18.1.1 V_{DD} = 4.5 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}	μPD78F0233[Note 1]		–0.5 to +10.5	V
	V_{LOAD}			V_{DD} – 45 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64 (P-ch open drain)		V_{DD} – 45 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}			V_{DD} – 45 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL}[Note 2]	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T[Note 3]	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}	μPD780232		–40 to +150	°C
	V_{PP}	μPD78F0233		–40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

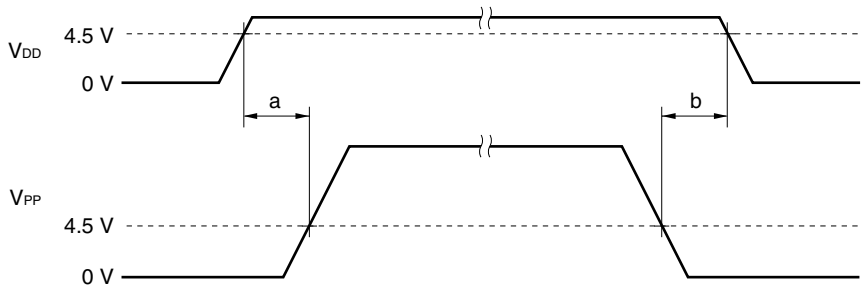
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Note 2. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

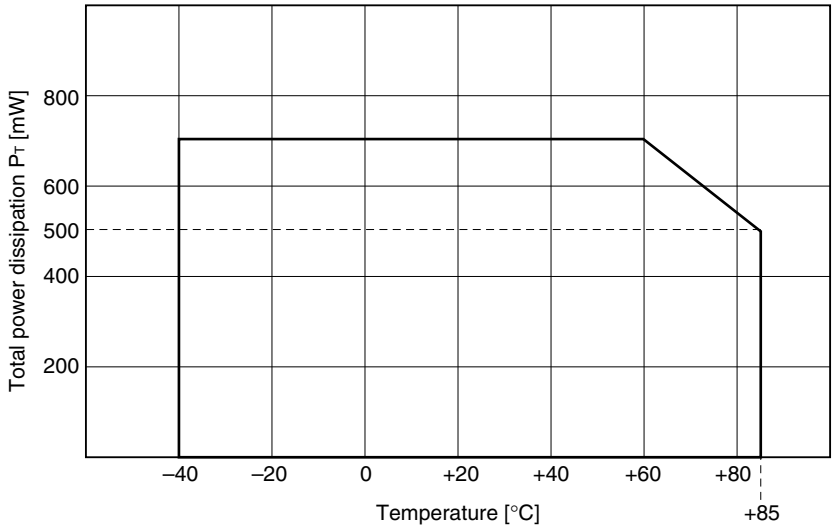
(Note 1 and Note 3 are shown on the following pages.)

Note 1. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (4.5 V) of the operating voltage range (see a in the figure below).
- **When supply voltage drops**
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (4.5 V) of the operating voltage range of V_{DD} (see b in the figure below).



Note 3. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780232 and 78F0233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) $\times$ I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids $\times$ 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} - 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} - 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 36.4\ \text{mW}$$

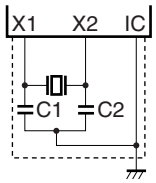
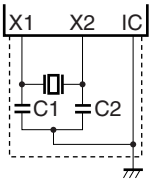
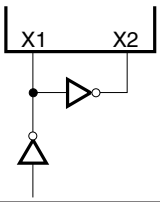
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**				10	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System Clock Ceramic resonator (T_A = –40 to +85°C)

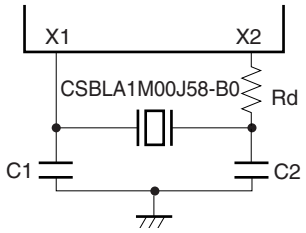
(1) μPD780232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0 (CSB1000J)	1.00	150	150	0	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip			
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

(2) μPD78F0232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0**Note** (CSB1000J)	1.00	100	100	2.2 k	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip	0		
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

Note A limiting resistor (Rd = 2.2 kΩ) is required when CSBLA1M00J58-B0 (1.00 MHz) manufactured by Murata Mfg. Co., Ltd. is used as the ceramic resonator in the μPD78F0233 (see the figure below). This is not necessary when using one of the other recommended resonators.



Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD780232 within the specifications of the DC and AC characteristics.

Remark Part numbers in parentheses are the old part numbers.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52				–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip pull-down resistance	R_2	FIP0 to FIP23 (μPD78F0233 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52 (μPD780232 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64 (μPD780232 only)		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation mode[Note 2]	μPD780232		7	14	mA
			μPD78F0233		9	18	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode	μPD780232		1.5	4.5	mA
			μPD78F0233		2.5	7.5	mA
	I_{DD3}	STOP mode			1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

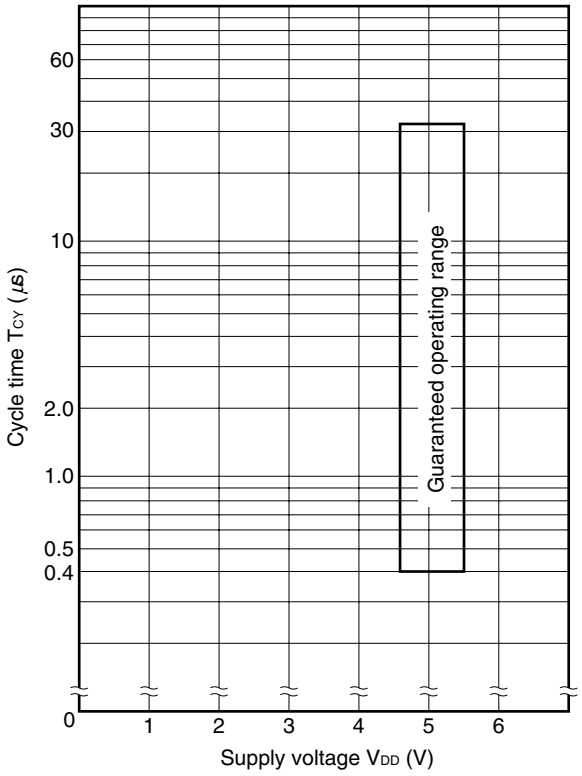
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2[Note]			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Flash Memory Programming Characteristics (μPD78F0233 only, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		1.0		5.0	MHz
Supply voltage	V_{DD}	Operation voltage when writing	4.5		5.5	V
	V_{PP}	Upon V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPH}	Upon V_{PP} high-voltage detection	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} =10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Number of rewrites	C_{WRT}				20	Times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		+10		+40	°C

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from $V_{DD}\uparrow$ to $V_{PP}\uparrow$	t_{DRPSR}	V_{PP} high voltage	10			μs
Set time from $V_{PP}\uparrow$ to $\overline{\text{RESET}}\uparrow$	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

18.1.2 V_{DD} = 3.0 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}	μPD78F0233**Note 1**		–0.5 to +10.5	V
	V_{LOAD}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 45 to V_{DD} + 0.3	V
		(P-ch open drain)	3.0 V ≤ V_{DD} < 4.5 V	V_{DD} – 43 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL}**Note 2**	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T**Note 3**	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}	μPD780232		–40 to +150	°C
	V_{PP}	μPD78F0233		–40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Note 2. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$
(Note 1 and Note 3 are shown on the following pages.)

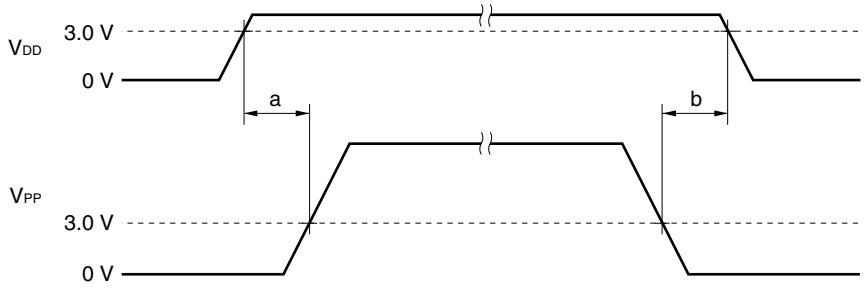
Note 1. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**

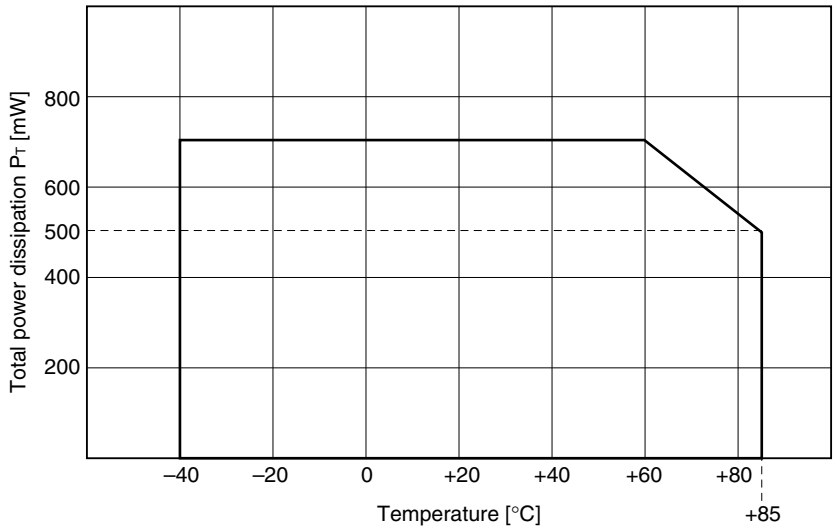
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (3.0 V) of the operating voltage range (see a in the figure below).

- **When supply voltage drops**

  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (3.0 V) of the operating voltage range of V_{DD} (see b in the figure below).



Note 3. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780232 and 78F0233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) $\times$ I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids $\times$ 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 36.4\ \text{mW}$$

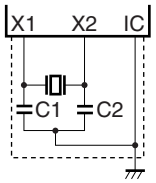
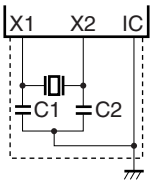
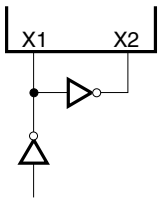
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			10	ms
			3.0 V ≤ V_{DD} < 4.5 V			30	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System Clock Ceramic resonator (T_A = –40 to +85°C)

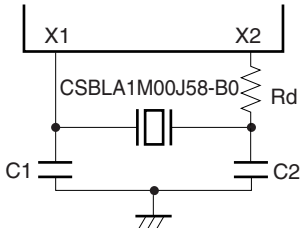
(1) μPD780232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0 (CSB1000J)	1.00	150	150	0	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip			
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

(2) μPD78F0232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0[Note] (CSB1000J)	1.00	100	100	2.2 k	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip	0		
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

Note A limiting resistor (Rd = 2.2 kΩ) is required when CSBLA1M00J58-B0 (1.00 MHz) manufactured by Murata Mfg. Co., Ltd. is used as the ceramic resonator in the μPD78F0233 (see the figure below). This is not necessary when using one of the other recommended resonators.



Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD780232 within the specifications of the DC and AC characteristics.

Remark Part numbers in parentheses are the old part numbers.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52	V_{DD} = 5 V ± 10%			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–10	mA
		FIP20 to FIP52	V_{DD} = 3.3 V ± 0.3 V			–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip pull-down resistance	R_2	FIP0 to FIP23 (μPD78F0233 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52 (μPD780232 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64 (μPD780232 only)		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation mode[Note 2]	μPD780232		7	14	mA
			μPD78F0233		9	18	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode	μPD780232		1.5	4.5	mA
			μPD78F0233		2.5	7.5	mA
	I_{DD3}	STOP mode			1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

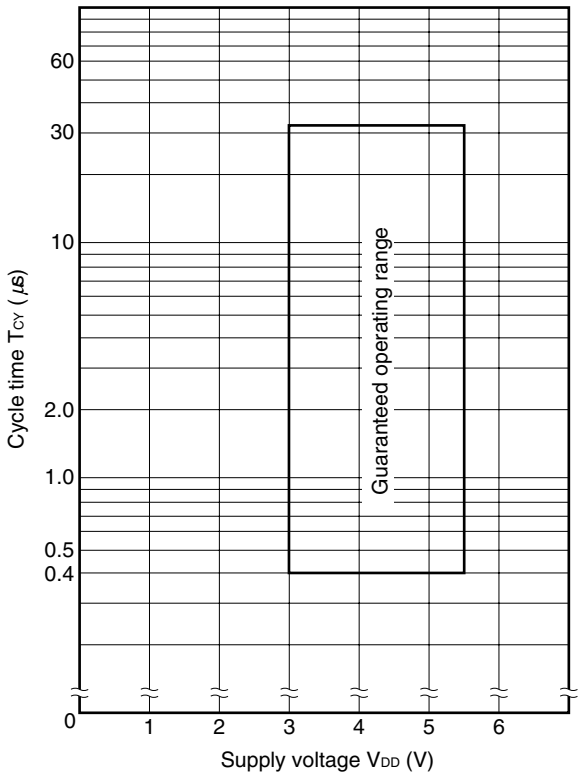
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2 **Note**			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 3.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Flash Memory Programming Characteristics (μPD78F0233 only, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		1.0		5.0	MHz
Supply voltage	V_{DD}	Operation voltage when writing	3.0		5.5	V
	V_{PP}	Upon V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPH}	Upon V_{PP} high-voltage detection	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} =10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Number of rewrites	C_{WRT}				20	Times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		+10		+40	°C

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from $V_{DD}\uparrow$ to $V_{PP}\uparrow$	t_{DRPSR}	V_{PP} high voltage	10			μs
Set time from $V_{PP}\uparrow$ to $\overline{\text{RESET}}\uparrow$	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

18.1.3 V_{DD} = 2.7 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}	μPD78F0233**Note 1**		–0.5 to +10.5	V
	V_{LOAD}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
		2.7 V ≤ V_{DD} < 3.0 V		V_{DD} – 42.7 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64 (P-ch open drain)	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 45 to V_{DD} + 0.3	V
			3.0 V ≤ V_{DD} < 4.5 V	V_{DD} – 43 to V_{DD} + 0.3	V
			2.7 V ≤ V_{DD} < 3.0 V	V_{DD} – 42.7 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
		2.7 V ≤ V_{DD} < 3.0 V		V_{DD} – 42.7 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL}**Note 2**	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T**Note 3**	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}	μPD780232		–40 to +150	°C
	V_{PP}	μPD78F0233		–40 to +125	°C

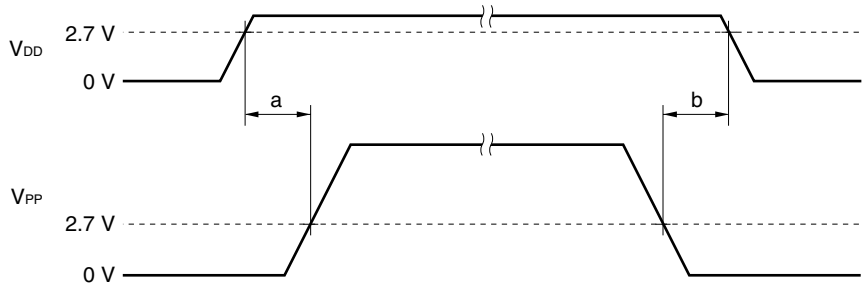
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

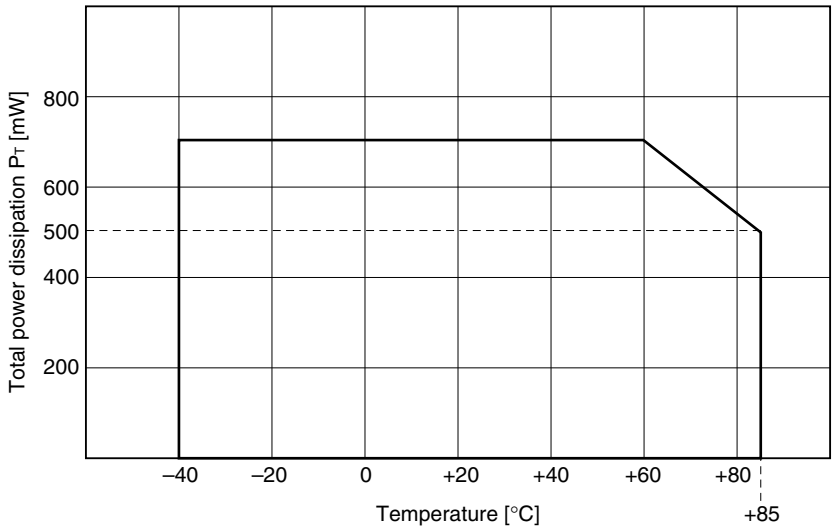
Note 2. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$
(Note 1 and Note 3 are shown on the following pages.)

Note 1. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (2.7 V) of the operating voltage range (see a in the figure below).
- **When supply voltage drops**
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (2.7 V) of the operating voltage range of V_{DD} (see b in the figure below).



Note 3. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780232 and 78F0233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) $\times$ I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids $\times$ 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 36.4\ \text{mW}$$

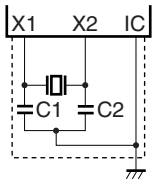
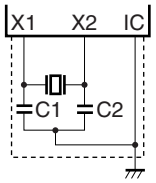
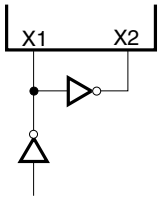
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids + 1}} \times (1 - \frac{1}{16}) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			10	ms
			2.7 V ≤ V_{DD} < 4.5 V			30	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System Clock Ceramic resonator (T_A = –40 to +85°C)

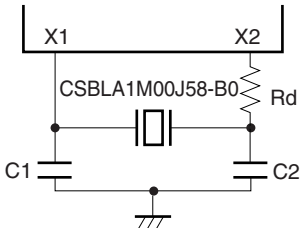
(1) μPD780232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0 (CSB1000J)	1.00	150	150	0	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip			
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

(2) μPD78F0232

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Murata Mfg. Co.,	CSBLA1M00J58-B0**Note** (CSB1000J)	1.00	100	100	2.2 k	4.5	5.5
	CSTLS2M00G56-B0	2.00	On-chip	On-chip	0		
	CSTLS3M58G56-B0 (CSTS0358MG06)	3.58					
	CSTLS4M19G56-B0 (CSTS0419MG06)	4.194					
	CSTLS5M00G56-B0 (CSTS0500MG06)	5.00					

Note A limiting resistor (Rd = 2.2 kΩ) is required when CSBLA1M00J58-B0 (1.00 MHz) manufactured by Murata Mfg. Co., Ltd. is used as the ceramic resonator in the μPD78F0233 (see the figure below). This is not necessary when using one of the other recommended resonators.



Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD780232 within the specifications of the DC and AC characteristics.

Remark Part numbers in parentheses are the old part numbers.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52	V_{DD} = 5 V ± 10%			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–10	mA
		FIP20 to FIP52	V_{DD} = 3.3 V ± 0.3 V			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–8	mA
		FIP20 to FIP52	V_{DD} = 2.7 V to 3.0 V			–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip pull-down resistance	R_2	FIP0 to FIP23 (μPD78F0233 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52 (μPD780232 only)	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64 (μPD780232 only)		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation mode[Note 2]	μPD780232		7	14	mA
			μPD78F0233		9	18	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode	μPD780232		1.5	4.5	mA
			μPD78F0233		2.5	7.5	mA
	I_{DD3}	STOP mode			1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

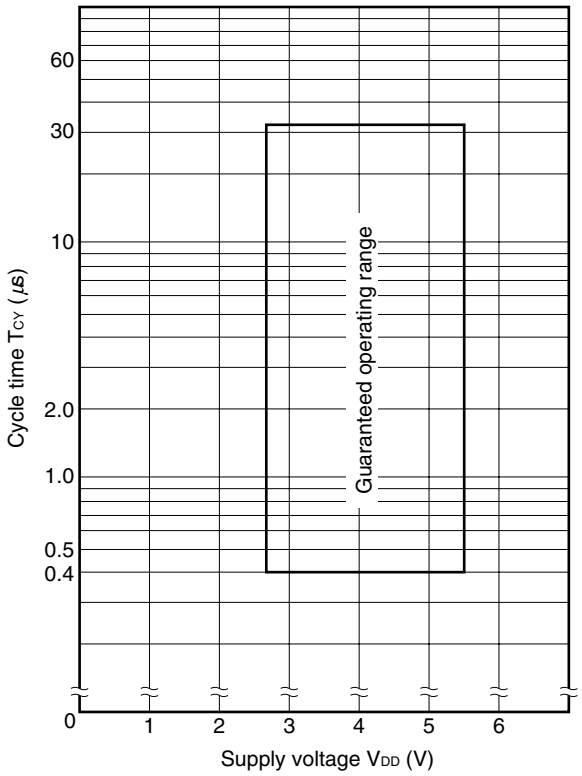
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2 Note			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 3.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Flash Memory Programming Characteristics (μPD78F0233 only, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		1.0		5.0	MHz
Supply voltage	V_{DD}	Operation voltage when writing	2.7		5.5	V
	V_{PP}	Upon V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPH}	Upon V_{PP} high-voltage detection	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} =10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Number of rewrites	C_{WRT}				20	Times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		+10		+40	°C

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from $V_{DD}\uparrow$ to $V_{PP}\uparrow$	t_{DRPSR}	V_{PP} high voltage	10			μs
Set time from $V_{PP}\uparrow$ to $\overline{\text{RESET}}\uparrow$	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{\text{RESET}}\uparrow$	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

18.2 Electrical Specifications of μPD780233 (Preliminary)

These specifications are only preliminary values. Therefore, the mass-produced products do not always satisfy these values.

18.2.1 V_{DD} = 4.5 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

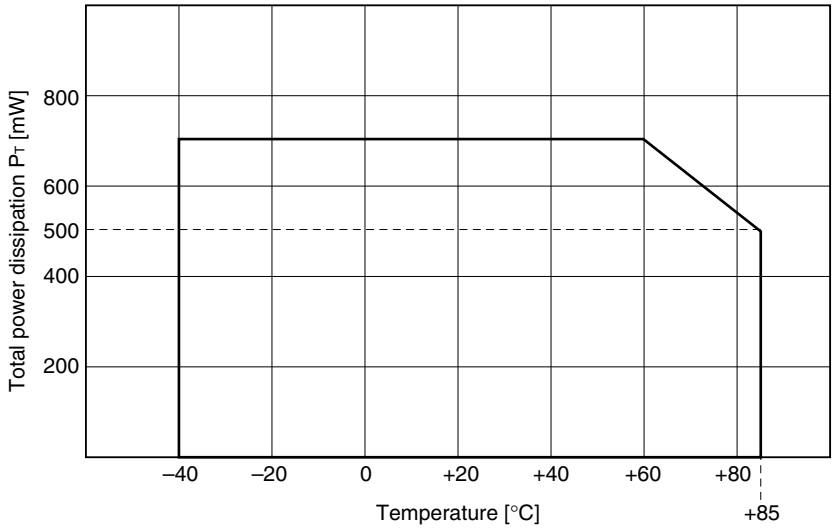
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{LOAD}			V_{DD} – 45 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64 (P-ch open drain)		V_{DD} – 45 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}			V_{DD} – 45 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL} Note 1	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T Note 2	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Note 1. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Note 2. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) × I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids × 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ V \times \frac{15\ mA \times 11\ grids}{11\ grids + 1} \times (1 - \frac{1}{16}) = 25.8\ mW$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ V \times \frac{5\ mA \times 31\ dots}{11\ grids + 1} \times (1 - \frac{1}{16}) = 6.1\ mW$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ V - 2\ V - (-35\ V))^2}{35\ k\Omega} \times \frac{11\ \ grids}{11\ grids + 1} \times (1 - \frac{1}{16}) = 36.4\ mW$$

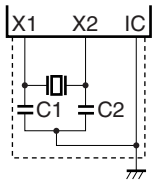
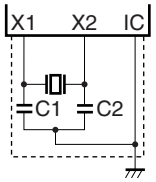
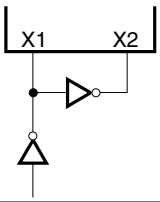
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ V - 0.5\ V - (-35\ V))^2}{35\ k\Omega} \times \frac{31\ dots}{11\ grids + 1} \times (1 - \frac{1}{16}) = 110.7\ mW$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**				10	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52				–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation[Note 2]		7	14	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode		1.5	4.5	mA
	I_{DD3}	STOP mode		1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

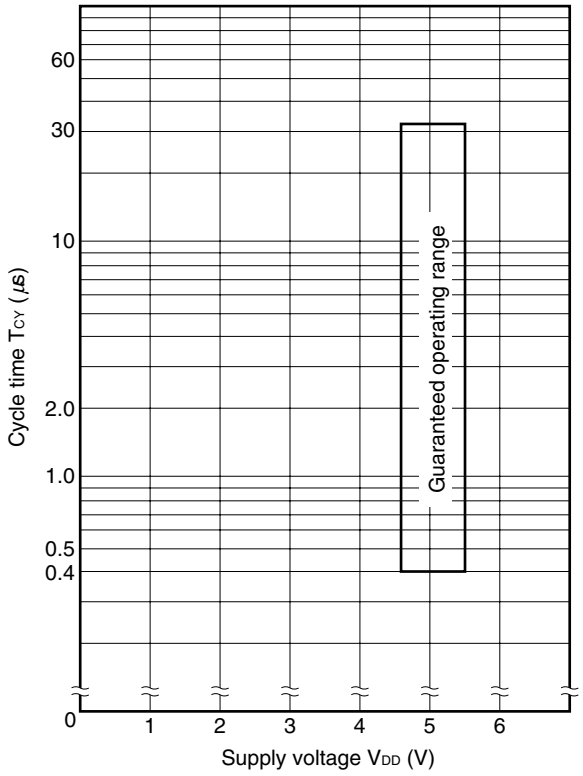
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2 Note			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

18.2.2 V_{DD} = 3.0 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

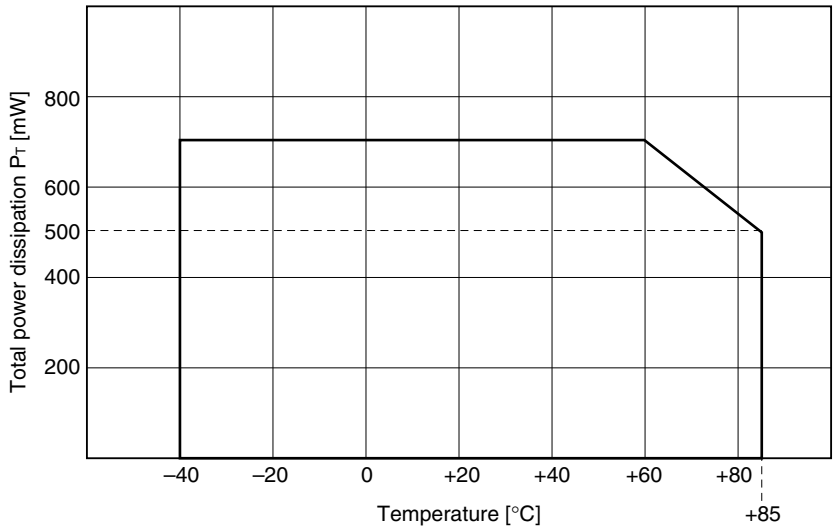
Parameter	Symbol	Conditions			Rating	Unit
Supply voltage	V_{DD}				–0.3 to +6.5	V
	V_{LOAD}	4.5 V ≤ V_{DD} ≤ 5.5 V			V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V			V_{DD} – 43 to V_{DD} + 0.3	V
	AV_{DD}				–0.3 to V_{DD} + 0.3	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{RESET}$			–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		(P-ch open drain)	3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
Output voltage	V_{O1}				–0.3 to V_{DD} + 0.3	V
	V_{O2}	4.5 V ≤ V_{DD} ≤ 5.5 V			V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V			V_{DD} – 43 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins		AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27			–10	mA
		Total for P00 to P02 and P20 to P27			–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64			–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		Peak value	–300	mA
				rms value	–120	mA
Output current, low	I_{OL} **Note 1**	Per pin for P00 to P02 and P20 to P27		Peak value	10	mA
				rms value	5	mA
		Total for P00 to P02 and P20 to P27		Peak value	20	mA
				rms value	10	mA
Total power dissipation	P_T **Note 2**	T_A = –40 to +60°C			700	mW
		T_A = +60 to +85°C			500	mW
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Note 1. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Note 2. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) $\times$ I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids $\times$ 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 36.4\ \text{mW}$$

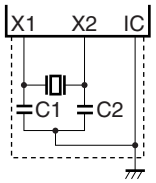
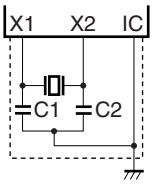
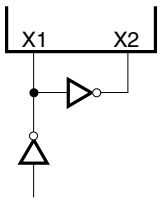
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids} + 1} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids} + 1} \times \left(1 - \frac{1}{16}\right) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			10	ms
			3.0 V ≤ V_{DD} < 4.5 V			30	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52	V_{DD} = 5 V ± 10%			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–10	mA
		FIP20 to FIP52	V_{DD} = 3.3 V ± 0.3 V			–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation[Note 2]		7	14	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode		1.5	4.5	mA
	I_{DD3}	STOP mode		1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

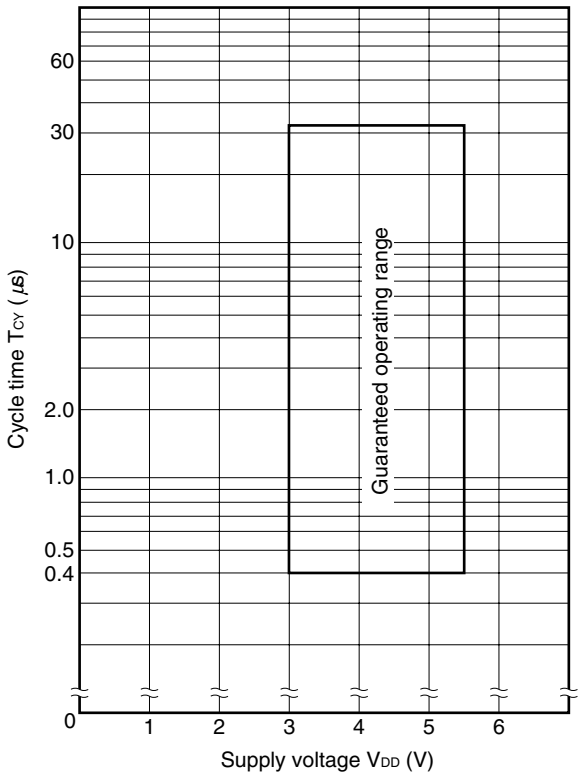
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2 **Note**			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF**Note**			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 3.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

18.2.3 V_{DD} = 2.7 to 5.5 V product

Absolute Maximum Ratings (T_A = 25°C)

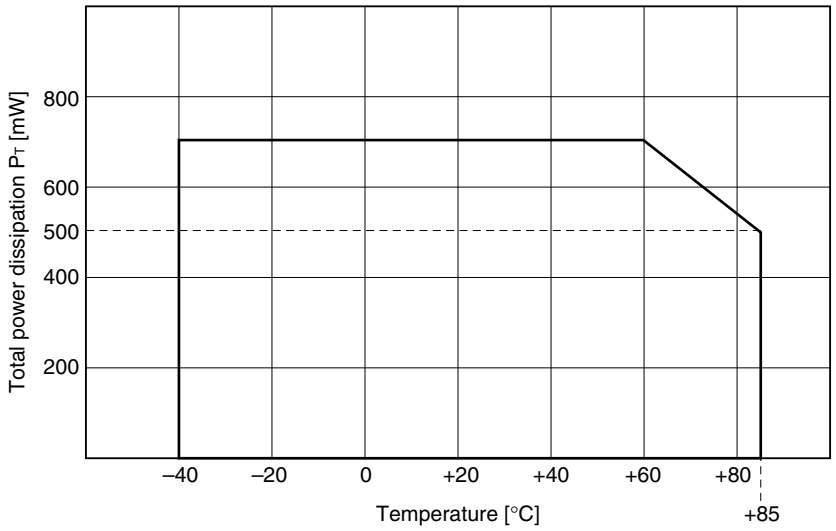
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{LOAD}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
		2.7 V ≤ V_{DD} < 3.0 V		V_{DD} – 42.7 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64 (P-ch open drain)	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 45 to V_{DD} + 0.3	V
			3.0 V ≤ V_{DD} < 4.5 V	V_{DD} – 43 to V_{DD} + 0.3	V
			2.7 V ≤ V_{DD} < 3.0 V	V_{DD} – 42.7 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}	4.5 V ≤ V_{DD} ≤ 5.5 V		V_{DD} – 45 to V_{DD} + 0.3	V
		3.0 V ≤ V_{DD} < 4.5 V		V_{DD} – 43 to V_{DD} + 0.3	V
		2.7 V ≤ V_{DD} < 3.0 V		V_{DD} – 42.7 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	Per pin for P00 to P02 and P20 to P27		–10	mA
		Total for P00 to P02 and P20 to P27		–30	mA
		Per pin for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total for FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms value	–120	mA
Output current, low	I_{OL} **Note 1**	Per pin for P00 to P02 and P20 to P27	Peak value	10	mA
			rms value	5	mA
		Total for P00 to P02 and P20 to P27	Peak value	20	mA
			rms value	10	mA
Total power dissipation	P_T **Note 2**	T_A = –40 to +60°C		700	mW
		T_A = +60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Note 1. The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Note 2. The allowable total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The power consumption of the μPD780233 can be divided to the following three types. The sum of the three power consumption types should be less than the total power dissipation P_T (80% or less of ratings is recommended).

<1> CPU power consumption: Calculate V_{DD} (MAX.) × I_{DD} (MAX.).

<2> Output pin power consumption: Power consumption when maximum current flows to VFD output pins.

<3> Pull-down resistor power consumption: Power consumption by the pull-down resistors incorporated in the VFD output pins by a mask option.

Example Assume the following conditions:

V_{DD} = 5.5 V, 5.0 MHz oscillation

Supply current (I_{DD}) = 21.0 mA

VFD output: 11 grids × 10 segments (blanking width = 1/16)
The maximum current at the grid pin is 15 mA.
The maximum current at the segment pin is 5 mA.
At the key scan timing, the VFD output pin is OFF.

VFD output voltage: Grids $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segments $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 35 kΩ

By placing the above conditions in calculations <1> to <3>, the total dissipation can be calculated.

<1> CPU power consumption: 5.5 V × 21.0 mA = 115.5 mW

<2> Output pin power consumption:

Grid $$(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= 2\ \text{V} \times \frac{15\ \text{mA} \times 11\ \text{grids}}{11\ \text{grids} + 1} \times (1 - \frac{1}{16}) = 25.8\ \text{mW}$$

Segment $$(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{Number of grids +1}} \times (1 - \text{Blanking width})$$

$$= 0.5\ \text{V} \times \frac{5\ \text{mA} \times 31\ \text{dots}}{11\ \text{grids} + 1} \times (1 - \frac{1}{16}) = 6.1\ \text{mW}$$

<3> Pull-down resistor power consumption:

Grid $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of grids}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 2\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{11\ \text{grids}}{11\ \text{grids} + 1} \times (1 - \frac{1}{16}) = 36.4\ \text{mW}$$

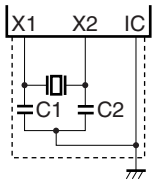
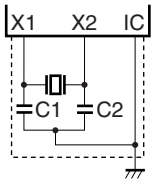
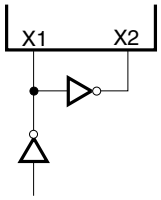
Segment $$\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{Number of illuminated dots}}{\text{Number of grids + 1}} \times (1 - \text{Blanking width})$$

$$= \frac{(5.5\ \text{V} - 0.5\ \text{V} - (-35\ \text{V}))^2}{35\ \text{k}\Omega} \times \frac{31\ \text{dots}}{11\ \text{grids} + 1} \times (1 - \frac{1}{16}) = 110.7\ \text{mW}$$

Total power consumption = <1> + <2> + <3> = 115.5 + 25.8 + 6.1 + 36.4 + 110.7 = 294.5 mW

In this example, the total power consumption does not exceed the rating of the allowable total power dissipation, so there is no problem in the power consumption. However, when the total power consumption exceeds the rating of the total power dissipation, it is necessary to lower the power consumption. To reduce the power consumption, reduce the number of pull-down resistors.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			10	ms
			2.7 V ≤ V_{DD} < 4.5 V			30	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52	V_{DD} = 5 V ± 10%			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–10	mA
		FIP20 to FIP52	V_{DD} = 3.3 V ± 0.3 V			–5	mA
		FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–8	mA
		FIP20 to FIP52	V_{DD} = 2.7 V to 3.0 V			–5	mA
Software pull-up resistance	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip mask option pull-down resistance (V_{LOAD} connection)	R_3	FIP0 to FIP52	V_{DD} – V_{LOAD} = 40 V	30	60	135	kΩ
On-chip mask option pull-down resistance (V_{SS0} connection)	R_4	P50 to P57, P60 to P64		15	35	90	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5 MHz crystal oscillation operation[Note 2]		7	14	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode		1.5	4.5	mA
	I_{DD3}	STOP mode		1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

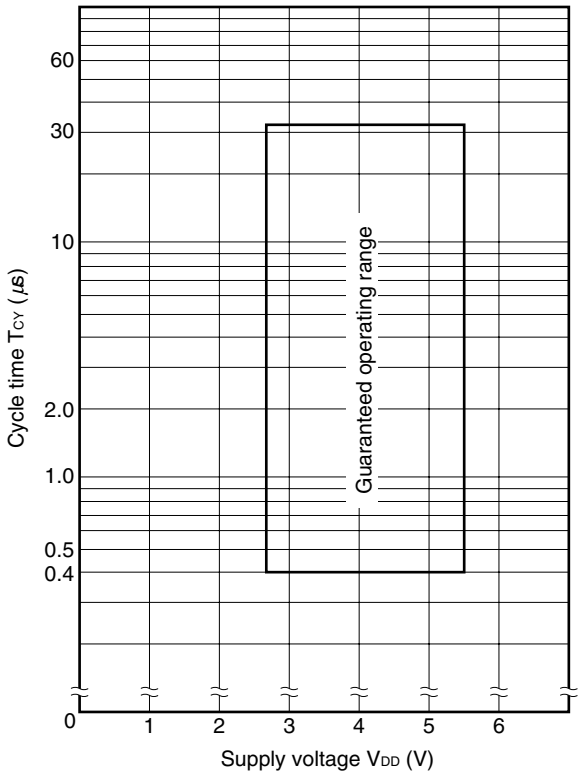
2. When the processor clock control register (PCC) is 00H.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ + 0.2 Note			μs

Note F_{COUNT} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 3.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Notes 1, 2**					±1.0	%FSR
Conversion time**Note 3**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Quantization error (±1/2LSB) is not included.

2. This parameter is indicated as the ratio to the full-scale value (%FSR).

3. Set the A/D conversion time to 14 μs or more.

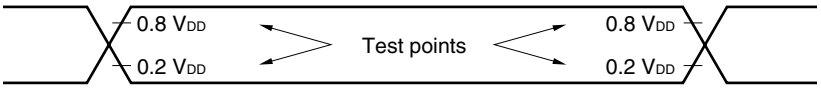
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

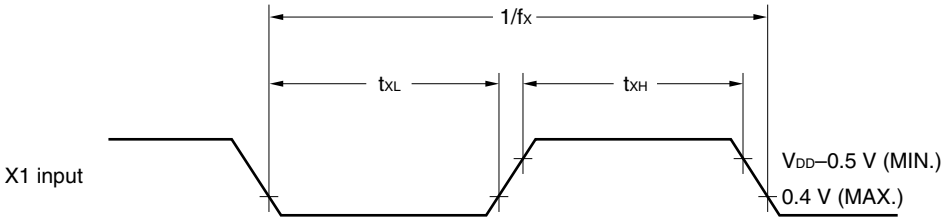
Note $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

18.3 Timing Chart

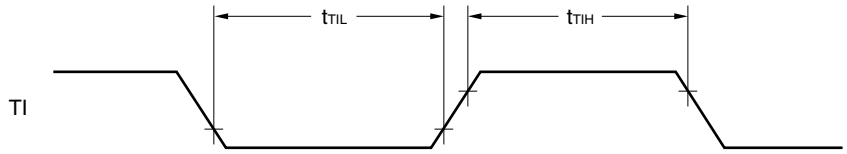
AC timing test point (excluding X1, XT1 input)



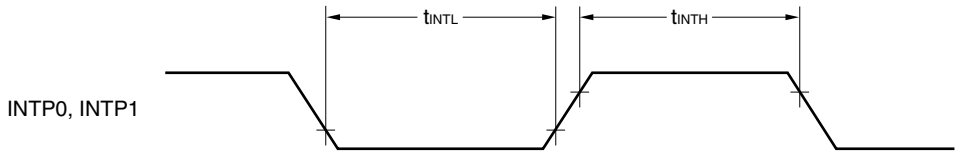
Clock timing



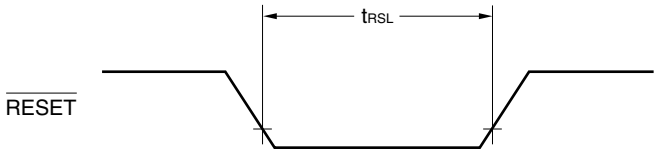
TI timing



Interrupt request input timing

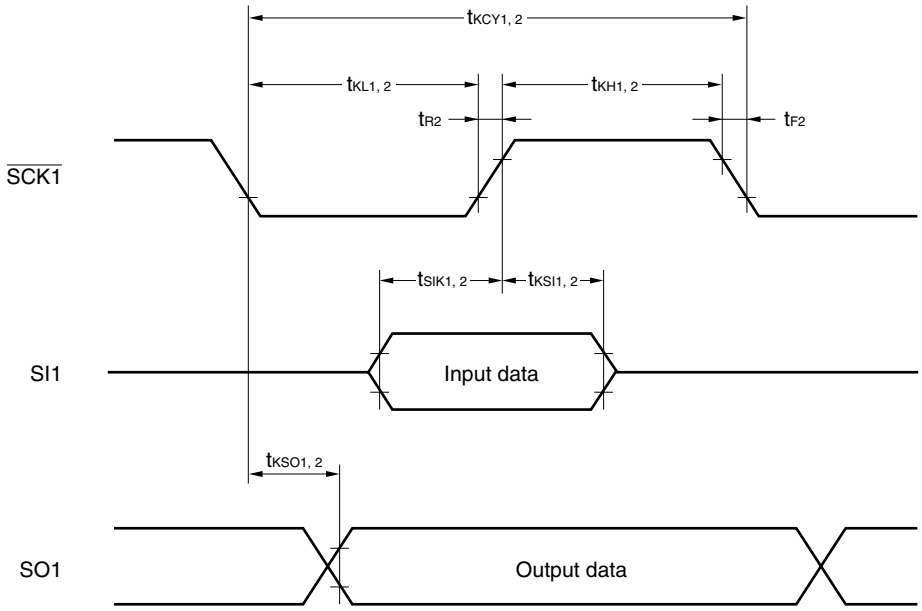


$\overline{\text{RESET}}$ input timing

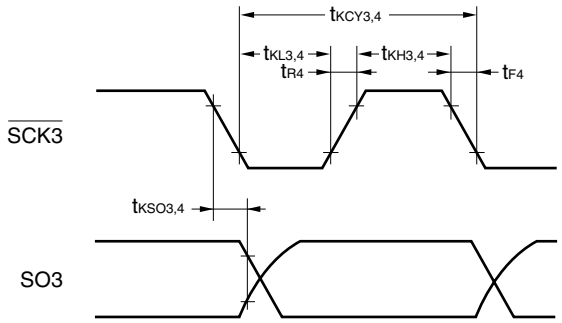


Serial transfer timing

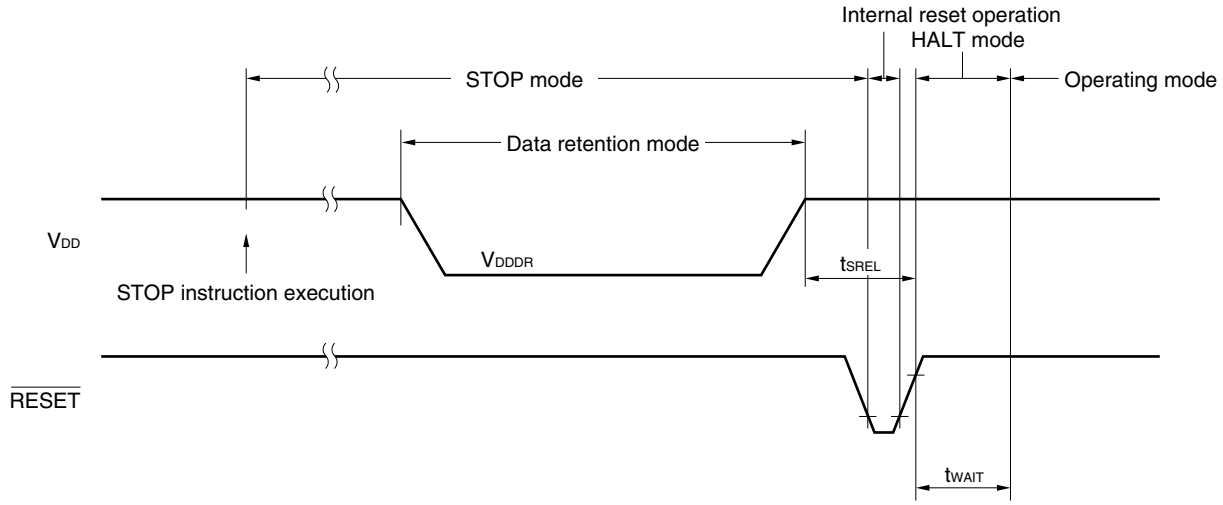
3-wire serial mode:



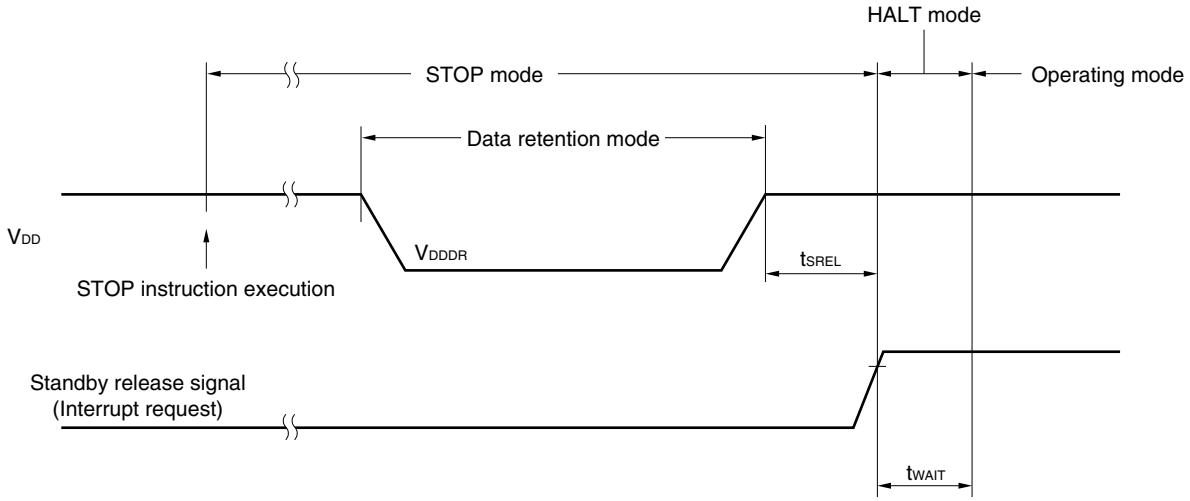
2-wire serial mode:



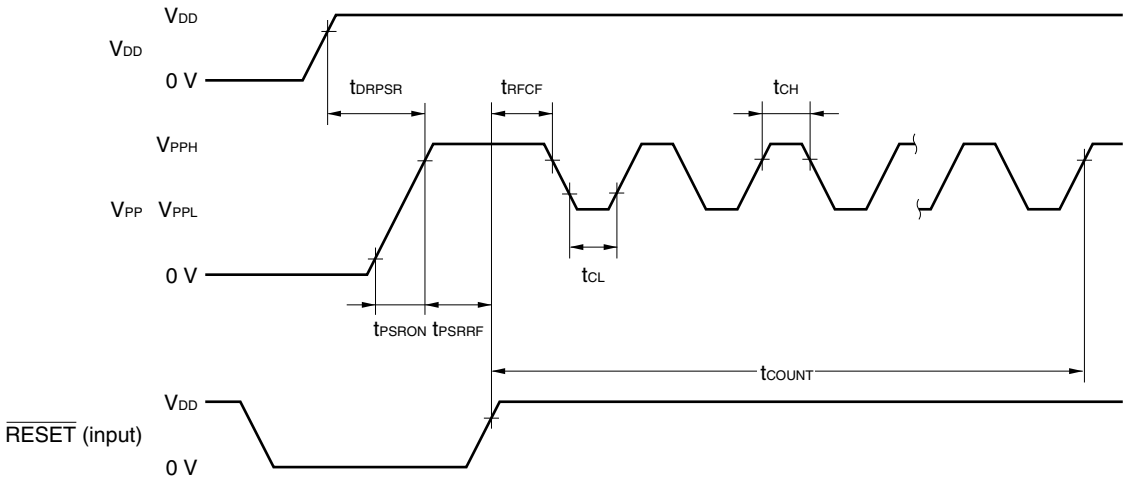
Data retention timing (STOP mode release by $\overline{\text{RESET}}$)



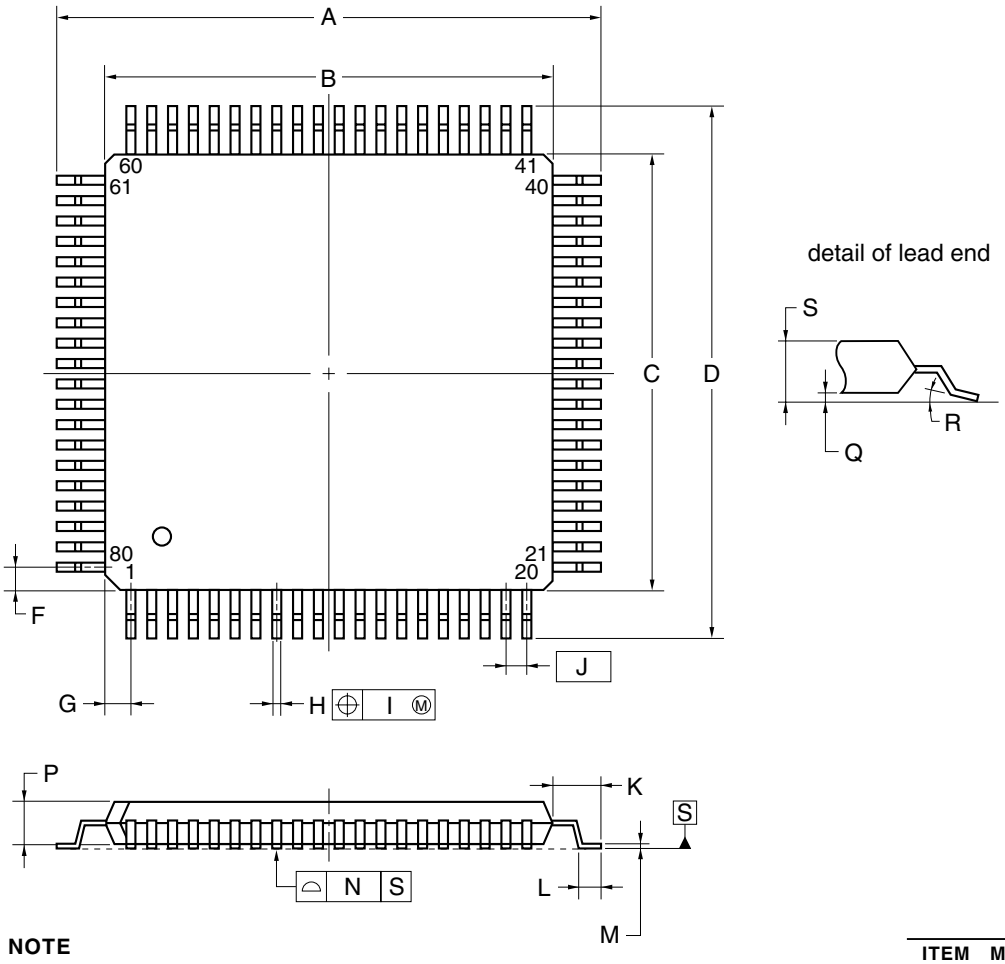
Data retention timing (standby release signal: STOP mode release by interrupt request signal)



Flash memory write mode setting timing



80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

★ CHAPTER 20 RECOMMENDED SOLDERING CONDITIONS

The μPD780232 and 78F0233 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Caution The μPD780233GC-×××-8BT is under development, so its recommended soldering conditions have not been defined.

Table 20-1. Surface Mounting Type Soldering Conditions

μPD780232GC-×××-8BT: 80-pin plastic QFP (14 × 14)
μPD78F0233GC-8BT: 80-pin plastic QFP (14 × 14)

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DIFFERENCES BETWEEN μPD780232 AND 780208 SUBSERIES

Table A-1 shows the major differences between the μPD780232 and 780208 Subseries.

★ **Table A-1. Major Differences Between μPD780232 and 780208 Subseries (1/2)**

Item \ Part Number	μPD780232 Subseries	μPD780208 Subseries
PROM or flash memory model	μPD78F0233 (flash memory)	μPD78P0208 (PROM)
Supply voltage	V_{DD} = 4.5 to 5.5 V[Note]	V_{DD} = 2.7 to 5.5 V
★ Internal ROM size	μPD780232: 16 KB μPD780233: 24 KB μPD78F0233: 24 KB	μPD780204: 32 KB μPD780205: 40 KB μPD780206: 48 KB μPD780208: 60 KB μPD78P0208: 60 KB
Internal high-speed RAM size	768 bytes	1024 bytes
Internal expansion RAM size	None	μPD780206, 780208, and 78P0208 only: 1024 bytes
Internal buffer RAM size	32 bytes	64 bytes
VFD display RAM size	112 bytes	80 bytes
CPU clock	Main system clock only	Main system clock or subsystem clock selectable
I/O port	40 pins	74 pins
Total of VFD display output pins	53 pins	53 pins
Serial interface	2 channels	2 channels
Timer	8-bit remote control timer: 1 channel 8-bit timer: 2 channels Watchdog timer: 1 channel	16-bit timer/event counter: 1 channel 8-bit timer/event counter: 2 channels Watch timer: 1 channel Watchdog timer: 1 channel

★ **Note** Versions with an expanded supply voltage range (V_{DD} = 2.7 to 5.5 V and V_{DD} = 3.0 to 5.5 V) are also available. Since the electrical specifications vary depending on the product, refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS** for details.

Table A-1. Major Differences Between μPD780232 and 780208 Subseries (2/2)

Item \ Part Number		μPD780232 Subseries	μPD780208 Subseries
Clock output		None	Provided
Buzzer output		None	Provided
Vectored interrupt source	Internal	10	11
	External	2	4
Test input		None	Provided
Package		80-pin plastic QFP (14 × 14)	100-pin plastic QFP (14 × 20)
Electrical characteristics and recommended soldering conditions		Refer to the individual data sheet or user's manual (including electrical specifications)	

Remark In addition to the above items, the organization of the development tools also differ between the above subseries (especially between the PROM model and flash memory model). For details, refer to the User's Manual of each subseries.

APPENDIX B DEVELOPMENT TOOLS

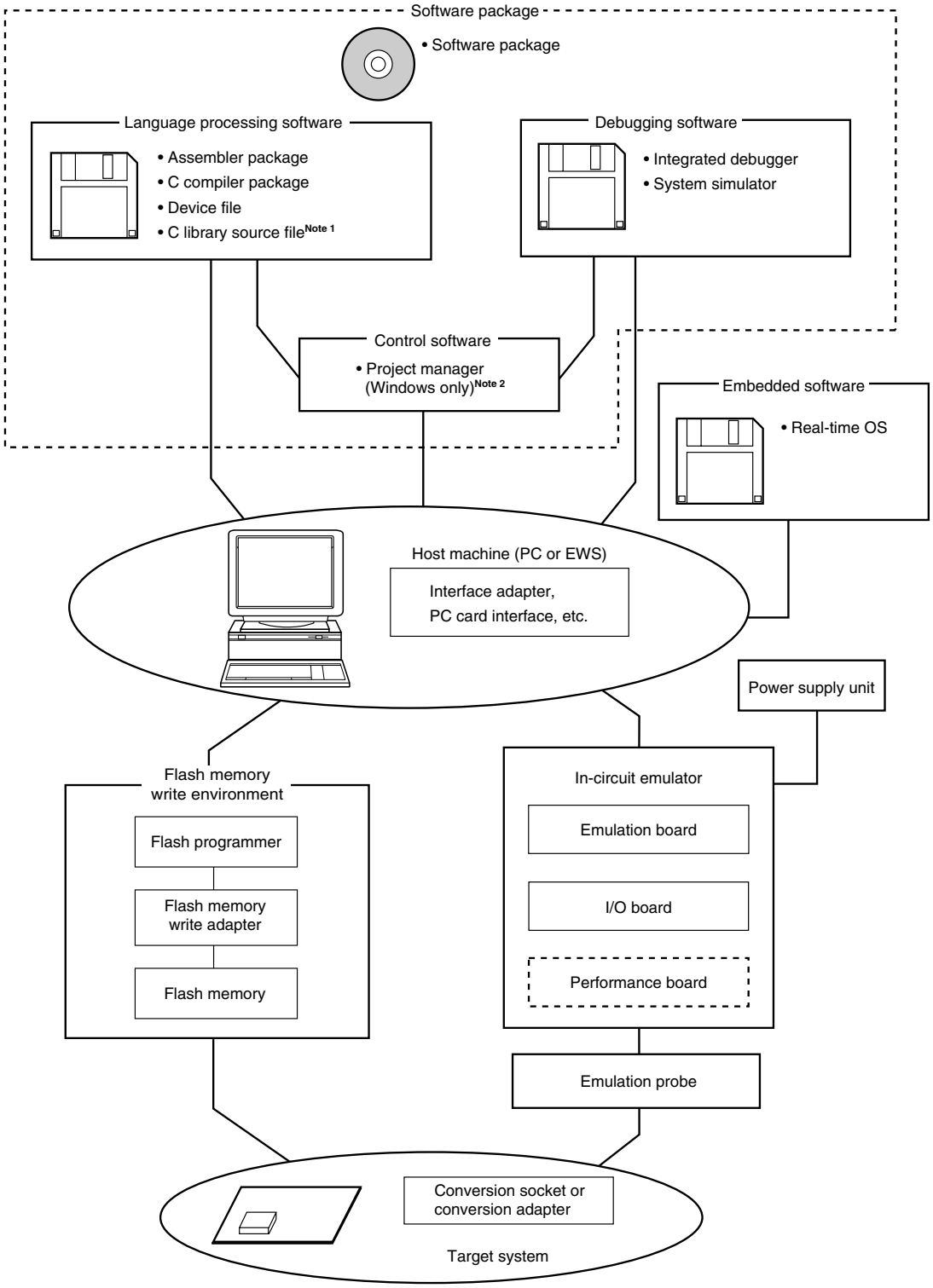
The following development tools are available for the development of systems that employ the μPD780232 Subseries. Figure B-1 shows the development tool configuration.

- **Support for PC98-NX series**
  Unless otherwise specified, products supported by IBM PC/AT™ compatibles can be used for PC98-NX series computers. When using PC98-NX series computers, refer to the description for IBM PC/AT compatibles.

- **Windows**
  Unless otherwise specified, "Windows" means the following OSs.
  - Windows 3.1
  - Windows 95
  - Windows 98
  - Windows 2000
  - Windows NT™ Ver. 4.0

Figure B-1. Development Tool Configuration (1/2)

★ **(1) When using the in-circuit emulators IE-78K0-NS, IE-78K0-NS-A**

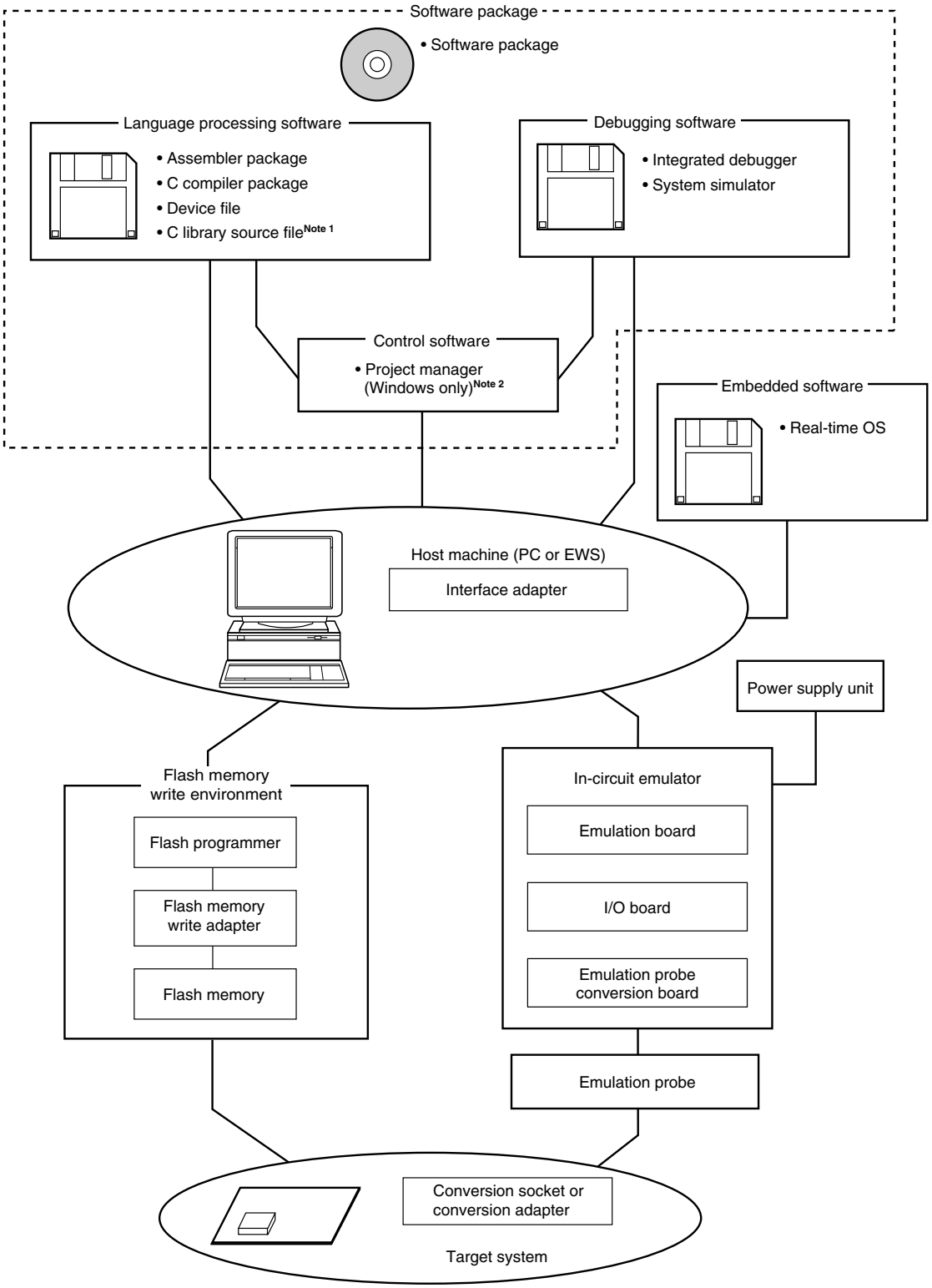


Notes 1. The C library source file is not included in the software package.

2. The project manager is included in the assembler package.
The project manager is only used for Windows.

Figure B-1. Development Tool Configuration (2/2)

★ **(2) When using the in-circuit emulator IE-78001-R-A**



Notes 1. The C library source file is not included in the software package.

2. The project manager is included in the assembler package.
The project manager is only used for Windows.

★ B.1 Software Package

SP78K0 Software package	This package contains various software tools for 78K/0 Series development. The following tools are included. RA78K0, CC78K0, ID78K0-NS, SM78K0, and various device files
	Part Number: μS××××SP78K0

Remark ×××× in the part number differs depending on the OS used.

μS××××SP78K0

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series,	Windows (Japanese version)	CD-ROM
BB17	IBM PC/AT compatibles	Windows (English version)	

B.2 Language Processing Software

RA78K0 Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. Further, this assembler is provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with an optional device file (DF780232). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part Number: μS××××RA78K0
CC78K0 C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an optional assembler package and device file. **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part Number: μS××××CC78K0
DF780232**Note 1** Device file	This file contains information peculiar to the device. This device file should be used in combination with an optional tool (RA78K0, CC78K0, SM78K0, ID78K0-NS, and RX78K0). Corresponding OS and host machine differ depending on the tool used.
	Part Number: μS××××DF780232
CC78K0-L**Note 2** C library source file	This is a source file of functions configuring the object library included in the C compiler package. This file is required to match the object library included in C compiler package to the user's specifications. It does not depend on the operating environment because it is a source file.
	Part Number: μS××××CC78K0-L

Notes 1. The DF780232 can be used in common with the RA78K0, CC78K0, SM78K0, ID78K0-NS, and RX78K0.

★ **2.** CC78K0-L is not included in the software package (SP78K0).

Remark ××××in the part number differs depending on the host machine and OS used.

μS××××RA78K0
μS××××CC78K0

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	
AB17		Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	
3P17	HP9000 series 700™	HP-UX™ (Rel. 10.10)	
3K17	SPARCstation™	SunOS™ (Rel. 4.1.4), Solaris™ (Rel. 2.5.1)	

μS××××DF780232
μS××××CC78K0-L

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	
3P16	HP9000 series 700	HP-UX (Rel. 10.10)	DAT
3K13	SPARCstation	SunOS (Rel. 4.1.4), Solaris (Rel. 2.5.1)	3.5-inch 2HD FD
3K15			1/4-inch CGMT

B.3 Control Software

Project manager	This is control software designed to enable efficient user program development in the Windows environment. All operations used in development of a user program, such as starting the editor, building, and starting the debugger, can be performed from the project manager. **<Caution>** The project manager is included in the assembler package (RA78K0). It can only be used in Windows.

B.4 Flash Memory Writing Tools

Flashpro III (Part number: FL-PR3, PG-FP3) Flashpro IV (Part number: FL-PR4, PG-FP4) Flash programmer	Flash programmer dedicated to microcontrollers with on-chip flash memory.
FA-80GC Flash memory writing adapter	Flash memory writing adapter used connected to the Flashpro III or Flashpro IV • FA-80GC: 80-pin plastic QFP (GC-8BT type)

Remark FL-PR3, FL-PR4, and FA-80GC are products of Naito Densei Machida Mfg. Co., Ltd.
Contact: +81-45-475-4191 Naito Densei Machida Mfg. Co., Ltd.

B.5 Debugging Tools (Hardware)

B.5.1 When using in-circuit emulators IE-78K0-NS and IE-78K0-NS-A

IE-78K0-NS In-circuit emulator		The in-circuit emulator serves to debug hardware and software when developing application systems using a 78K/0 Series product. It corresponds to integrated debugger (ID78K0-NS). This emulator should be used in combination with power supply unit, emulation probe, and interface adapter which is required to connect this emulator to the host machine.
★ IE-78K0-NS-PA Performance board		This board is used for extending the IE-78K0-NS functions, and is used connected to the IE-78K0-NS-PA. With the addition of this board, the addition of a coverage function, enhancement of tracer and timer functions, and other such debugging function enhancements are possible.
★ IE-78K0-NS-A In-circuit emulator		In-circuit emulator that combines IE-78K0-NS and IE-78K0-NS-PA
IE-70000-MC-PS-B Power supply unit		This adapter is used for supplying power from a receptacle of 100 to 240 V AC.
★ IE-70000-98-IF-C Interface adapter		This adapter is required when using the PC-9800 series computer (except notebook type) as the host machine (C bus compatible).
★ IE-70000-CD-IF-A PC card interface		This is PC card and interface cable required when using the notebook-type computer as the host machine (PCMCIA socket compatible).
IE-70000-PC-IF-C Interface adapter		This adapter is required when using the IBM PC/AT compatible computers as the host machine (ISA bus compatible).
★ IE-70000-PCI-IF-A Interface adapter		This adapter is required when using a PC with a PCI bus as the host machine.
★ IE-780233-NS-EM4 Emulation board		This board emulates the operations of the peripheral hardware peculiar to a device. It should be used in combination with an in-circuit emulator.
NP-80GC Emulation probe		This probe is used to connect the in-circuit emulator to the target system and is designed for 80-pin plastic QFP (GC-8BT type).
	EV-9200GC-80 Conversion socket (Refer to **Figure B-2**)	This conversion socket connects the NP-80GC to the target system board designed to mount an 80-pin plastic QFP (GC-8BT type).
★ NP-80GC-TQ ★ NP-H80GC-TQ Emulation probe		This probe is used to connect the in-circuit emulator to the target system and is designed for 80-pin plastic QFP (GC-8BT type).
★	TGC-080SBP Conversion adapter	This conversion adapter connects the NP-80GC-TQ or NP-H80GC-TQ to the target system board designed to mount an 80-pin plastic QFP (GC-8BT type).

Remarks 1. NP-80GC, NP-80GC-TQ, and NP-H80GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd.
For further information, contact Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191)

2. TGC-080SBP is a product of TOKYO ELETECH CORPORATION.
For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronics Department (+81-3-3820-7112)
Osaka Electronics Department (+81-6-6244-6672)

B.5.2 When using in-circuit emulator IE-78001-R-A

IE-78001-R-A In-circuit emulator		The in-circuit emulator serves to debug hardware and software when developing application systems using a 78K/0 Series product. It corresponds to integrated debugger (ID78K0). This emulator should be used in combination with emulation probe and interface adapter which is required to connect this emulator to the host machine.
IE-70000-98-IF-C Interface adapter		This adapter is required when using the PC-9800 Series computer (except notebook type) as the host machine (C bus support).
IE-70000-PC-IF-C Interface adapter		This adapter is required when using the IBM PC/AT and its compatible computers as the host machine (ISA bus support).
★ IE-70000-PCI-IF-A Interface adapter		This adapter is required when using a personal computer incorporating a PCI bus as the IE-78001-R-A host machine.
IE-780233-NS-EM4 Emulation board		This board emulates the operations of the peripheral hardware peculiar to a device. This can be used in combination with the in-circuit emulator and emulation probe conversion board.
	★ IE-78K0-NS-P01 I/O board	This board is used in combination with an emulation board and incorporates an FPGA
	IE-78K0-R-EX1 Emulation probe conversion board	This conversion board is required when using the IE-780233-NS-EM4 on the IE-78001-R-A.
★ EP-78230GC-R Emulation probe		This probe is used to connect the in-circuit emulator to the target system and is designed for 80-pin plastic QFP (GC-8BT type).
	★ EV-9200GC-80 Conversion socket (Refer to **Figure B-2**)	This conversion socket connects the EP-78230GC-R to the target system board designed to mount an 80-pin plastic QFP (GC-8BT type).

B.6 Debugging Tools (Software)

SM78K0 System simulator	This is a system simulator for the 78K/0 Series. The SM78K0 is Windows-based software. It is used to perform debugging at the C source level or assembler level while simulating the operation of the target system on a host machine. Use of the SM78K0 allows the execution of application logical testing and performance testing on an independent basis from hardware development, thereby providing higher development efficiency and software quality. The SM78K0 should be used in combination with the device file (DF780232) (sold separately).
	Part Number: μS××××SM78K0
ID78K0-NS Integrated debugger (supporting in-circuit emulators IE-78K0-NS and IE-78K0-NS-A)	This debugger supports the in-circuit emulators for the 78K/0 Series. The ID78K0-NS and ID78K0 are Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (sold separately).
ID78K0 Integrated debugger (supporting in-circuit emulator IE-78001-R-A)	Part Number: μS××××ID78K0-NS, μS××××ID78K0

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SM78K0
μS××××ID78K0-NS
μS××××ID78K0

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	3.5-inch 2HD FD
BB13		Windows (English version)	
AB17		Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

B.7 Embedded Software

RX78K0 Real-time OS	RX78K0 is a real-time OS conforming to the μITRON specifications. Tool (configurator) for generating nucleus of RX78K0 and plural information tables is supplied. Used in combination with an optional assembler package (RA78K0) and device file (DF780232). **<Precaution when using RX78K0 in PC environment>** The real-time OS is a DOS-based application. It should be used in the DOS Prompt when using in Windows.
	Part number: μS××××RX78013-ΔΔΔΔ

Caution When purchasing the RX78K0, fill in the purchase application form in advance and sign the user agreement.

Remark ×××× and ΔΔΔΔ in the part number differ depending on the host machine and OS used.

μS××××RX78013-ΔΔΔΔ

ΔΔΔΔ	Product Outline	Maximum Number for Use in Mass Production
001	Evaluation object	Do not use for mass-produced product.
100K	Mass-production object	0.1 million units
001M		1 million units
010M		10 million units
S01	Source program	Source program for mass-produced object

××××	Host Machine	OS	Supply Medium
AA13	PC-9800 series	Windows (Japanese version)	3.5-inch 2HD FD
AB13	IBM PC/AT compatibles	Windows (Japanese version)	
BB13		Windows (English version)	

B.8 Upgrading Old Type In-Circuit Emulator to IE-78001-R-A for 78K/0 Series

If you have an old-type in-circuit emulator for the 78K/0 series (IE-78000-R or IE-78000-R-A), your in-circuit emulator can be upgraded to be equivalent to IE-78001-R-A by only replacing the break board with the IE-78001-R-BK.

Table B-1. Upgrading Old Type In-Circuit Emulator to IE-78001-R-A for 78K/0 Series

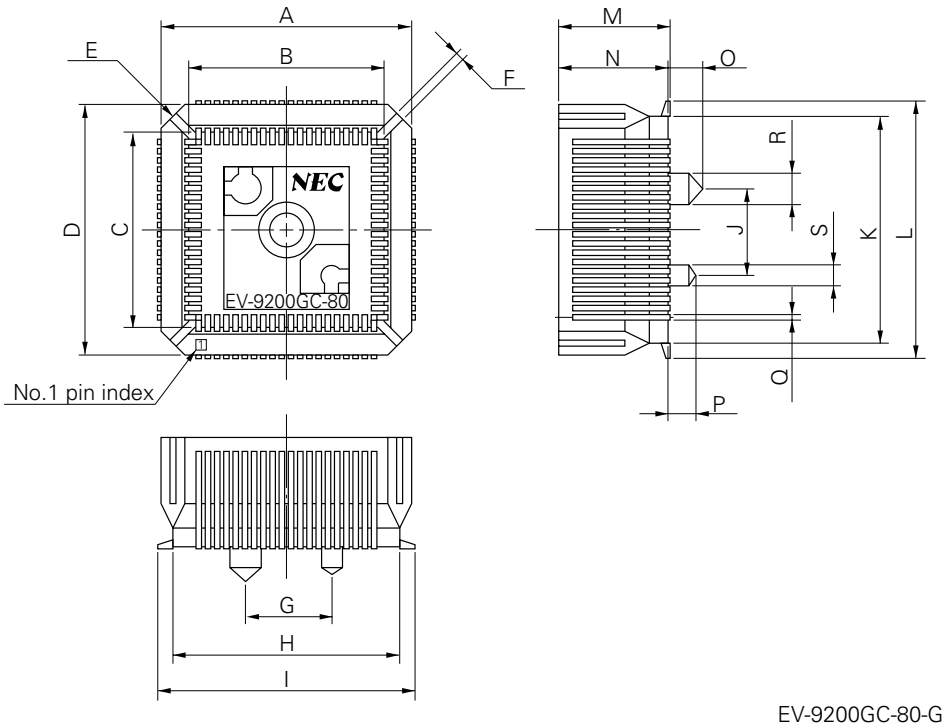
Your In-Circuit Emulator	Upgrading Housing[Note]	Necessary Board
IE-78000-R	Necessary	IE-78001-R-BK
IE-78000-R-A	Not necessary	

Note To upgrade housing, it is necessary for the unit to be brought to NEC Electronics.

B.9 Dimensions of Conversion Socket

Figure B-2. Dimensions of EV-9200GC-80 (Reference)

Based on EV-9200GC-80
(1) Package drawing (in mm)

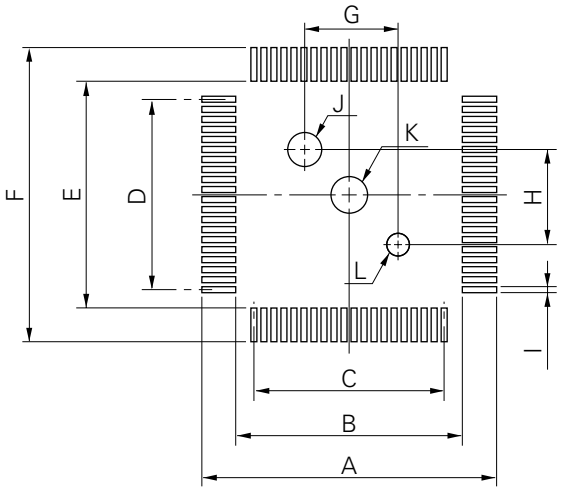


EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure B-3. Recommended Board Mounting Pattern of EV-9200GC-80 (Reference)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "Semiconductor Device Mount Manual" (http://www.necel.com/pkg/en/mount/index.html).

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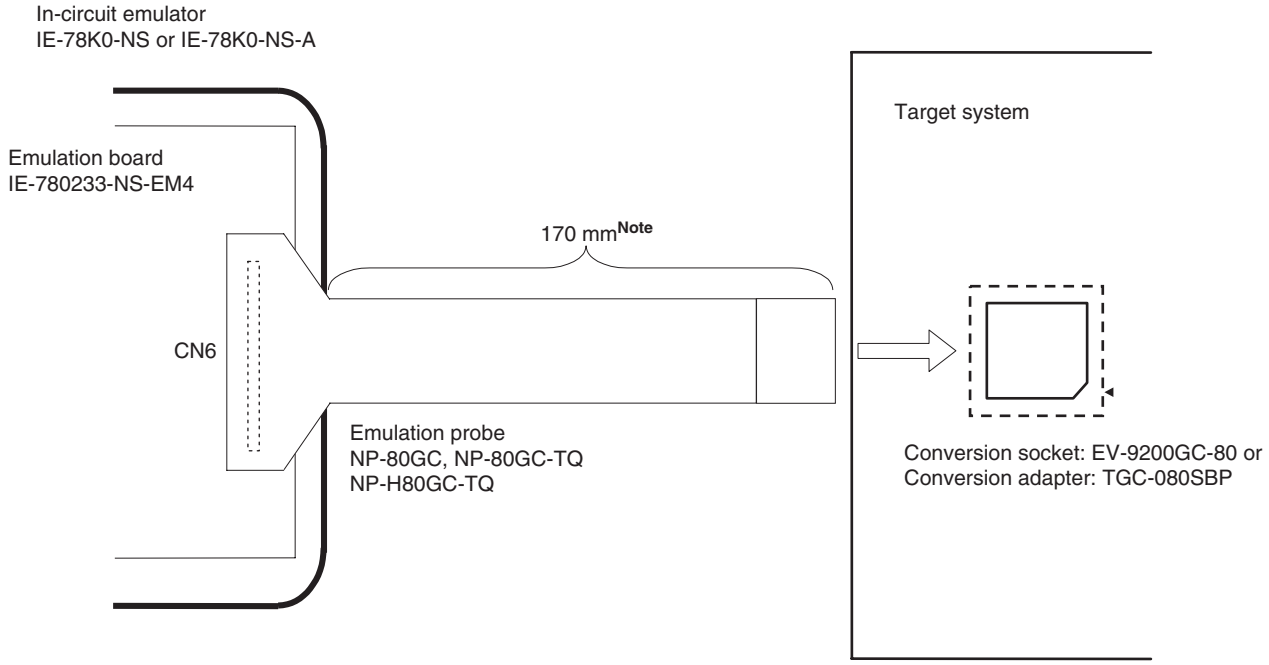
APPENDIX C CAUTIONS ON DESIGNING TARGET SYSTEM

Figures C-1 and C-2 show the conditions when connecting the emulation probe to the conversion adapter or conversion socket. Follow the configuration below and consider the shape of parts to be mounted on the target system when designing a system.

- NP-80GC, NP-80GC-TQ, NP-H80GC-TQ

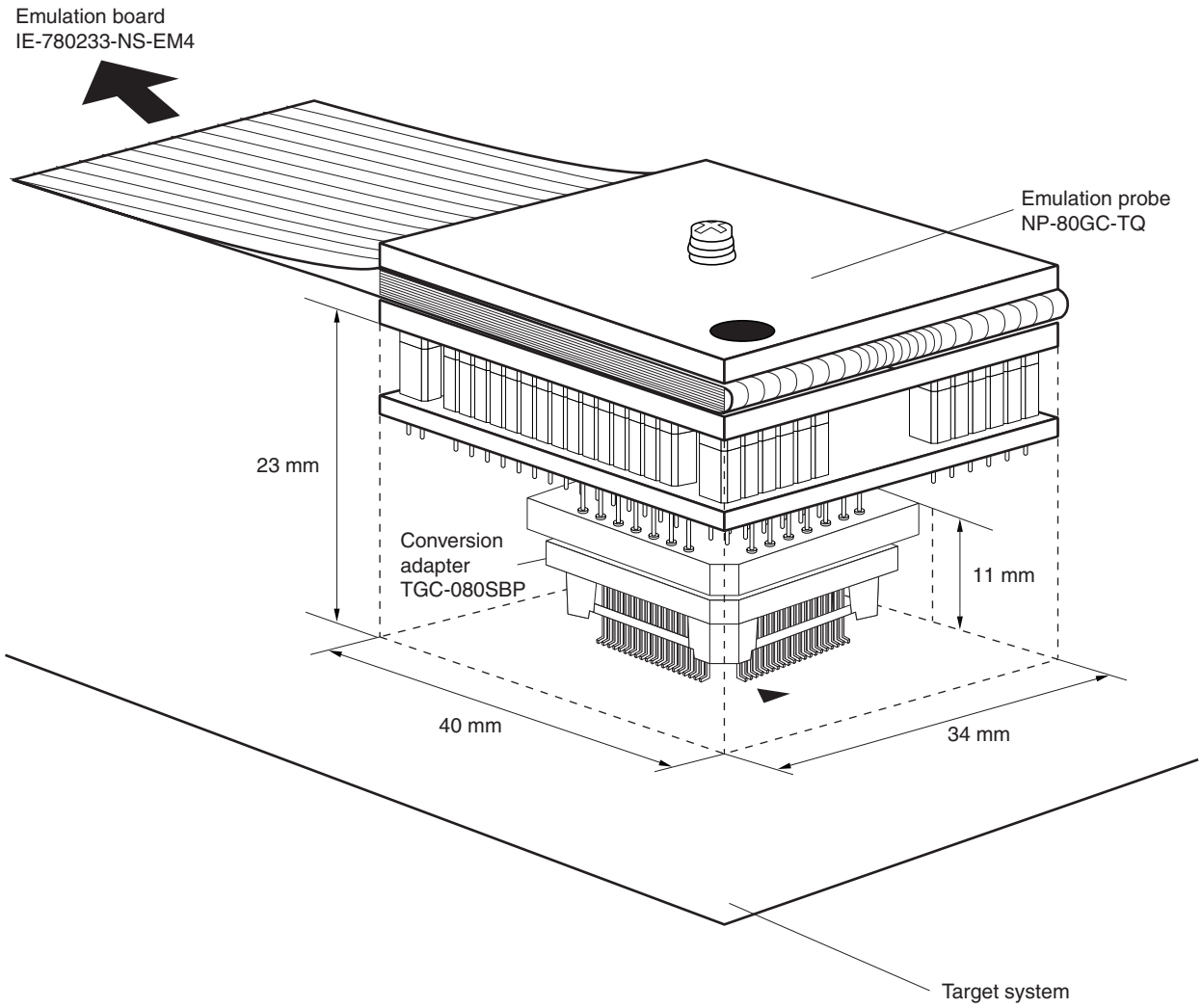
Figure C-1. Distance Between In-Circuit Emulator and Conversion Socket



Note When NP-H80GC-TQ is used, the distance is 370 mm.

Remark NP-80GC, NP-80GC-TQ, and NP-H80GC-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

Figure C-2. Connection Condition of Target System (NP-80GC-TQ)



Remark NP-80GC-TQ is a product of Naito Densei Machida Mfg. Co., Ltd.
TGC-080SBP is a product of TOKYO ELETECH CORPORATION.

APPENDIX D REGISTER INDEX

D.1 Register Index (In Alphabetical Order with Respect to Register Names)

D.2 Register Index (In Alphabetical Order with Respect to Register Symbol)

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APPENDIX E REVISION HISTORY

The history of revisions up to this edition is shown below. “Applied to:” indicates the chapters to which the revision was applied.

(1/2)

Edition	Contents	Applied to:
2nd edition	Addition of product μPD780233GC-×××-8BT	Throughout
	Change of description from FIP controller/driver to VFD controller/driver	
	Addition of description of expanded supply voltage range version (V_{DD} = 2.7 to 5.5 V and V_{DD} = 3.0 to 5.5 V)	
	Addition of **Caution** to **1.8 Mask Option**	**CHAPTER 1 GENERAL**
	Addition of description on pull-down resistor to FIP0 to FIP23, FIP24 to FIP31, FIP32 to FIP39, FIP40 to FIP47, and FIP48 to FIP52 in **2.1 Pin Function List (2) Non-port pins**	**CHAPTER 2 PIN FUNCTIONS**
	Addition of description on pull-down resistor to **2.2.7 FIP0 to FIP23**	
	Change of **Table 2-1 Types of Pin I/O Circuits**	
	Modification of block diagrams **Figure 4-2 Block Diagram of P00 to P02** **Figure 4-3 Block Diagram of P20 and P27** **Figure 4-4 Block Diagram of P21, P24 to P26** **Figure 4-5 Block Diagram of P22 and P23**	**CHAPTER 4 PORT FUNCTIONS**
	Addition of **Caution** to **4.2.3 Port 3** to **4.2.6 Port 6**	
	Change of description of **(2) Pull-up resistor option registers (PU0, PU2) in 4.3 Port Function Control Registers**	
	Modification of **Table 4-4 Comparison Between Mask Options of Mask ROM Models and μPD78F0233**	
	Change of configuration in **6.2 Configuration of 8-Bit Remote Control Timer 9** and **6.3 Registers Controlling 8-Bit Remote Control Timer 9**	**CHAPTER 6 8-BIT REMOTE CONTROL TIMER 9**
	Change of **Figure 7-5 Timing of Interval Timer Operation**	**CHAPTER 7 8-BIT TIMERS 80, 81**
	Change of **Figure 7-6 Start Timing of 8-Bit Timer Register 8n (TM8n)**	
	Modification of cautions in **CHAPTER 8 WATCHDOG TIMER**	**CHAPTER 8 WATCHDOG TIMER**
	Addition of **9.5 How to Read A/D Converter Characteristics Table**	**CHAPTER 9 A/D CONVERTER**
	Addition of the following items to **9.6 Cautions for A/D Converter** (6) Input impedance of ANI0 to ANI3 pins (12) Timing at which A/D conversion result is undefined (13) Notes on board design (14) Internal equivalent circuit of ANI0 to ANI3 pins and permissible signal source impedance	
	Modification of description in **(3) Communication operation**, **(4) Synchronization control**, and **(5) Timing of interrupt request signal generation** in **10.4.3 3-wire serial mode with automatic transmit/receive function**	**CHAPTER 10 SERIAL INTERFACE SIO1**
	Change of **Figure 11-1 Block Diagram of Serial Interface SIO3**	**CHAPTER 11 SERIAL INTERFACE SIO3**

(2/2)

Edition	Contents	Applied to:
2nd edition	Change of description of **(6)** in **12.1 Function of VFD Controller/Driver** and addition of **Note**	**CHAPTER 12 VFD CONTROLLER/ DRIVER**
	Change of **Figure 12-2 Format of Display Mode Register 0** (change of set value of FOUT5 to FOUT0 and the number of VFD output pins) and addition of **Caution 4**	
	Addition of **Figure 12-7 Relationship Between Address Location of Display Data Memory and VFD Output (with 42 VFD Output Pins and 14 Patterns)**	
	Addition of **Remark** to **Table 13-1 Interrupt Sources**	**CHAPTER 13 INTERRUPT FUNCTIONS**
	Change of **Figure 13-1 Basic Configuration of Interrupt Function (D) Software interrupt**	
	Addition of **Cautions 3** and **4** to **Figure 13-2 Format of Interrupt Request Flag Register**	
	Change of **Figure 13-5 Format of External Interrupt Rising Edge Enable Register (EGP), External Interrupt Falling Edge Enable Register (EGN)** (The two registers were separately explained in the previous edition. In this version, they are combined and explained in one figure.)	
	Modification of **Table 16-1 Differences Between uPD78F0233 and Mask ROM Models**	**CHAPTER 16 μPD78F0233**
	Addition of **16.2 Flash Memory Features**	
	Addition of **CHAPTER 18 ELECTRICAL SPECIFICATIONS**	**CHAPTER 18 ELECTRICAL SPECIFICATIONS**
	Addition of **CHAPTER 19 PACKAGE DRAWINGS**	**CHAPTER 19 PACKAGE DRAWINGS**
	Addition of **CHAPTER 20 RECOMMENDED SOLDERING CONDITIONS**	**CHAPTER 20 RECOMMENDED SOLDERING CONDITIONS**
	Change of **Table A-1 Major Differences Between uPD780232 and 780208 Subseries**	**APPENDIX A DIFFERENCES BETWEEN μPD780232 AND 780208 SUBSERIES**
	Modification of **APPENDIX B DEVELOPMENT TOOLS**	**APPENDIX B DEVELOPMENT TOOLS**
	Addition of **APPENDIX C CAUTIONS ON DESIGNING TARGET SYSTEM**	**APPENDIX C CAUTIONS ON DESIGNING TARGET SYSTEM**
	Addition of **APPENDIX E REVISION HISTORY**	**APPENDIX E REVISION HISTORY**