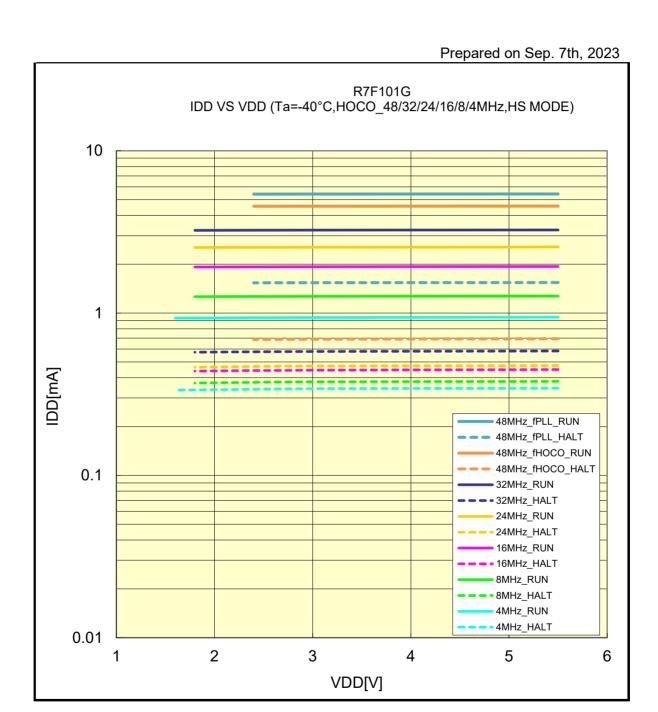
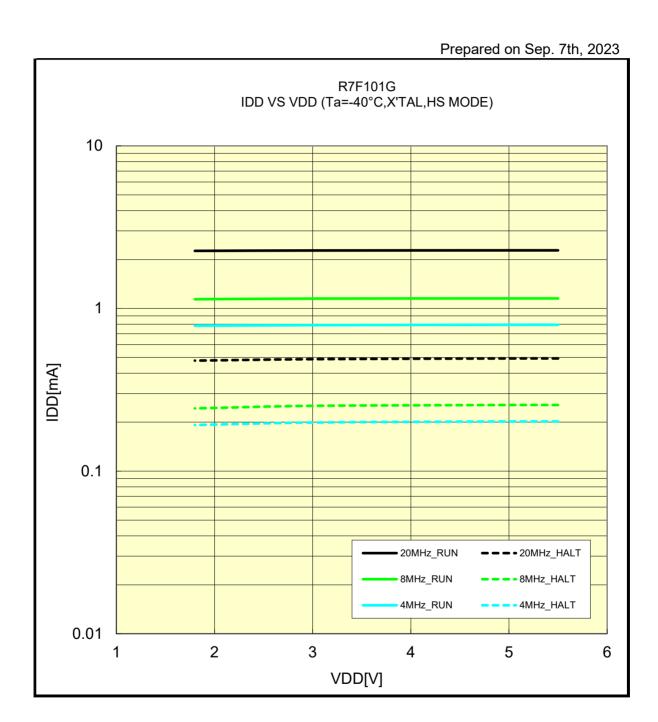
### IDD VS VDD(-40°C/HOCO\_48/32/24/16/8/4MHz/HS MODE)

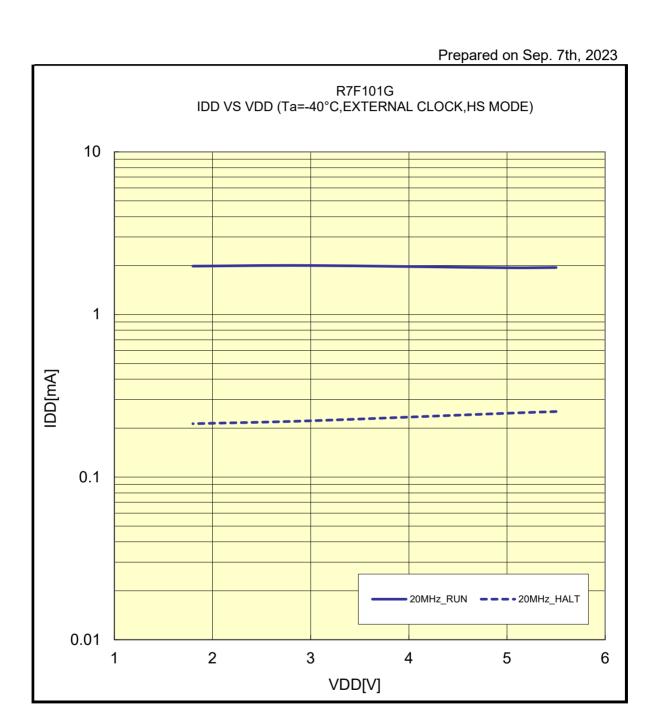


Remark 48MHz\_fPLL: fHOCO = 8MHz, fCLK = fPLL/2 = 48MHz, PFBE=1 48MHz\_fHOCO: fHOCO = fCLK = 48MHz, PFBE=1

## IDD VS VDD(-40°C/X'TAL/HS MODE)



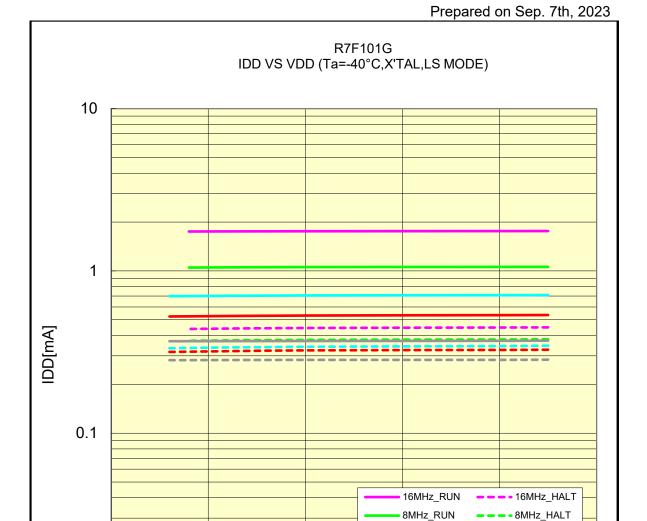
# IDD VS VDD(-40°C/EXTERNAL CLOCK/HS MODE)



0.01

2

# IDD VS VDD(-40°C/HOCO\_16/8/4/2/1MHz/LS MODE)



4MHz\_RUN

2MHz\_RUN

1MHz\_RUN

4

4MHz\_HALT

6

-- - 2MHz\_HALT

--- 1MHz\_HALT

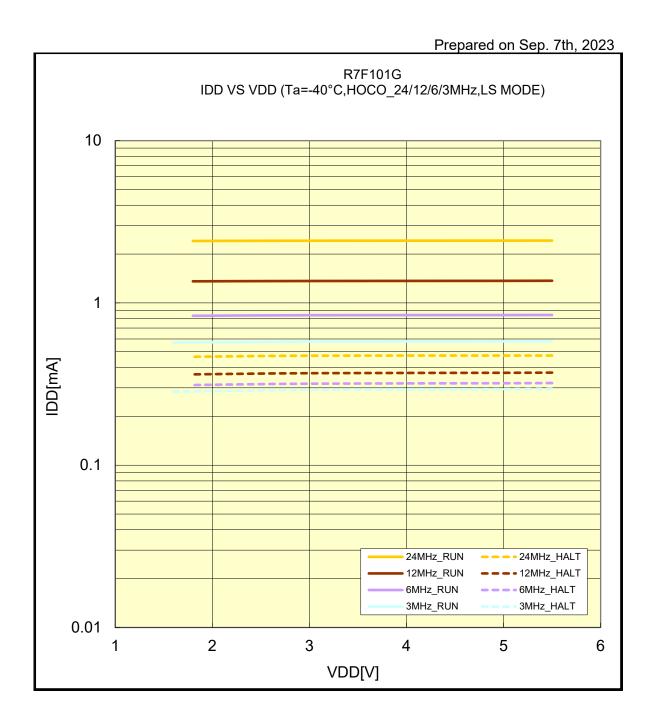
5

The above mentioned value is only for your reference. The value was measured under certain conditions and does not guarantee the product's characteristics.

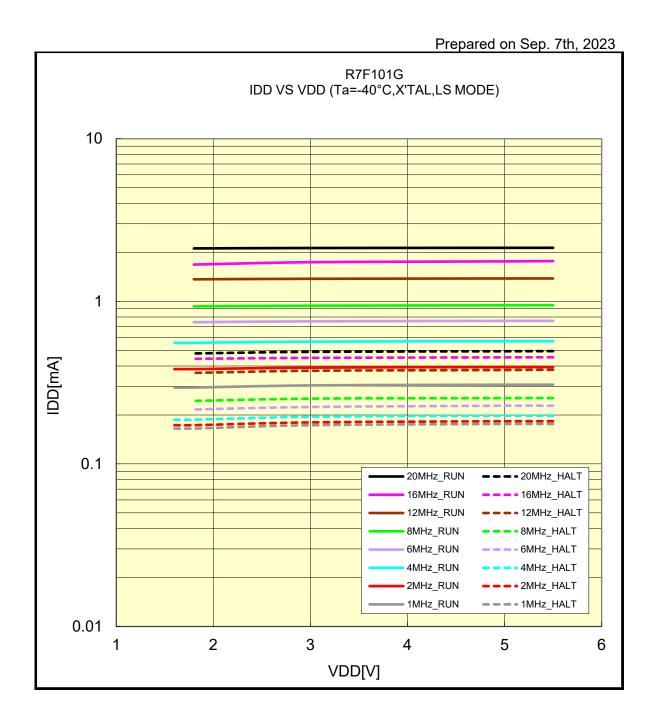
3

VDD[V]

## IDD VS VDD(-40°C/HOCO\_24/12/6/3MHz/LS MODE)

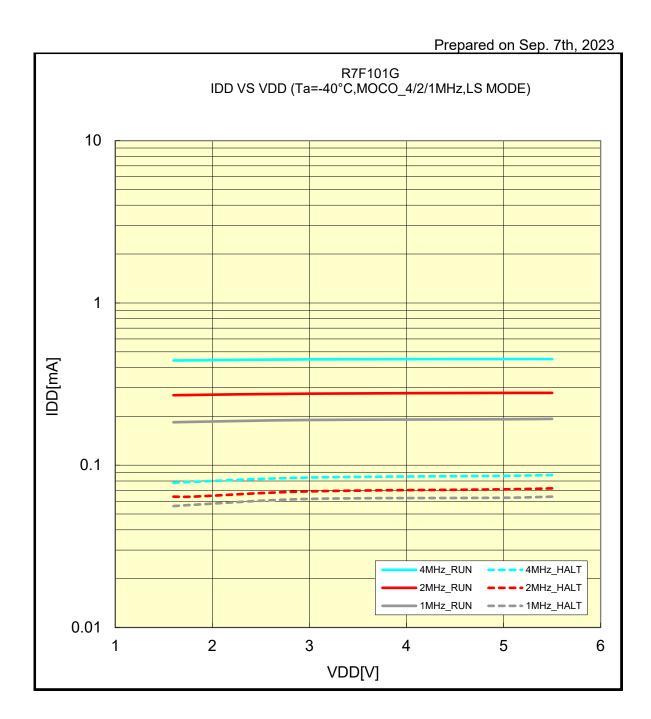


### IDD VS VDD(-40°C/X'TAL/LS MODE)

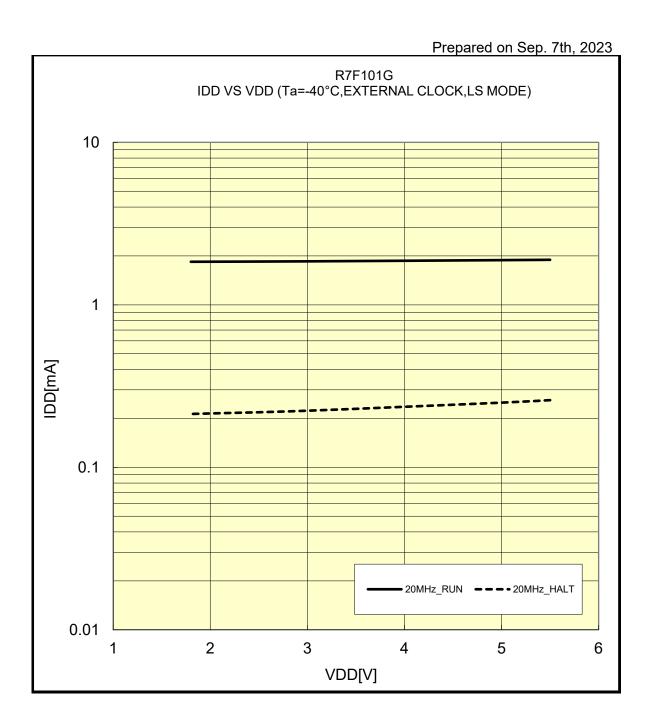


Remark 1MHz:4MHz/4 (MOSCDIV = 02H) 2MHz:4MHz/2 (MOSCDIV = 01H)

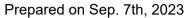
# IDD VS VDD(-40°C/MOCO\_4/2/1MHz/LS MODE)

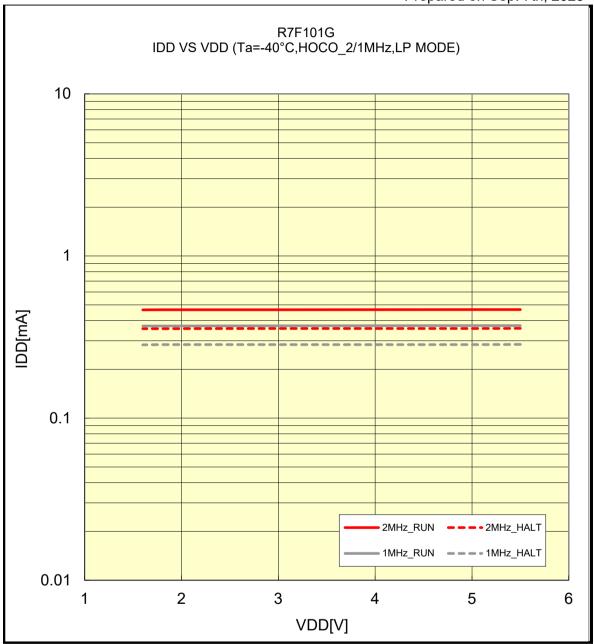


# IDD VS VDD(-40°C/EXTERNAL CLOCK/LS MODE)

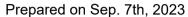


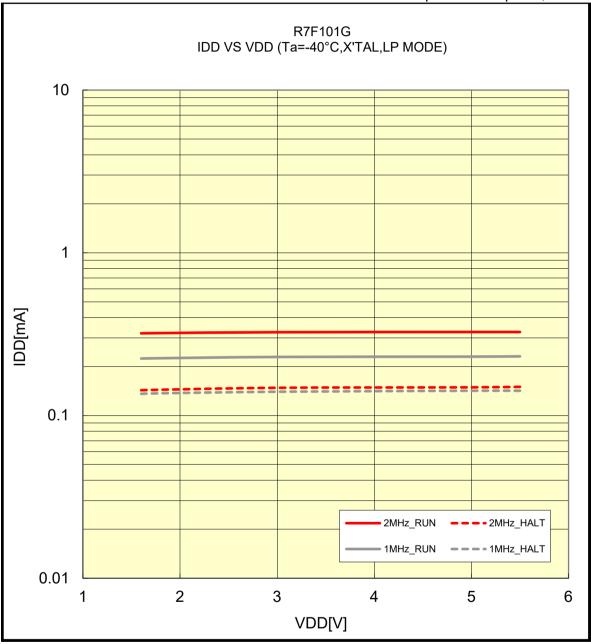
# IDD VS VDD(-40°C/HOCO\_2/1MHz/LP MODE)





## IDD VS VDD(-40°C/X'TAL/LP MODE)



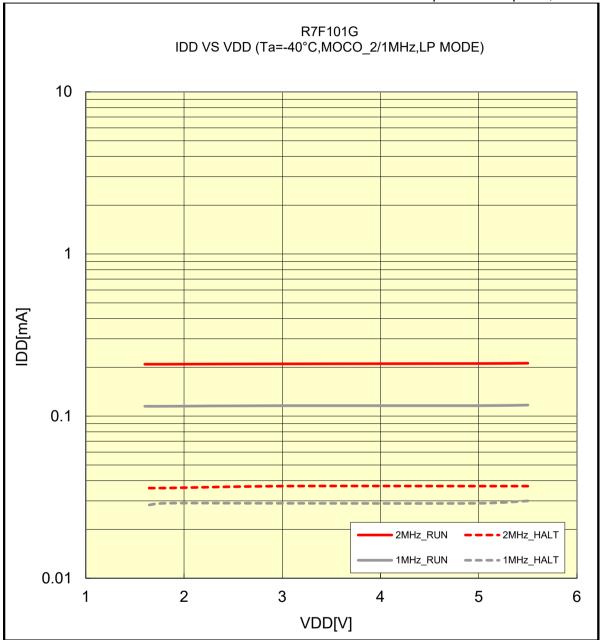


Remark 1MHz:4MHz/4 (MOSCDIV = 02H)

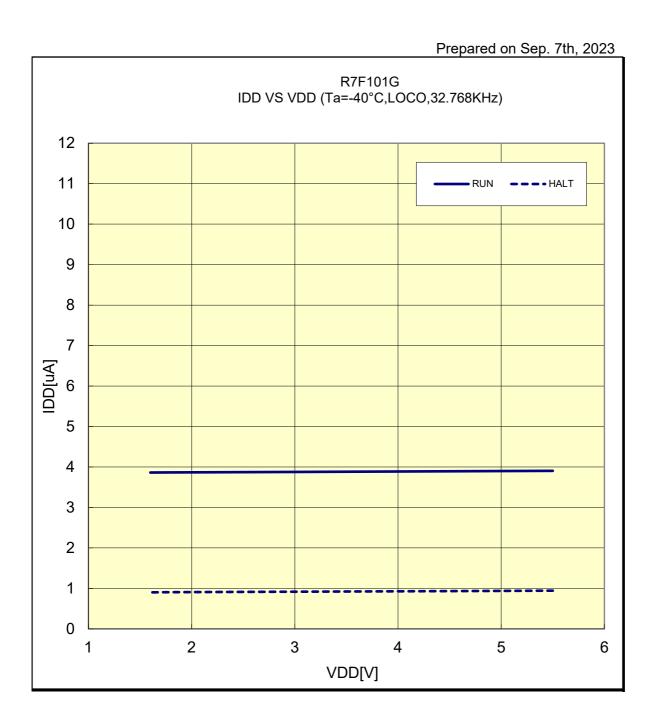
2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(-40°C/MOCO\_2/1MHz/LP MODE)

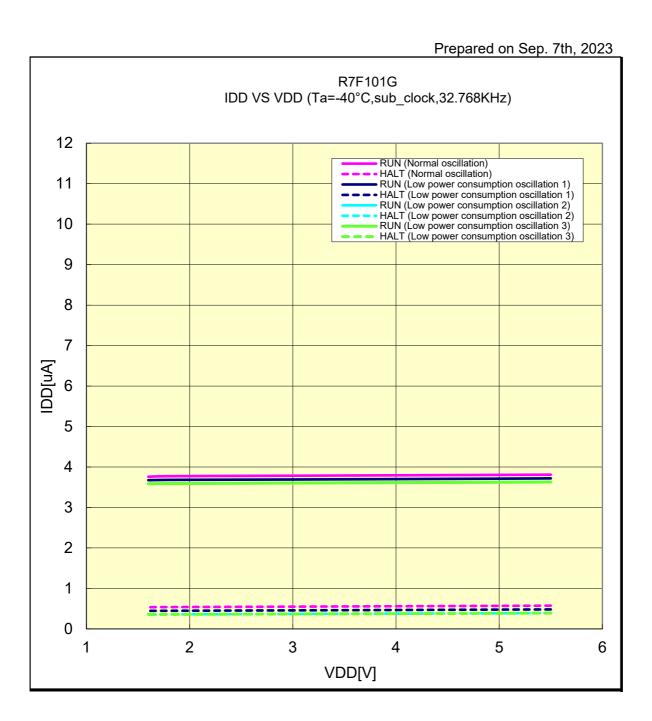




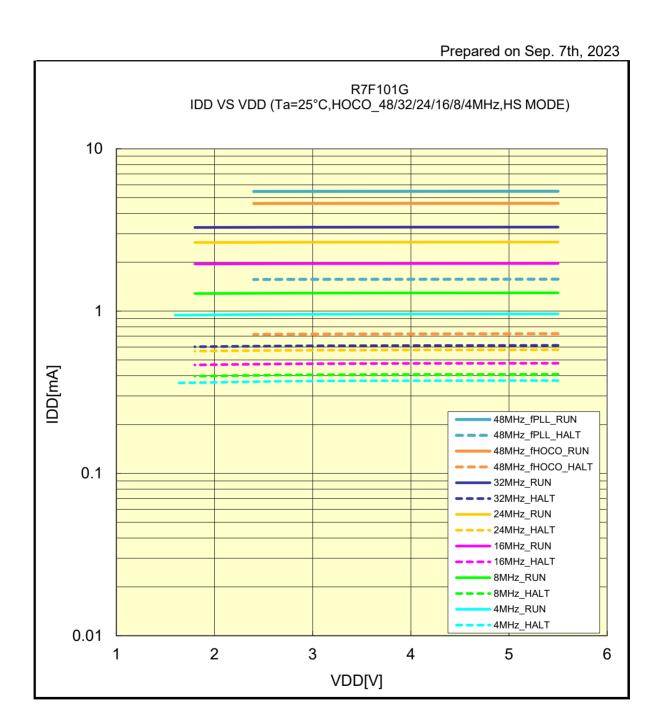
# IDD VS VDD(-40°C/LOCO/32.768KHz)



# IDD VS VDD(-40°C/sub\_clock/32.768KHz)

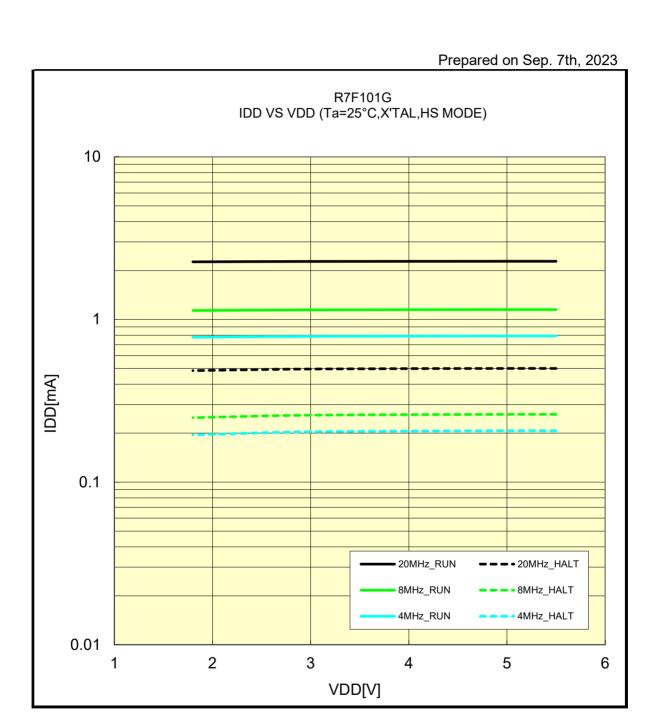


### IDD VS VDD(25°C/HOCO\_48/32/24/16/8/4MHz/HS MODE)

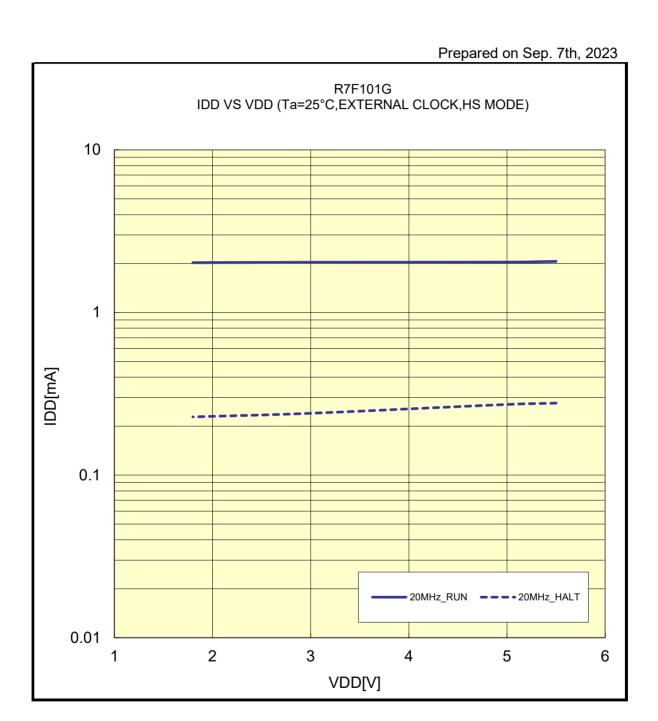


Remark 48MHz\_fPLL: fHOCO = 8MHz, fCLK = fPLL/2 = 48MHz, PFBE=1 48MHz\_fHOCO: fHOCO = fCLK = 48MHz, PFBE=1

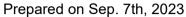
## IDD VS VDD(25°C/X'TAL/HS MODE)

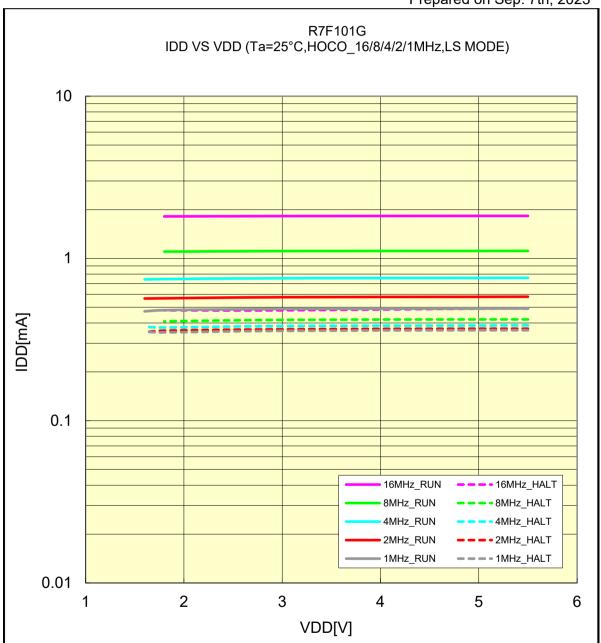


# IDD VS VDD(25°C/EXTERNAL CLOCK/HS MODE)

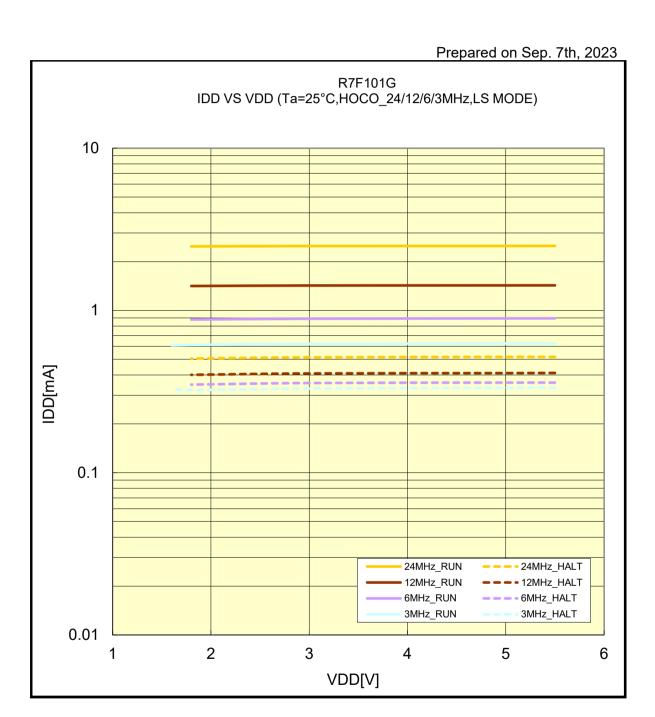


## IDD VS VDD(25°C/HOCO\_16/8/4/2/1MHz/LS MODE)

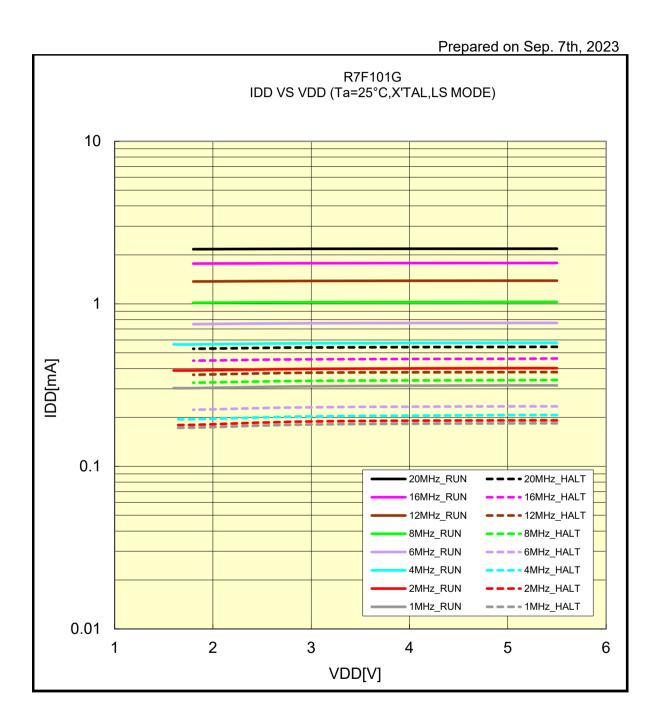




## IDD VS VDD(25°C/HOCO\_24/12/6/3MHz/LS MODE)

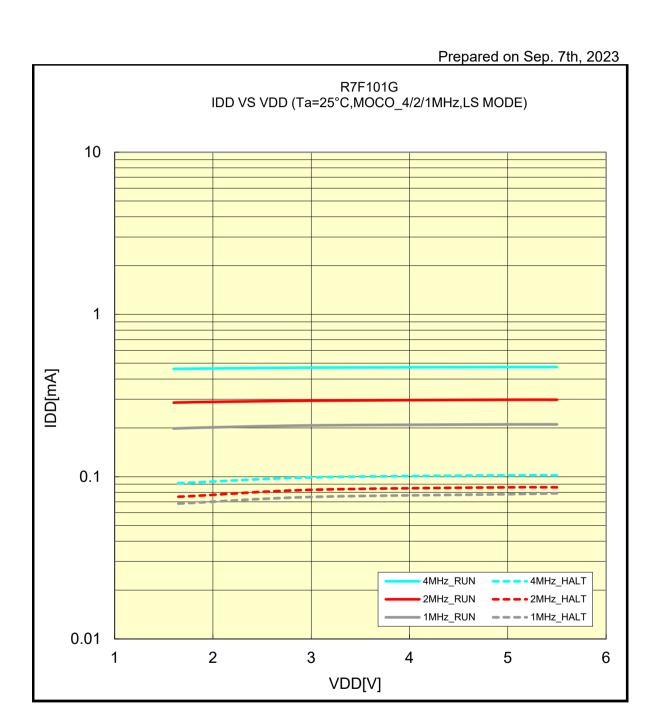


## IDD VS VDD(25°C/X'TAL/LS MODE)

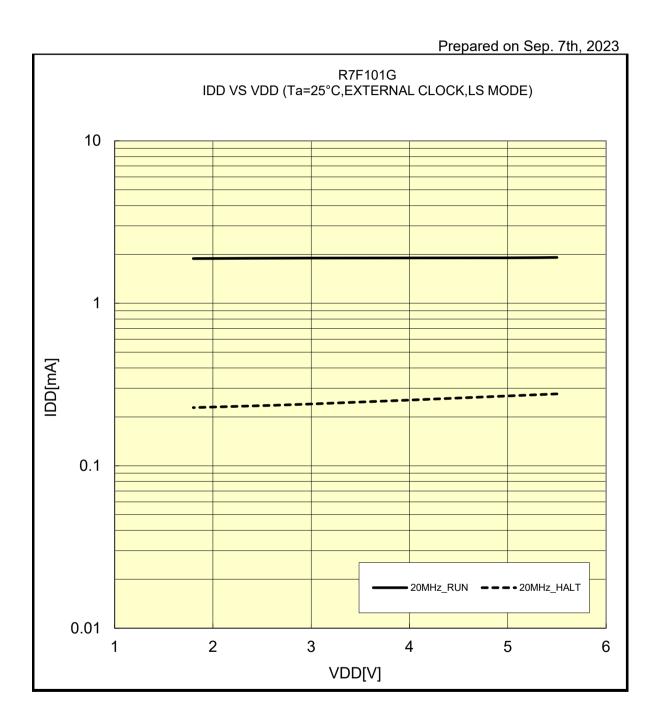


Remark 1MHz:4MHz/4 (MOSCDIV = 02H) 2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(25°C/MOCO\_4/2/1MHz/LS MODE)

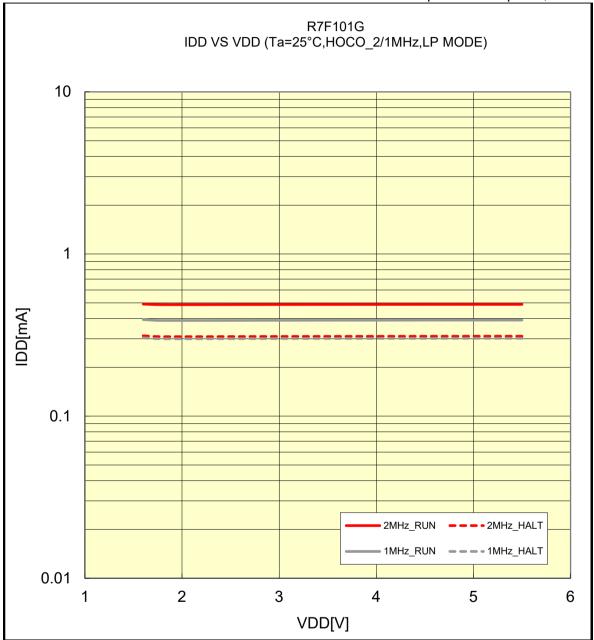


## IDD VS VDD(25°C/EXTERNAL CLOCK/LS MODE)

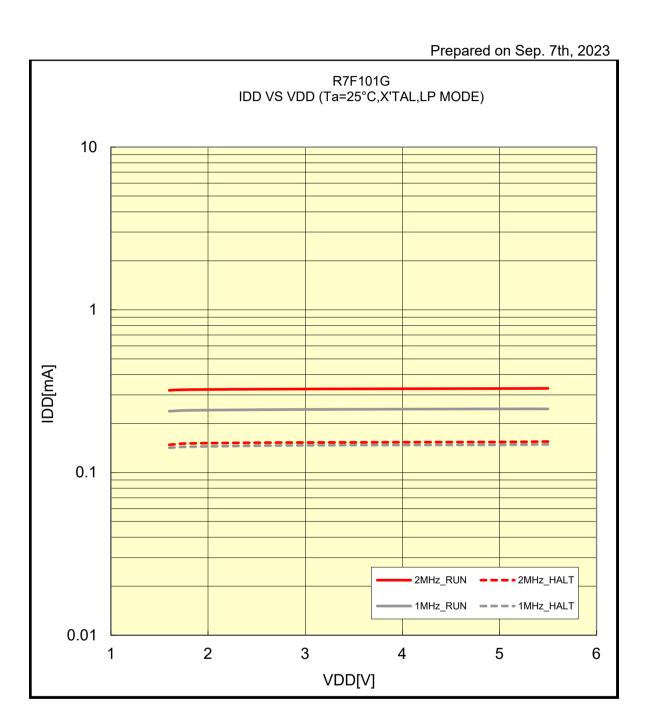


# IDD VS VDD(25°C/HOCO\_2/1MHz/LP MODE)





# IDD VS VDD(25°C/X'TAL/LP MODE)

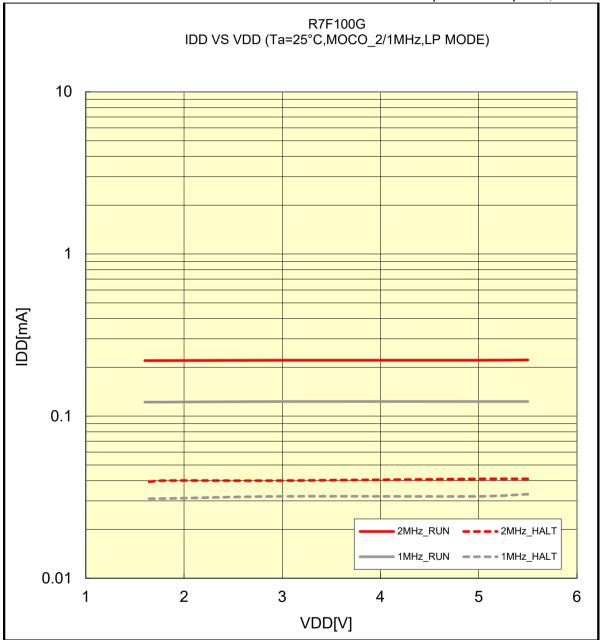


Remark 1MHz:4MHz/4 (MOSCDIV = 02H)

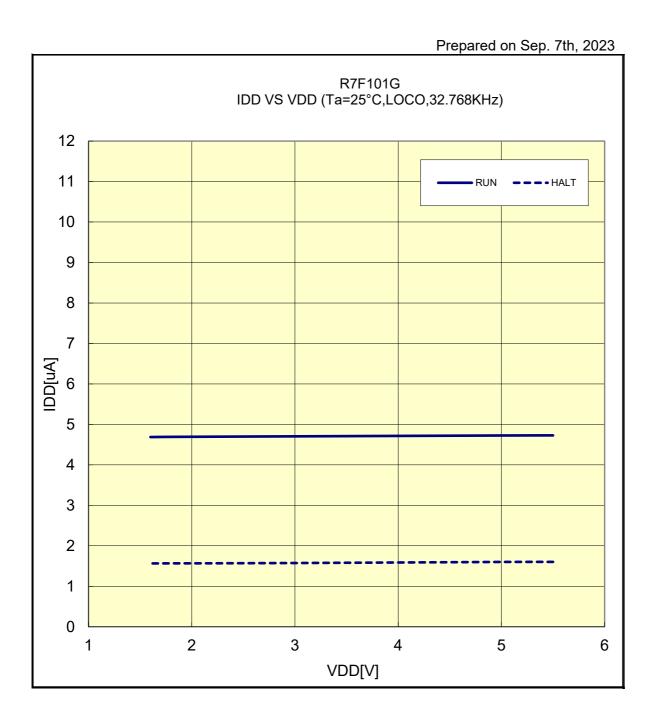
2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(25°C/MOCO\_2/1MHz/LP MODE)

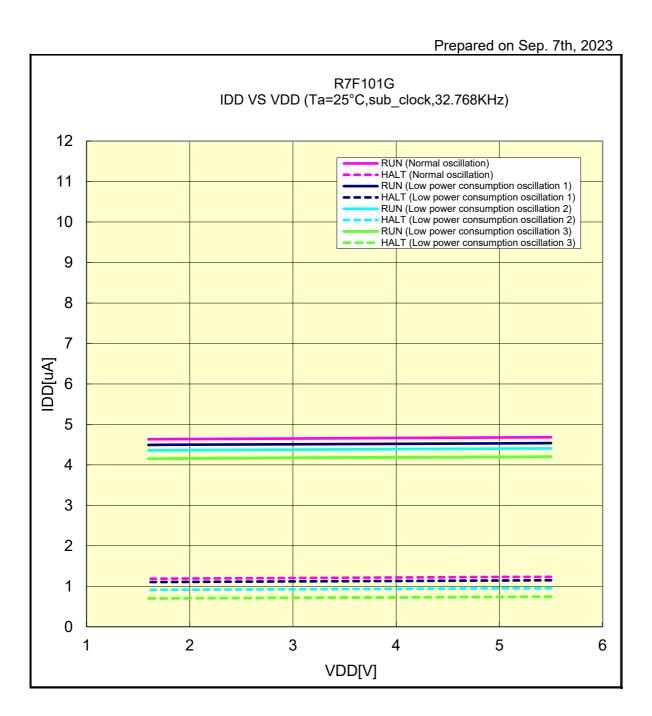




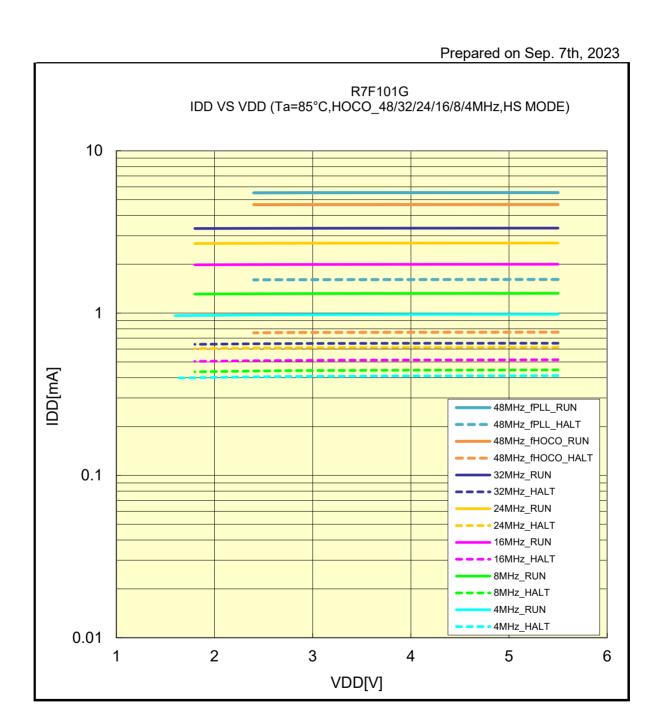
# IDD VS VDD(25°C/LOCO/32.768KHz)



# IDD VS VDD(25°C/sub\_clock/32.768KHz)

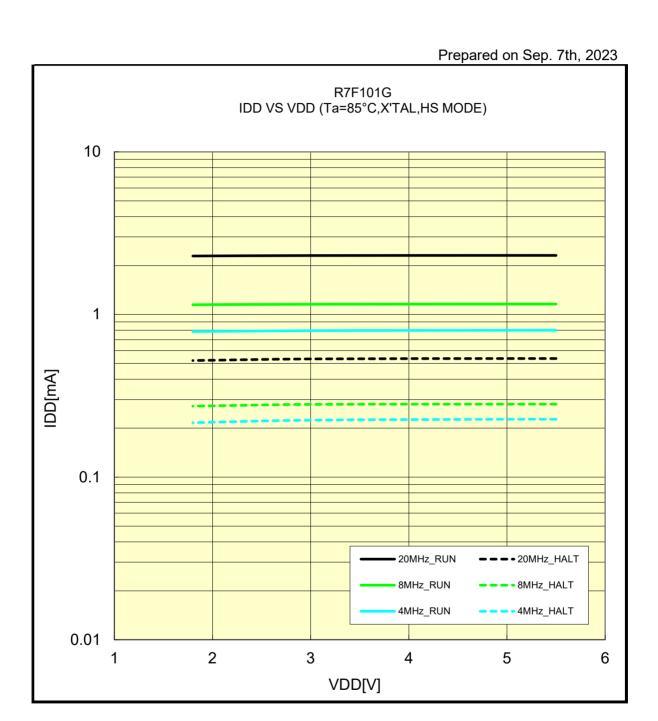


### IDD VS VDD(85°C/HOCO\_48/32/24/16/8/4MHz/HS MODE)

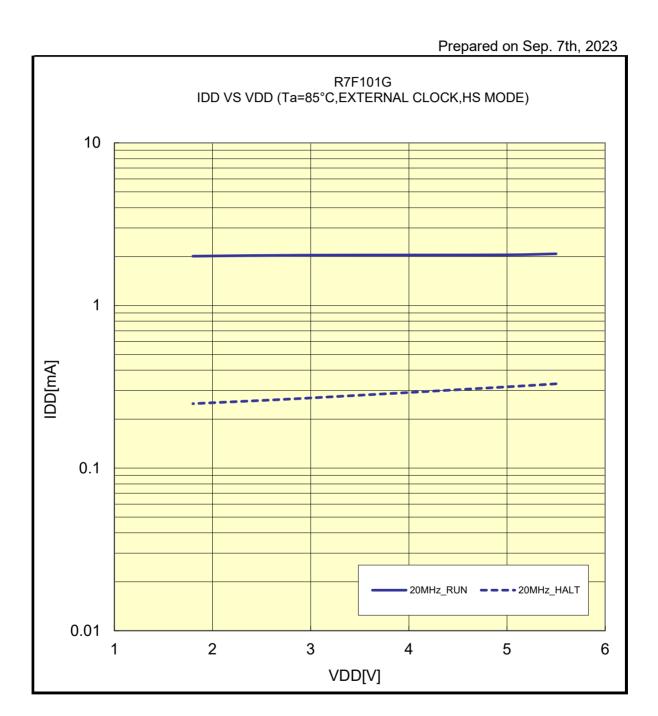


Remark 48MHz\_fPLL: fHOCO = 8MHz, fCLK = fPLL/2 = 48MHz, PFBE=1 48MHz\_fHOCO: fHOCO = fCLK = 48MHz, PFBE=1

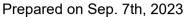
## IDD VS VDD(85°C/X'TAL/HS MODE)

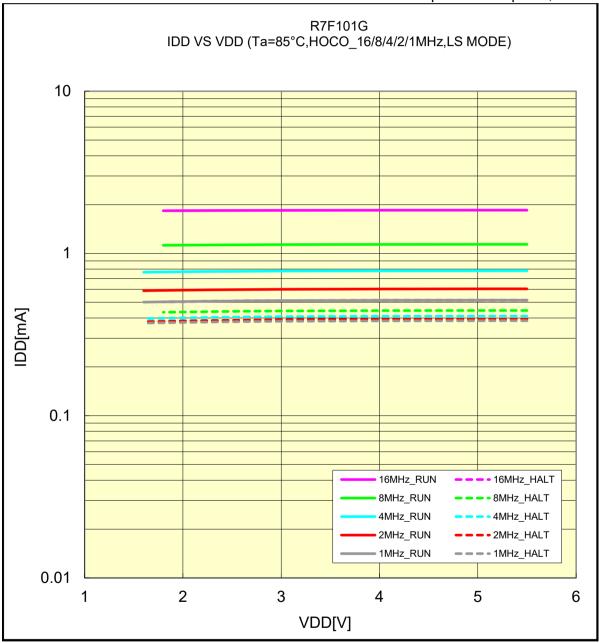


# IDD VS VDD(85°C/EXTERNAL CLOCK/HS MODE)



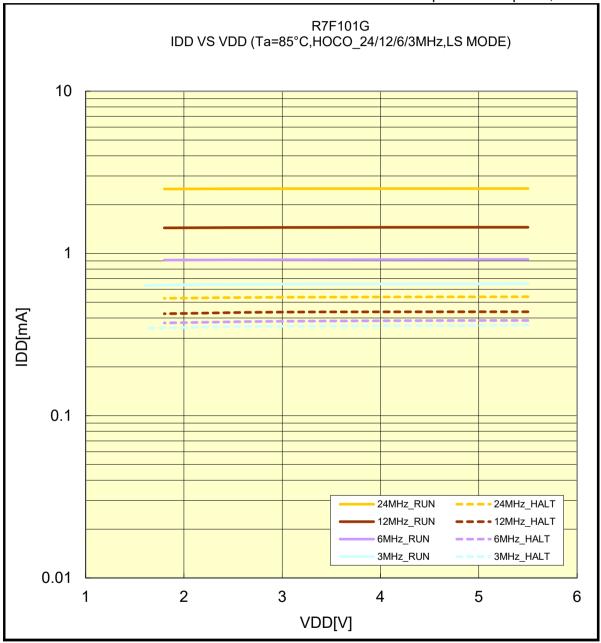
## IDD VS VDD(85°C/HOCO\_16/8/4/2/1MHz/LS MODE)



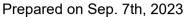


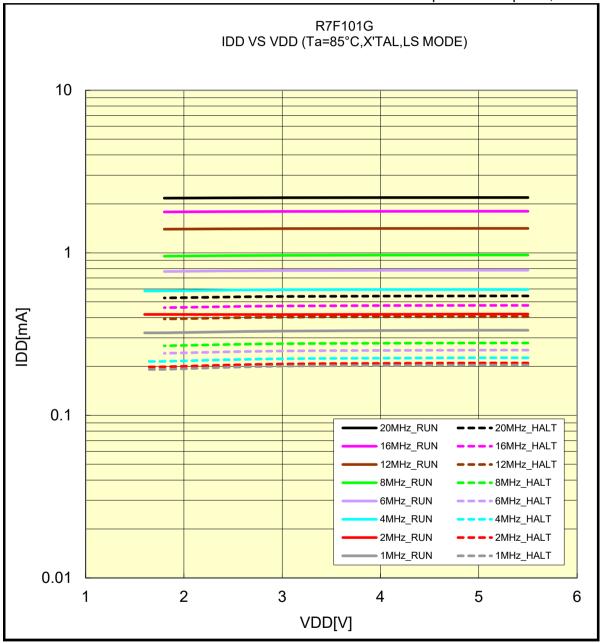
# IDD VS VDD(85°C/HOCO\_24/12/6/3MHz/LS MODE)





## IDD VS VDD(85°C/X'TAL/LS MODE)

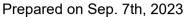


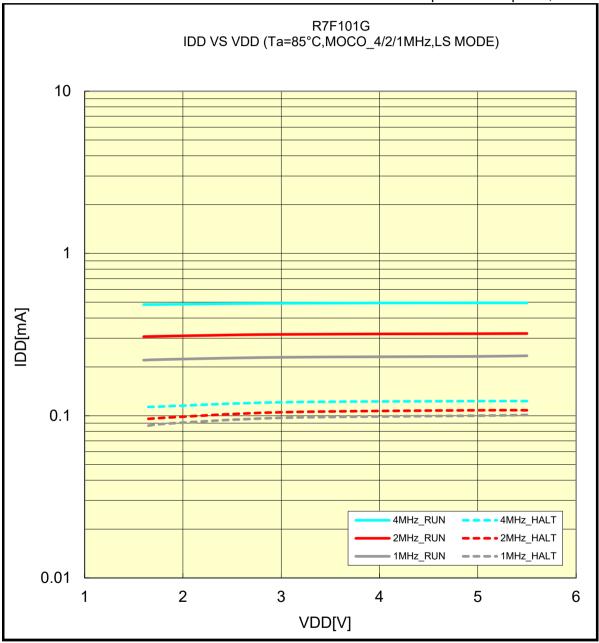


Remark 1MHz:4MHz/4 (MOSCDIV = 02H)

2MHz:4MHz/2 (MOSCDIV = 01H)

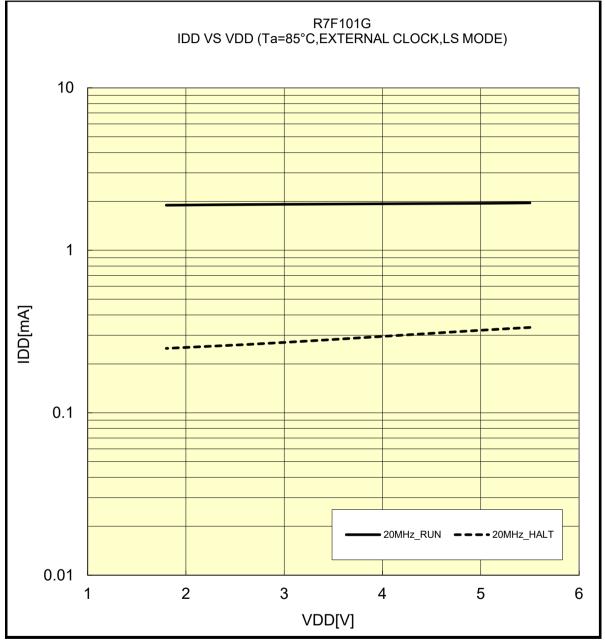
# IDD VS VDD(85°C/MOCO\_4/2/1MHz/LS MODE)



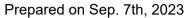


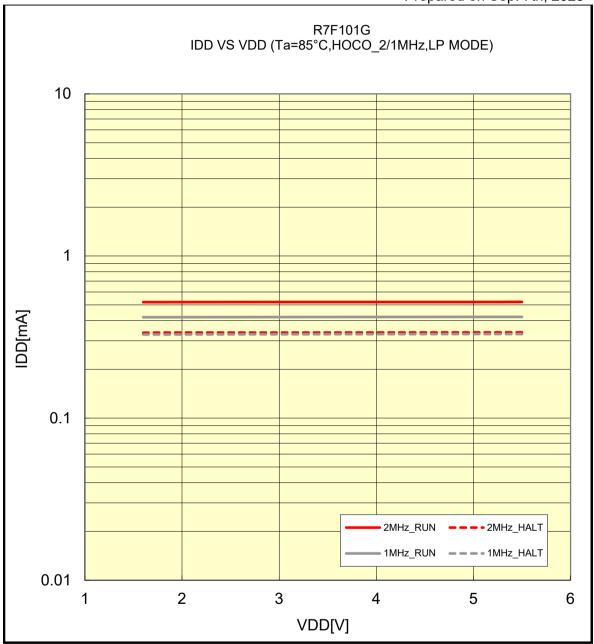
# IDD VS VDD(85°C/EXTERNAL CLOCK/LS MODE)



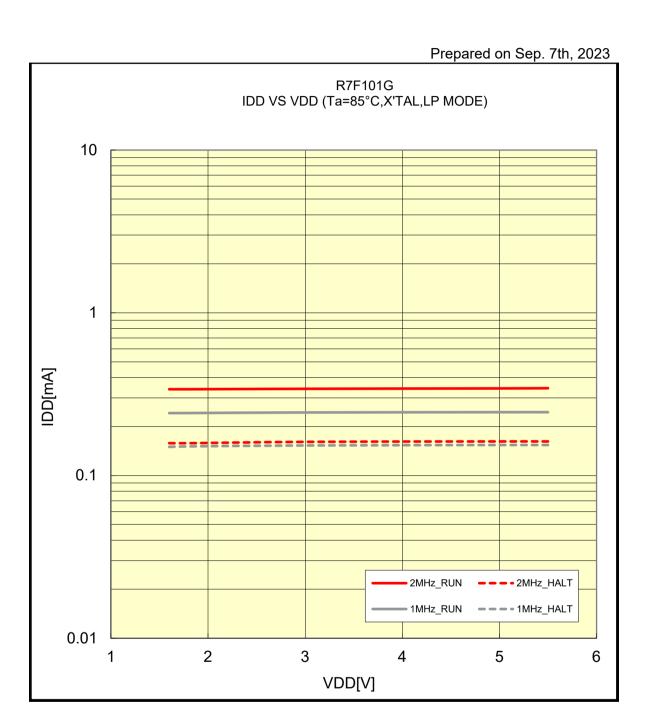


# IDD VS VDD(85°C/HOCO\_2/1MHz/LP MODE)





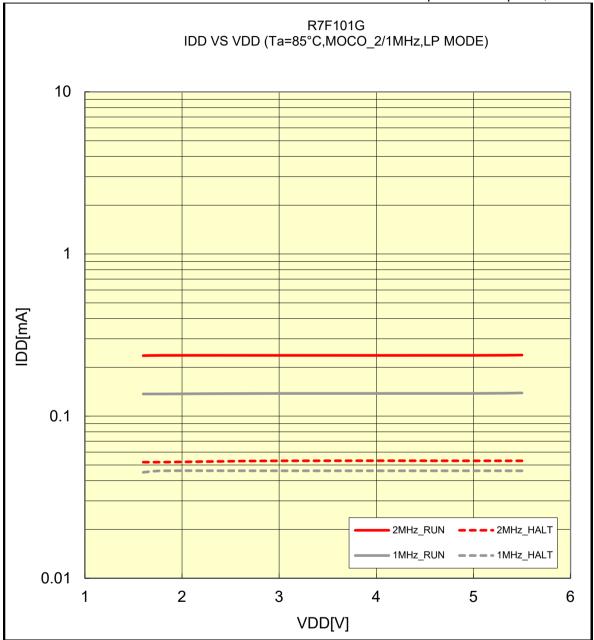
# IDD VS VDD(85°C/X'TAL/LP MODE)



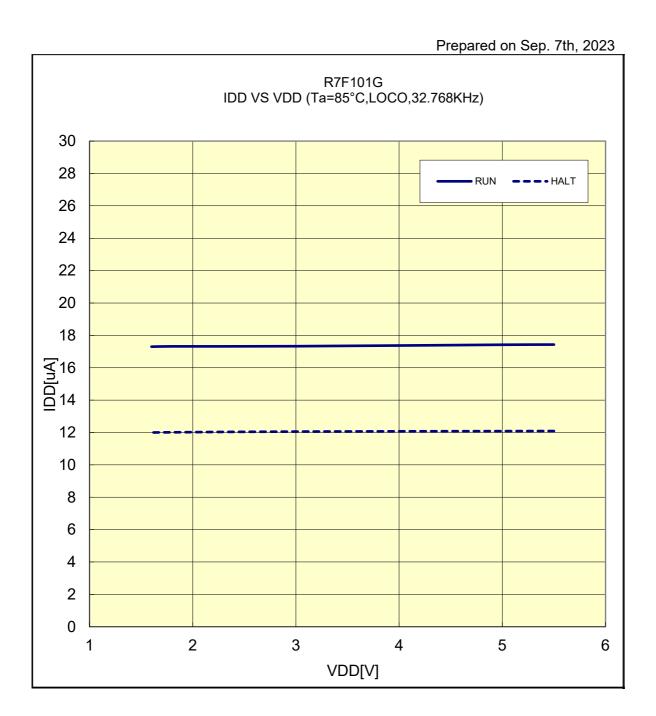
Remark 1MHz:4MHz/4 (MOSCDIV = 02H) 2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(85°C/MOCO\_2/1MHz/LP MODE)

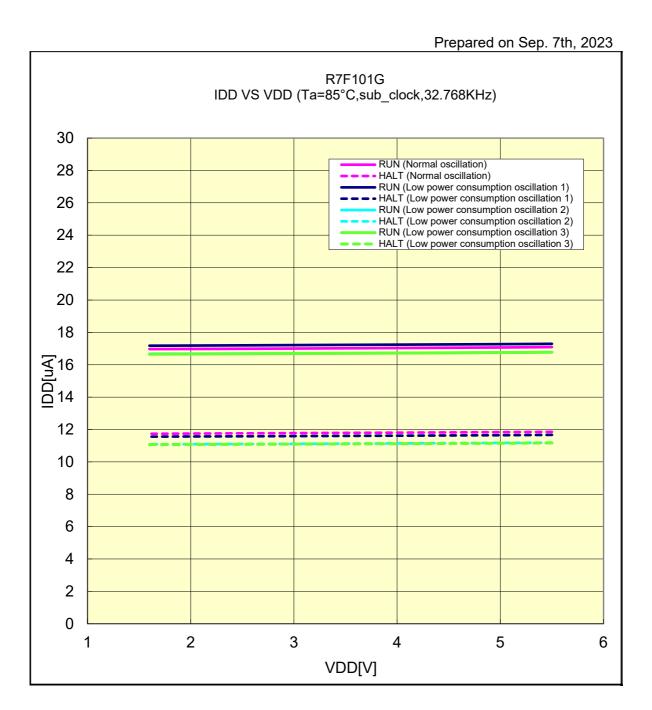




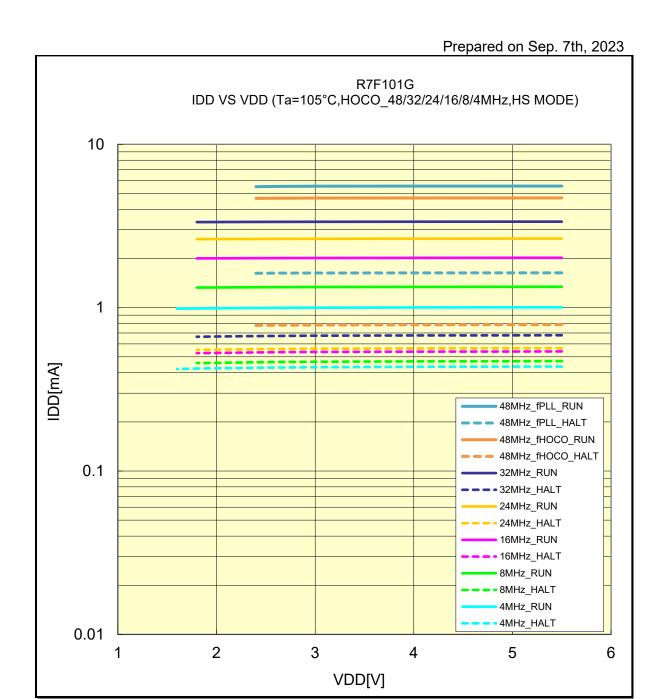
# IDD VS VDD(85°C/LOCO/32.768KHz)



## IDD VS VDD(85°C/sub\_clock/32.768KHz)

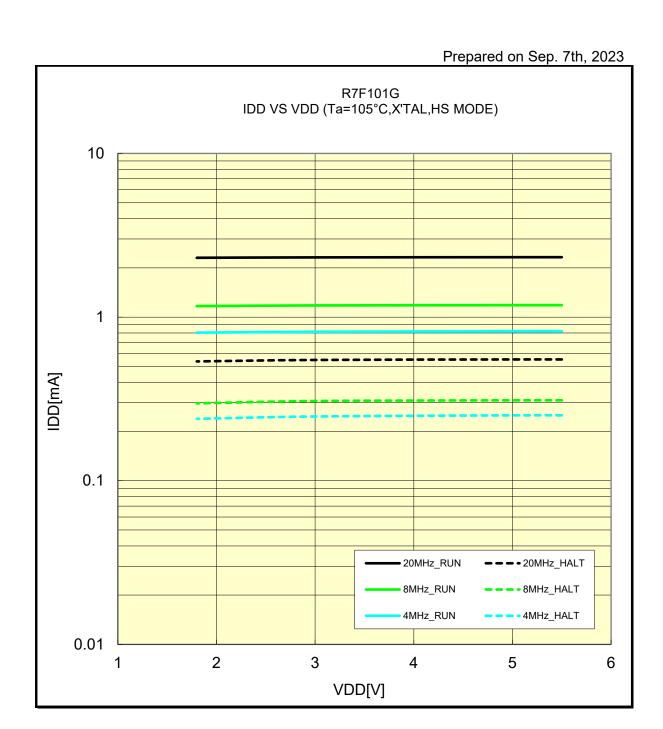


# IDD VS VDD(105°C/HOCO\_48/32/24/16/8/4MHz/HS MODE)

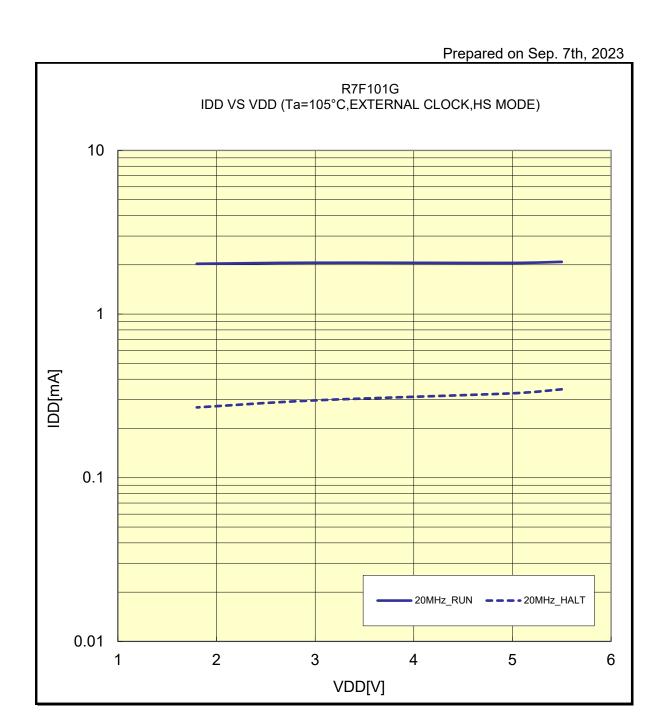


Remark 48MHz\_fPLL: fHOCO = 8MHz, fCLK = fPLL/2 = 48MHz, PFBE=1 48MHz fHOCO: fHOCO = fCLK = 48MHz, PFBE=1

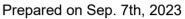
# IDD VS VDD(105°C/X'TAL/HS MODE)

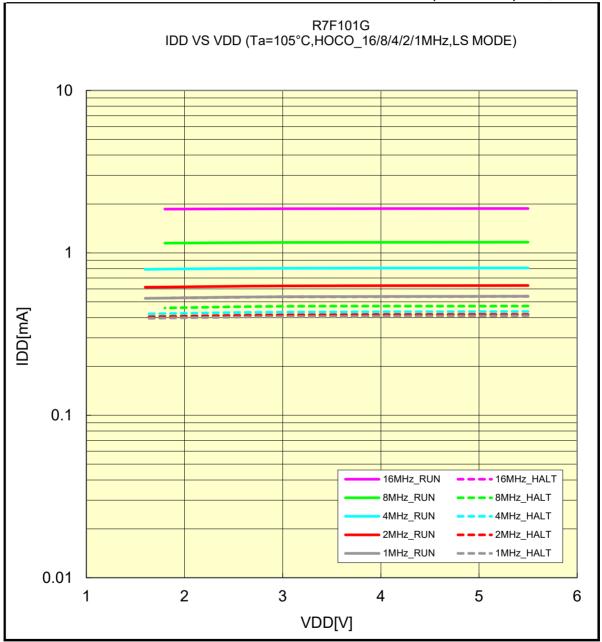


# IDD VS VDD(105°C/EXTERNAL CLOCK/HS MODE)



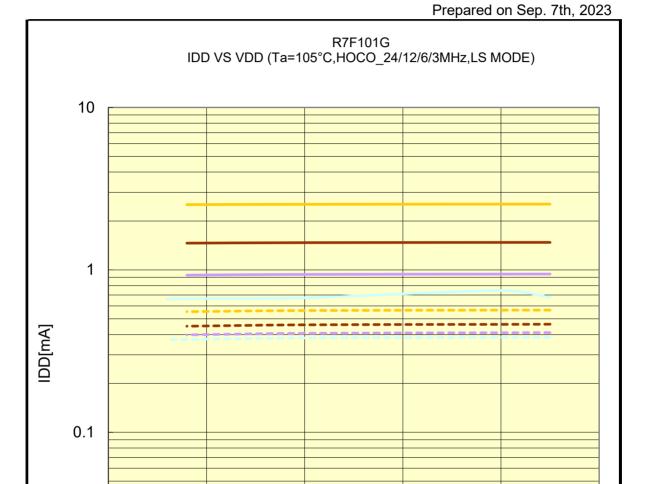
# IDD VS VDD(105°C/HOCO\_16/8/4/2/1MHz/LS MODE)





0.01

## IDD VS VDD(105°C/HOCO\_24/12/6/3MHz/LS MODE)



24MHz\_RUN

12MHz\_RUN

6MHz\_RUN

3MHz\_RUN

4

- 24MHz\_HALT

• 12MHz\_HALT

6MHz\_HALT

3MHz\_HALT

6

5

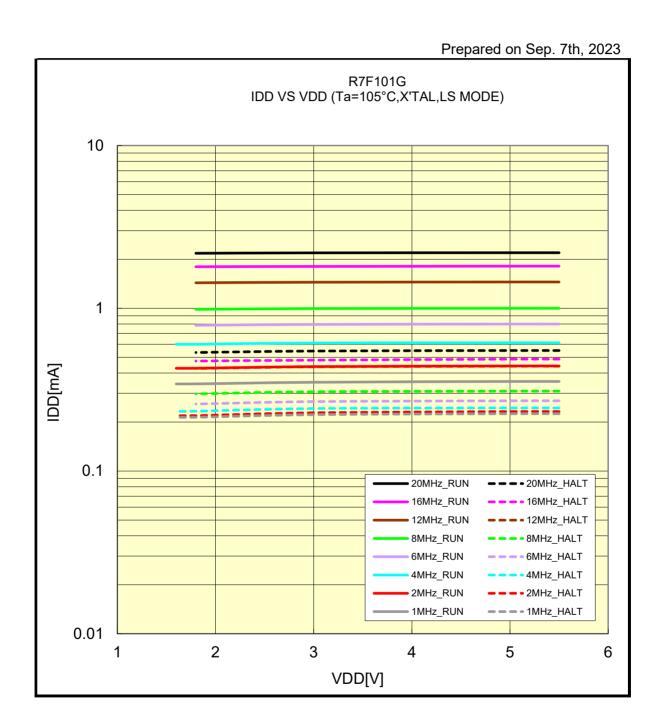
The above mentioned value is only for your reference. The value was measured under certain conditions and does not guarantee the product's characteristics.

3

VDD[V]

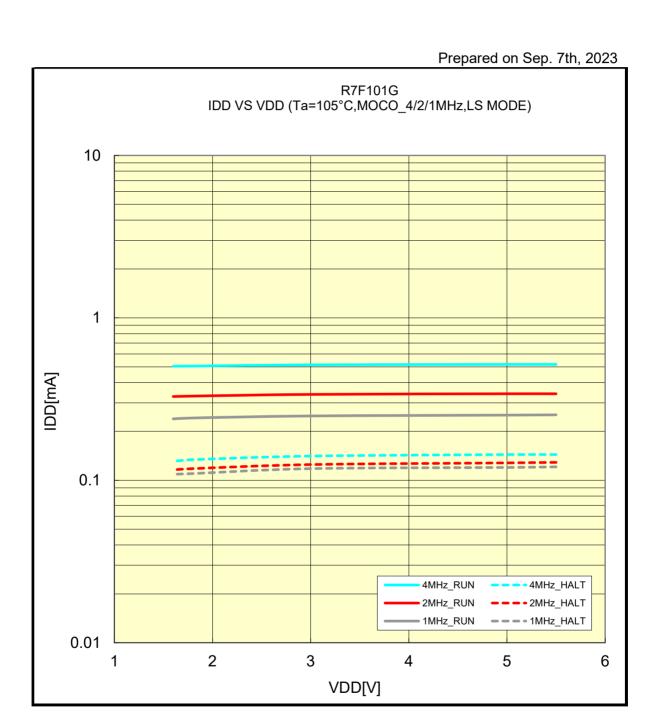
2

## IDD VS VDD(105°C/X'TAL/LS MODE)

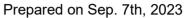


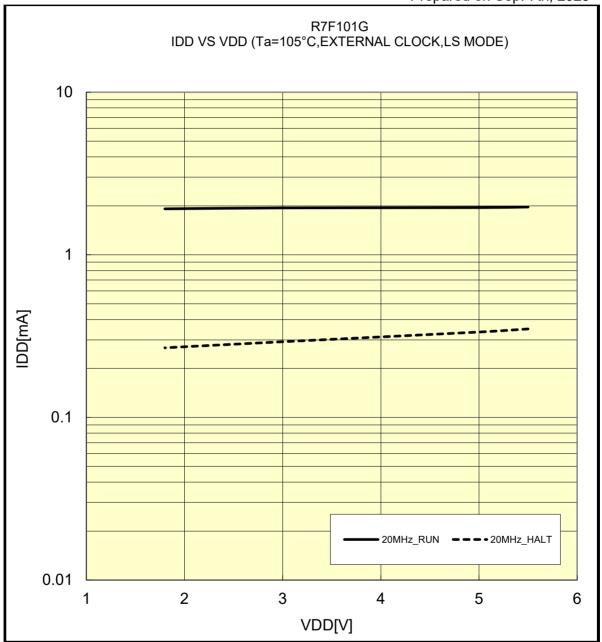
Remark 1MHz:4MHz/4 (MOSCDIV = 02H) 2MHz:4MHz/2 (MOSCDIV = 01H)

## IDD VS VDD(105°C/MOCO\_4/2/1MHz/LS MODE)



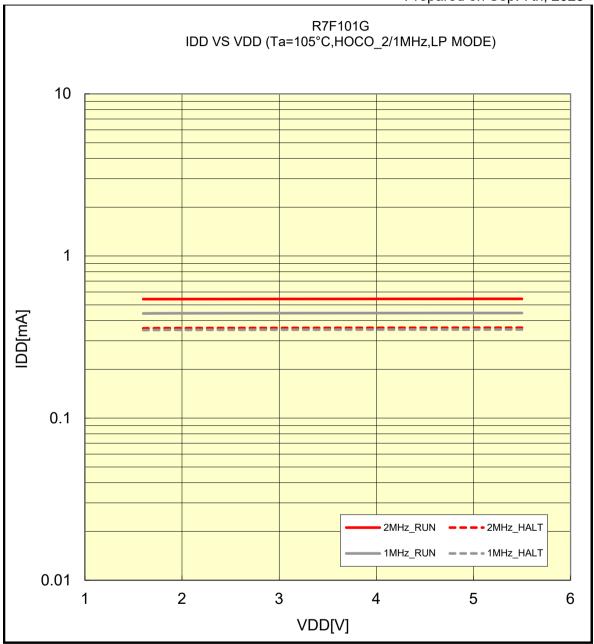
## IDD VS VDD(105°C/EXTERNAL CLOCK/LS MODE)



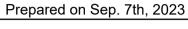


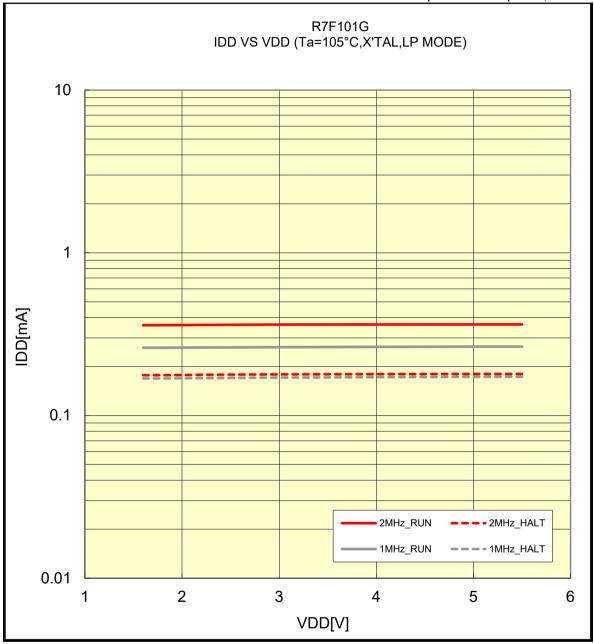
# IDD VS VDD(105°C/HOCO\_2/1MHz/LP MODE)





## IDD VS VDD(105°C/X'TAL/LP MODE)



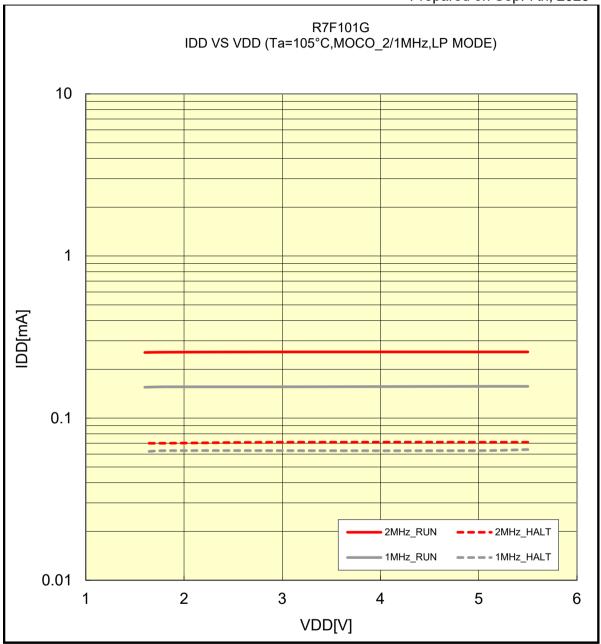


Remark 1MHz:4MHz/4 (MOSCDIV = 02H)

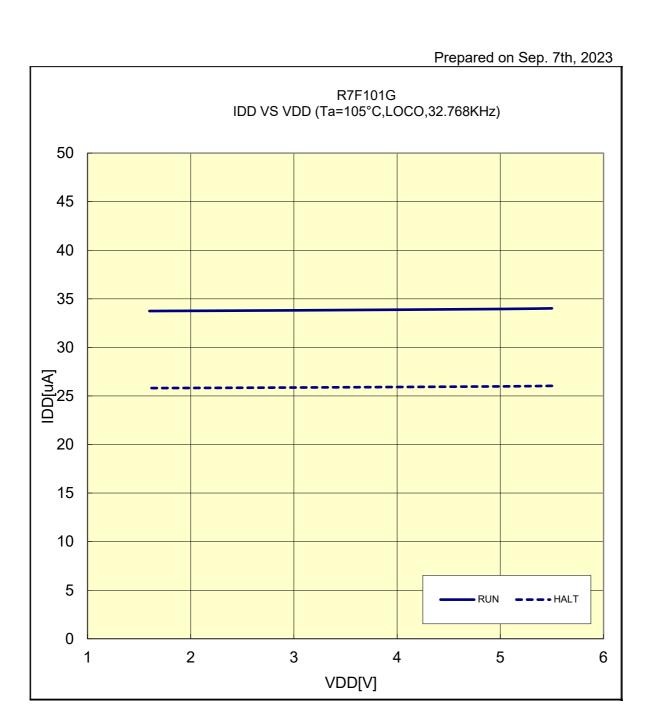
2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(105°C/MOCO\_2/1MHz/LP MODE)

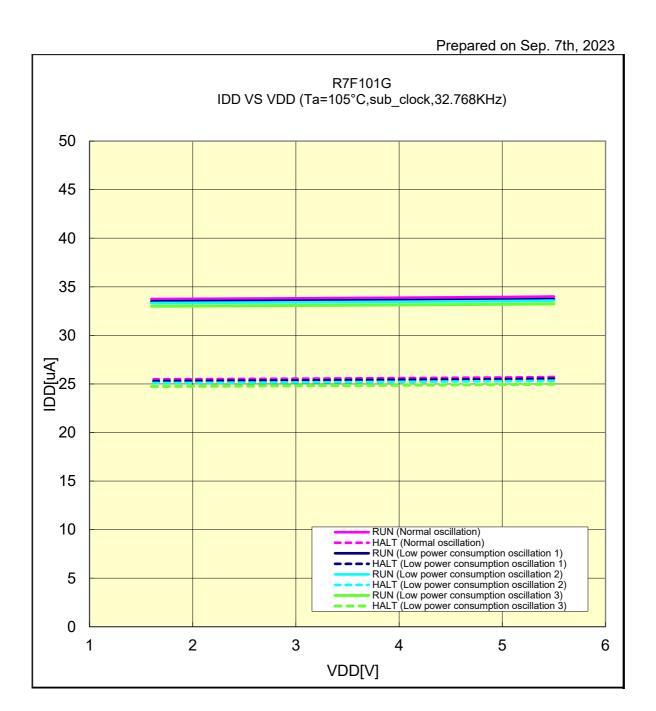




# IDD VS VDD(105°C/LOCO/32.768KHz)

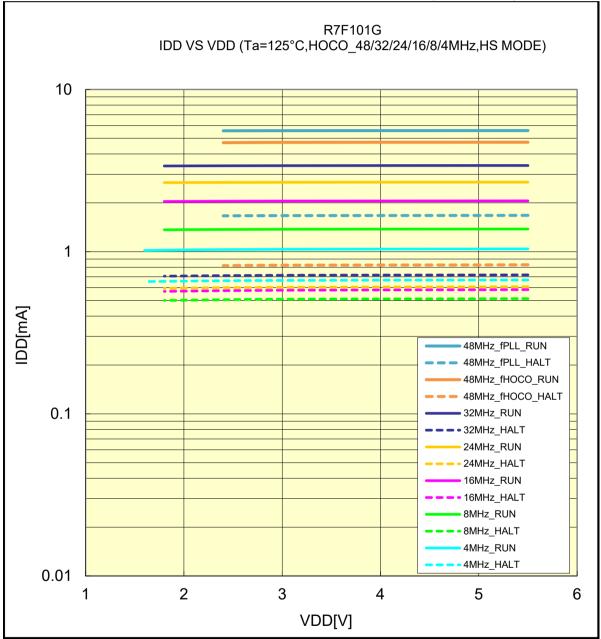


## IDD VS VDD(105°C/sub\_clock/32.768KHz)



## IDD VS VDD(125°C/HOCO\_48/32/24/16/8/4MHz/HS MODE)

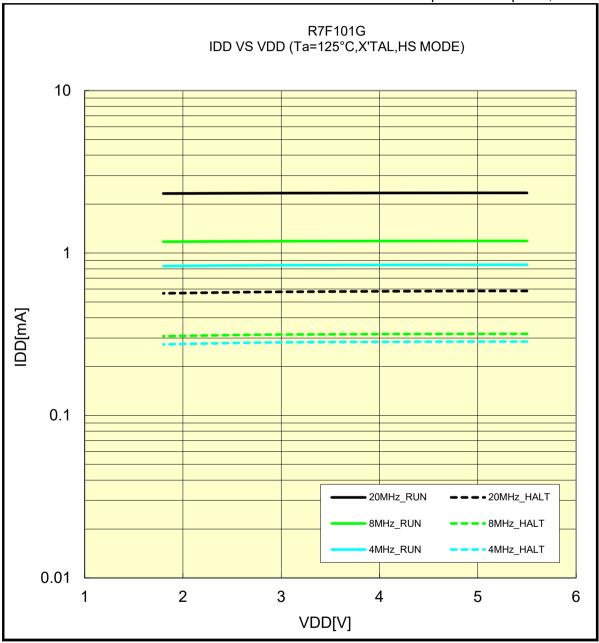




Remark 48MHz\_fPLL: fHOCO = 8MHz, fCLK = fPLL/2 = 48MHz, PFBE=1 48MHz fHOCO: fHOCO = fCLK = 48MHz, PFBE=1

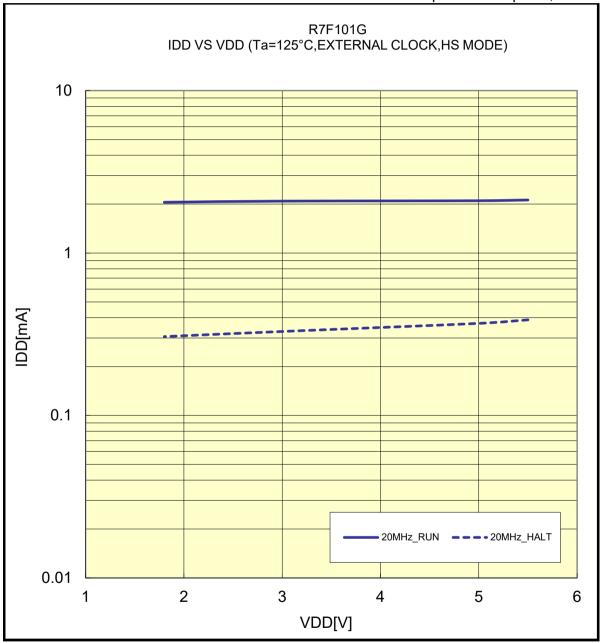
# IDD VS VDD(125°C/X'TAL/HS MODE)



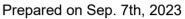


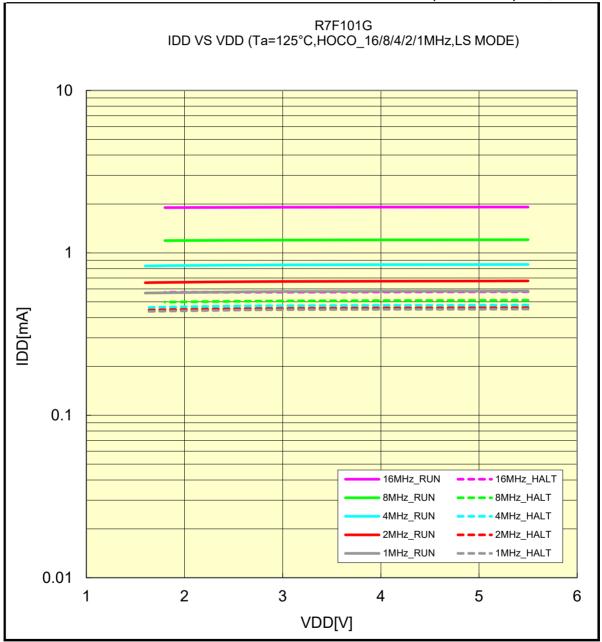
# IDD VS VDD(125°C/EXTERNAL CLOCK/HS MODE)





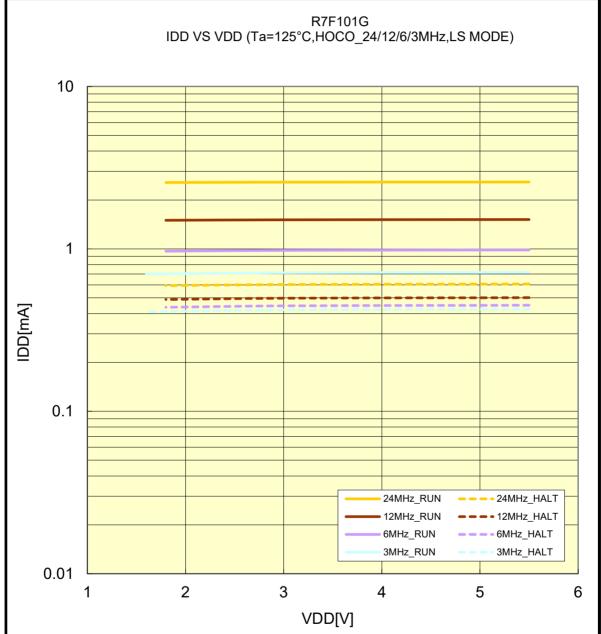
## IDD VS VDD(125°C/HOCO\_16/8/4/2/1MHz/LS MODE)



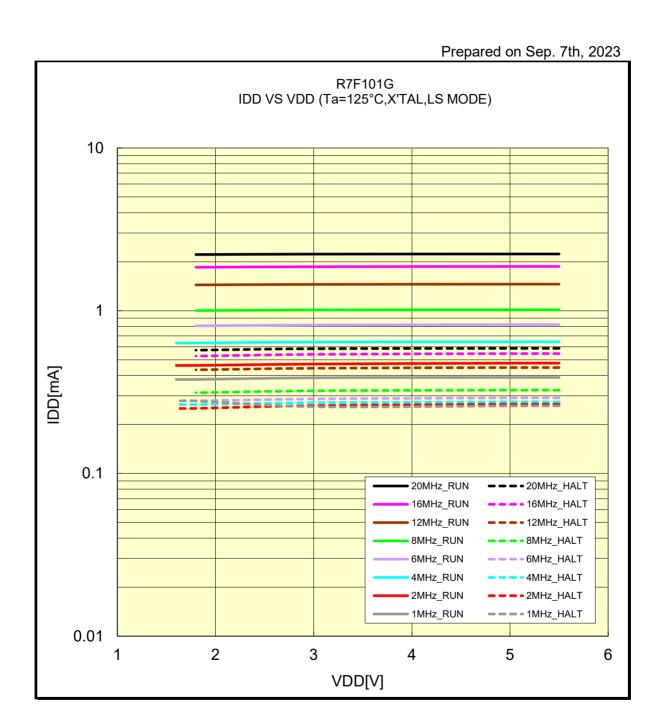


## IDD VS VDD(125°C/HOCO\_24/12/6/3MHz/LS MODE)





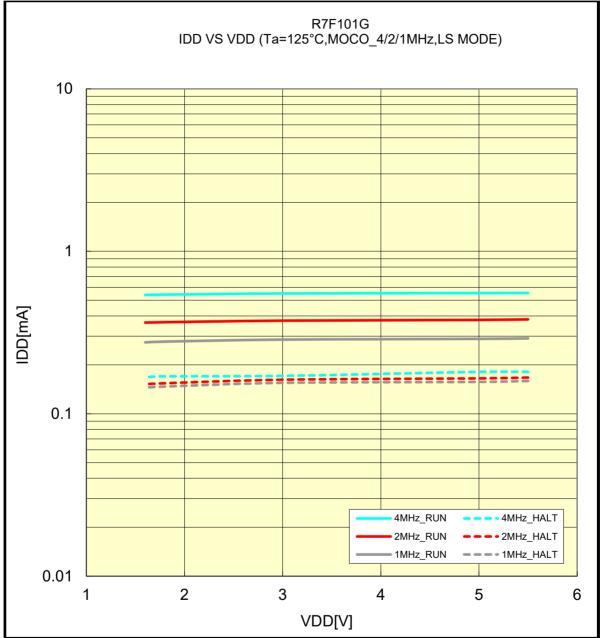
## IDD VS VDD(125°C/X'TAL/LS MODE)



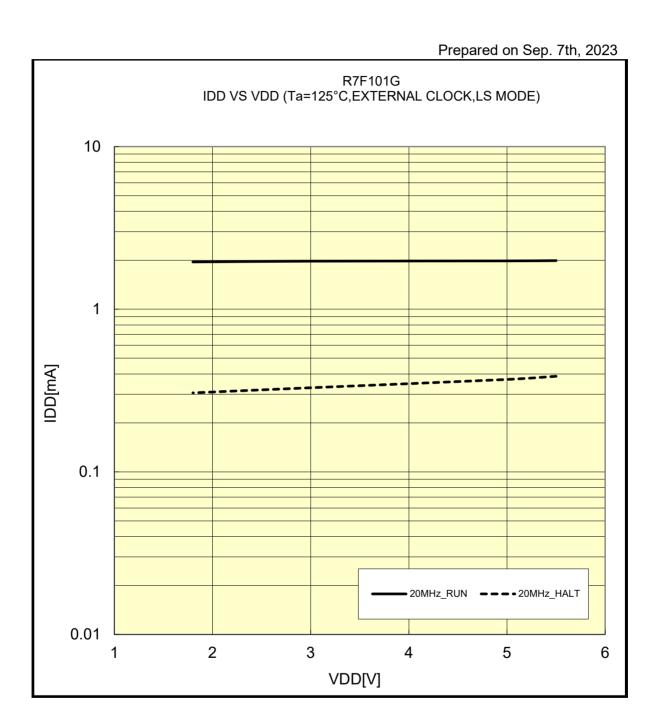
Remark 1MHz:4MHz/4 (MOSCDIV = 02H) 2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(125°C/MOCO\_4/2/1MHz/LS MODE)



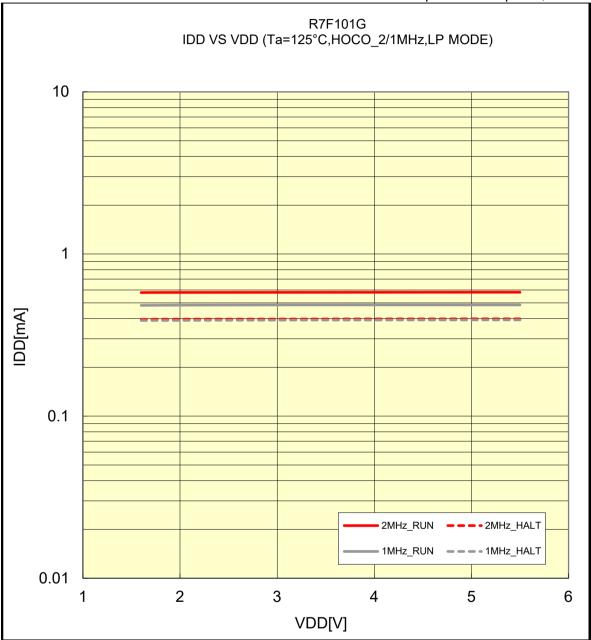


## IDD VS VDD(125°C/EXTERNAL CLOCK/LS MODE)



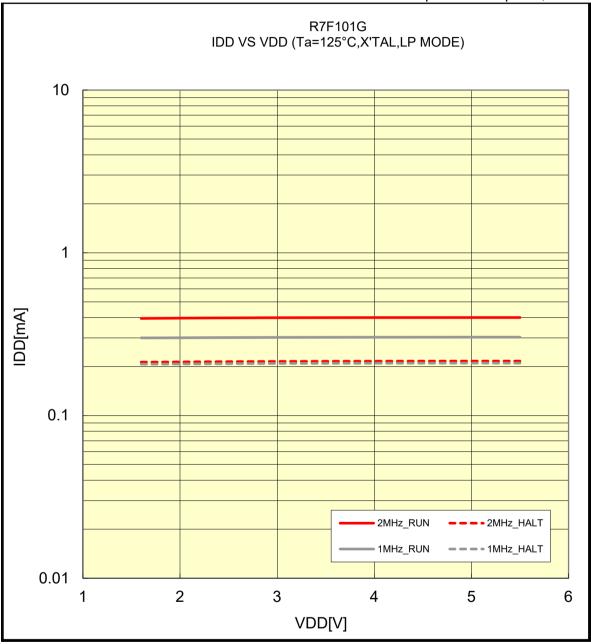
# IDD VS VDD(125°C/HOCO\_2/1MHz/LP MODE)





## IDD VS VDD(125°C/X'TAL/LP MODE)



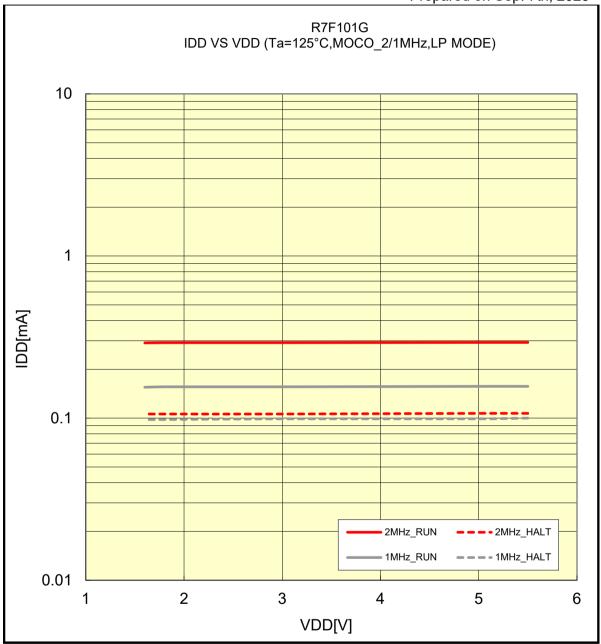


Remark 1MHz:4MHz/4 (MOSCDIV = 02H)

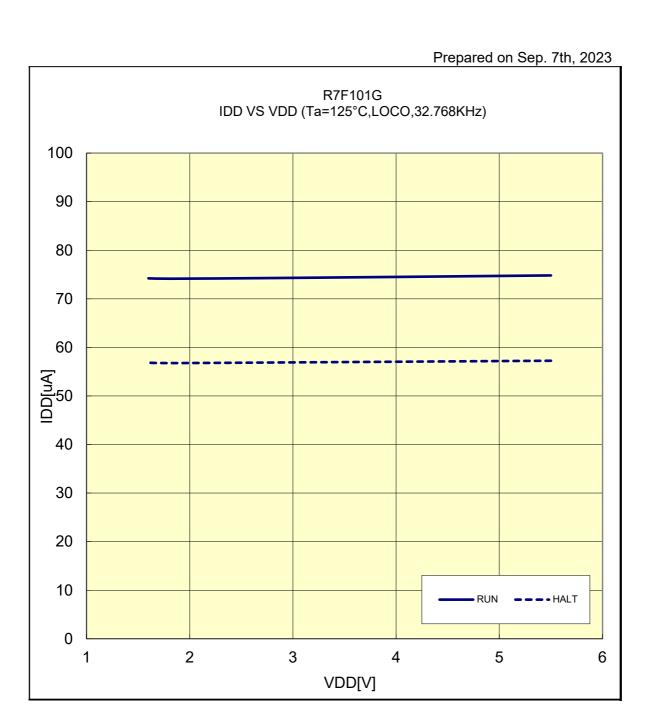
2MHz:4MHz/2 (MOSCDIV = 01H)

# IDD VS VDD(125°C/MOCO\_2/1MHz/LP MODE)

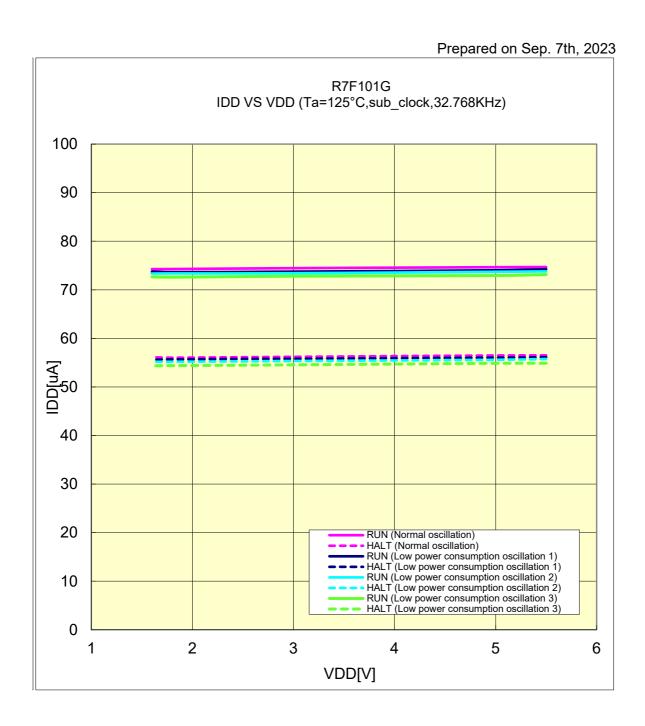




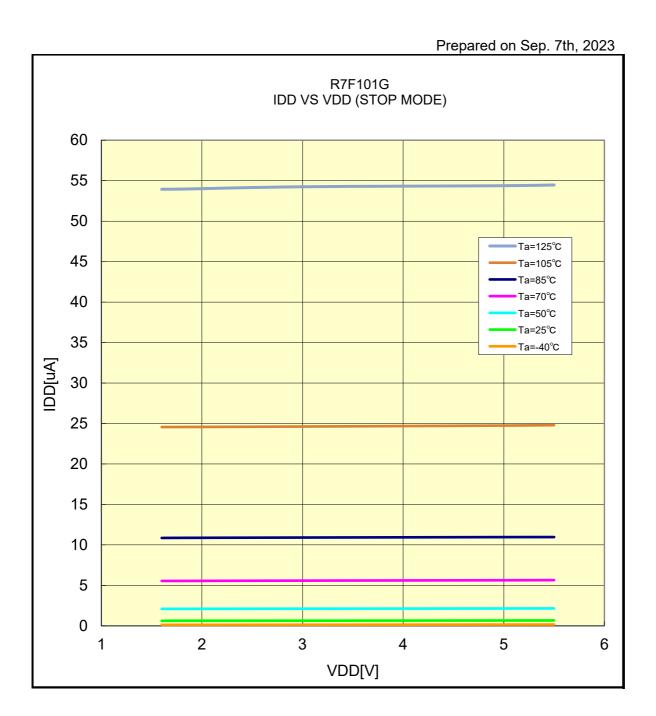
# IDD VS VDD(125°C/LOCO/32.768KHz)



# IDD VS VDD(125°C/sub\_clock/32.768KHz)



# IDD VS VDD(STOP MODE)



# IDD VS Ta(STOP MODE)

