

Product Change Notice (PCN)

Subject: Add New Substrate Supplier Daeduck for FCBGA-400 and FCBGA-784

Publication Date: 12/10/2021

Effective Date: 3/10/2022

Revision Description:

Initial Release

Description of Change:

Renesas is adding Daeduck, Korea as an alternate substrate supplier in addition to the current UMTC and Kinsus. Daeduck has decades of experience and expertise in Flip Chip BGA/CSP substrates and is ranked among the top 10 worldwide substrate suppliers in terms of revenue. Refer to appendix for the company profile.

There will be no changes to the substrate design, physical dimensions and electrical performance. Daeduck will be exactly the same as Kinsus and UMTC substrate in terms of form, fit and function. Daeduck uses mainstream HVM core and build-up materials for better 'future availability'. These have equivalent performance as the current materials used by Kinsus and UMTC substrate. Daeduck's ENEPIG surface finish provides the same protection against corrosion as the immersion Sn to ensure the same level of solder joint quality and reliability.

Refer to appendix for comparison between the current substrate suppliers versus the newly added substrate supplier.

Affected Product List: Refer Appendix B.

Reason for Change:

To alleviate supply shortages by ABF material and manufacturing capacity limitations.

Impact on Fit, Form, Function, Quality & Reliability:

The change will have no impact on the product form, fit, function, quality, reliability and environmental compliance of the products.

Product Identification:

Assembly Lot# traceable to the substrate material supplier

Qualification Status: Completed. Refer Appendix A

Sample Availability Date: 12/13/2021

Material Declaration: Available on request

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.

2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.
3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Appendix A – Comparison of Substrate Design and Materials

Features	FCBGA-400		FCBGA-784	
Supplier	Kinsus and UMTC	Daeduck	Kinsus and UMTC	Daeduck
Bump Pad Pitch (mm)	0.18	0.18	0.2	0.2
Bump Pad Opening (mm)	0.09	0.09	0.1	0.1
Bump Pad Metal Size (mm)	0.12	0.12	0.14	0.14
Trace Space (mm)	0.04	0.04	0.04	0.04
Trace Width (mm)	L1 (Bump): 0.020 L1 (Other) & L3: 0.025	L1 (Bump): 0.020 L1 (Other) & L3: 0.025	L1 (Bump): 0.020 L1 (Other) & L3: 0.025	L1 (Bump): 0.020 L1 (Other) & L3: 0.025
Ball Pad Opening (mm)	0.500±0.050	0.500±0.050	0.480±0.050 and 0.500±0.050	0.480±0.050
Ball Pad Metal Size (mm)	0.630±0.050	0.630±0.050	0.630±0.050	0.630±0.050
Core Thickness (mm)	0.8	0.8	0.8	0.8
Build-up	3/2/2003	3/2/2003	3/2/2003	3/2/2003
Hole Fill	Taiyo PHP-900 IR-6P	Taiyo PHP-900 IR-6P	Taiyo PHP-900 IR-6P	Taiyo PHP-900 IR-6P
Core Material	Hitachi E679FGR	Hitachi E700GR	Hitachi E679FGR	Hitachi E700GR
Build-up Material	ABF GX13	ABF GX92	ABF GX13	ABF GX92
Solder Mask	Taiyo PSR 4000 AUS703	Taiyo PSR 4000 AUS703	Taiyo PSR 4000 AUS703	Taiyo PSR 4000 AUS703
Surface Finish (Bump)	SAC305 ULA	SAC305 ULA	SAC305 ULA	SAC305 ULA
Surface Finish (Fiducials and External)	Immersion Sn (1 um min)	ENEPIG (Ni 6.6+/- 3.4um, Pd & Au 0.09 +/- 0.06um)	Immersion Sn (1 um min)	ENEPIG (Ni 6.6+/- 3.4um, Pd & Au 0.09 +/- 0.06um)

Appendix A – Comparison of Process Control

Substrate Process		QC Item	Process Control		
			Kinsus	UMTC	Daeduck
Core Layer	Mechanical Drill	Hole size	Yes	Yes	Yes
	Cu plating	Cu Thickness	Yes	Yes	Yes
	Lithography	Trace width	Yes	Yes	Yes
Build Up Layer	ABF lamination	ABF Thickness	Yes	Yes	Yes
	Laser drill	Via Diameter	Yes	Yes	Yes
	Cu plating	Cu Thickness	Yes	Yes	Yes
	Lithography	Trace Width	Yes	Yes	Yes
	Lithography	Trace Space	Yes	Yes	Yes
Solder Mask Layer	SM Lithography	SM Thickness-Top	Yes	Yes	Yes
	SM Lithography	SM Thickness-Bottom	Yes	Yes	Yes
	SM Lithography	SRO-Top	Yes	Yes	Yes
	SM Lithography	SRO-Bottom	Yes	Yes	Yes
Surface Finish	Immersion Tin	IT Thickness	Yes	Yes	Yes
	ENEPIG	Ni, Au, Pd Thickness	Yes	Yes	Yes
Backend	Pre-solder	Bump height	Yes	Yes	Yes
	Pre-solder	Bump diameter	Yes	Yes	Yes
	Pre-solder	Bump Coplanarity	Yes	Yes	Yes
	Routing	Body size X	Yes	Yes	Yes
	Routing	Body size Y	Yes	Yes	Yes
	FVI	Warpage	Yes	Yes	Yes

Appendix A - Qualification Results

Affected Packages: FCBGA-400 and FCBGA-784

Qual Vehicle: FCBGA-400 and FCBGA-784

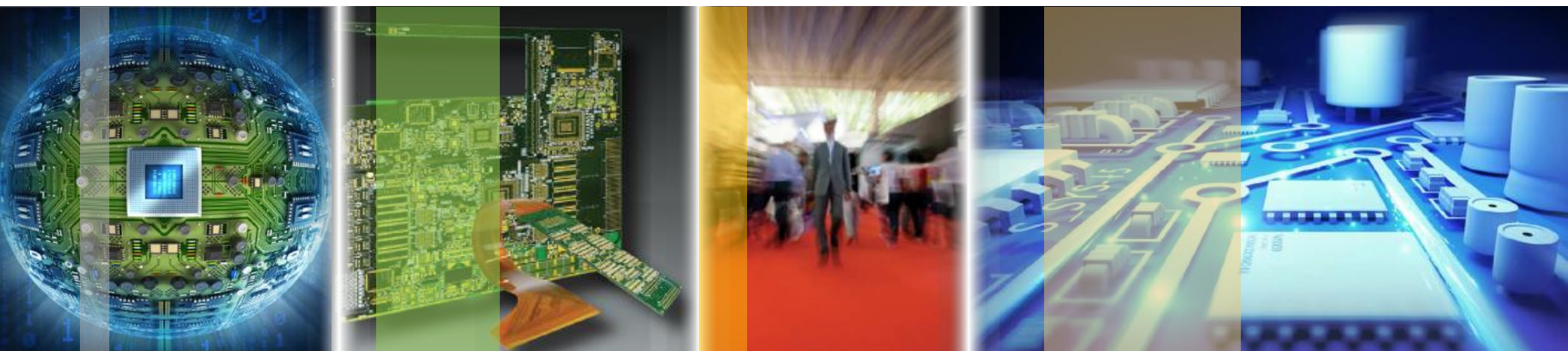
Qual Plan & Results: Tests are in accordance with JEDEC47 recommended tests.

Test Descriptions	Test Method	Test Results (Rej/SS)			
		Lot 1 FCBGA-784	Lot 2 FCBGA-784	Lot 3 FCBGA-400	Lot 4 FCBGA-400
* Temperature Cycling (-55°C to 125°C, 700 cycles)	JESD22-A104	0/25	0/25	0/25	0/25
* HAST - unbiased (130°C/85% RH, 96 Hrs)	JESD22-A118	-	-	0/25	0/25
* Temperature Humidity Bias (85°C/85% RH, 1000 Hrs)	JESD22-A101	0/25	0/25	-	-
High Temperature Storage Bake (150°C, 1000 Hrs)	JESD22-A103	0/25	0/25	0/25	0/25
Solder Ball Shear Test	JESD22-B117	0/5	0/5	0/5	0/5
Physical Dimensions	JESD22-B100	0/30	0/30	0/30	0/30
Moisture Sensitivity Level, MSL	J-STD-20 / MSL 4, 245°C	0/25	0/25	0/25	0/25

**Tests were subjected to Preconditioning per JESD22-A113 prior to stress test*

Appendix B – Affected Product List

80HCPS1616CHLG	80HCPS1848CBLGI8	80HCPS1616CHLG8	80HCPS1616CHMGI8
80HCPS1848C-LBLGI	80HSPS1616CHMG	80HCPS1616CHLGI	80HCPS1848C-5BLG
80HCPS1848C-LBLGI8	80HSPS1616CHMG8	80HCPS1616CHLGI8	80HCPS1848C-5BLG8
80HCPS1848CBLG	80HSPS1616CHMGI	80HCPS1616CHMG	80HSPS1616CHMGI8
80HCPS1848CBLG8	80HCPS1848C-5BLGI8	80HCPS1616CHMG8	
80HCPS1848CBLGI	80HCPS1848C-5BLGI	80HCPS1616CHMGI	



DDE Company Introduction

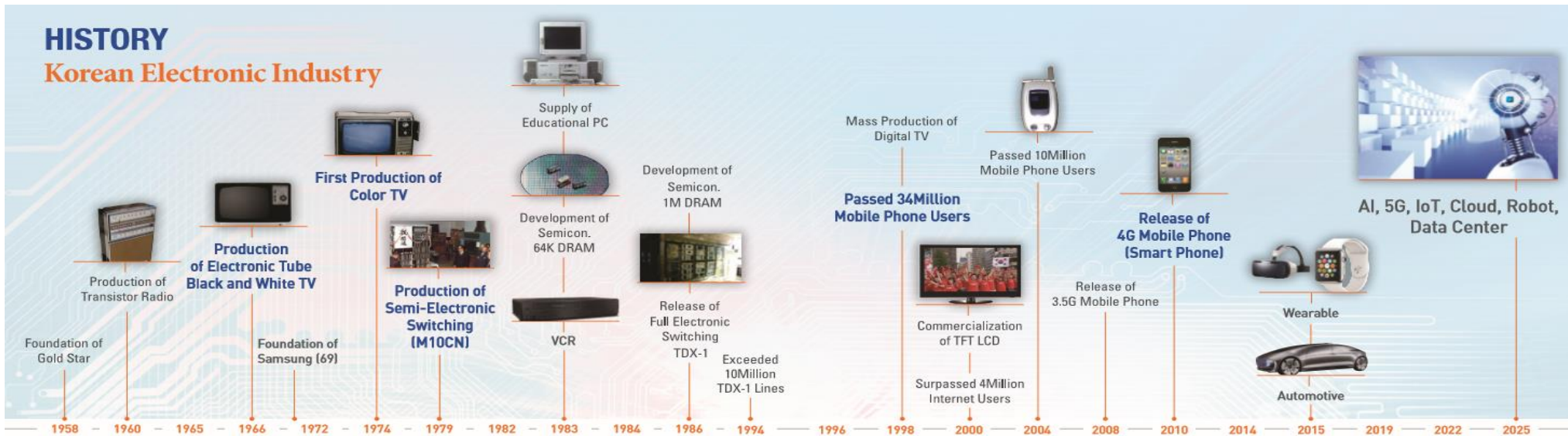
Jan. 26, 2021

Daeduck Electronics Co., Ltd.

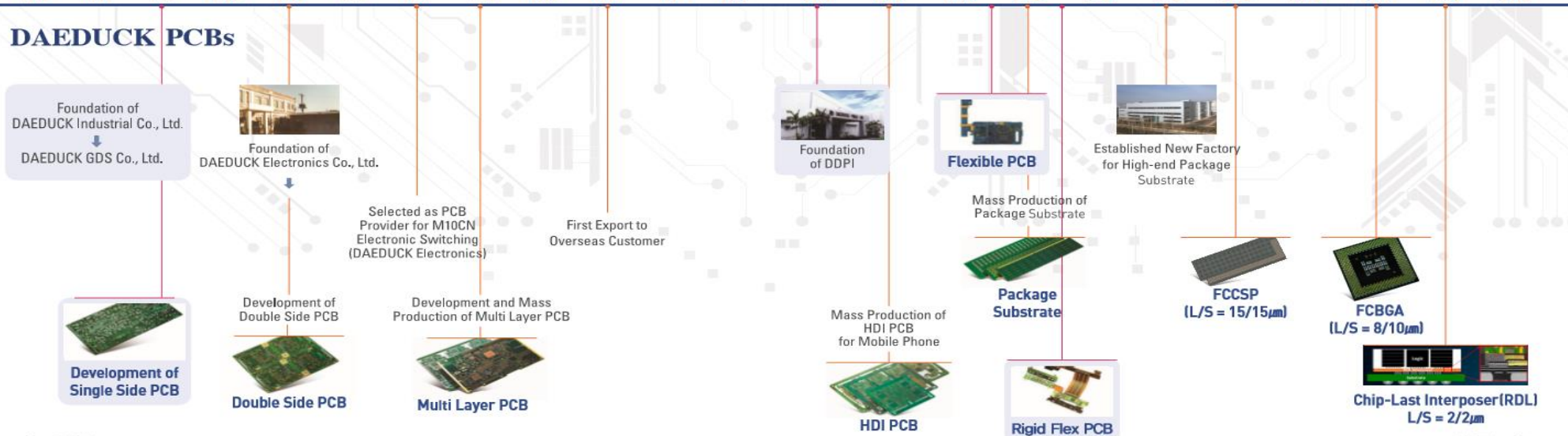
DAEDUCK History

HISTORY

Korean Electronic Industry



DAEDUCK PCBs



Business Unit (BU)

DAEDUCK Electronics

PKG Div.



Mobile Div.



MLB Div.



Portfolio & Product	<u>Semiconductor</u> utCSP, fcCSP, fcBGA, SiP	<u>Mobile</u> Flexible & Rigid Flex HDI / mSAP	<u>Network/Automotive</u> High Multi Layer PCB Complex HDI
Capacity	53,000 sqm/month ** Ave. Layer #: 4L ** Max. Layer #: 16L ** mSAP: 45,000 sqm	30,000 sqm/month ** Ave. Layer #: 4L(R/F), 10L(HDI) ** Max. Layer #: 10L(R/F), 14L(HDI) ** mSAP: 10,000 sqm	15,000 sqm/month ** Ave. Layer #: 20L ** Max. Layer #: 116L
Locations	[Factory] Korea ** Local Office: USA, Canada, Taiwan, China, Singapore	Korea / Vietnam	Korea / Philippine

Global Manufacturing Strategy



❖ Global Presence

- DDE Korea: PKG (900), Mobile (900), MLB (400)
- DDV: Hanoi, Vietnam (400)
- DDPI: Cavite, Philippines (700)

(): # of employees

DDE - Korea

[HQ/Mobile BU-Ansan, Korea]



[Package BU-Ansan, Korea]



[MLB BU-Ansan, Korea]

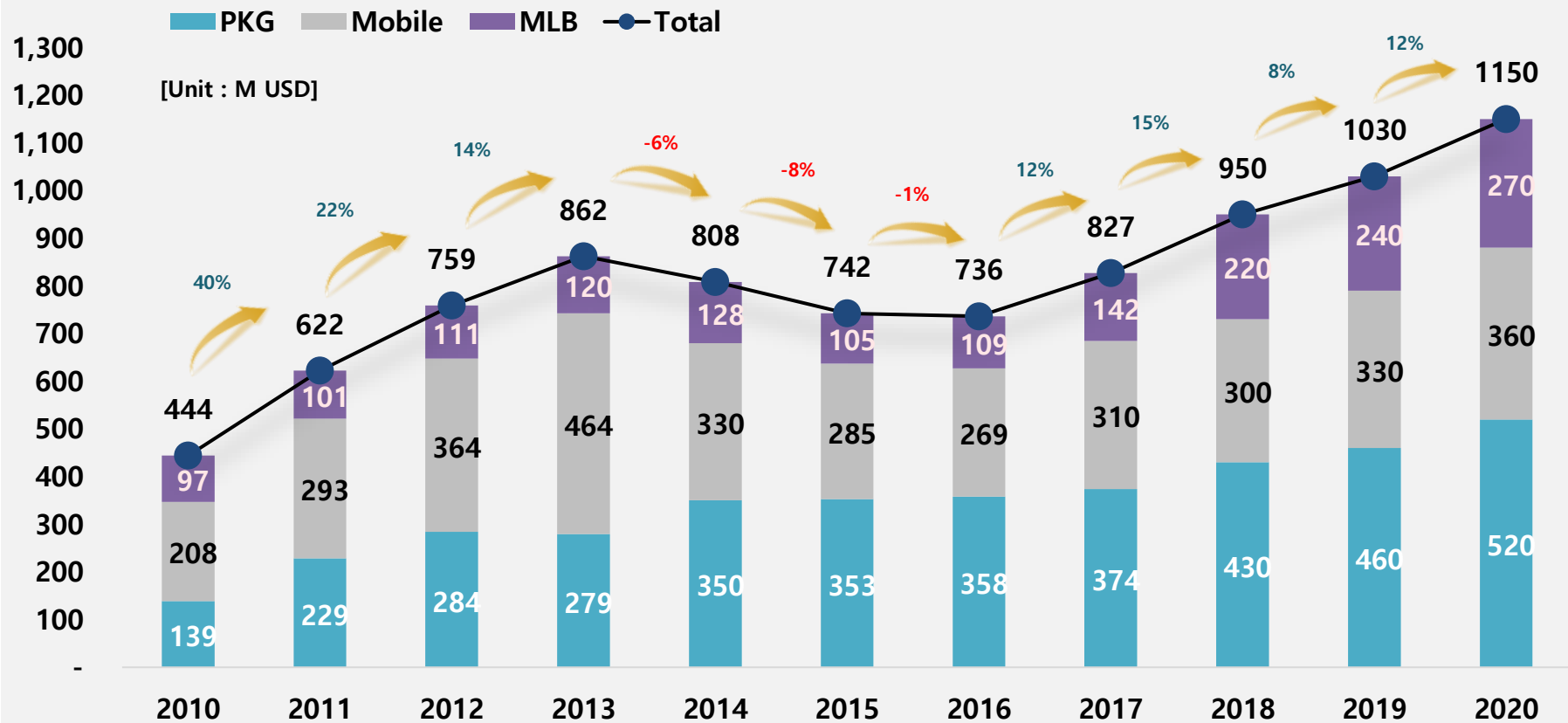


Company Growth

◆ Worldwide Rank #8 in Substrate Supplier Revenue (Prismark Q2, 2020)

◆ Achieved over \$1B sales in 2019 and projecting continuous growth in 2020

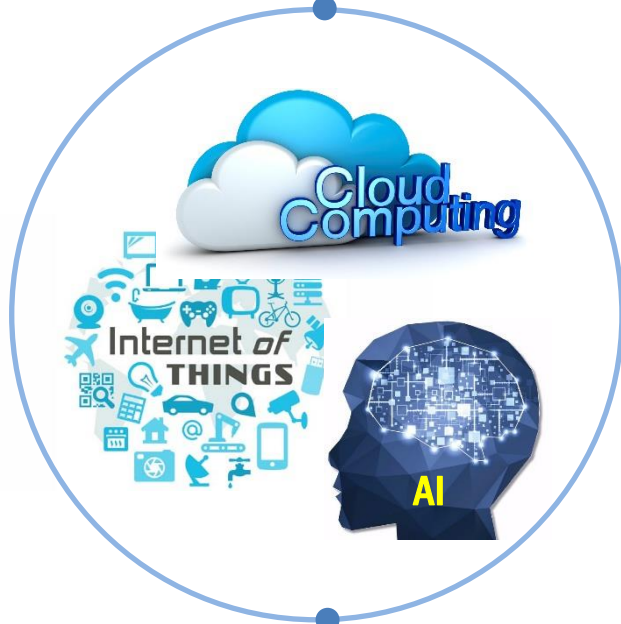
- Package BU: Portfolio diversification into 5G modules and focus on FCCSP (strip/unit. ABF/PPG)
- Mobile BU: Continue driving Rigid Flex applications and 5G module development
- MLB BU: Expanding on high layer, high density products in networking and automotive products



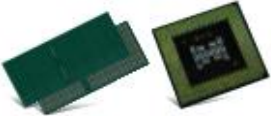
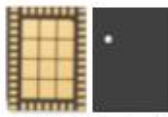
Product Portfolio – PKG BU

SEMICONDUCTOR

Memory



Non Memory

 DRAM	 Flip Chip/POP	• Mobile DRAM (POP) Thin Sub. 3Layer : 80μm • Controlled-Warpage Material for Low CTE/Tg
 Flash Memory	 Ultra Thin CSP/xMCP	• Ultra Thin Substrate 2L 70μm, 3L 80μm, 4L 120μm • Flatness & Stiffness
 Data Center / Automotive	 FCBGA	• Stack-Up 6~16L • Line/Space 8/10μm • ABF Available
 Application Processor	 FCCSP	• Stack-Up 2~4L, ETS Type • Line/Space 8/10μm • SAP Available
 RF Module / 5G	 SiP/Cavity	• Thermal Enhanced Via • High Layer Coreless 5~11L • Layer to Layer Align <15μm

❖ **To provide world class manufacturing & quality support in meeting customer prerequisites**

-  DAEDUCK

DAEDUCK organization chart

