I^2C 2-Wire Bus Buffer With Hot Swap Capability and Rise Time Accelerators

The ISL33001-ISL3003 I^2C Bus Buffer provides the necessary buffering for extending the bus capacitance beyond the 400pF max specified by the I^2C specification. In addition, the ISL33001-ISL33003 features rise time accelerator circuitry to reduce power consumption from passive bus pull-up resistors, hot swappable circuitry to prevent transmission corruption of the data and clock lines when I^2C devices are plugged into a live backplane and level translation for mixed logic level applications.

The ISL33001-ISL33003 operates at supply voltages from +2.3V to +5.5V. The ISL33001-ISL33003 is offered in an 8Ld MSOP or 8Ld 3x3mm TDFN packages.

TABLE 1. SUMMARY OF FEATURES

Part Number	Level Translation	Enable Pin	Ready Pin	Accelerator Disable
ISL33001	NO	YES	YES	NO
ISL33002	YES	NO	NO	YES
ISL33003	YES	YES	NO	NO

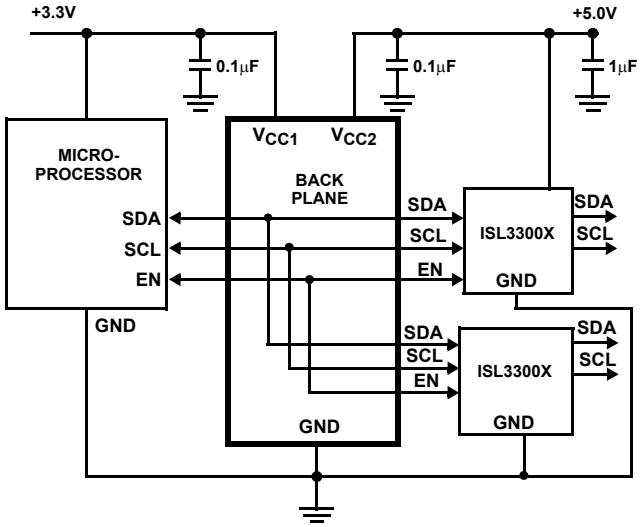
Features

- 2 Channel Bi-directional Buffer
- 400kHz Operation
- Rise Time Accelerators
- Hot-Swapping Capability
- Enable Pin with Low Current Shutdown (ISL33001 and ISL33003)
- Logic Level Translation (ISL33002 and ISL33003)
- READY Logic Pin (ISL33001)
- Accelerator Disable Pin (ISL33002)
- +2.3VDC to +5.5VDC Supply Range
- Pb-Free (RoHS Compliant) 8Ld TDFN (3x3 mm) and 8Ld MSOP packages.

Applications

- I^2C Bus Extender and Capacitance Buffer
- Server racks for telecom, datacom, and computer servers
- Desktop Computers
- Hot-Swap Board Insertion and Bus Isolation

Typical Operating Circuit



Ordering Information

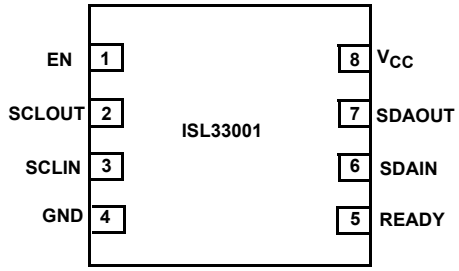
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL33001EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3A
ISL33001EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3H
ISL33001IEIUZ-T		-40 to +85	8 Ld MSOP	M8.118
ISL33002EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3A
ISL33002EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3H
ISL33002IEIUZ-T		-40 to +85	8 Ld MSOP	M8.118
ISL33003EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3A
ISL33003EIRZ-T		-40 to +85	8 Ld TDFN	L8.3X3H
ISL33003IEIUZ-T		-40 to +85	8 Ld MSOP	M8.118

NOTES:

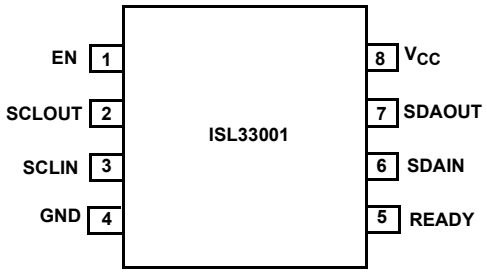
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Please refer to TB347 for details on reel specifications.

Pinouts

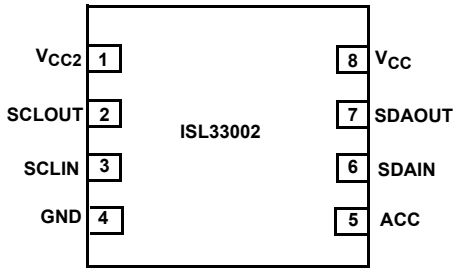
ISL33001
(8 Ld TDFN)
TOP VIEW



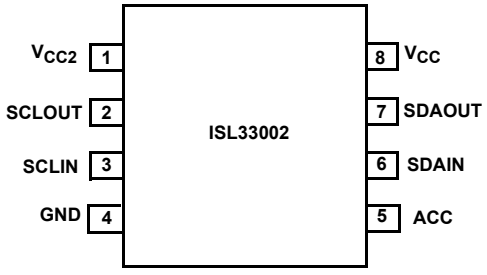
ISL33001
(8 Ld MSOP)
TOP VIEW



ISL33002
(8 Ld TDFN)
TOP VIEW

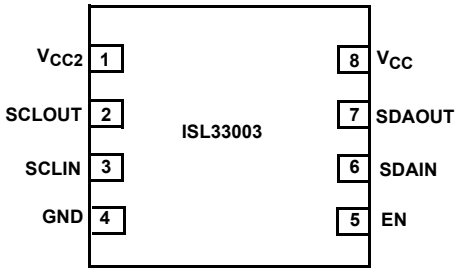


ISL33002
(8 Ld MSOP)
TOP VIEW

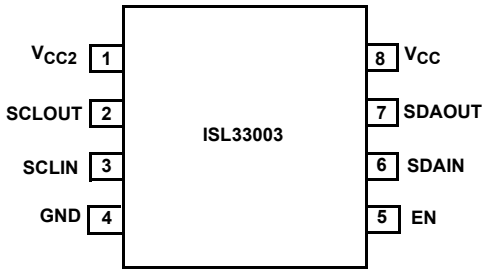


Pinouts

ISL33003
(8 Ld TDFN)
TOP VIEW



ISL33003
(8 Ld MSOP)
TOP VIEW



Pin Descriptions

(See Applications Notes for full pin descriptions)

NAME	NOTES	PIN NUMBER	FUNCTION
V_{CC}		8	V_{CC} power supply, +2.3V to +5.5V. Decouple V_{CC} to ground with a 0.01uF capacitor or larger.
V_{CC2}	ISL33002 and ISL33003 only	1	V_{CC2} power supply, +2.3V to +5.5V. Decouple V_{CC2} to ground with a 0.01uF capacitor or larger. In level shifting applications, SDA_OUT and SCL_OUT are referenced to V_{CC2} .
GND		4	Device Ground Pin
EN	ISL33001 and ISL33003 only	1 (ISL33001), 5 (ISL33002)	Buffer Enable Pin. Logic “0” puts the device in shutdown. Logic “1” enables the device.
READY	ISL33001 only	5	Ready Digital Logic Output
ACC	ISL33002 only	5	Rise Time Accelerator Enable Pin
SDAIN, SDAOUT		6 (SDA_IN), 7 (SDA_OUT)	Data I/O Pins
SCLIN, SCLOUT		3 (SCL_IN), 2 (SCL_OUT)	Clock I/O Pins

Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{CC}, V_{CC2} . . . . . -0.3V to +7V
SDA_IN, SDA_OUT . . . . . -0.3V to +(V_{CC} + 0.3)V
SCL_IN, SCL_OUT . . . . . -0.3V to +(V_{CC} + 0.3)V
ENABLE, READY, ACC . . . . . -0.3V to +(V_{CC} + 0.3)V
Maximum Sink Current (SDA and SCL Pins) . . . . . TBD
Continuous Power Dissipation (T_A = +70°C)
8 Ld TDFN (derate 25.0mW/°C) . . . . . TBDmW
8 Ld MSOP (derate 25.0mW/°C) . . . . . TBDmW

Thermal Information

Thermal Resistance
8Ld TDFN Package (Note 3) . . . . . TBD
8Ld MSOP Package (Note 4) . . . . . TBD
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +150°C
Lead Temperature (soldering, 10s) . . . . . +300°C
Pb-free reflow profile . . . . . .see link below
http://www.intersi.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range, T_A . . . . . -40°C to 85°C
V_{CC} Supply Voltage Range . . . . . +2.3V to +5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. theta JA is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB7379 for details.
4. theta JA is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications

V_{EN} = V_{CC}, T_A = -40°C to +85°C; Typical values are at V_{CC} = +3.3V, V_{CC2} = +3.3V unless otherwise noted. (Notes 5)

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
POWER SUPPLIES							
V_{CC} Supply Range	V_{CC}		Full	2.1		5.5	V
V_{CC2} Supply Range	V_{CC2}	ISL33002 and ISL33003 only	Full	2.1		5.5	V
Supply Current from V_{CC}	I_{CC}	V_{CC} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V, ISL33001 only (Note 9)	Full		2.3	4.3	mA
		V_{CC} = V_{CC2} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V, ISL33002 and ISL33003 (Note 9)	Full		1.8	3.2	mA
Supply Current from V_{CC2}	I_{CC2}	V_{CC2} = V_{CC} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V; ISL33002 and ISL33003 (Note 9)	Full		0.5	0.8	mA
V_{CC} Shut-down Supply Current	I_{SHDN}	V_{CC} = 5.5V, V_{EN} = GND; ISL33001 only	Full		0.025		µA
		V_{CC} = V_{CC2} = 5.5V, V_{EN} = GND; ISL33002 and ISL33003 only	Full		0.025		µA
V_{CC2} Shut-down Supply Current	I_{SHDN2}	V_{CC} = V_{CC2} = 5.5V, V_{EN} = GND, ISL33002 and ISL33003 only	Full		TBD		µA
START UP CIRCUITRY							
Precharge Circuitry Voltage	V_{PRE}	SDA and SCL pins floating	Full	0.8	1	1.2	V
Enable Threshold Voltage	V_{EN}	ISL33001 and ISL33003; Rising Edge	25	1	1.4	2	V
Enable Pin Input Current	I_{EN}	Enable from 0V to V_{CC}; ISL33001 and ISL33003	Full	-1	0.1	1	µA
Enable Delay, On-Off	t_{EN-HL}	ISL33001 and ISL33003 (Note 7)	25		10		ns
Enable Delay, Off-On	t_{EN-LH}	ISL33001 and ISL33003 (Note 7)	25		95		µs
Bus Idle Time	t_{IDLE}	See Figure 2	Full	50	95	150	µs
Ready Pin OFF State Leakage Current	I_{OFF}	ISL33001 only	25	-1	0.1	1	µA
Ready Delay, On-Off	$t_{READY-HL}$	ISL33001 only (Note 7)	25		10		ns

Electrical Specifications $V_{EN} = V_{CC}$, T_A = -40°C to +85°C; Typical values are at V_{CC} = +3.3V, V_{CC2} = +3.3V unless otherwise noted. (Notes 5) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Ready Delay, Off-On	$t_{READY-LH}$	ISL33001 only (Note 7)	25		10		ns
Ready Output Low Voltage	V_{OL_READY}	V_{CC} = +2.5V, I_{PULLUP} = 3mA; ISL33001only	Full			0.4	V
RISE-TIME ACCELERATORS							
Transient Accelerator Current	I_{TRAN_ACC}	V_{CC} = 2.7V, Positive Transition on SDA and SCL pins; V_{CC2} = 2.7V, ACC = 0.7*V_{CC2} , ISL33002 only (Note 7)	25		8.5	-	mA
Accelerator Enable Threshold	V_{ACC_EN}	ISL33002 only	25	-	0.5*V_{CC}	0.7*V_{CC}	V
Accelerator Disable Threshold	V_{ACC_DIS}	ISL33002 only	25	0.3*V_{CC}	0.5*V_{CC}	-	V
Accelerator Pin Input Current	I_{ACC}	ISL33002 only	25	-1	0.1	1	µA
Accelerator Delay, On-Off	t_{PDOFF}	ISL33002 only (Note 7)	25		10		ns
ESD PROTECTION							
SDA,SCL I/O Pins	HBM_ESD	Human Body Model, C_{VCCx} =1.0µF	25		TBD		kV
		IEC 61000-4-2 Air-Gap Discharge, C_{VCCx} = 1.0µF	25		TBD		kV
		IEC 61000-4-2 Contact Discharge, C_{VCCx} = 1.0µF	25		TBD		kV
Input-Output Connections							
Input-Output Offset Voltage	V_{OS}	V_{CC} = 3.3V, 10kΩ to V_{CC} on SDA and SCL pins, V_{INPUT} = 0.2V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 3)	Full	0	100	1750	mV
Output Low Voltage	V_{OL}	V_{CC} = 2.7V, V_{INPUT} = 0V, I_{SINK} = 3mA on SDA/SCL pins; V_{CC2} = 2.7V, ISL33002 and ISL33003 (Figure 4)	Full			0.4	V
Buffer SDA and SCL pins Input Capacitance	C_{IN}	(Note 7)	25			10	pF
Input Leakage Current	I_{LEAK}	SDA and SCL pins = V_{CC} = 5.5V; V_{CC2} = 5.5V, ISL33002 and ISL33003	Full	-5	0.1	5	µA
Timing Characteristics							
SCL/SDA Propagation Delay High to Low	t_{PHL}	C_{LOAD} = 50pF, 2.7kΩ to V_{CCx} on SDA and SCL pins, V_{CC} = 3.3V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 5)	25		65		ns
SCL/SDA Propagation Delay Low to High	t_{PLH}	C_{LOAD} = 50pF, 2.7kΩ to V_{CCx} on SDA and SCL pins, V_{CC} = 3.3V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 5)	25		10		ns
SCL/SDA Transition Time Low to High	t_{RISE}	V_{CC} = 2.3V, C_{LOAD} = 15pF on SDA_IN and SCL_IN pins, C_{LOAD} = 15pF on SDA_OUT and SCL_OUT pins, 3.3kΩ to V_{CCx} on SDA and SCL pins; V_{CC2} = 2.3V, ISL33002 and ISL33003, (Note 8, Figure 6)	25	20+ 0.1*C_B	-	300	ns
		C_{LOAD} = 100pF, 10kΩ to V_{CCx} on SDA and SCL pins; V_{CC} = 3.3V, V_{CC2} = 3.3V, ISL33002 and ISL33003, (Note 8, Figure 6)	25	-	30	300	ns

Electrical Specifications $V_{EN} = V_{CC}$, T_A = -40°C to +85°C; Typical values are at V_{CC} = +3.3V, V_{CC2} = +3.3V unless otherwise noted. (Notes 5) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SCL/SDA Transition Time High to Low	t_{FALL}	V_{CC} = 2.3V, C_{LOAD} = 15pF on SDA_IN and SCL_IN pins, C_{LOAD} = 15pF on SDA_OUT and SCL_OUT pins, 3.3kΩ to V_{CCx} on SDA and SCL pins; V_{CC2} = 2.3V, ISL33002 and ISL33003, (Note 8, Figure 6)	25	20+ 0.1*C_B		300	ns
		C_{LOAD} = 100pF, 10kΩ to V_{CCx} on SDA and SCL pins; V_{CC} = 3.3V, V_{CC2} = 3.3V, ISL33002 and ISL33003, (Note 8, Figure 6)	25		30	300	ns

NOTES:

5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
6. Parts are 100% tested at +25°C. Over temperature limits are established by characterization and are not production tested.
7. Guaranteed by design. Not subject to test.
8. C_B = total capacitance of the associated bus in pF.
9. Buffer is in the connected state.

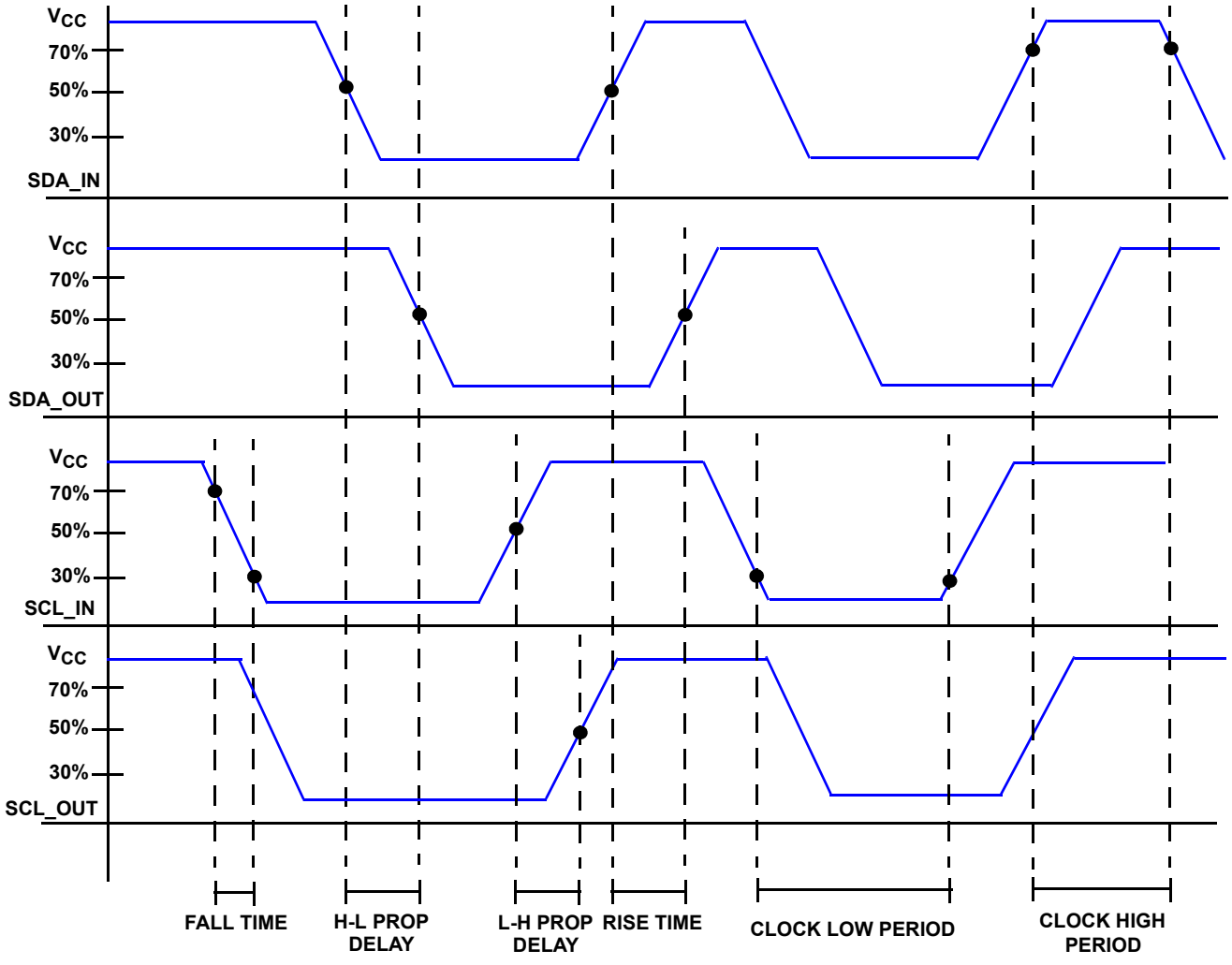


FIGURE 1. I2C BUFFER TIMING DIAGRAM

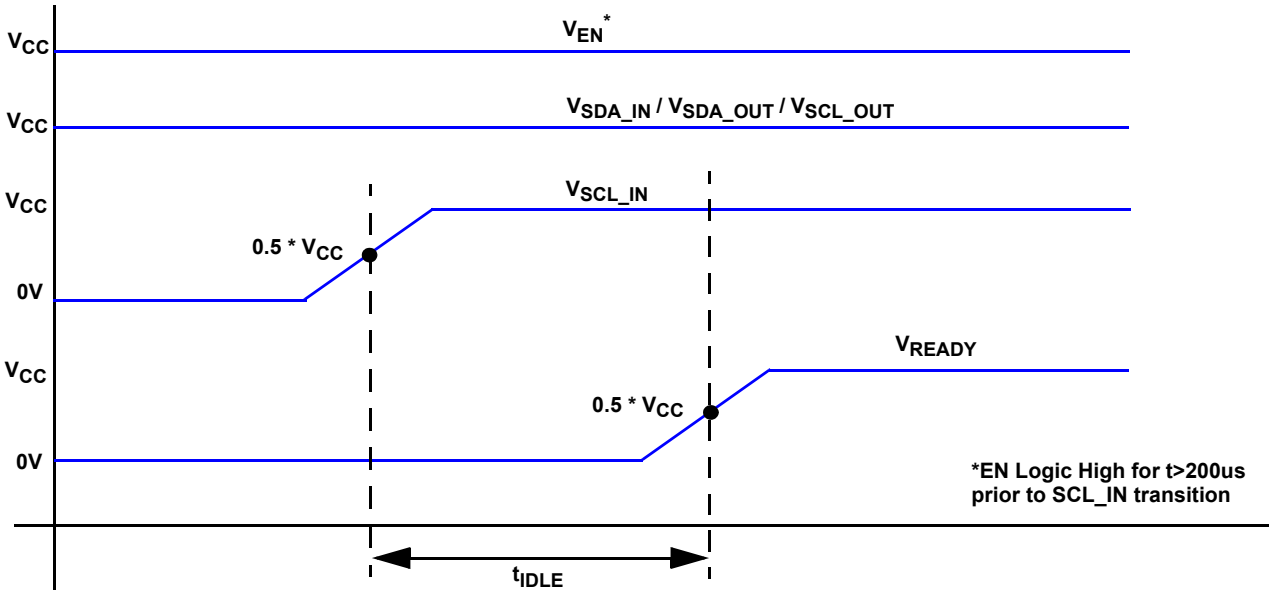


FIGURE 2. BUS IDLE TIME (ISL33001 only)

Test Circuits and Waveforms

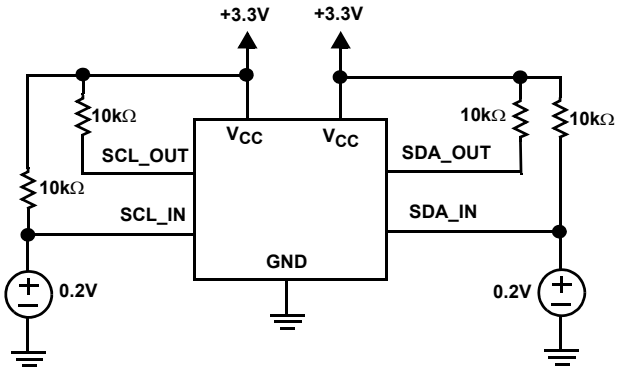


FIGURE 3A. TEST CIRCUIT

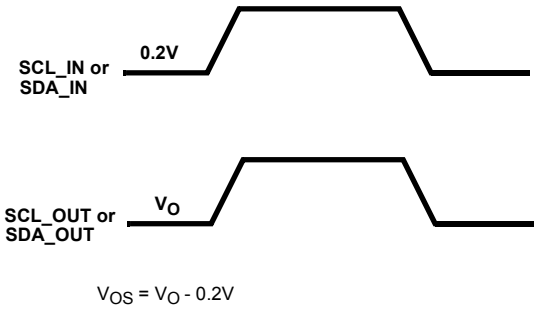


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. INPUT TO OUTPUT OFFSET VOLTAGE

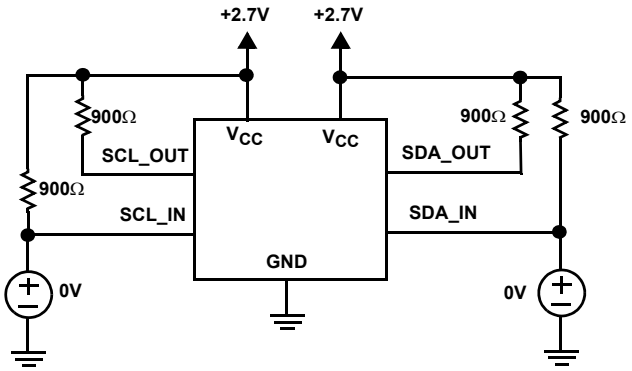


FIGURE 4A. TEST CIRCUIT

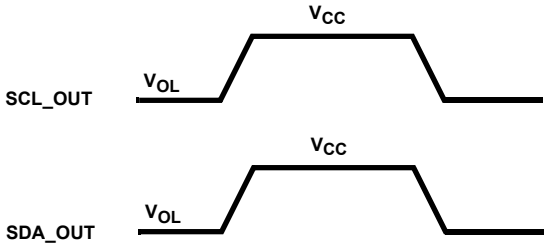


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. OUTPUT LOW VOLTAGE

Test Circuits and Waveforms (Continued)

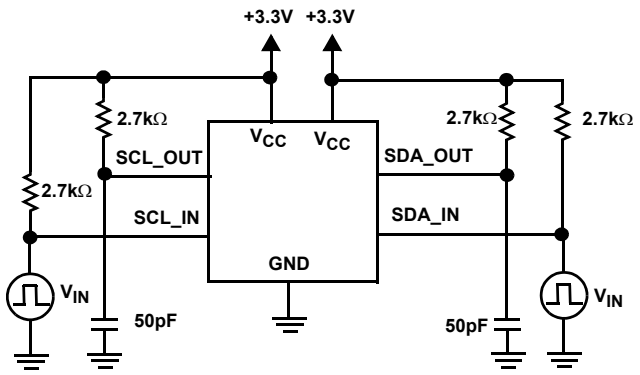
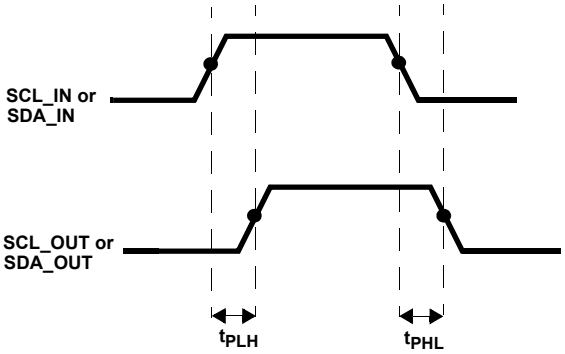


FIGURE 5A. TEST CIRCUIT



*Propagation delay measured at 50% of V_{CC} points

FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. PROPAGATION DELAY

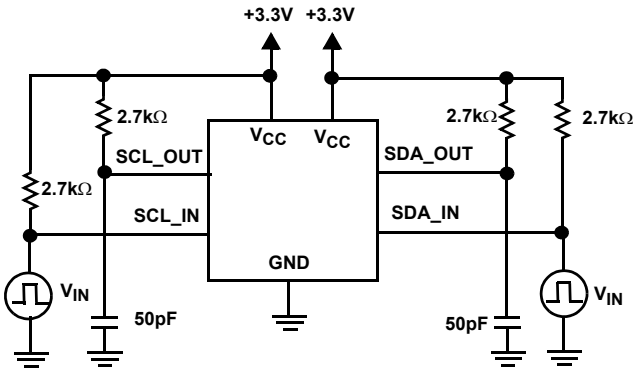
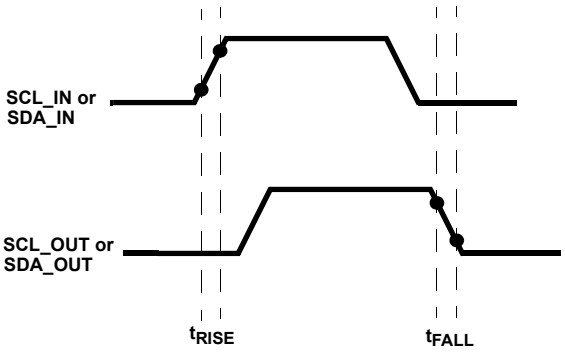


FIGURE 6A. TEST CIRCUIT



*Rise/fall times measured at 30% of V_{CC} to 70% of V_{CC} points

FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RISE/FALL TIME

Application Information

The ISL33001-ISL33003 IC's are 2 Wire Bi-directional Bus Buffers designed to drive heavy capacitve loads in open drain systems. The ISL33001-ISL33003 incorporate rise time accelerator circuitry that improves the rise time for open drain systems that use a passive pull up resistor in bus systems. These devices also feature hot swapping capability for applications that require hot insertion of boards into a host system (rack servers and ATCA applications). The ISL33001 features a logic output flag (READY) that signals the status of the buffer and an ENABLE pin to enable or disable the buffer. The ISL3302 features level shifting capability on the I/O pins and a logic input to disable the rise time accelerator circuitry. The ISL33003 features an ENABLE pin and the level shifting functionality.

I2C and SMBUS Compatiblity

The ISL33001-ISL33003 IC's are I2C and SMBUS compatible devices. designed to work in an I2C open drain bus environment. The IC's supports both clock stretching and bus arbitration on the SDA and SCL pins. They are designed to operate between from DC to more than 400kHz, supporting Fast Mode data rates of the I2C specification.

Startup And Hot Swap Circuitry

The ISL33001-ISL33003 buffers contain under voltage lock out (UVLO) circuitry that prevents operation of the buffer until the IC recieves the proper voltage. For VCC, this voltage is TBD and for VCC2 the voltage is TBD. Signals at the SDA/SCL pins are ignored until the device reaches the proper supply voltage. This prevents any communication errors on the bus until the device is properly powered up.

At the same time during the UVLO, the SDA and SCL pins are pre-charged to 1V for hot insertion actions. Because the bus at any time can be between 0V and VCC, precharging the I/O pins to 1V minimizes system disturbance when the IC is hot plugged into a live back plane that may have the bus communicating with other devices.

Once the IC comes out of the UVLO state, the buffer will remain disconnected until it recieves a valid connection state. A valid connection state is either a BUS IDLE condition or a STOP BIT condition.

Connection Circuitry

Once a valid connection condition is met, the buffer is connected and the state of the SDA/SCL pins will be determined by external drivers. A low voltage forced on either SDA_IN or SDA_OUT will keep both pins LOW. Both pins remain in a LOW state until all external drivers are released, which will allow the pull up resistors to pull the SDA line HIGH. The SCL_IN and SCL_OUT pins function in the same way as the SDA_IN and SDA_OUT pins. These features allow clock strectching, where a slave device may hold a CLK line LOW to stall the master clock, and bus arbitration, which allows communication of multi master systems. The directionality of the IN/OUT pins are not exclusive (bidirectional pins) and functionally behave indentical to each other.

Typical Performance Curves C_L = pF, T_A = +25°C; Unless Otherwise Specified.

FIGURE 7. I_{CC1} QUIESCENT CURRENT vs TEMPERATURE ENABLED

FIGURE 8. I_{CC1} QUIESCENT CURRENT vs TEMPERATURE DISABLED

FIGURE 9. I_{CC2} QUIESCENT CURRENT vs TEMPERATURE ENABLED

FIGURE 10. I_{CC2} QUIESCENT CURRENT vs TEMPERATURE DISABLED

Typical Performance Curves C_L = pF, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

FIGURE 11. OUTPUT LOW vs TEMPERATURE

FIGURE 12. INPUT TO OUTPUT OFFSET vs TEMPERATURE

FIGURE 13. OFFSET VOLTAGE vs PULL UP RESISTANCE vs TEMPERATURE

FIGURE 14. INPUT TO OUTPUT HIGH TO LOW PROPAGATION DELAY vs TEMPERATURE

FIGURE 15. INPUT TO OUTPUT HIGH TO LOW PROPAGATION DELAY vs CAPACITANCE

FIGURE 16. OUTPUT RISE TIME vs CAPACITANCE

Typical Performance Curves C_L = pF, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

FIGURE 17.

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

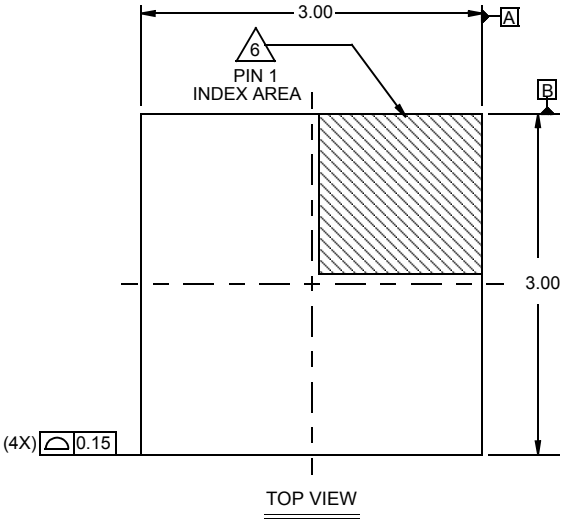
GND

TRANSISTOR COUNT:

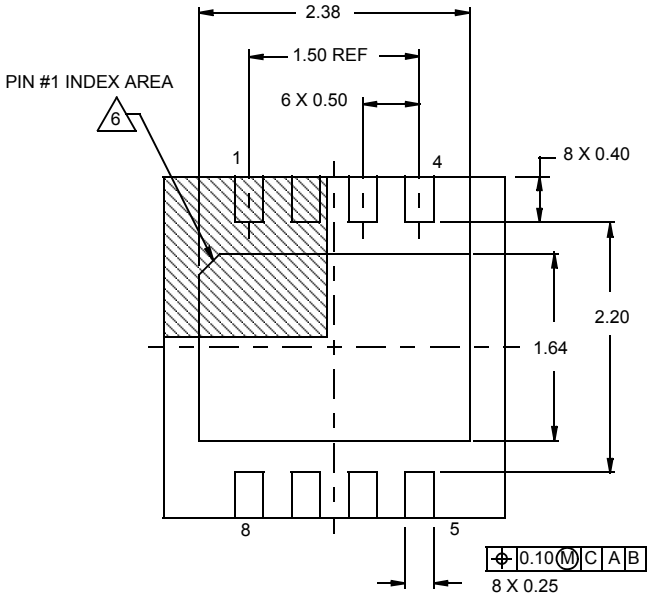
xxx

PROCESS:

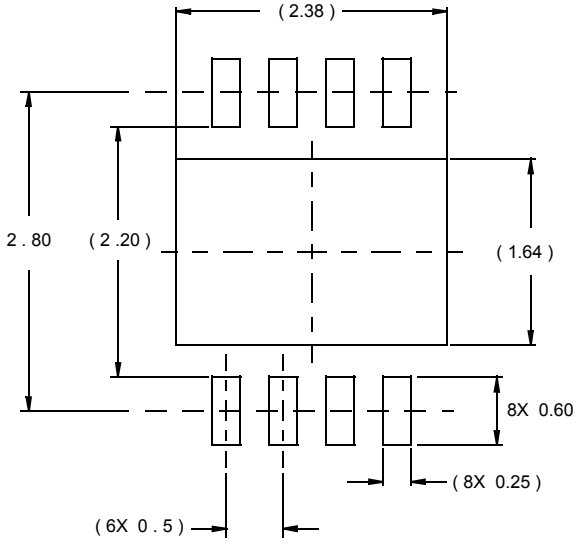
Package Outline Drawing
L8.3x3H
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN)
Rev 0, 2/08



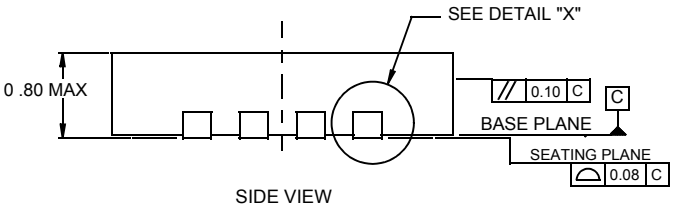
TOP VIEW



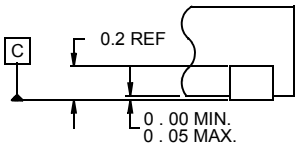
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

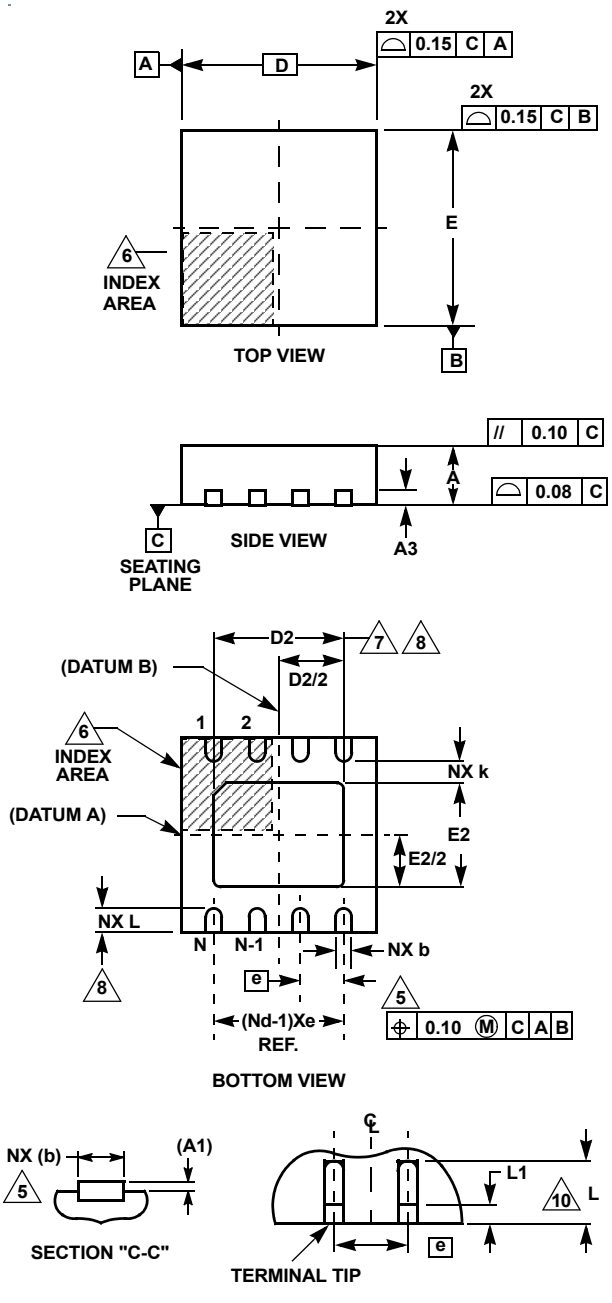


DETAIL “X”

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

hin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

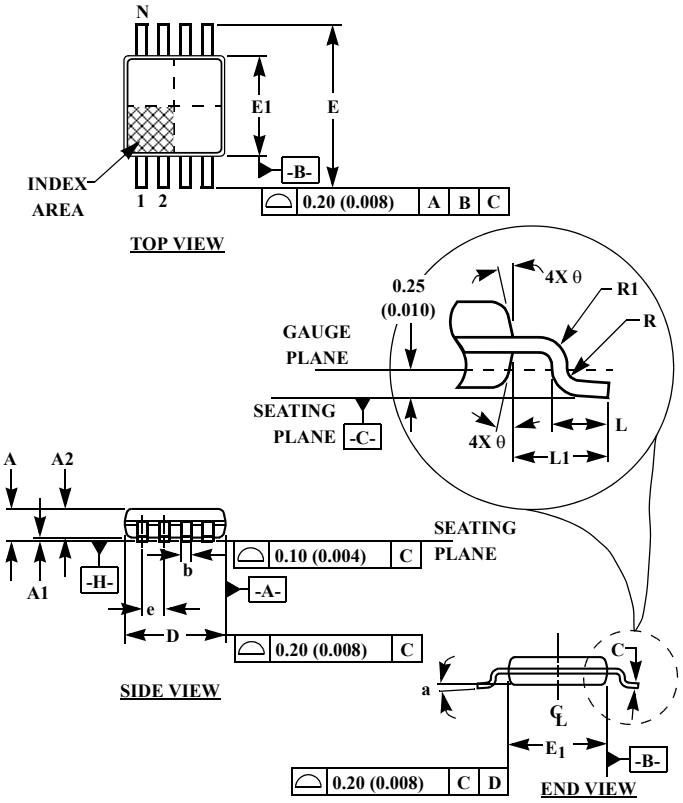
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3		0.20 REF		-
b	0.25	0.30	0.35	5, 8
D		3.00 BSC		-
D2	2.20	2.30	2.40	7, 8, 9
E		3.00 BSC		-
E2	1.40	1.50	1.60	7, 8, 9
e		0.65 BSC		-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N		8		2
Nd		4		3

Rev. 3 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the “L” min dimension.

Mini Small Outline Plastic Packages (MSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. - H - Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums -A - and - B - to be determined at Datum plane - H -.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03