1.5A, Rad Hard, Positive, High Voltage LDO

ISL75052SRH

The ISL75052SRH is a radiation hardened, single output LDO specified for an output current of upto 1.5A. The device operates from an input voltage range of 4.0V to 13.2V and provides for output voltages of 0.6V to 12.7V. The output is adjustable based on a resistor divider setting. Dropout voltages as low as 200mV worst case can be realized using the device

The ENABLE feature allows the part to be placed into a low shutdown current mode of 10µA typ. When enabled the device operates witha low ground current of 11mA typ which provides for operation with Low Quiescent Power consumption.

The device has good transient response and designed keeping Single Event Effects in mind. This results in reduction of the magnitude of SET seen on the output. There is no need for additonal protection diodes and filters.

COMP pin is provided to enable the use of external compensation. This is acheived by connecting a resistor and capacitor from COMP to ground.

The device is stable with Tantalum capacitors as low as 47uF and provides excellent regulation all the way from no Load to full Load. The programmable soft start allows one to program the inrush current by means of the decoupling capacitor value used on the BYP pin.

The OCP pin allows the short circuit output current limit threshold to be programmed by means of a resistor from OCP pin to GND. The OCP setting range is from a 0.25A min to 4.25A max.The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value, it will subsequently enter a ON/OFF cycle till the fault is removed.

Features

- **DSCC SMD#5962-F-xxxxx**
- **Input supply range 4.0V to 13.2V.**
- **Output Current up to 1.5A at a T_J=150°C**
- **Output Accuracy ±1.5% Guaranteed over MIL temp range.**
- **Ultra Low Dropout:**
  - **200mV Dropout @ 0.5A**
  - **500mV Dropout @ 1.5A**
- **Noise of 100µV_{RMS} between 300Hz to 300kHz**
- **SET mitigation with no added filtering/diodes**
- Shutdown Current of 10µA Typ.
- Output Adjustable using preset resistors
- PSRR 60dB Typical @ 1kHz
- **EN**able and **PG**ood Feature
- Programmable Soft Start / Inrush Current Limiting
- Adjustable Over Current Protection
- Over-Temperature Shutdown
- Stable with 47µF Min Tantalum Capacitor
- Package 16 Ld Flat Pack
- **Radiation Environment**
  - **High Dose .....100 krad(Si)**
  - **Low Dose .....100 krad(Si)**
  - **SET/SEL/SEB .....86 MeV.cm^2/mg**

Applications

- LDO regulator for Space Power Systems
- DSP, FPGA and µP Core Power Supplies
- Post Regulation of Switched Mode Power Supplies
- Down Hole Drilling

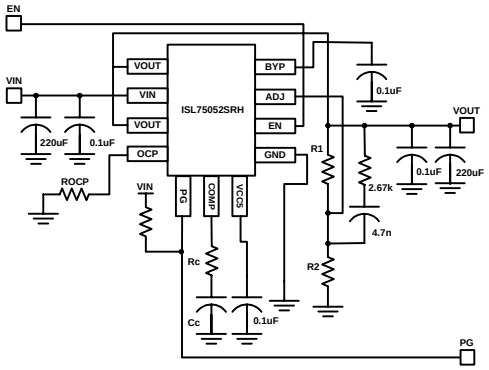
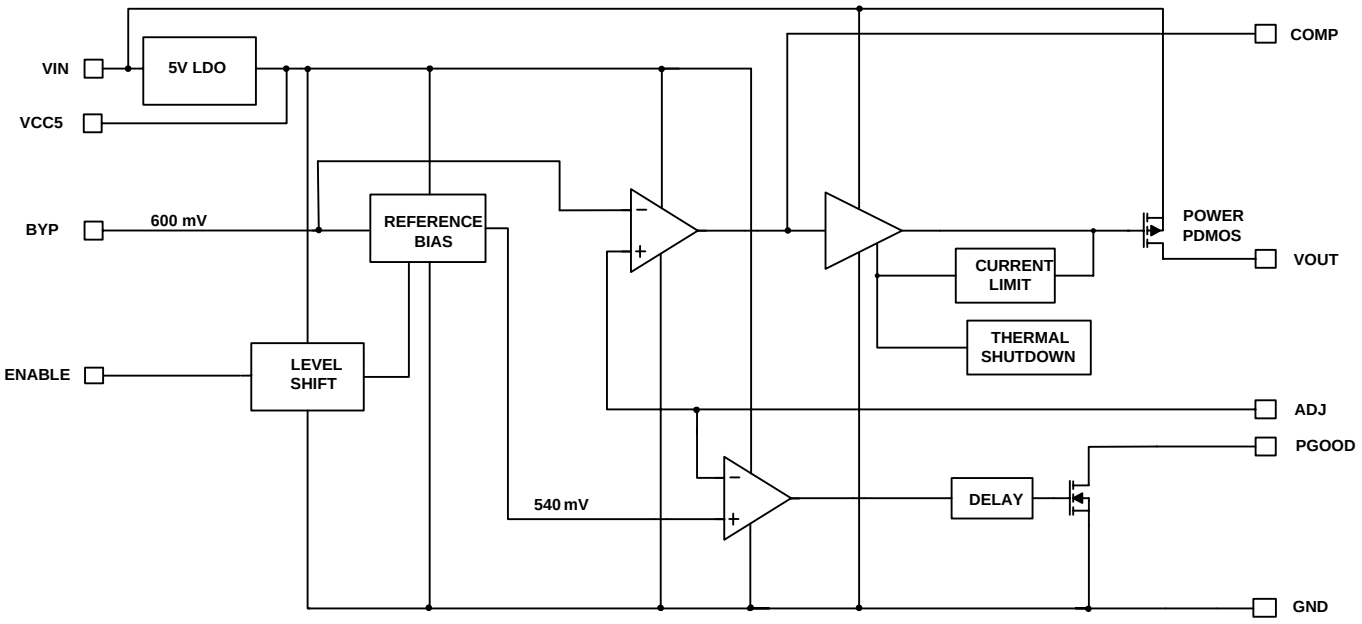


FIGURE 1. TYPICAL APPLICATION

FIGURE 2. DROPOUT VS IOUT

THIS IS A PRE-DEVELOPMENT TARGET DATASHEET. DEVICE FUNCTIONALITY AND SPECIFICATIONS ARE SUBJECT TO CHANGE

Block Diagram



Typical Applications

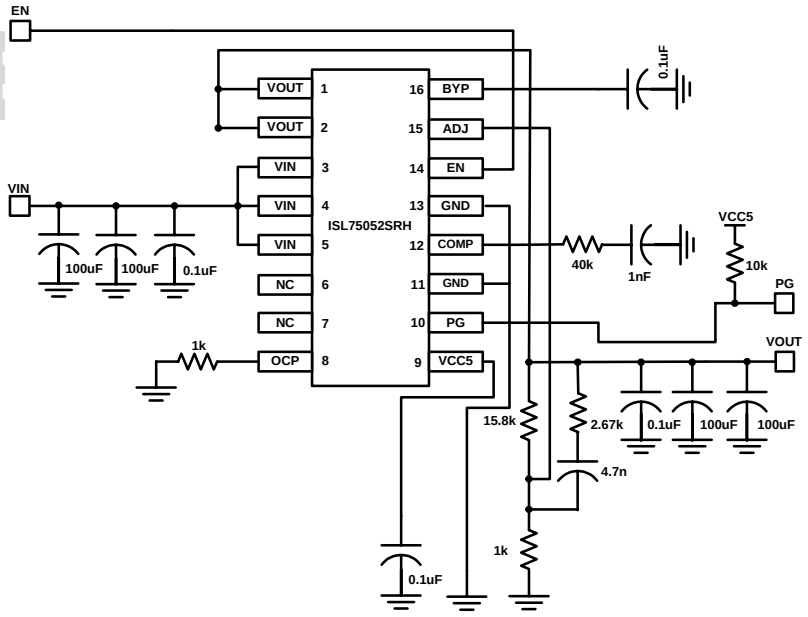
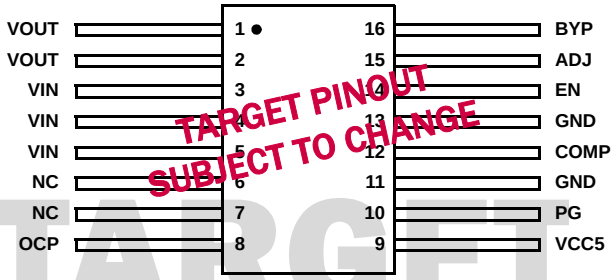


FIGURE 3.

Pin Configuration

ISL75052SRH
(16Ld CDFP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
3,4,5	V_{IN}	Input supply pins.
10	PG	This pin is logic high when V_{OUT} is in regulation signal. A logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
11,13	GND	GND pin. This pin is also connected to the metal lid of the package
9	VCC5	The 5V internal bus is pinned out to accept a decoupling capacitor.
1,2	V_{OUT}	Output voltage pins.
12	COMP	Add compensation capacitor & resistor between COMP and GND, C=1nF typ & R=40kΩ typ
15	VADJ	VADJ pin allows V_{OUT} to be programmed with an external resistor divider.
6,7,11		No connect
16	BYP	Connect a 0.2µF capacitor from BYP pin to GND, to filter the internal VREF.
8	OCP	OCP pin allows the Current limit to be programmed with an external resistor
14	EN	V_{IN} independent chip enable. TTL and CMOS compatible.

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG DWG. #
5962-xxxxxxxxx	ISL75052SRHVF-T	TBD	-55 to +125	16 Ld CDFP	K16.A
5962-xxxxxxxxx	ISL75052SRHQF-T	TBD	-55 to +125	16 Ld CDFP	K16.A
5962-xxxxxxxxx	ISL75052SRHVX-T	TBD	-55 to +125	Die	TBD
ISL75052SRHF/Sample	ISL75052SRHF/Sample	TBD	-55 to +125	Die Sample	TBD
ISL75052SRHF/Proto	ISL75052SRHF/Proto	TBD	-55 to +125	16 Ld CDFP	K16.A

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Absolute Maximum Ratings

V_{IN} Relative to GND (Note 2) . . . . . -0.3 to +14.7V
V_{OUT} Relative to GND (Note 2) . . . . . -0.3 to +14.7V
PG,EN,OCP/ADJ,COMP,REFIN,REFOUT relative to GND (Note 6) . . . -0.3 to +6.5VDC

Recommended Operating Conditions (Notes 10, 11)

Ambient Temperature Range (T_A) (Note 5) . . . . . -55°C to +125°C
Junction Temperature (T_J) (Note 5). . . . . +150°C
V_{IN} Relative to GND . . . . . 4.0V to 13.2V
V_{OUT} Range . . . . . 2.5V to 12.7V
PG, EN, OCP/ADJ relative to GND . . . . . 0V to +5.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
18 Ld CDFP Package (Notes 3, 4)	TBD	8

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Radiation Information

High Dose(Dose Rate = 50 - 300radSi/s) . . . . . 100 krads (Si)
Low Dose(Dose Rate = 10milliradSi/s) . . . . . 100 krads (Si)
SET (V_{OUT} within ±5% During Events . . . . . 86MeV/mg/cm^2
SEL/B (No Latchup/Burnout . . . . . 86MeV/mg/cm^2
The output capacitance used for SEE testing is 2x100µF for C_{IN} and C_{OUT}, 100nF for BYPASS

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 13.2V of 1%.
3. TBD (θ_{JA})
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
6. Electromigration specification defined as lifetime average junction temperature of +150°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: V_{IN} = V_{OUT} + 0.5V, V_{OUT} = 4.0V, C_{IN} = C_{OUT} = 2x100µF 60mohm, AVX type TBJV107K020LBSB0023 or equivalent , T_J = +25°C, I_L = 0A
Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 6 of the data sheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines guaranteed limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Resistor adjust to : 2.5V and 5.0V				
		VOUT=2.5V, 4.0V < V_{IN} < 5.0V; 0A < I_{LOAD} < 1.5A; T_J = -55°C to +125°C	**-1.0**	0.2	**1.0**	%
		VOUT=5.0V, 5.6V < V_{IN} < 6.9V; 0A < I_{LOAD} < 1.5A; T_J = -55°C to +125°C	**-1.0**	0.2	**1.0**	%
		V_{OUT} Resistor adjust to: 10.0V				
		VOUT=10.0V, 10.6V < V_{IN} < 13.2V; 0A < I_{LOAD} < 1.5A, T_J =-55°C to +125°C	**-1.0**	0.2	**1.0**	%
Feedback Pin	V_{ADJ}	T_J = -55°C to +125°C	**596**	600	**604**	mV
BYP Pin	V_{BYP}	4.0V < V_{IN} < 13.2V; I_{LOAD}=0A; T_J = -55°C to +125°C	**596**	600	**604**	mV
DC Input Line Regulation		4.0V < V_{IN} < 13.2V, V_{OUT}=2.5V		3.13	**6.25**	mV
DC Input Line Regulation		4.0V < V_{IN} < 13.2V, V_{OUT}=5.0V		12.5	**25**	mV
DC Input Line Regulation		10.5V < V_{IN} < 13.2V, V_{OUT}=10.0V		50.0	**100.00**	mV
DC Output Load Regulation		V_{OUT}=2.5V; 0A < I_{LOAD} < 1.5A, V_{IN} = 4.0V	**-18.75**	-7.5	**-0.375**	mV
DC Output Load Regulation		V_{OUT}=5.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 4.5V	**-37.5**	-15.0	**-0.75**	mV
DC Output Load Regulation		V_{OUT}=10.0V; 0A < I_{LOAD} < 1.5A, V_{IN} = 10.5V	**-75.0**	-30.0	**-1.5**	mV
Feedback Input Current		V_{ADJ} = 0.6V			1	µA
Ground Pin Current	I_Q	VOUT=2.5V; I_{LOAD} = 0A, 4.0V < V_{IN} < 13.2V	**12**	16	**19**	mA

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: V_{IN} = V_{OUT} + 0.5V, V_{OUT} = 4.0V, C_{IN} = C_{OUT} = 2x100µF 60mohm, AVX type TBJV107K020LBSB0023 or equivalent , T_J = +25°C, I_L = 0A
Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 6 of the data sheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines guaranteed limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Ground Pin Current	I_Q	VOUT=2.5V; I_{LOAD} = 1.5A, 4.0V < V_{IN} < 13.2V	**14**	20	**30**	mA
Ground Pin Current	I_Q	VOUT=10.0V; I_{LOAD} = 0A, 10.5V < V_{IN} < 13.2V	**12**	16	**19**	mA
Ground Pin Current	I_Q	VOUT=10.0V; I_{LOAD} = 1.5A, 10.5V < V_{IN} < 13.2V	**14**	20	**30**	mA
Ground Pin Current in Shutdown	I_{SHDNL}	ENABLE Pin = 0V, V_{IN} = 4.0V, T_A = +125°C		5	**220**	µA
Ground Pin Current in Shutdown	I_{SHDNH}	ENABLE Pin = 0V, V_{IN} = 13.2V, T_A = +125°C		5	**400**	µA
Dropout Voltage (Note 9)	V_{DO}	I_{LOAD} = 0.5A, V_{OUT} = 3.6V & 10V		66	**166**	mV
Dropout Voltage (Note 9)	V_{DO}	I_{LOAD} = 1.0A, V_{OUT} = 3.6V & 10V		130	**330**	mV
Dropout Voltage (Note 9)	V_{DO}	I_{LOAD} = 1.5A, V_{OUT} = 3.6V & 10V		200	**500**	mV
Output Short Circuit Current for 16Ld FP	ISCL	V_{OUT} = 0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 6k, Note 12)	0.4	0.5	0.75	A
Output Short Circuit Current for 16Ld FP	ISCH	V_{OUT} = 0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 600Ω, Note 12)	1.9	2.75	3.6	A
Output Short Circuit Current for TO257	ISCL	V_{OUT} = 0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 6k, Note 12)	0.4	0.5	0.75	A
Output Short Circuit Current for TO257	ISCH	V_{OUT} = 0V, V_{OUT} + 0.5V < V_{IN} < 13.2V, R_{SET} = 600Ω, Note 12)	2.5	3.35	4.2	A
Thermal Shutdown Temperature Note x.x) GNT	TSD	V_{OUT} + 0.5V < V_{IN} < 13.2V	154	175	**196**	°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	V_{OUT} + 0.5V < V_{IN} < 13.2V			**25**	°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	V_{P-P} = 300mV, f = 1kHz, I_{LOAD} = 1.5A; V_{IN} = 4.5V, V_{OUT} = 4.0V	42	60		dB
Input Supply Ripple Rejection Note x.x) GNT	PSRR	V_{P-P} = 300mV, f = 100kHz, I_{LOAD} = 1.5A; V_{IN} = 4.5V, V_{OUT} = 4.0V	15	30		dB
Phase Margin, Note 8)	PM	V_{OUT} = 2.5V,4.0V & 10V C_{OUT} = 2x100µF	50			dB
Gain Margin, Note 8)	GM	V_{OUT} = 2.5V,4.0V & 10V C_{OUT} = 2x100µF	10			dB
Output Noise Voltage, Note 8)		I_{LOAD} = 10mA, BW = 300Hz < f < 300kHz, BYPASS to GND capacitor = 0.2µF		100		$µV_{RMS}$
DEVICE START-UP CHARACTERISTICS						
Enable Pin Characteristics						
Turn-on Threshold		4.0V < V_{IN} < 13.2V	**0.4**	0.8	**1.2**	V
Enable Pin Leakage Current		V_{IN} = 13.2V, EN = 5.5V			**1**	µA
Enable Pin Propagation Delay (EN rise to IOUT rise)		V_{IN}=4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 2x100µF, C_{BYP} = 0.2µF	TBD	TBD	TBD	µs
Enable Pin Turn-on Delay		V_{IN}=4.5V, V_{OUT} = 4.0V, I_{LOAD} = 1.5A, C_{OUT} = 2x100µF, C_{BYP} = 0.2µF		6		ms
Enable Pin Turn-on Delay		V_{IN}= 4.5V, V_{OUT} =4.0V, I_{LOAD} = 1.5A, C_{OUT} = 47µF, C_{BYP} = 0.2µF		50		µs
Hysteresis (Falling Threshold)		Must be independent of V_{IN}, 4.0V < V_{IN} < 13.2V	**TBD**	-120	**TBD**	mV
PG Pin Characteristics						
V_{OUT} Error Flag Rising Threshold			**85**	90	**96**	%
V_{OUT} Error Flag Falling Threshold			**82**	88	**93**	%
V_{OUT} Error Flag Hysteresis			2	2.5	3	$\%V_{OUT}$

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the following specified conditions: V_{IN} = V_{OUT} + 0.5V, V_{OUT} = 4.0V, C_{IN} = C_{OUT} = 2x100µF 60mohm, AVX type TBJV107K020LBSB0023 or equivalent , T_J = +25°C, I_L = 0A
Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 6 of the data sheet and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A defines guaranteed limits.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Error Flag Low Voltage		I_{SINK} = 1mA		60	**100**	mV
Error Flag Low Voltage		I_{SINK} = 10mA		200	**400**	mV
Error Flag Leakage Current		V_{IN} = 13.2V, PG = 5.5V		0.05	**1**	µA

7. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and 125°C, unless otherwise specified.
8. Temperature limits established by characterization and are not production tested.
9. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.
10. Refer to thermal package guidelines in "Applications Information" on page 6. (TBD)
11. Minimum cap on V_{IN} and V_{OUT} required for stability.
12. OCP recovery overshoot should be within +/-4% of the nominal VOUT setpoint.
13. The device can work down to a VOUT of 0.8V however the SET performance of <+/-5% at LET=86MeV.cm2/mg is guaranteed at VOUT=>2.5V only. SET tests performed with 2x100uF 10V 60mohm & 0.1uF CDR04 X7R capacitor on the input and output. Capacitor on BYP=0.1uF CDR04 X7R

Applications Information

Input Voltage Requirements

This RH LDOs will work from a V_{IN} in the range of 4.0V to 13.2V. The input supply can have a tolerance of as much as ±10% for conditions noted in the specification table. The minimum guaranteed input voltage is 4.0V. However, due to the nature of an LDO; V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The Dropout spec of this family of LDOs has been generously specified in order to allow applications to design for efficient operation.

External Capacitor Requirements

GENERAL GUIDELINE

External capacitors are required for proper operation. Careful attention must be paid to layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

RH operation requires the use of a combination of Tantalum and Ceramic capacitors to achieve a good volume to capacitance ratio. The recommended combination is a 2x100µF 60mohm, DSSC 07016 rated tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 ceramic capacitor to be connected to V_{OUT} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

INPUT CAPACITOR

RH operation requires the use of a combination of Tantalum and Ceramic capacitors to achieve a good capacitance to volume ratio. The recommended combination is a 2x100µF 60mohm, DSSC 07016 rated tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 ceramic capacitor to be connected to V_{IN} and Ground pins of the LDO with PCB traces no longer than 0.5cm.

Current Limit Protection

The RH LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit performs as a constant current source when the output current exceeds the current limit threshold which can be adjusted by means of a resistor connected between the OCP pin and GND. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition the LDO will begin to cycle on and off due to the die temperature exceeding thermal fault condition. However, one may never witness thermal cycling if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown.

Thermal Fault Protection

In the event the die temperature exceeds typically +170°C, then the output of the LDO will shut down to zero until the die temperature can cool down to typically +150°C. The level of power combined with the thermal impedance of the package (RthJC of 5°C/W for the 18Ld CDFP package) will determine if the junction temperature exceeds the thermal shutdown temperature specified in the specification table (see thermal packaging guidelines).

TABLE 1.

FN#	Rev	Date	Description
SPGLDO15A.0	0.0	12/10/10	First Draft
SPGLDO15A.0	0.1	02/22/11	Update VINmin & VREF
SPGLDO15A.0	0.2	05/23/11	Update EC table
SPGLDO15A.0	0.3	06/21/11	Update pin assignment & EC table
SPGLDO15A.0	0.4	07/06/11	Format, Front Page, 16Ld FP updates

FN#	Rev	Date	Description
SPGLDO15A.0	0.5	07/06/11	Change pin assignment in order to have a common die for 16ld and TO257 packages and maintain PTP.
SPGLDO15A.0	0.6	09/23/11	Change pin 11 to GND and updates
SPGLDO15A.0	0.7	11/16/11	Updated PGOOD thresholds

Typical Operating Performance

PLACEHOLDER

FIGURE 4.

PLACEHOLDER

FIGURE 5.

PLACEHOLDER

FIGURE 6.

PLACEHOLDER

FIGURE 7.

PLACEHOLDER

FIGURE 8.

PLACEHOLDER

FIGURE 9.

Typical Operating Performance

PLACEHOLDER

FIGURE 10.

PLACEHOLDER

FIGURE 11.

PLACEHOLDER

FIGURE 12.

PLACEHOLDER

FIGURE 13.

PLACEHOLDER

FIGURE 14.

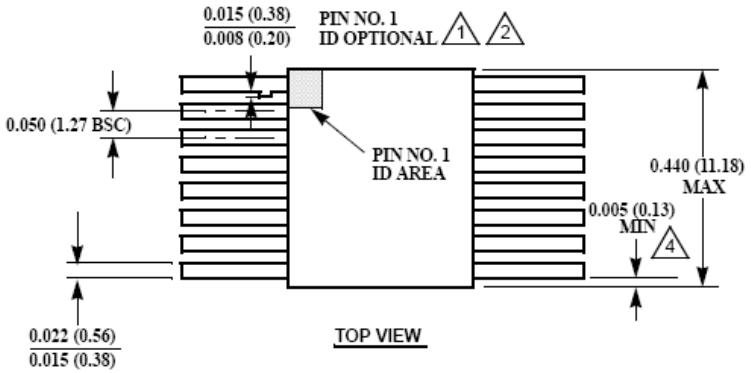
PLACEHOLDER

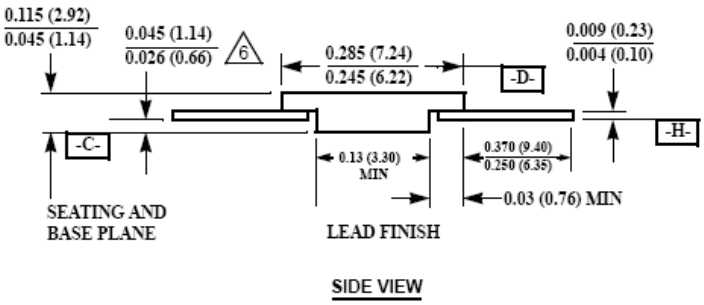
FIGURE 15.

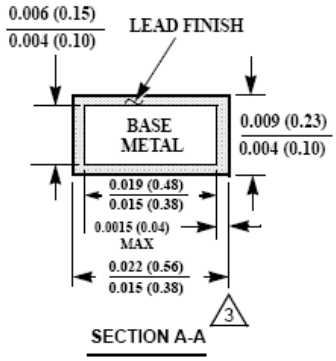
Package Outline Drawing

K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Die Map & Coordinates