ISLA224S25IR48EV1Z

-Title

-Device Under Test

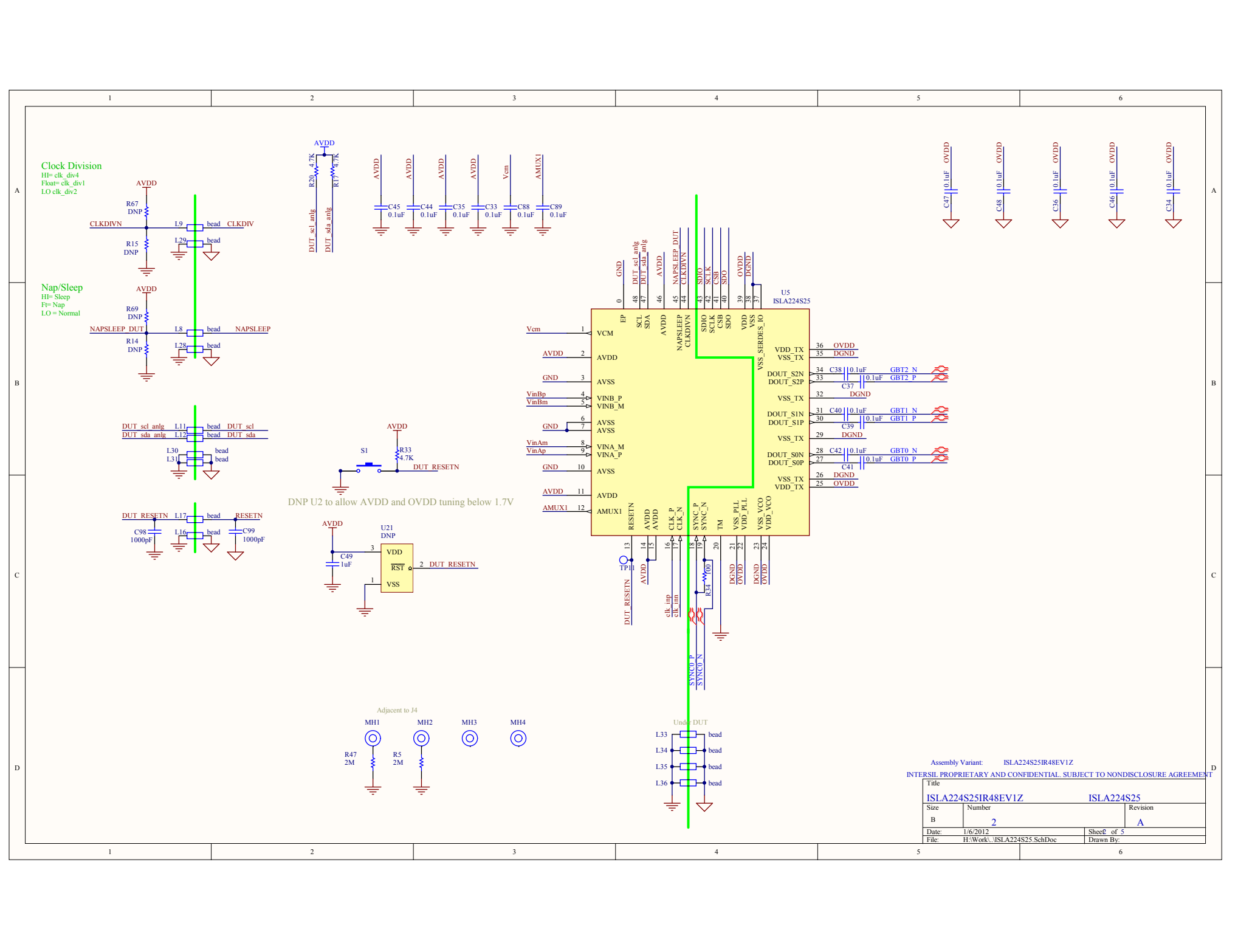
-Analog Inputs & Sampling Clock

-Digital IO, ID and Config EEPROM

-Power Regulator & Measurement

Assembly Variant: ISLA224S25IR48EV1Z

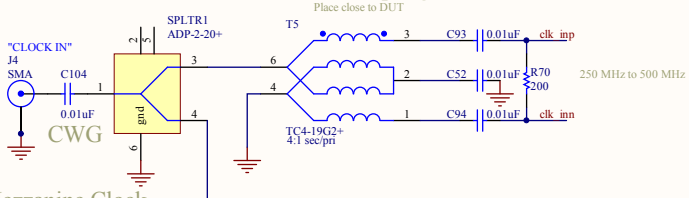
Title		
ISLA224S25IR48EV1Z Title		
Size: B	Number: 1	Revision: A
Date: 1/6/2012		Sheet 1 of 5
File: H:\Work\..\Title.SchDoc		Drawn By:


Clock Division
HI= clk_div4
Float= clk_div1
LO clk_div2
Nap/Sleep
HI= Sleep
Ft= Nap
LO = Normal
DNP U2 to allow AVDD and OVDD tuning below 1.7V
Adjacent to J4
Under DUT
U5
ISLA224S25
U21
DNP
MH1
MH2
MH3
MH4
Assembly Variant: ISLA224S25IR48EV1Z
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
ISLA224S25IR48EV1Z ISLA224S25
Size B
Number 2
Revision A
Date: 1/6/2012
Sheet 2 of 5
File: H:\Work\..\ISLA224S25.SchDoc
Drawn By:

C32/C43
For Sampling Rates > 200MSPS, DNP
For Sampling Rates <= 200MSPS and Input Frequenices <= 200MHz,
use 5.1pF 0603 cap (x2y not necessary).

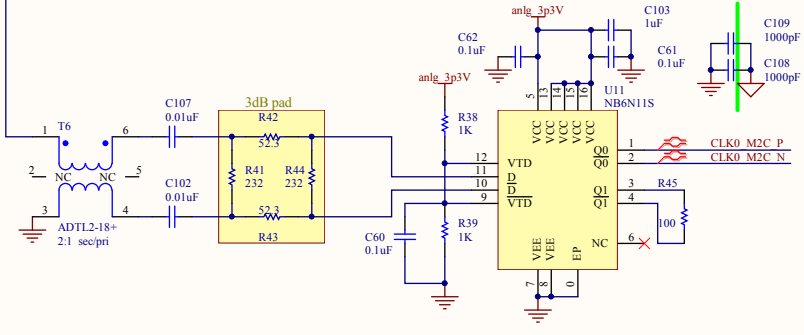
Sampling Clock

Place close to DUT



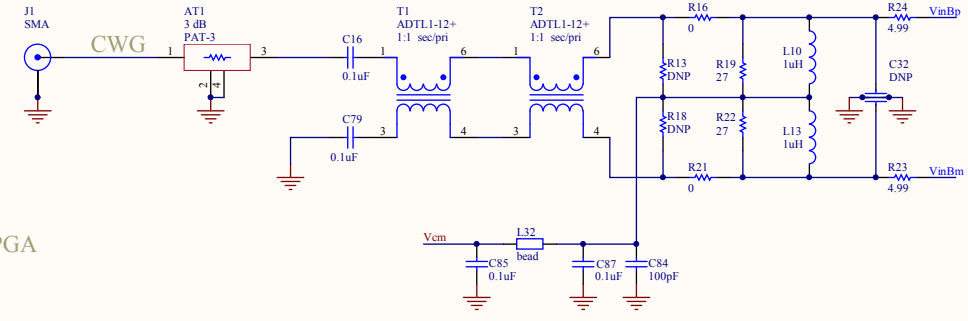
Mezzanine Clock

Reference Clock

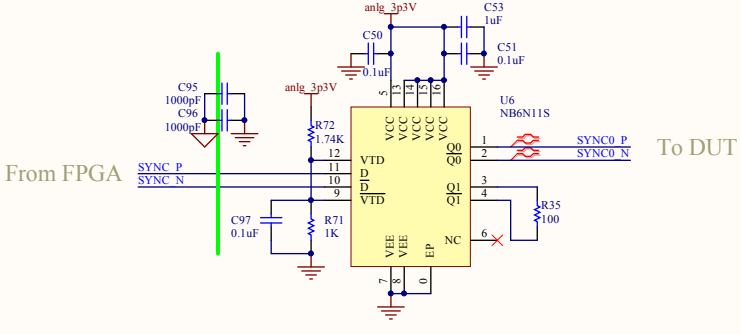


To FPGA

Analog Input B

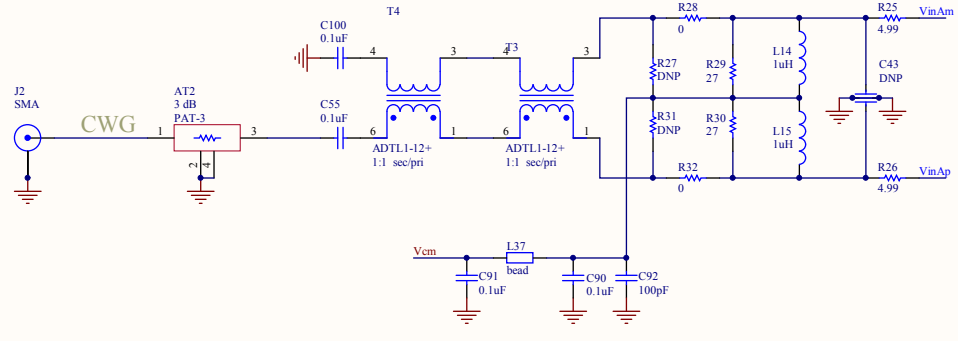


SYNC from FPGA



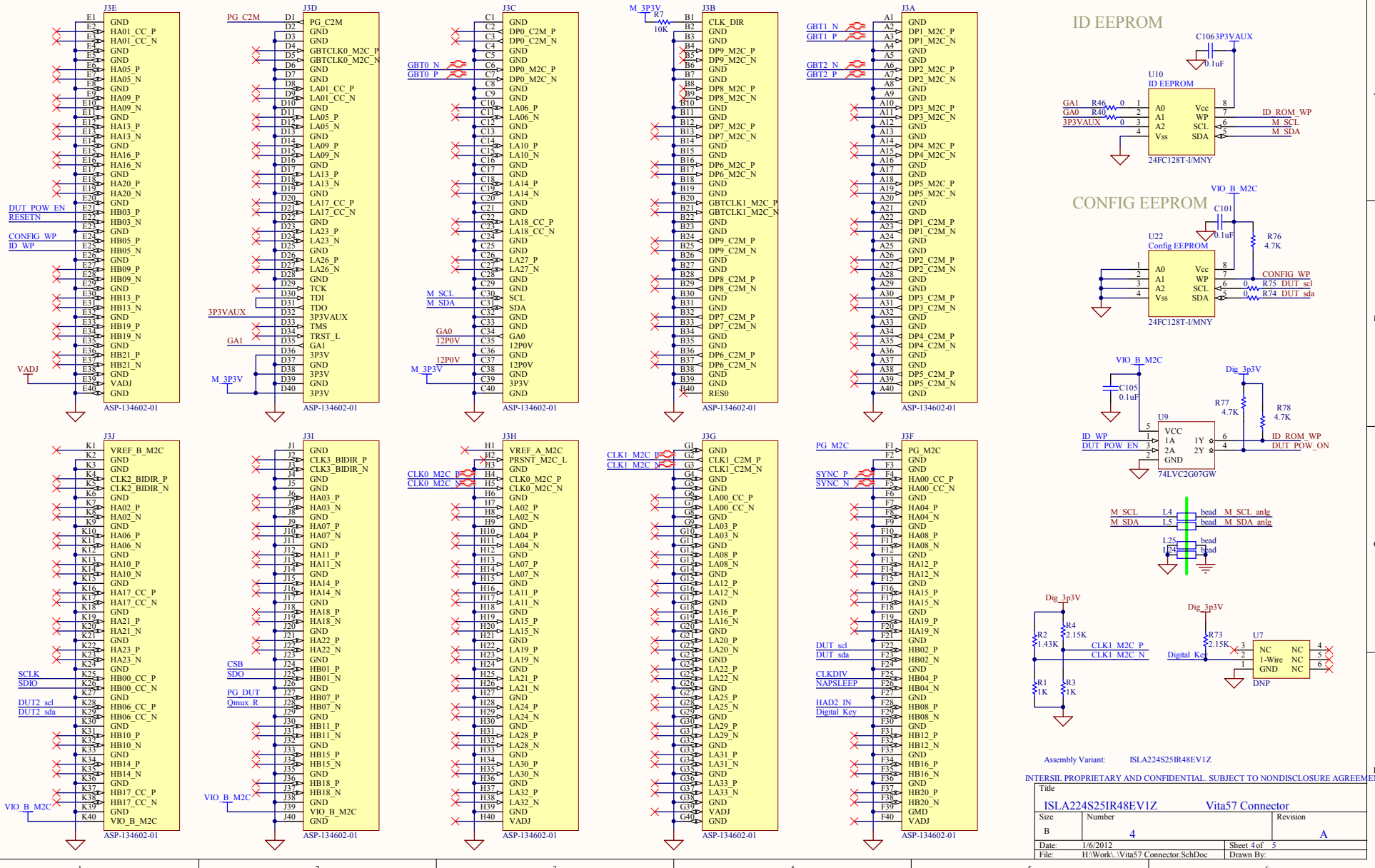
To DUT

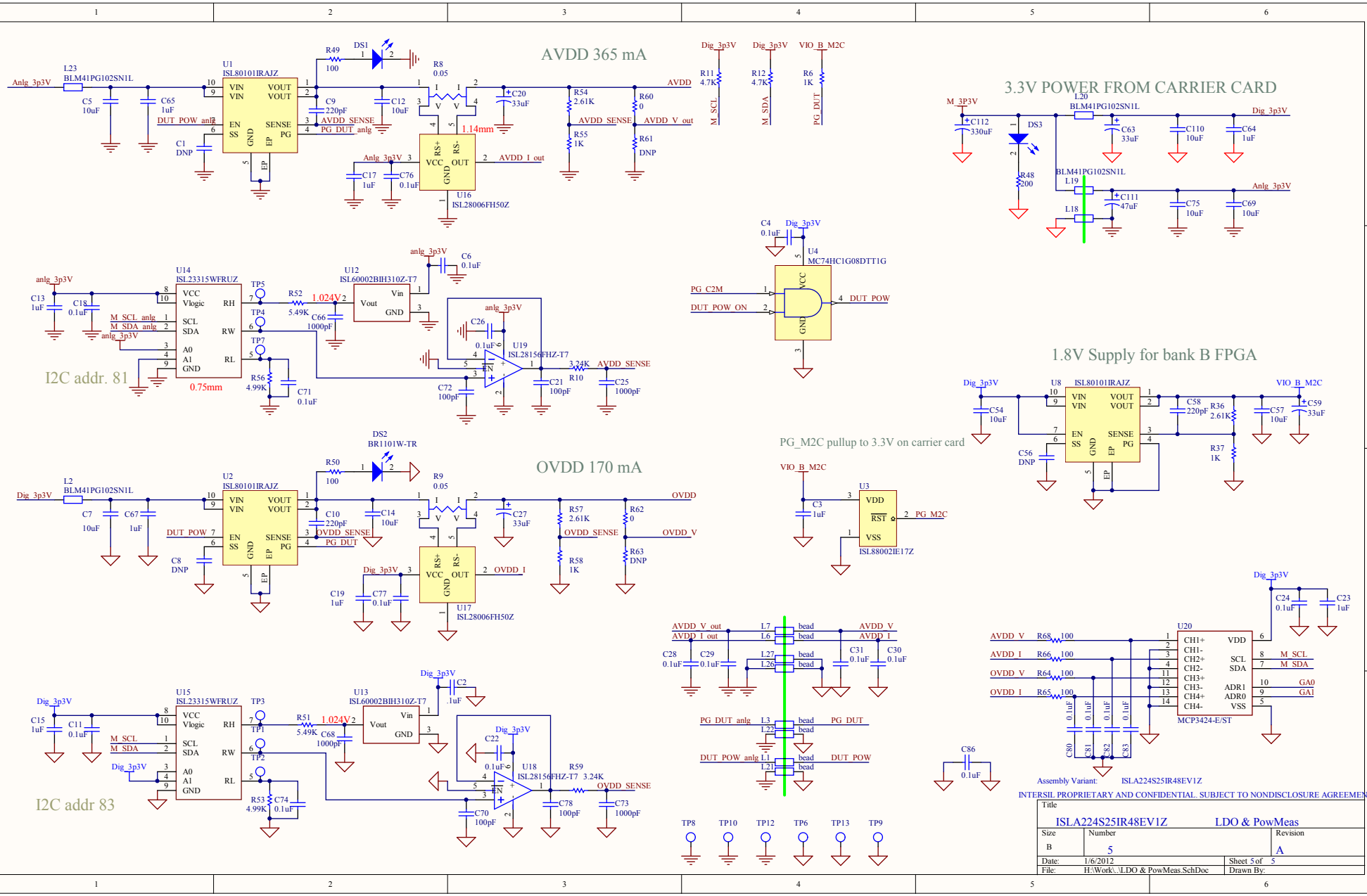
Analog Input A



Assembly Variant: ISLA224S25IR48EV1Z

Title	ISLA224S25IR48EV1Z AnlgInput & SampClk	
Size: B	Number: 3	Revision: A
Date: 1/6/2012	Sheet 3 of 5	
File: H:\Work\..\AnlgInput & SampClk.SchDoc	Drawn By:	


J3E
J3D
J3C
J3B
J3A
J3J
J3I
J3H
J3G
J3F
ASP-134602-01
DUT_POW_EN
RESETN
CONFIG_WP
ID_WP
VADJ
PG_C2M
GBT0_N
GBT0_P
M_SCL
M_SDA
GA0
12P0V
M_3P3V
3P3VAUX
GA1
GBT1_N
GBT1_P
GBT2_N
GBT2_P
SCLK
SDIO
DUT2_scl
DUT2_sda
CSB
SDO
PG_DUT
Qmux_R
VIO_B_M2C
CLK0_M2C_P
CLK0_M2C_N
CLK1_M2C_P
CLK1_M2C_N
SYNC_P
SYNC_N
DUT_scl
DUT_sda
CLKDIV
NAPSLEEP
HAD2_IN
Digital_Key
ID EEPROM
U10
ID EEPROM
24FC128T-I/MNY
ID_ROM_WP
CONFIG EEPROM
U22
Config EEPROM
R75_DUT_scl
R74_DUT_sda
U9
74LVC2G07GW
ID_ROM_WP
DUT_POW_ON
M_SCL_anlg
M_SDA_anlg
Dig_3p3V
U7
DNP
Assembly Variant:
ISLA224S25IR48EV1Z
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
ISLA224S25IR48EV1Z
Vita57 Connector
Size
B
Number
4
Revision
A
Date:
1/6/2012
Sheet 4 of 5
File:
H:\Work\..\Vita57 Connector.SchDoc
Drawn By:


AVDD 365 mA
OVDD 170 mA
3.3V POWER FROM CARRIER CARD
1.8V Supply for bank B FPGA
PG_M2C pullup to 3.3V on carrier card
I2C addr. 81
I2C addr 83
0.75mm
1.14mm
U1 ISL80101IRAJZ
U2 ISL80101IRAJZ
U8 ISL80101IRAJZ
U14 ISL23315WFRUZ
U15 ISL23315WFRUZ
U12 ISL60002BIH310Z-T7
U13 ISL60002BIH310Z-T7
U16 ISL28006FH50Z
U17 ISL28006FH50Z
U18 ISL28156FHZ-T7
U19 ISL28156FHZ-T7
U3 ISL88002IE17Z
U4 MC74HC1G08DTT1G
U20 MCP3424-E/ST
DS1
DS2 BR1101W-TR
DS3
Anlg_3p3V
Dig_3p3V
M_3P3V
VIO_B_M2C
AVDD
OVDD
AVDD_V_out
OVDD_V
AVDD_I_out
OVDD_I
AVDD_SENSE
OVDD_SENSE
PG_DUT_anlg
PG_DUT
DUT_POW_anlg
DUT_POW
PG_C2M
DUT_POW_ON
PG_M2C
M_SCL
M_SDA
Assembly Variant: ISLA224S25IR48EV1Z
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
ISLA224S25IR48EV1Z LDO & PowMeas
Size B
Number 5
Revision A
Date: 1/6/2012
Sheet 5 of 5
File: H:\Work\..\LDO & PowMeas.SchDoc
Drawn By: