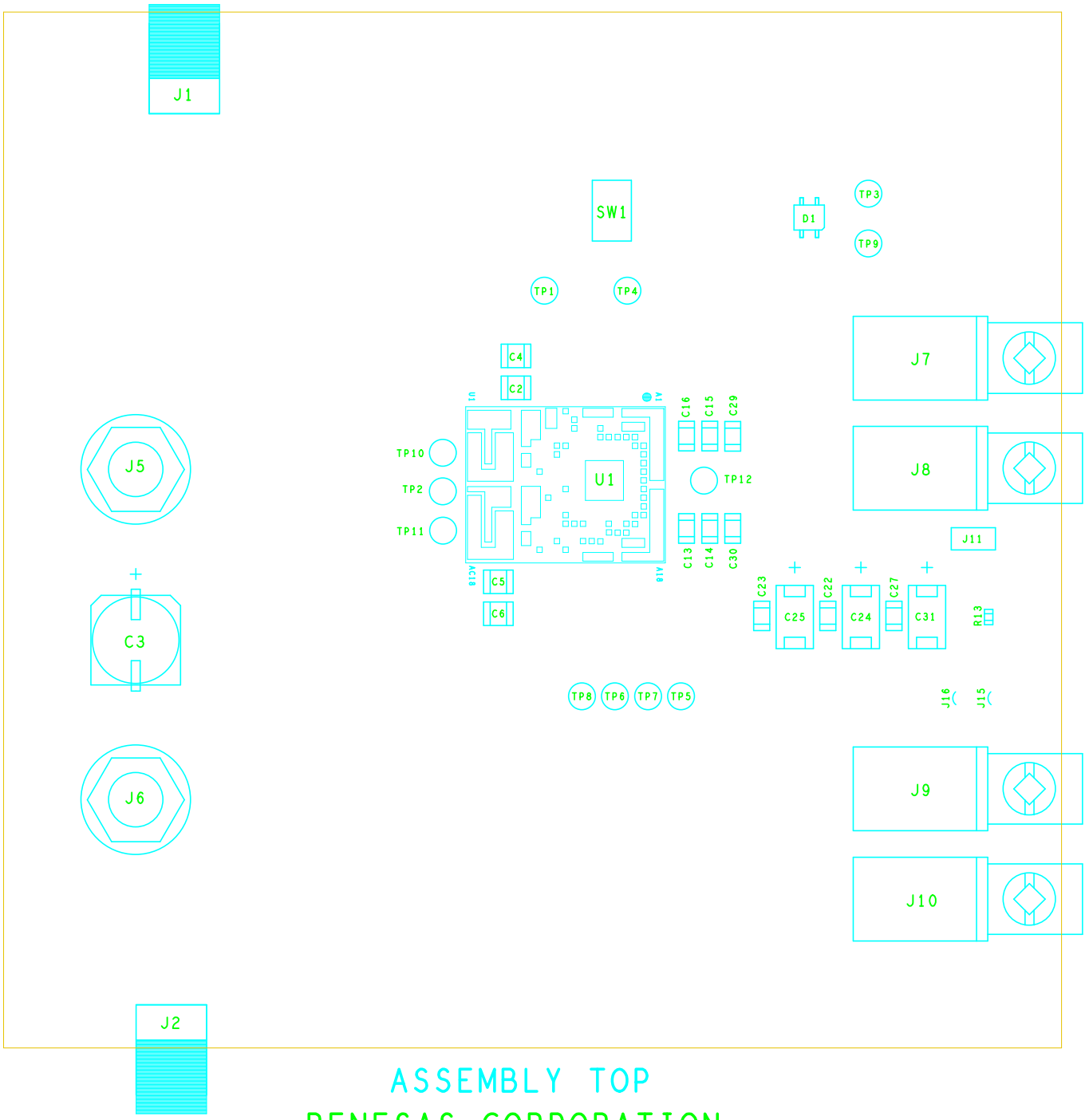
# RTKA2108702H00000BU Rev.B

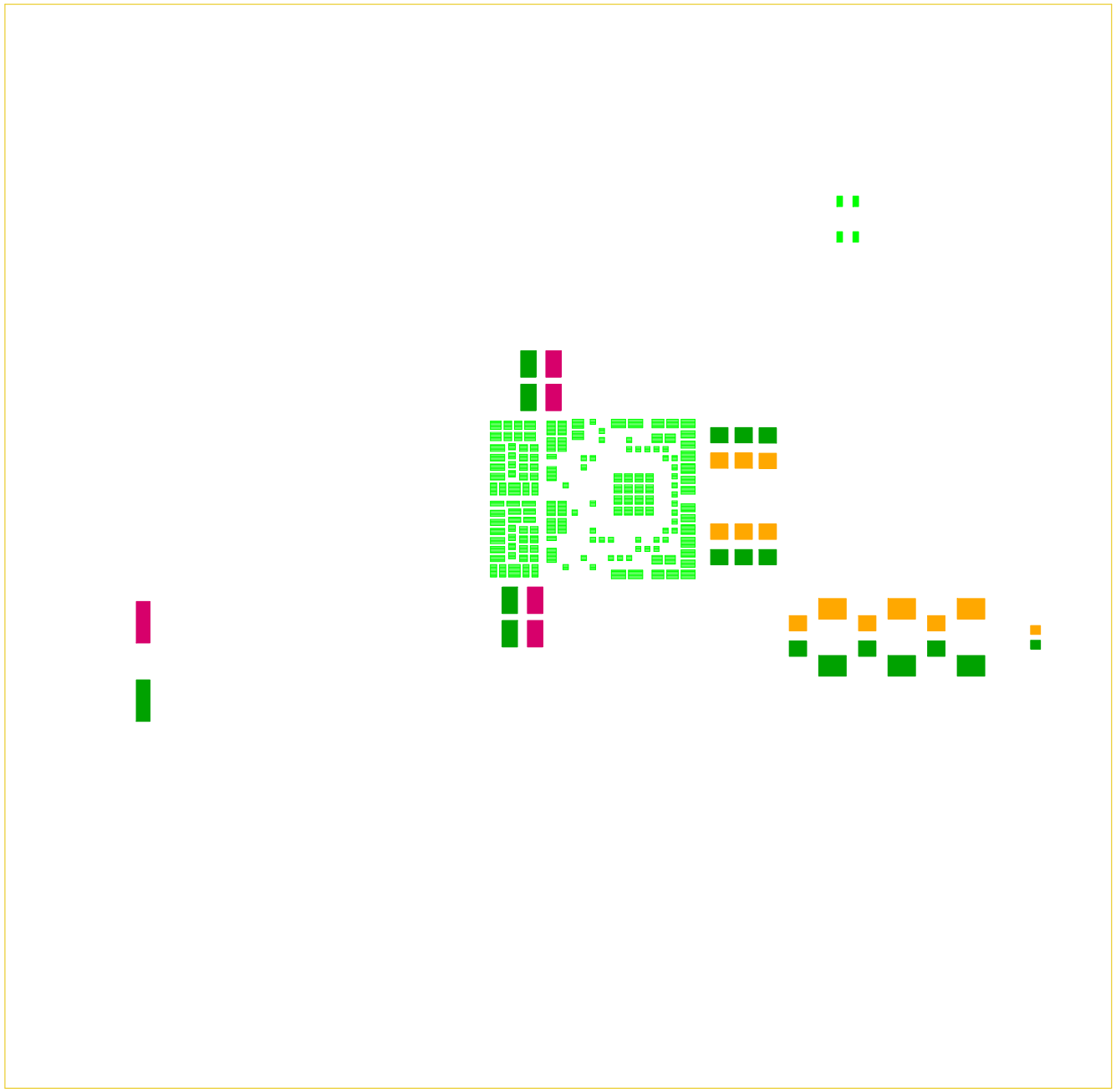



ASSEMBLY TOP

RENESAS CORPORATION

07-26-2018

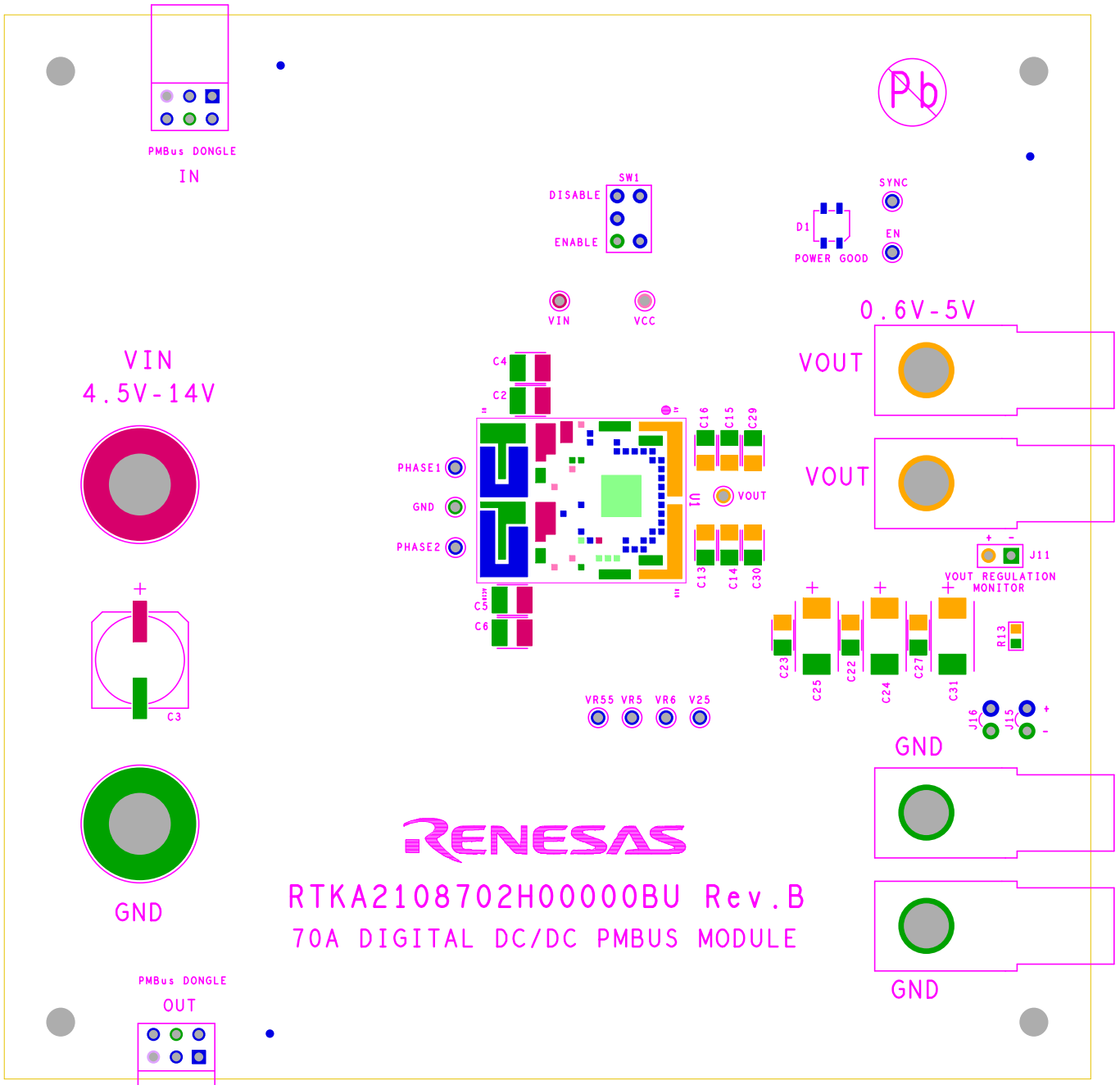
RTKA2108702H00000BU Rev.B



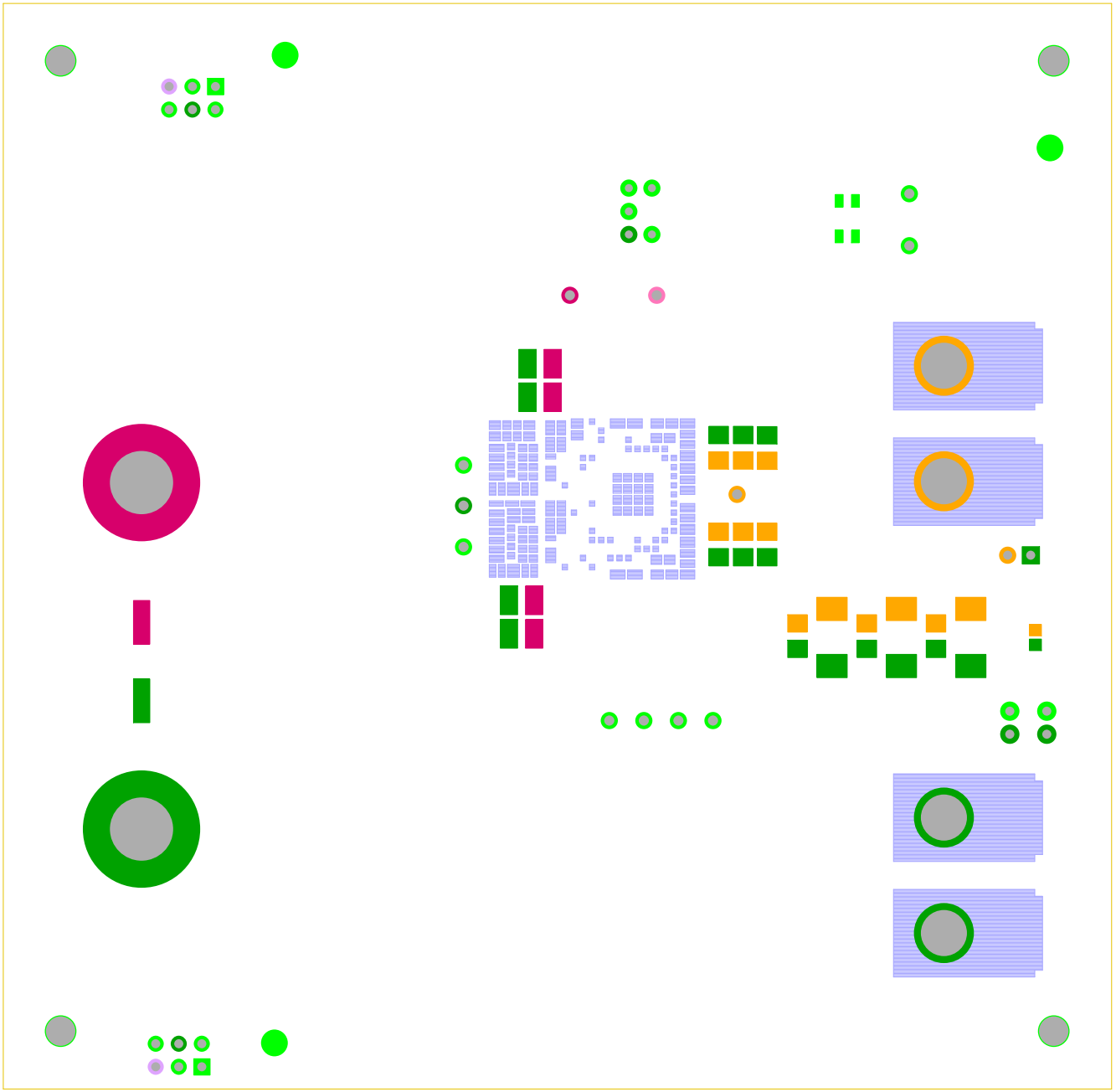
SOLDER PASTE TOP

RENESAS CORPORATION

07-26-2018


RTKA2108702H00000BU Rev.B
PMBus DONGLE
IN
SW1
DISABLE
ENABLE
D1
POWER GOOD
SYNC
EN
VIN
VCC
0.6V-5V
VOUT
VOUT
VIN
4.5V-14V
C4
C2
C16
C15
C29
PHASE1
GND
PHASE2
U1
VOUT
C13
C14
C30
C3
C6
J11
VOUT REGULATION
MONITOR
R13
C23
C25
C22
C24
C27
C31
VR55
VR5
VR6
V25
J16
J15
GND
GND
RENESAS
RTKA2108702H00000BU Rev.B
70A DIGITAL DC/DC PMBUS MODULE
PMBus DONGLE
OUT
SILK SCREEN TOP
RENESAS CORPORATION
07-26-2018

RTKA2108702H00000BU Rev.B

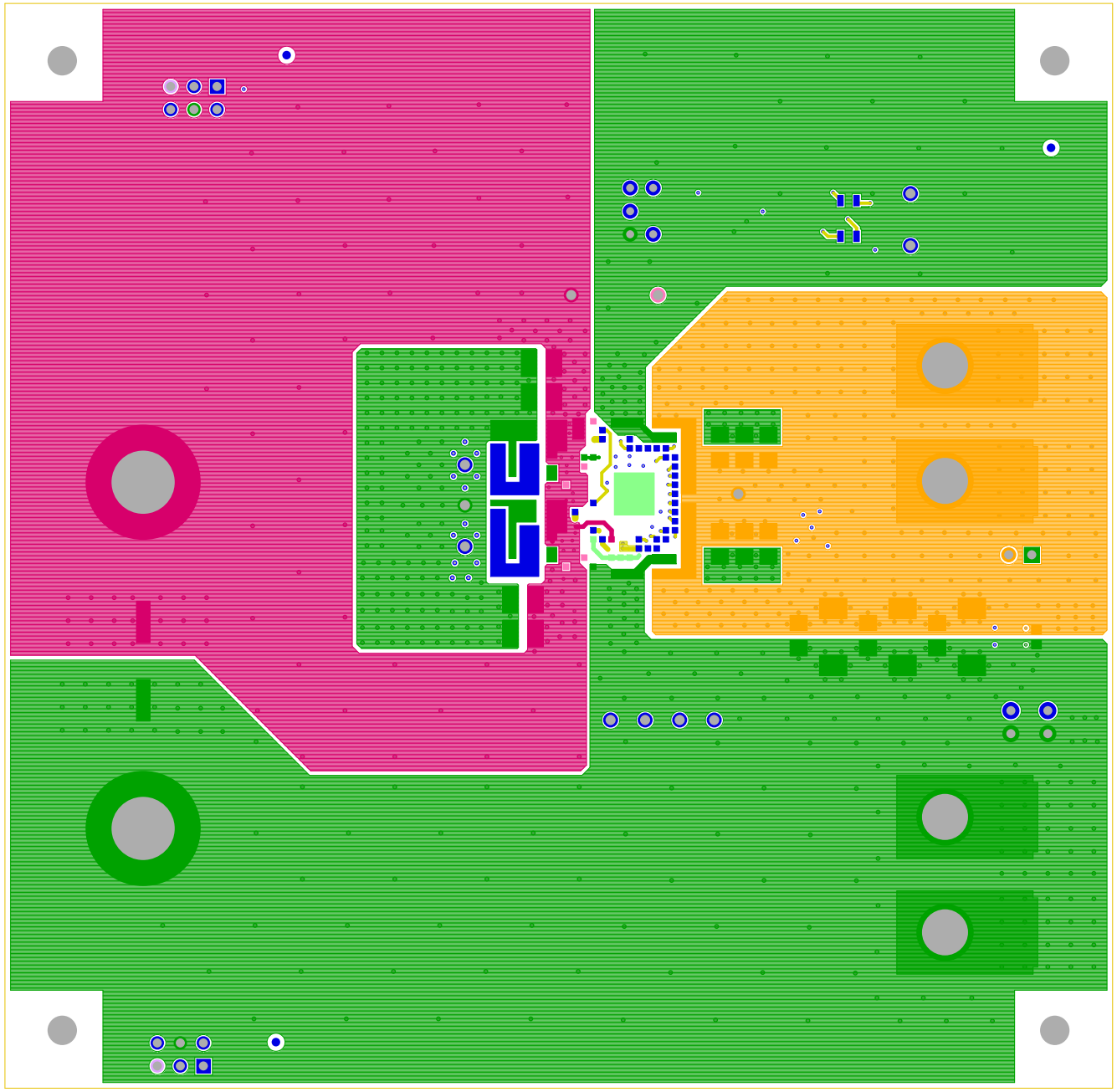


SOLDER MASK TOP

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

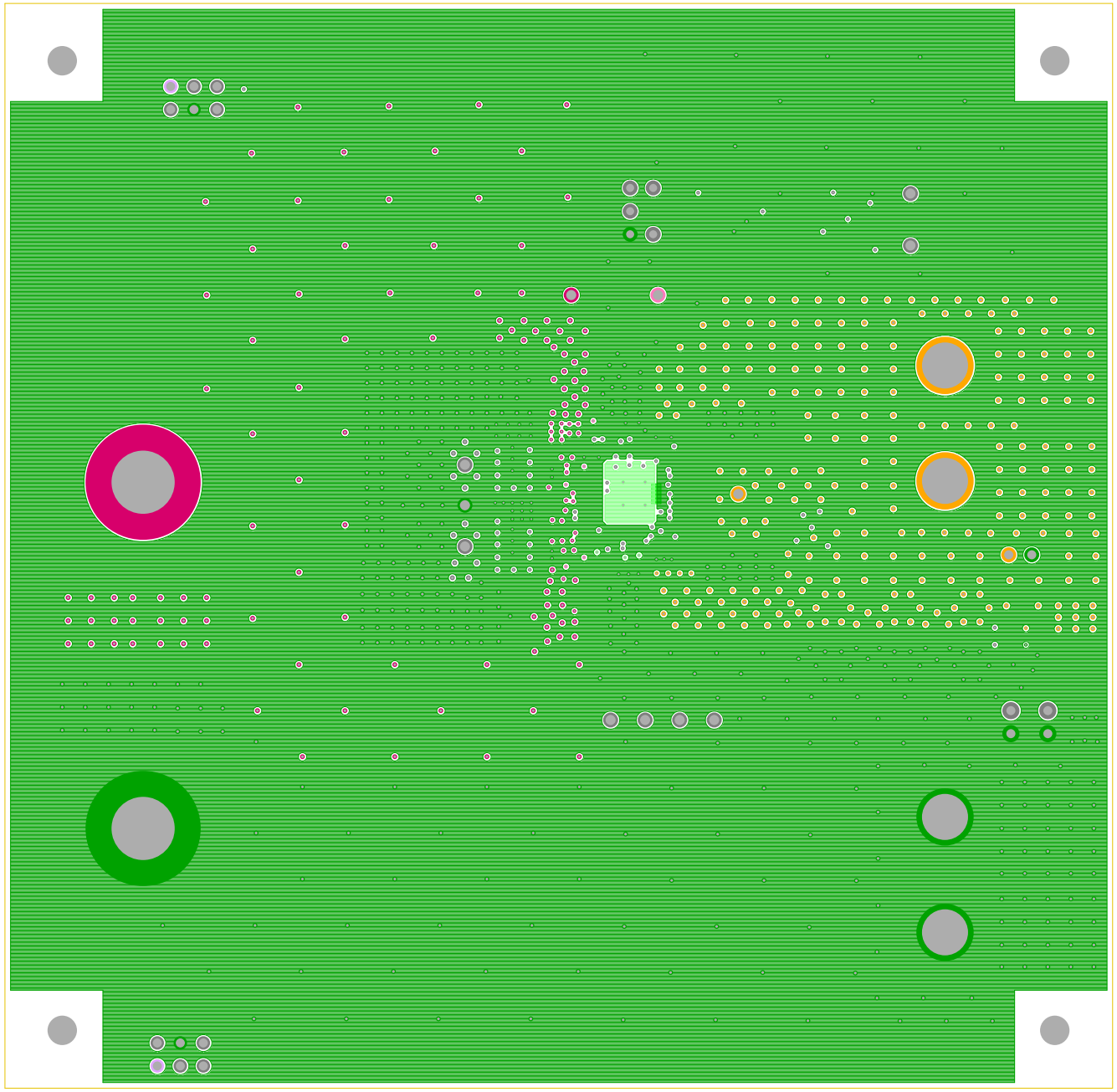


TOP LAYER COMPONENT SIDE

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

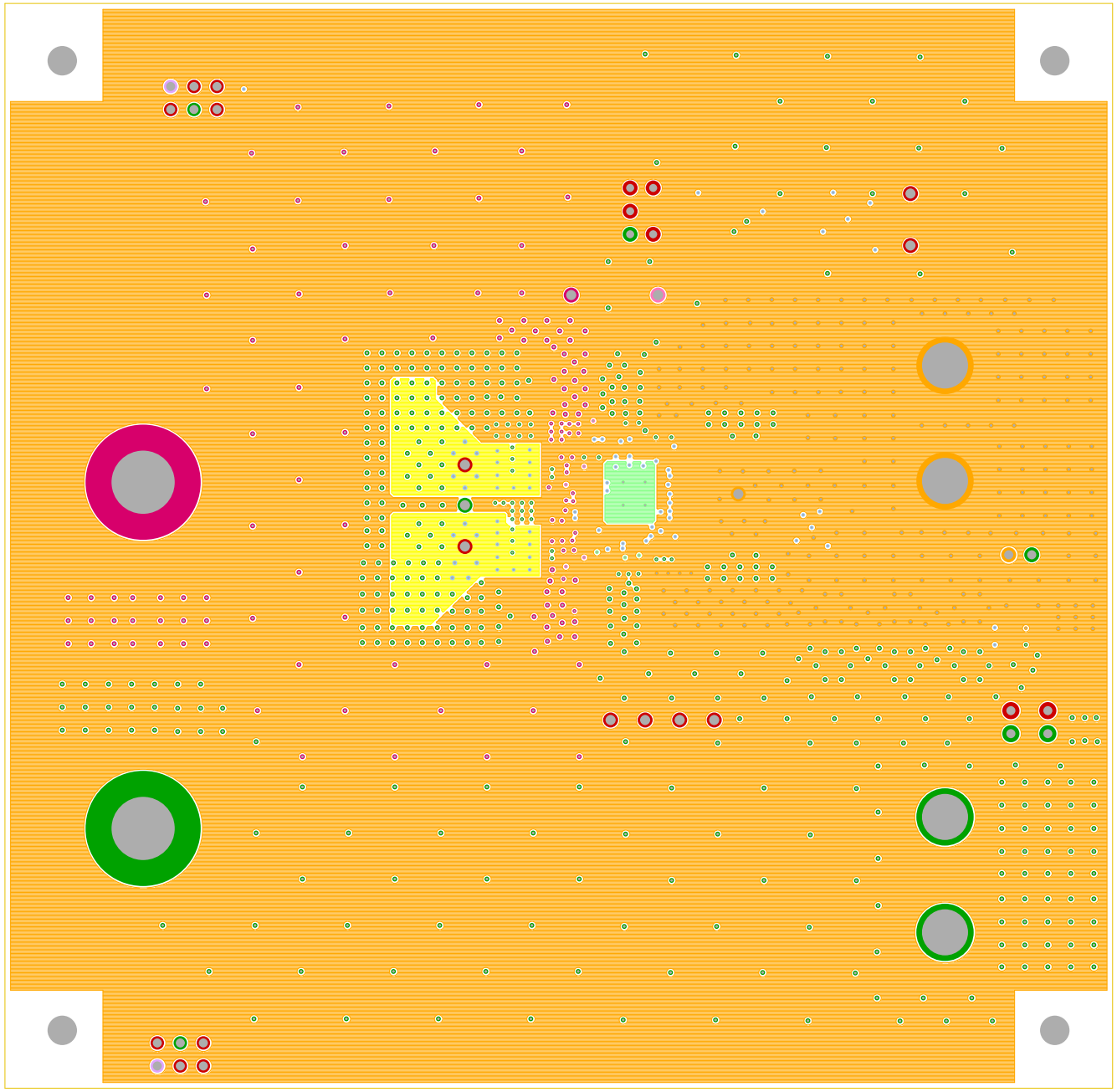


LAYER 2

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

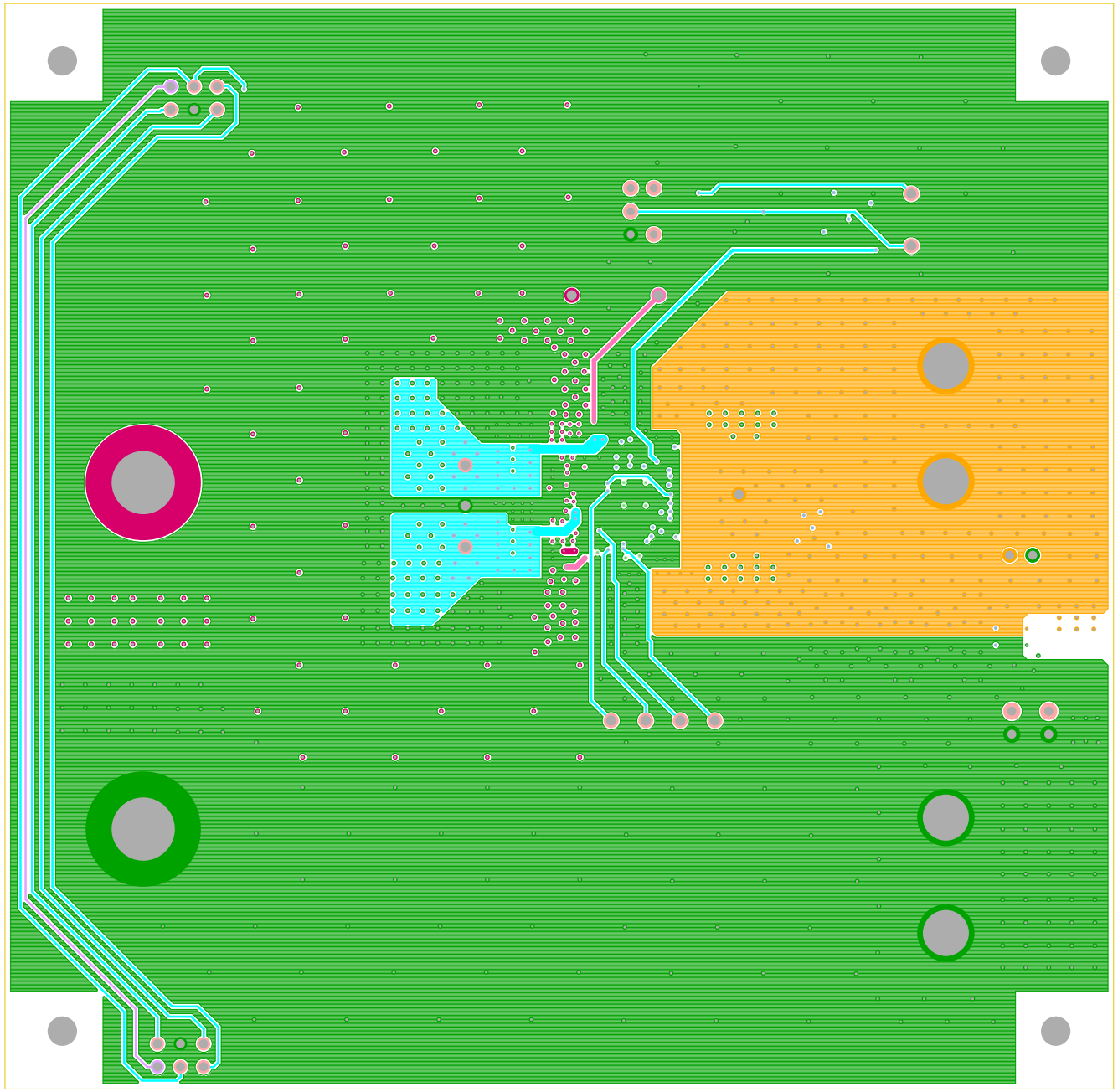


LAYER 3

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

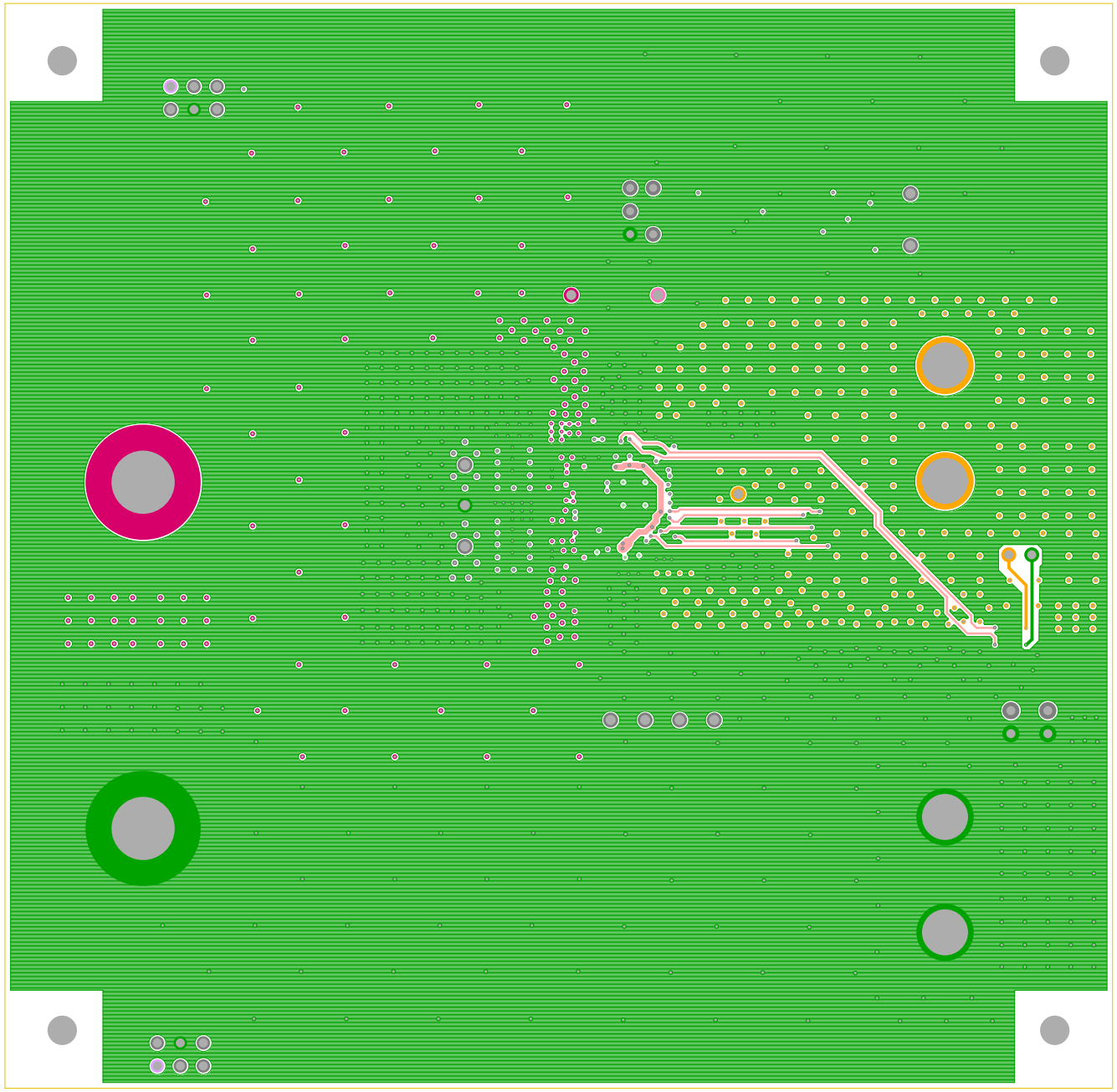


LAYER 4

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

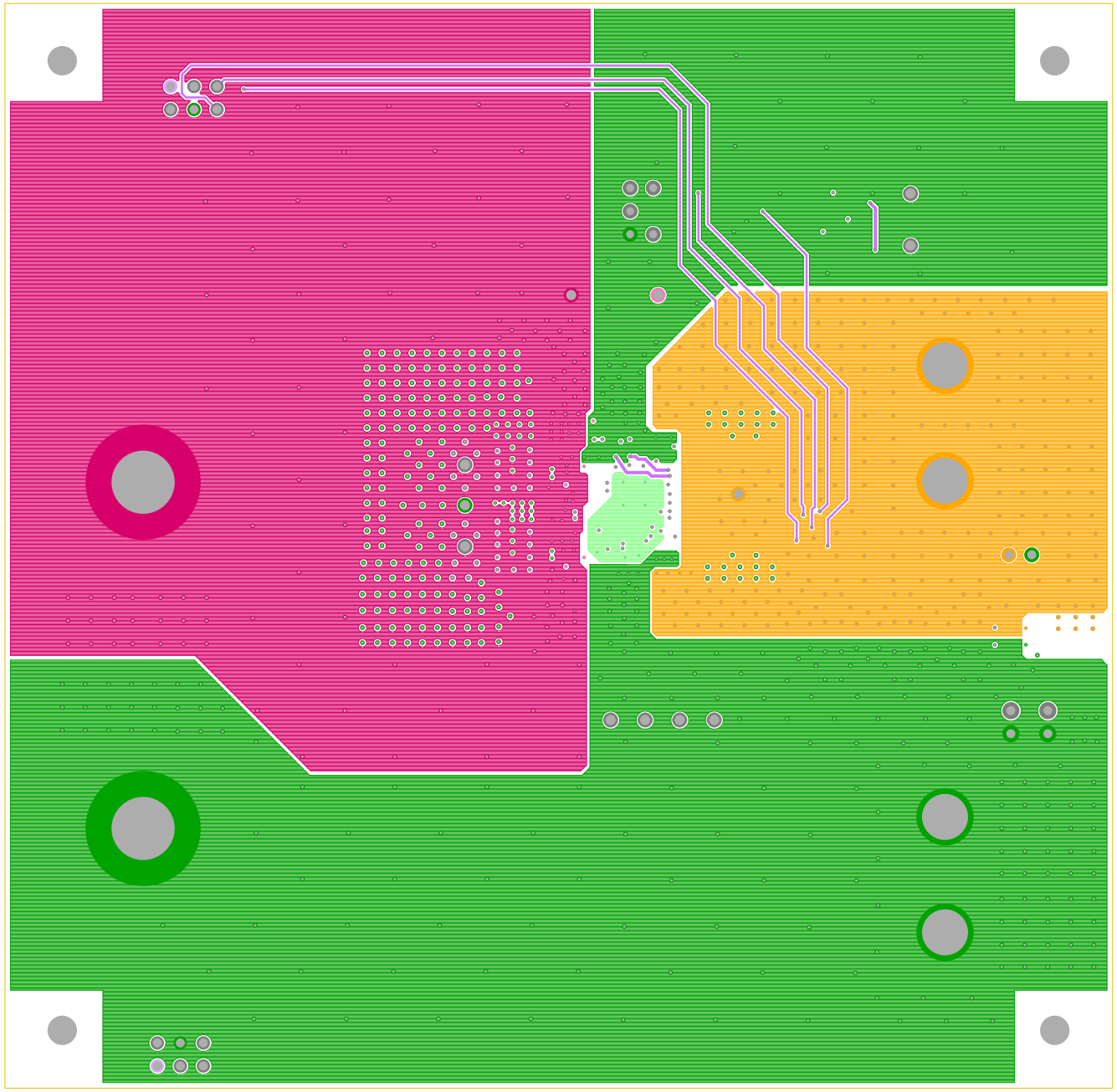


LAYER 5

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

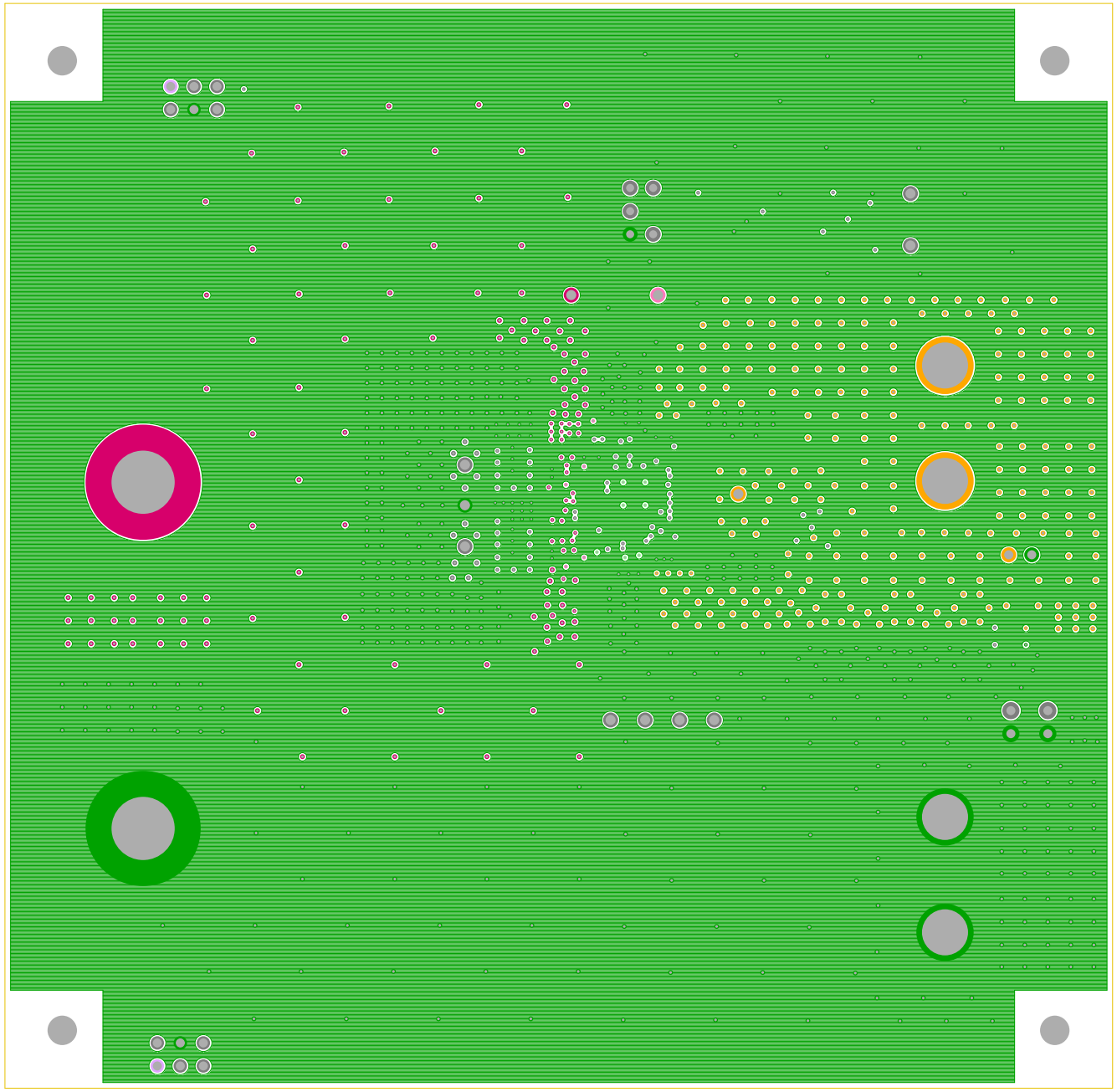


LAYER 6

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

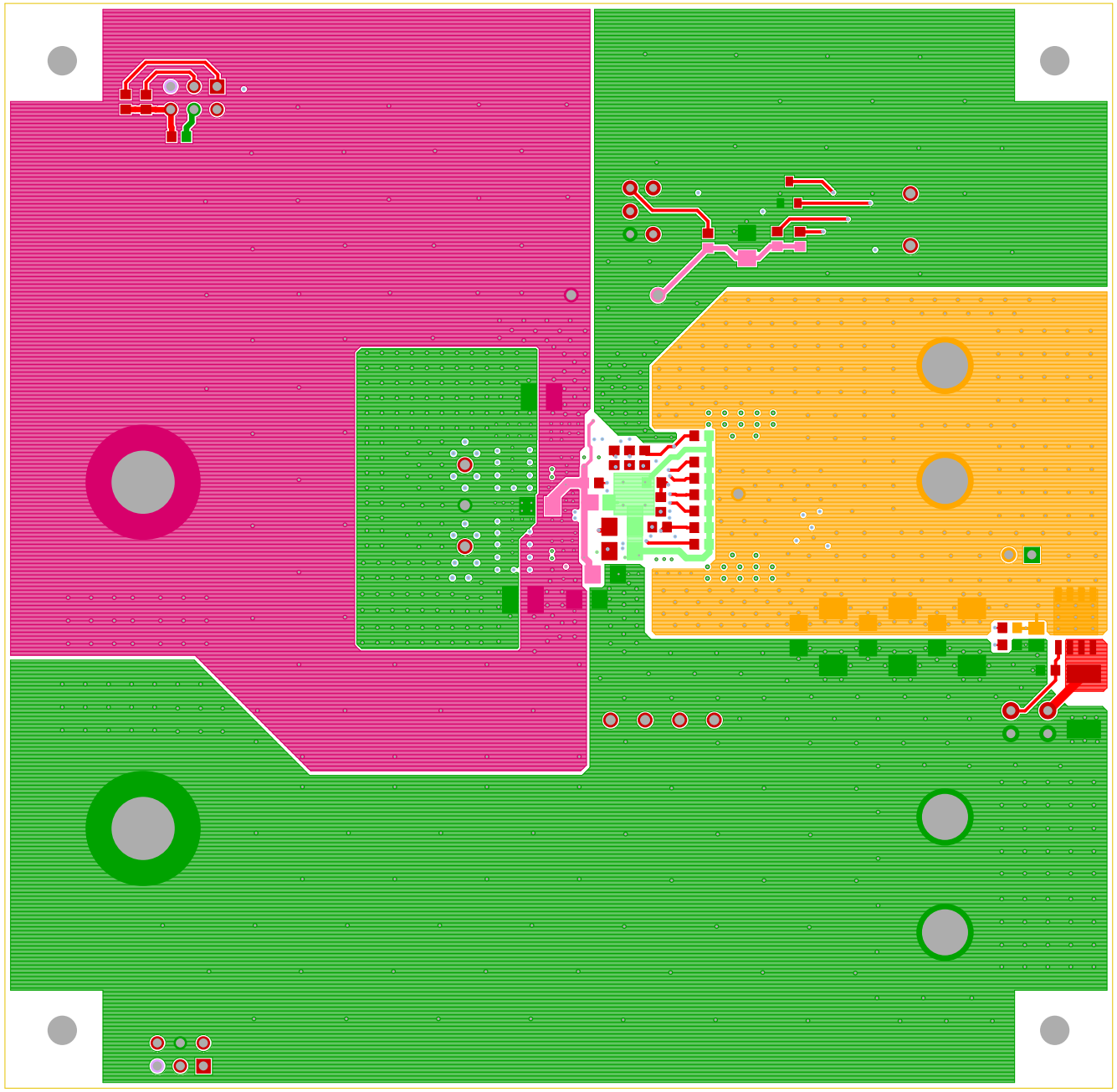


LAYER 7

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

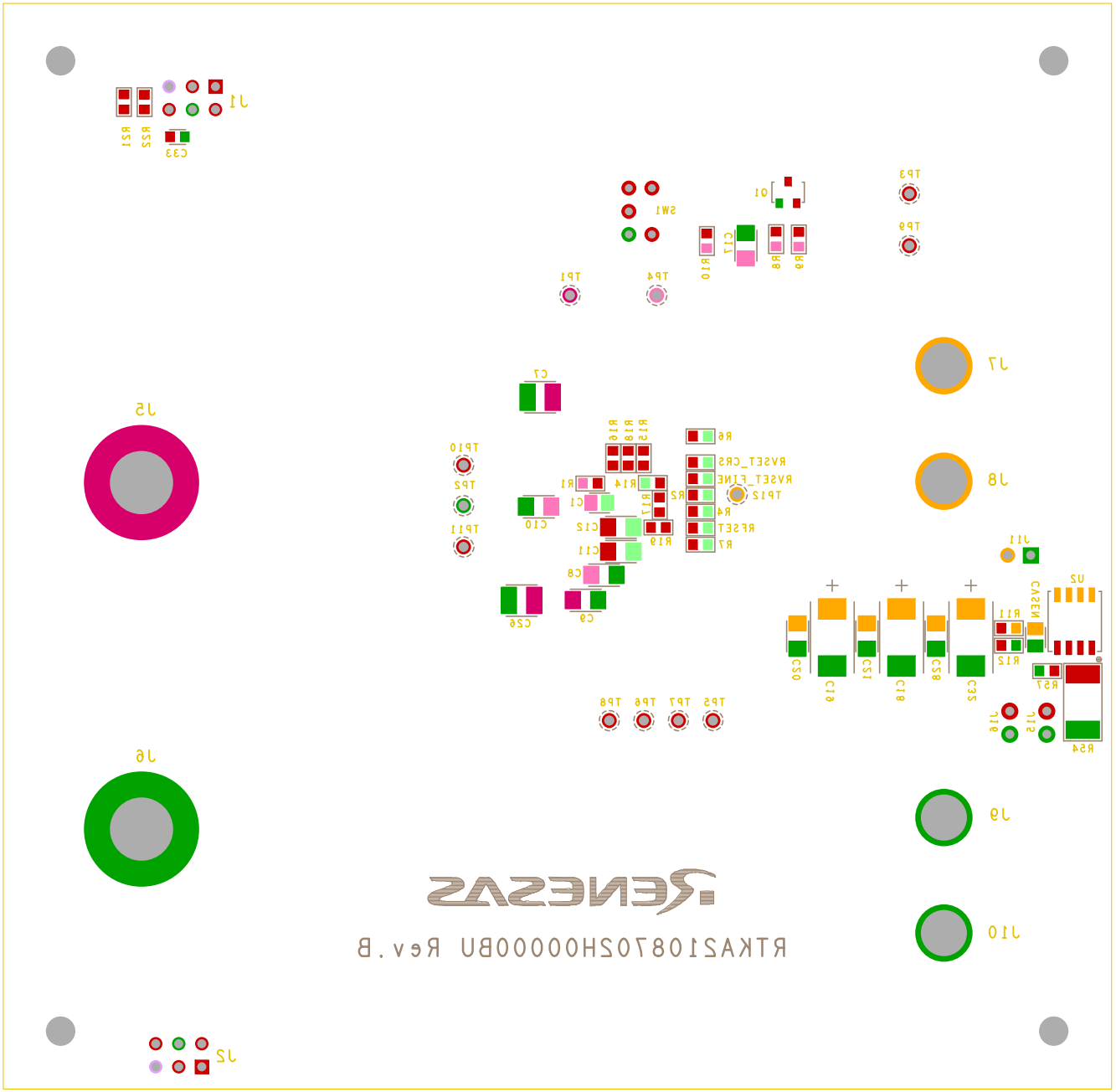


BOTTOM LAYER SOLDER SIDE

RENESAS CORPORATION

07-26-2018

# RTKA2108702H00000BU Rev.B




SILK SCREEN BOTTOM

RENESAS CORPORATION

07-26-2018

RTKA2108702H00000BU Rev.B

SILK SCREEN BOTTOM

RENESAS CORPORATION

07-26-2018

RTKA2108702SH00000BU Rev.B

MOTION COMPUTING ASSEMBLY DRAWING

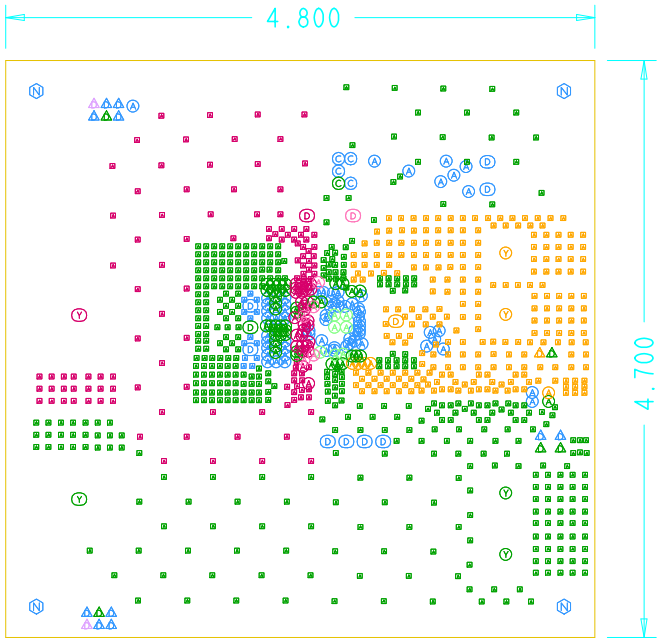
8105-09-02-07

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| | | | |

## PHYSICAL BOARD DIMENSIONS & LAYER STRUCTURE

.062" +/- 10%

| | |
|---|---|
| SILK TOP | silkt.art |
| MASK TOP | smaskt.art |
| COMPONENT | layer1.art |
| LAYER 2 | layer2.art |
| LAYER 3 | layer3.art |
| LAYER 4 | layer4.art |
| LAYER 5 | layer5.art |
| LAYER 6 | layer6.art |
| LAYER 7 | layer7.art |
| SOLDER | layer8.art |
| MASK BOTTOM | smaskb.art |
| SILK BOTTOM | silkb.art |




DRILL

| DRILL CHART: TOP to BOTTOM | | | |
|---|---|---|---|
| ALL UNITS ARE IN MILS | | | |
| FIGURE | SIZE | PLATED | QTY |
| Ⓐ | 10.0 | PLATED | 154 |
| ▣ | 12.0 | PLATED | 796 |
| Ⓒ | 35.0 | PLATED | 5 |
| ◬ | 41.0 | PLATED | 18 |
| Ⓓ | 45.0 | PLATED | 12 |
| Ⓨ | 200.0 | PLATED | 4 |
| Ⓨ | 275.0 | PLATED | 2 |
| Ⓝ | 128.0 | NON-PLATED | 4 |

NOTES:
1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 2 OZ COPPER.
4. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840, CLASS 2 (LPI) (BLUE MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED RTKA2108702H00000BU-B_IPC356.IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10. TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.
11. NETS GND AND GND_POWER ARE INTENTIONALLY SHORTED ON LAYER 2.
12. ALL 10 MIL VIAS (VIA18C10P) ARE TO BE FILLED WITH CONDUCTIVE MATERIAL AND PLATED OVER (VIPPO)

PART TO BE FREE OF BURRS AND SHARP EDGES
COMMERCIAL TOLERANCES APPLY TO STOCK SIZES
MANUFACTURING TOLERANCES PER 900002
WORKMANSHIP PER 900045
SCREW THREADS PER ANSI Y14.6
ABBREVIATIONS PER MIL-STD-12
LOGIC SYMBOLS PER IEEE STD 91
DIMENSIONING AND TOLERANCING PER ANSI Y14.5
ELECTRICAL AND ELECTRONIC DIAGRAM PER ANSI Y14.15
GRAPHIC SYMBOLS FOR ELECTRICAL AND ELECTRONIC DIAGRAM PER IEEE STD 315
ELECTRICAL AND ELECTRONIC REFERENCE DESIGNATIONS PER IEEE STD 200
WELDING SYMBOLS PER ANSI/AWS A2.4
INTERPRET DRAWING IAW DOD-STD-100

UNLESS OTHERWISE SPECIFIED
DIMENSION ARE IN INCHES
AND INCLUDE APPLIED FINISH
TOLERANCES
2 PLACE DIM. ± .---
3 PLACE DIM. ± .---
ANGLES ± ---

| | | |
|---|---|---|
| CONTRACT NO. | | |
| DWN BY 07/26/2018 Richard Kovacs | CHK BY | |
| ENGR | ELEC ENGR | |
| PROJ ENGR | MFG ENGR | |
| RELIABILITY | CONFIGURATION | |
| APPROVAL- DFTG | QA | |
| APPROVAL | SYS ENGR | |

PRINTED WIRING BOARD, EVAL-
RTKA2108702H00000BU

| SIZE | DWG NO. | REV |
|---|---|---|
| D | RTKA2109702H00000BU | B |

SCALE 2/1 SHEET 1 OF 1