

Product Advisory (PA)

Subject: Correction to the Renesas ISL70005SEH and ISL73005SEH Datasheets

Publication Date: 1/10/2020

Effective Date: 1/10/2020

Revision Description:

Initial Release

Description of Change:

This notice is to inform you of datasheet corrections as below;

1. UVLO pin association changed from B_VCC to L_VCC.
2. Power Supply Biasing updated.
3. B_COMP output voltage range in the Buck Error Amplifier Output updated.

Corrections are reflected in Appendix A of the notice.

Products Impacted by the change;

Renesas Part Number	Renesas Part Number	Renesas Part Number
ISL70005SEHDEMO1Z	ISL70005SEHF/SAMPLE	ISL70005SEHX/SAMPLE
ISL70005SEHEV2Z	ISL70005SEHVF	ISL73005SEHVF
ISL70005SEHF/PROTO	ISL70005SEHVX	ISL73005SEHVX

Reason for Change:

Change corrects the datasheet to reflect the actual product performance. Details regarding the change are contained within Appendix A, for an updated datasheet please contact your local sales or marketing representative.

Impact on fit, form, function, quality & reliability:

The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:

There have been no changes to the product, this is a documentation correction only. There will be no change in the external marking of the packaged products.

Qualification status: Not Applicable, correction only

Sample availability: 1/10/2020

Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@Renesas.COM	Europe: PCN-EU@Renesas.COM	Japan: PCN-JP@Renesas.COM	Asia Pac: PCN-APAC@Renesas.COM

Appendix A:

- UVLO pin association changed from B_VCC to L_VCC.

FROM:

2.4.1 Buck Regulator Electrical Specifications

Unless otherwise noted, B_VINx = B_VCC = 3V to 5.5V; B_GND = B_PGNDx = 0V; B_EN = 2.0V; B_SYNC = B_LXx = Open Circuit; B_PG is pulled up to B_VCC with a 3kΩ resistor; VREF is bypassed to L_GND with a 22nF capacitor; B_SS is bypassed to B_GNDx with a 220nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. Boldface limits apply across the operating temperature range, -55°C to +125°C, without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrads(Si)/s.

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Operating Supply Current - Switching	B_EN = 2V, 100kHz switching, B_LXx floating		10	15	mA
Shutdown Supply Current - Idle	B_EN = GND		0.6	3.0	mA
Power-On Reset					
B_VCC Internal UVLO Rising Threshold		2.6	2.8	2.95	V
B_VCC Internal UVLO Falling Threshold		2.45		2.80	V
B_VCC Internal UVLO Hysteresis		75	175	420	mV

TO:

2.4.2 LDO Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: C_{OUT} = 150μF tantalum, T_A = T_J = +25°C, I_L = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See ["Applications Information" on page 31](#) and [TB379](#). Boldface limits apply across the operating temperature range, -55°C to +125°C without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrads(Si)/s. Pulse load techniques used by ATE to ensure T_J = T_A.

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Characteristics					
L_VIN Voltage Range	MIN ensured by L_VIN dropout testing	0.775		L_VCC	V
L_OUT Voltage Range	MIN ensured by L_VIN dropout testing; MAX ensured by L_VCC dropout testing; L_EA+ = 0.600V	0.6		L_VCC - 1.5	V
VREF Voltage		0.591		0.609	V
Power-On Reset					
L_VCC Internal UVLO Rising Threshold		2.6	2.8	2.95	V
L_VCC Internal UVLO Falling Threshold		2.45		2.80	V
L_VCC Internal UVLO Hysteresis		75	175	420	mV

2. Power Supply Biasing updated

FROM:

5.1 Power Supply Biasing

It is necessary in application to have B_VCC, L_VCC, and B_VIN biased to the same RMS DC voltage. A low pass filter can be placed on B_VIN to B_VCC and L_VCC to provide noise filtering on the analog supplies. A 1Ω resistor and 0.1μF capacitor on B_VCC = L_VCC to B_GND = L_GND is recommended. The B_VCC and L_VCC have input UVLO threshold as specified in the electrical specification table with a typical rising threshold of 2.8V. Below UVLO both the B_LXx and L_OUT output is high impedance. B_VIN is the input to the buck synchronous power MOSFETs and L_VIN is the input to the LDO upper NMOS FET. The recommended input voltage range of B_VCC, L_VCC, and B_VIN is 3V to 5.5V. The recommended input voltage range of L_VIN is from 1.0V to L_VCC. There are no power sequencing requirements for the B_VCC = L_VCC = B_VIN and L_VIN power supplies.

TO:

5.1 Power Supply Biasing

It is necessary in application to have B_VCC, L_VCC, and B_VIN biased to the same RMS DC voltage. A low pass filter can be placed on B_VIN to B_VCC and L_VCC to provide noise filtering on the analog supplies. A 1Ω resistor and 0.1μF capacitor on B_VCC = L_VCC to B_GND = L_GND is recommended. The L_VCC input UVLO threshold is specified in the electrical specification table with a typical rising threshold of 2.8V. Below UVLO both the B_LXx and L_OUT output is high impedance. B_VIN is the input to the buck synchronous power MOSFETs and L_VIN is the input to the LDO upper NMOS FET. The recommended input voltage range of B_VCC, L_VCC, and B_VIN is 3V to 5.5V. The recommended input voltage range of L_VIN is from 1.0V to L_VCC. There are no power sequencing requirements for the B_VCC = L_VCC = B_VIN and L_VIN power supplies.

3. B_COMP output voltage range in the Buck Error Amplifier Output updated.

FROM:

4.1.7 Buck Error Amplifier Output

The B_COMP pin is the output of the error amplifier. The voltage on B_COMP determines the duty cycle at B_LXx. For voltage mode control, a Type III compensation network must be connected between B_FB and B_COMP to stabilize the feedback loop. See ["Buck Feedback Compensation Design" on page 38](#) for the design of the Type III compensator. The B_COMP pin analog range is from 100mV to 1.4V that correlates to the B_LXx duty cycle from minimum on-time to minimum off-time.

TO:

4.1.7 Buck Error Amplifier Output

The B_COMP pin is the output of the error amplifier. The voltage on B_COMP determines the duty cycle at B_LXx. For voltage mode control, a Type III compensation network must be connected between B_FB and B_COMP to stabilize the feedback loop. See ["Buck Feedback Compensation Design" on page 38](#) for the design of the Type III compensator. The B_COMP pin analog range is from 100mV to 0.4*B_VCC that correlates to the B_LXx duty cycle from minimum on-time to minimum off-time.