

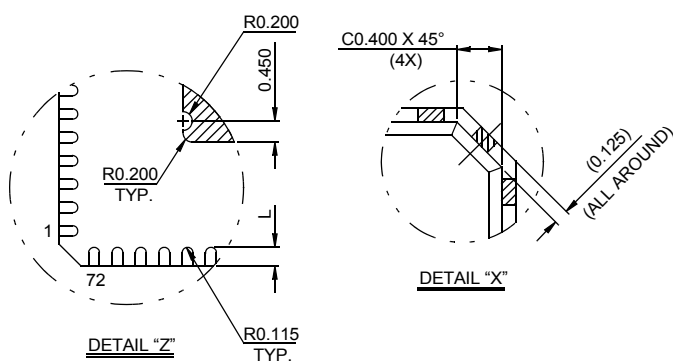
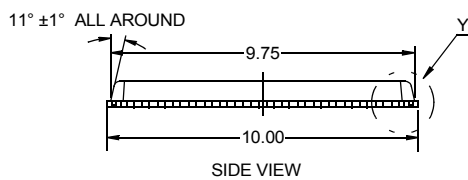
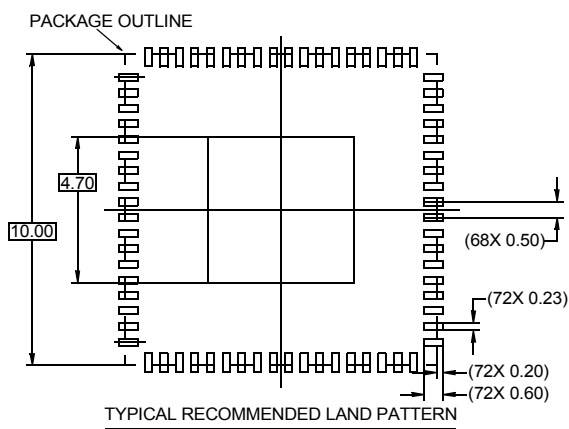
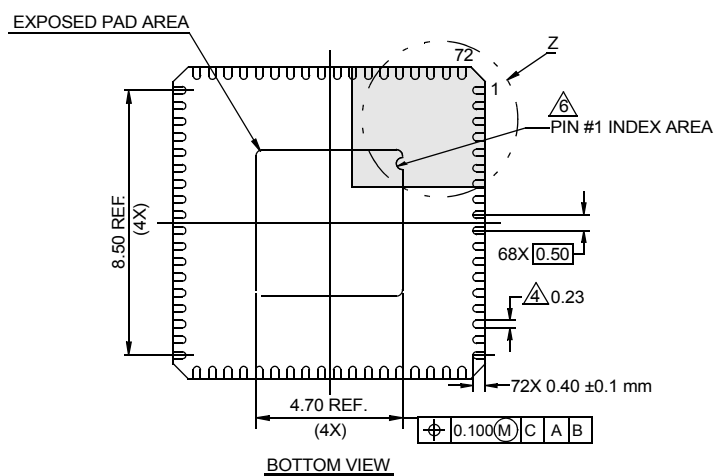
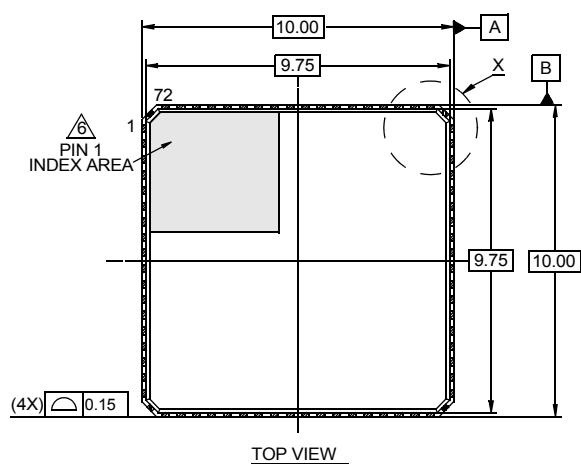
# Plastic Packages for Integrated Circuits

## Package Outline Drawing

### L72.10x10B

#### 72 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

Rev 0, 5/07



#### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to JESD-MO220.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$ ;  
body tolerance:  $\pm 0.1\text{mm}$
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

