ISL70321SEH, ISL73321SEH

Combined Neutron and TID Test Results of the Radiation Hardened Quad Power Supply Sequencers

Introduction

This report summarizes the results of testing of the ISL70321SEH radiation tolerant quad power supply sequencer after 1MeV equivalent neutron exposure followed by 100krad(Si) high dose rate (HDR) total ionizing dose (TID) exposure. The test was conducted to determine the sensitivity of the part to the combination of displacement damage (DD) caused by neutron or proton environments and HDR total ionizing dose. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2. The TID levels were 30k, 50k, and 100krad(Si). These results also apply to the ISL73321SEH.

Product Description

The ISL7x321SEH is a radiation tolerant and SEE-mitigated power supply sequencer designed to control Point-of-Load (POL) regulators with enable pins. Up to four power supplies can be sequenced by a single device, or multiple devices can be easily cascaded to sequence an unlimited number of power supplies for dense RF applications in EW, radar, and SIGINT platforms. The sequencer requires only two feedback resistors per power supply and a single resistor to set the rising and falling delay. The device features precision input comparators with an input threshold voltage of 600mV ±1.5% for the highest possible accuracy when monitoring the power supply voltages.

The ISL70321SEH is offered in an 18-lead 10mm×12mm CDFP package or die form and is fully specified across the military ambient temperature range of -55°C to +125°C. With minimal external component count, precision voltage monitoring, and SET mitigation, the ISL70321SEH is the ideal choice to control many of today's spaceborne power systems.

A typical application schematic for the ISL7x321SEH is shown in Figure 1.

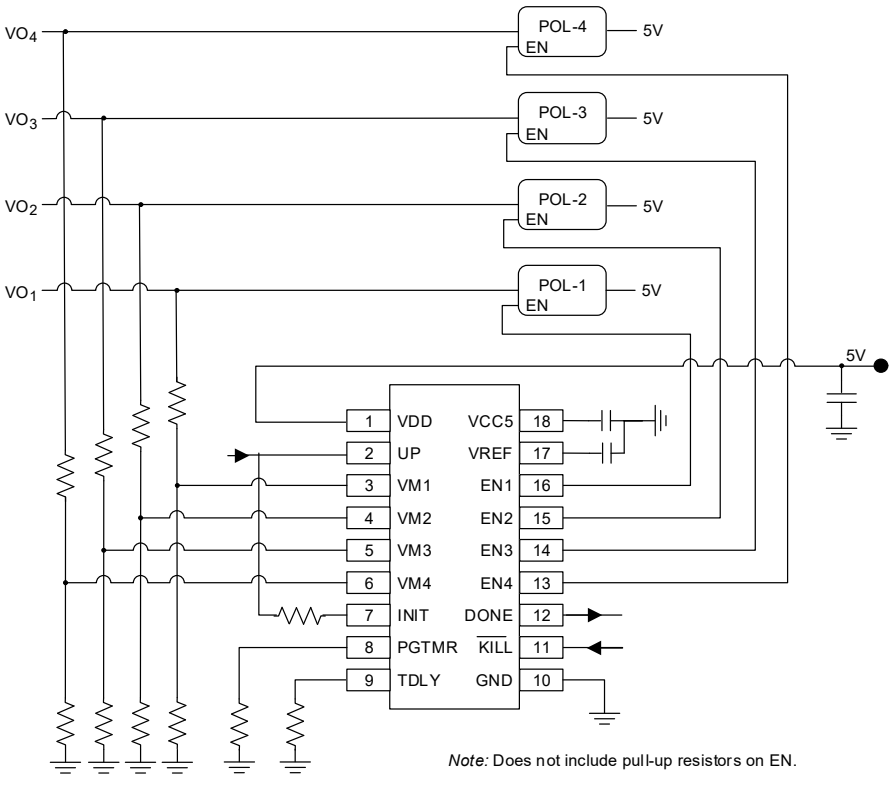

Figure 1. ISL7x321SEH Typical Application Schematic

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1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on August 31, 2021, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5×10^{11}n/cm^2, 2×10^{12}n/cm^2, and 1×10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

Total dose testing was performed at 77.2rad(Si)/s using a Gammacell 220 industry standard irradiator in the Renesas facility in Palm Bay, Florida. The irradiator uses a PbAl spectrum hardening filter to shield the test board and devices under test against low-energy secondary gamma radiation. All samples were irradiated under bias. No anneal was performed.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

Figure 2 shows the configuration used for TID irradiation.

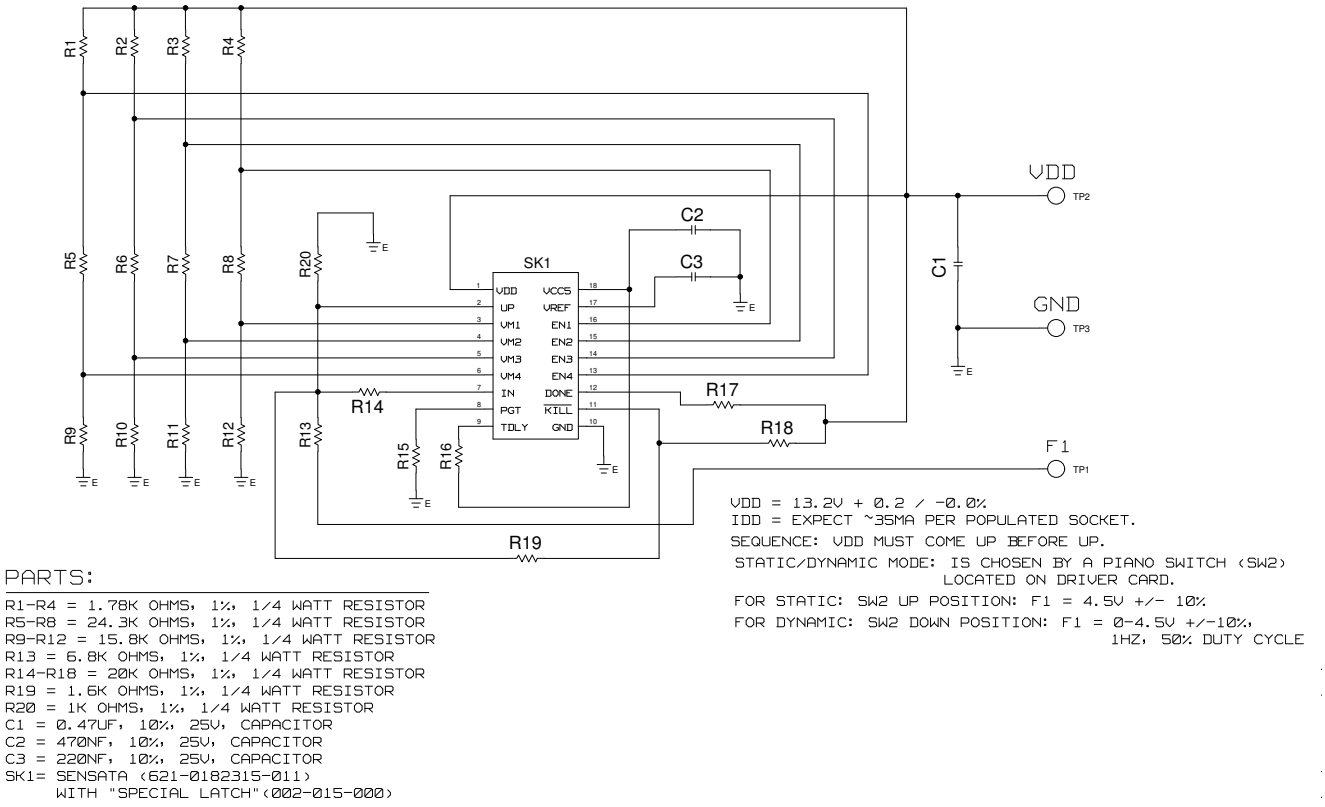

Figure 2. ISL7x321SEH TID Bias Schematic

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell, indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. ISL7x321SEH Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm^2-s)[1][2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#62106-A	5.00E+11	10	617	8.10E+08	70	5.38E+11
CRF#62106-B	2.00E+12	100	247	8.10E+09	281	2.05E+12
CRF#62106-C	1.00E+13	1000	123	8.10E+10	1401	1.14E+13

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell* (6/18/02). Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41 ±5.3% krad(Si)/hr as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

The fifteen ISL7x321SEH samples were drawn from Lot 5STWBEH. Samples were packaged in the standard hermetic 18 lead ceramic (CDFP) production package. Samples were processed through burn-in before irradiation and screened to the SMD limits at room, low, and high temperatures before the neutron testing.

Neutron testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. As shown in Table 2, the experimental matrix consisted of five samples to be irradiated at $5\times10^{11}n/cm^2$, five at $2\times10^{12}n/cm^2$, and five at $1\times10^{13}n/cm^2$. Table 1 shows the actual levels achieved, which were all within 10% of the target fluences, at $5.4\times10^{11}n/cm^2$, $2.1\times10^{12}n/cm^2$, and $1.1\times10^{12}n/cm^2$. Two control units were used.

Total dose irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. All fifteen samples were irradiated at HDR under bias with down-points at 30k, 50k, and 100krad(Si). Two control units were used.

2. Results

Combined neutron and HDR total ionizing dose testing of the ISL7x321SEH is complete, and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; the damage from neutron testing was not cumulative. Following neutron testing, each set of samples underwent HDR TID testing in which the damage was cumulative.

2.1 Attributes Data

Neutron plus total dose testing of the ISL7x321SEH is complete. All units passed all parameters to the post-irradiation SMD limits. Table 2 summarizes the results.

Table 2. ISL7x321SEH Attributes Data

1MeV Fluence Neutrons (n/cm^2)		TID (krad(Si))	Sample Size	Pass[1]	Fail	Notes
Planned	Actual					
5×10^{11}	5.38×10^{11}	30	5	5	0	All passed
		50				
		100				
2×10^{12}	2.05×10^{12}	30	5	5	0	All passed
		50				
		100				
1×10^{13}	1.14×10^{13}	30	5	5	0	All passed
		50				
		100				

1. A Pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figure 3 through Figure 19 show data for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron and total dose irradiation. Each set of samples was irradiated to a different neutron fluence and plotted as a distinct line. Each line only has markers at the radiation levels to which the corresponding set of samples was exposed. For example, the line representing a parameter of the set of samples irradiated to $5\times10^{11}n/cm^2$ has a marker at $5\times10^{11}n/cm^2$ but not at $2\times10^{12}n/cm^2$ or $1\times10^{13}n/cm^2$. All lines have makers at the pre-irradiation level and the total dose levels of 30krad(Si), 50krad(Si), and 100krad(Si).

While the applicable electrical limits taken from the SMD are also shown, these limits are provided for guidance only as the ISL7x321SEH is not specified for the neutron environment. All samples passed the post-irradiation SMD limits after neutron exposures up to $1.14\times10^{13}n/cm^2$ and HDR irradiation through 100krad(Si).

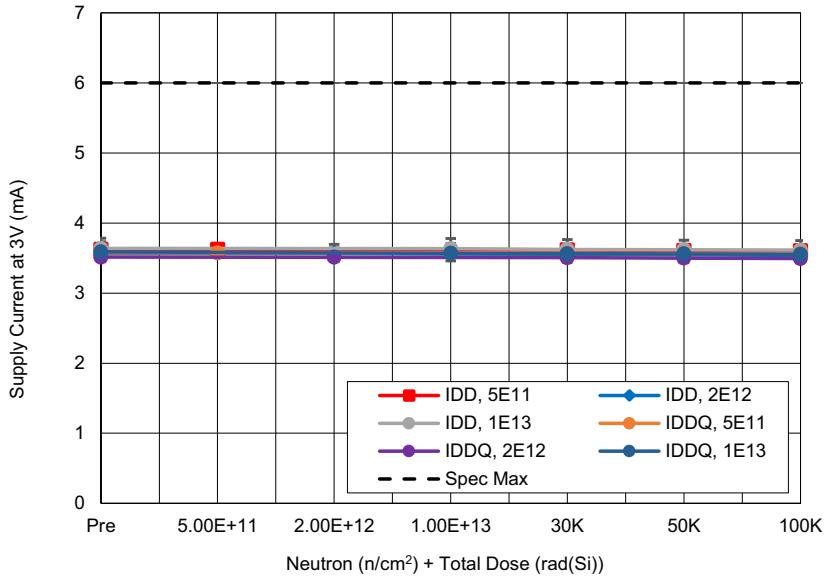

Figure 3. ISL7x321SEH average quiescent (I_{DDQ}) and operating (I_{DD}) supply current at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 6mA maximum.

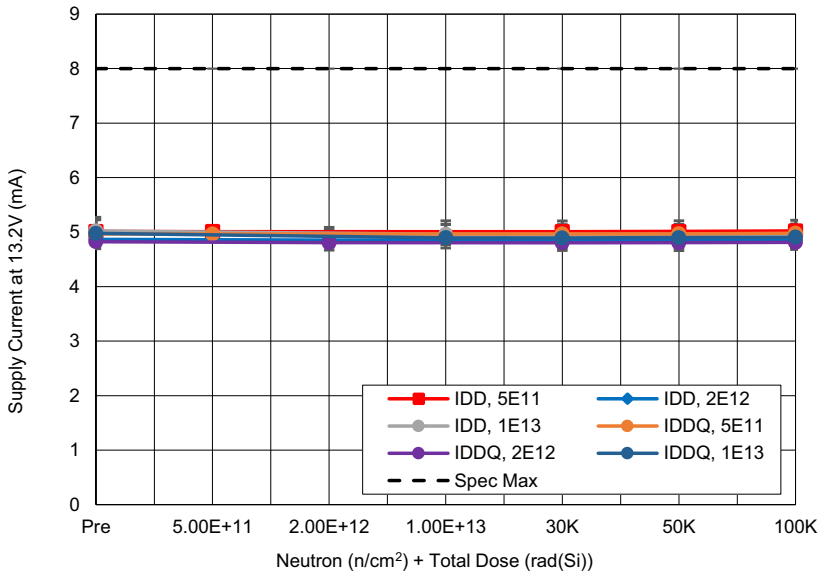

Figure 4. ISL7x321SEH average quiescent (I_{DDQ}) and operating (I_{DD}) supply current at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 8mA maximum.

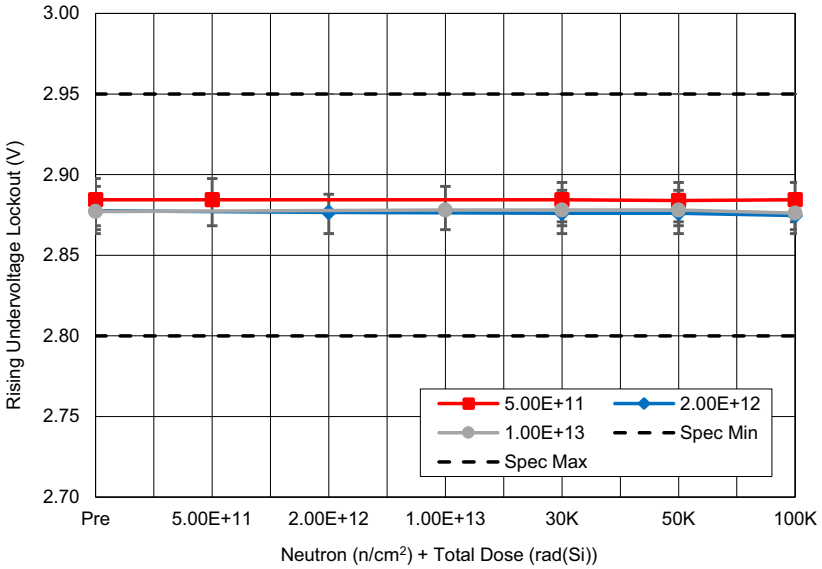

Figure 5. ISL7x321SEH average rising undervoltage lockout (UVLO) voltage following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 2.80V minimum and 2.95V maximum.

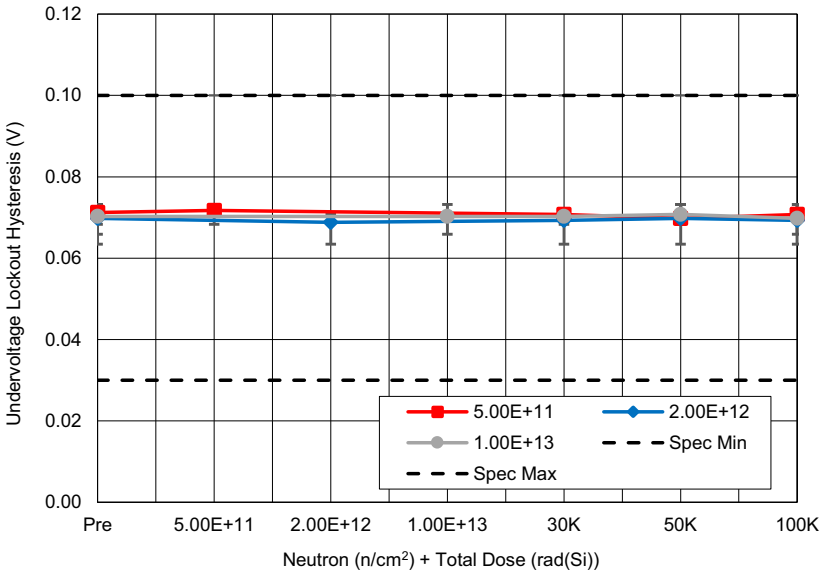

Figure 6. ISL7x321SEH average undervoltage lockout hysteresis (UVLO_HYS) voltage following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.03V minimum and 0.1V maximum.

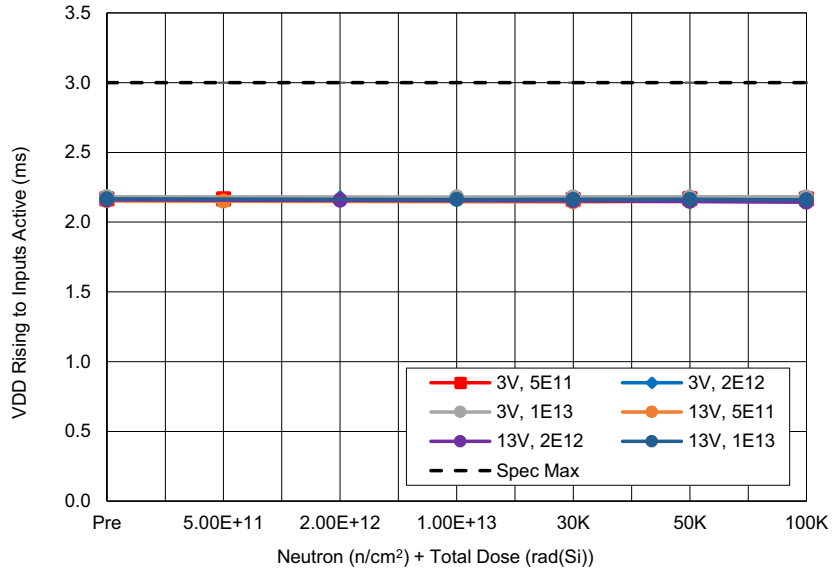

Figure 7. ISL7x321SEH average time from VDD rising to inputs active (t_{VDD_INPUT}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 3ms maximum.

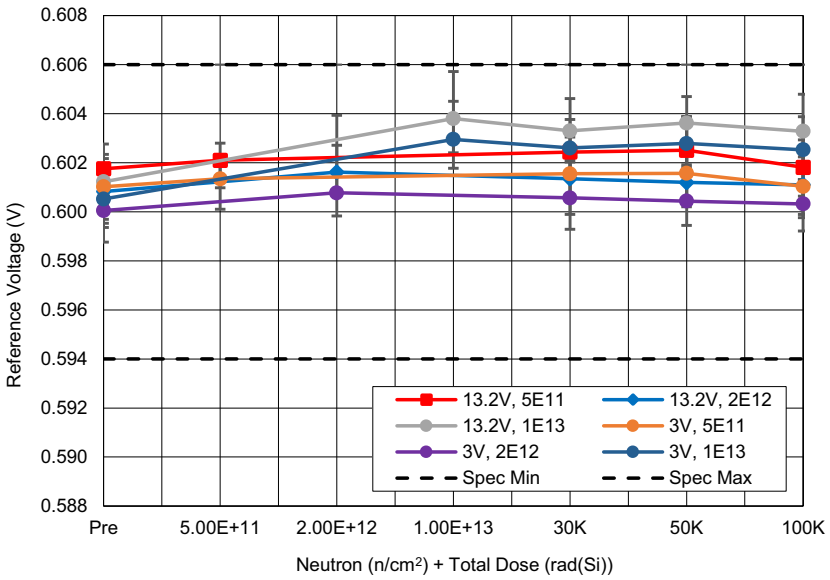

Figure 8. ISL7x321SEH average reference voltage (V_{REF}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.594V minimum and 0.606V maximum.

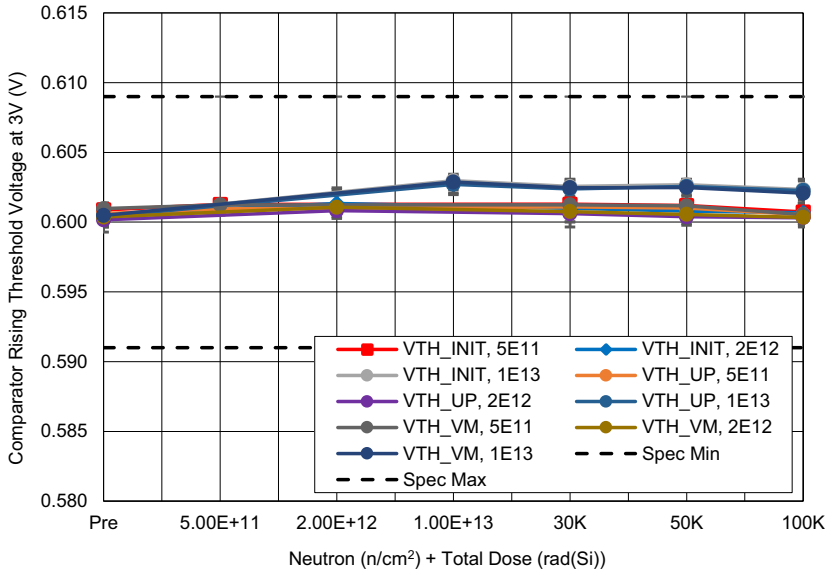

Figure 9. ISL7x321SEH average comparator rising threshold voltage (V_{TH}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.591V minimum and 0.609V maximum.

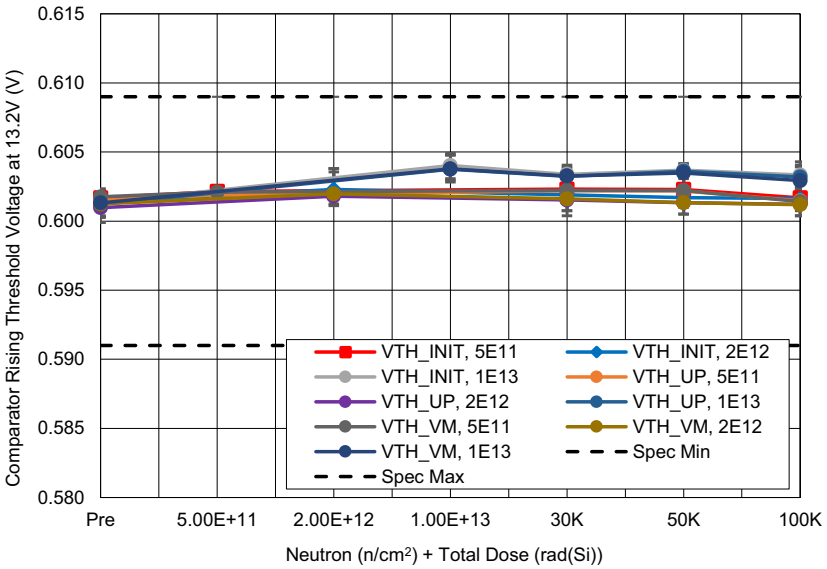

Figure 10. ISL7x321SEH average comparator rising threshold voltage (V_{TH}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.591V minimum and 0.609V maximum.

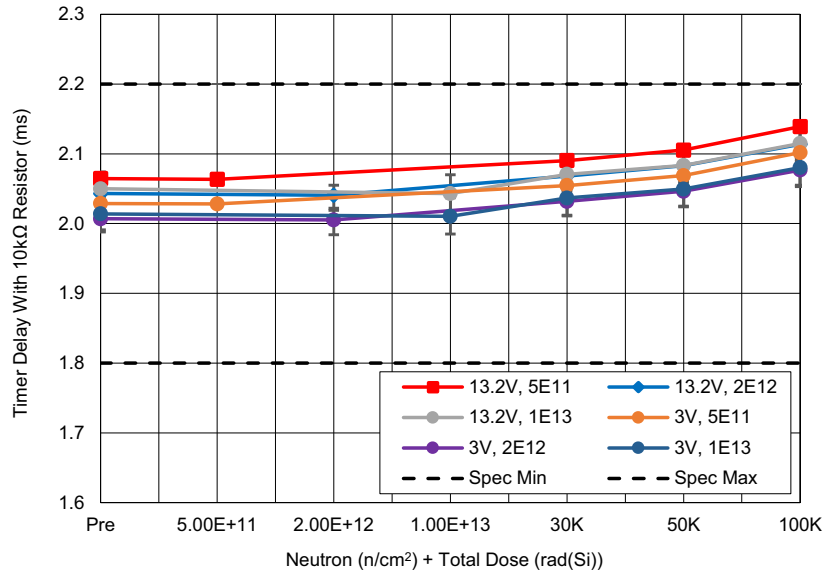

Figure 11. ISL7x321SEH average timer delay with 10KΩ resistor (t_{DLY_10}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 1.8ms minimum and 2.2ms maximum.

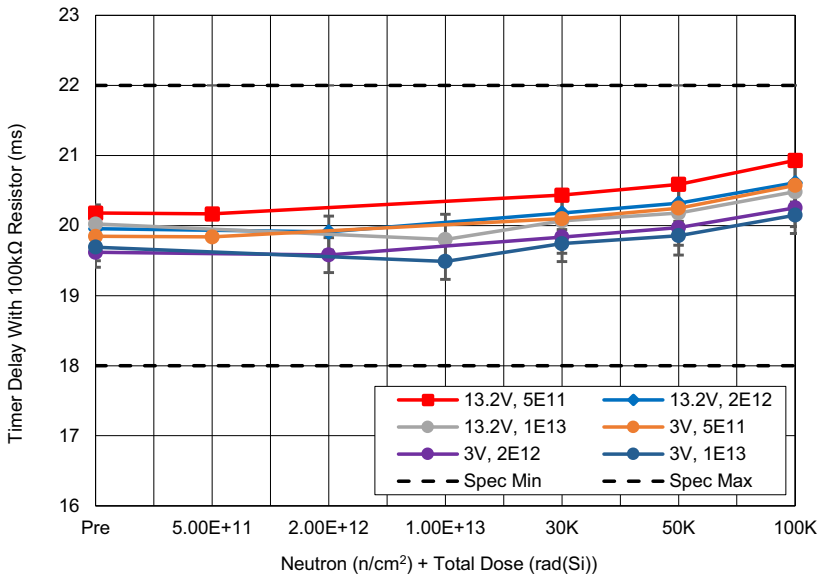

Figure 12. ISL7x321SEH average timer delay with 100KΩ resistor (t_{DLY_100}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 18ms minimum and 22ms maximum.

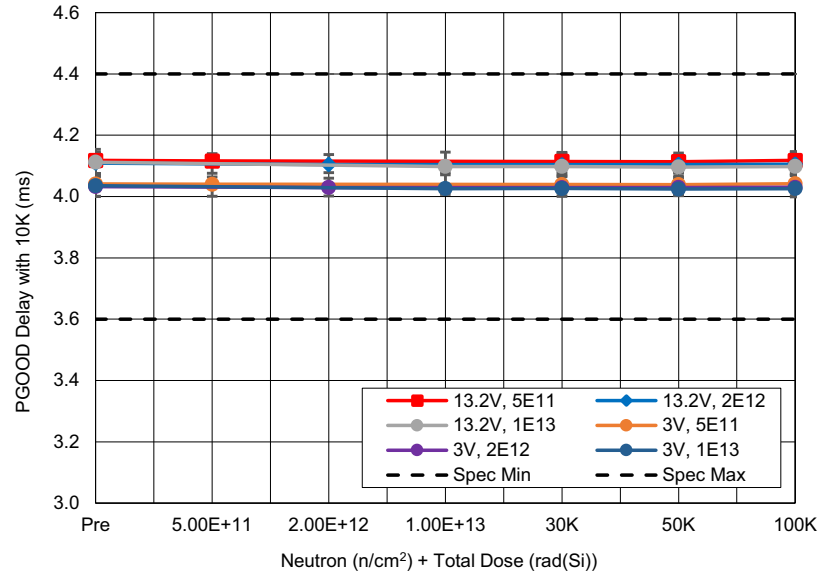

Figure 13. ISL7x321SEH average Power Good delay with 10KΩ resistor (t_{PG_10}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 3.6ms minimum and 4.4ms maximum.

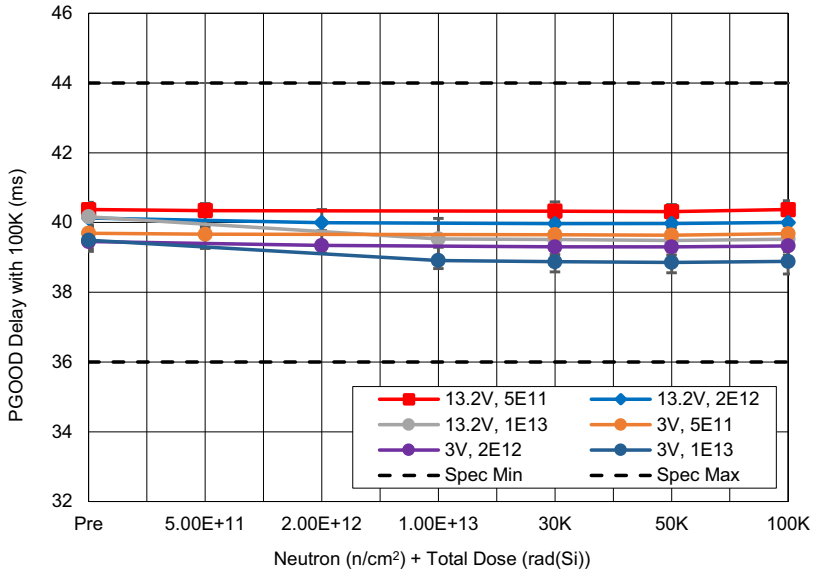

Figure 14. ISL7x321SEH average Power Good delay with 100KΩ resistor (t_{PG_100}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 36ms minimum and 44ms maximum.

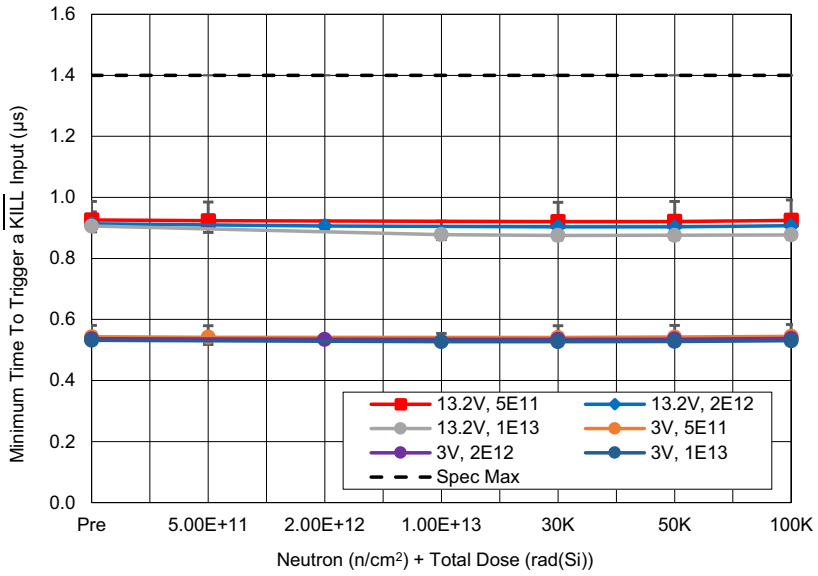

Figure 15. ISL7x321SEH average minimum time to trigger a $\overline{\text{KILL}}$ input (t_{KON}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.4µs maximum.

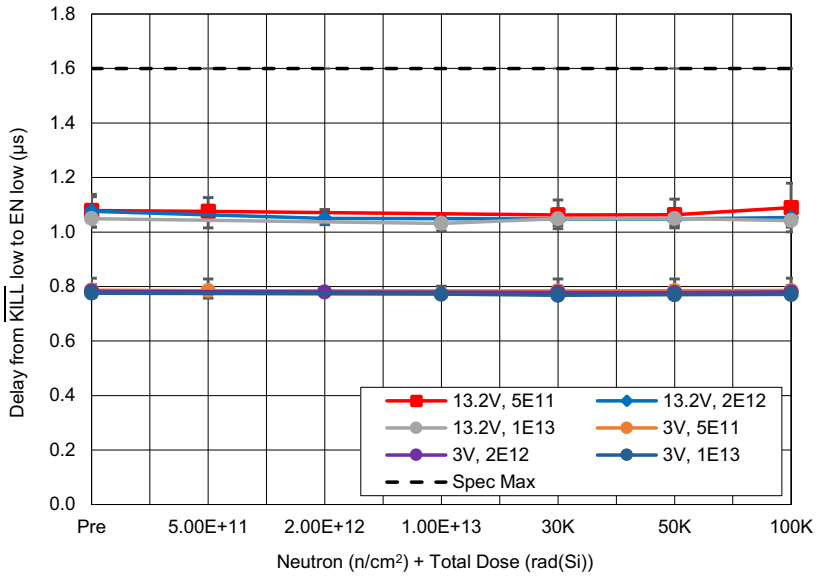

Figure 16. ISL7x321SEH average Delay from $\overline{KILL}$ low to EN1 - EN4 low (t_{KDLY}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.6µs maximum.

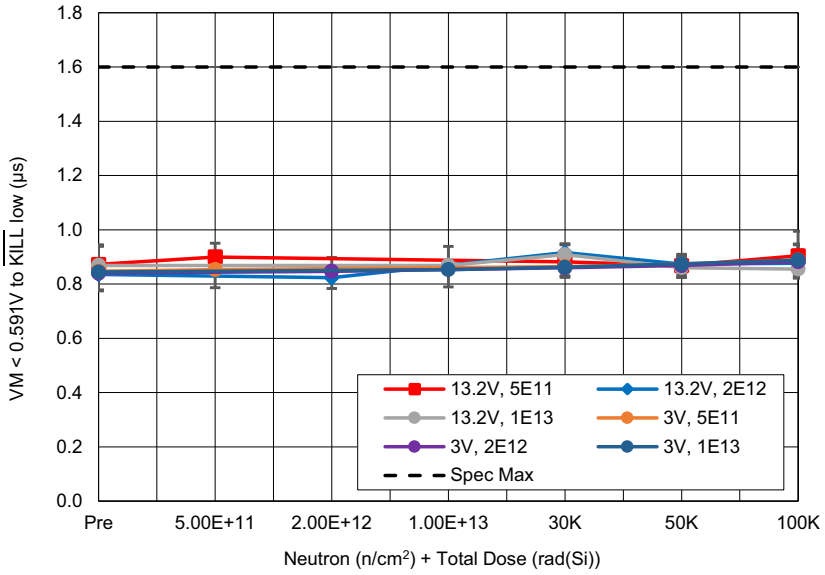

Figure 17. ISL7x321SEH delay from VM < 0.591V to $\overline{KILL}$ low (t_{KRESP}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.6µs maximum.

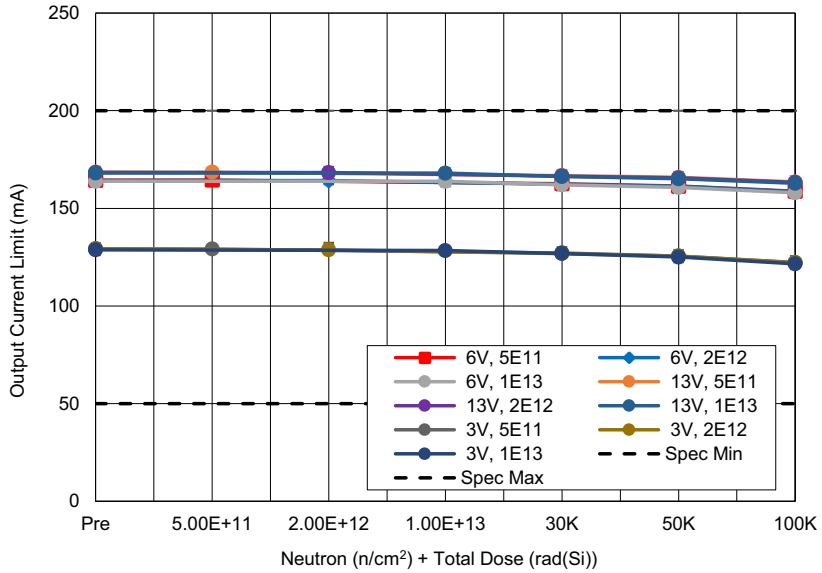

Figure 18. ISL7x321SEH average output current limit on VCC5 (I_{LIM}) at V_{DD} = 3V, 6V and 13.2V, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 50mA minimum and 200mA maximum.

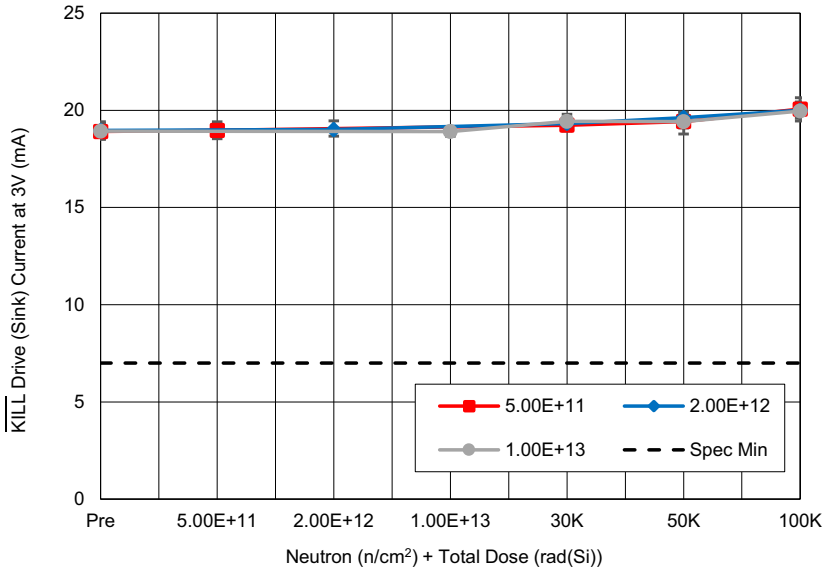

Figure 19. ISL7x321SEH average $\overline{\text{KILL}}$ Drive (Sink) Current (I_{KS}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 7mA minimum.

3. Discussion and Conclusion

This report summarizes the results of 1MeV equivalent neutron testing followed by HDR Total Ionizing Dose (TID) testing of the ISL7x321SEH radiation tolerant quad power supply sequencer. Parts were tested at fluences of 5.4×10^{11}n/cm^2, 2.1×10^{12}n/cm^2, and 1.1×10^{13}n/cm^2. Following neutron irradiation and testing, each set of samples underwent HDR TID testing. Each set of samples was irradiated under bias to 100krad(Si) with downpoints at 30krad(Si), 50krad(Si), and 100krad(Si). No anneal was performed.

The results of key parameters before and after irradiation to each level are plotted in Figure 3 through Figure 19. The plots show the mean of each parameter as a function of neutron and total dose irradiation, with error bars representing the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD. However, these limits are provided for guidance only as the ISL7x321SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all exposures up to and including 1.1×10^{13}n/cm^2.

4. Revision History

Revision	Date	Description
1.00	Jul 17, 2023	Initial release.

A. Appendix

A.1 Reported Parameters

The table below lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 19. All limits are taken from the ISL7x321SEH SMD.

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	3V Quiescent Supply Current	I_{DDQ_3}	UP and INIT = 0.5V	-	6	mA
	3V Operating Supply Current	I_{DD_3}	UP and INIT = 0.7V with EN tied to VM to 5V			
4	13.2V Quiescent Supply Current	I_{DDQ_13}	UP and INIT = 0.5V	-	8	mA
	13.2V Operating Supply Current	I_{DD_13}	UP and INIT = 0.7V with EN tied to VM to 5V			
5	Rising Undervoltage Lockout Level	UVLO	V_{DD} rising to V_{REF} rising, VCC5 = 45mA	2.8	2.95	V
6	Undervoltage Lockout Hysteresis	UVLO_hys	UVLO - V_{DD} falling to V_{REF} turn-off	0.03	0.1	V
7	Time from V_{DD} to Inputs being Active	t_{VDD_INPUT}	V_{DD} rising to inputs active, t_{DLY} timer disabled	-	3	ms
8	Reference Voltage	V_{REF}	-	0.594	0.606	V
9	Comparator Rising Threshold Voltage at 3V	V_{TH}	V_{DD} = 3V	0.591	0.609	V
10	Comparator Rising Threshold Voltage at 13.2V	V_{TH}	V_{DD} = 13.2V	0.591	0.609	V
11	10kΩ Delay Timer	t_{DLY_10}	RSET = 10K, V_{DD} = 3V, 13.2V	1.8	2.2	ms
12	100kΩ Delay Timer	t_{DLY_100}	RSET = 100K, V_{DD} = 3V, 13.2V	18	22	ms
13	10kΩ Power-Good Timer	t_{PG_10}	RSET = 10K, V_{DD} = 3V, 13.2V	3.6	4.4	ms
14	100kΩ Power-Good Timer	t_{PG_100}	RSET = 100K, V_{DD} = 3V, 13.2V	36	44	ms
15	Minimum Time to Trigger a $\overline{KILL}$ Input	t_{KON}	V_{DD} = 3V and 13.2V	-	1.4	µs
16	Delay from $\overline{KILL}$ low to EN1 - EN4 Low	t_{KDLY}	V_{DD} = 3V and 13.2V	-	1.6	µs
17	VM < 0.591V to $\overline{KILL}$ Low	t_{KRESP}	V_{DD} = 3V and 13.2V	-	1.6	µs
18	Current Limit on VCC5	I_{LIM}	V_{DD} = 3V, 6V and 13.2V	50	200	mA
19	Drive (Sink) Current	I_{KS}	V_{DD} = 3V, V_{KILL} = 0.4V	7	-	mA

A.2 Related Information

For a full list of related documents, visit our website:

- ISL70321SEH, ISL73321SEH device pages
- MIL-STD-883 test method 1017
- MIL-STD-883 Test Method 1019

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