

ISL73321SEH

Total Dose Testing

TR054
Rev.0.00
Sep 14, 2017**Introduction**

This report documents the results of Low Dose Rate (LDR) total dose testing and subsequent anneals of the ISL73321SEH radiation hardened quad power supply sequencer. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias sensitivity. Parts were irradiated under bias and with all pins grounded. The ISL73321SEH is acceptance tested on a wafer by wafer basis to 75 krad(Si) at LDR (0.01 rad(Si)/s).

Product Description

The ISL73321SEH is a radiation hardened and SEE mitigated power supply sequencer designed to control Point-of-Load (POL) regulators with enable pins. Up to four power supplies can be sequenced by a single device or multiple devices can be easily cascaded to sequence an unlimited number of power supplies for dense RF applications in EW, radar, and SIGINT platforms. The sequencer requires only two feedback resistors per power supply and a single resistor to set the rising and falling delay. The device features precision input comparators with an input threshold voltage of 600mV \pm 1.5% for the highest possible accuracy when monitoring the power supply voltages.

The ISL73321SEH is offered in an 18 Ld 10mmx12mm CDFP package or in die form and is fully specified across the military ambient temperature range of -55°C to +125°C. With minimal external component count, precision voltage monitoring and SET mitigation, the ISL73321SEH is the ideal choice to control many of today's spaceborne power systems.

Related Literature

- For a full list of related documents, visit our website
 - [ISL73321SEH](#) product page

1. Test Description

1.1 Irradiation Facilities

Total dose irradiation was performed at 0.01 rad(Si)/s using the Hopewell Designs N40 panoramic ^{60}Co irradiator in the Palm Bay, FL Intersil facility. Biased irradiation and annealing were performed using the bias configuration listed in [“Appendix” on page 13](#) at 100°C for 168 hours using a small temperature chamber.

1.2 Test Fixturing

[“Appendix” on page 13](#) shows the configuration used for biased irradiation.

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging at each downpoint.

1.4 Experimental Matrix

Total dose irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of four samples irradiated under bias and four samples irradiated with all pins grounded. Three control units were used to ensure high-quality data. The ISL73321SEH samples were drawn from preproduction wafer lot 5STWB. All samples were packaged in the hermetic 18-pin solder-sealed production flatpack (package code K18.B). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints were zero, 10, 30, 50, and 75 krad(Si). The irradiations were followed by a high temperature anneal at 100°C under bias.

2. Test Results

2.1 Attributes Data

Part	Dose Rate Rad(Si)/s	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
ISL73321SEH	0.01	Appendix 1	4	Pre-irradiation	4	
				10 krad(Si)	4	0
				30 krad(Si)	4	0
				50 krad(Si)	4	0
				75 krad(Si)	4	0
				Anneal	4	0
ISL73321SEH	0.01	Grounded	4	Pre-irradiation	4	
				10 krad(Si)	4	0
				30 krad(Si)	4	0
				50 krad(Si)	4	0
				75 krad(Si)	4	0
				Anneal	4	0

Note:

1. Pass indicates a sample that passes all SMD Group A limits.

2.2 Critical Parameters

The table below lists 13 critical parameters that are indicative of part performance. These parameters are discussed in detail below and are plotted in [Figures 1](#) through [13](#).

Figure	Parameter	Limit, low	Limit, high	Units	Notes
1	Quiescent power supply current	-	6	mA	3V supply
	Quiescent power supply current	-	8	mA	13.2V supply
2	Average comparator rising threshold voltage	0.591	0.609	V	3V supply
3	Average comparator rising threshold voltage	0.591	0.609	V	13.2V supply
4	Average comparator input leakage current	-50	50	nA	3V supply
5	Average comparator input leakage current	-50	50	nA	13.2V supply
6	Average comparator hysteresis current	-28	-20	μA	3V supply
7	Average comparator hysteresis current	-28	-20	μA	13.2V supply
8	Delay timer delay	1.8	2.2	ms	RSET = 10K, 13.2V supply
9	Delay timer delay	18	22	ms	RSET = 100K, 13.2V supply
10	Power Good (PGOOD) timer delay	3.6	4.4	ms	RSET = 10K, 13.2V supply
11	Power Good (PGOOD) timer delay	36	44	ms	RSET = 100K, 13.2V supply
12	Rising undervoltage lockout level	2.8	2.95	V	13.2V supply
13	Undervoltage lockout hysteresis	30	100	mV	13.2V supply

Note:

2. All limits are SMD Group A values.

[Figure 1](#) plots the quiescent power supply current for the 3V supply and 13.2V supply cases.

[Figures 2](#) and [3](#) plot the average comparator rising threshold voltage for the six comparator-type inputs. We also show minimum/maximum error bars. The six comparator-type inputs are:

- The Sequence INITIATE input (pin 7), which is connected to the UP pin when the device is in a standalone application or is the first in a cascade configuration. For the subsequent parts in a cascade configuration, the Sequence INITIATE input is driven by the DONE output pin of the previous ISL73321SEH.
- The UP input (pin 2), which commands the ISL73321SEH to start the power-up sequence.
- The VM1 through VM4 inputs (pins 3, 4, 5, and 6), which are voltage monitor inputs indicating the sequenced power supply has reached the desired power-on voltage or has reached the desired power-off voltage.

[Figures 4](#) and [5](#) plot the average comparator input leakage current for the above six comparator-type inputs. We also show minimum/maximum error bars.

[Figures 6](#) and [7](#) plot the average comparator hysteresis current for the above six comparator-type inputs. We also show minimum/maximum error bars.

[Figures 8](#) and [9](#) plot the rising and falling time delay between a supply ON/OFF signal (UP or VMx) and the enabling or disabling of the next power supply in the sequence. This delay is set by an external 10 k Ω to 100 k Ω resistor. [Figure 8](#) shows the 10 k Ω case (2ms delay) and [Figure 9](#) shows the 100k Ω case (20ms delay).

[Figures 10](#) and [11](#) plot the ramp time for a power supply to reach a power-good state after being enabled with ENx. A 10 k Ω to 100 k Ω resistor connected between PGTMR to GND sets the Power-Good (PGOOD) timer delay.

[Figure 10](#) shows the 10 k Ω case (4ms) and [Figure 11](#) shows the 100k Ω case (40ms).

[Figure 12](#) plots the rising undervoltage lockout (UVLO) level. The UVLO function monitors the output voltage (VCC5) of the internal linear regulator. When this voltage rises above ~2.8V the ISL73321SEH initializes by turning on the 600mV bandgap reference voltage and the internal PGOOD and delay timer oscillators. If the voltage on VCC5 falls below 2.8V, the UVLO shuts off both oscillators and the band-gap reference. It also holds the open-drain ENx outputs low until VCC5 drops below 1.2V.

Finally [Figure 13](#) plots the UVLO hysteresis. This circuit allows the level of the sequenced power supply output voltage to precisely gate the turn-on/turn-off of the next regulator. The internal IHYS current source has a typical value of 24 μ A and adds hysteresis between the turn-on and turn-off levels.

Refer to the ISL73321SEH data sheet for further details.

2.3 Critical Parameter Variables Data

The plots in [Figures 1](#) through [13](#) show the total dose response of the critical parameters outlined in “[Critical Parameters](#)” on [page 3](#). The input comparator threshold, input leakage current and hysteresis current ([Figures 2](#) through [7](#)) include minimum/maximum error bars. The remaining figures plot the median only.

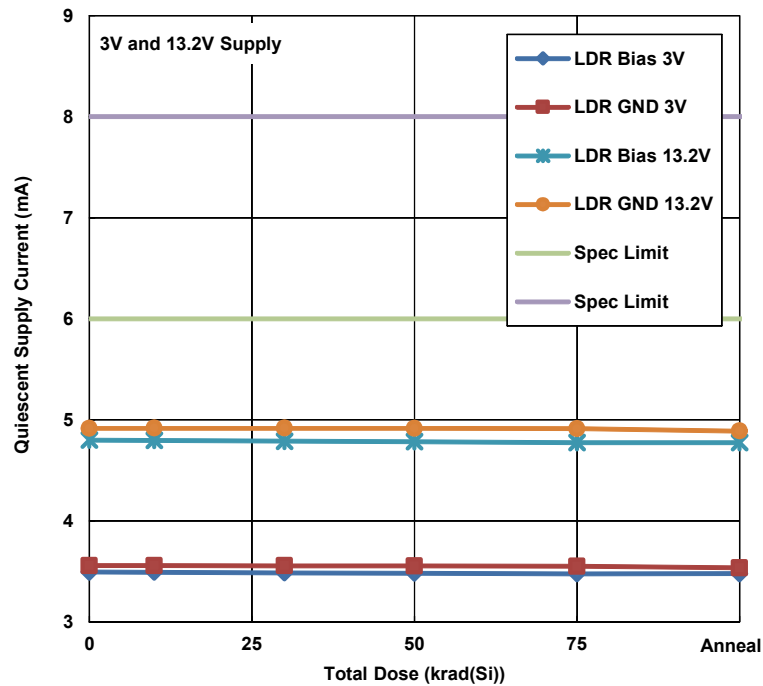


Figure 1. ISL73321SEH quiescent power supply current, 3V and 13.2 V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 6mA maximum (3V supply) and 8mA maximum (13.2V).

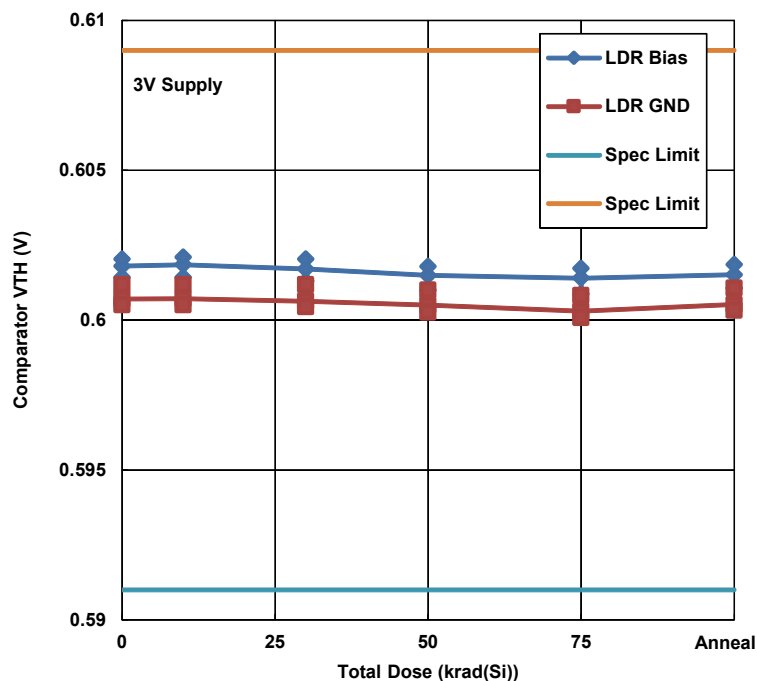


Figure 2. ISL73321SEH comparator rising threshold voltage, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 0.591V to 0.609V.

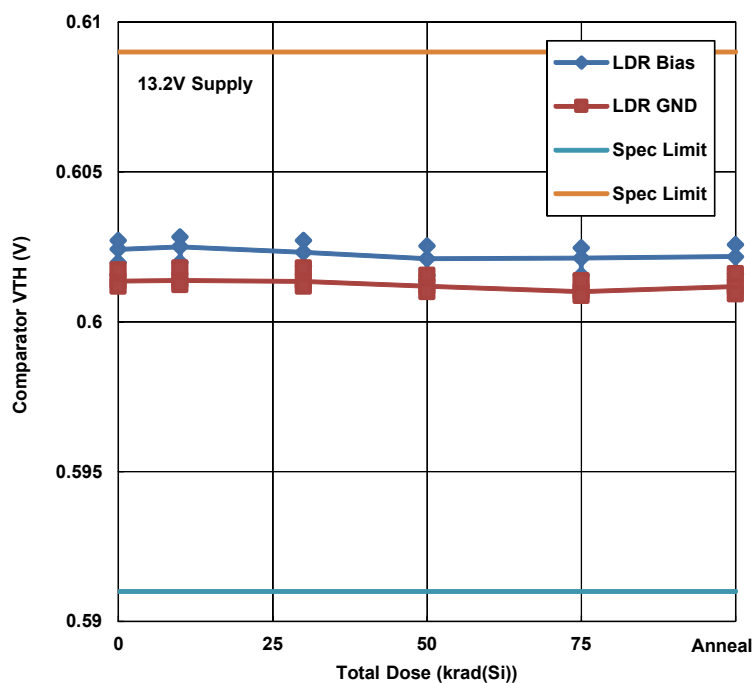


Figure 3. ISL73321SEH comparator rising threshold voltage, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 0.591V to 0.609V.

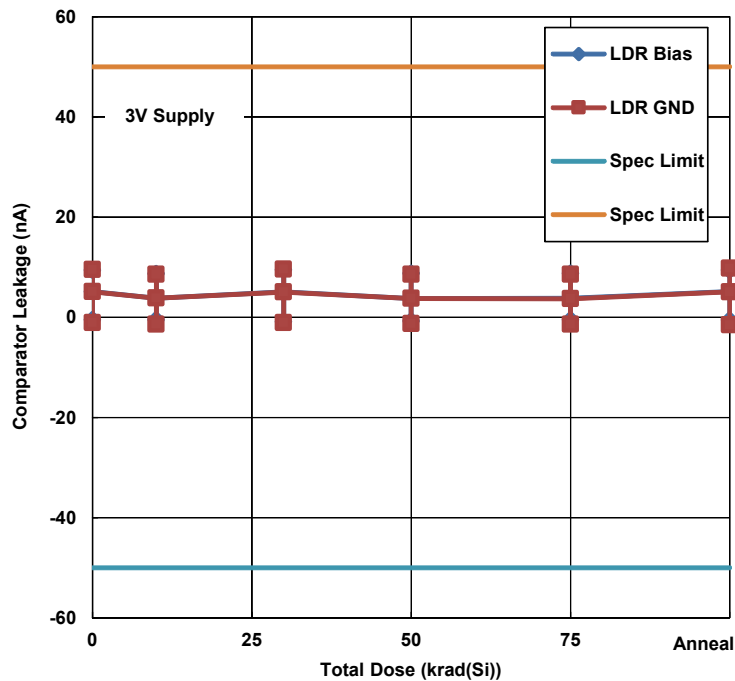


Figure 4. ISL73321SEH comparator input leakage current, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are -50nA to 50nA.

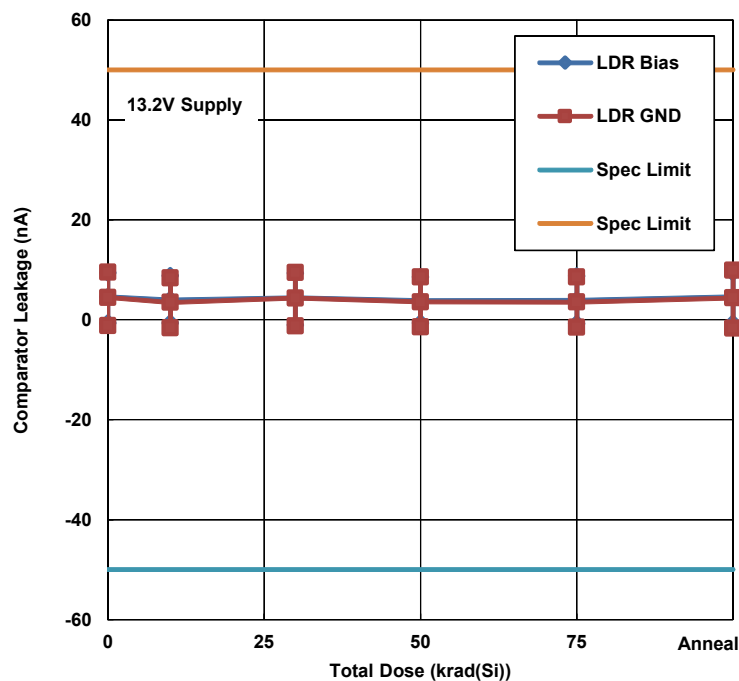


Figure 5. ISL73321SEH comparator input leakage current, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are -50nA to 50nA.

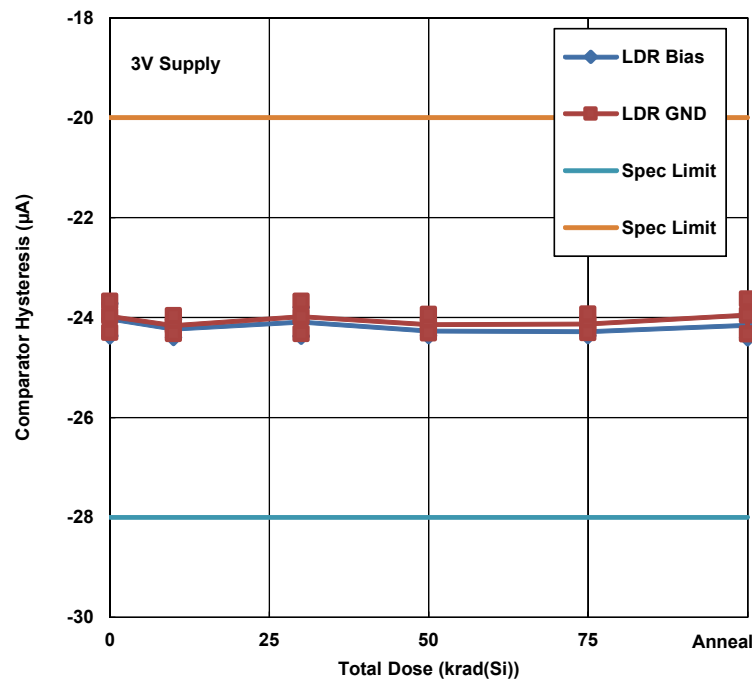


Figure 6. ISL73321SEH comparator hysteresis current, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are -28µA to -20µA.

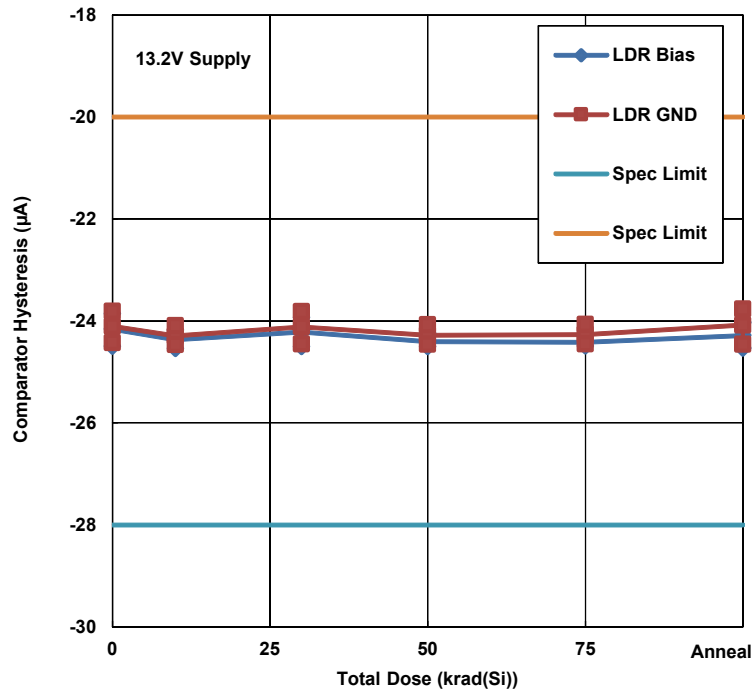


Figure 7. ISL73321SEH comparator hysteresis current, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are -28µA to -20µA.

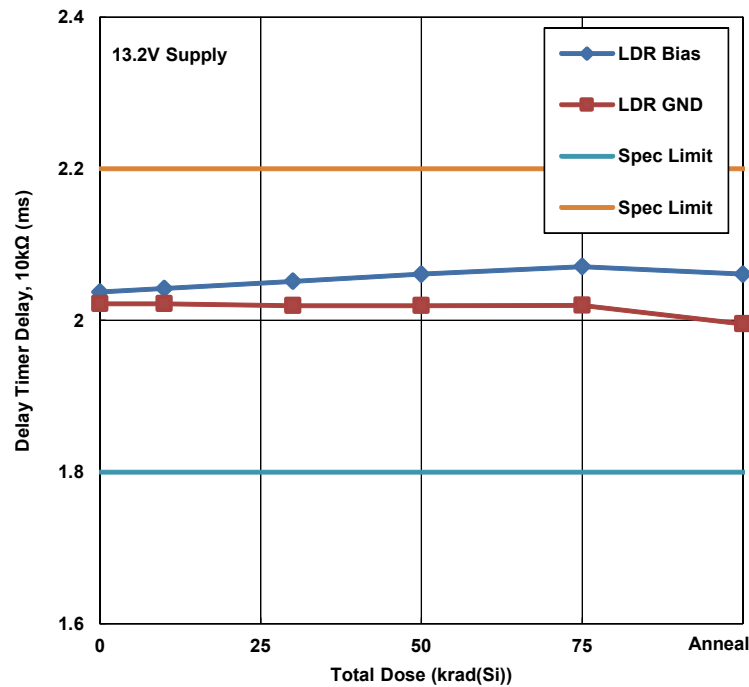


Figure 8. ISL73321SEH delay timer delay with a timer delay resistor value of 10kΩ, 13.2V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 1.8ms to 2.2ms.

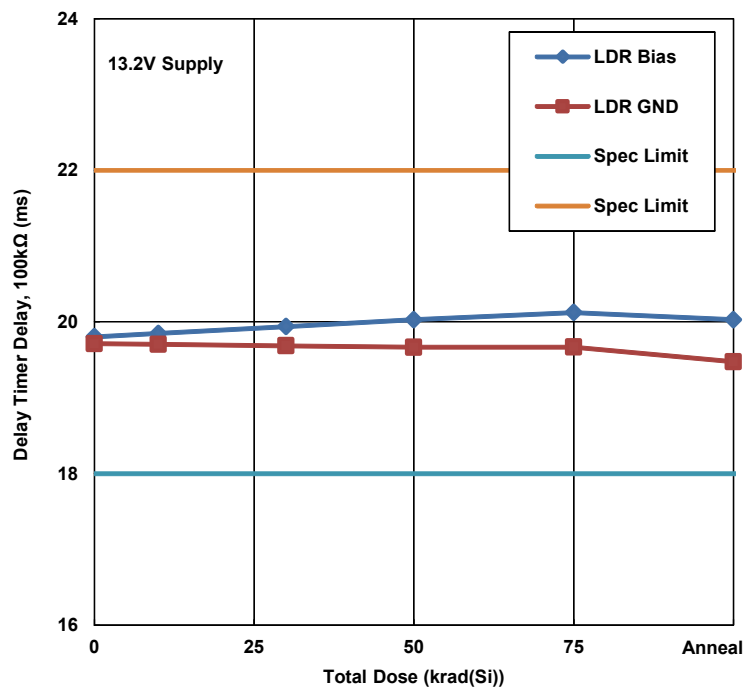


Figure 9. ISL73321SEH delay timer delay with a timer delay resistor value of 100kΩ, 13.2V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 18ms to 22ms.

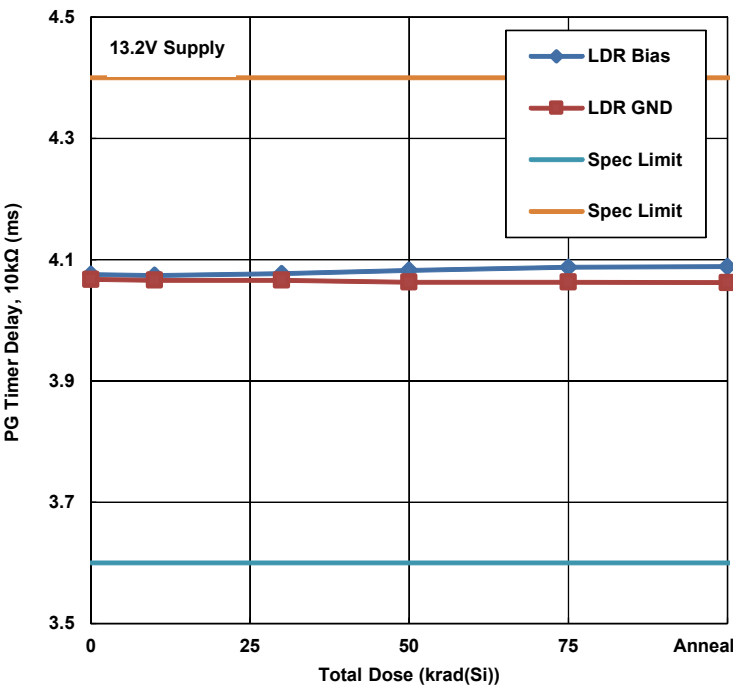


Figure 10. ISL73321SEH Power Good (PGOOD) timer delay with a timer delay resistor value of 10kΩ, 13.2V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 3.6ms to 4.4ms.

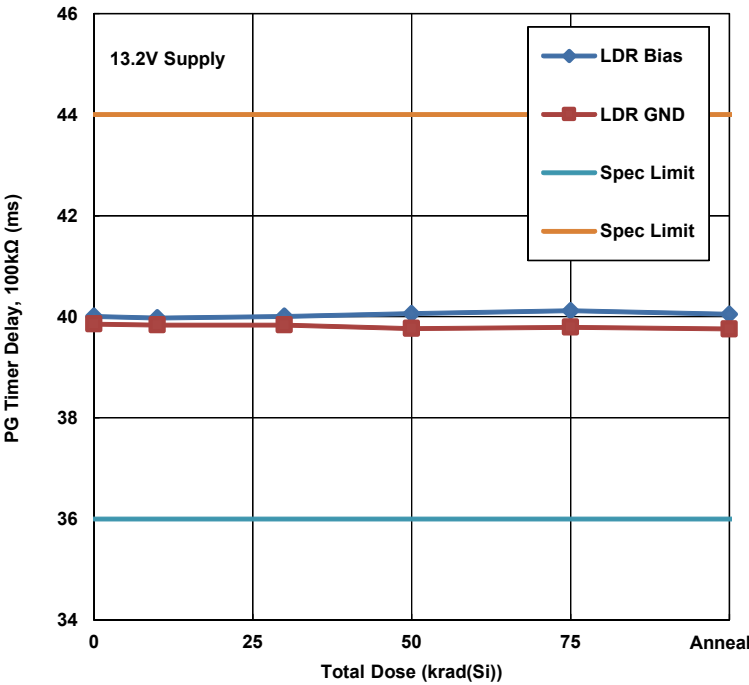


Figure 11. ISL73321SEH Power Good (PGOOD) timer delay with a timer delay resistor value of 100kΩ, 13.2V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 36ms to 44ms.

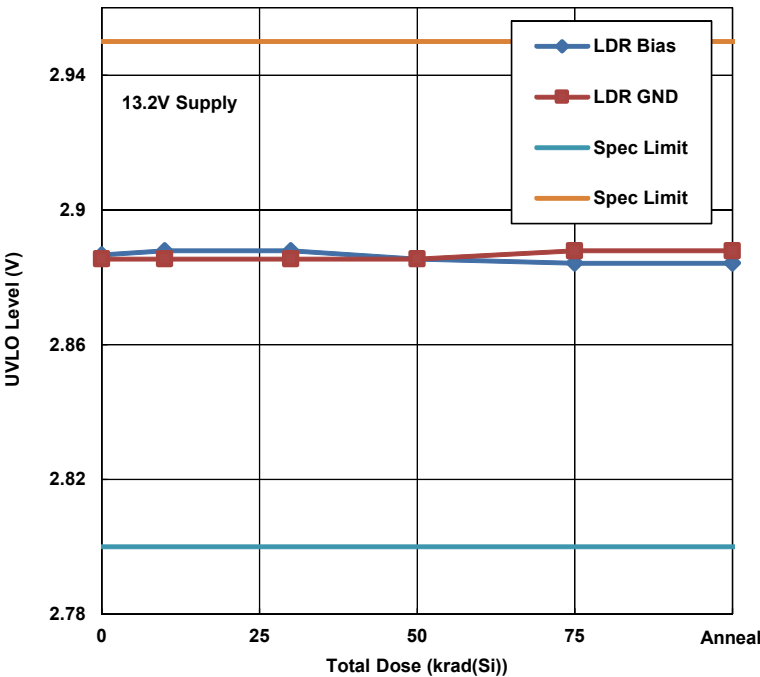


Figure 12. ISL73321SEH rising undervoltage lockout level, 13.2V supply, as a function of total dose irradiation for the biased (per Appendix 1) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 2.8V to 2.95V.

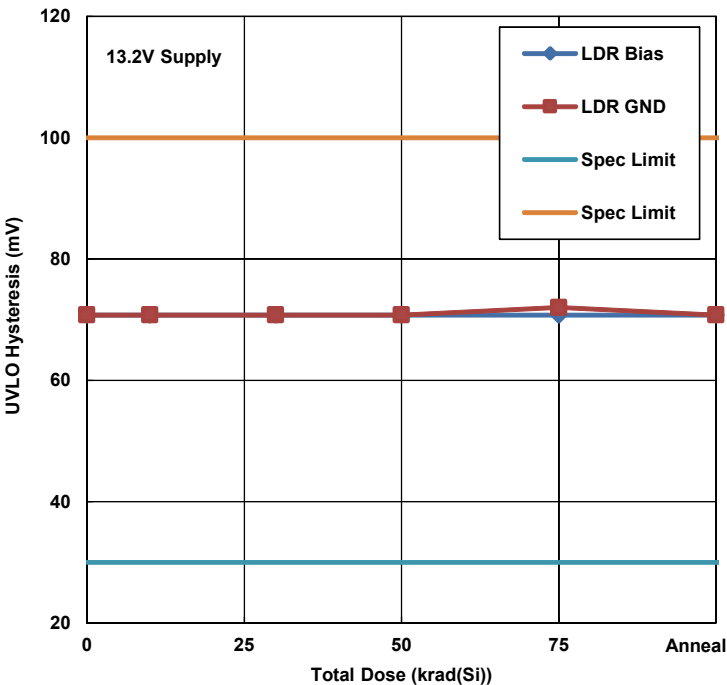


Figure 13. ISL73321SEH undervoltage lockout hysteresis, 13.2V supply, as a function of total dose irradiation for the biased (per [Appendix on page 13](#)) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The dose rate was 0.01 rad(Si)/s. The irradiations were followed by a 100°C 168-hour biased anneal. The sample size of both cells was 4. The SMD Group A limits are 30mV to 100mV.

3. Discussion and Conclusion

We report the results of a low dose rate total dose test of the ISL73321SEH radiation hardened quad power supply sequencer. All irradiations were followed by a 168-hour anneal at 100°C under bias.

[“Attributes Data” on page 3](#) summarizes the attributes data for the test. [“Critical Parameters” on page 3](#) summarizes thirteen critical parameters for the part. Finally [“Critical Parameter Variables Data” on page 5](#) provides plots of the total dose and anneal response for these critical parameters.

All parameters remained well within the SMD Group A limits at all downpoints. [Figures 2](#) through [7](#) plot parameter averages for the INIT, UP, VM1, VM2, VM3, and VM4 inputs; we plotted the median as well as minimum/maximum error bars for these averages. No differences in total dose response between biased and grounded irradiation were noted and the part is hence not considered bias sensitive.

TR054 Rev.0.00
Sep 14, 2017



Page 13 of 14

5. Revision History

Rev.	Date	Description
0.00	Sep 14, 2017	Initial release

© Copyright Intersil Americas LLC 2017. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the document is current before proceeding.

For information regarding Intersil Corporation and its products, see www.intersil.com