Smart Configurator for RX V2.0.0

Release Note

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Abstract

Thank you for using the Smart Configurator for RX.

This document describes the restrictions and points for caution. Read this document before using the product.

Contents

1. Introduction

The Smart Configurator for RX is a software tool to generate control programs (device driver programs) for peripheral modules (timers, UART, A/D, etc.). It generates device driver codes using user settings through GUI. Initialize code and API (Application Programming Interface) functions are provided.

1.1 System requirements

The operating environment is as follows.

1.1.1 PC

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1, Windows® 7)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-bit Windows requires 2 GB or more)
- Hard disk capacity: 200 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to Windows OS: .NET Framework version4.5

1.1.2 Development Environments

- Renesas electronics Compiler for RX [CC-RX] V3.00.00 or later
- GNURX 4.8.4.201803 or later
- IAR Embedded Workbench 4.10.2 or later

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RX V2.0.0.

Table 1-1 Support Devices

Group (HW Manual number)	PIN	Device name
RX110 Group (R01UH0421EJ0120)	36pin	R5F5110HAxLM, R5F5110JAxLM, R5F51101AxLM, R5F51103AxLM
	40pin	R5F51101AxNF, R5F51103AxNF, R5F5110HAxNF, R5F5110JAxNF
	48pin	R5F51101AxNE, R5F51103AxNE, R5F51104AxNE, R5F51105AxNE, R5F5110JAxNE, R5F51101AxFL, R5F51103AxFL, R5F51104AxFL, R5F51105AxFL, R5F5110JaxFL
	64pin	R5F51101AxLF, R5F51103AxLF, R5F51104AxLF, R5F51105AxLF, R5F5110JAxLF, R5F51101AxFK, R5F51103AxFK, R5F51104AxFK, R5F51105AxFK, R5F5110JAxFK, R5F51101AxFM, R5F51103AxFM, R5F51104AxFM, R5F51105AxFM, R5F5110JAxFM
RX111 Group (R01UH0365EJ0130)	36pin	R5F51111AxLM, R5F51113AxLM, R5F5111JAxLM
	40pin	R5F51111AxNF, R5F51113AxNF, R5F5111JAxNF
	48pin	R5F51111AxFL, R5F51113AxFL, R5F51114AxFL, R5F51115AxFL, R5F51116AxFL, R5F51117AxFL, R5F51118AxFL, R5F5111JAxFL, R5F51111AxNE, R5F51113AxNE, R5F51114AxNE, R5F51115AxNE, R5F51116AxNE, R5F51117AxNE, R5F51118AxNE, R5F5111JAxNE
	64pin	R5F51111AxFM, R5F51113AxFM, R5F51114AxFM, R5F51115AxFM, R5F51116AxFM, R5F51117AxFM, R5F51118AxFM, R5F5111JAxFM, R5F51111AxFK, R5F51113AxFK, R5F51114AxFK, R5F51115AxFK, R5F51116AxFK, R5F51117AxFK, R5F51118AxFK, R5F5111JAxFK, R5F51111AxLF, R5F51113AxLF, R5F51114AxLF, R5F51115AxLF, R5F51116AxLF, R5F51117AxLF, R5F51118AxLF, R5F5111JAxLF
RX113 Group (R01UH0448EJ0110)	64pin	R5F51135AxFM, R5F51136AxFM, R5F51137AxFM, R5F51138AxFM
	100pin	R5F51135AxLJ, R5F51136AxLJ, R5F51137AxLJ, R5F51138AxLJ, R5F51135AxFP, R5F51136AxFP, R5F51137AxFP, R5F51138AxFP
RX130 Group (R01UH0560EJ0200)	48pin	R5F51303AxFL, R5F51305AxFL, R5F51303AxNE, R5F51305AxNE, R5F51306AxNE, R5F51306AxFL, R5F51307AxNE, R5F51307AxFL, R5F51308AxNE, R5F51308AxFL, R5F51306BxFL
	64pin	R5F51303AxFM, R5F51305AxFM, R5F51303AxFK, R5F51305AxFK, R5F51306AxFK, R5F51306AxFM, R5F51307AxFK, R5F51307AxFM, R5F51308AxFK, R5F51308AxFM R5F51308AxFK, R5F51308AxFM, R5F51306BxFK, R5F51306BxFM
	80pin	R5F51303AxFN, R5F51305AxFN, R5F51306AxFN, R5F51306BxFN
	100pin	R5F51305AxFP, R5F51306AxFP, R5F51307AxFP, R5F51308AxFP, R5F51305BxFP, R5F51306BxFP
RX230 Group (R01UH0496EJ0110)	48pin	R5F52305AxNE, R5F52306AxNE, R5F52305AxFL, R5F52306AxFL
	64pin	R5F52305AxND, R5F52306AxND, R5F52305AxFM, R5F52306AxFM, R5F52305AxLF, R5F52306AxLF
	100pin	R5F52305AxLA, R5F52306AxLA, R5F52305AxFP, R5F52306AxFP

Table 1-2 Support Devices

Group (HW Manual number)	PIN	Device name
RX231 Group (R01UH0496EJ0110)	48pin	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64pin	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, R5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, R5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100pin	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23T Group (R01UH0520EJ0110)	48pin	R5F523T3AxFL, R5F523T5AxFL
	52pin	R5F523T5AxFD, R5F523T3AxFD
	64pin	R5F523T5AxFM, R5F523T3AxFM
RX24T Group (R01UH0576EJ0200)	64pin	R5F524TAAxFM, R5F524T8AxFM
	80pin	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100pin	R5F524TCAxFP, R5F524T8AxFP, R5F524TBAxFP, R5F524TEAxFP, R5F524TAAxFP
RX24U Group (R01UH0658EJ0100)	100pin	R5F524UEAxFP, R5F524UCAxFP, R5F524UBAxFP
	144pin	R5F524UEAxFB, R5F524UBAxFB, R5F524UCAxFB
RX64M Group (R01UH0377EJ0110)	100pin	R5F56MFCxFP, R5F56MFCxLJ, R5F56MFDxFP, R5F56MFDxLJ, R5F56MGCxFP, R5F56MGCxLJ, R5F56MGDxFP, R5F56MGDxLJ, R5F56MJCxFP, R5F56MJCxLJ, R5F56MJDxFP, R5F56MJDxLJ, R5F56MLCxFP, R5F56MLCxLJ, R5F56MLDxFP, R5F56MLDxLJ
	144/145pin	R5F56MFCxFB, R5F56MFCxLK, R5F56MFDxFB, R5F56MFDxLK, R5F56MGCxFB, R5F56MGCxLK, R5F56MGDxFB, R5F56MGDxLK, R5F56MJCxFB, R5F56MJCxLK, R5F56MJDxFB, R5F56MJDxLK, R5F56MLCxFB, R5F56MLCxLK, R5F56MLDxFB, R5F56MLDxLK
	176/177pin	R5F56MFDxFC, R5F56MFDxBG, R5F56MFDxLC, R5F56MFCxFC, R5F56MFCxBG, R5F56MFCxLC, R5F56MGDxFC, R5F56MGDxBG, R5F56MGDxLC, R5F56MGCxFC, R5F56MGCxBG, R5F56MGCxLC, R5F56MJDxFC, R5F56MJDxBG, R5F56MJDxLC, R5F56MJCxFC, R5F56MJCxBG, R5F56MJCxLC, R5F56MLDxFC, R5F56MLDxBG, R5F56MLDxLC, R5F56MLCxFC, R5F56MLCxBG, R5F56MLCxLC

Table 1-3 Support Devices

Group (HW Manual number)	PIN	Device name
RX65N Group (R01UH0590EJ0210)	100pin	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP, R5F565NCHxLJ, R5F565NCDxLJ, R5F565NEHxLJ, R5F565NEDxLJ, R5F565NCHxFP, R5F565NCDxFP, R5F565NEHxFP, R5F565NEDxFP
	144/145pin	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565NCHxFB, R5F565NCDxFB, R5F565NEHxFB, R5F565NEDxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK, R5F565NCHxLK, R5F565NCDxLK, R5F565NEHxLK, R5F565NEDxLK
	176/177pin	R5F565NCHxBG, R5F565NCDxBG, R5F565NEHxBG, R5F565NEDxBG, R5F565NCHxFC, R5F565NCDxFC, R5F565NEHxFC, R5F565NEDxFC, R5F565NCHxLC, R5F565NCDxLC, R5F565NEHxLC, R5F565NEDxLC
RX651 Group (R01UH0590EJ0210)	100pin	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145pin	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F5651CDxFB, R5F5651CHxFB, R5F5651EDxFB, R5F5651EHxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK, R5F5651CDxLK, R5F5651CHxLK, R5F5651EDxLK, R5F5651EHxLK
	176177pin	R5F5651CDxBG, R5F5651CDxFC, R5F5651CHxBG, R5F5651CHxFC, R5F5651EDxBG, R5F5651EDxFC, R5F5651EHxBG, R5F5651EHxFC, R5F5651CDxLC, R5F5651CHxLC, R5F5651EDxLC, R5F5651EHxLC
RX66T Group (R01UH0749EJ0100)	64pin	R5F566TAAxFM, R5F566TAExDFM, R5F566TEAxFM, R5F566TEExFM
	80pin	R5F566TAAxFF, R5F566TAExFF, R5F566TEAxFF, R5F566TEExFF, R5F566TAAxFN, R5F566TAExFN, R5F566TEAxFN, R5F566TEExFN
	100pin	R5F566TAAxFP, R5F566TABxFP, R5F566TAExFP, R5F566TAFxFP, R5F566TEAxFP, R5F566TEBxFP, R5F566TEExFP, R5F566TEFxFP
	112pin	R5F566TAAxFH, R5F566TAExFH, R5F566TEAxFH, R5F566TEExFH

Table 1-4 Support Devices

Group (HW Manual number)	PIN	Device name
RX71M Group (R01UH0493EJ0110)	100pin	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145pin	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLK, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177pin	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RX V2.0.0.

Table 2-1 Support Components **○: Support, /: Non-support**

No	Components	Mode	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	Remarks
1	8-Bit Timer	-	/	/	○	○	○	○	○	○	○	○	○	
2	CRC Calculator	-	○	○	○	○	○	○	○	○	○	○	○	
3	D/A Converter	-	/	○	○	○	○	○	○	○	○	○	○	
4	DMA Controller	-	/	/	/	/	○	/	/	○	○	○	○	
5	I2C Slave Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	
6	I2C Master Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	
7	LCD Controller		/	/	○	/	/	/	/	/	/	/	/	
8	PWM Mode Timer	PWM mode 1	○	○	○	○	○	○	○	○	○	○	○	
		PWM mode 2	○	○	○	○	○	○	○	○	○	○	○	
9	SCI/SCIF Clock Synchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2, 3, 4 in Table 4
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
10	SCI/SCIF Asynchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Transmission	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
11	SPI Clock Synchronous Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	○	
12	SPI Operation Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit only	○	○	○	○	○	○	○	○	○	○	○	
13	Event Link Controller	-		○	○	○	○	/	/	○	○	○	○	
14	Watchdog Timer	-	○	○	○	○	○	○	○	○	○	○	○	
15	Clock Frequency Accuracy Measurement Circuit	-	○	○	○	○	○	○	○	○	○	○	○	

Table 2-2 Support Components

○: Support, /: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	Remarks
16	Group Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	
17	Comparator	-	/	/	○	○	○	/	/	/	/	○	/	
18	Compare Match Timer	-	○	○	○	○	○	○	○	○	○	○	○	
19	Single Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	
20	Smart Card Interface Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	
		Reception	○	○	○	○	○	○	○	○	○	○	○	
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	
21	Dead-time Compensation Counter	-	○	○	○	○	○	○	○	○	○	○	○	
22	Data Transfer Controller	-	○	○	○	○	○	○	○	○	○	○	○	
23	Data Operation Circuit	-	○	○	○	○	○	○	○	○	○	○	○	
24	Normal Mode Timer		○	○	○	○	○	○	○	○	○	○	○	Refer to No 1 in Table 3
25	Buses	-	○	○	○	○	○	○	○	○	○	○	○	
26	Programmable Pulse Generator	-	/	/	/	/	/	/	/	○	○	/	○	
27	Ports	-	○	○	○	○	○	○	○	○	○	○	○	
28	Port Output Enable	-	/	○	○	○	○	○	○	○	○	○	○	
29	Real Time Clock	Binary	○	○	○	○	○	/	/	○	○	/	○	
		Calendar	○	○	○	○	○	/	/	○	○	/	○	
30	Remote Control Signal Receiver	-	/	/	/	○	/	/	/	/	/	/	/	
31	Low-Power Timer	-	/	/	○	○	○	/	/	/	/	/	/	
32	Phase Counting Mode Timer	-	○	○	○	○	○	○	○	○	○	○	○	
33	Interrupt Controller	-	○	○	○	○	○	○	○	○	○	○	○	
34	General PWM Timer	Saw-wave PWM mode	/	/	/	/	/	○	○	○	/	○	○	Refer to No 1 in Table 4
		Saw-wave one-shot pulse mode	/	/	/	/	/	○	○	○	/	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 1	/	/	/	/	/	○	○	○	/	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 2	/	/	/	/	/	○	○	○	/	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 3	/	/	/	/	/	○	○	○	/	○	○	Refer to No 1 in Table 4
35	Low Power Consumption	-	○	○	○	○	○	○	○	○	○	○	○	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	/	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 2	/	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 3	/	○	○	○	○	○	○	○	○	○	○	
37	Continuous Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	
38	Voltage Detection Circuit	-	○	○	○	○	○	○	○	○	○	○	○	

3. Changes

This chapter describes changes to the Smart Configurator for RX V2.0.0.

3.1 New support

3.1.1 Supports RX23T, RX24T, RX24U devices

Supported RX23T, RX24T, RX24U group devices. For the supported components, refer to "2.2 Support Components List".

3.1.2 Supports change device at project level

Changing device of Smart Configurator project has been supported at the project level.
When using IDE function to change device of Smart Configurator project from a supported device to another supported device, compatible project settings and components configurations will be ported to the new device selected. For the supported devices, refer to "2.1 Support Devices List".

3.1.3 Enhanced board usability and functionality

Board functionality in Smart Configurator for RX V.2.0.0 has been enhanced to improve usability.

1) Supports switching between assigned pins and default board pins in MCU Package view.

2) In Pin Number list of Pin page, a new column is added to display the default pin function of the board selection in Board page.

3) Pin Number list of Pins page supports assigning of all pins to default pin functions based on board selection in Board page and clearing of all default pin functions assigned.

4) Search function in Pins page is improved to search text in all columns.

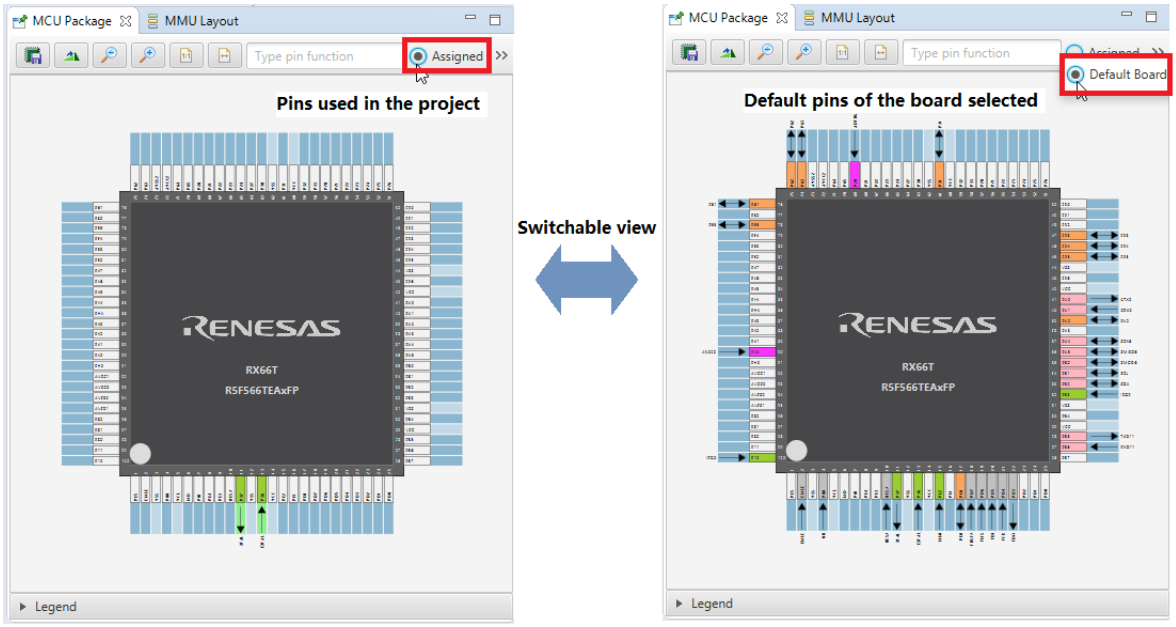

Figure 3-1 Switch between “Assigned” pins view and “Default Board” pins view

3.1.4 Supports FreeRTOS project with configuration of kernel settings on GUI

Using Smart Configurator GUI to configure kernel settings of FreeRTOS project has been supported for RX64M, RX651, RX65N and RX71M.

3.1.5 Supports change FIT modules version

Changing the version of r_bsp and FIT modules that have been added to Smart Configurator project is now supported in Smart Configurator for RX V2.0.0.

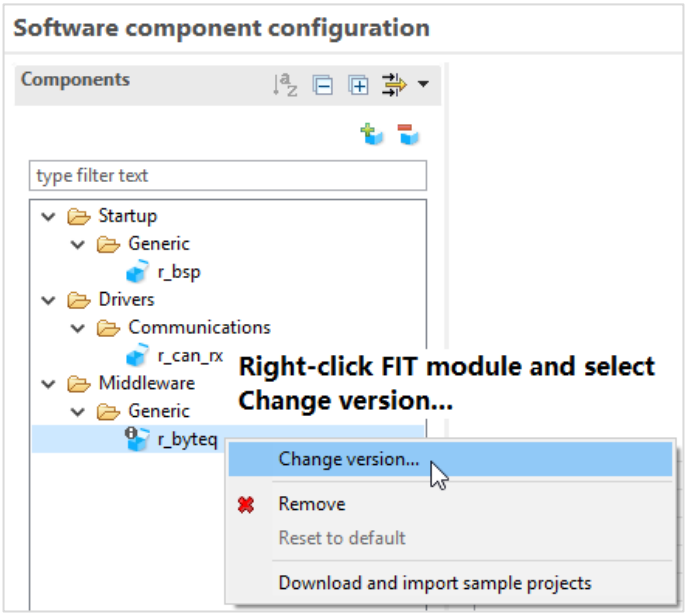

Figure 3-2 Change FIT modules version

3.1.6 Supports download and import sample projects of FIT modules

Download and import sample projects of FIT modules to e^2 studio project workspace has been supported In Smart Configurator for RX V2.0.0.

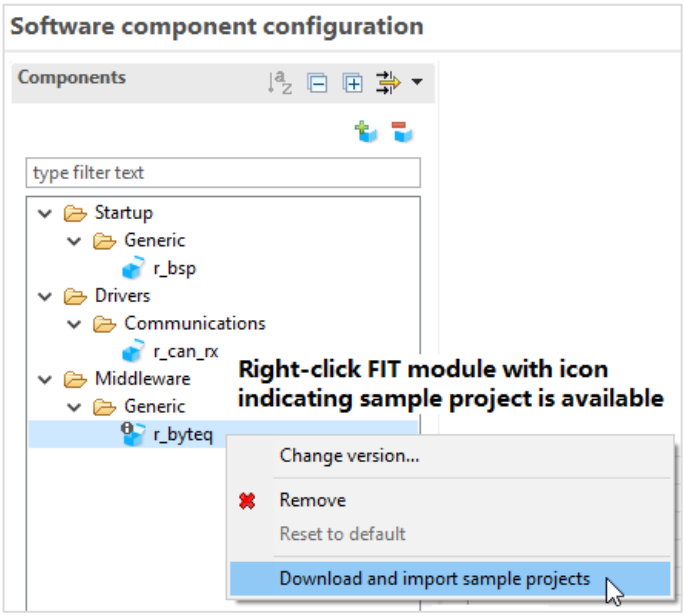

Figure 3-3 Download and import sample projects for FIT modules

3.2 Correction of issues/limitations

3.2.1 Fixed the issue of P50-P53 in PORT5 cannot be set as input port when using RX130 group 100-pins devices

The issue of P50-P53 in PORT5 cannot be set as input port when using RX130 group 100-pins devices is fixed.

3.2.2 Fixed the issue of redundant code to set output trigger signal for unused PPG1 Group 4 operation

The issue of redundant code to set output trigger signal for unused PPG1 Group 4 operation in Programmable Pulse Generator (RX64M, RX651, RX65N, RX71M) has been fixed.

3.2.3 Fixed the issue of only allows input of 16-bits count to TRGn register in Normal Mode Timer

The issue of only allows input of 16-bits count to TRGn register in Normal Mode Timer when using Smart Configurator for RX Ver.1.5.0 or before for RX64M, RX651, RX65N and RX71M has been fixed.

3.3 Specification changes

3.3.1 Changed code of TXI handler in Smart Card Interface Mode

When using Smart Card Interface Mode in Smart Configurator for RX Ver.1.5.0 or before (RX110, RX111, RX113, RX23T, RX24T, RX24U, RX64M, RX66T, RX71M), API R_< Configuration Name>_Stop need to be called after completing the first cycle of data transmission to allow the next cycle of data transmission. From Smart Configurator for RX Ver.2.0.0, code in API r_<Configuration Name>_transmit_interrupt is changed to set SCR.TE bit to '0U' after setting SCR.TIE bit to '0U'. With this code change, next cycle of data transmission can be started smoothly without the need to call R_< Configuration Name>_Stop after completing the first cycle of data transmission.

Example: Smart Card Interface Mode (SCI6)

```
static void r_Config_SCI6_transmit_interrupt(void)
{
  if (0U < g_sci6_tx_count)
  {
    SCI6.TDR = *gp_sci6_tx_address;
    gp_sci6_tx_address++;
    g_sci6_tx_count--;
  }
  else
  {
    SCI6.SCR.BIT.TIE = 0U;
    SCI6.SCR.BIT.TE = 0U;                    Added
    r_Config_SCI6_callback_transmitend();
  }
}
```

Figure 3-4 SCR.TE bit is set to '0U' after setting SCR.TIE bit to '0U'

3.3.2 Removed "CACREF pin" as clock selection for Measurement target setting in Clock Frequency Accuracy Measurement Circuit (CAC)

"CACREF pin" as clock selection for Measurement target setting when using Clock Frequency Accuracy Measurement Circuit (CAC) was removed for RX130, RX230, RX231, RX64M, RX651, RX65N and RX71M.

4. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RX V2.0.0. Please refer to a document of each module about a caution of a FIT module.

4.1 List of Limitation

Table 3 List of Limitation

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	Remarks
1	Note on using double buffer function in Complementary PWM Mode Timer	/	/	/	/	/	○	○	○	○	○	○	
2	Note on using 10-bit address mode in I2C Master Mode component	○	○	○	○	○	○	○	○	○	○	○	

4.2 Details of Limitation

4.2.1 Note on using double buffer function in Complementary PWM Mode Timer

When using double buffer function in Complementary PWM Mode Timer, the initial PWM duty ratio value of TGRE and TRGF registers are incorrect.
As workaround, manually change the value of TGRE and TGRF registers in API (R_<Configuration Name>_Create) to the desired value + 1.

Example: Complementary PWM Mode 3 (MTU3 and MTU4)

```
void R_Config_MTU3_MTU4_Create(void)
{
  /* Release MTU channel 3 from stop state */
  MSTP(MTU3) = 0U;

  /* Enable read/write to MTU3, MTU4 registers */
  MTU.TRWERA.BIT.RWE = 1U;

  /* Stop MTU channel 3 counter */
  MTU.TSTRA.BIT.CST3 = 0U;

  /* Set A/D conversion signal output for ADSM0, ADSM1 pins */
  MTU.TADSTRGR0.BYTE = _00_MTU_TADSTRS_NOSOURCE;
  MTU.TADSTRGR1.BYTE = _00_MTU_TADSTRS_NOSOURCE;

  /* MTU channel 3 is used as complementary PWM mode 3 */
  MTU3.TIER.BYTE = 0x00U;
  MTU4.TIER.BYTE = 0x00U;
  MTU.TITCR1A.BIT.T3AEN = 0U;
  MTU.TITCR1A.BIT.T4VEN = 0U;
  MTU3.TCR.BYTE = _00_MTU_PCLK_1 | _00_MTU_CKCL_DIS;
  MTU4.TCR.BYTE = _00_MTU_PCLK_1;
  MTU3.TCR2.BYTE = _00_MTU_PCLK_1;
  MTU4.TCR2.BYTE = _00_MTU_PCLK_1;
  MTU.TGCRA.BYTE = _80_MTU_BDC_OUT;
  MTU3.TCNT = _0280_3TCNT_VALUE;
  MTU4.TCNT = 0x0000U;
  MTU.TSYRA.BIT.SYNC3 = 0U;
  MTU.TSYRA.BIT.SYNC4 = 0U;
  MTU3.TGRB = _0064_3TGRB_VALUE;
  MTU3.TGRD = _0064_3TGRB_VALUE;
  MTU4.TGRA = _0064_4TGRA_VALUE;
  MTU4.TGRC = _0064_4TGRA_VALUE;
  MTU4.TGRB = _0064_4TGRB_VALUE;
  MTU4.TGRD = _0064_4TGRB_VALUE;
  MTU3.TGRE = _0063_3TGRE_VALUE;
  MTU4.TGRE = _0063_4TGRE_VALUE;
  MTU4.TGRF = _0063_4TGRF_VALUE;
  :  (codes are omitted)
}
```

Manually change the value of TGRE and TGRF to the desired value + 1 after code is generated.

Figure 4-1 Workaround for setting TGRE and TRGF registers value

4.2.2 Note on using 10-bit address mode in I2C Master Mode component

When configuring I2C-bus Interface (RIICa) by I2C Master Mode component in Smart Configurator, the slave address smaller than 0x80 cannot be sent with 10-bit address mode in master transmission operation triggered by calling R_<Configuration Name>_Master_Send function. The address mode is set to 7-bit address mode if the address value specified by the parameter of R_<Configuration Name>_Master_Send function is smaller than 0x80.

5. Points for Caution

This section describes points for caution regarding the Smart Configurator for RX V2.0.0. Please refer to a document of each module about a caution of a FIT module.

5.1 List of Caution

Table 4 List of Caution

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	Remarks
1	Note on configuring GPT interrupt	/	/	/	/	/	/	○	○	/	○	○	
2	Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode	○	○	○	○	○	○	○	○	○	○	○	
3	Note on using only reception in SCI Clock Synchronous Mode	○	○	○	○	○	○	○	○	○	○	○	
4	Notes on using high transfer speed in SCIF Synchronous Mode	/	/	/	/	/	/	/	○	/	/	○	

5.2 Details of Caution

5.2.1 Note on configuring GPT interrupts

The GPT interrupts are not specified as the Software Configurable Interrupt in the initial state even after the GPT interrupts are configured by GPT component. To specify GPT interrupts as Software Configurable Interrupt source, release unused Software Configurable interrupt source on the Interrupt sheet and allocate GPT interrupts instead.

5.2.2 Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode

Sequence of setting SCR.TE bit does not follow the usage note in User's Manual: Hardware.
Instead, SCR.TE bit is set to 1 after changing the pin function to TXDn. Output of TXDn pin becomes high impedance.
Please connect a pull-up resistor to the TXDn line, prevent the TXDn line from becoming high impedance.

5.2.3 Note on using only reception in SCI Clock Synchronous Mode

In SCI Clock Synchronous Mode using internal clock, if only reception is enabled in high communication speed, extra clocks are generated even though reception has been completed.
This is due to the delay in disabling RE to stop the clock after the desired number of data is received.
To prevent this issue, select Transmission/Reception work mode when using Smart Configurator. Use "R_<Configuration Name>_Serial_Send_Receive" function instead of "R_<Configuration Name>_Serial_Receive". The same number of data for tx_num and rx_num should be specified.
Disable TXDn pin in Smart Configurator Pins page and send dummy data if transmission is not required.
There will be warnings when TXDn pin is disabled. These warnings can be ignored as TXDn pin is not intended to be used originally.

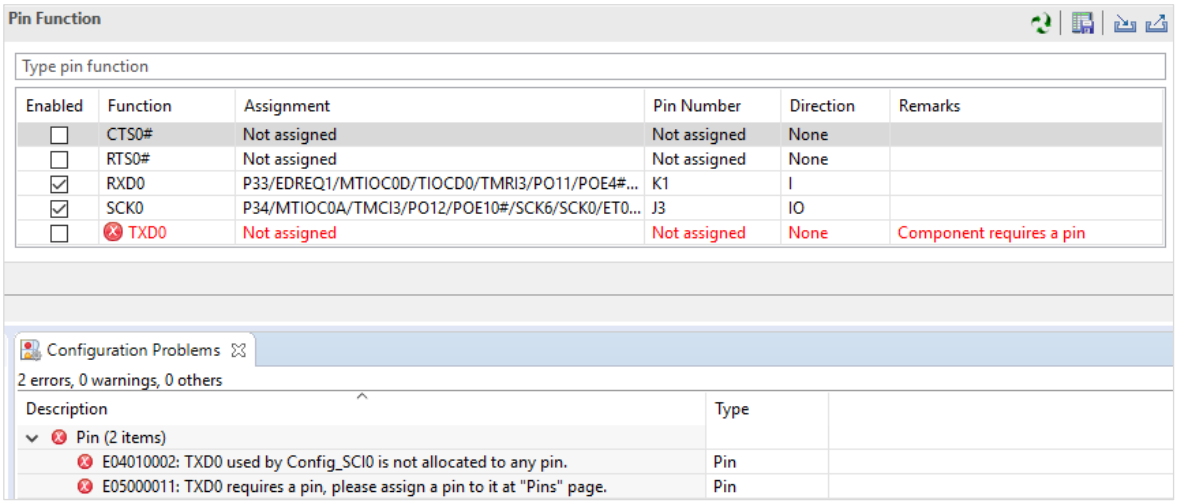

Figure 5-1 Ignore warnings when TXDn pin is disabled (Example with TXD0)

5.2.4 Note on using high transfer speed in SCIF Synchronous Mode

If the number of reception data specified for the API (R_<Configuration Name>_Serial_Receive or R_<Configuration Name>_Serial_Send_Receive) and reception FIFO threshold specified on GUI do not satisfy the formula below:

(Reception Data Size) = n * (Reception FIFO threshold) (n=1,2,3,,,,)

extra clock generation may occur after the desired number of data is received in high communication speed when using internal clock.
To prevent this issue, specify the reception data size and reception FIFO threshold that satisfy the formula.

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