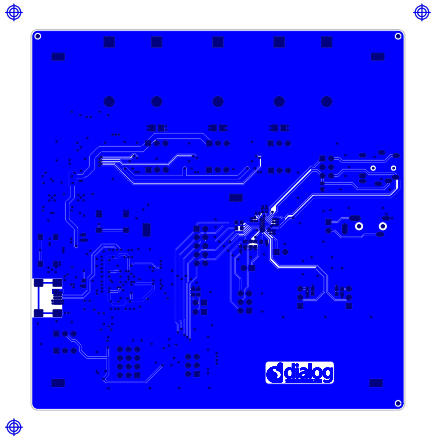
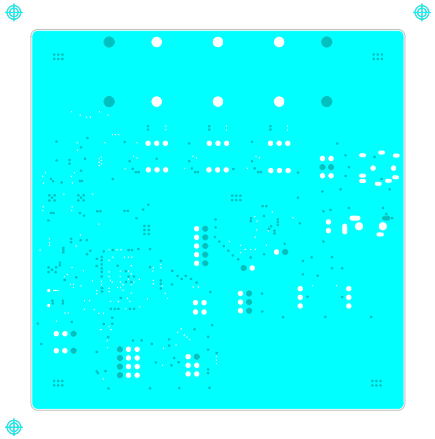
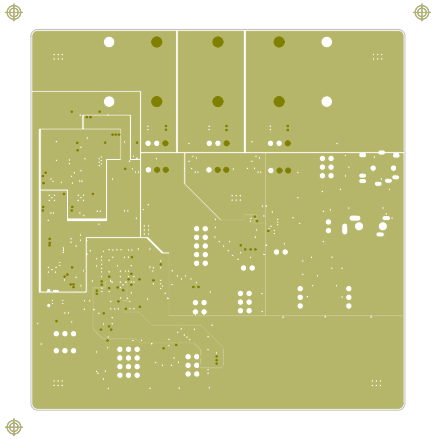


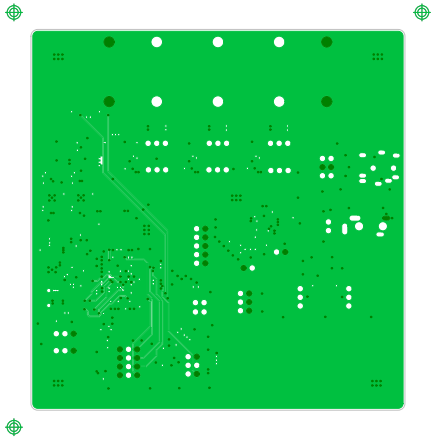
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C1	
LAYER TOP SIDE TRACK	



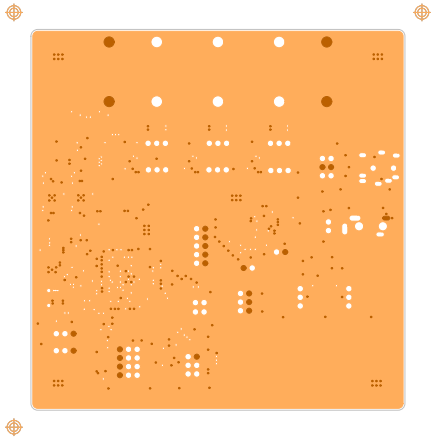
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C2	
LAYER INNER LAYER 2	



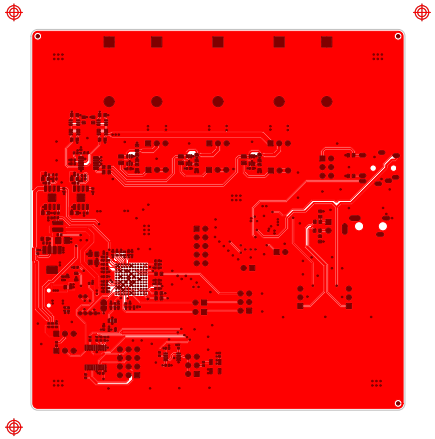
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C3	
LAYER INNER LAYER 3	



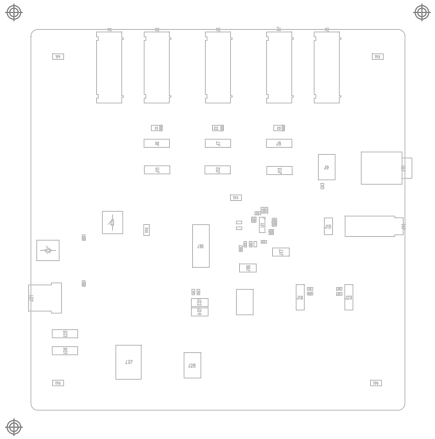
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C4	
LAYER INNER LAYER 4	



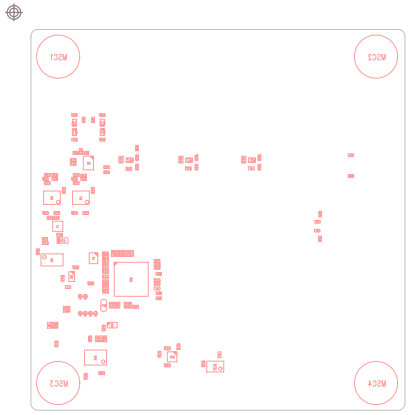
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C5	
LAYER INNER LAYER 5	



dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_C6	
LAYER BOTTOM SIDE TRACK	



dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_TA	
LAYER TOP ASSEMBLY DRAWING	



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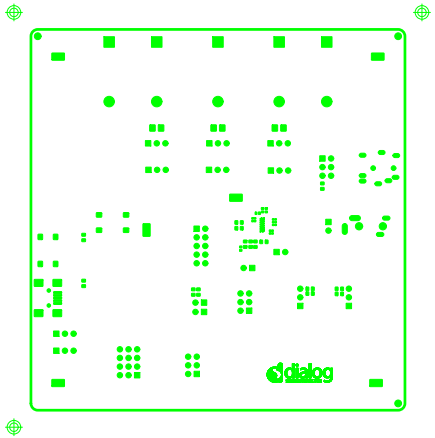
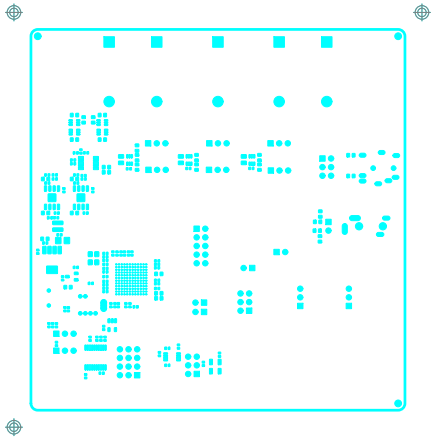
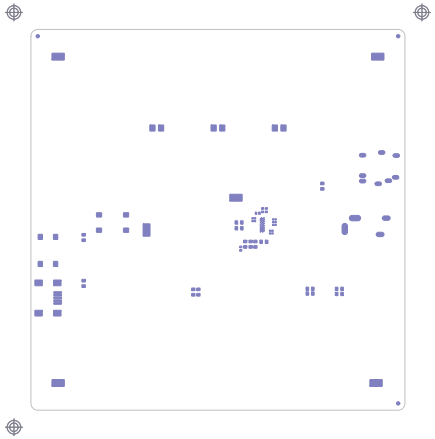
DRAWING NUMBER 284-02-C_BA	
LAYER BOTTOM ASSEMBLY DRAWING	



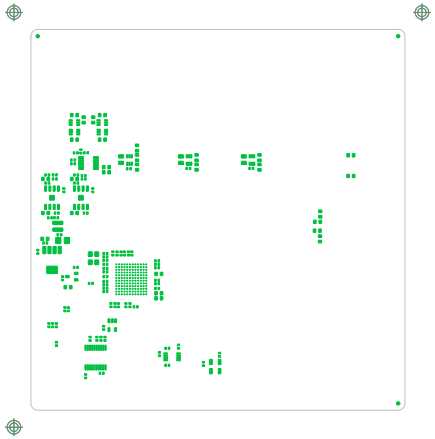
PROJECT
Cadie Performance Board
DRAWING NUMBER 284-02-C_TR
LAYER TOP SOLDER RESIST



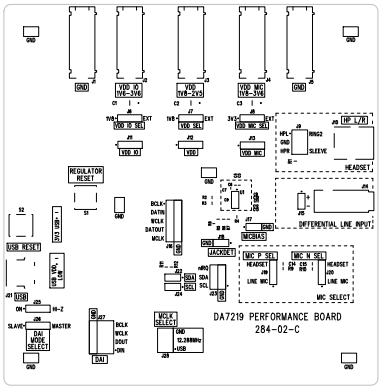
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_BR	
LAYER BOTTOM SOLDER RESIST	



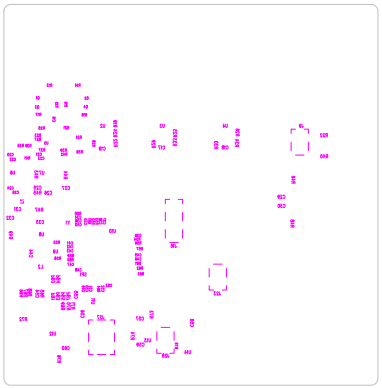
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_TP	
LAYER TOP SOLDER PASTE	



dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_BP	
LAYER BOTTOM SOLDER PASTE	

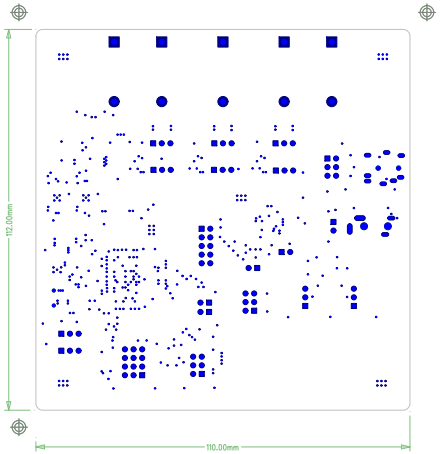


dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_TS	
LAYER TOP SILKSCREEN	



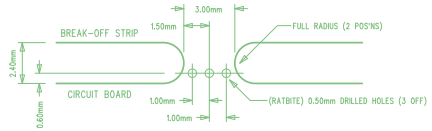
dialog SEMICONDUCTOR	PROJECT Cadie Performance Board
DRAWING NUMBER 284-02-C_BS	
LAYER BOTTOM SILKSCREEN	

IF IN DOUBT ASK!

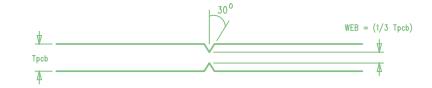


PREFERRED PANELISATION REQUIREMENTS	
REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW	
PRINTED CIRCUIT BOARDS THAT REQUIRE PANELISATION	
01	ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES
02	ANY 'ODD' SHAPE PCB e.g. ROUND
PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING	
01	ASSEMBLY PANEL TO BE A 2X1, 2UP ARRAY
02	PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES
03	BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm
04	MAXIMUM PANEL SIZE NOT TO EXCEED 380mm X 440mm
TOOLING HOLES	
01	ADD 3 TOOLING HOLES 2.5mm +/-0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE
FIDUCIALS	
01	ADD 3 FIDUCIALS ON BOTH SIDES (1mm DIA./2mm DIA. CLEARANCE) 5mm FROM PANEL EDGE
BREAKOUTS (FOR REFERENCE SEE ROUTING DETAIL BELOW)	
01	ADD BREAKOUTS IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS, GROUND PLANES, VITAL SILKSCREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.
02	USE LOCATIONS SHOWN BY '++' IF PRESENT
03	AT LEAST TWO BREAKOUTS MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF GREATER THAN 75MM IN LENGTH
04	AT LEAST ONE BREAKOUT MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF LESS THAN 75MM IN LENGTH
05	THE SPACING BETWEEN BREAKOUTS SHOULD BE BETWEEN 40mm TO 50mm
06	BREAKOUTS TO BE POSITIONED AT LEAST 12MM FROM CIRCUIT CORNER TO ALLOW CUTOUT ACCESS
07	STEPPED GERBERS MUST BE SENT TO THE PCD DESIGNER FOR VERIFICATION BEFORE MANUFACTURE COMMENCES
08	IF ANY OF THIS SECTION CANNOT BE ADHERED TO THEN PLEASE CONSULT THE PCB DESIGNER

PREFERRED ROUTING / V-SCORING REQUIREMENTS	
ROUTING	REQUIRED
01	USE A 2.40mm (+/-0.1mm) ROUT



V-SCORING	NOT REQUIRED
WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE THE FOLLOWING RULES ARE TO BE APPLIED	
01	SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)
02	COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)
03	SCORE ANGLE = 30 deg
04	REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS



NOTES		
01	BOARD TO BE MANUFACTURED TO IPC-A-600 CLASS 2	
02	BOARD IS TO MEET UL94V0 APPROVAL	
03	ALL BOARD'S MUST BE 100% TESTED FOR ELECTRICAL CONTINUITY AND ISOLATION	
04	NO REPAIRS MAY BE PERFORMED ON ANY IMPEDANCE CRITICAL TRACKS (WHERE APPLICABLE)	
05	ALIGNMENT OF ALL LAYERS TO BE SUCH THAT NO BREAKOUT OCCURS	
06	SUPPLIER'S UL IDENTIFICATION MARK, FLAMMABILITY RATING AND DATECODE MUST BE APPLIED TO THE BOARD - BOTTOM SIDE ONLY	
07	VARIATION IN TRACK WIDTH AND GAP TO MEET IMPEDANCE REQUIREMENTS ARE PERMISSABLE, SO LONG AS THESE ARE MINIMAL, AND THE OVERALL BOARD THICKNESS IS NOT COMPROMISED.	
08	MATERIAL TO BE RoHS COMPLIANT FR4, SUITABLE FOR LEAD-FREE PROCESSING	
09	BOW AND TWIST TO BE NO GREATER THAN 0.75% ACROSS DIAGONALS	
10	NON-FUNCTIONAL PADS MAY BE REMOVED FROM INTERNAL LAYERS (WHERE APPLICABLE)	
11	ALL STUBS MAY BE REMOVED	
12	REMOVE SILKSCREEN FROM EXPOSED COPPER (WHERE APPLICABLE)	
13	CHECK BUILD ORDER AGAINST PLOTS	
14	ALL DIMENSIONS IN mm (UNLESS STATED)	
15	FINISHED BOARD THICKNESS	1.60mm +/-10%
16	SURFACE FINISH	ELECTROLESS NICKEL/IMMERSION GOLD
17	SOLDER RESIST	BLACK GLOSS PHOTO-IMAGABLE
18	SILKSCREEN COLOUR	WHITE
19	MINIMUM TRACK WIDTH	0.100mm
20	MINIMUM GAP	0.160mm
21	MINIMUM P.T.H. PAD SIZE	0.450mm
22	MINIMUM PITCH OF SURFACE MOUNT PADS	0.650mm
23	No. TOP SIDE SURFACE MOUNT PADS	116
24	No. BOTTOM SIDE SURFACE MOUNT PADS	502

ADDITIONAL NOTES

PCB LAYER	MANUFACTURING DETAIL	GERBER FILES
	TOP SILKSCREEN	284-02-C_TS.GER
	TOP RESIST	284-02-C_TR.GER
LAYER 1	TOP SIDE TRACK	284-02-C_C1.GER
LAYER 2	INNER LAYER 2	284-02-C_C2.GER
LAYER 3	INNER LAYER 3	284-02-C_C3.GER
LAYER 4	INNER LAYER 4	284-02-C_C4.GER
LAYER 5	INNER LAYER 5	284-02-C_C5.GER
LAYER 6	BOTTOM SIDE TRACK	284-02-C_C6.GER
	BOTTOM RESIST	284-02-C_BR.GER
	BOTTOM SILKSCREEN	284-02-C_BS.GER
	CNC DRILL FILE (PLATED/NON-PLATED THROUGH HOLE)	284-02-C.DRT
	CNC DRILL TOOLING (PLATED/NON-PLATED THR'H HOLE)	284-02-C.REP
	MANUFACTURE DETAIL	284-02-C_MC.GER

LAYER/ LAYER TYPE	BOARD STACK	COPPER WEIGHT
01 MIXED		305g/m
02 GROUND		152g/m
03 POWER		152g/m
04 MIXED		152g/m
05 GROUND		152g/m
06 MIXED		305g/m

dialog SEMICONDUCTOR

PROJECT: Cadie Performance Board

DRAWING NUMBER 284-02-C_MC

LAYER MANUFACTURE DETAIL

DRILL DETAIL NOTES	
ALL PLATED HOLES ARE FINISHED SIZES WITH +/-0.075mm TOLERANCE	
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH +/-0.050mm TOLERANCE	
ALL VIAS ARE DRILLED SIZES WITH +0/-DRILL TOLERANCE	
TOTAL PLATED HOLE QTY	505
TOTAL NON-PLATED HOLE QTY	6

Pb Free

COMPANY CONFIDENTIAL

TOLERANCES UNLESS OTHERWISE STATED
0 PLACE DECIMALS +/- 1
1 PLACE DECIMALS +/- 0.5
2 PLACE DECIMALS +/- 0.1

DRAWN BY	DATE
BL	13/10/2015
CHK'D BY	DATE
CM	13/10/2015

DIALOG SEMICONDUCTOR UK LTD
2 MULTREES WALK
EDINBURGH
EH1 3DQ

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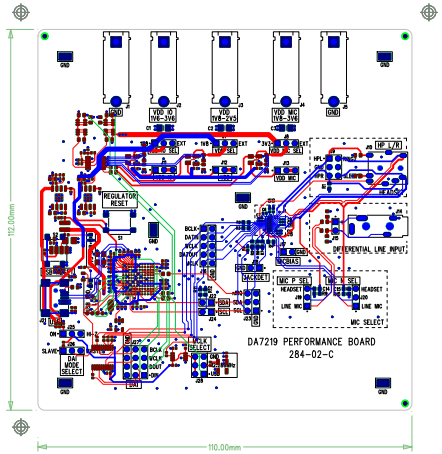
TITLE MANUFACTURE DETAIL
DA7218 Cadie Performance Board

DRAWING NUMBER
284-02-C

IF IN DOUBT ASK!



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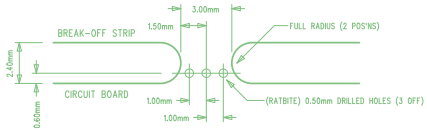

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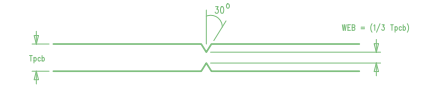

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TOTAL NON-PLATED HOLE QTY	6

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PROJECT: Cadie Performance Board

DRAWING NUMBER 284-02-C_TS

LAYER TOP SILKSCREEN DETAIL

Pb Free

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TOLERANCES UNLESS OTHERWISE STATED
0 PLACE DECIMALS +/- 1
1 PLACE DECIMALS +/- 0.5
2 PLACE DECIMALS +/- 0.1

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BL	13/10/2015
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2 MULTREES WALK
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