VID Interfacing for AMD K-8 Processors

Technical Brief | March 2004 | TB433.1

Author: Ross Staffhorst

Introduction

This paper describes inexpensive and effective techniques for interfacing AMD K-8 processor VID pins with various Intersil Pulse Width Modulated (PWM) controllers [1- 4] with integrated ESD protection.

Typically I/O pins include some form of integrated ESD protection, and the topology of the structure varies depending on a number of factors. One typical implementation is a diode pair that steers the ESD current pulse either to the positive (VCC) or negative (GND) supply. The Intersil AMD K-8 families of PWM controllers all feature this type of ESD protection (Figure 1).

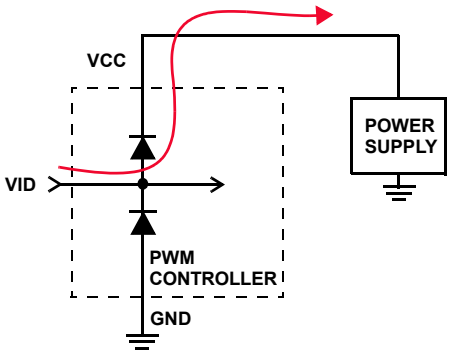

FIGURE 1. DUAL DIODE ESD PROTECTION ARRAY WITHIN CONTROLLER

Motherboard power sequencing during microprocessor state transitions requires careful coordination of a number of rails. It is important to consider all issues associated with back biasing and forward biasing components that are connected between two or more rails to address potential pitfalls.

If VCC is removed from the PWM controller during a sleep state and any combination of VID pins is still energized, a current path is formed by the forward biased ESD protection device as shown in Figure 1. Depending on the impedance looking into the supply rail, the resulting current draw could exceed recommended current density levels or operational temperature for the ESD protection devices or the processor VID pins.

Intersil does not recommend forward biasing ESD protection diodes on the PWM controllers. Systems which retain active VID inputs to the PWM controller after VCC power has been removed result in forward biased VID input protection diodes. Intersil has evaluated the reliability impact to such systems and found the risk to be minimal. Despite the minimal risk, designers should employ one of the four techniques described in this brief to avoid ESD diode current in future platform designs.

Design Considerations

The simplest solution is to never remove the supply rail to the power management IC as the processor advances through sleep states. The enable pin of the PWM controller allows for a safe and controlled shutdown of the converter to conserve power and is intended for this purpose.

Typically, motherboards are powered from an ATX style power supply which features a standby voltage (5VSB) output and a power good signal (PWR_OK). Intersil recommends using 5VSB to keep the PWM controller IC biased during the power-down state of other power rails.

The enable input of the controller can be controlled by the PWR_OK signal of the ATX power supply. Entering a lower power state, the PWR_OK signal transitions low indicating the removal of the +12VDC, +5VDC, and +3.3VDC rails. The enable input of the PWM controller is pulled low commanding the PWM controller to shutdown in a controlled manner. Wake-up begins when PWR_OK is asserted high by the power supply to indicate that the rails are above their undervoltage thresholds.

In cases where standby voltage is not available, external blocking or limiting of the reverse current path can be achieved in one of three ways.

A PNP transistor between the VCC pin of the controller and the supply rail, as shown in Figure 2, limits current flow in the reverse direction. A low reverse-current-gain transistor must be selected. The low voltage drop across the transistor must be taken into account when dealing with the controller POR threshold.

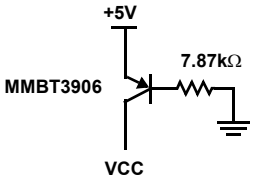

FIGURE 2. PNP PASS ELEMENT

If a +12V supply is available, the ISL6559 and ISL6569 controllers allow use of a blocking diode in series with a current limiting resistor in the VCC path. The voltage drop across the diode must be taken into account when dealing with the controller POR threshold.

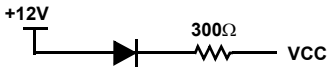

FIGURE 3. BLOCKING DIODE FROM +12V POWER SUPPLY

A series resistor added in each VID trace limits the reverse current magnitude to a level that the ESD protection diode can sustain.

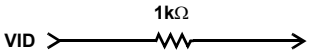

FIGURE 4. VID SERIES RESISTORS

Summary

Four techniques have been presented that meet the technical requirements for interfacing Intersil PWM controllers to AMD K-8 processor VID pins. Based on the availability of an ATX power supply, one of these solutions provides the most cost effective means of interfacing. All future design activity should employ one of these methods.

References

For Intersil documents available on the internet, see our web site at http://www.intersil.com/

[1] ISL6559 Data Sheet, Intersil Corporation, File No. FN9084

[2] ISL6569 Data Sheet, Intersil Corporation, File No. FN9805

[3] ISL6569A Data Sheet, Intersil Corporation, File No. FN9092

[4] ISL6244 Data Sheet, Intersil Corporation, File No. FN9106